UNIVERSITY OF CALIFORNIA SAN DIEGO

Design of Wideband Millimeter-Wave Beamformers and Transceivers in Advanced CMOS SOI Technology

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2020

The dissertation of Li Gao is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2020

DEDICATION

To my family

EPIGRAPH

Man proposes, God disposes.

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ACKNOWLEDGEMENTS

First of all, I would like to express my sincerest and deepest gratitude to my supervisor Professor Gabriel M. Rebeiz for his guidance, support and encouragement. He provided me with the precious opportunity to do research in his group and let me enter the new RFIC world. Throughout the past five years, his consistent encouragement and heartfelt suggestions vitalized my persistence on the way of research. I am also thankful to Prof. Gabriel M. Rebeiz allowing me to attend conferences all over the country, expanding my knowledge of this profession and inspiring me to be exposed to many people from academia and industry and their technical experiences.

I also would like to thank my dissertation committee members, Prof. Drew Hall, Prof. Patric Mercier, Prof. Gert Cauwenberghs and Prof. William Hodgkissfor their time, interest, and valuable comments.

Besides, I must thank current TICS group members Qian Ma, Hyunchul Chung, Yaochen Wang, Abdurrahman Alijuhani, Omar Elaasar, Ahmed Nafe, Tom Phelps, Yusheng Yin, Siwei Li, Changtian Wang, Kevin Low, Zhe Zhang, Abdurrahman Alhamed and Sultan Alqarni for their technical interactions and friendship. I would also like to thank previous TICS group members, Mustafa Sayginer, Hasan Al-Rubaye, Kerim Kibaroglu, Eric Wagner, Umut Kodak, Bhaskar Rupakula and Mustafa Lokhandwala and for their help and support.

I also thank my friends in UCSD. I would not have been able to complete my studies without their encouragement, friendship, and support. My appreciation should go to Po-Han Wang, Haowei Jiang, Xiaoyang Wang, Da Ying, Xiahan Zhou, Jiannan Huang, Hui Wang, Lujiang Yan and Edwin Hsu, to name only a few.

I also would like to thank my supervisors when I was an intern in Mediatek San Jose. They provided an excellent platform for industry experience and guided me in product design. My appreciation should go to Dr. Osama Shanna, Mr. Eric Lu, Dr. Zhiming Deng and Dr. Kachun Kwok, to name only a few.

Most of all, I would like to express my sincere thanks to my family members: my parents, brother and sister for their unconditional love and support. My life and doctoral studies at UCSD would have not been ever started without their devotion.

Last and most important, I thank my beloved fiancee Qianfei Su. She accompanied me since I was an undergraduate student. Till now, it has passed ten years. During these ten years, she endured many hardships but she never gave up on me. She is the right person that I should spend all of my life to love.

dissertation author was the primary investigator and first author.

Chapter 5, in full, contains material that is currently being prepared for submission for publication as it may appear in: L. Gao and G. M. Rebeiz, "Design of 20-42 GHz IQ receiver in 22-nm CMOS SOI for 5G application," *IEEE Trans. Microw. Theory Techn.*, in preparation (to be submitted June 2020). The dissertation author was the primary investigator and first author.

Chapter 6, in full, is a reprint of the material as it appears in: L. Gao, E. Wagner, and G. M. Rebeiz, "Design of E- and W-band low-noise amplifiers in 22-nm CMOS FD-SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 1, pp. 132-143, Jan. 2020. and L. Gao, Q. Ma, and G. M. Rebeiz, "A 4.7 mW LNA with 4.2 dB NF and 12 dB gain using drain to gate feedback in 45nm CMOS RFSOI technology," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 280-283, Jun. 2018. The dissertation author was the primary investigator and first author.

Chapter 7, in full, is a reprint of the material as it appears in: L. Gao, Q. Ma, and G. M. Rebeiz, "A 1-17 GHz stacked distributed power amplifier with 19-21 dBm saturated output power in 45nm CMOS SOI technology," in *IEEE International Microwave Symposium (IMS)*, pp. 454-456, Jun. 2018. The dissertation author was the primary investigator and the first author.

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ABSTRACT OF THE DISSERTATION

Design of Wideband Millimeter-Wave Beamformers and Transceivers in Advanced CMOS SOI Technology

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2020

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With the development of wireless communications, high data rate is becoming essential since it not only augments the current wireless systems but also enables many emerging applications. In order to achieve multi-gigabit-per-second data rates, the fifth generation communication system (5G) is moving forward to the millimeter-wave band, such as 24-29 GHz and 37-42 GHz. Since the frequency is more than 10 times than the current communication protocols, the wavelength is 10 times smaller, which makes the transmission line effects more notable and increases the design complexity. Moreover, the path loss is much larger and therefore a higher output power or antenna EIRP (effective isotropic radiated power) is required to overcome this

loss. Previous millimeter-wave 5G research focused on narrow band, such as 28 GHz and 39 GHz. But if a single system can be wideband and include all of these bands, the simultaneous data rate can be increased and the system cost can be reduced. The research projects in this dissertation, in consequence, focus on different wideband RF ICs, and include power amplifiers (PA), low noise amplifiers (LNA), wideband phased-array receivers with high single-sideband rejection, wideband IQ receivers and wideband front-end circuits including phase-shifters and variable gain amplifiers. All of these circuits were done in advanced CMOS SOI technologies. The thesis concludes with a list of future work to be done in this area.

Chapter 1

Introduction

1.1   Background

Wireless communication system has been driving the connectivity speeds faster and faster. The global mobile data traffic continues to increase with a compound annual growth rate of 46%. In order to fulfill the high data-rate requirements, the fifth-generation (5G) communication has been proposed and is becoming a popular topic in the past several years. With the carrier frequency moving to the millimeter-wave band, the available bandwidth is much larger than 4G communication systems. Based on Shannon theorem, the communication channel capacity is proportional to the bandwidth and inverse proportional to signal to noise ratio (SNR). With a wider bandwidth, a higher date rate can be achieved. Compared with 4G data rate of hundreds of Mbps, the 5G data-rate can goes up to ten of Gbps, which can not only support traditional communication protocols but also allow for emerging applications, such as remote high definition video conferencing, autonomous vehicles and virtual reality.

Despite of the high data-rate advantages, there are also some obstacles. The first one arises from the transistor technology. With the frequency moving to the millimeter-wave band, the maximum available gain from the transistor decreases drastically. Also the parasitic effects

become more and more notable, which makes RFIC design harder. Fortunately, with the continuous scaling of CMOS technology, the f_t/f_{max} of the CMOS transistors have been driven to higher than 250 GHz, which makes the design of millimeter-wave circuits possible.

The second one is due to the frequency choice. The space path loss factor is proportional to frequency squared. For a 200 meter communication link, the signal attenuation is 86 dB for a 2.4 GHz signal while it is 107 dB for a 28 GHz signal. The exists of atmospheric absorption and mechanical resonance in gaseous molecules further attenuate the signal strength, and limits the wireless communication distance. Therefore, a high density of base stations is required and thus the total system cost is higher than previous 4G communication networks. In order to deal with this issue, large phased-arrays are proposed. With a N×N element phased-array system, the effective isotropic radiated power (EIRP) increases by 20log(N) when compared to a single-channel transmitter. Thus, the communication distance is increased. Also, due to the over-the-air power combining, a single channel does not need to provide a high output power, thus, mitigating thermal concerns and making possible the integration of Si-based power amplifiers (PAs).

The last one comes from the design experience. The wavelength at 30 GHz is 10 mm in the free space and it is even shorter when a substrate exists. Thus, the distributed effect is remarkable, and the designer needs to pay more attention. Moreover, the device model that is provided by the foundry may be inaccurate and results in non-optimal results at mm-wave frequencies. Furthermore, the 3-D electromagnetic simulation tools for passive and active devices must be carefully used to accurately mode the integrated circuit. All of the factors complicate the design and require a higher level of attention and expertise from the designer.

Still the demand for high-data rate communication systems is a strong driving factor of implementing fully integrated mm-wave circuits. Therefore, various research and development activities are in progress both in academia and industry at different frequency ranges in the mm-wave region.
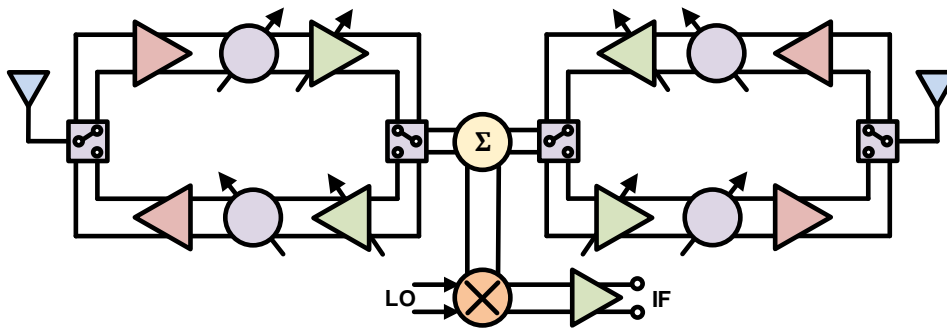
Figure 1.1: Block diagram of a beamformer phased array chip.

1.2   Motivation

We have fortunately witnessed the rapid development of wireless communications. And the development of RFIC also evolved into unimaginable complexity and integration. From a technology aspect, CMOS has undoubtedly been one of the most promising technologies due to its performance, low cost and the potential compatibility with baseband circuits, which is the trend for system-on-chip (SOC) solutions. In terms of circuit design, the operating frequency is moving higher and higher, the output power is becoming larger, the noise figure (NF) is becoming lower while the dc power consumption is required to remain approximately the same.

In terms of 5G millimeter-wave IC design, the Federal Communication Commission (FCC) has issued multiple frequency bands for 5G, such as 24-29 GHz and 37-42 GHz. However, most of the previous research focused on 28 GHz design in the past several years. Fig. 1.1 shows a popular phase-array beamformer and transceiver topology, which is widely used in the published literature. Various topology and design techniques are applied to optimize the performance of each block, in the 24-29 GHz band or in the 37-42 GHz band. If one handset needs to be compatible with two mm-wave bands, two sets of phase-array transceivers are needed, which greatly increases the area and cost. Therefore, if one design can include both bands and operate over a very wide bandwidth while maintaining similar performance, then the area and cost can be greatly reduced. The aim of this thesis is to pave the way for the design wideband

beamformers and transceivers for 5G millimeter-wave communication circuits.

1.3   Thesis Overview

This thesis presents fully integrated mm-wave circuits for high performance transceiver circuits and systems in advanced CMOS SOI technology.

Chapter 2 presents a 22-44 GHz phased-array beamformer in the GlobalFoundries (GF) 45-nm CMOS SOI. The channel includes a wideband single-ended to differential low-noise amplifier (LNA), a 5-bit vector modulator (VM) phase shifter with a measured rms error of < 6°, an attenuator and a variable gain amplifier (VGA) with 16 dB of gain control. The phased-array channel results in a peak gain of 26.3 dB and a 3-dB bandwidth of 20.5-44 GHz. The measured NF is 3-3.6 dB at 22-44 GHz with an IP1dB of -27.5 to -24.5 dBm, and a dc power consumption of 112 mW.

Chapter 3 presents a wideband millimeter-wave front end in 45 nm CMOS SOI for 5G applications. The front-end is composed of a low noise amplifier (LNA), power amplifier (PA) and a single-pole double-throw switch (SPDT). A double-tuned PA is used, and is based a two-stage stacked-amplifier with a reconfigurable load using SOI switches, so as to achieve an optimal load for both 5G frequencies. A wideband series-shunt switch is also developed with high power handling (P1dB > 23 dBm), and < 1 dB insertion loss at 20-40 GHz. In the receive mode, the front-end has a measured peak gain of 19.3 dB with a 3-dB bandwidth of 19.7-40 GHz, a noise figure (NF) < 4 dB at 18-40 GHz and an IP1dB of -19 to -16 dBm. In the transmit mode, and for low-band operation, the peak gain is 17.6 dB with a 3-dB bandwidth of 22.7-30.8 GHz. The Psat is > 18.8 dBm and the peak PAE is 18% at 24-30 GHz, and include the switch loss and compression. For high-band operation, the gain at 36-40 GHz is 13.6±1.5 dB with Psat > 18 dBm. To the author's knowledge, this is the first front-end that covers both the 24-28 GHz and 37-40 GHz 5G bands with high output power and low noise figure. Application areas are in

multi-standard base-stations and small-cells.

Chapter 4 presents presents a 20-44 GHz image-rejection receiver in 22-nm CMOS FD-SOI. The receiver includes a wideband LNA with a 3-pole high-pass rejection filter coupled to a double-balanced mixer with a wideband LO driver and an IF amplifier. At an intermediate frequency (IF) of 16 GHz, the image band at DC-12 GHz is filtered by the LNA response and is greater than 75 dB over the entire 20-44 GHz range. The receiver results in a gain of 24-28.5 dB and a NF of 3.3-5 dB at 20-44 GHz and achieves a EVM of 3.6-3.7% at the carrier frequency of 28 GHz and 39 GHz with 2 Gbaud symbol rate at 64QAM waveform.

Chapter 5 presents a 20-42 GHz IQ receiver in 22-nm CMOS FD-SOI. The receiver includes a wideband low noise variable gain amplifier (LNVGA), double-balance IQ mixers, a wideband IQ generation network and wideband LO driver, lowpass filters and IF amplifiers. The measured receiver has a peak conversion gain of 22.3 dB with 3-dB bandwidth of 19.8-42 GHz, which covers the whole 5G millimeter-wave band. The measured single sideband NF is 5.2-7 dB and IP1dB is -26 to -23 dBm. The conversion gain can be adjusted by 8 dB and the IP1dB is improved by 5 dB and NF just degrades by 1.2 dB. The gain mismatch between I and Q channel is smaller than 0.6 dB at 20 to 42 GHz. The phase mismatch is smaller than 5°at 28-42 GHz.

Chapter 6 first presents *E*- and *W*-band low noise amplifiers (LNA) in GlobalFoundries 22-nm CMOS FD-SOI (fully depleted silicon-on-insulator). Both amplifiers employ a three-stage cascode design with gain-boosting transformer loads. Design procedures are presented for E- and W-band LNAs for narrowband and wideband applications. The *E*-band LNA focuses on a high-gain, low-power implementation, and results in a gain and noise figure (NF) of 20 dB and 4.6 dB at 77 GHz with a 3-dB bandwidth of 12 GHz, and an input P1dB of -27.4 dBm, for a power consumption of 9 mW. The *W*-band LNA focuses on wideband applications, and results in a peak gain of 18.2 dB with a 3-dB bandwidth of 31 GHz, for a power consumption of 16 mW. The LNAs have a high figure-of-merit (FoM) and show very low power operation in the 70-100 GHz range. After the LNAs in GF 22-nm SOI, another *W*-band LNA with low power

consumption in GF 45-nm CMOS SOI is presented. The LNA has a measured gain is > 10 dB at 80-95 GHz with a peak of 12 dB at 90 GHz. The measured noise figure (NF) is < 4.9 dB at 85-95 GHz with minimum of 4.2 dB at 90 GHz. This is achieved with a total power consumption of 4.7 mW.

Chapter 7 presents a uniform distributed amplifier (DA) based on 45nm CMOS SOI. Four stacked transistors are employed in a single arm to construct a four-stage DA. The wideband distributed amplifier results in a measured maximum gain of 17.1 dB with a 3-dB small-signal bandwidth of 1-17 GHz. The saturated output power is 19 - 21 dBm at 1-17 GHz, with a peak power-added efficiency (PAE) is 12.2-19%. The DA consumes 97 mA from a 4.4 V supply.

Chapter 8 summarizes this dissertation and discusses future works.

Chapter 2

A 22-44 GHz Phased-Array Receive Beamformer in 45-nm CMOS SOI for 5G Applications with 3-3.6 dB NF

2.1 Introduction

Millimeter-wave 5G phased-arrays is an active area of development and results in communication links with increased date-rate between the base-station and the user. Phased-arrays with high antenna gain and high effective isotropic radiated power (EIRP) are commonly used, both at the base-station and the customer premise equipment (CPE) cites to combat the high path loss at millimeter-waves and increased atmospheric attenuation. The 24-29 GHz and 37-43 GHz bands are now approved worldwide as the standard 5G communication bands, and several 5G systems have been presented in the 28 GHz and 39 GHz bands [1–12].

Phased-array design is now based on the all-RF architecture at the antenna level, where gain and phase control on each channel is done in the RF domain (Fig. 2.1). In order to grow the array to a large number of antenna elements, the beamformer chips have an all-RF design
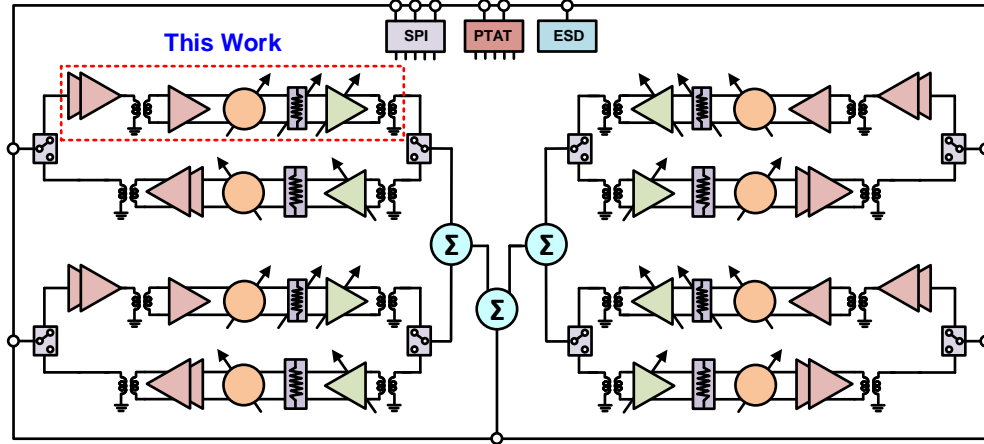
Figure 2.1: Block diagram of a wideband 2×2 beamformer chip.

(RF-in/RF-out, 2x2 quad-core, or 8 or 16-elements on the same chip) and a millimeter-wave Wilkinson network is used on the printed-circuit board (PCB) to add the signals from the antennas. A single transceiver and a high-Q filter are then placed at the sum point for up/down-conversion and to filter out the mixer harmonics (TX mode) and interferers (RX mode). In [1–12], various RF beamformers and phased-arrays have been demonstrated, but they are usually narrowband, centered either at 28 GHz or at 39 GHz.

In this chapter, a wideband phased-array beamformer receive channel is proposed and covers the entire 5G millimeter-wave band (22-44 GHz) (Fig. 2.1). There are several challenges to wideband phased-arrays: 1) wideband antenna and array design, 2) wideband and efficient transmit channel with a low-loss Tx/Rx switch, 3) wideband receive channel with low noise and high linearity, and 4) a wideband transceiver with filtering of spurious harmonics. The goal is to eliminate the need of building two phased-arrays, one at 24-29 GHz and one at 37-42 GHz, which results in increased area and cost.

The phased-array receive channel results in a peak gain of 26.3 dB and a 3-dB bandwidth of 20.5-44 GHz. The measured NF is 3-3.6 dB at 22-44 GHz with an IP1dB of -27.5 to -24.5 dBm, and a dc power consumption of 112 mW. This is the first wideband phased-array beamformer which covers the entire millimeter-wave 5G band.

2.2 Block Design

Fig. 2.1 presents the block diagram of a wideband 2x2 beamformer chip. This work focuses on the receive beamformer channel, and is well known, the wideband phase shifter and VGA can also be re-used in the transmit channel.

The GlobalFoundries 45-nm RF-SOI process is used and provides 7 layers of copper and one aluminum top-layer [13]. In this technology, the SOI transistors are built in a buried oxide layer that isolates the active device from the 2.5 kΩ-cm resistivity substrate. The high resistivity also results in an inductor Q is at 20-25 at 30 GHz, one of the highest in any process. A floating-body transistor is used with a measured f_t/f_{max} of 250/310 GHz, including all connections to the top metal, at a current density of 0.4-0.5 mA/μm [14]. The current density (J) for lowest NF_{min} is 0.1-0.2 mA/μm.

2.2.1 Wideband Input and Output Matching Network

A common-source amplifier is used at the wideband beamformer input for low-noise performance, and in order to realize wideband matching and avoid NF degradation, a two-pole matching is employed. The first solution is shown in Fig. 2.2a, where $R_L=g_m L_s/C_{gs}$ and C_2 is the series effect of L_s and C_{gs}, and results in a shunt-series resonant matching network. For example, a transistor with g_m=40 ms, L_s=70 pH and C_{gs}=80 fF results in R_L=35 Ω. Assuming that k=0 for simplified analysis, and L_1/C_1 and L_2/C_2 having resonant frequencies of f_1 and f_2, respectively (note that, in general, $f_2 < f_1$). When $f < f_2$, the circuit is shown in Fig. 2.2b where L_1/C_1 is now equivalent to L_{eq1} and L_2/C_2 is equivalent to C_{eq2}, and this network can transform R_L (<50 Ω) to R_s (50 Ω). When $f_2 < f < f_1$, the circuit cannot transform R_L to R_s perfectly and results in degraded matching (Fig. 2.2c). When $f > f_1$, the circuit can transform R_L to R_s again (Fig. 2.2d). Therefore, this circuit realizes a wideband two-pole matching network, and solutions with k_0 can be used to tune the two inductor values.

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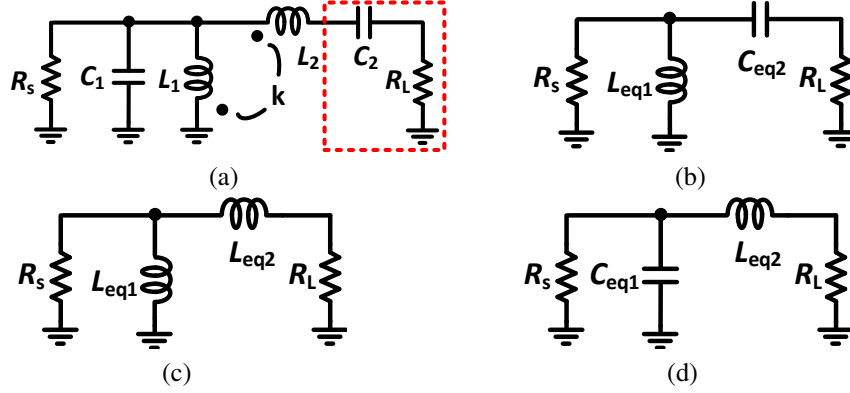
Figure 2.2: (a) Option 1 for a two-stage matching network; Equivalent circuit for (b) $f < f_2$, (c) $f_2 < f < f_1$, (d) $f > f_1$.

An alternative matching network is to use a two-stage transformer network with $R_{eq}=(Q^2+1)R_L$, $C_{eq}=Q^2C_2/(Q^2+1)$ and $Q=1/\omega C_2 R_L$, and where the first and second stages utilize parallel resonators (Fig. 2.3a-b). For one-pole matching, the lumped-element values are derived using:

$$L_1C_1 = L_2C_{eq} \tag{2.1}$$

$$L_1R_{eq} = L_2R_s \tag{2.2}$$

$$k_0 = \frac{L_1}{L_1+R_s^2C_1} \tag{2.3}$$

When $k > k_0$, the two poles are split apart, and the network becomes a two-pole matching network. It is well known that for wideband performance one must choose a large k, but note that the matching at mid-frequencies (between the two poles) deteriorates when the two poles are split far apart. Therefore, in theory, the performance of this circuit is similar to Fig. 2.2, but in practice, there are practical issues which render the circuit in Fig. 2.3 to be less desirable. For example, due to circuit constraints, $R_{eq} \gg R_s$ and therefore $L_1 \ll L_2$, making it hard to achieve a large transformer k. Also, for a given transformer, k changes considerably versus frequency from 20 to 45 GHz (from lower to higher values), and which results in less effective matching.

Fig. 2.3c presents the simulated results of these two matching networks, with C_1=94 fF, L_1=233 pH, L_2=195 pH and k=0 for Option 1, and C_1=132 fF, L_1=156 pF, L_2=350 pH and k=0.66
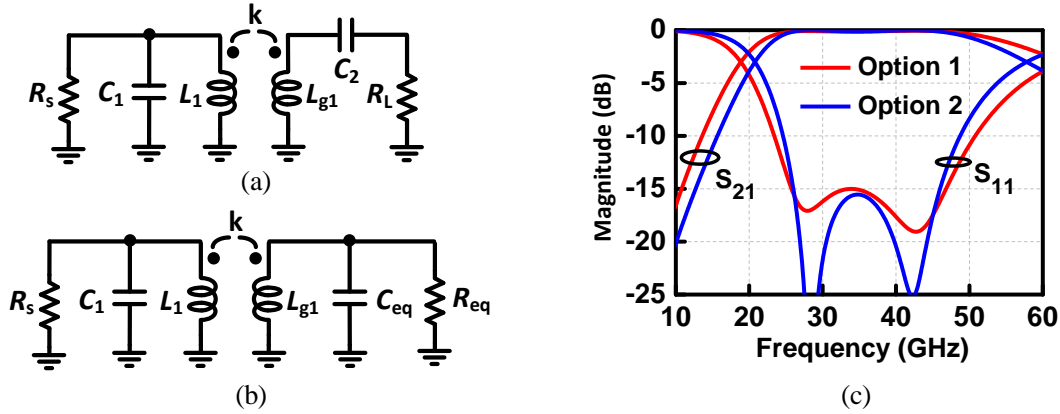
Figure 2.3: (a) Option 2 for a two-stage matching network; (b) Equivalent circuit; (c) Simulated results for Option 1 and Option 2.
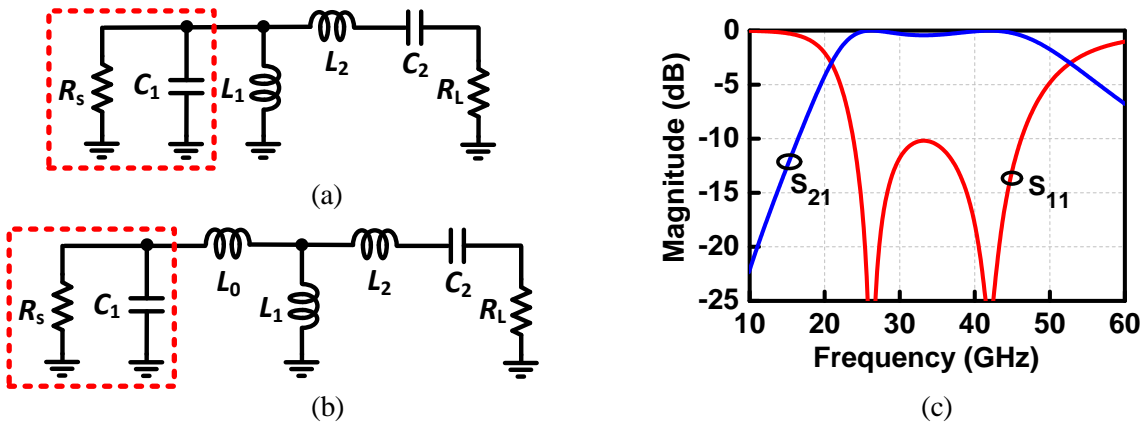
Figure 2.4: (a) Schematic of the output matching network; (b) Revised version; (c) Simulated results.

for Option 2. As shown above, both circuits realize similar performance. However, in Option 1, there is no limitation for L_1 and L_2, but in Option 2, L_2 is much larger than L_1 and k is chosen to be relatively large. Therefore, in this paper, Option 1 is adopted for wideband LNA input matching.

For wideband output matching, a two-stage matching network is also desired, and is similar to the input matching network (Fig. 2.4a). A typical CMOS amplifier has an output impedance composed of an RC parallel-load with $R_s \gg 50\ \Omega$, and therefore, a step-down impedance transformation is required. The same matching procedure can therefore be implemented, but since $R_s \gg 50\ \Omega$, a series inductor L_0 is inserted to reduce the real part (Fig. 2.4b). Fig. 2.4c presents the
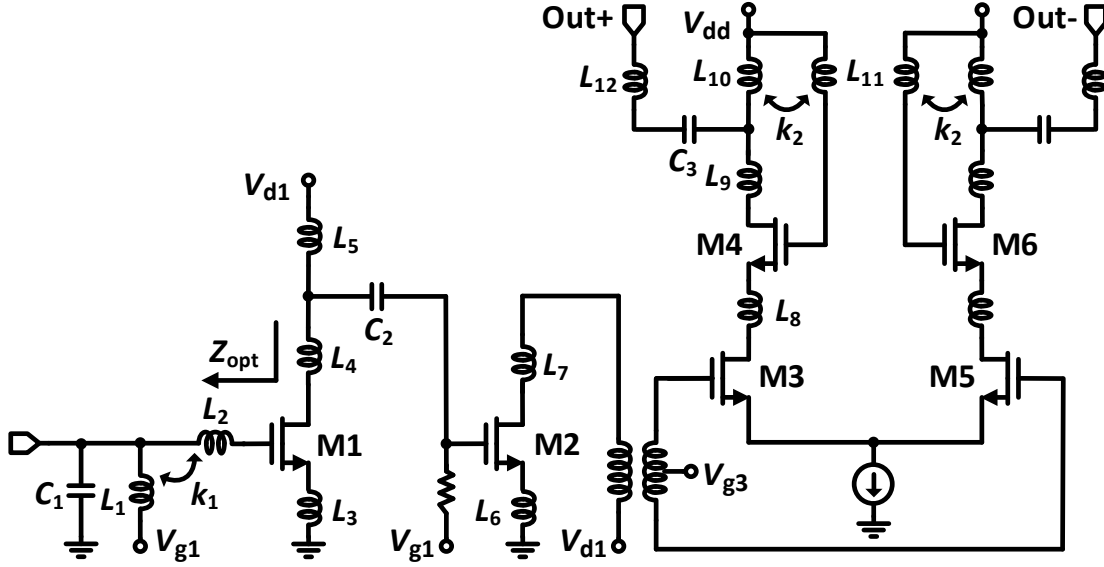
Figure 2.5: Schematic of the wideband single-end to differential LNA.

Table 2.1: LNA Component Values

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}
400 p	350 p	70 p	100 p	400 p	20 p	200 p	200 p	110 p	300 p	100 p
L_{12}	C_1	C_2	C_3	k_1	k_2	V_{g1}	V_{d1}	V_{g3}	V_{dd}	M1-6
300 p	75 f	250 f	88 f	-0.1	0.3	0.5 V	0.5 V	1 V	1.5 V	60 μm

simulated results for R_s=200 Ω, C_1=50 fF, and L_0=145 pH, L_1=320 pH, L_2=355 pH and C_2=50 fF. It can be observed that a wideband two-pole matching network is realized.

2.2.2 Wideband LNA

The wideband LNA is based on a two-stage common-source amplifier followed by a cascode amplifier. The single-ended signal is converted to a differential signal at the output of second stage using a passive transformer, as shown in Fig. 2.5. If the first and second stages are differential, then the power consumption will double and the NF will increase due to the use of a wideband balun at the input port. This design results in the lowest noise figure while still maintaining acceptance common-mode rejection which can create oscillations when the chip is packaged (due to ground inductance). The transistor sizes are all 60 μm and the NF_{min} at 20-40

12
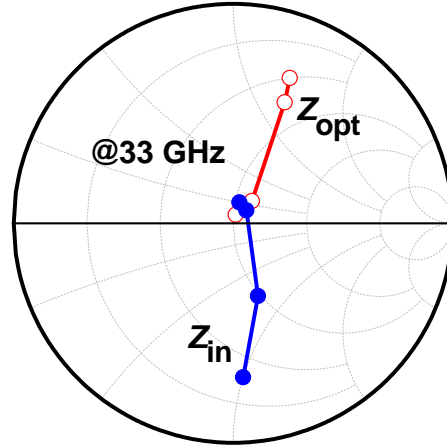
Figure 2.6: Simulated LNA input impedance matching and noise matching at 33 GHz.

GHz is 0.5-0.9 dB with a current density of 0.15-0.2 mA/μm.

The input matching is realized using Option 1, and Fig. 2.6 presents the details of noise matching and impedance matching procedures. A transistor size of 60 μm is chosen which results in Z_{in}=18-j50 Ω and Z_{opt}=25+j67 Ω at midband (f_0 = 33 GHz), where Z_{in} is the gate input impedance and Z_{opt} is the optimal impedance required for lowest noise. By adding a degeneration inductor L_3, Z_{in} and Z_{opt} are changed to 49-j37 Ω and 36+j62 Ω, respectively. Then, a series inductor at the gate, L_2, transforms Z_{in} and Z_{opt} to 56+j7 Ω and 58+j12 Ω, respectively, and impedance and noise matching are realized simultaneously. At 22 GHz, Z_{in} = 38-j7.3 Ω and Z_{opt} = 62-j19 Ω which is a little far from each other and degrades the LNA NF by 0.4 dB. This is a limitation of the two-pole input impedance network, which fulfills simultaneous noise and input-impedance matching at a relatively narrow frequency range. In this design, the simultaneous noise and impedance matching is optimized at higher frequencies since the LNA has intrinsically higher NF than at lower frequencies.

The bandwidth extension utilizes different techniques for each stage (Fig. 2.7). For the first stage, an *L-C-L* matching load is used, which peak 22 GHz and provides a wideband load impedance with the gain dropping slowly at 30-44 GHz. The second stage utilizes a single-to-differential balun, which behaves as a second-order filter, and provides two peaks at 30 and 51

13
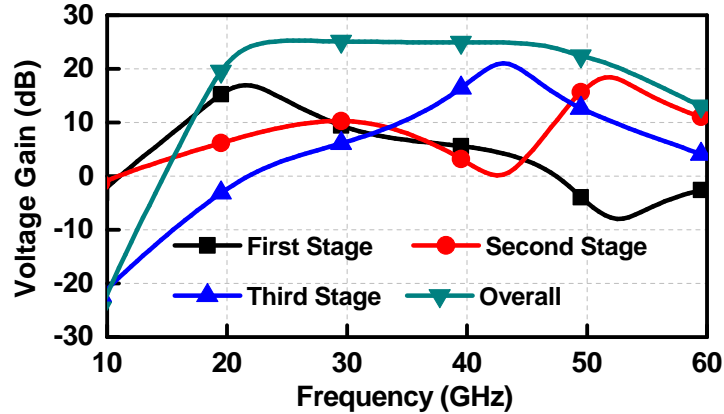
Figure 2.7: Simulated voltage gain of each stage in the LNA.

GHz. The third stage utilizes a cascode amplifier for higher gain and a transformer feedback load which broadens the bandwidth with a peak at 43 GHz [15]. A two-stage matching network at the third-stage drain node also provides a wideband output matching. Note that since the first stage peaks at 22 GHz, the effect of the subsequent stages on the system NF at 22 GHz is suppressed, and this is why stage two and stage three can be tuned to higher frequencies.

The simulated LNA has a peak gain of 22.2 dB with a 3-dB bandwidth of 20.5-49.7 GHz. Both S_{11} and S_{22} are < -10 dB at 23-47 GHz. The simulated NF is 2.5-3.8 dB and the IP1dB is -19±2 dBm at 20-50 GHz. The dc power consumption is 24.5 mW.

2.2.3 Wideband VGA and Switched Attenuator

Gain control is achieved using a switched 4-dB attenuator (for linearity) and a current-steering VGA. The 4 dB attenuator is built using a switched-resistor cell (Fig. 2.8a). When V_c is high, the attenuator is off and the equivalent circuit is shown in Fig. 2.8b, where C_3 and R_4 are C_{off} of transistor W_1 and R_{on} of transistor W_2, respectively. When V_c is low, the attenuator is on and the equivalent circuit is shown in Fig. 2.8c, where R_3 and C_4 are R_{on} of transistor W_1 and C_{off} of transistor W_2, respectively. The S_{21} of the on/off states can be derived as:
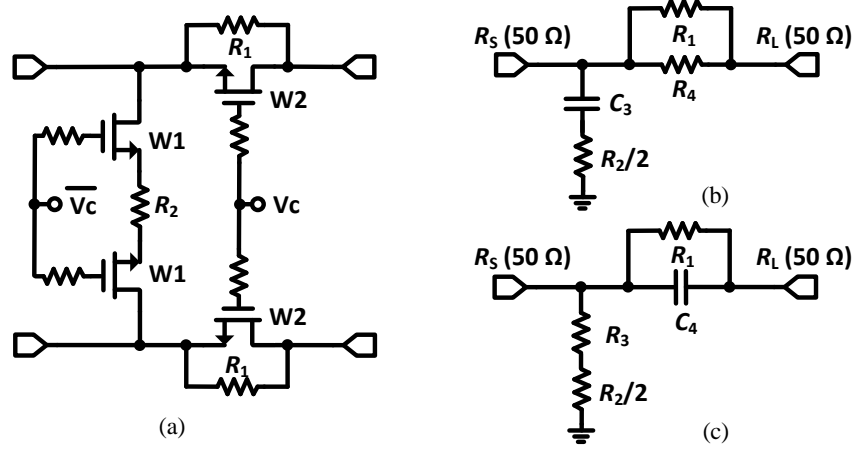
Figure 2.8: One-bit 4 dB attenuator (a) schematic; (b) attenuator off circuit; (c) attenuator on circuit.
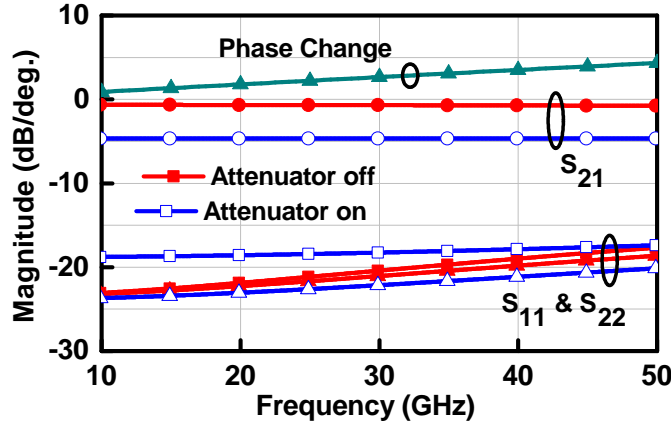
Figure 2.9: One-bit 4 dB attenuator simulated results.

$$S_{21\text{-off}} = (1 - S_{11\text{-off}}^2) \times \frac{1/sC_3 + R_2/2}{R_1||R_4 + R_L + 1/sC_3 + R_2/2} \times \frac{R_L}{R_1||R_4 + R_L} \qquad (2.4)$$

$$S_{21\text{-on}} = (1 - S_{11\text{-on}}^2) \times \frac{R_3 + R_2/2}{1/sC_4||R_1 + R_L + R_3 + R_2/2} \times \frac{R_L}{R_1||1/sC_4 + R_L} \qquad (2.5)$$

where $S_{11\text{-off}}$ and $S_{11\text{-on}}$ are the S_{11} for the off- and on-states. S_{11} and S_{22} are designed to be < -15 dB for minimal reflections in both states. Also, for the off-state, the insertion loss should be < 1 dB at 33 GHz. Based on these requirements, the design parameters are chosen as follows: W_1=15 μm, W_2=40 μm, R_1=25 Ω and R_2=125 Ω. Note that the 45RFSOI process results in $R_{on}C_{off} \sim$

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L_1	400 p	L_{10}	300 p
C_1	245 f	C_2	128 f
L_2	350 p	V_{g1}	1 V
k	-0.2	V_{g2}	1.5 V
L_3	120 p	V_{g3}	2 V
L_7	150 p	V_{dd}	2 V
L_9	400 p	M1-6	60 μ
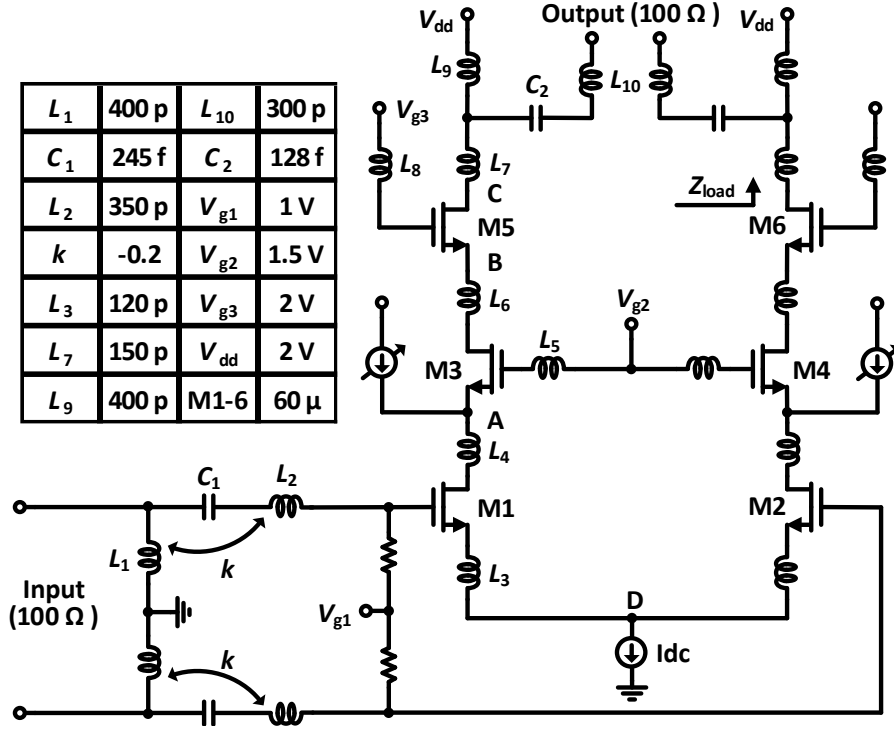
Figure 2.10: Schematic of the triple-stack wideband VGA core.

160-180 fs referenced to the top metal. The simulated attenuator is shown in Fig. 2.9 with S_{21}=0.65 (4.65) dB for the off- (on-) state with S_{11}, S_{22} <-15 dB. The phase change from the off- to on-state at 20-44 GHz is 1.8-3.8°.

The VGA employs a 3-stack amplifier design with source degeneration so as to create enough peaks and compensate for the pole roll-off at high frequencies (Fig. 2.10) [16]. The input matching is similar to the LNA, and this ensures easy connection to the LNA and the VM (vector modulator). There are three main poles in this stack, as seen on points A, B and C in Fig. 2.10. Pole C is compensated using a two-stage *LC* network, and the circuit is the same as Fig. 2.5 which generates a wideband high inductive impedance. Fig. 2.11a presents the differential impedance looking out of the drain of the upper transistors and two peaks can be observed. Poles B and A are compensated using series inductors (L_6 and L_4), which also resonate out the parasitic capacitance of 45 fF and boosts the gain. It also can be observed from Fig. 2.10, there are small gate inductors at M3 and M5, which help to boost the gain at high frequencies.
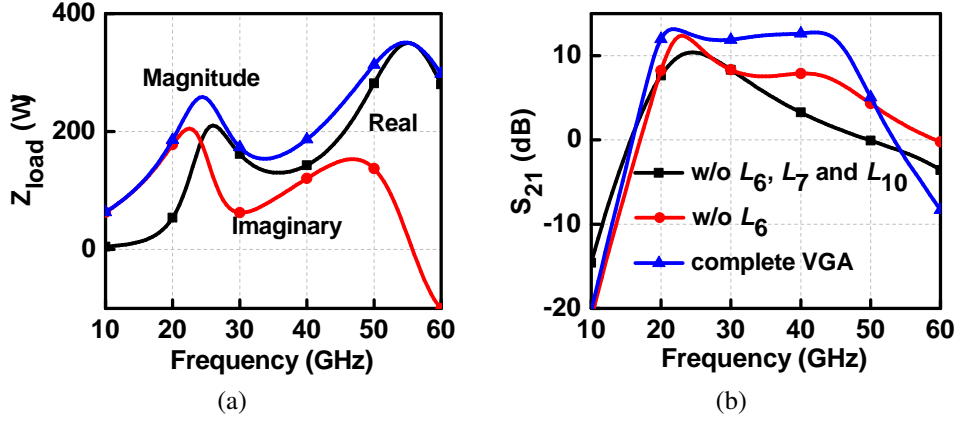
Figure 2.11: Wideband VGA: (a) simulated differential load impedance; (b) simulated gain for different conditions.

Fig. 2.11b presents the simulated gain response for different cases. When L_6, L_7 and L_{10} are removed, the load becomes a simple *LC* load and only one peak is observed. When L_7 and L_{10} are added, the gain still has one peak but exhibits a flat response at 30-43 GHz. When L_6 is added, the gain role-off is compensated and the single-stage VGA exhibits a flat response at 21-43 GHz.

A wideband balun is used at the beamformer channel output (after the VGA), and converts the differential signal to a single-end signal. The 45RFSOI process provides three thick metals, e.g. LD, OB and OA. The balun primary coil and secondary coil are implemented on OA and OB, respectively. In order to balance the amplitude and phase response, series and parallel capacitors are added in the first and second stage, respectively. The simulated balun loss is 1-2.4 dB at 22-44 GHz.

Fig. 2.12a presents the simulated VGA performance (with output balun). The simulated S_{21} has a peak gain of 11.7 dB with a 3-dB bandwidth of 19-47 GHz and a dc power consumption of 25 mW. The current steering gain tuning range is 12 dB with 0.8 dB steps. During gain tuning, the voltage of point D is nearly constant, the current source remains in saturation mode and does not limit the input linearity. The one-bit 4 dB attenuator provides another 4 dB tuning range with high linearity. S_{11} is < -10 dB at 23-58 GHz and S_{22} is < -9 dB at 20-50 GHz. The simulated NF is 3.2-5.3 dB at 20-45 GHz for the highest gain state. The simulated phase variation

17
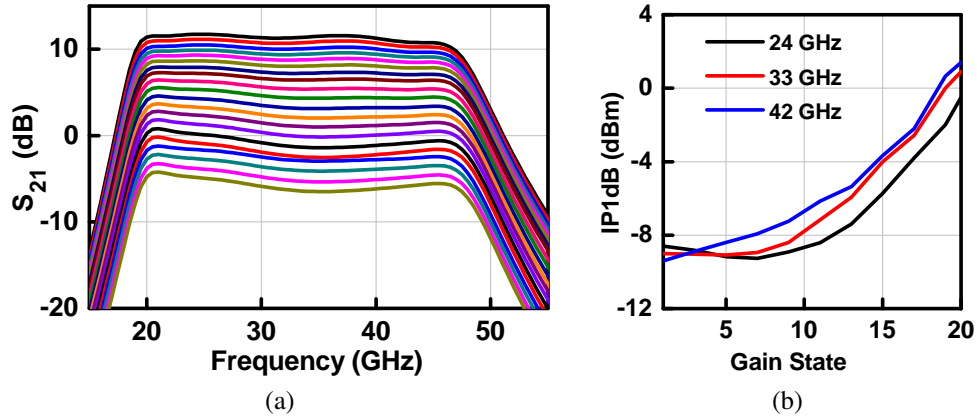
Figure 2.12: (a) Simulated VGA S_{21}; (b) Simulated VGA IP1dB versus gain state.

is 4-12°at 20-44 GHz with 16 dB gain tuning range. This can be improved in future designs using techniques described in [16]. Fig. 2.12b presents the simulated IP1dB versus gain state. The IP1dB is -8/-8.9/-9.4 dBm at 22/33/44 GHz for the maximum gain state, and increases when gain is reduced.

2.2.4   Wideband Vector Modulator

Fig. 2.13a presents the wideband vector modulator. A differential input signal is fed into an I/Q generation network, and by controlling the two VGA amplitudes, different phase shifts are realized. The relative phase shift is expressed by $\tan^{-1}(Q/I)$, and a gain control of 14.96 dB in each VGA results in a phase shift of 11.25°.

Generating a wideband I/Q signal at 20-50 GHz is not straightforward, and a wideband quadrature all-pass filter (QAF) network is used. This network has a better performance than the traditional 2-stage RC polyphase filter and is less susceptible to capacitance loading [17]. Also, it has much lower loss at the expense of using inductors and a larger size. Fig. 2.13b presents a modified QAF which includes three parts. The left side is a wideband matching network, the middle is a traditional QAF structure, and the right side is a compensation network used to reduce the phase and gain mismatch at 20-50 GHz. The input port is differential 100 Ω and the output

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(a)

(b)

(c)
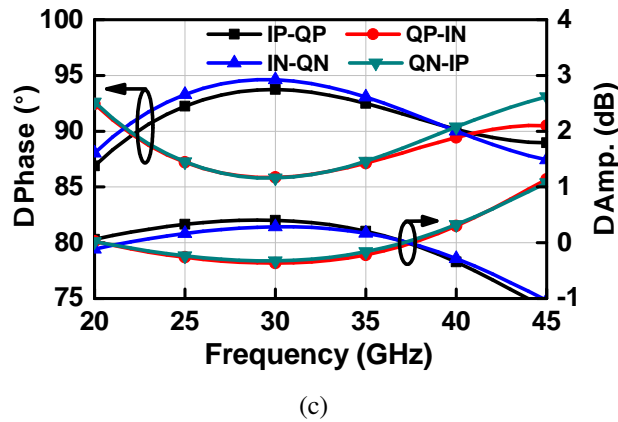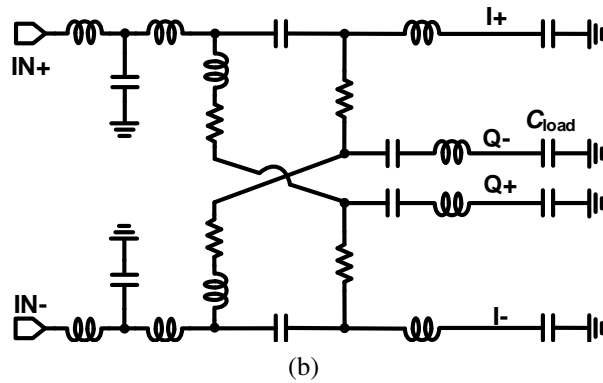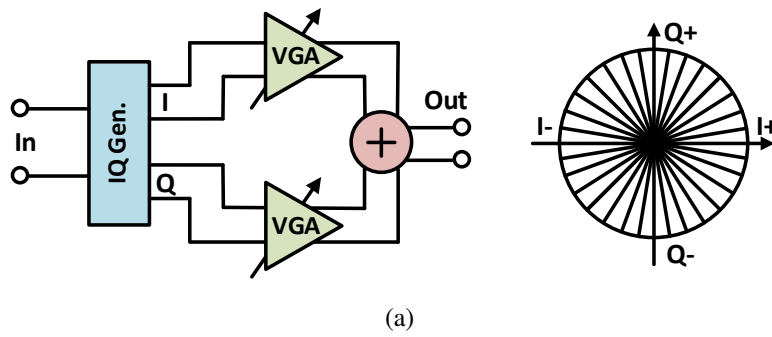
Figure 2.13: (a) Block diagram of the vector modulator and ideal 5-bit response; (b) wideband quadrature all-pass filter and its (c) simulated amplitude and phase mismatch.

is connected to the VGA transistor gates, which have an equivalent capacitance of 75 fF each. Note that by adding a 20 Ω series resistor in the QAF, the I/Q amplitude and phase sensitivity to the loading capacitance is reduced and the bandwidth can be extended [17]. Fig. 2.13c presents the simulated wideband QAF phase mismatch ($< 3°$) and amplitude mismatch (< 1 dB) at 20-45 GHz.
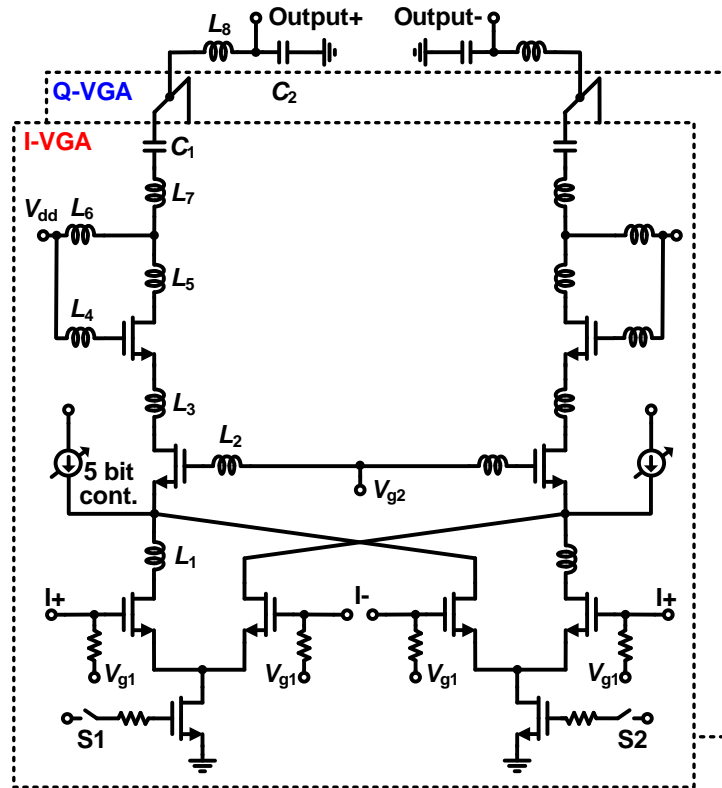
Figure 2.14: Schematic of wideband VM using triple stack amplifier.

After the differential I/Q signals are generated, the signals are fed to two 3-stack VGAs (Fig. 2.14). The VGA structure is the same as previously discussed but each VGA has 5 bits of gain control to cover the desired phase resolution. Four switches are used at the bottom (S1 and S2 for I control, S3 and S4 for Q control) and select the phase-shift quadrant.

The simulated VM peak gain is 0 dB with a 3-dB bandwidth of 19.5-47 GHz and a dc power of 62 mW when the phase shift is 45°. S_{11} and S_{22} are $<$ -10 dB at 18-57 GHz and 20.5-44 GHz, respectively. The simulated average NF is 14.3-15.5 dB with a variation less of ±1 dB over all phase states, and the average IP1dB is -1.9 to 1.5 dBm with variation of ±2 dB over all phase states at 20-45 GHz. A high IP1dB is desired as this phase shifter is placed after the LNA.
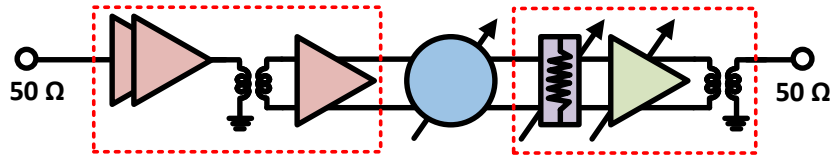
Channel	LNA	VM	VGA
Gain: 31 dB	Gain: 21 dB	Gain: -1 dB	Gain: 11 dB
NF: 3.35 dB	NF: 2.8 dB	NF: 15 dB	NF: 4 dB
IP1dB: -31.2 dBm	IP1dB: -20 dBm	IP1dB: -1 dBm	IP1dB: -9 dBm

Figure 2.15: Wideband beamformer channel: Gain, NF and linearity breakup.
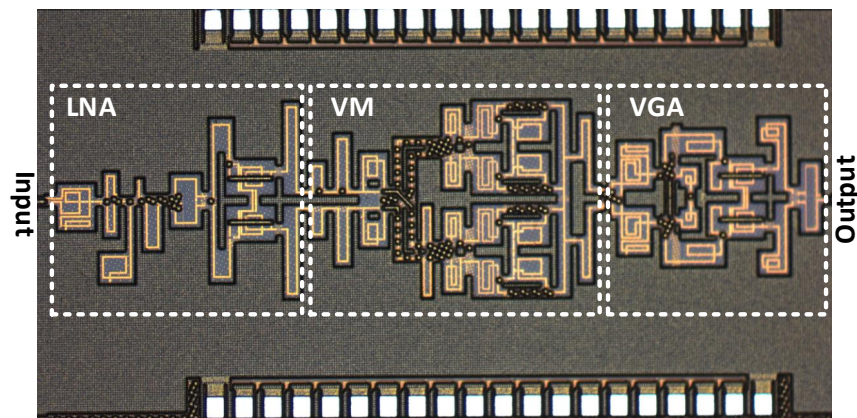
Figure 2.16: Fabricated photograph of the one channel (Core size: 2.7×0.7 mm^2).

2.2.5 Entire 20-44 GHz Beamforming Channel

The LNA, VM, VGA are then combined to make a wideband 20-44 GHz beamforming channel (Fig. 2.15). The calculated channel gain, NF and IP1dB are 31 dB, 3.35 dB and -31.2 dBm, respectively, at midband (33 GHz). The channel linearity is limited by the VGA OP1dB, and can be improved when the VGA gain is reduced. The channel consumes 112 mW and employs 3 different V_{dd} domains. The 0.5 V and 1.5 V supplies are used for the LNA due to the CS and cascode structures, and 2 V is used for the phase shifter and VGA due to the three-stack design. Since the LNA uses low current, one can employ an on-chip LDO (low dropout) regulator for the LNA block and the chip will then employ one power supply.
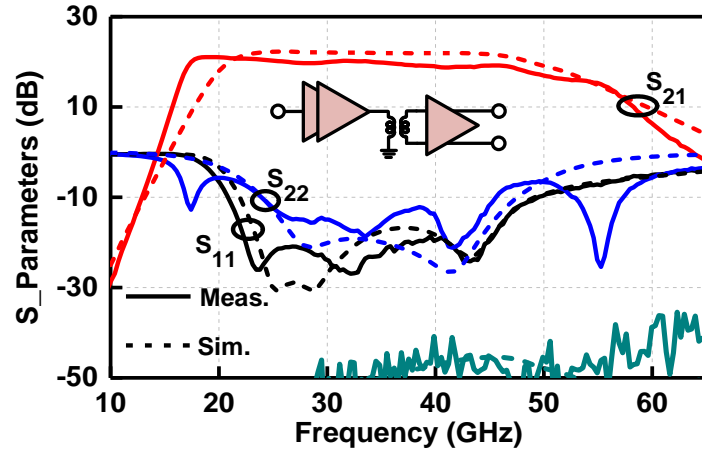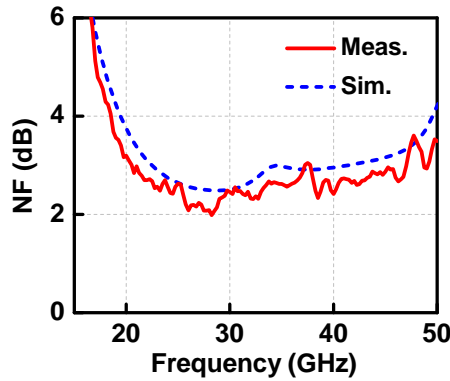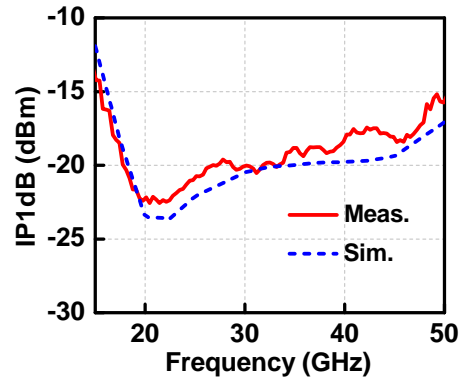
Figure 2.17: Measured and simulated LNA: (a) S-parameters; (b) NF; (c) IP1dB.

2.3 LNA, VM and VGA Block Measurement

Fig. 2.16 presents the beamformer channel with a size of 3 mm × 1.5 mm including pads. All measurements including NF and linearity were performed using on-chip probing with the Keysight N5247B network analyzer (PNA-X). For better characterization, each block is first measured and reported.

2.3.1 LNA

A wideband balun is added at the LNA output port for single-end measurements. Since the LNA has 20 dB gain, the output balun loss increases the NF by < 0.1 dB.

Table 2.2: Comparison with State-of-the-art Wideband LNA

Ref.	Tech.	BW (GHz)	Peak Gain (dB)	NF (dB)	P_{dc} (mW)	FoM
[19]	0.25-μm SiGe	25-34	26.4	2.1-3.5	134	1-7.1
[20]	65-nm CMOS	15.8-30.3	10.2	3.3-5.7	12.4	2.9-10.4
[21]	0.25-μm SiGe	29-37	28.5	3.1-4.1	80	4.6-8.1
[22]	45-nm CMOS SOI	24-44	20	4.2-5.5	58	2.6-6.5
[18]	22-nm CMOS SOI	24-43	23	3.1-3.7	20.5	19.7-21.9
This work	45-nm CMOS SOI	17-48	20.5	2-3.2	25	20.9-26.3

Fig. 2.17a presents the measured and simulated LNA S-parameters. The measured gain has a peak of 20.5 dB (output balun loss is de-embedded) with a 3-dB bandwidth of 17-48 GHz. The measured S_{11} is < -15 dB at 22.5-47.5 GHz. This near-perfect input matching makes it easy to integrate with a wideband Tx/Rx switch. The measured S_{22} is degraded because the output balun is not perfectly matched. The measured S_{12} is < -40 dB and the K-factor is > 1 (not shown).

Fig. 2.17b presents the measured and simulated LNA NF, and is done using the PNA-X which calibrates up to the probe tips. The measured NF is 2-3.2 dB at 20-45 GHz. Fig. 4.17c presents the measured and simulated LNA IP1dB with good agreement. The input P1dB is -22.5 to -17.5 dBm.

Table 2.2 compares the LNA with the state of the art wideband LNAs. It is observed that this work demonstrates the lowest NF and widest bandwidth and power consumption. It should also be mentioned that the dc power is slightly higher than [18]. That is because this design has a differential output stage, which consumes more power. Overall, this single LNA achieves the best figure-of-merit (FoM) in the 20-45 GHz range.
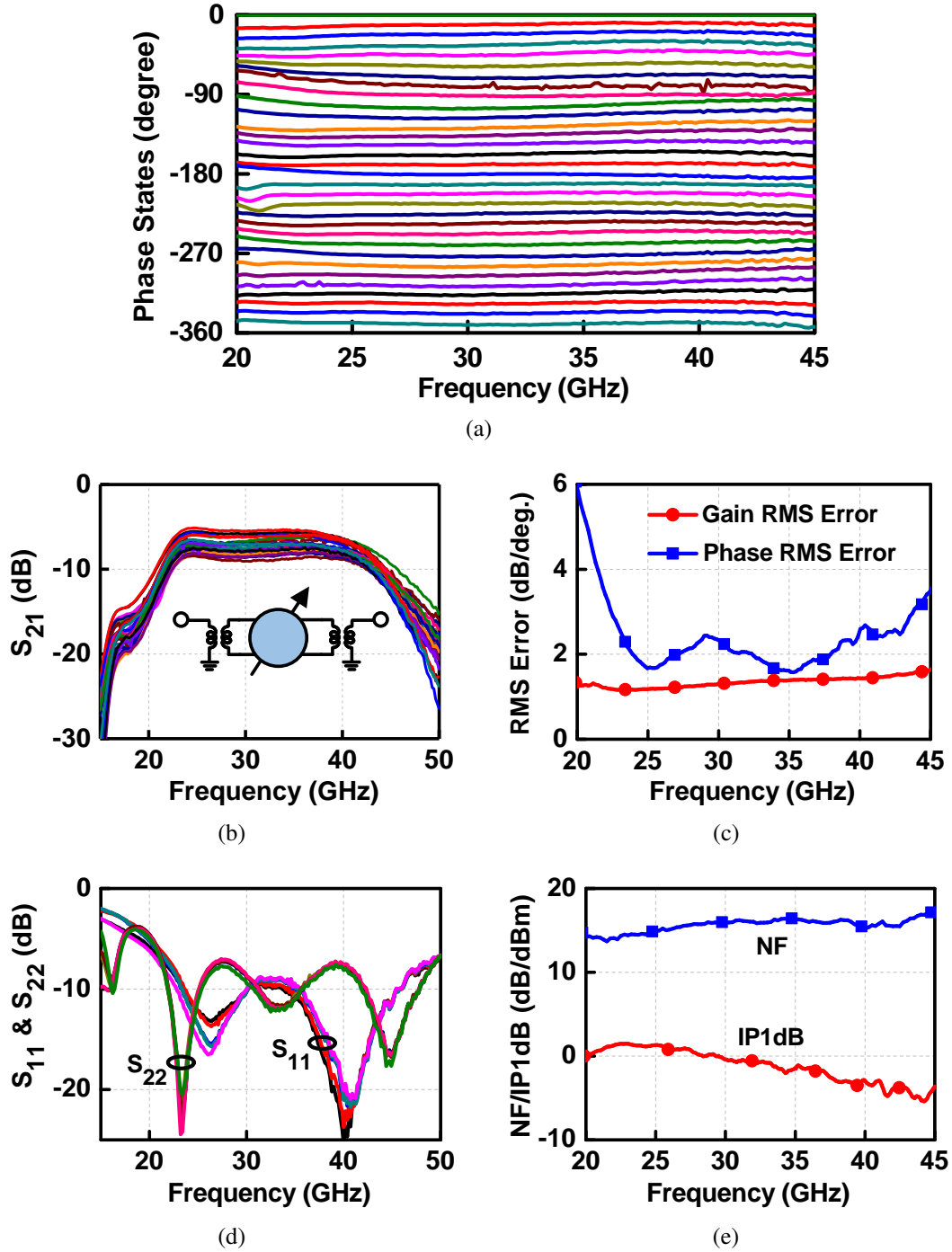
Figure 2.18: Measured VM performance (a) Phase state; (b) S_{21}; (c) Phase and gain RMS error; (d) S_{11} and S_{22}; (e) NF and IP1dB.

2.3.2   VM

For measurement purpose, wideband baluns are added at the input and output port of the VM test chip. The baluns add ∼2-3 dB loss for S_{21} (at middle band) and increase the NF by 1.5-2

dB (the input and output balun losses are not de-embedded).

Fig. 2.18a presents the measured VM phase response, and the 5-bit control realize 349° of phase shift at 20-45 GHz with no crossovers in the phase response. Fig. 2.18b presents the measured gain at different phase state, with a 3-dB bandwidth of 22-44 GHz (limited by the input and output baluns). The measured RMS phase and gain errors are < 3° and < 1.6 dB, respectively, at 22-44 GHz. The input and output matching is also limited by the baluns, but the S_{11} and S_{22} are still better than -9 dB and -7 dB at 22-44 GHz (Fig. 2.18d). Fig. 2.18e presents the measured NF and IP1dB when the phase shift is set to 45°. The NF is 14 to 17 dB and IP1dB is -4 to 1.5 dBm at 22-44 GHz. The dc power consumption is 62 mW.

2.3.3   VGA

A wideband input balun is added at the input of the VGA test block for single-ended measurements, but in this case, the balun loss is de-embedded to get the VGA gain (loss introduced by the mismatch is ignored). Fig. 2.19 presents the measured S-parameters of the VGA. The measured peak gain is 10.5 dB with a 3-dB bandwidth of 18.7-44 GHz. The gain shape has a slight difference compared with simulations and is due to the de-embedding procedure which considered the balun loss and ignored the mismatch. When the attenuator is off, the gain tuning is 11.6/12.4/11.5 dB at 22/33/44 GHz, respectively. When the attenuator is on, an additional ∼4 dB of gain control is achieved. The measured S_{11} is < -10 dB at 22-50 GHz and S_{22} < -8 dB.

Fig. 2.20 presents the measured VGA NF and IP1dB. For the highest gain state, the NF is 2.4-5.7 dB and the IP1dB is -11 to -7.7 dBm at 20-44 GHz. Table 2.3 compares the wideband VGA with previous work. It is observed this work realizes wideband performance with lower power consumption and with high linearity.
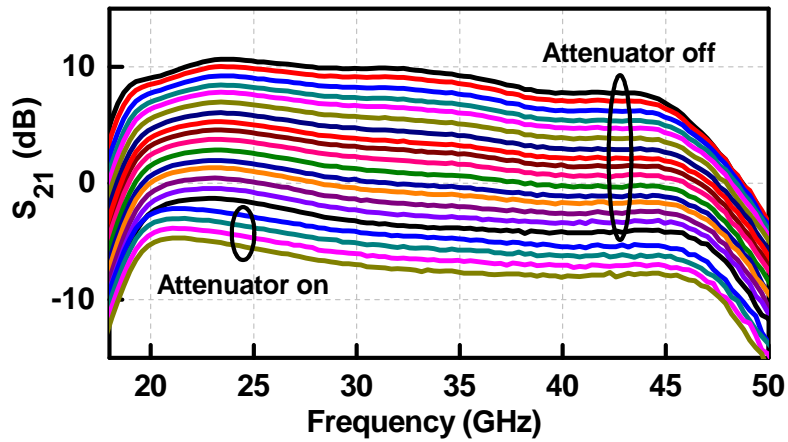
(a)
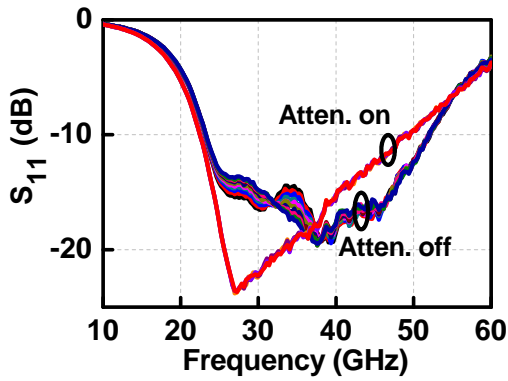
(b)
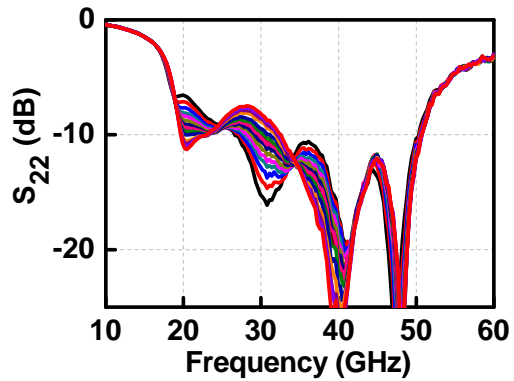
(c)

Figure 2.19: Measured VGA performance (a) S_{21}; (b) S_{11}; (c) S_{22}.
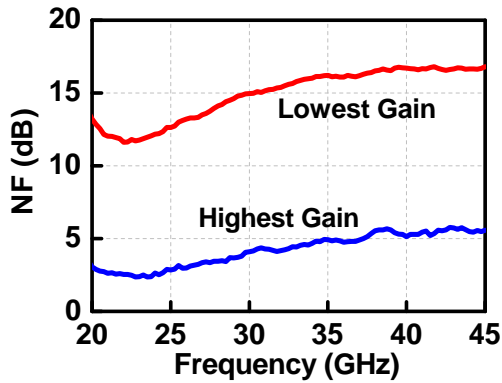
(a)
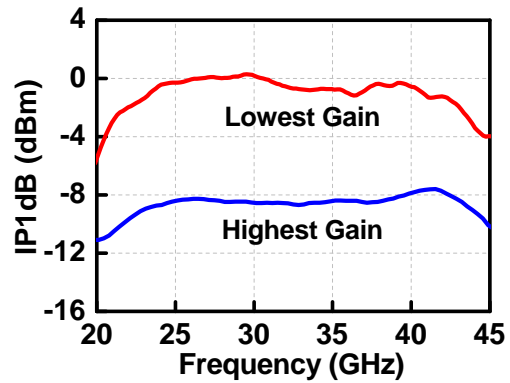
(b)

Figure 2.20: Measured VGA at highest (10.5 dB) and lowest (-5.5 dB) gain mode (a) NF; (b) IP1dB.

Table 2.3: Comparison with Previous Wideband VGA

Ref.	Tech.	BW (GHz)	Peak Gain (dB)	Tuning Range (dB)	Mini. NF (dB)	P_{dc} (mW)
[23]	40-nm CMOS	26-33	27.1	9	3.3-4.3	31.4
[16]	SiGe	15.5-39	17	23	3.6-9	104
[24]	0.12-µm SiGe	26-40	20	11	3.3-5	33
[25]	65-nm CMOS	27-42	9.6	7.8	N.A	15.6
This work	45-nm SOI	18.7-44	10.5	16	2.4-5.7	25

2.4 Beamformer Channel Measurements

Fig. 2.21a presents the measured and simulated S-parameters of the Rx beamformer channel at the highest gain state. The total power consumption is 112 mW. The peak gain is 26.3 dB with a 3-dB bandwidth of 20.5-44 GHz. An S_{11} < -10 dB at 22-50 GHz and S_{22} < -9.5 dB at 24-49 GHz is obtained. The measured S_{12}<-40 dB and the K-factor is > 1 (not shown). The gain control is similar to the VGA and therefore is not shown here. At the highest gain state, the measured NF is 3-3.6 dB at 22-44 GHz. At the lowest gain state, the measured NF is 3.4-4.2 dB at 22-44 GHz (Fig. 2.21b).

The measured IP1dB and IIP3 are shown in Fig. 2.21c, where the IIP3 is measured using a two-tone separation of 100 MHz. At the highest gain state, the IP1dB and IIP3 is -26.8 and -17.5 dBm at 35 GHz and the linearity is limited by the VGA. At the lowest gain state, the measured IP1dB and IIP3 improve to -24.4 and -19.5 dBm at 35 GHz and the linearity is limited by both the VGA and VM.

Fig. 2.22a-b presents the measured relative phase and gain response. The RMS phase and gain error is < 6° and < 1.9 dB, respectively, at 22-44 GHz (Fig. 2.22c). The ripple in the phase state is due to a small ground inductance between the input and output ports (this can be eliminated in future designs).

Table 2.4 compares the 22-44 GHz beamforming receive channel with start-of-art phased-
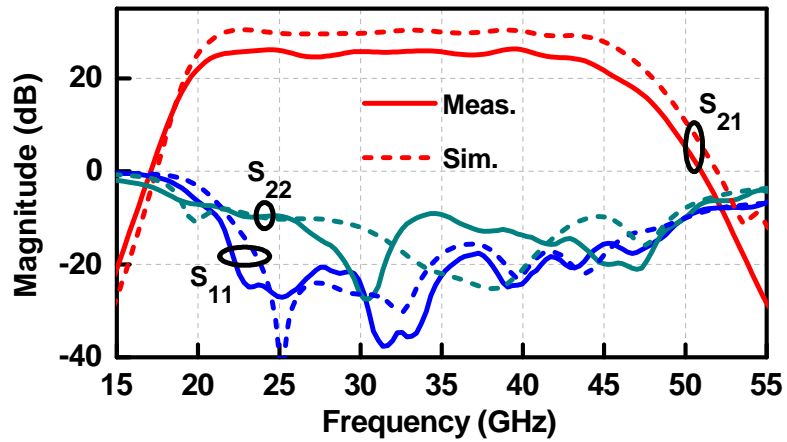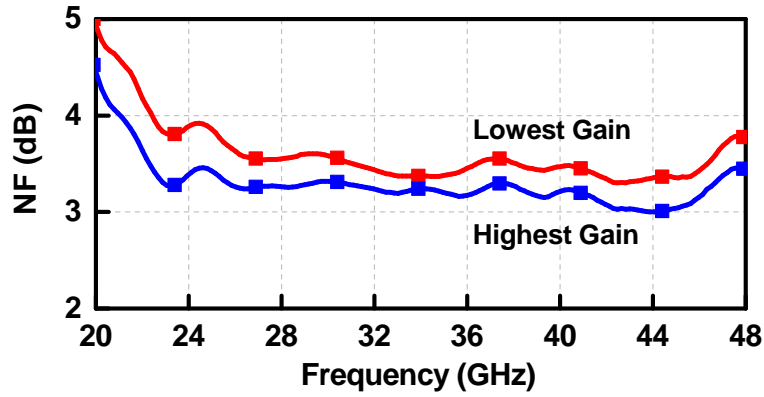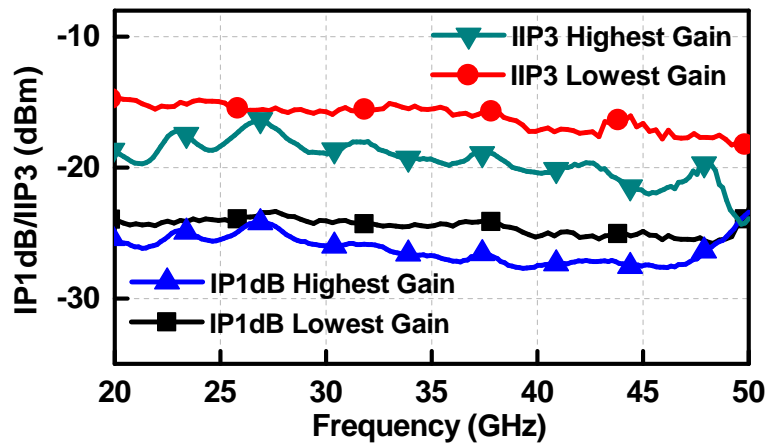
Figure 2.21: Measured wideband beamforming channel (a) S-parameters at highest gain; (b) NF; (c) IP1dB and IIP3.
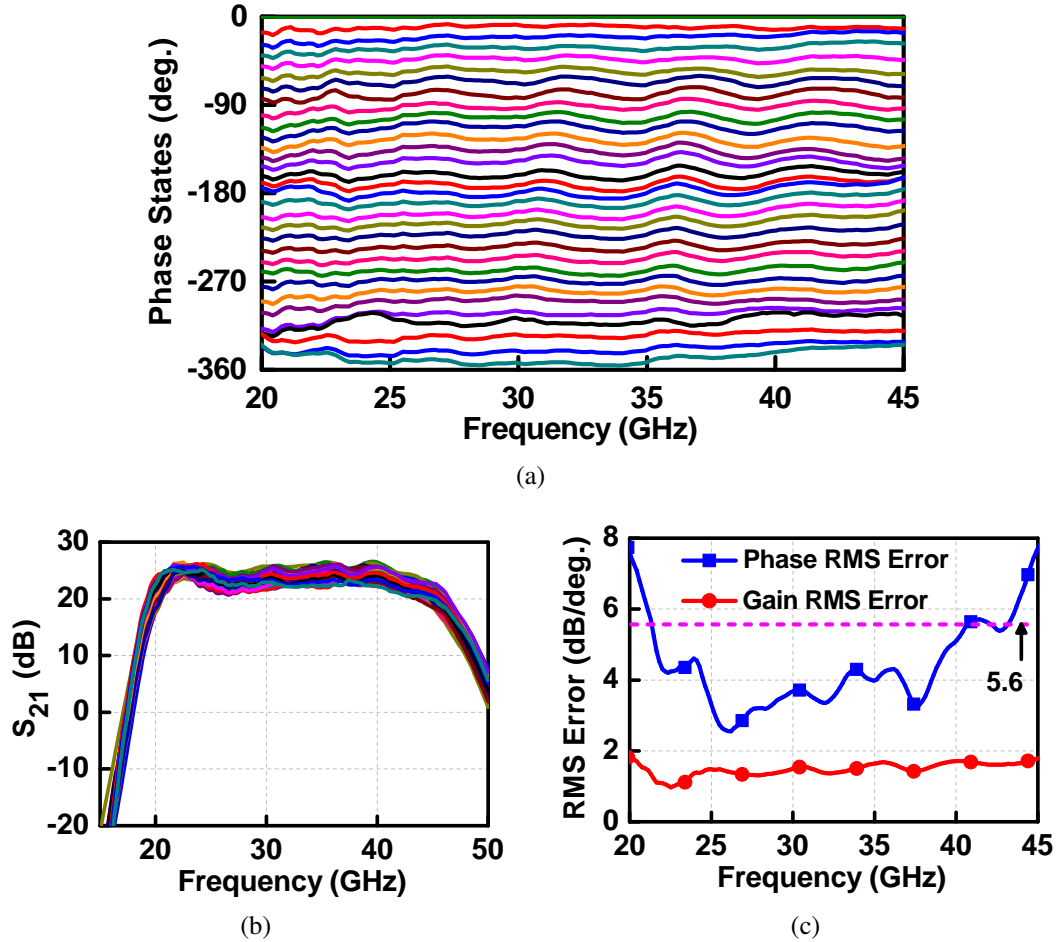
Figure 2.22: Measured wideband channel performance (a) 5-bit phase control; (b) S_{21}; (c) Phase and gain RMS error.

array receivers. It can be observed that this work achieves the widest bandwidth and lowest NF with comparable gain control and phase control resolution.

2.5   Conclusion

This chapter presented a wideband phased array receiver channel that covers the entire 22-44 GHz millimeter wave 5G band in GF 45-nm CMOS SOI. The receiver channel has realized a peak gain of 26.3 dB with 3 dB bandwidth of 20.5-44 GHz with NF of 3-3.6 dB. Input and output are well matched. The phase and gain rms error is is $< 6°$ and < 1.9 dB. Both the single blocks

Table 2.4: Comparison with State-of-the-art Wideband Beamformer Receiver

Ref.	Tech.	BW (GHz)	Gain (dB)	NF (dB)	Gain Tuning (dB)	PS Res. (°)	Phase/Gain RMS Error (°/dB)	IP1dB (dBm)	P$_{dc}$ (mW)
This work	45-nm SOI	22-44	26.2	3-3.6	16	11.25	6/1.9	-25.4	112
[1]	28-nm CMOS	24.2-31.7	16	3.2-4.4*	8	45	N.A	N.A	42
[2]	0.18-μm SiGe	24.5-30.5	19	5.5*	26	5.6	4/0.6	-19	160
[3]	45-nm SOI	24-30	16	3.7*	7.5	11.25	5.6/1	-15	54
[4]	0.18-μm SiGe	27-33	20	4.6*	14	5.6	6/0.8	-22	130
[8]	0.13-μm SiGe	34-39	-1	9*	8	11.25	12/0.9	-16	35.5
[9]	65-nm CMOS	36-40	40	6-9	20	22.5	5.5/2	-41	174
[12]	28-nm CMOS	37-40	42	6-7.6*	27	11.25	N.A/2	-44	78.5

* including SPDT loss

and the channel achieve state-of-the-art performance. The wideband response, low NF, and high gain, wide gain tuning range and low phase RMS error makes it suitable for 5G millimeter-wave beamforming systems.

2.6 Acknowledgment

Chapter 3

A High Power 24-40 GHz Transmit-Receive Front-End For Phased-Arrays in 45-nm CMOS SOI

3.1   Introduction

This chapter presents a dual-band front-end, which covers both the 24-28 GHz and the 37-40 GHz band (Fig. 3.1). The front-end antenna ports are differential because most wideband antennas are of a differential nature (tapered slot antennas, tightly coupled-dipoles, wideband conical and bow tie antennas [26–28]). Also, all circuits are differential for stable and robust packaging. There are several innovations in the present work: First, the 20-40 GHz LNA employs a combination of resistive feedback and multi-state matching and results in low NF and high figure of merit. Second, the asymmetrical wideband SPDT switch is co-designed with the PA and LNA, and is optimized for handling a high transmit power (> 20 dBm) while at the same time achieving low-loss in the Rx path. The switch achieves state-of-the art insertion-loss both in the Tx and Rx paths, which is not typical at these frequencies as either the Tx or Rx path is generally

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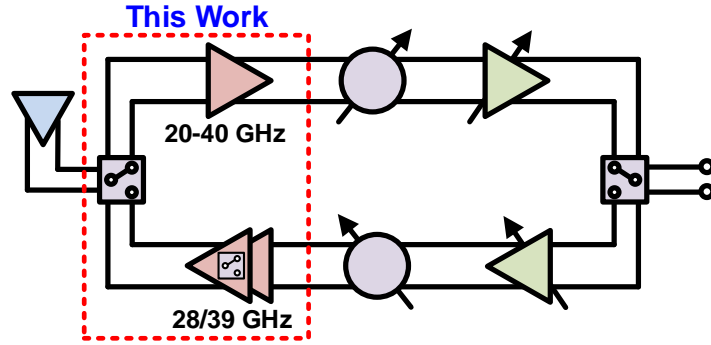
Figure 3.1: A dual-band phased array beamformer channel. Several channels are combined together on a single chip to form a 4-16 channel chip.

compromised. Third, in the Tx path, the PA is designed with a switched-load, therefore achieving an optimum load-line for the 24-28 GHz band (low-band) and the 37-40 GHz (high band). The front-end achieves high performance at 24-40 GHz, and design details and measurements are presented in this chapter.

3.2 Design

The PA/LNA/SPDT switch front-end is also based on the GlobalFoundries (GF) 45-nm RFSOI process, as described in chapter 2. The substrate resistivity is 2.5 kΩ-cm, which increases the inductor Q to > 20 at 30 GHz, is beneficial for switch design, and results in increased isolation between different transistors.

3.2.1 SPDT Switch

There are three main design techniques for millimeter-wave SPDT switches. The first is transformer-based with a compact size and high out-of-band rejection due a second-order bandpass response [29]. However, it has a relatively high loss due to the inductor Q and is not suitable for very wideband designs. The second is based on quarter-wavelength transmission-lines (TL), or equivalent C-L-C networks, to synthesize open circuits at the rejection ports [4]. In some
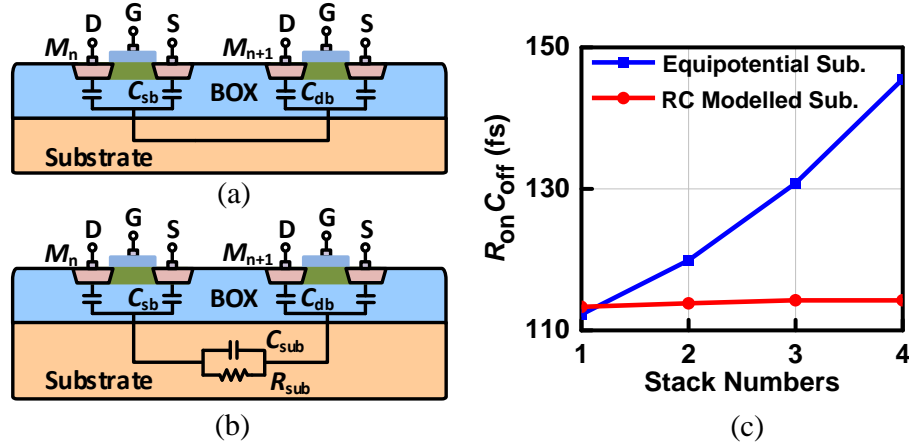
Figure 3.2: (a) Cross section view of a two-stack transistor (a) using equipotential substrate assumption; (b) using RC modelled substrate; (c) Simulated $R_{on}C_{off}$ for different stack numbers.Schematic of the output matching network.

cases, a switch is removed from the transmit side to improve the Tx path loss [1, 5, 30]. This is a narrowband design and cannot be used for wideband systems. Therefore, for a wideband design, the series-shunt switch topology is still one of the best choices [31–35], provided that it is used with a minimal number of passive components for reduced loss, and the transistors are sized appropriately.

In order to achieve high linearity, the switch employs stacked transistors to divide the voltage swing across multiple transistors [31–33]. For mm-wave designs, it is important to correctly account for the substrate effects between adjacent transistors in the stack. The parasitic extraction tool assumes that the substrate is an equipotential layer and shorts the substrate nodes in the stack (Fig. 3.2a). This may be acceptable for bulk CMOS processes but results in inaccurate values for the device capacitance in the SOI process, and can detune the matching networks.

A more accurate way to model the substrate coupling is to make use of a parallel RC network which correctly represents the substrate coupling between the diffusion regions of adjacent transistors, and then explicitly connect this RC model between the substrate nodes (Fig. 3.2b). Given the area occupied by the two devices on the substrate and the distance between them, the 45RFSOI PDK utilizes quasi-static capacitance calculation and substrate's dielectric
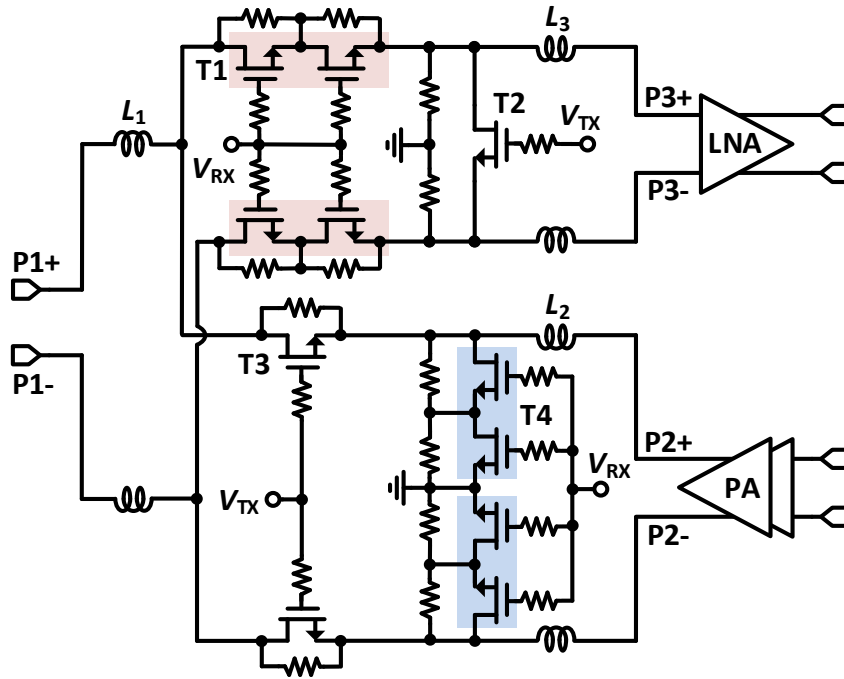
Figure 3.3: Schematic of the differential asymmetrical SPDT.

constant to estimate the values of R_{sub} and C_{sub}. Fig. 3.2c presents the simulated figure of merit (FoM= $R_{on}C_{off}$) of 100 μm NMOS transistors with 1 to 4 stacks, where the transistor diffusion layers are separated by 5 μm (edge to edge). It can be observed that the equipotential substrate assumption significantly degrades the stack FoM and if overlooked, may lead to pessimistic simulation results.

Fig. 3.3 presents the differential asymmetrical SPDT switch used in this work. Note that 2-stacks are used for T4 (due to the ground node in the middle) and T1 to handle the voltage waveform resulting from a transmit power of 20 dBm. For T4, the transistor width is 100 μm with R_{on} = 3.25 Ω and C_{off} = 34.4 fF (FoM= 112 fs referenced to the top metal layer). For T1, the transistor width is 150 μm with R_{on} = 2.2 Ω and C_{off} = 51 fF. In the Tx mode, T4 and T1 stacks are biased at V_{RX} = -1 V for added voltage handling and are in the OFF state. T2 (30 μm, R_{on}= 10.3 Ω) and T3 (90 μm, R_{on}=3.61 Ω) transistor stacks are biased ON with low resistance and therefore, only 1 or 2-stack is needed for proper operation. A single transistor is used for T3 for low insertion loss in the Tx path.
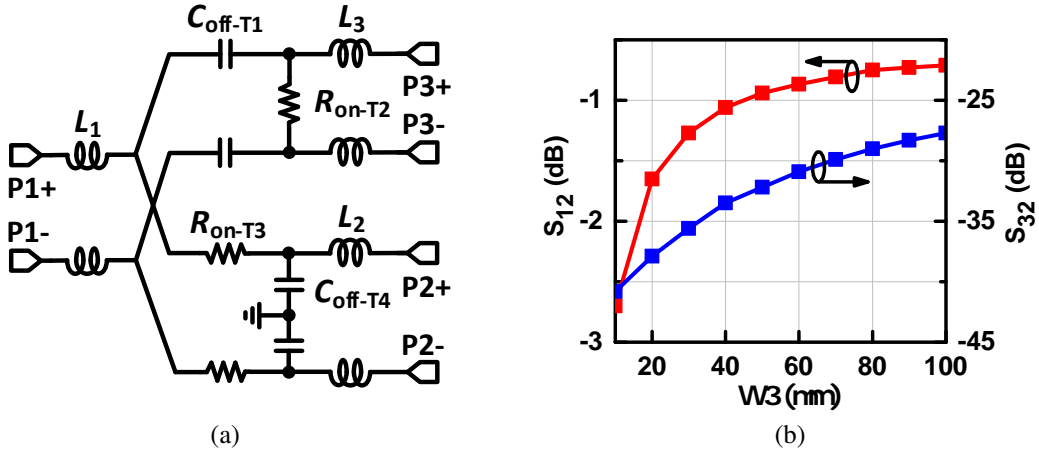
Figure 3.4: (a) Tx mode equivalent circuit; (b) Simulated insertion loss and isolation versus transistor size at 40 GHz.

To achieve wideband performance, the transistor off-state capacitance C_{off} needs to be tuned using an L_S-C_{off}-L_S network (Fig. 3.4a). Such a circuit can match a maximum capacitance $C_{off\text{-}max}=1/(2\pi f_0 Z_0)$ at DC to f_0 using $L_s=Z_0/2\pi f_0$, where Z_0 is the port impedance. For $f_0=40$ GHz, $Z_0=50$ Ω, $C_{off\text{-}max}=80$ fF and $L_s=200$ pH. In reality, C_{off} is less than $C_{off\text{-}max}$ due to added capacitance from the planar inductors. The final design employs $L_1=L_2=L_3=140$ pH, implemented on OA and OB layers with a Q of 25 at 30 GHz.

A key point in the design is the width of T3. A large transistor results in low insertion loss in the Tx mode (T3 ON), but poor Tx-Rx isolation in the Rx mode (T3 OFF), and a small transistor results in the opposite trend. Fig. 3.4b presents the simulated S_{12} and S_{32} versus T3 size in the Tx mode. A width of 90 μm is chosen and results in 0.8 dB insertion loss and > 29 dB Tx-Rx isolation at 40 GHz.

When the SPDT is biased for the Tx mode, there is a large voltage swing across T4 and T1 at peak output power levels. T4 and T1 are in the OFF state and can be potentially turned on. Fig. 3.5 presents the simulated voltage and current across the switches when a 20 dBm (differential) power is applied at P2. It is observed both the voltage and current are perfectly sinusoidal showing no harmonic content, and the voltage swing across each transistor is ± 1 V_{pk}
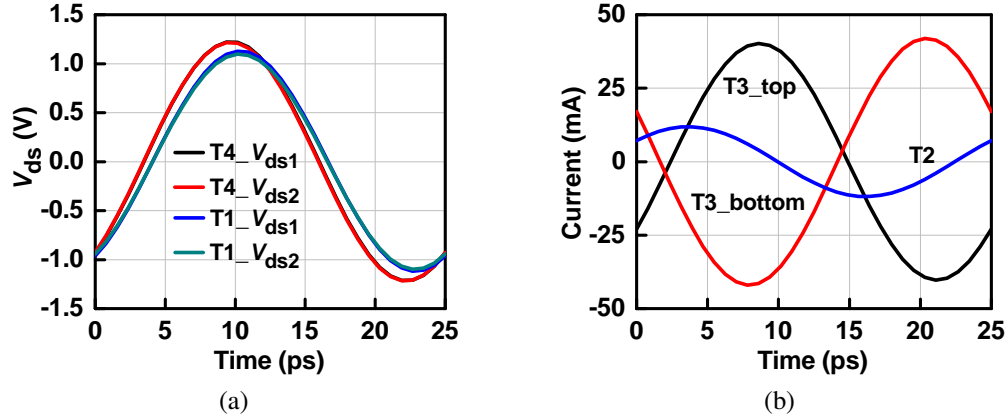
Figure 3.5: Simulated waveform when P2 (differential) is excited with Pin=20 dBm (a) Voltage across each transistor for the T1 and T4 upper arms at 40 GHz; (b) Current across T2 and T3 at 40 GHz.

and therefore, the transistor does not turn on with a gate bias of -1 V. The current in T3 peaks a 41 mA while the current in T2 peaks at 12 mA due to the isolation of T1.

The simulated SPDT results in $S_{11} < -10$ dB up to 45 GHz in both the Tx and Rx modes, with an insertion loss of 0.63-1.09 dB in the Rx mode, and 0.5-0.77 dB in the Tx mode at 20-40 GHz. The simulated IP1dB for the Tx mode is > 26 dBm up to 40 GHz. When the input is 20 dBm, the gain compression is only 0.3-0.4 dB. The Rx mode IP1dB is 17 dBm, which is much higher than LNA IP1dB and does not limit the Rx linearity.

3.2.2 LNA Design

The wideband differential LNA is realized using a two-stage cascode amplifier (Fig. 3.6). The transistor is chosen with W=60 μm to result in the real part of the optimal source impedance close to 50 Ω at 32 GHz (mid-band). Layout is done using 60 fingers each 1 μm wide, and with double gate connection for reduced gate resistance. The amplifier is biased at a current density is 0.15 mA/μm, which is ideal for low noise and high gain (0.1-0.2 mA/μm), resulting in a dc power consumption of 36 mW.

The first stage is designed with resistive feedback for wideband performance, and a multi-section inter-stage matching network consisting of L_4, L_5, R_2, C_2 and L_6 is used to match
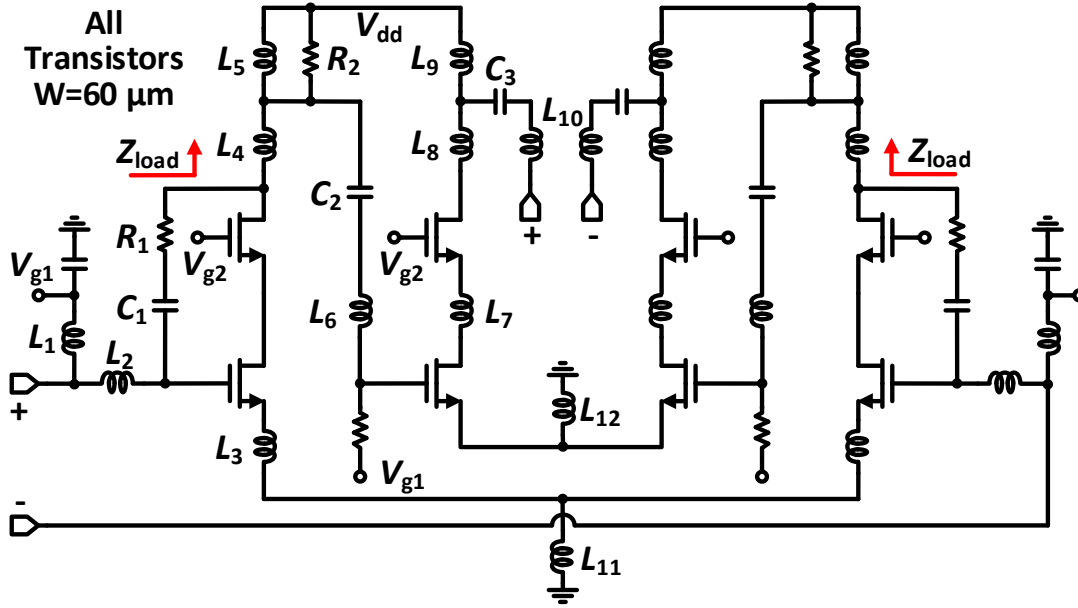
Figure 3.6: Schematic of two stage differential wideband LNA.

Table 3.1: LNA Component Values (H or F)

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8
400 p	120 p	70 p	400 p	250 p	200 p	200 p	100 p
L_9	L_{10}	L_{11}	L_{12}	C_1	C_2	C_3	R_1
380 p	350 p	400 p	400 p	315 f	190 f	77 f	1 k

the relatively high output impedance to the second stage. Again, all inductors have a $Q > 20$ at 32 GHz. Fig. 3.7a presents an analysis of the wideband load impedance of first stage. It is observed that the imaginary part is wideband and inductive, and resonates with the output capacitance of of the cascode trransistor in the first stage to provide a wideband gain response. A similar load network is used at the second stage. The simulated voltage gain of each stage is shown in Fig. 3.7b. The first stage has two peaks at 25 GHz and 46 GHz and maintains > 9 dB gain at 20-40 GHz. This suppresses the noise of the second stage and maintains a low NF over the entire band. Due to a similar load matching network, the second stage also exhibits a wideband response.

A wideband input matching is realized using source-inductor degeneration and low-level resistive feedback ($R_1=1$ kΩ). Fig. 3.7c presents amplifier simulations with and without the feedback resistor. The resistive feedback flattens the gain and improves the input match from -7
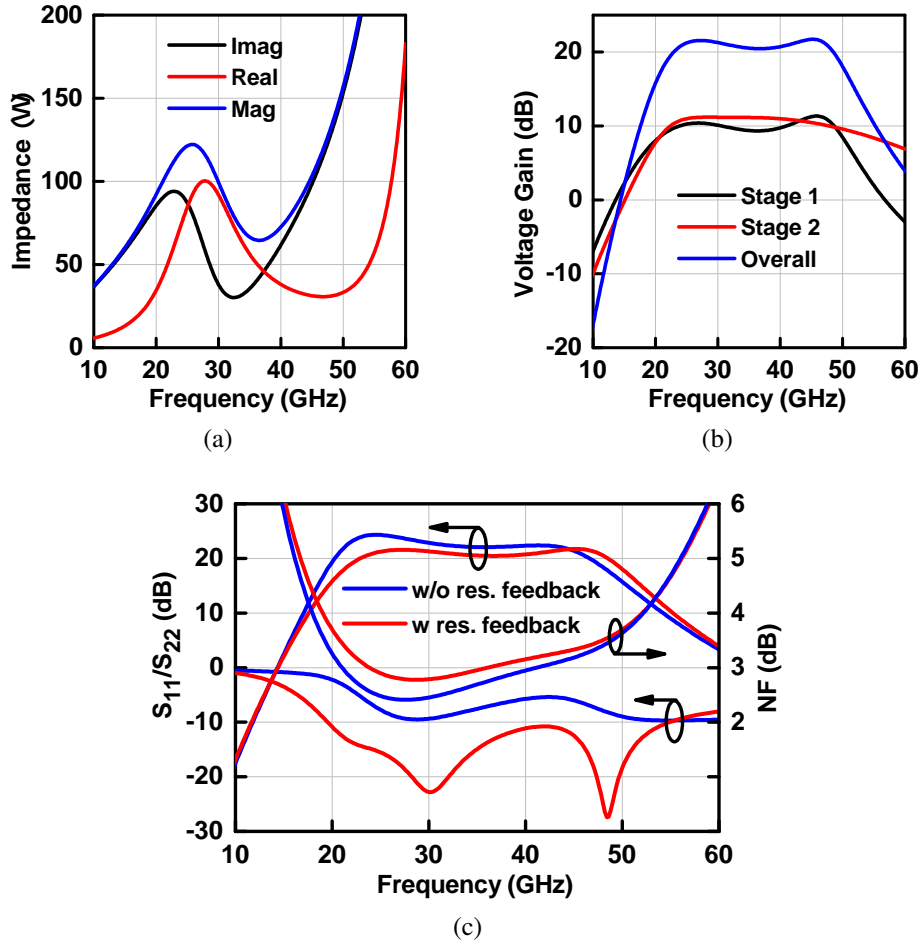
Figure 3.7: (a) Simulated load impedance of stage 1 with next stage input impedance (marked as Z_{Load}), (b) Simulated voltage gain of each stage of complete circuit. (c) Simulated LNA versus resistive feedback.

dB to -13 dB over the band, at an average increase of 0.2 dB in the NF at 20-45 GHz.

The common-mode rejection is realized by adding tail inductors (L_{12} and L_{13}), which improve the common-mode rejection by 18 dB without affecting the differential mode. The final important parameter values are listed in Table 3.1. The simulated LNA peak gain is 22.2 dB with a 3-dB bandwidth of 21-46 GHz and a NF less than 3.5 dB at 20-44 GHz.

3.2.3 PA Design

The dual-band differential PA consists of a two-stack driver amplifier and three-stack main amplifier, coupled together using a transformer-based inter-stage matching network as shown in
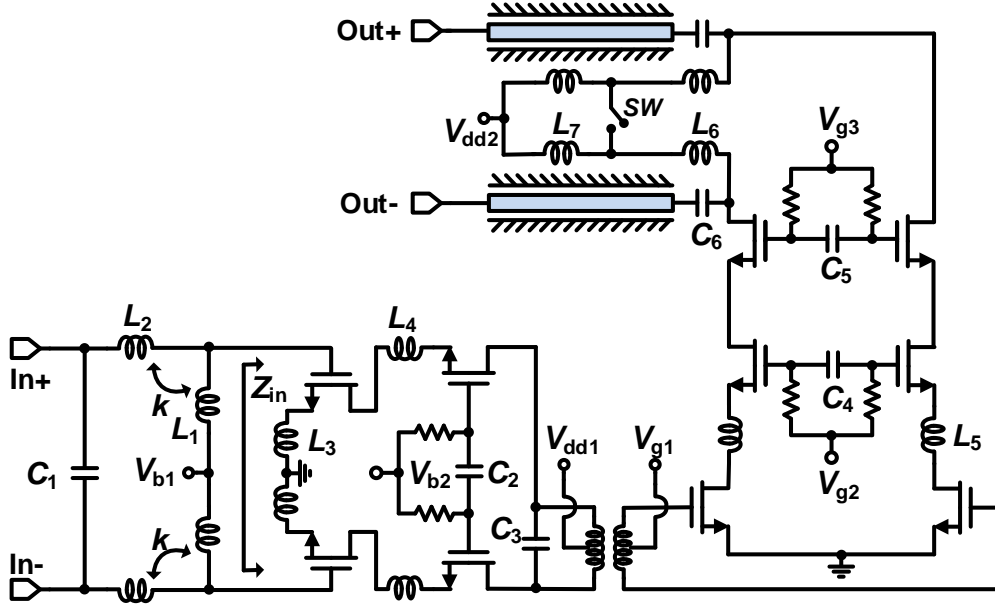
Figure 3.8: Schematic of the differential two-stage dual-band power amplifier.

Table 3.2: PA Component Values (H or F)

L_1	L_2	L_3	L_4	L_5	L_6	L_7	C_1	C_2	C_3	C_4	C_5
77 p	100 p	20 p	30 p	30 p	115 p	80 p	70 f	166 f	45 f	166 f	53 f

Fig. 3.8. Each transistor in the driver as well as the main amplifier has a width of W=252 μm.

The driver amplifier needs to provide wideband (or dual-band) input matching to 100 Ω, and inductive degeneration, L_3, is used to increase the real part of the transistor input impedance, as shown in Fig. 3.9a. A larger degeneration inductor results in a higher real impedance, however, this also results in a lower amplifier gain. Therefore, $L_3 = 20$ pH is chosen and provides a real part of 10-16 Ω at 26-45 GHz. To create dual-band matching, a weakly-coupled transformer is also used which generates two distinct poles. The coupled inductors are implemented in the OA and OB layers, as shown in Fig. 3.9b. L_1 and L_2 are 77 pH and 100 pH with Q of 23 and 28 at 30 GHz, respectively. The coupling factor is designed to be 0.17 in order to achieve a double-tuned response, and k is used to tune the pole separation. The simulated S_{11} is < -10 dB at 26-44 GHz, with two distinct poles at 28 GHz and 41 GHz (Fig. 3.9c).

Load-pull simulations are then performed for the driver amplifier in order to optimize

(a)

(b)

(c)
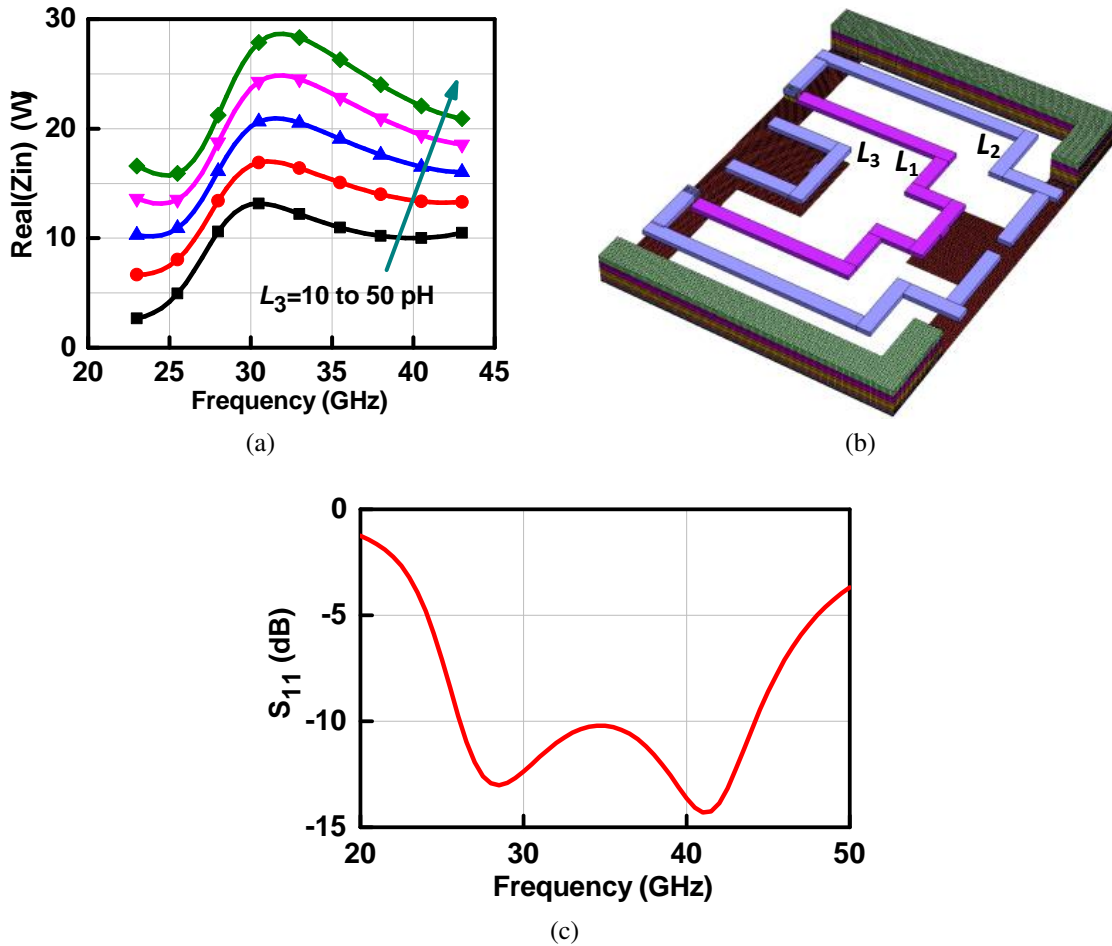
Figure 3.9: Simulated real part of the driver input impedance versus L_3; (b) 3-D layout of L_1, L_2, and L_3; (c) Simulated S_{11} .

its efficiency and output power. The inter-stage matching is also designed using a double-tuned transformer to match the main amplifier's input impedance to the desired load-pull impedance (Fig. 3.10a). This matching network has a high-Q as the input impedance of the main amplifier is nearly purely capacitive and inductive de-generation is not used in the main amplifier. Therefore, to extend the inter-stage matching bandwidth, a large k is used in the transformer design, and this result in a matching ripple versus frequency. However, the 5G millimeter-wave bands are around 28 and 39 GHz and attention is paid to these two bands for interstage matching.

The double-tuned poles are derived as [36]

$$\omega_{\mathrm{L,H}} = \omega_0 \sqrt{1 - \frac{1}{2Q^2} \pm \sqrt{(1 - \frac{1}{2Q^2})^2 - (1 - k^2)}} \qquad (3.1)$$

$$Q = R_{\mathrm{S}}C_{\mathrm{P}}\omega_0 = R_{\mathrm{L}}C_{\mathrm{S}}\omega_0 \qquad (3.2)$$

$$\omega_0 = \frac{1}{\sqrt{L_{\mathrm{P}}C_{\mathrm{P}}(1 - k^2)}} = \frac{1}{\sqrt{L_{\mathrm{S}}C_{\mathrm{S}}(1 - k^2)}} \qquad (3.3)$$

where L_{P}, C_{P}, L_{S} and C_{S} are the equivalent primary and secondary-stage networks. In this design, L_{P} and L_{S} are 192 pH and 157 pH, and k is 0.5. L_{P} is realized on the OB layer and L_{S} is realized on the OA layer, both with 3 μm thick Cu metal. Fig. 3.10b presents the simulated load-pull contours for the diver stage at 28 GHz and 39 GHz, and the simulated impedance from the inter-stage matching network (Z_{ISM}). The transformed main amplifier input impedance is located close to the center of the high-efficiency contours.

The main amplifier employs three-stack transistors in order to achieve the required output power, with a peaking inductor L_5=30 pH between the first and second transistor in the stack. By carefully choosing the external gate capacitors (C_4=166 fF, C_5=53 fF) for the stacked transistors, the voltage swing at the output node can be divided equally across each transistor in the three-stack [37, 38]. Similar peaking inductor and external gate capacitor have been used for the two-stack driver amplifier (C_2=166 fF, L_4=30 pH).

For a differential amplifier, the gate capacitor can be connected between the gates of the corresponding transistors exploiting the virtual ground. This reduces the required gate capacitance to half of the single-ended equivalent circuit, while also providing common mode rejection. In the differential-mode small-signal equivalent circuit, the gate capacitor connects to the virtual ground at the center, and provides differential-mode gain since the voltage swing at the source is divided between transistors C_{gs} and $2C_4$ (or $2C_5$). For the common-mode signal, the gate capacitor is connected to a virtual open, and the voltage swings across the large bias resistor (R_{b}=12 kΩ)
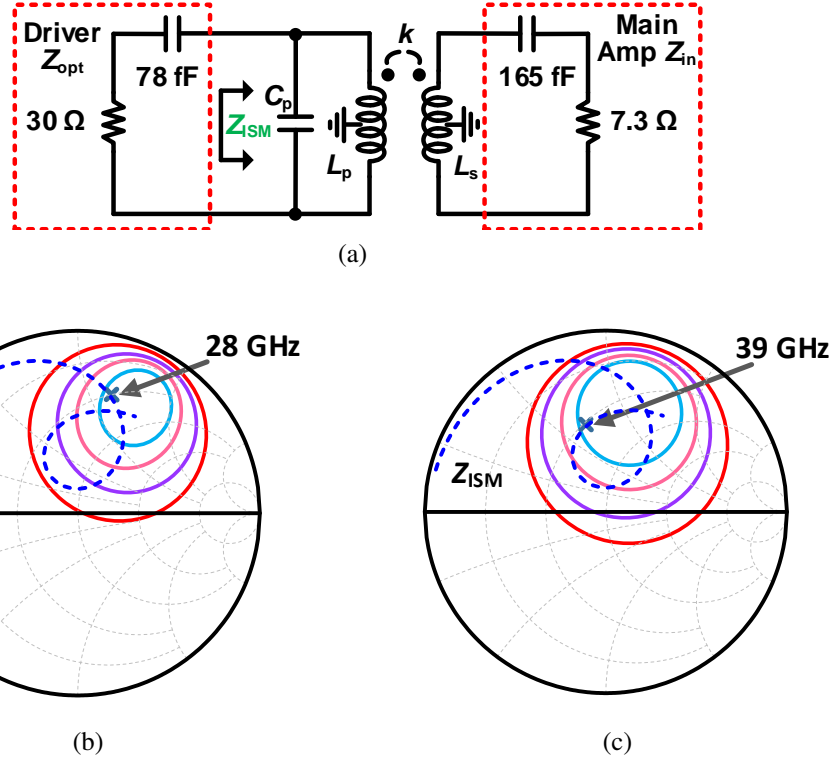
Figure 3.10: (a) Inter-stage transformer matching; Simulated PAE contour and input impedance of the inter-stage matching, Z_{ISM}, at (b) 28 GHz; (c) 39 GHz.

rather than C_{gs}, since $R_{\mathrm{b}} \gg 1/\omega C_{\mathrm{gs}}$. The driver amplifier also provides common-mode rejection in a similar manner. The common-mode rejection ratio (CMRR) can be approximated using the small-signal equivalent model for the NMOS transistors (ignoring C_{gd}) as:

$$CMRR \approx \frac{(1+g_{\mathrm{m}}r_0\frac{2C_2}{C_{\mathrm{gs}}})(1+g_{\mathrm{m}}r_0\frac{2C_4}{C_{\mathrm{gs}}})(1+g_{\mathrm{m}}r_0\frac{2C_5}{C_{\mathrm{gs}}})}{(\sqrt{1+(g_{\mathrm{m}}r_0\frac{1}{sR_{\mathrm{b}}C_{\mathrm{gs}}})^2})^3} \tag{3.4}$$

Equation (3.4) is an optimistic estimate and in reality, transistor and layout non-idealities limit the CMRR. Nevertheless, this technique provides a simulated CMRR > 15 dB at 24-40 GHz. Note that the differential capacitor presents an added layout constraint in that the corresponding pair of transistors need to be laid out close to each other.

Load-pull simulations are also done for the main amplifier to obtain the optimal impedances for achieving the highest PAE. The output matching is designed using a series-*C*, shunt-*L* network

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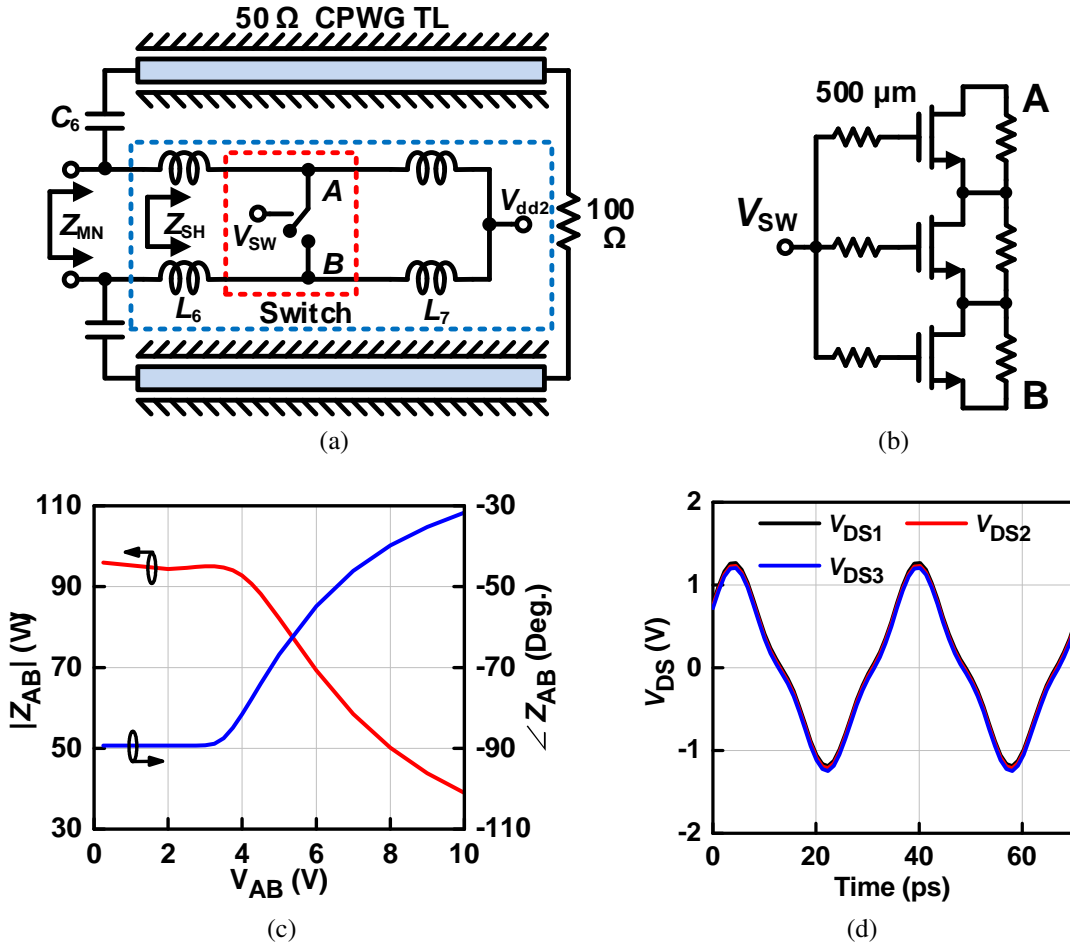
Figure 3.11: (a) Structure of output matching network; (b) Three-stack switch in MN (all un-labelled resistors are 12 kΩ); (c) Simulated switch impedance (Z_{AB}) versus voltage swing; (d) Simulated the voltage swing across the three switch transistor at 28 GHz when operating at P1dB.

as shown in Fig. 3.8 (C_6, L_6, L_7). However, such a matching network requires a larger effective shunt-L at 28 GHz than at 39 GHz. Fig. 3.11a presents an output matching network topology that can effectively implement the above condition and maintain an optimal load impedance to the main amplifier (within the high PAE contours). An SOI switch is connected between nodes A

and B, and this reconfigures the shunt branch impedance such that:

$$Z_{\text{SH}} = j\omega 2L_6 + (\frac{1}{j\omega C_{\text{OFF,SW}}} || j\omega 2L_7) \qquad \text{Switch OFF} \qquad (3.5)$$

$$Z_{\text{SH}} = j\omega 2L_6 + (R_{\text{ON}} || j\omega 2L_7) \qquad \text{Switch ON} \qquad (3.6)$$

$$Z_{\text{MN}} = 2 \times (50 + \frac{1}{j\omega C_6}) || Z_{\text{SH}} \qquad (3.7)$$

where $R_{\text{ON,SW}}$ and $C_{\text{OFF,SW}}$ are the on-resistance and off- capacitance of the SOI switch. For high-band operation when the switch is ON, it is evident that $R_{\text{ON,SW}}$ causes additional loss in the switch network and hence decreases the output power and efficiency. The switch should also be designed to withstand the current levels at maximum output power. At the same time, for low-band operation when the switch is OFF, the switch should neither breakdown due to a large instantaneous voltage swing across nodes A and B (V_{AB}), nor should it turn-on and compress the output power. Therefore, the shunt switch is implemented using a stack of three NMOS transistors of width 500 μm (Fig. 3.11b). The switch transistors are tightly connected together using the top five copper layers to minimize $R_{\text{ON,SW}}$, and results in $R_{\text{ON,SW}}$=2.35 Ω and $C_{\text{OFF,SW}}$=58.7 fF. The DC voltage at nodes A and B is equal to V_{dd2}, and V_{SW} is nominally biased at (V_{dd2}+1) V or (V_{dd2}-1) V for turn-on or turn-off, respectively.

Fig. 3.11c presents the impedance of the switch stack (Z_{AB}) in the OFF state versus $|V_{\text{AB}}|$ at 28 GHz. The switch impedance (phase and magnitude) remain close to that of an ideal capacitor of value $C_{\text{OFF,SW}}$ for $|V_{\text{AB}}|$ up to 3.5-4 V, before turn-on starts to occur. Fig. 3.11d shows the simulated V_{DS} across each individual transistor in the switch stack at 28 GHz at P1dB operation. The peak V_{DS} across any transistor remains within ±1.3 V, which is within the breakdown limit of the device. In the ON state, the switch stack has to handle to a large instantaneous current flowing though it as it shunts the L_7 inductors. The simulated current through the switch stack at 39 GHz, for a P1dB of 20 dBm, shows a peak amplitude of 87 mA, resulting in a current density of 0.17 mA/μm and meeting all current-density rules. Compared to an ideal switch with 0 Ω resistance,
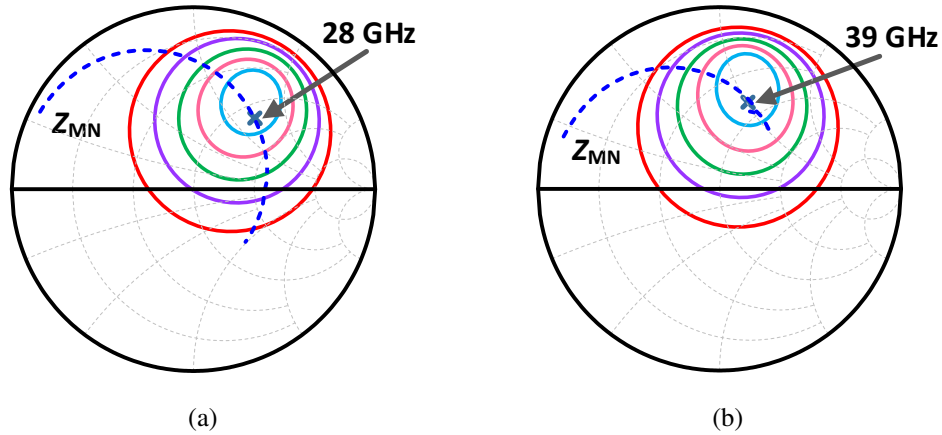
Figure 3.12: Simulated PAE contour and input impedance of the output matching network, Z_{MN}, at (a)28 GHz (switch ON);(b)39 GHz (switch OFF).

the 3-stack SOI switch adds a matching loss of 0.4 dB at 36-40 GHz and degrades the PAE by 3% at 40 GHz.

Fig. 3.12 presents ZMN plotted with the main-amplifier PAE contours at 28 GHz and 39 GHz, with the switch in the OFF and ON states, respectively, for C_6=200 fF, L_6=115 pH ($Q = 22$ at 30 GHz) and L_7=81 pH ($Q = 20$ at 30 GHz). It can be observed the Z_{MN} is located at the high PAE contour region. In the low-band setting, the simulated OP1dB and Psat are 20.3-21.7 dBm and 21-21.8 dBm, respectively, at 24-30 GHz, with a peak PAE of 29-34.6% (Fig. 3.13). In the high-band setting, the simulated OP1dB and Psat are 19-19.8 dBm and 20.8-21.4 dBm, respectively, at 36-40 GHz, with a peak PAE of 25.5-28%. If the switch is kept OFF for high-band operation, the simulated peak PAE at 37-40 GHz degrades 22.5-18.5%. Note that the Psat is not affected at 37-40 GHz by keeping the switch OFF because one can drive the PA to saturation even if not optimally matched.

The PA output impedance has been optimized for operation in the class-AB regime for both low-band and high-band operation, so as to offset the gain compression by the increase in the drain current at high power. The simulated current density is 0.04 mA/μm and 0.06 mA/μm in the small-signal regime, and 0.2 mA/μm and 0.18 mA/μm at P1dB power levels at 28 GHz and
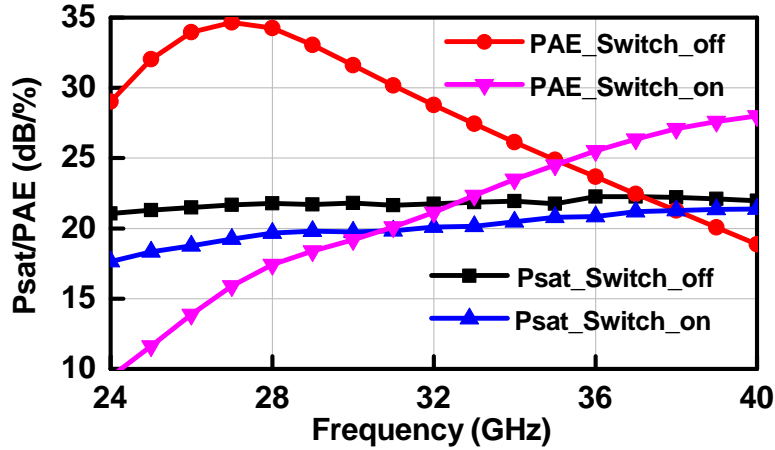
Figure 3.13: Simulated Psat and PAE at 24-40 GHz for the 2-stage PA with the three-stack load-tuning switch in the ON (low-band) and OFF (high-band) position.
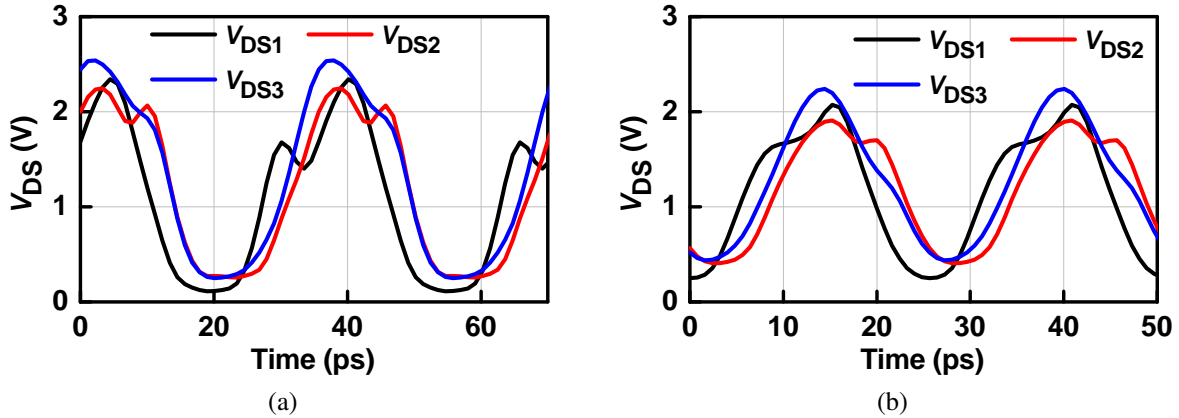
Figure 3.14: Simulated waveform of the stacked amplifier at (a) 28 GHz at P1dB of 21.3 dBm (switch ON); (b) 39 GHz at 20 dBm (Switch OFF).

39 GHz, respectively.

Fig. 3.14 presents the simulated waveform when the 2-stage PA is operating at P1dB at 28 and 39 GHz. It can be observed that the Vpp is smaller than 2.4 V and each of the main amplifier transistors VDS is nearly the same. Slight distortion can be observed because of the 2nd and 3rd harmonic content, and is due to the class AB bias mode (see [37, 38] for more detail).

To maintain the integrity of the PA-SPDT interface in the front-end design, it is also ensured that SPDT switch input impedance is well matched to 100 Ω in order to keep Z_{MN} close to the high-efficiency contours, and, also that the SPDT switch power handling does not limit the
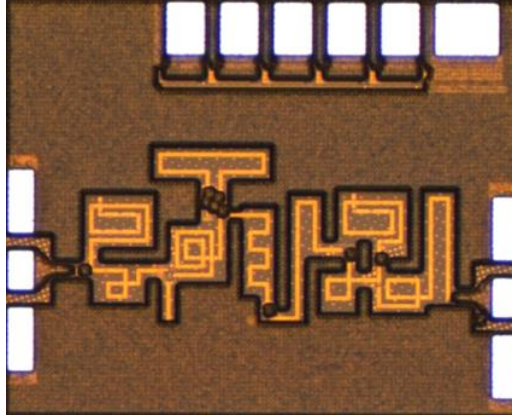
Figure 3.15: Microphotograph of LNA test chip (0.9×0.75 mm^2).

output power.

3.3 Measurements

All measurements including NF and linearity were performed in either a single-ended or in a differential-mode using on-chip probing and a 4-port Keysight N5247B network analyzer (PNA-X). The LNA and SPDT switch were first measured independently using test cells.

3.3.1 LNA

A single-end test cell was first fabricated for the LNA, as shown in Fig. 3.15, and is measured with V_{g1}=0.5 V and V_{g2}=V_{dd}=1 V, and at a dc current of 9 mA per stage (Pdc=18 mW).

The measured peak gain is 21.2 dB at 36.7 GHz with a 3-dB bandwidth of 20-40 GHz (Fig. 3.16a). The measured gain starts dropping at 38 GHz and we believe that this is due to the EM simulator underestimated parasitic capacitance of the inductors. The measured S$_{11}$ is < -10 dB at 18.3-50 GHz and S$_{22}$ is < -10 dB at 20.5-44 GHz. The measured S$_{12}$ < -40 dB, which results in a stability factor (K factor) > 1.

The LNA results in a measured NF < 3 dB at 18-42.5 GHz, a minimum NF of 2.5 dB at 24 GHz, and agrees well with simulations (Fig. 3.16b). The measured IP1dB and IIP3 are -20

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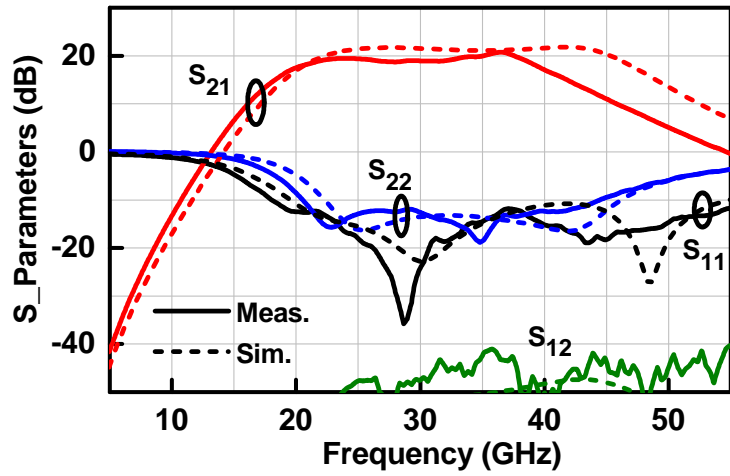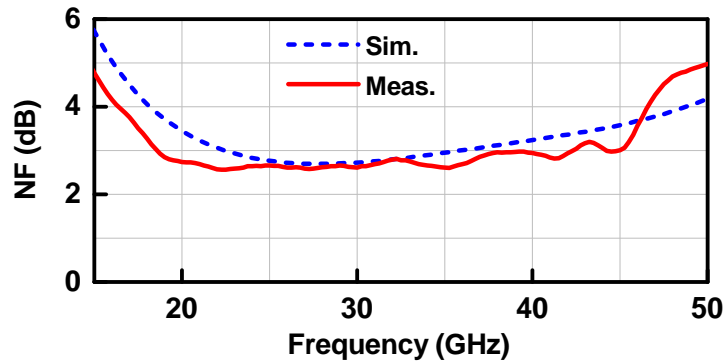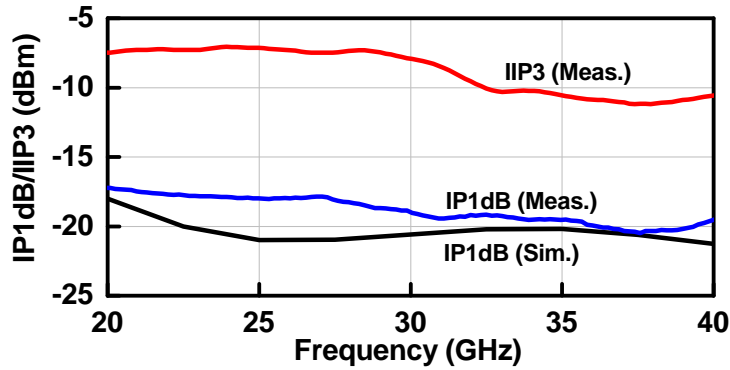
Figure 3.16: (a) Measured and simulated S-parameters of the LNA test cell; (b) Measured and simulated NF; (c) Measured IP1dB and IIP3.

to -17 dBm and -11 to -7 dBm, respectively, at 20-40 GHz, where the IIP3 is measured using

two tones with a spacing of 100 MHz (Fig. 3.16c). Table 3.3 compares the wideband LNA with

Table 3.3: Comparison with State-of-the-art Wideband LNA

Ref.	This work	[21]	[22]	[18]	[39]
Tech.	45-nm SOI	0.25-µm SiGe	45-nm SOI	22-nm SOI	22-nm SOI
BW (GHz)	20-40	29-37	24-44	24-43	22-32
Gain(dB)	21.1	28.5	20	23	21.5
NF (dB)	2.5-3	3.1-4.1	4.2-5.5	3.1-3.7	1.7-2.2
IP1dB (dBm)	-20 to -17	-32	-19 to -16	-27 to -21	N.A
IIP3 (dBm)	-11 to -7	-12.5	N.A	-19 to -13	-13.4
Pdc (mW)	18	80	58	20.5	17.3
FoM (dB)	22.1-24.2	4.6-8.1	2.6-6.5	19.7-21.9	20.3-23.1

previous millimeter-wave designs. It is observed that state-of-the-art performance is achieved with comparable FoMs to the best published LNAs.

3.3.2   SPDT

A single-ended SPDT switch test cell was fabricated and characterized (Fig. 3.17a). For all measurements, 1 V and -1 V are used as turn-on and turn-off voltages, respectively. The measured loss is < 0.8 dB and < 1 dB in the Tx and Rx modes, respectively, up to 40 GHz, with each port matching at < -10 dB up to 45-50 GHz (Fig. 3.17b-c). At 28 GHz, the measured IL is only 0.66 dB and 0.76 dB in the Tx and Rx modes, respectively. The Tx-Rx isolation is higher than 25 dB in the Tx mode and 22 dB in the Rx mode, up to 50 GHz.

The SPDT power handling is measured using the PNA-X and an external power amplifier. The compression of the external power amplifier is calibrated out. The measured Rx-mode IP1dB is 14 dBm and the Tx-mode IP1dB is 21-22 dBm, both being 3-4 dB lower than simulations (Fig. 3.17d). This may be due to the simulation tool which not model the switch P1dB accurately.

Table 3.4 compares the asymmetrical SPDT switch with recent mm-wave switches. The design achieves the lowest insertion loss with comparable IP1dB and Tx-Rx isolation. It is clear that the optimized *L-C-L* matching network resulted in wideband performance and low loss.

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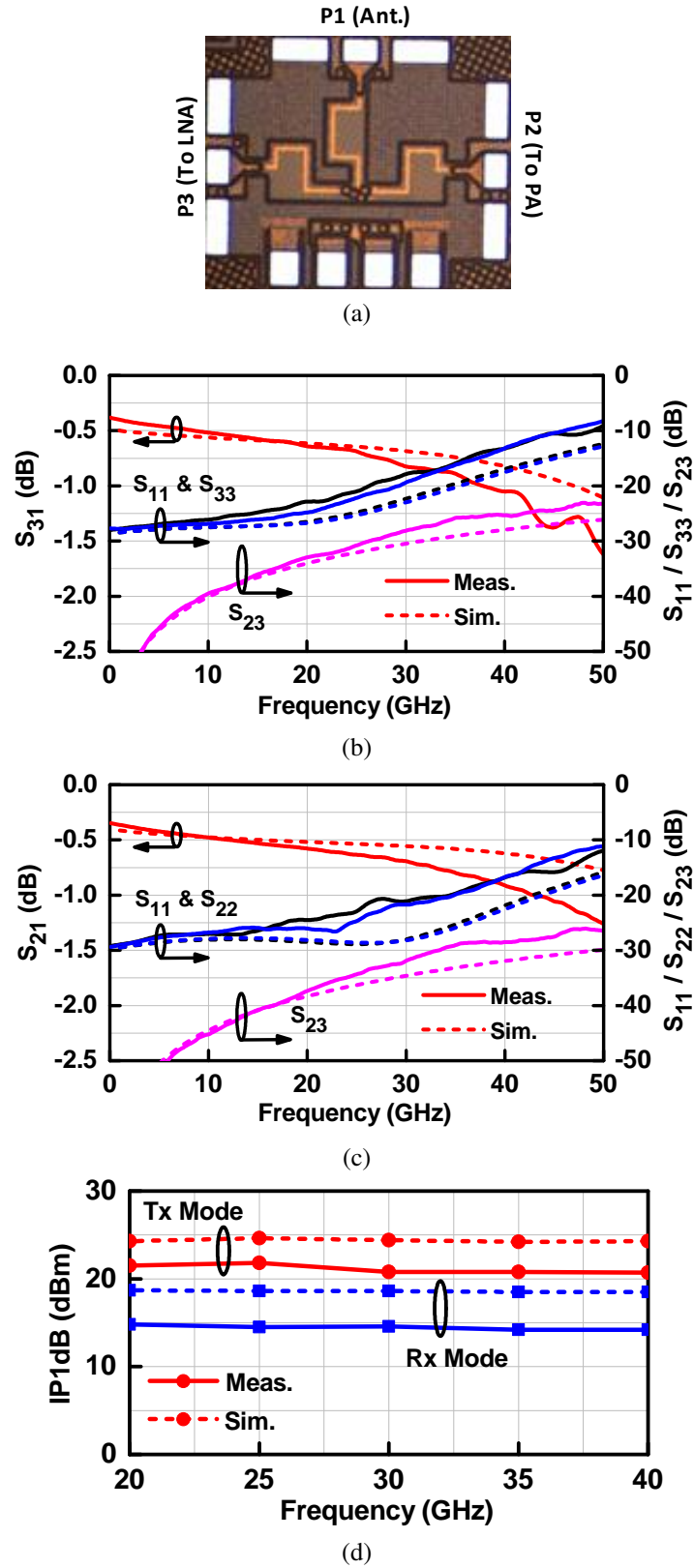
Figure 3.17: (a) Microphotograph of the fabricated single-end SPDT test chip (0.64×0.52 mm²); Measured SPDT S-parameters (b) Rx mode; (c) Tx mode; (d) Measured IP1dB in the Tx and Rx modes (single-ended).

Table 3.4: Comparison with Wideband SPDT(Single-Ended)

Ref.	This work	[32]	[33]	[34]	[35]
Tech.	45-nm SOI	40-nm SOI	45-nm SOI	45-nm SOI	0.12-μm SOI
1 dB BW (GHz)	DC-50	DC-40	DC-50	DC-35	DC-45
IL @28/40 GHz in Tx mode(dB)	0.66/0.8	1.2/1.7	0.78/1	1.3/1.5	1.3/1.6
IL @28/40 GHz in Rx mode(dB)	0.76/1	1.4/1.9	0.78/1	1.3/1.5	1.3/1.6
Isolation at 40 GHz (dB)	>25	>20	>22	>28	>30
Tx Mode IP1dB (dBm)	21-22	21.1	29	7.1	10.5

3.3.3 Front-End Rx Mode

Fig. 3.18a presents a micro-photograph of the differential front-end chip with a size of 2.1×1 mm^2 including pads. In the Rx mode, the measured peak gain is 19.3 dB with a 3-dB bandwidth of 19.7-40 GHz (Fig. 3.18b). The input matching (S_{22}) is < -10 dB at 19-45 GHz and the output matching is < -9 dB. The measured common-mode gain is < 1 dB over the entire frequency range. The results agree well with the independent LNA and SPDT switch measurements done on the test cells. The Rx mode NF cannot be measured due to the fully differential structure, but it can be deduced from the LNA and SPDT test cells, and is < 4 dB at 18-40 GHz. The measured IP1dB is -16 to -13 dBm which is high for a wideband receive module. The differential LNA consumes 36 mW.

3.3.4 Front-End Rx Mode

The front-chip Tx-mode is measured using a low-band (24-29 GHz) and a high-band (36-40 GHz) setup. For low-band measurements (Fig. 3.19a), the bias conditions are: V_{b1}=0.24 V,
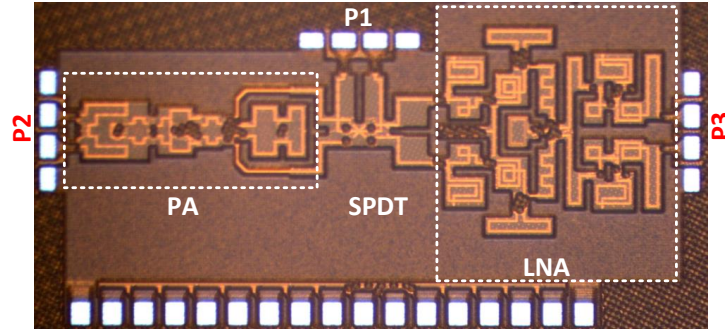
(a)
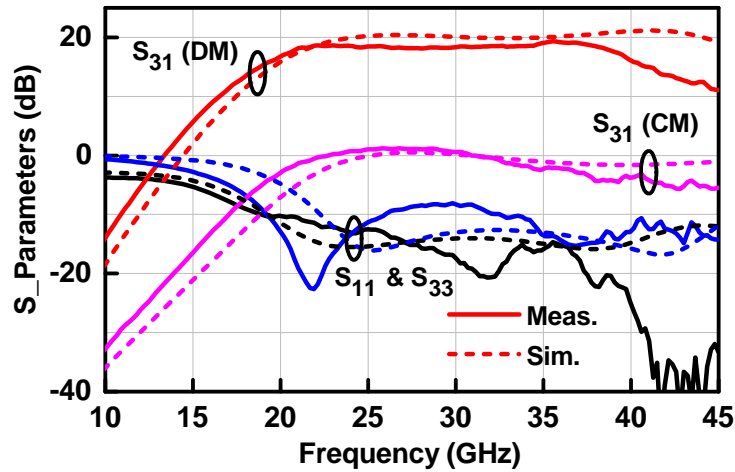
(b)

Figure 3.18: (a) Microphotograph of the fabricated front-end chip. Size: 2.1×1 mm^2. (b) Measured and simulated S-parameters of the front-end module in the Rx mode.

V_{b2}=1.3 V, V_{dd1}=2.4 V, V_{g1}=0.19 V, V_{g2}=1.45 V, V_{g3}=2.6 V, V_{dd2}=4 V, and the switch is actuated with V_{SW}=3 V. The peak gain is 17.6 dB with a 3-dB bandwidth of 22.7-30.8 GHz and includes the switch loss.

Fig. 3.19b presents the measured large-signal performance at 28 GHz, with a P1dB and Psat of 18.3 and 19.1 dBm, and a PAE of 17.8% and 18%, respectively, after the switch loss and compression. Note that there is an additional 0.7 dB switch compression included in these measurements and the PA OP1dB and Psat are actually 1.5-1.6 dB higher than the quoted values. In hindsight, a 3-stack switch would have been better at these power levels, and we were misguided by the switch simulations. The measured Psat and PAE at 28 GHz of 19.1 dBm and
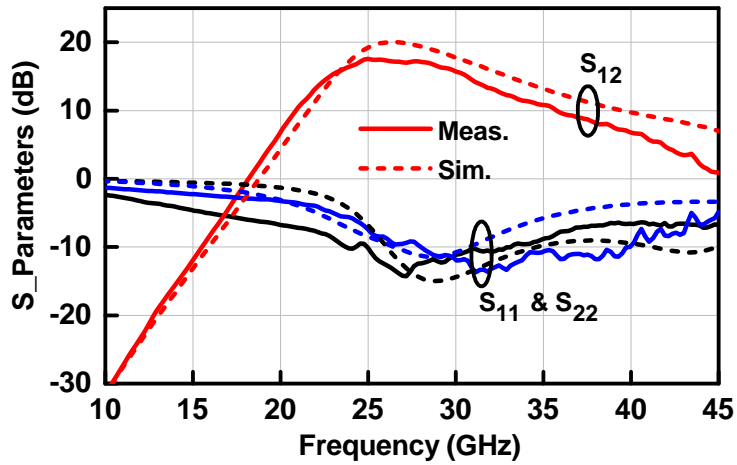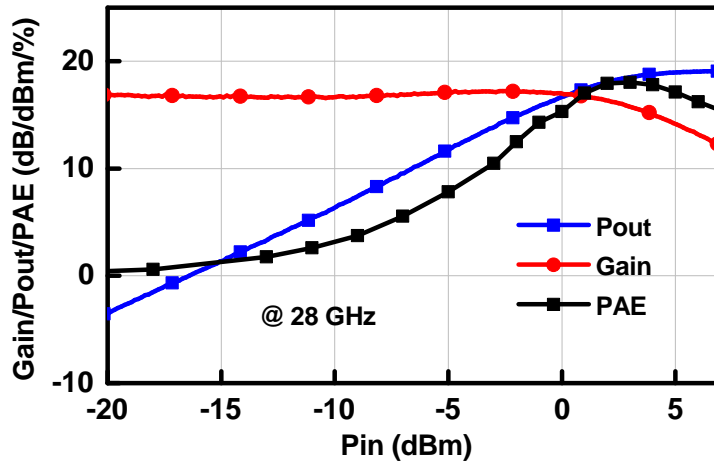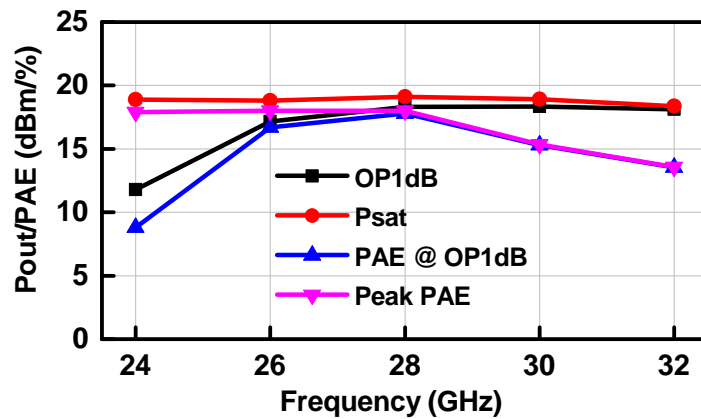
Figure 3.19: (a) Measured and simulated S-parameters for low-band setting; (b) Measured Pout, PAE, Gain versus Pin at 28 GHz; (c) Measured Pout and PAE versus frequency.

18%, respectively, compare reasonable well with simulations when one considers the switch loss and compression. In this case, the simulated Psat and PAE are 19.7 dBm (21.5-1.7 dB) and 22.7% (34% ×0.67).

Fig. 3.19c presents a summary of the large-signal performance versus frequency. The bias is optimized at a single frequency (28 GHz) and the transistors operate in class AB mode with a slight gain expansion (< 0.5 dB). However, at 24 GHz, the PA operates in a class A mode, and there is a substantial difference between its OP1dB and Psat. The measured OP1dB and Psat is 11.8-18.35 dBm and 18.4-19.1 dBm, respectively, with a peak PAE of 18-13.6%. Note that these values include the SPDT switch loss and compression. A different amplifier bias could be applied at 24 GHz to achieve better performance at P1dB, but this was not done here.

For the high-band measurements, the bias conditions are: V_{b1}=0.4 V, V_{b2}=1.5 V, V_{dd1}=2.4 V, V_{g1}=0.22 V, V_{g2}=1.5 V, V_{g3}=2.5 V, V_{dd2}=4 V, and the switch control voltage is set at V_{SW}=5 V. The measured gain is 13.6±1.5 dB at 36-41 GHz with input and output matching better than -10 dB (Fig. 3.20a). Compared to the low-band setting, the high-band gain setting increases the PA gain from 7 dB to 12.8 dB at 40 GHz, showing the effect of the switchable load-line network.

Fig. 3.20b-c presents the measured gain, and large-signal performance at 36-39 GHz. The gain shape has a slight expansion (<0.5 dB), with an OP1dB of 18.2 dBm. Due to the differential design, the PNA-X cannot drive the amplifier to P1dB and Psat levels, and therefore, these values are not quoted as the achievable P1dB and Psat. The highest Pout is 18.6-13.9 dBm with corresponding PAE of 14.1-6.7% at 36-39 GHz. Again, the 36 GHz Pout value of 18.6 dBm compares very well with simulations when considering a 1.7 dB switch loss and compression (Psim = 19.3 dBm = 21-1.7 dB). This also applies to the measured PAE of 14.1% (Psim=25%×0.67=16.9%).

In order to estimate the P1dB, the measured Pout versus Pin is plotted in Fig. 3.20d at 38 GHz. It is seen that the gain is compressed by < 0.5 dB up to a Pout of 16 dBm. This shows that the achievable OP1dB and Psat should be > 18 dBm with 3-5 dB more input power. Note that
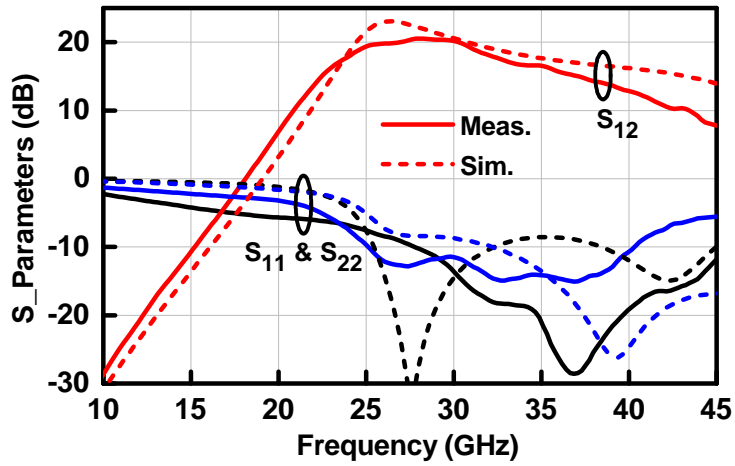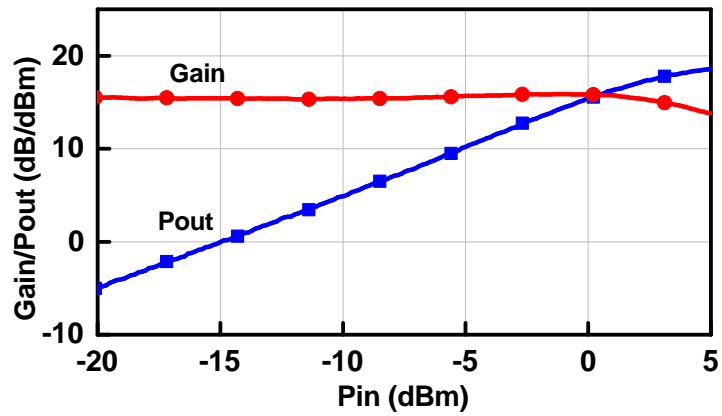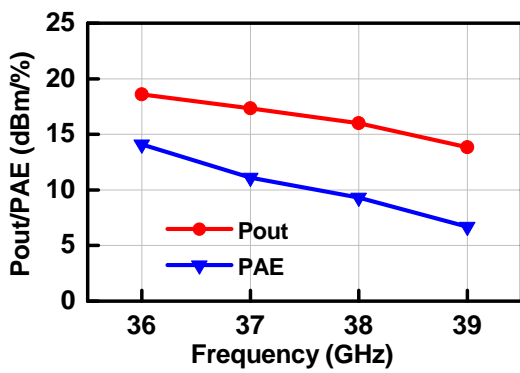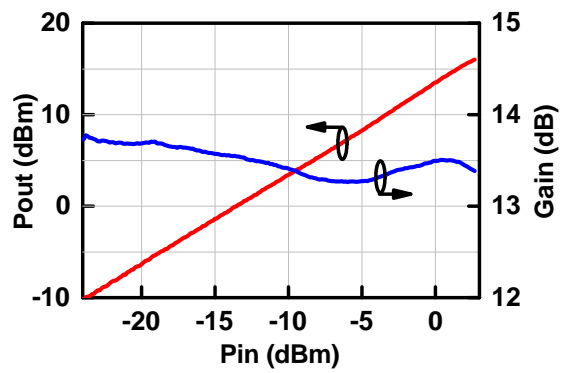
Figure 3.20: (a) Measured and simulated S-parameters for high-band setting; (b) Measured Pout vs. Pin at 36 GHz; (c) Measured highest possible Pout and corresponding PAE versus frequency; (d) Measured Pout and gain versus Pin at 38 GHz with < 0.5 dB compression up to 16 dBm.
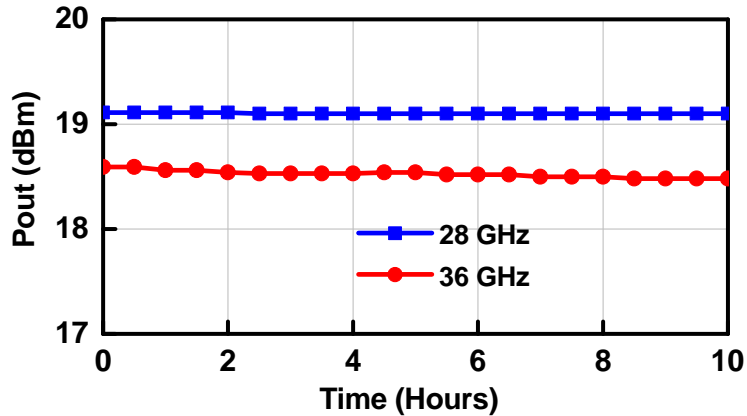
Figure 3.21: Measured output power at the P1dB level for a period of 10 hours.

this compression is due mostly to the switch and not due to the PA. Similar tests were done at different frequencies and with 0.2-0.5 dB compression at the highest quoted power.

To validate the reliability of this design, the front-end was measured in the Tx mode for > 10 hours (Fig. 3.21). In this measurement, the input power is set to achieve the highest Pout at 28 and 36 GHz. At 28 GHz, the Pout does not change over 10 hours while it changes by < 0.1 dB at 36 GHz (we believe that this is due to calibration and temperature errors). Of course, more reliability measurements should be done and this is only a single test. Finally, measurements were done with no cooling (chip placed on the wafer-probe chuck with a vacuum pull) and also with active cooling to 25°(concentrated air blowing on the chip using nozzles), and we have not seen any difference in the measured power results. At maximum power levels, the front-end consumes 450 mW, with 80 mW delivered to the load and 370 mW consumed as heat.

Table 3.5 compares the dual-band front-end with state-of-the-art designs. It can be observed that, for the Rx mode, the design achieves the widest bandwidth and comparable NF to narrowband designs. In the Tx mode, this design achieves dual-band operation and comparable output power to narrowband high-power amplifiers. The PAE is lower than what narrowband designs can achieve, but is still acceptable. In our design, the PAE is affected by the SPDT switch saturation and would be 15% higher if a 3-stack switch was used.

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Table 3.5: Comparison with Previous Millimeter-Wave 5G Front-Ends

Ref.	Integration Level	Tech.	Rx-Mode				Tx-Mode			
			Freq. (GHz)	Gain (dB)	NF (dB)	IP1dB (dBm)	Freq. (GHz) BW (GHz)	Gain (dB)	Psat (dBm)	Peak PAE
This Work	PA, LNA SPDT	45-nm SOI	19.7-40	19.3	<4 at 18-42 GHz	-15	22.7-30.8 / 36-40	17.6 / 13.6	>18.8 / >18	18 / 14.1%
[1]	Full TRX 24-antennas	28-nm CMOS	28 25-30.5	16	3.8-4.4 One-chan.	N.A	28 24-33.5	44	>14	20%
[4]	PA, LNA, SPDT PS Antenna	0.18-μm SiGe	28 27.5-31	20	4.6 One-chan.	-22	28 27.5-31	20	12.5	N.A
[12]	PA, LNA, SPDT PS, Antenna	28-nm CMOS	39 37-40	40	6-7.6 One-chan.	-39	39 37-40	46	10.2	N.A
[40]	PA, LNA, SPDT	45-nm CMOS	27 24-30	11.2	<4 at 24-30 GHz	-7.1	26 23-30.9	12	23.6	28%
[41]	PA, LNA, SPDT	22-nm FDSOI	28 24-31.3	17	<4.5 at 25-31 GHz	-22	28 N.A	16.7	13.5	33.8%
[42]	PA, LNA, SPDT PS, Antenna	40-nm CMOS	28 27-30	16.8	5.5 One-chan.	-16	28 27-30	12.4	>15	>21%

3.4   Conclusion

This chapter presented a high–power, switchable load-line millimeter-wave front-end in 45RFSOI. Three different circuits have been designed for wideband operation and optimized for high-performance. An SPDT switch with ultra-low-loss (< 1 dB in both Tx and Rx modes up to 40 GHz) and with high power handling of 21-22 dBm was first demonstrated. Next, a wideband LNA was designed and measured showing high linearity (IP1dB of -20 to -17 dBm) and low noise figure (2.5-3 dB) at 20-40 GHz. Also, a two-stage power-amplifier with a switched load-line was developed, and care was done in the switch design so as not compress the switch under high-power operations. These three blocks were then co-optimized in a high-power front-end and resulting in > 18 dBm of output power at 28 GHz and at 36 GHz, including the SPDT switch loss and compression. We believe that the methods presented in this paper will pave the way for wideband front-end designs for dual-band 5G systems.

3.5   Acknowledgment

Chapter 4

A 20-44 GHz Image Rejection Receiver with > 75 dB Image Rejection Ratio in 22-nm CMOS FD-SOI for 5G Applications

4.1 Introduction

Millimeter wave is now an important topic of research due to the increased data-rate requirements and the new 5G standard, which operates at 24-29 GHz and 37-43 GHz for fixed wireless systems, hotspots and base-station to mobile users communications. Several LNAs, PAs and phased-arrays have been demonstrated at 28 GHz and 39 GHz [1–3, 6, 8, 11, 43–50]. In general, they operate either in the 24-28 GHz band, or in the 37-42 GHz, but a new generation of phased-arrays will be coming which will operate over a wideband region, such as 24-44 GHz so as to meet all the 5G frequencies in a single aperture. Such a system will reduce size, power consumption and cost of a multiple aperture system as done today. Driven by these benefits, wideband millimeter-wave circuits, such as antennas, power amplifiers and variable gain amplifier (VGA) have been investigated [16, 51–53].

As an important block in receivers, several techniques have been proposed for wideband LNAs [19–22]. Unfortunately, the 24-43 GHz LNAs have high power consumption or high noise figure (NF). Also, their tolerance to the in-band and out-of-band interferers is poor. The in-band interferers can be handled with a high in-band LNA IP1dB and IIP3 (at a cost of additional power consumption), but the out-of-band interferers can be very large especially at 10-16 GHz due to the presence of X/Ku-band radar systems, high power point-to-point backhaul systems, and Ku-band satellite transmitters. One way to suppress these interferers is to use a sharp external passive filter on each antenna element in a phased-array. However, this will greatly increase the system cost and the filter loss will increase the system NF. Therefore, it is better to design the LNA with an integrated filter response as will be seen in this work.

Wideband receivers have also been explored in [54–59]. Most wideband receivers employ the traditional I/Q architecture for image rejection, but due to the mismatch between I path and Q path, the image rejection ratio (IRR) is limited to 30-40 dB. Also, this architecture consumes high dc power due to the presence of two mixes, two LO drivers and typically results in a higher NF due to the I/Q circuits involved.

This chapter presents a high-IF wideband image rejection receiver with very high IRR. By choosing a suitable operating frequency for the RF, LO and IF (RF: 20-44 GHz, IF: 16 GHz), the image can be rejected by the LNA without the use of external filtering. Also, a double-sideband mixer is used which greatly reduces the LO power requirements. The wideband single-sideband (SSB) receiver achieved state-of-art performance in terms of low NF, low power dissipation and the ultra-high image rejection.
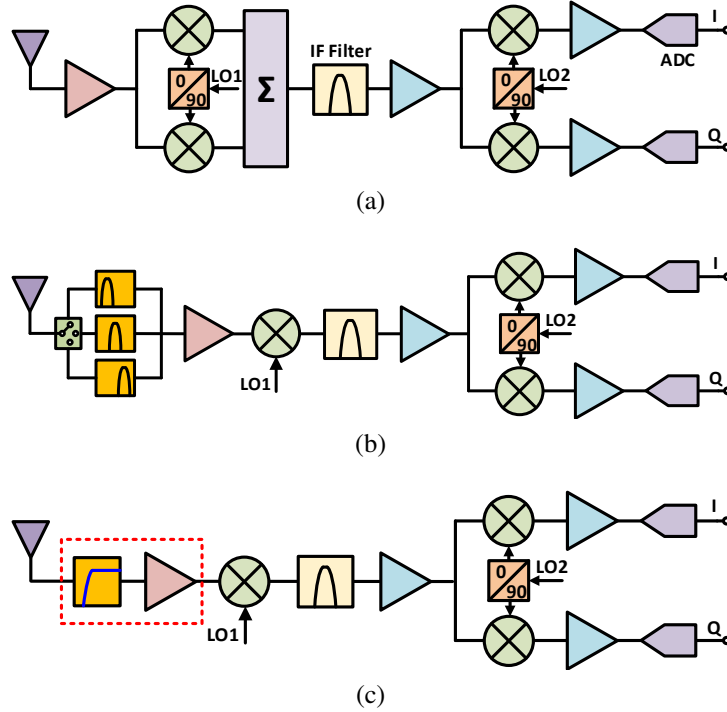
Figure 4.1: (a) Traditional low-IF single-sideband receiver, (b) output power contour vs Alternative single-sideband receiver with medium IF, (c)Proposed single-sideband receiver with high IF.

4.2 Receiver Architecture

4.2.1 Receiver Comparison

Fig. 4.1a presents a traditional single-side band receiver with a low-IF architecture. The RF signal is down-converted using a SSB mixer with I and Q paths to an IF of 2-5 GHz, and another IF down-converter is used to convert the IF signal to baseband. The Image Rejection Ratio (IRR) depends on the I/Q mismatch and is

$$\text{IIR(dB)} = 10\log\frac{(\Delta G/G)^2 + \theta^2}{4} \tag{4.1}$$

where ΔG and θ is the gain and phase mismatch between the I and Q paths. For a 50-60 dB IRR, the gain and phase mismatch should be lower than 0.05-0.02 dB and 0.5-0.2° which is very hard to achieve over a wideband frequency range and temperature, even with calibration.
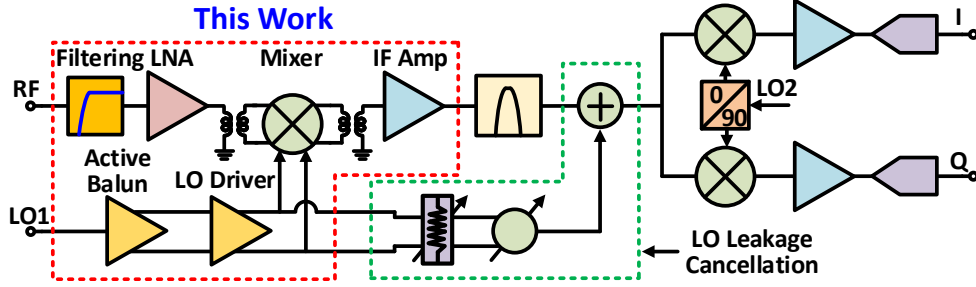
Figure 4.2: Wideband single-sideband receiver with high IF and LO leakage cancellation circuit.

An alternative SSB receiver design with mid-IF is shown in Fig. 4.1b. In this case, a filter bank is placed before the wideband receiver and a switch is used to select the RF band. This topology requires the use of an IF of 6-10 GHz and a set of high isolation filters with sharp rejection. The filter bank occupies a large area, and together with the loss of the switch network, results in a substantial increase in the system NF. Also, note that in both the quadrature (low-IF) and the switched-filter bank architectures (mid-IF), the LO chain must operate up to 36-40 GHz which increases the LO dc power consumption.

In order to alleviate these issues, a high-IF receiver is proposed for 22-44 GHz operation (Fig. 4.1c). In this case, an IF of 16 GHz is selected together with a high-pass filter having a cutoff frequency at 19 GHz. The high-pass filter is integrated within the LNA reducing its loss impact, and the image band is filtered using the receiver high-pass response with minimum NF impact. The complete structure is shown in Fig. 4.2. For an RF band given by $f_{RF,L}$ and $f_{RF,H}$, the image frequency (f_{IM}) for $f_{RF,L}$ and $f_{RF,H}$ can be written as $2f_{IF}$-$f_{RF,L}$ and $2f_{IF}$-$f_{RF,H}$, respectively. To avoid that $f_{RF,L} < f_{IM} < f_{RF,H}$ (in the RF band), should fulfill:

$$\text{maximum}\left\{|2f_{IF} - f_{RF,L}|, |2f_{IF} - f_{RF,H}|\right\} < f_{RF,L} \tag{4.2}$$

For 20-44 GHz operation, $f_{RF,L}$ and $f_{RF,H}$ are chosen to be 20 and 44 GHz, respectively, and f_{IF} is therefore between 12 GHz and 20 GHz. In this work, f_{IF} is centered at 16 GHz with a 1 GHz instantaneous bandwidth (15.5-16.5 GHz). As seen later, f_{IF} can also be centered at 15.5
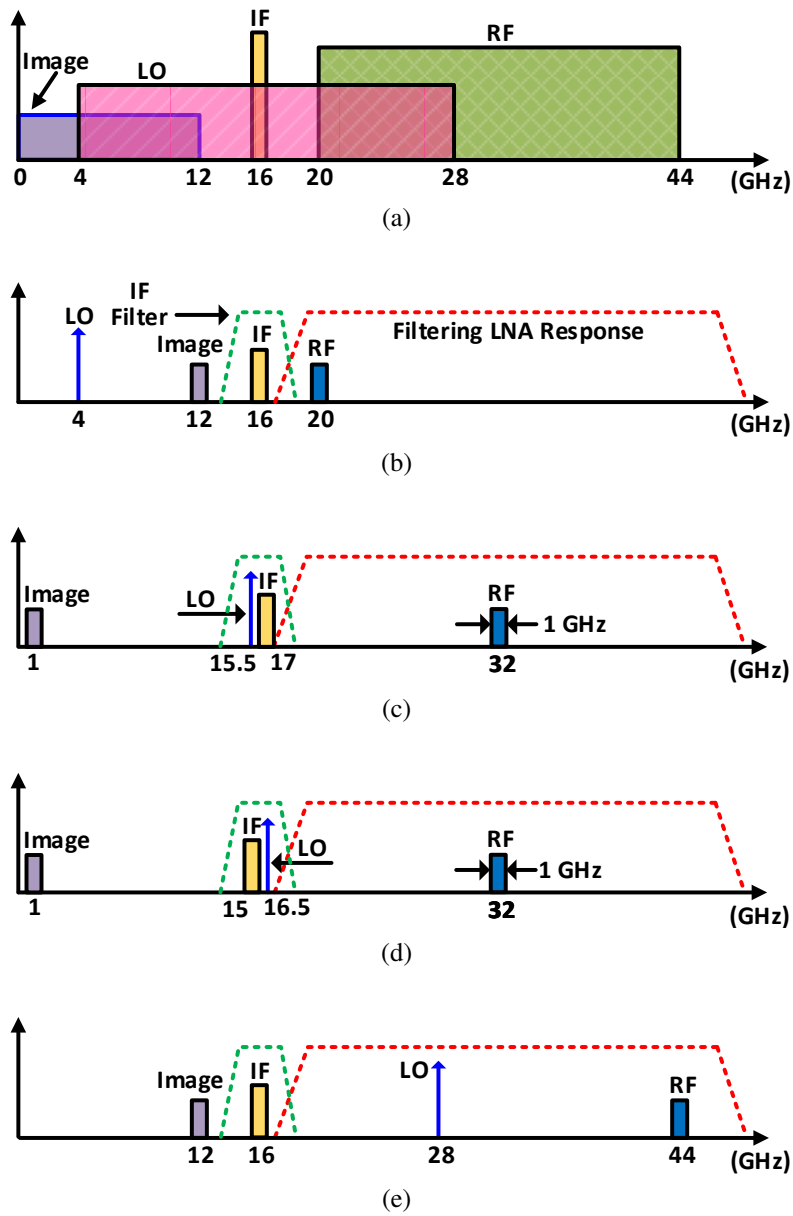
Figure 4.3: (a) Frequency plan; (b) spectrum for RF=19.5-20.5 GHz, LO=4 GHz; (c) spectrum for RF=31.5-32.5 GHz, LO=15.5 GHz; (d) spectrum for RF=31.5-32.5 GHz, LO=16.5 GHz; (e) spectrum for RF=43.5-44.5 GHz, LO=28 GHz.

or 16.5 GHz. The image frequency f_{IM} is at DC-12 GHz and the LO frequency (f_{LO}) is at 4-28 GHz, such a wideband LO can be generated by several oscillators [60] or using a low frequency commercial synthesizer with a x4 low-harmonic multiplier [56].

4.2.2   Image Rejection Consideration

Fig. 4.3a illustrates the frequency plan for 20-44 GHz operation. A high-pass filtering LNA with a cutoff frequency of 19 GHz and a rejection > 60 dB at 13 GHz is used. Fig. 4.3b-e present three frequency examples, and note the negative IF which reflects back into the positive frequency range. When the RF band is at 19.5-20.5 GHz, the LO is set at 4 GHz, and the image band is -11.5 to -12.5 GHz (11.5-12.5 GHz), as shown in Fig. 4.3b. At an RF band of 31.5-32.5 GHz, the LO is set at 15.5 GHz, the IF is at 16-17 GHz and the image band is at 0.5-1.5 GHz (Fig. 4.3c). The LO can also be set at 16.5 GHz and then the IF is 15-16 GHz, which results in an image at 0.5-1.5 GHz (Fig. 4.3d). At an RF band of 43.5-44.5 GHz, the LO is set at 28 GHz and the image is 11.5-12.5 GHz again and with high rejection (Fig. 4.3e). Note that image is never higher than 13 GHz and high-pass filter results in high image rejection.

4.2.3   LO Feedthrough Consideration

The high-IF architecture can result in a LO feedthrough issue for operation around 32 GHz. As shown in Fig. 4.3b and Fig. 4.3c, the LO can be close to the IF band and any LO leakage to the IF port can saturate the subsequent I/Q down-converter. Note that this is not relevant for 5G operation since the frequencies are 24-30 GHz (LO is far enough and can be filtered using a 16 GHz off-chip bandpass filter) and 37-44 GHz (LO is easily filtered too), but is relevant to wideband receivers covering all frequencies at 20-44 GHz. In order to remove the LO feedthrough, a symmetrical mixer is employed in the SSB receiver and results in a LO leakage signal at the IF port of < -33 dBm. Also, an LO cancellation circuit can be used as shown in Fig. 4.2 (not implemented in this work). This cancellation circuit will reduce the LO feedthrough by an additional 30-40 dB and allow the LO leakage signal to pass by the I/Q down-converter without overloading it [61]. DC cancellation is also required in the I/Q down-converter due to the LO self-mixing effects. To illustrate this in detail, consider two cases: 1) f_{RF}=31.5-32.5 GHz (1
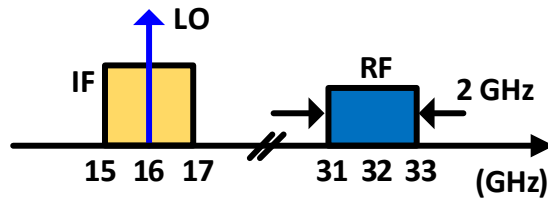
Figure 4.4: Spectrum for RF=31-33 GHz and LO=16 GHz.

GHz bandwidth), f_{LO}= 15.5 GHz (or 16.5 GHz) and f_{IF}=16-17 GHz (or 15-16 GHz). The LO leakage is 500 MHz away from the IF band and can be filtered out using either the IF filter or the base-band filters and DSP techniques in the modem, 2) f_{RF}=31-33 GHz: This is the most severe case with f_{LO}=16 GHz and f_{IF}=15-17 GHz (Fig. 4.4). In this case, the LO leakage signal is in the middle of the IF band and can generate DC offsets in the I/Q down-converter which need to be removed using DC cancellation techniques. In conclusion, for standard 5G operation, the high-IF is an excellent alternative and does not suffer from LO feedthrough issues. For wideband operation, a LO cancellation circuit is needed at the IF port for operation around 32 GHz.

4.3   Circuits Designs

This receiver is designed in GlobalFoundries 22-nm FD-SOI, which provides 10 layers of copper and one aluminum top-layer [15]. The technology provides several types of transistors, and the super-low Vt NMOS is used in this design due to its low NF_{min} and high f_t/f_{max} (270/320 GHz).

4.3.1   LNA Design

For a transistor used in LNA design, the most important technology parameters are f_t/f_{max}, NF_{min} and R_g, with R_g being highly dependent on the gate layout. Usually a wide and multi-layer structure is used to connect the transistor fingers together to reduce R_g. However, due to design rule constraints in deep CMOS nodes, M1 metal linewidth cannot exceed 0.1 μm, resulting in
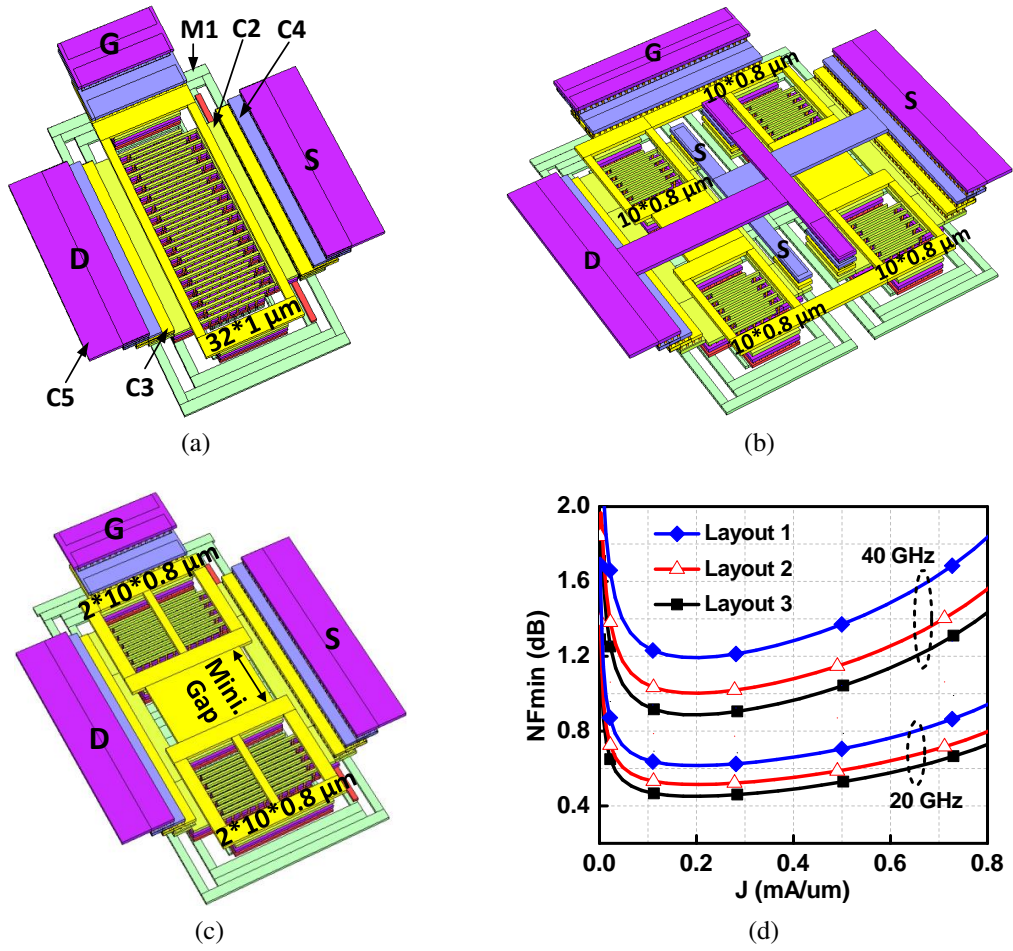
Figure 4.5: Three different layouts up to C5 for a 32 μm width transistor (a) Layout 1; (b) Layout 2; (c) Layout 3 and (d) Simulated NFmin.

a large R_g. Therefore, if a 32 μm–wide transistor is connected as in Fig. 4.5a, which employs 32 fingers each with a finger length of 1 μm, the NF_{min} is relatively high due to an increased R_g. In order to reduce R_g, four smaller transistors can be connected in parallel, with each a width of 8 μm. Also, it is best to stack the M1 to C3 layers first and then use the thick and low-loss C3-C5 layer for the routing (Fig. 4.5b). However, each transistor still has a long interconnection metal which is used to connect the back gate and the body. To further reduce R_g, multi-number of vertical gate fingers connection is provided in this technology, which eliminates part of the interconnection stack and allow the transistors to be placed closer to each other, as shown for a 2x2 cell (Fig. 4.5c).
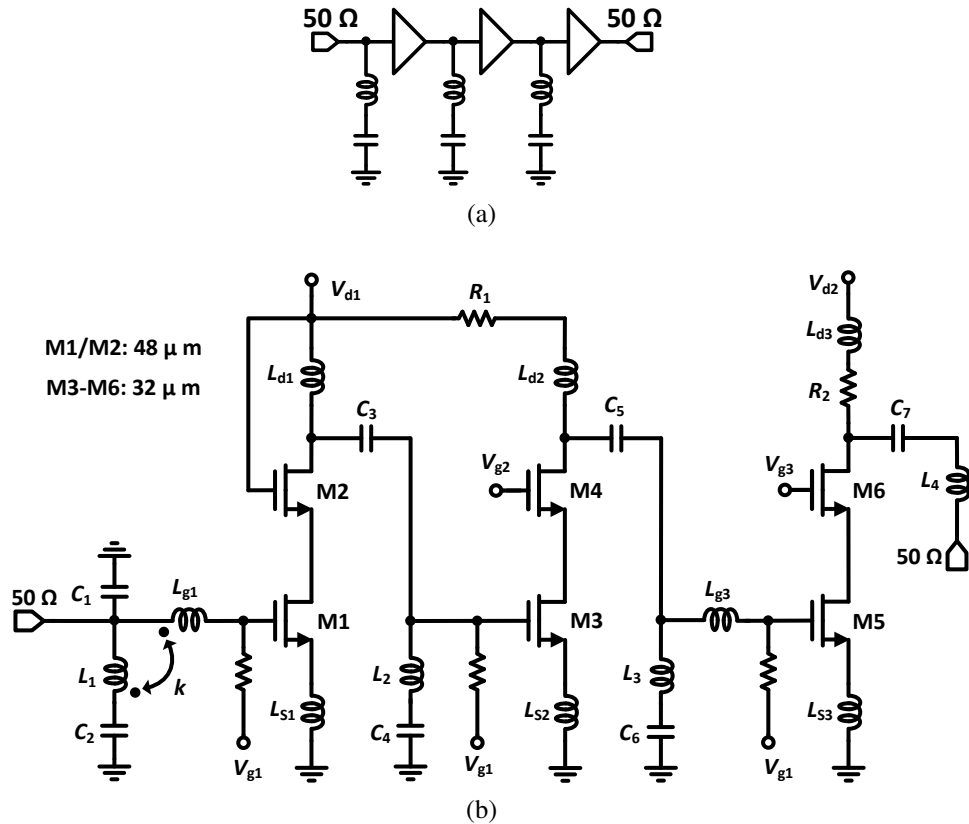
Figure 4.6: (a) Filter/amp/filter distributed topology; (b) LNA schematic.

The simulated NF_{min} of the three layouts are shown in Fig. 4.5d. It can be observed that layout 3 exhibits the lowest NFmin, and is 0.45/0.88 dB at 20/40 GHz, with a current density of 0.15-0.25 mA/μm. In this layout, the 32 μm transistor is realized using 4×8 μm wide transistors. A 48 μm transistor is also realized using 4×12 μm transistors in a 2x2 cell and is used in the LNA design.

To reject the X/Ku-band interferences and the DC-12.5 GHz image, two topologies can be chosen. The first one places a third-order high-pass filter before the amplifier, while the second one uses a filter/amplifier/filter distributed topology, as shown in Fig. 4.6a. The second topology results in lower system NF by distributing the third-order filter into the amplifier inter-stage matching networks. Fig. 4.6b presents the LNA schematic with an embedded high-pass filter. At each gate, a shunt-series LC notch filter is used with a resonant frequency of 13 GHz for high

Table 4.1: LNA Component Values (H or F)

L_1	L_{g1}	L_{s1}	L_{d1}	L_2	L_{s2}	L_{d2}	L_3	L_{g3}	L_{s3}	L_{d3}
400 p	400 p	100 p	220 p	400 p	20 p	300 p	400 p	400 p	20 p	200 p
L_4	C_1	C_2	C_3	C_4	C_5	C_6	C_7	R_1	R_2	
400 p	75 f	430 f	152 f	430 f	100 f	430 f	230 f	20 Ω	50 Ω	

rejection. Series resistors are added at the shunt drain inductor of the 2nd and 3rd cascode stages for wideband response. Note that the relatively large resistor used in the third stage has minimal effect on the LNA NF, and provides wideband output matching.

The input match is realized by source degeneration and a ladder-based transformer which introduces multiple resonant points for wideband impedance matching. The output matching is also realized using a second-order matching network. One order is created by the shunt inductor and the shunt parasitic capacitor, while the second order is formed by the series inductor and cap. Fig. 4.7a presents the simulated input matching versus k. When $k=0$, one obvious pole is at 37.5 GHz and the other obscure pole is around 28 GHz (due to limited inductor Q of 16 at 30 GHz). When k is increased, the two poles are split resulting in a wide matching bandwidth but also a higher matching ripple. A $k=0.2$ is used in the wideband LNA with poles located at 22 and 44 GHz. A bandstop filter is thus embedded in the input matching network without deteriorating its performance.

However, due to the limited Q of the inductors, the rejection level is not enough if only a first-order bandstop filter is utilized. Therefore, we implemented a third-order bandstop filter in the LNA by placing three different bandstop filters at the input of the three cascode stages. This also reduces their effect on the LNA NF. Fig. 4.7b presents the simulated S_{21} with different bandstop filter orders. If L_1/C_2 is used, S_{21} is -15 dB at ~13 GHz and the gain shows a peaked single-pole response. When L_1/C_2 and L_2/C_4 are both used, S_{21} is -30 dB, and this dual-pole network changes the gain shape to a flat response with a sharp cutoff. When L_1/C_2, L_2/C_4 and L_3/C_6 are all used, S_{21} is < -40 dB at < 15 GHz, and the gain shows > 60 dB rejection at < 15 GHz when compared to the passband response.
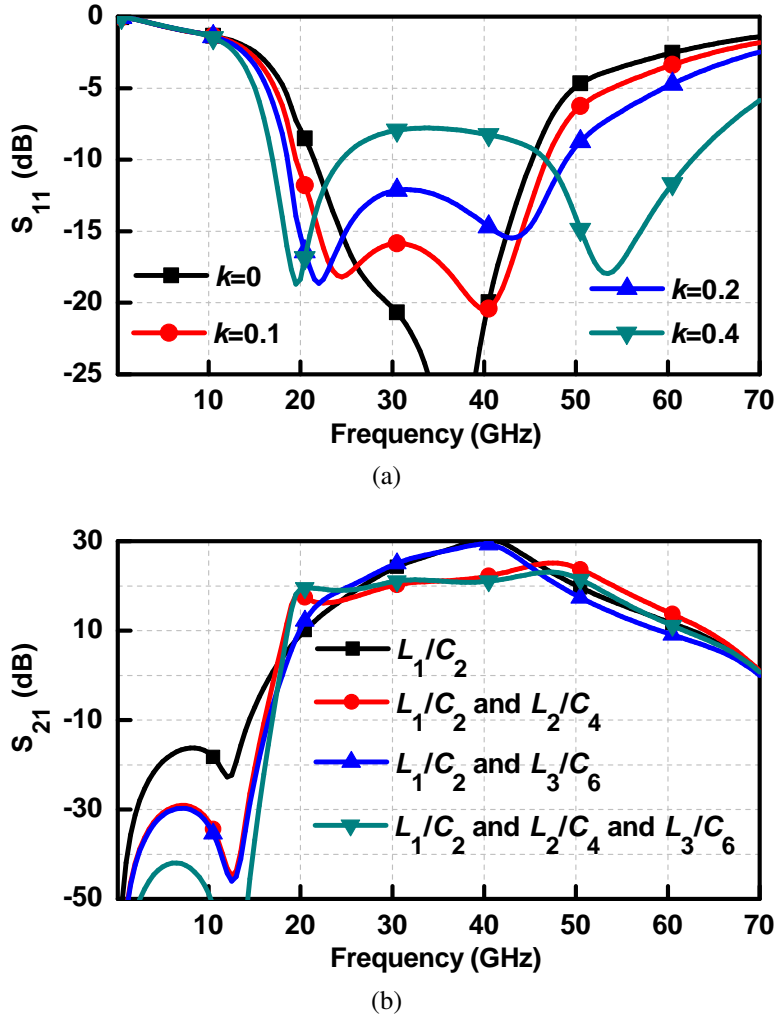
Figure 4.7: (a) Simplified input matching versus k; (b) Simulated S_{21} response with different filter order.

The overall wideband response is realized by designing a different gain-peaking frequency for each stage, as shown in Fig. 4.8a and 4.8b. Since the shunt bandstop LC increases the NF at low frequencies and the transistor has intrinsic higher NF at higher frequencies, the first stage peaks at 20 and 48 GHz to keep an overall low NF over the band. The second stage is then designed to peak at 30 GHz. Thus, the first and second stage can realize a roughly flat gain and NF response at 20-44 GHz. Next, the third stage provides a wide response to increase the gain. Thus, the overall gain has a wideband response and peaks at 48 GHz.

The simulated LNA gain is 19-22 dB with a 3-dB bandwidth of 20-50 GHz. The simulated
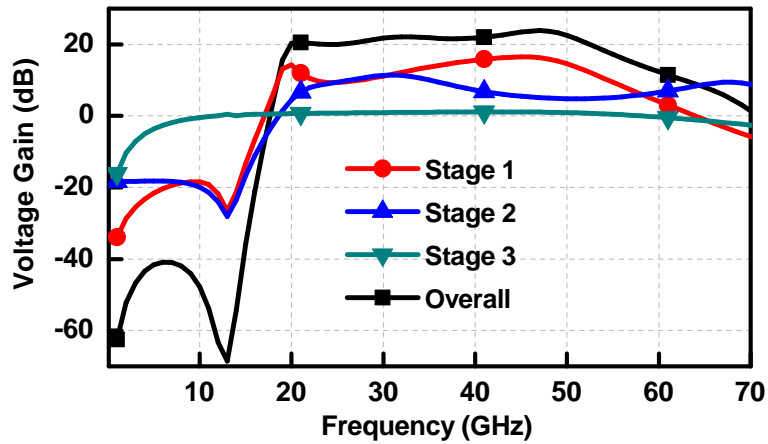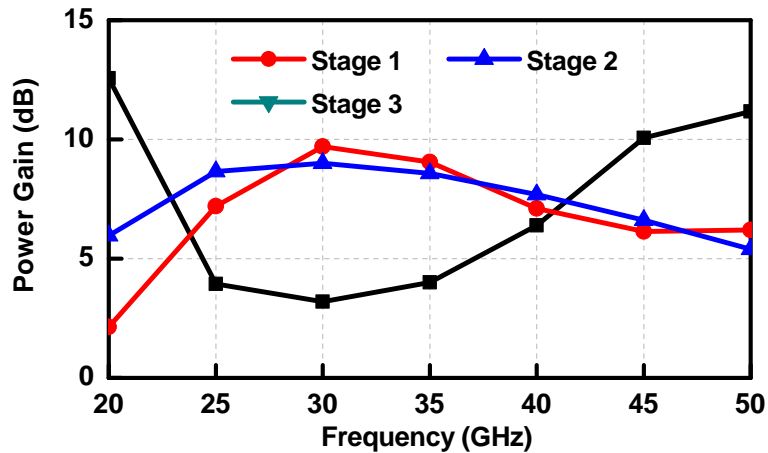
Figure 4.8: (a)Simulated voltage gain of each stage and the overall gain; (b) Simulated power gain.

NF is 3.3-4.2 dB and the simulated IP1dB is -26 to -23 dBm at 20-50 GHz. Note that the gain response at DC-13 GHz is 60 dB (or more) lower that at 20-50 GHz. The LNA can handle 0 dBm of incident power at 9-10 GHz without compression due to the high-pass response and the distributed notch, and consumes 20.5 mW.

4.3.2   Wideband RF Balun

The RF signal is then converted to a differential signal is using by a wideband passive RF balun and fed to an active double-balanced mixer. The balun is implemented using QA and
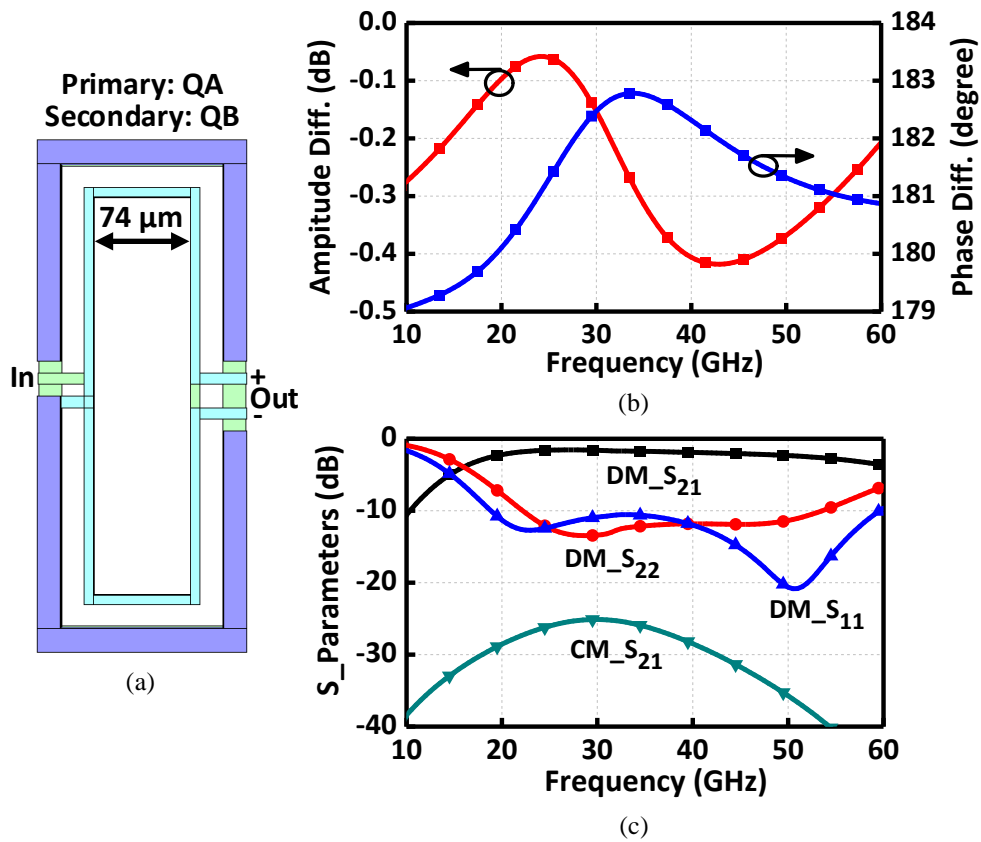
Figure 4.9: (a) Structure of the wideband RF balun; (b) Simulated phase and amplitude difference; (c) Simulated DM and CM response.

QB metal layer with a coupling ratio of k=0.7 (Fig. 4.9a), and is matched to 50 Ω using a 250 fF series capacitor. Fig. 4.9b presents the simulated amplitude and phase mismatch at the differential outputs. The amplitude difference is < 0.5 dB and the phase imbalance is < 3° at 20-50 GHz. The simulated differential-mode (DM) and common-mode (CM) S-parameters are shown in Fig. 4.9c, and an insertion loss of < 2.4 dB with > 20 dB CM rejection is obtained at 20-50 GHz.

4.3.3   LO Chain and Mixer

An active balun is used in the LO chain so as to generate a wideband differential LO signal at 4-28 GHz. Fig. 4.10a-b presents the active balun and LO driver with a de-Q inductive load for wideband operation. For the driver, a large transistor size is used in the second stage to

(a)

(b)
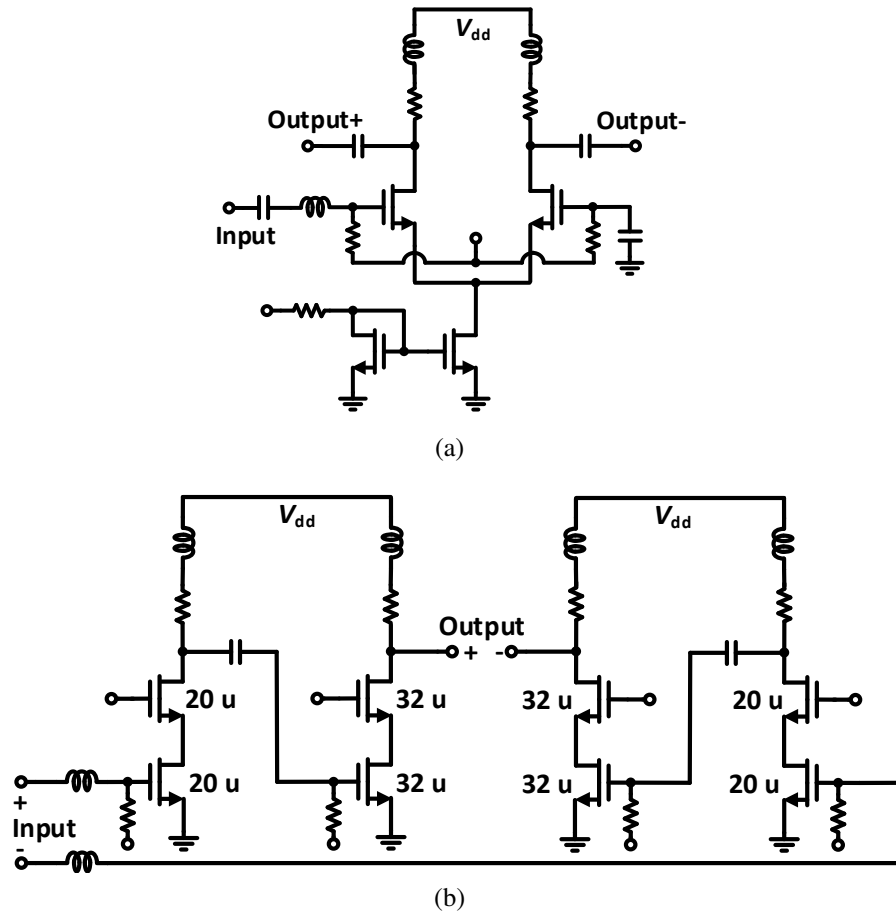
Figure 4.10: (a) Schematic of the wideband active balun at the LO port; (b) Schematic of the LO driver.

result in 0 dBm of drive power to the Gilbert-cell mixer. The active balun and LO driver consume 21.8 mA from 1.6 V (35 mW) and is half of the total receiver power consumption. The simulated LO driver gain is 18±2 dB at 0.1-45 GHz, and with a saturated output power of 1 dBm (tested using a 100 Ω differential load). This results in a voltage swing of 1.6 V_{pp} at the gates of the switching transistors in the mixer.

The LNA OP1dB is around -5 dBm, and the RF balun has 2 dB loss. Therefore, the mixer IP1dB is designed to be higher than -4 dBm so as to not to not limit the receiver linearity. Fig. 4.11a-b presents the schematic and the core layout of the wideband double-balanced mixer. The RF and LO signal paths are designed to be symmetric to minimize the LO feedthrough to the IF port. The simulated LO to IF feed-through is < -40 dB. For measurement purposes, the
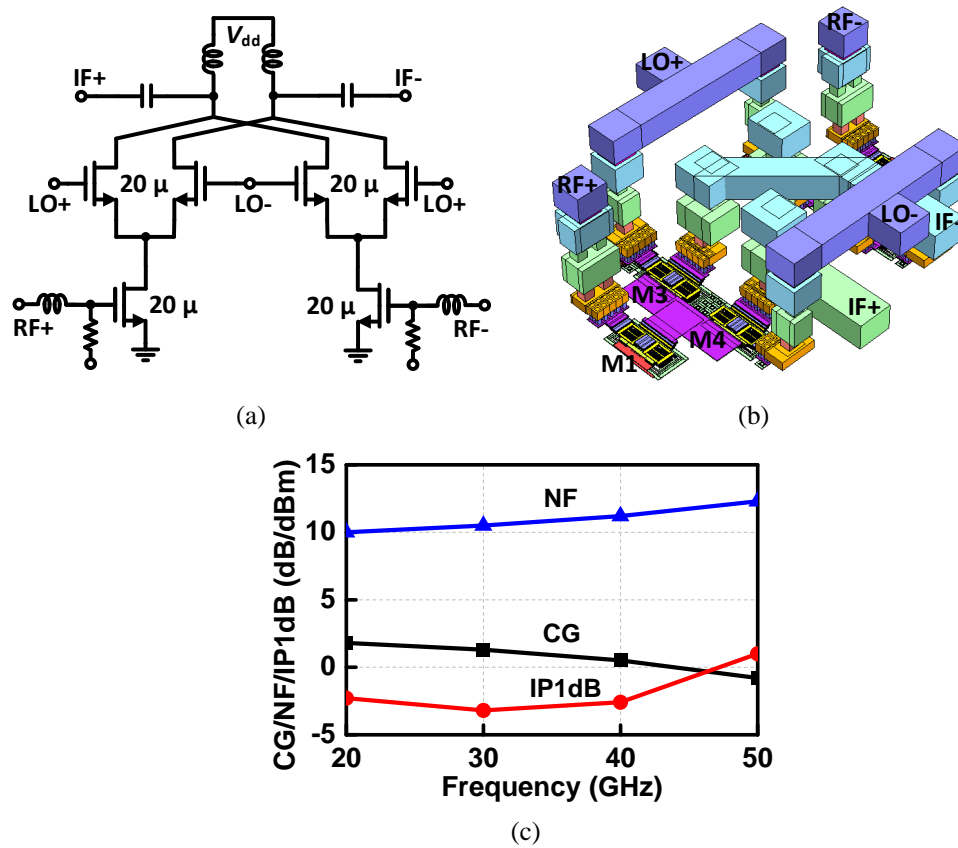
Figure 4.11: (a) Schematic of the double balanced mixer; (b) Core layout; (c) Simulated CG/NF/IP1dB using the wideband LO driver.

output mixer matching is realized using a shunt L and a series C and then followed by an IF balun (centered at 16 GHz). In a completed receiver, the differential IF will be fed into an IF filter and then into a 15-17 GHz I/Q down-converter.

Fig. 4.11c presents the simulated mixer performance with a source and load impedances of 100 Ω and 50 Ω, respectively. The mixer conversion gain (CG) is +2 to -1 dB at 20-50 GHz, and the CG slope is corrected by the LNA (which has an upward gain slope). The mixer IP1dB is -3 dBm to 0 dBm with a NF of 9-12 dB, and consumes 6 mA from a 1.6 V (9.6 mW).
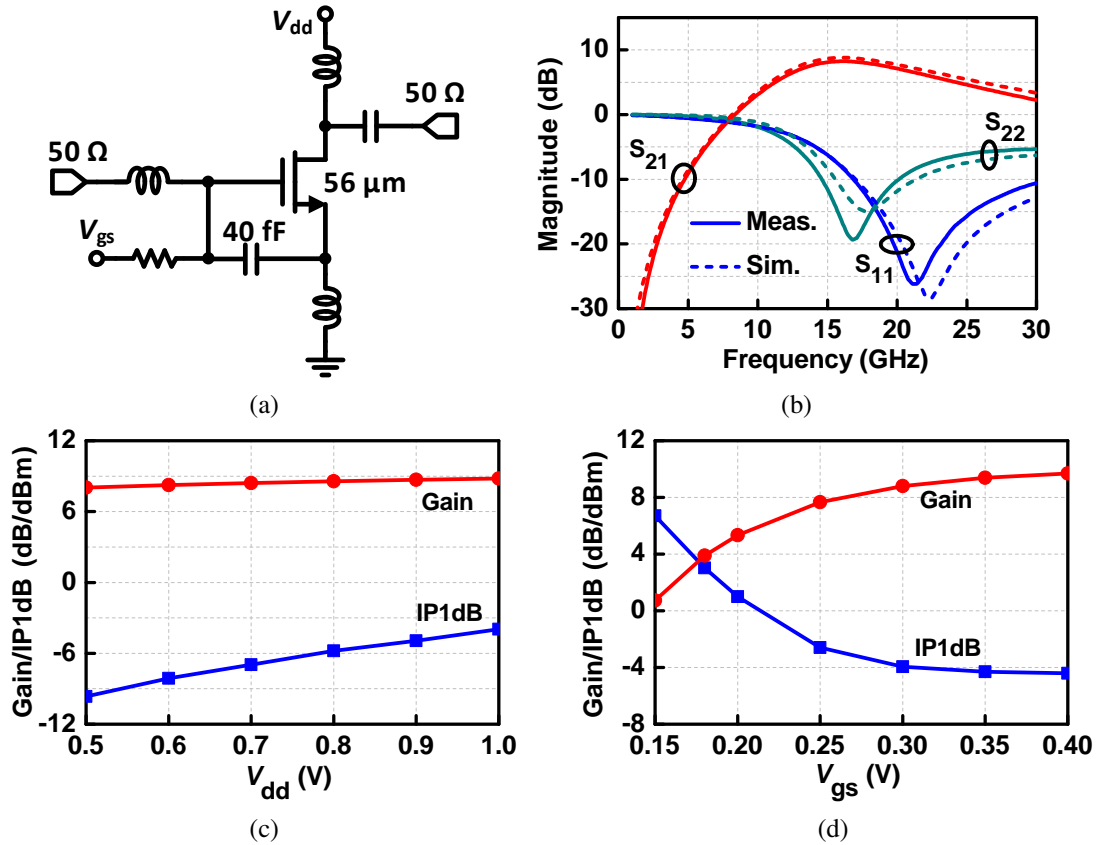
Figure 4.12: (a) Schematic of IF amplifier; (b) Simulated and measured S-parameters; (c) Simulated IP1dB and gain versus V_{dd} (V_{gs}=0.3 V); (d) Simulated IP1dB and gain versus V_{gs} (V_{dd}=1 V).

4.3.4   IF Amplifier

Since the LNA/mixer block have a total gain > 20 dB, the IF amplifier does not need to be designed for high gain, and its linearity is more important. Also, the IF amplifier gain cannot be high so as not to saturate the I/Q down-conversion mixer with any LO-to-IF feedthrough. Therefore, a simple common-source amplifier is used and a 40 fF capacitor is added between the gate and source nodes to ease the input impedance matching while keeping a small transistor size and low power consumption (Fig. 4.12a). Fig. 4.12b presents the simulated results with a peak gain of 8.7 dB and excellent input and output matching.

Fig. 4.12c presents the IF amplifier simulated gain and IP1dB versus V_{dd} at 16 GHz (V_{gs}= 0.3 V). A V_{dd} of 1 V can be used to achieve a gain of 9 dB and an IP1dB > -5 dBm, at a
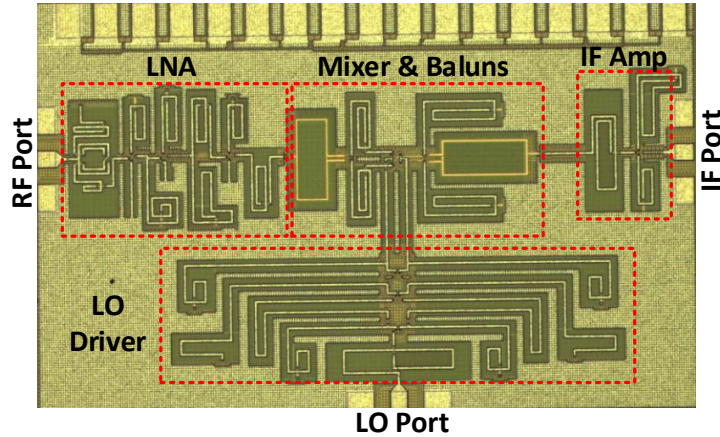
Figure 4.13: Microphotograph of the 20-44 GHz single-sideband receiver. (1.8×1 mm^2).

power consumption of only 4 mW. Note that if a differential amplifier is used, then the power consumption will be 8 mW which is still a small fraction of the receiver power budget. Additional gain and linearity control can also be achieved using gate bias (Fig. 4.12d).

4.4   Measurements

Fig. 4.13 presents a micro-photograph of the 20-44 GHz single-sideband receiver chip with a size of 1.8×1 mm^2 including pads. All measurements including NF and linearity were performed using on-chip probing and the Keysight N5247B network analyzer (PNA-X). An LNA chip is also measured independently using a test cell.

4.4.1   LNA

The biasing conditions are: V_{g1}, V_{g2} and V_{g3} = 0.4, 1 and 1.4 V, respectively. V_{d1} and V_{d2} are 1 V and 1.6 V, respectively, with a dc power consumption of 20.5 mW.

Fig. 4.14a presents the measured and simulated S-parameters. The measured gain is > 17 dB at 20-44 GHz with a peak gain of 23 dB at 40 GHz. The gain variation is ±1.1 dB at 24-29 GHz (S_{21av}=18 dB) and at 37-42 GHz bands (S_{21av}=22 dB) Measurements do not agree with the

75
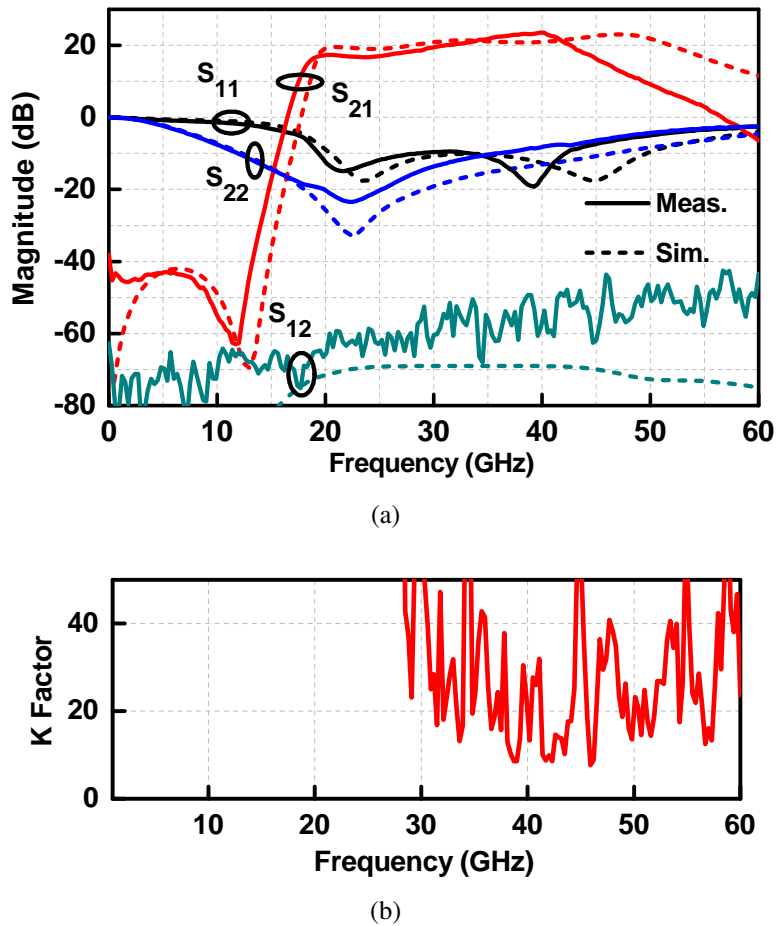
Figure 4.14: (a) Measured and simulated S-parameters of the LNA; (b) Measured K factor.

simulated response above 42 GHz, and this is due to the mandatory dense metal-fill for all metal layers, which results in higher parasitic capacitances. The high-pass elliptic filter response is clearly observed, with a gain of -20 dB at 15 GHz and < -40 dB at frequency < 13.2 GHz. Note that the LNA passband response is designed with a slight positive slope so as to compensate the negative mixer gain slope. The measured S_{12} is < -50 dB over the whole band. The measured K-factor is > 1, and indicates the LNA is unconditionally stable (Fig. 4.14b).

Fig. 4.15a presents the measured and simulated NF and with good agreement. This is also done using the PNA-X which calibrates up to the GSG probes. The measured NF is 3.1-3.7 dB at 24-43 GHz and < 4 dB at 20-45 GHz.

Fig. 4.15b presents the measured LNA linearity. The input P1dB is -20.4 to -27 dBm
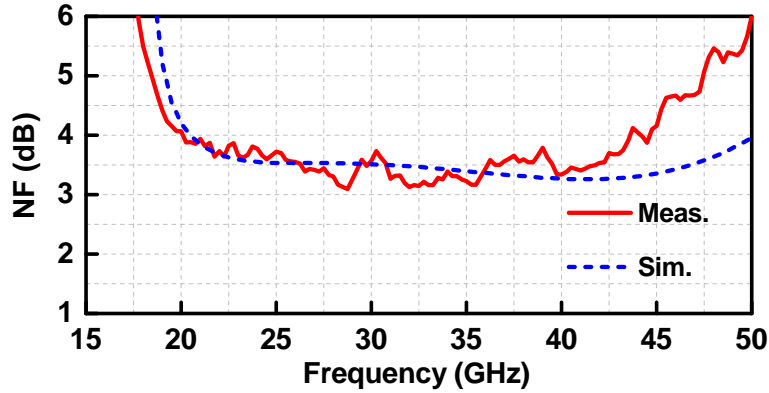
(a)
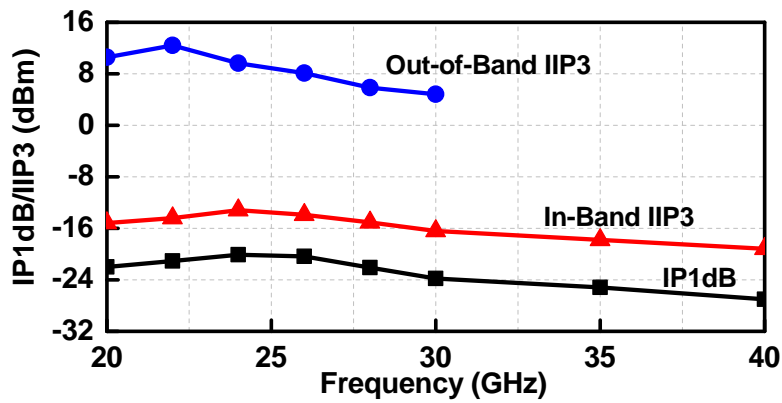
(b)

Figure 4.15: (a) Measured and simulated NF; (b) Measured input P1dB, in-band IIP3 and out-of-band IIP3.

and the in-band IIP3 is -13.2 to -19 dBm at 20-40 GHz. Due to the high-pass filtering effect, the out-of-band IIP3 is 20 dB higher than the in-band IIP3 (Fig. 4.15b). This is measured using a tone at 15 GHz (f_1) and another tone at 2-10 GHz (f_2) and taking the IM3 value at 20-30 GHz ($2f_1$-f_2).

The LNA can also be operated at lower power with competitive performance. When both V_{d1} and V_{d2} are reduced to 0.8 V, the LNA Pdc becomes 12.1 mW. In this case, the LNA exhibits a maximum gain of 18.2 dB at 40 GHz and a NF of 3.4-4.3 dB at 24-43 GHz (Fig. 4.16). The 3-pole high-pass elliptic response is conserved.

The measured IF amplifier shows a peak gain of 8.2 dB at 16 GHz, with a 1-dB bandwidth
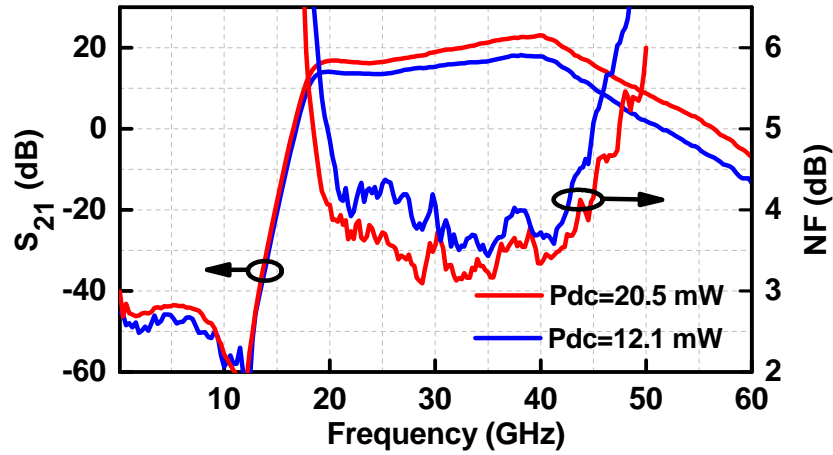
Figure 4.16: Measured LNA gain and NF versus DC power consumption.

Table 4.2: LNA Harmonic-Related IM3

f_1 (GHz)	f_2 (GHz)	IB Tones (GHz)	IM3 Tone (GHz)	P_{in} @ f_1 (dBm)	OP_{tones} (dBm)	OP_{IM3} (dBm)
27.5	28	same	27 ($2f_1$-f_2)	-30	-11.4 (Mea.)	-42.8
13.8	14	27.6 ($2f_1$)	27.2 ($2*2f_1$-$2f_2$)	-10	-34.4 (Mea.)	-109.4
				-20	-55.9 (Sim.)	<-110
				-30	-75.9 (Sim.)	<-110
9.16	9.33	27.48 ($3f_1$)	26.97 ($2*3f_1$-$3f_2$)	-4	-39.9 (Mea.)	-110
				-10	-55.8 (Sim.)	<-110
				-20	-85.8 (Sim.)	<-110
				-30	-115.8 (Sim.)	<-110

of 6 GHz (see Fig. 4.12b). The input and output ports are well matched, and the measured IP1dB is -4.2 dBm (not shown for brevity).

4.4.2 LNA Harmonics and Intermodulation Study

Another study of the LNA out-of-band linearity is shown in Table 4.2. In one case, interferers at 13.8 GHz (f_1) and 14 GHz (f_2) are used, which generate second-harmonic components at 27.6 GHz ($2f_1$) and 28 GHz ($2f_2$) with an OP_{tones} of -34.4 dBm. The resulted second-harmonic signal mixes and generates an IM3 at 27.2 GHz, which is measured to be -109.4 dBm for -10 dBm interferer power levels. The same analysis is done for -20 and -30 dBm interferer levels

Table 4.3: LNA IIP2 with Different Frequency Scenarios

f_1	f_2	f_1 (GHz)	f_2 (GHz)	$2f_1$ (GHz)	$2f_2$ (GHz)	f_2-f_1 (GHz)	f_2+f_1 (GHz)	IIP2 (dBm)
IB	IB	30	31	60	62	1	61	3.5
IB	IB	21	43	42	86	22	64	3.8
IB	IB	20	21	40	42	1	41	4.2
OB	IB	16	34	32	68	18	50	20.5
OB	IB	12	37	24	74	25	49	31.5
OB	IB	12	25	24	50	13	37	22.6
OB	IB	10	32	20	64	22	42	22.8
OB	OB	10	15	20	30	5	25	28

and the $2f_1$, $2f_2$ components are -56 and -76 dBm, respectively. This power level can be easily handled by the mixer and IF amplifier and these components will be filtered out in baseband by the modem. If the two components fall within the RF band of interest, then they cannot be filtered out. In this case, -76 dBm interferer level is 9 dB higher than the noise floor for a 400 MHz bandwidth signal (P_{in} = -174 dBm+3.5+86 = -84.5 dBm) and will degrade the system EVM.

Another case is done by having interferers at 9.16 GHz (f_1) and 9.33 GHz (f_2), which generate the third-harmonic components at 27.48 GHz ($3f_1$) and 27.99 GHz ($3f_2$). An interferer power of -4 dBm generates an OP_{tones} of -39.9 dBm and an IM3 level of -110 dBm at 26.97 GHz. In the case of -20 dBm input interferer, an OP_{tones} of -85.8 dBm is generated and is comparable to the noise floor for a 400 MHz bandwidth signal. Also, the generated OP_{tones} is much lower than the noise floor for a -30 dBm signal and has no effect. This shows that the 3-pole elliptic filter in the LNA does reduces the out-of-band 2nd and 3rd order effects and inter-modulation products.

Another interferer scenario to consider is with the IIP2 effect. In this case, two interferers (f_1 and f_2) results in f_2-f_1 or f_2+f_1 components and these can be located in-band or out-of-band. Table 4.3 summarizes some frequency scenarios. It is seen that the simulated IIP2 is 3.5-4 dBm for in-band signals, and 20-30 dBm for out-of-band signals, again showing the LNA filtering effect. The in-band IIP2 can be greatly improved in the future by using a differential amplifier.

Table 4.4: Comparison with State-of-the-art Wideband LNA

Ref.	Tech.	BW (GHz)	Peak Gain (dB)	NF (dB)	P_{dc} (mW)	FoM
[19]	0.25-µm SiGe	25-34	26.4	2.1-3.5	134	1-7.1
[20]	65-nm CMOS	15.8-30.3	10.2	3.3-5.7	12.4	2.9-10.4
[21]	0.25-µm SiGe	29-37	28.5	3.1-4.1	80	4.6-8.1
[22]	45-nm CMOS SOI	24-44	20	4.2-5.5	58	2.6-6.5
This work	22-nm CMOS SOI	24-43	23	3.1-3.7	20.5	19.7-21.9
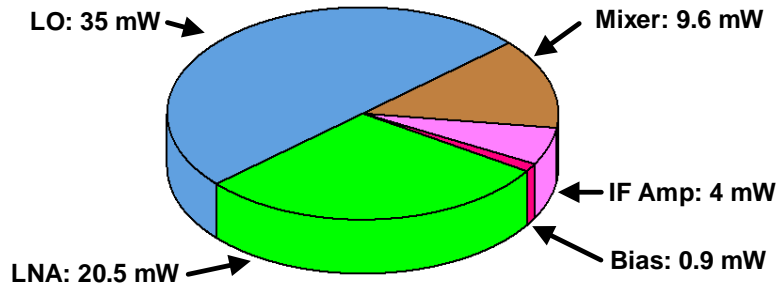
Figure 4.17: SSB receiver dc power breakdown.

Table 4.4 compares this LNA with state of the art wideband LNAs. It is observed that this work demonstrates state-of-the-art gain, NF, bandwidth and power consumption. The achieved FoM are very high compared to previous results and show the advantages of deep-CMOS SOI technology. The LNA also has a high in-band IIP3 in the 23-29 GHz range (-13.2 to -16 dBm).

4.4.3 SSB Receiver: Gain, NF, IP1dB and LO Feedthrough

Fig. 4.17 presents the power breakdown of the 20-44 GHz receiver, with a total dc power of 70 mW. The receiver measurements are shown in Fig. 4.18a-c. For the conversion gain measurements, the IF is fixed at 16 GHz, and the RF bandwidth is split into two bands: The first band has f_{RF}=16.1-50 GHz with f_{LO}=0.1-34 GHz. The second band has f_{RF}= 0.1-15.9 GHz with
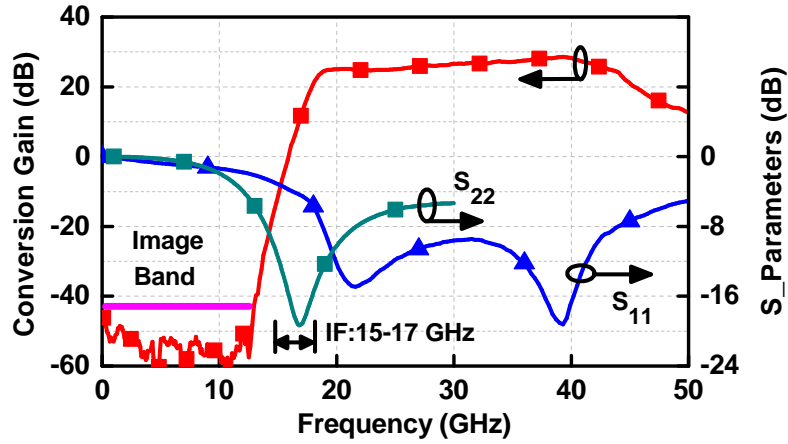
(a)
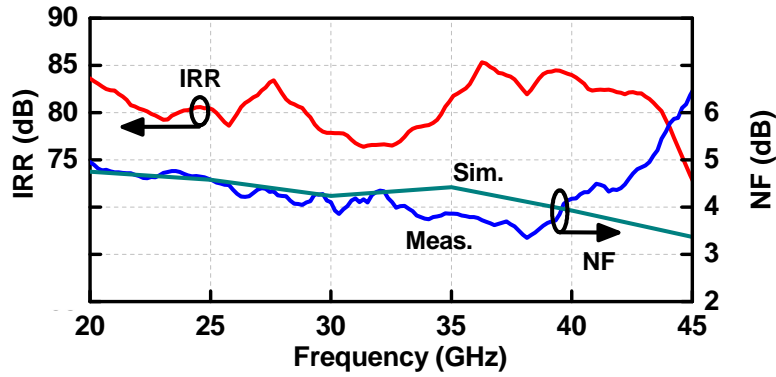
(b)
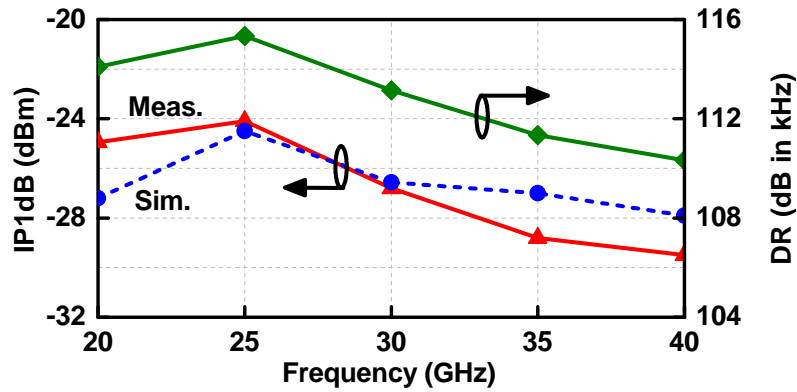
(c)

Figure 4.18: Measured (a) conversion gain and S_{11}/S_{22} of the 20-44 GHz SSB receiver; (b) IRR and NF; (c) IP1dB and dynamic range.

f_{LO}=15.9-0.1 GHz. In both cases, the LO power input to the chip is set at -10 dBm. It should

be mentioned that when f_{RF}=32 GHz, a slightly different IF is used and this does not affect the
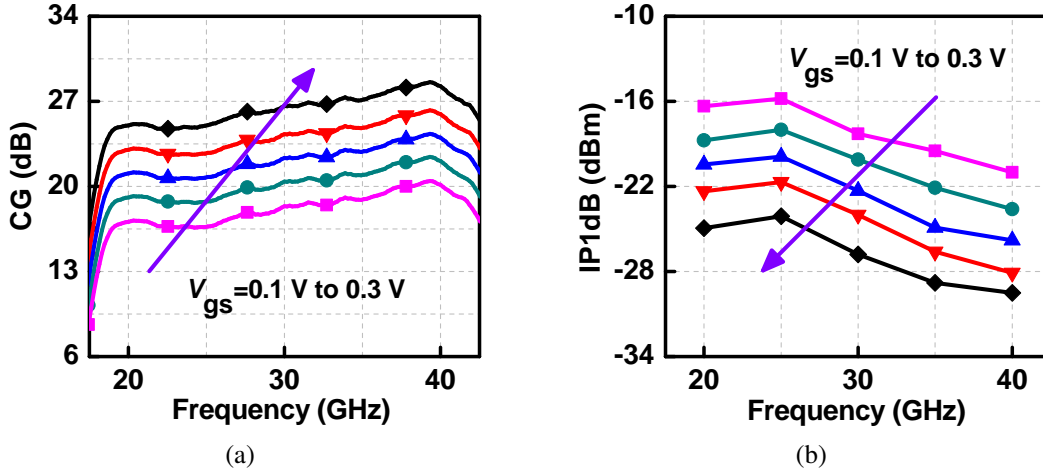
Figure 4.19: Measured (a) conversion gain and (b) IP1dB versus IF amplifier gate bias.

results.

The measured peak conversion gain is 28.5 dB and is > 24 dB at 20-44 GHz. The CG is < -20 dB at <15 GHz due to the filtering LNA response. At 20-44 GHz band, the measured IRR is > 75 dB (Fig. 4.18b). Both the input and output ports are well matched. The measured SSB receiver NF is 3.3-5 dB at 20-44 GHz, and the IP1dB is -25/-26.8/-29.5 dBm at 20/30/40 GHz, respectively. Based on the measured NF and IP1dB, and for a reference 1 kHz bandwidth signal and an SNR of 0 dB, the calculated dynamic range (DR) is higher than 110 dB, as shown in Fig. 4.18c.

Fig. 4.19 presents the measured CG and IP1dB versus the IF amplifier gate bias, and 8 dB of gain control is achieved. At the lowest gain setting, the IP1dB can be improved by $\sim$ 9 dB and the NF is nearly not affected.

Fig. 4.20 presents the measured LO leakage at the IF port, and as discussed before, the severe case occurs when f_{RF}=31-33 GHz and f_{LO}=16 GHz. The measured LO power at the IF port is < -30 dBm at 15-17 GHz. For this case, the measured SSB receiver gain and NF are 25 dB and 4 dB, respectively, and the output noise spectrum at the IF port has a level of -145 dBm/Hz. For an SNR of 25 dB (needed for an EVM < -25 dB), the signal power level at the IF port is -120 dBm/Hz, and a 2 GHz bandwidth signal, these translate to an output noise and signal power
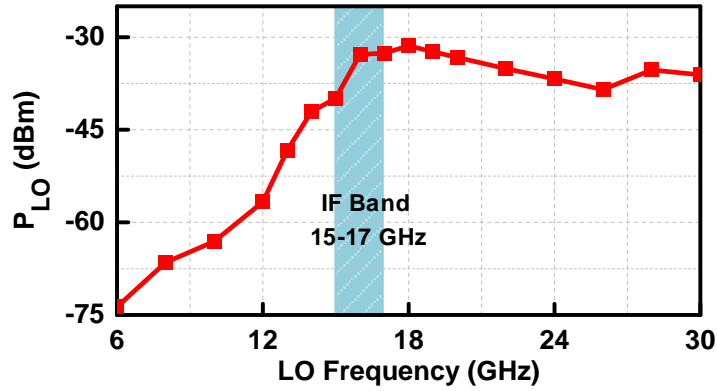
Figure 4.20: Measured LO power at the IF port.
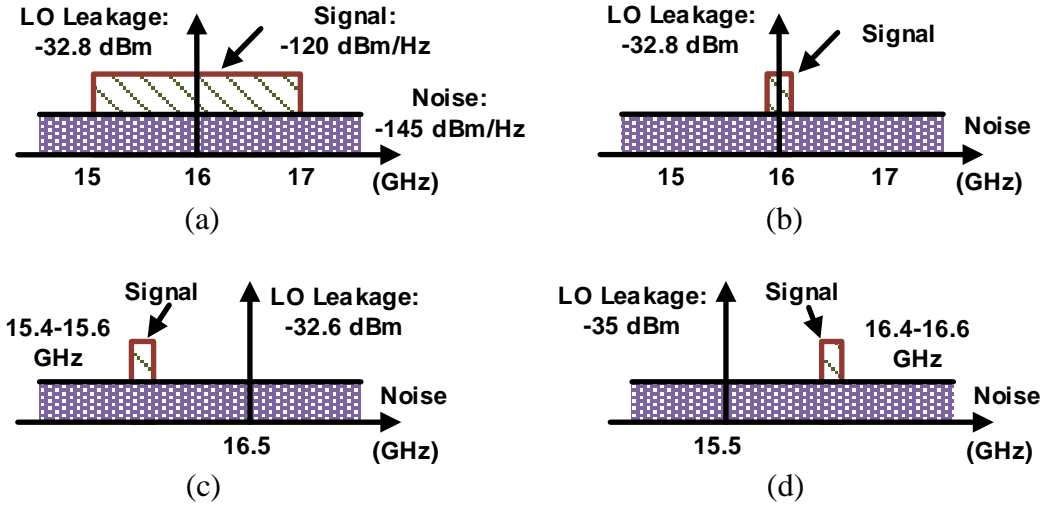
Figure 4.21: Output spectrum for different cases: (a) RF=31-33 GHz, LO=16 GHz; (b) RF=31.9-32.1 GHz, LO=16 GHz; (c) RF=31.9-32.1 GHz, LO=16.5 GHz; (d) RF=31.9-32.1 GHz, LO=15.5 GHz.

levels of -52 and -27 dBm, respectively. The LO leakage level is therefore comparable with the IF signal power, and LO leakage cancellation is required Fig. 4.21a. If the signal bandwidth is 200 MHz (RF: 31.9-32.1 GHz) and LO is still at 16 GHz, as shown in Fig. 4.21b, then the signal power is -37 dBm, which is lower than the LO leakage level and cancellation is essential. But as mentioned in Section II, for this relatively narrowband signal, a suitable LO frequency can always be chosen to avoid any LO leakage in the IF band, as shown in Figs. 4.21c-d.
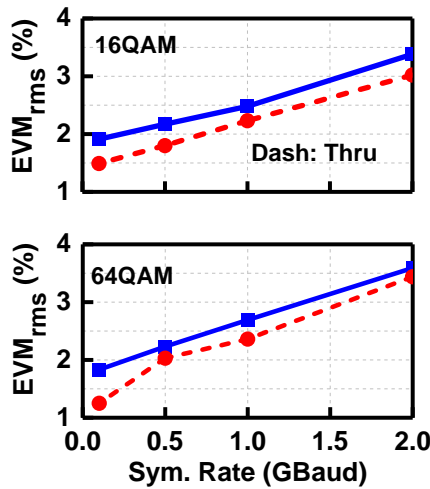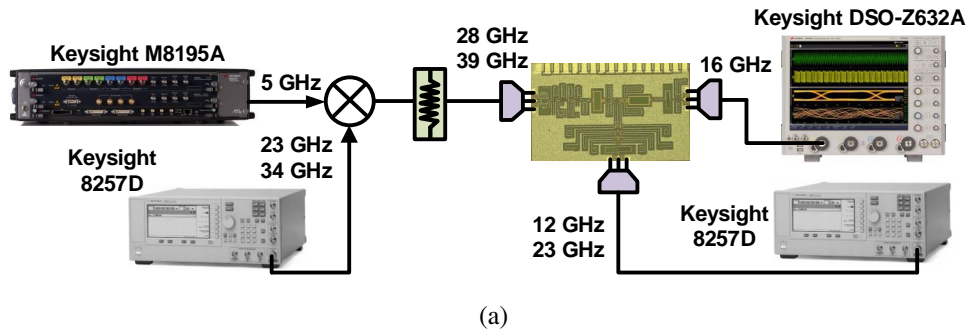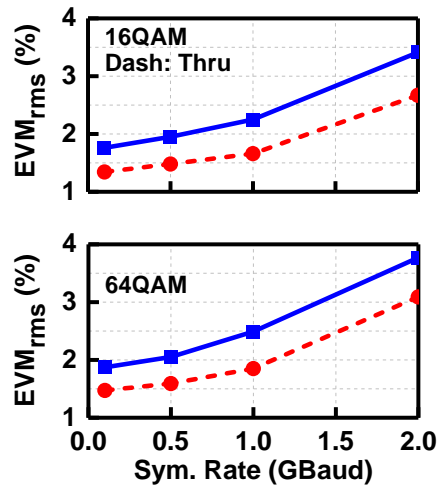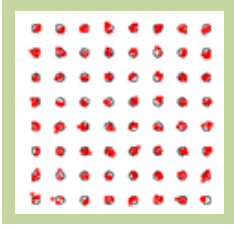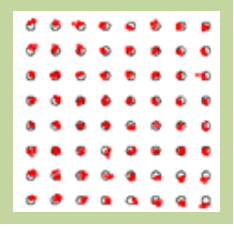
Figure 4.22: (a) EVM measurement setup. Measured EVM$_{rms}$ for different symbol rates, different modulation and 10 dB backoff from IP1dB at (b) 28 GHz; (c) 39 GHz.

4.4.4 SSB Receiver: Complex Modulation

The error vector magnitude (EVM) measurements are carried at f_{RF}=28 GHz and f_{RF}=39 GHz with different bandwidths and modulation waveforms. Fig. 4.22a presents the measurement setup: A Keysight M8195A arbitrary waveform generator is used to generate a modulated waveform (16QAM/64QAM) at a carrier frequency of 5 GHz. This waveform is then up-converted to 28 GHz (or 39 GHz) using a single-sideband up-conversion mixer with > 35 dB image rejection, and the RF signal is fed to the wideband receiver. The input signal level is set to be > 40 dB than the measurement-system output noise (at 100 MHz - 1 GHz bandwidth) so as to limit the SNR contribution to the EVM at < 1%. Also, the input signal level is always lower than

Table 4.5: Measured Constellation with 2 GHz Bandwidth of 10 dB Backoff

Constellation		
Carrier Frequency	28 GHz	39 GHz
EVM/Data Rate	3.59%/12 Gbps	3.77%/12 Gbps
Thru EVM	3.44%	3.1%

IP1dB -10 dB so as not to compress the DUT (SSB receiver), and therefore, the maximum RF signal level allowed at the SSB RF port is around -38 dBm. The receiver output is fed directly to a real-time scope (DSO-Z632A) running the Keysight VSA 89600 software for demodulation. The DSO scope results in an EVM of < 0.8% for 200 MHz waveforms even at an input power of -40 dBm. The measurement system EVM floor is between 1.2% and 1.6% at 28 GHz and 39 GHz for 200 MHz waveform bandwidth, and is measured using a short transmission line on a test chip (a thru), and includes the LO phase noise contribution of the transmit side. The system EVM increases linearly with modulation bandwidth indicating an SNR-limited system. Also, the equalizer function in the VSA software is used during the EVM measurements.

Fig. 4.22b and c present the measured SSB receiver EVM versus waveform bandwidth and modulation type at 28 and 39 GHz. It is seen that the SSB receiver EVM is very close to the system-level EVM. Table 4.5 presents the measured at 2 GHz constellations at 28 GHz and 39 GHz for a 64QAM waveform and root-mean-square filtering factor α=0.35, resulting in a PAPR=7.7 dB. The measured EVM_{rms} is 3.59% and 3.77% at 28 and 39 GHz, respectively, and are close to the thru measurements.

Table 4.6 compares the 20-44 GHz SSB receiver with start-of-art receivers. This work achieves the best performance in terms of the NF and image rejection.

Table 4.6: Comparison with Previous Wideband Receivers

Ref.	Tech.	f_0 (GHz)	RF BW (dB)	Peak Gain (dB)	NF (dB)	P_{dc} (mW)	IIR
[54]	0.18-µm SiGe	24	N.A	30	>5.6	21.5	36 dB
[55]	0.13-µm SiGe	27	24-30	39.5	4.2	1270	18 dB
[56]	0.12-µm SiGe	25	10-40	39	6.8-9.5	232	N.A
[57]	0.13-µm SiGe	30	25-45	21	6	N.A	>30 dB
[58]	45-nm CMOS SOI	34	24-44	35.2	3.2-6.1	60	>32 dB
[59]	0.18-µm SiGe	24/31	N.A	21/18	8/9.5	60	27/57 dB
This work	22-nm CMOS SOI	32	20-44	28.5	3.3-5	70	>75 dB

4.5   Conclusion

This chapter presented a wideband image rejection receiver that covers the 22-44 GHz millimeter-wave 5G band in 22-nm CMOS SOI. The LNA presents a flat gain response at 24-29 GHz and 37-43 GHz with a low noise figure and high linearity performance. A very high tolerance to the out-of-band interferers is observed, which helps to remove the lossy passive filters between the antenna and the LNA. The LNA realized a peak gain of 23 dB and NF < 4 dB at 20-45 GHz with P_{dc} of 20.5 mW, which creates a record FoM compared to the other state-of-art LNAs. The SSB receiver has a maximum small-signal gain of 28.5 dB and maintains > 24 dB gain at 20-44 GHz with P_{dc} of 70 mW. The receiver NF is < 5 dB over the whole band, with an IRR of > 75 dB. The wideband responses, low NF and high IRR makes it suitable for 5G communication systems.

4.6   Acknowledgment

The material in this chapter have been published in the following papers and the dissertation author was the first author of this material.

L. Gao, Q. Ma, and G. M. Rebeiz, "A 20-44 GHz image rejection receiver with > 75 dB image rejection ratio in 22-nm CMOS FD-SOI for 5G applications," *IEEE Trans. Microwave Theory and Techn.*, Accepted. Early Access, Mar. 2020.

L. Gao, and G. M. Rebeiz, "A 24-43 GHz LNA with 3.1-3.7 dB noise figure and embedded 3-pole elliptic high-pass responses for 5G applications in 22nm FDSOI," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 239-242, Jun. 2019.

Chapter 5

Design of 20-42 GHz IQ Receiver in 22-nm CMOS FD-SOI for 5G Applications

5.1 Introduction

There is a growing interest for utilizing millimeter-wave bands for 5G communication systems in recent years. As indispensable building blocks in the transceivers, wideband PA, LNA, VGA have been investigated. And wideband quadrature receivers also have been explored [56–58, 62–64]. The bottleneck in the wideband IQ transceiver is the generation of low amplitude/phase mismatch wideband differential IQ LO. Typically, there are several popular methods. The first one is to use divide-by-two circuits with a VCO running at twice of the LO frequency [65], which increases the design complexity and degrades the LO performance due to the two time higher operating frequency. The second one is to use 90°coupler. But it is hard to cover wideband since the 90°transmission line only valid in a small frequency range. Phase and gain mismatch increases when operating frequency is beyond the range [66, 67]. The third method is to employ poly-phase filter (PPF). For a 66% fractional bandwidth application, two stages PPF is required, which results in high loss [68, 69]. Therefore, it is still a challenge to design wideband IQ with
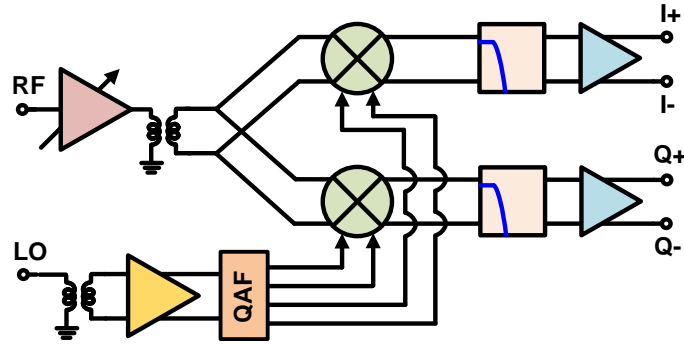
Figure 5.1: Wideband IQ receiver topology.

low loss and low amplitude/phase mismatch.

This chapter presents a low-IF wideband IQ receiver, which covers both 28 GHz and 39 GHz 5G band. The wideband IQ is generated by a quadrature allpass filter (QAF) network with low amplitude and phase mismatch, which ensure the whole receiver maintain a low IQ mismatch. The entire receiver realizes a peak CG of 22.3 dB with NF of 5.2-7 dB and IP1dB of -25 dBm.

5.2 Design

Fig. 5.1 shows the topology of the wideband IQ receiver. It includes a wideband low noise variable gain amplifier, which covers 20-50 GHz with low noise figure (NF). When the gain is reduced, the IP1dB is improved, and therefore improve the receiver linearity. After the LNVGA, a wideband double-balance mixer down converts the signal to IF. The IF section includes lowpass filters and IF amplifiers, which works at DC-6 GHz. The LO chain includes a wideband balun, which converts the single-end external LO to differential and then feeds the differential LO to wideband LO drivers. After that, a wideband QAF is used to generate the differential IQ LO to drive the active IQ mixer. This receiver is implemented in the Global Foundries 22-nm FD-SOI process.
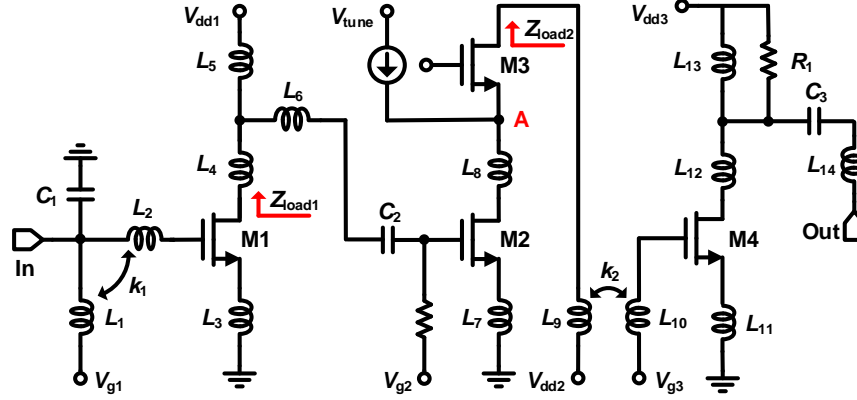
Figure 5.2: Schematic of proposed LNVGA.

Table 5.1: LNVGA Component Values

L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}
400 p	350 p	70 p	100 p	400 p	20 p	200 p	200 p	110 p	300 p
L_{11}	L_{12}	L_{13}	L_{14}	C_1	C_2	C_3	k_1	k_2	R_1
50 p	100 p	300 p	400 p	75 f	250 f	188 f	-0.2	0.55	100 Ω

5.2.1 LNVGA

Fig. 5.2 shows the schematic of the proposed LNVGA, which is a three stage amplifier. The first stage is an inductor source degeneration common source amplifier for lowest NF operation and the second stage is a cascode amplifier, which is used to implement the gain tuning. The third stage is a common source amplifier since it is easier to realize wideband output matching. By using this topology, the effect of gain tuning on NF is reduced since the NF is dominated by the first stage and the following stage noise can be suppressed by the gain of first stage. And for linearity, the cascade input third-order intercept point (IIP3) can be written as

$$\frac{1}{\text{IIP}_{3,\text{LNA}}} = \frac{1}{\text{IIP}_{3,1}} + \frac{G_1}{\text{IIP}_{3,2}} + \frac{G_1 G_2}{\text{IIP}_{3,3}} \tag{5.1}$$

Where $\text{IIP}_{3,n}$ is the nth stage IIP3. When G_2 is reduced, the $\text{IIP}_{3,\text{LNA}}$ is improved. Therefore, the dynamic range is increased. Since the gain tuning is realized at the second stage, the input and output matching will not be affected by the tuning and therefore it is convenient for
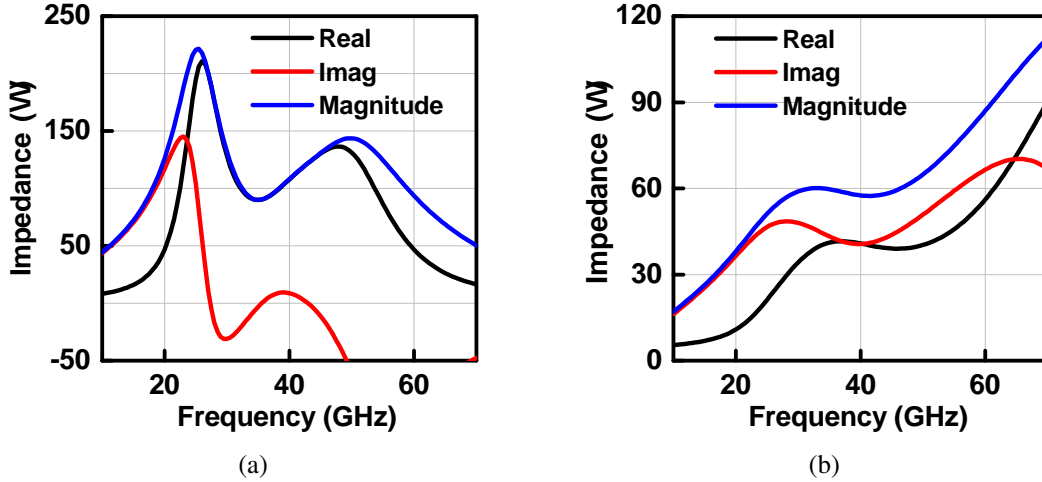
Figure 5.3: Simulated (a) stage 1 load impedance (marked as Z_{load1}); (b) stage 2 load impedance (marked as Z_{load2}).

previous and subsequent stage design.

The transistor width of M1-M3 is 48 μm and the width of M4 is 60 μm. The transistors are biased with a DC current of 6.2/6.5/7.2 mA. The current density of 0.15 mA/μm, which locates in the lowest NFmin current density range. In order to realize wideband input matching, a transformer based two stages matching network is used, which can generate two matching poles and board the bandwidth. The output matching is realized by low Q inductor and two stage matching network. Since the previous two stages provide enough gain, the effect of low Q load to NF is reduced. In order to cover the whole 5G band, each stage peaks at different frequency. But the peak frequencies need to be considered carefully. For the cascode stage, the noise increases when the gain is reduced. Therefore, to maintain a low NF during gain tuning, the first stage need provide a wideband gain. As shown in Fig. 5.2, the load of first stage is a three inductor network, which is an equivalent model of transformer and therefore exhibits dual peak impedance and provides high gain over a wide bandwidth. Fig. 5.3a shows the simulated first stage load impedance and it can be observed one peak is 27 GHz and the other peak is at 50 GHz. In order to realize gain tuning over 22-44 GHz, two peaks are also desired at stage 2. Otherwise if only one peak is realized, then the gain tuning range will be different at peak frequency and

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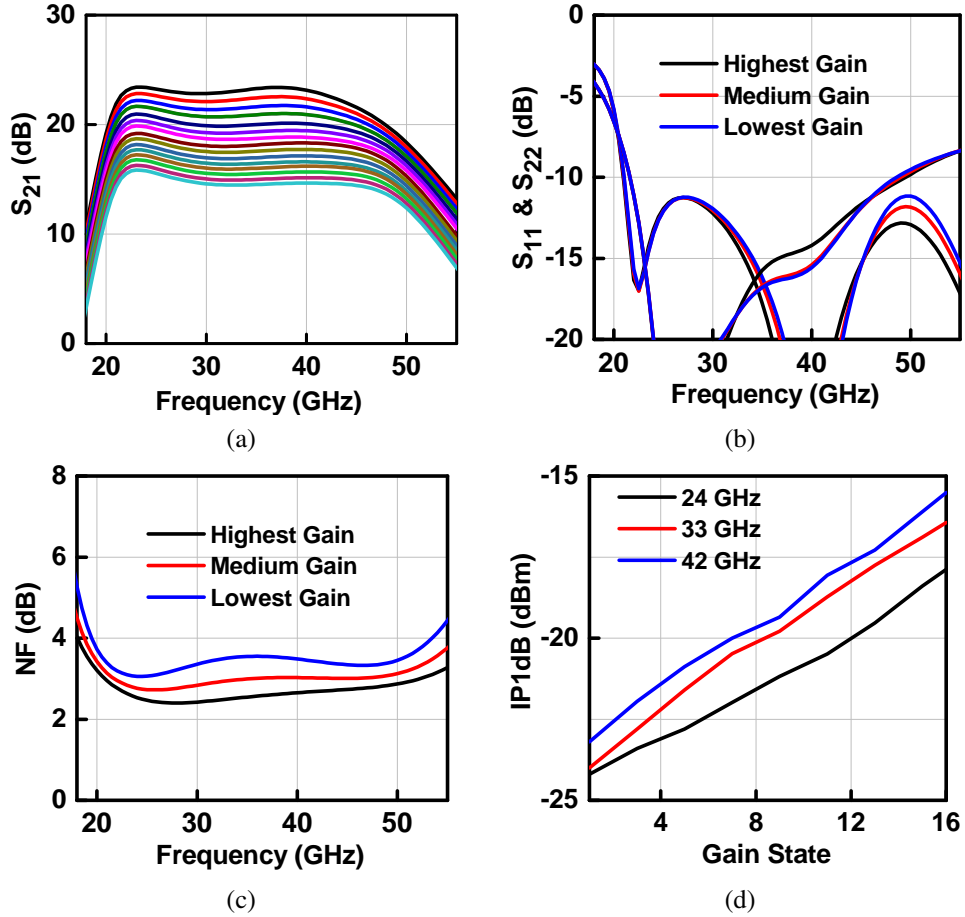
Figure 5.4: Simulated (a) S_{21}; (b) S_{11} and S_{22}; (c) NF versus gain tuning; (d) IP1dB versus gain tuning.

other frequency, which results in large ripple in the gain response or even reduce the bandwidth. Therefore, a transformer is used for the load of the tuning stage (cascode stage). Due to the double tuned transformer, the load impedance peaks at two frequencies and their separation can be controlled by the coupling coefficient (k). Fig. 5.3b shows the simulated load impedance of the second stage. Similarly, there is one peak at 30 GHz and the other one is at high frequency. Since the peak of stage 1 and stage 2 compensates each other and stage 3 exhibit a wideband flat response due to the low Q load, the three stage overall can realize a flat gain responses. The linearity is limited by last stage, therefore linearity is improved when the gain is reduced.

Fig. 5.4 shows the simulated LNVGA performance. The peak gain is 23.2 dB with 3-dB bandwidth of 20.5-47 GHz and dc power of 16 mW. The gain tuning range is 8 dB with 4 bit
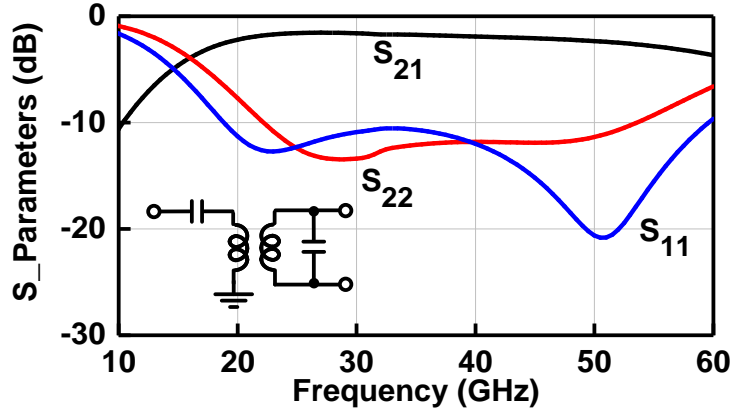
Figure 5.5: Passive RF balun simulation results.

control. The tuning range can be increased by using a large V_{tune}. The simulated S_{11} and S_{22} are < -10 dB at 22-48 GHz. At highest gain state, the NF is 2.4-3.2 dB at 20-45 GHz. At lowest gain state, the NF is 3-3.7 dB. The IP1dB is around -24 dBm at highest gain state. When the gain is reduced to lowest gain state, the IP1dB is increased to around -17 dBm. Thus, during the gain reducing procedure, the NF just increases 0.6 dB but the IP1dB is improved by 7 dB. Therefore, the dynamic range is increased. Since the OP1dB is limited by last stage, the OP1dB is nearly fixed, which does have not linearity effect of the following stage.

5.2.2 LO Chain and Mixer

After the LNA, a wideband passive balun converts the single-end signal to differential and feed to the IQ mixer. The balun is implemented by using QA and QB layer as its primary and secondary coil with both width of 4 μm. Then a series cap and a shunt cap are added to the primary and secondary stage to balance the amplitude and phase. The simulated insertion loss of the balun is < 2.4 dB at 20-50 GHz, as shown in Fig. 5.5.

The LO is provided externally and it is fed to a passive balun first. The RF is 22-44 GHz and the IF is first fixed at 2 GHz, results in a LO of 20-42 GHz. Therefore, a similar wideband passive balun is used. The differential LO is then amplified by LO driver amplifier. In
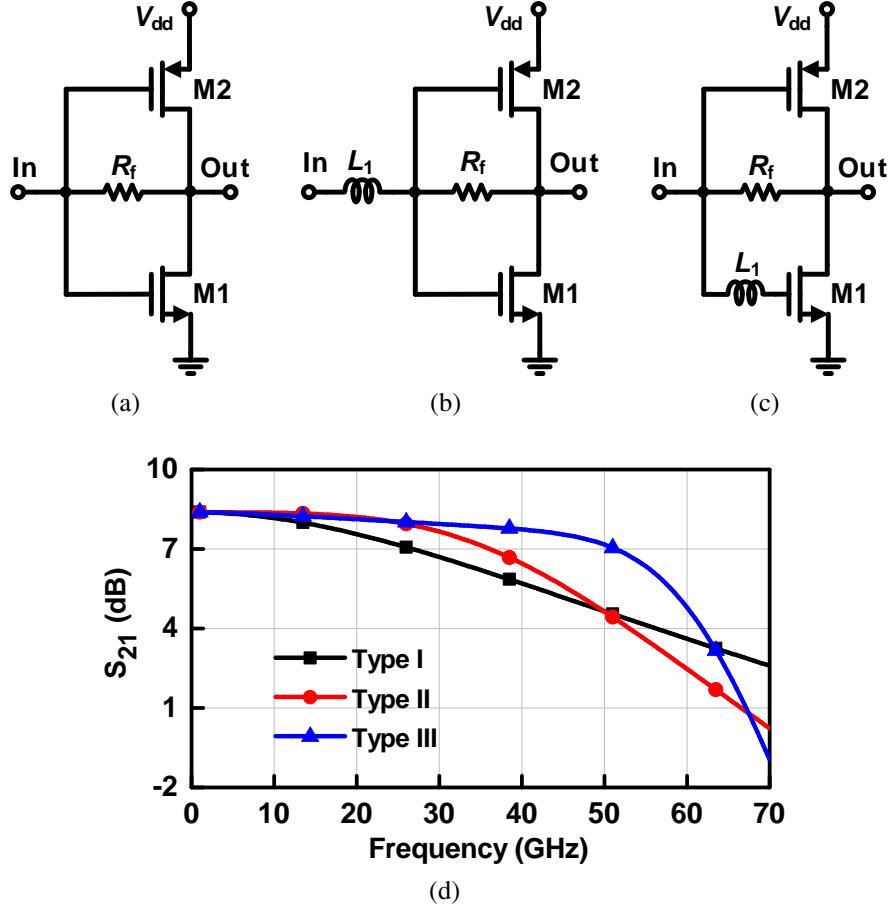
Figure 5.6: (a)-(c) Type I-III inverter amplifier structure; (d) Simulated results of these three type amplifiers.

order to cover the wideband frequency range, inverter amplifier is adopted due to its wideband characteristic and simple structure, as shown in Fig. 5.6a. However, due to the parasitic cap, the gain decreases at high frequency. And the dominate pole is at the input node due to the miller effect, which increases the input shunt cap by $A_{\mathrm{v}}C_{\mathrm{gd}}$. In order to extend the bandwidth, a series inductor can be added at the input node (Fig. 5.6b). The series inductor can resonant out the input node cap and therefore can extend the bandwidth. And the gain can be derived as [70]

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \approx \frac{1}{1 + s^2 L_1 (C_{\mathrm{gsn}} + C_{\mathrm{gsp}})} \times \frac{1 - R_{\mathrm{f}}(g_{\mathrm{mn}} + g_{\mathrm{mp}})}{1 + s R_{\mathrm{f}}(C_{\mathrm{gdn}} + C_{\mathrm{gdp}})} \tag{5.2}$$

where g_{m}, C_{gs} and C_{gd} are the transconductance, gate-source and gate-drain capacitance
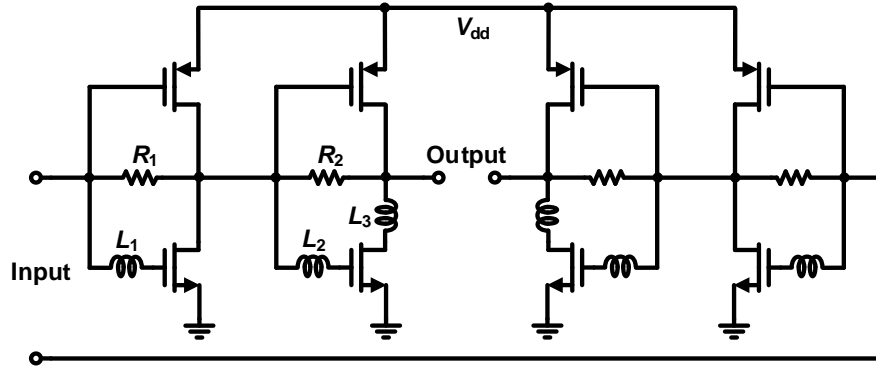
(a)
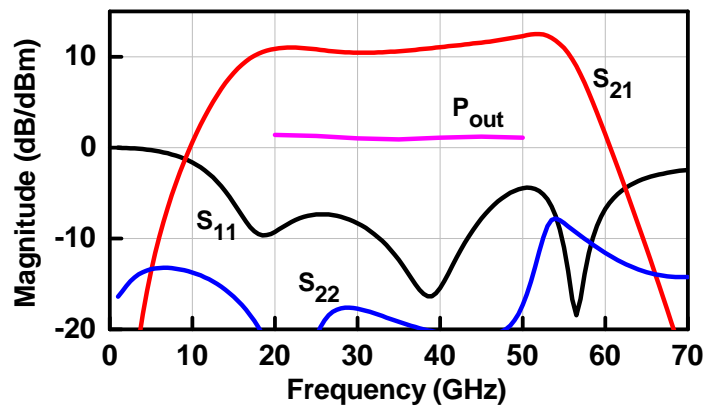
(b)

Figure 5.7: (a) Schematic of the LO driver amplifier; (b) Simulated results of LO balun and driver amplifier together.

of NMOS/PMOS. Another method to extend the bandwidth is to add the inductor at the gate of NMOS or PMOS, as shown in Fig. 5.6c, which resonant out the parasitic cap of NMOS and also can extend the bandwidth. Fig. 5.6d shows the simulated results of the three type inverter amplifiers. The original one has a 1-dB bandwidth of 24 GHz. The 1-dB bandwidth is extended to 35 GHz with type II structure and to 48 GHz with type III structure. Therefore, type III is used for the LO driver amplifier.

Fig. 5.7a shows the schematic of the LO driver amplifier. It is a two stage type III inverter-based amplifier. The PMOS transistor size is 1.4 times larger than the NMOS to balance the gm. Fig. 5.7b shows the simulated LO balun and driver amplifier result. The gain is 11.5±1 dB at 20-50 GHz and there is a gain peaking at 52 GHz, which is generated by L_3. And L_3 also

improves the output matching. With an input power of -9 dBm, the output power is around 1 dBm with dc power consumption of 22.6 mW.

After the driver amplifier, the differential LO is fed into a wideband differential IQ generation network, as shown in Fig. 5.8a and the IQ mismatch will affect the image rejection ratio, which is expressed in equation (4.1). The phase mismatch of the LO directly will show up at the converted IF signal while the gain mismatch of LO has a smaller effect of converted IF signal. Therefore, the IQ generation network can be optimized for minimum phase mismatch.

The differential IQ generation network in this design is based on quadrature all-pass filter (QAF). L and C resonant at ω_0 and the characteristic impedance is $Z_0 = \sqrt{L/C} = R_0$, which results in a network Q of 1. The transfer function can be written as

$$\begin{bmatrix} V_{I\pm} \\ V_{Q\pm} \end{bmatrix} = V_{in} \begin{bmatrix} \pm\dfrac{\omega^2 + \omega_0^2 - \dfrac{2\omega_0}{Q}j\omega}{\omega^2 - \omega_0^2 - \dfrac{2\omega_0}{Q}j\omega} \\[4mm] \pm\dfrac{\omega^2 + \omega_0^2 + \dfrac{2\omega_0}{Q}j\omega}{-\omega^2 + \omega_0^2 + \dfrac{2\omega_0}{Q}j\omega} \end{bmatrix} \qquad (5.3)$$

Based on equation (5.3), the $|V_{I\pm}|=|V_{Q\pm}|$ is realized for any ω and orthogonal phase splitting is realized at $\omega=\omega_0$ with Q of 1 and two poles locate at the same frequency. The two poles can be split by using a lower network Q. An issue of this QAF is that I/Q errors are sensitive to the load capacitance (C_L), which comes from the gate capacitance of next stage. In order to mitigate the effect of C_L, low Q network can be used [17, 71]. As shown in Fig. 5.8a, series resistor is added in the high Q branch, which can reduce the gain mismatch with the expense of higher loss but it nearly does not help with the phase mismatch. Fig. 5.8b shows the simulated phase and gain mismatch with the following three cases: C_L=0 and R=0; C_L=40 fF and R=0; C_L=40 fF and R=50 Ω. It can be observed that when C_L=0 and R=0, ω_0=35 GHz. There is no gain mismatch as expected and the phase mismatch is < 5° at 22.6-52.7 GHz. When the 40 fF load capacitance is
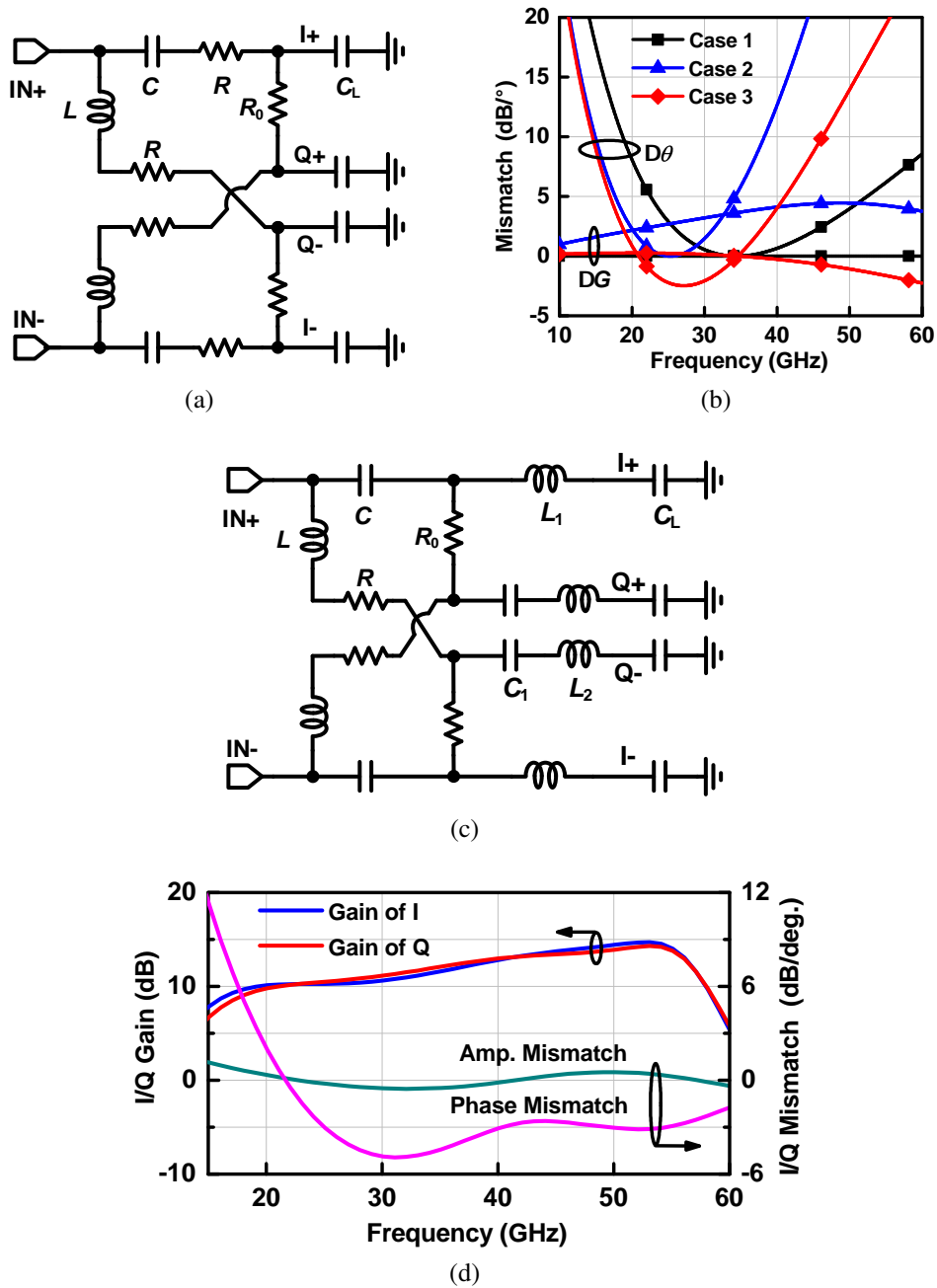
Figure 5.8: (a) Schematic of traditional QAF; (b) Simulated amplitude and phase mismatch of the QAF for different cases; (c) Modified QAF; (d) Simulated amplitude and phase mismatch.

added, ω_0 is shift to 25.3 GHz. The gain mismatch is 2-4.4 dB at 20-50 GHz and phase mismatch is $< 5°$ at 17.7-34.2 GHz. Therefore, the load cap decreases the bandwidth and also increases the amplitude/phase mismatch. By adding series R for L and C, the gain mismatch is reduced to 1
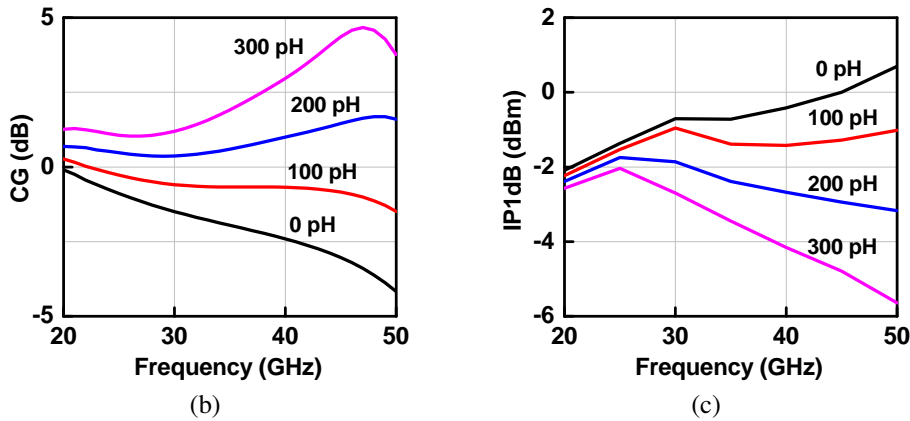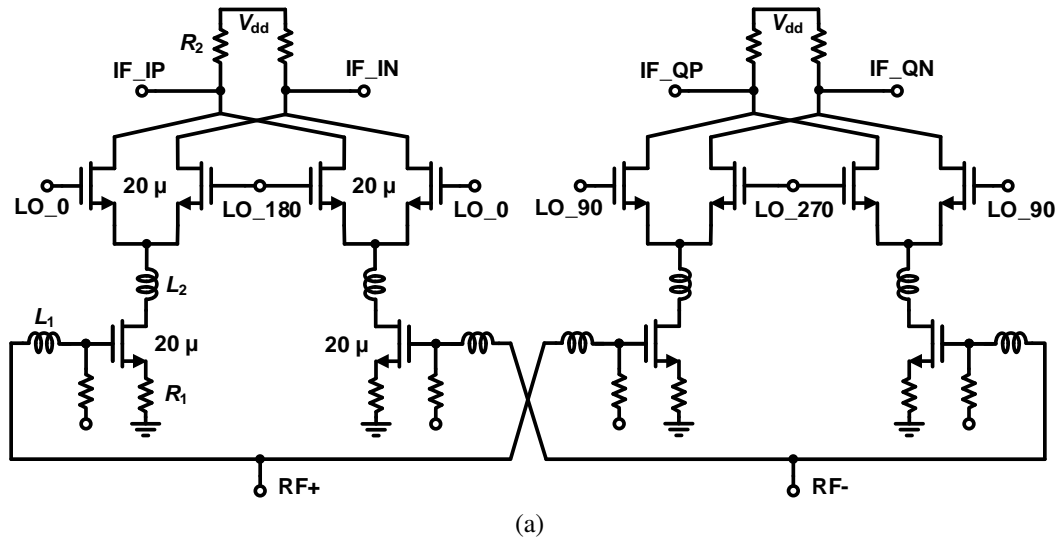
Figure 5.9: (a) Schematic double balance IQ down conversion mixer; (b) Simulated CG versus L_2; (c) Simulated IP1dB versus L_2.

dB and phase mismatch is $< 5°$ at 17-41.3 GHz. However, the voltage gain is greatly reduced due to the extra R. In order to reduce the loss, a compensation network can be added instead of R, as shown in Fig. 5.8c. Fig. 5.8d shows the simulated results. The gain is simulated together with LO balun and driver since the balun also introduces mismatch between positive and negative branch. The simulated voltage gain is 10-15 dB at 20-55 GHz. The gain mismatch is < 0.6 dB and phase mismatch is $< 5°$.

Usually low IF or direct down receivers employ passive mixer due to its low flicker noise. However, the application will be limited to narrow band since passive mixer requires rail to rail

swing at the gate, which dramatically increases the power consumption. Moreover, 25% duty cycle LO is required to avoid LO overlap for differential IQ mixer, which also increases the design complexity. Therefore, active mixer is used in this design. Fig. 5.9a shows the schematic of the double-balance IQ down conversion mixer. A resistor load (R_2) is used due to the low IF frequency. Degenerated resistor (R_1) is added in the g_m stage to improve the linearity and also help the input matching. In order to improve the conversion gain at high frequency, a series inductor L_2 is inserted between the g_m stage and the switching quad. The inductor resonant out the parasitic cap, which improves the conversion gain and also improve the noise performance of the mixer. The switching quad transistor size is a key parameter to determine. A large size results in a low overdrive voltage, which makes the switching quad easily to turn on or off. However, a large size also results in a large parasitic cap, which reduces the slew rate. In this design, 20 μm width is used for the switching quad transistors. Fig. 5.9b-c shows the simulated conversion gain and IP1dB versus L_2, where IF is fixed at 2 GHz. It can be observed that without L_2, the CG drops when frequency increases. With a larger L_2, the CG increases and generates a peak. But with a larger L_2, the IP1dB decreases, especially at high frequency. Taking CG and IP1dB into consideration, 150 pH is chosen for L_2. The IQ double-balance mixer consumes 27 mW dc power.

5.2.3   LPF and IF Amplifier

After the mixer, a LPF is added to suppress the unwanted high frequency tones. In order to improve the roll-off rate, a third-order version is used, as shown in Fig. 5.10a. The IF amplifier is a one stage inverter based amplifier and the gain can be controlled by the tail current and feedback resistor (R_f). Since the LPF and the IF amplifier directly load the mixer, the input impedance of IF amplifier affects the mixer conversion gain. A larger R_f results in a higher gain, narrower bandwidth and larger input impedance, which will be beneficial to the mixer. However, a larger R_f decreases the IP1dB and limits the linearity. Taking all of these into consideration, $R_f = 300 \, \Omega$

(a)

(b)

(c)
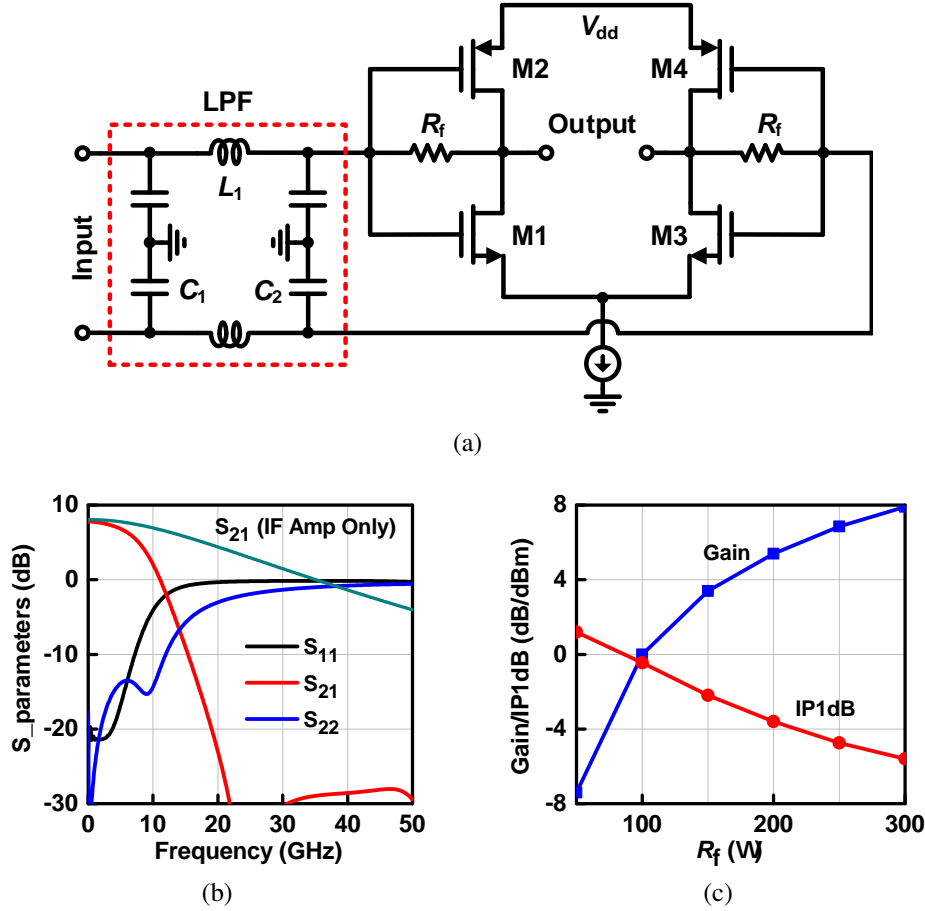
Figure 5.10: (a) Schematic of lowpass filter and IF amplifier; (b) Simulated S-parameters; (c) Simulated gain and IP1dB versus R_f.

is chosen. The input impedance can be calculated by

$$Z_{in} = \frac{R_f + R_L}{1 + (g_{mp} + g_{mn})R_L} \tag{5.4}$$

With a total gm of 0.04 S, the input impedance is calculated to be 116 Ω. Thus, a mixer load resistor of 120 Ω is chosen to make the LPF design easier. Another issue need to be considered is that in order to make the receiver works as low as tens of MHz (limited by the flicker noise), there is no AC coupling cap between the IF amp and mixer. Thus, the DC of the mixer output and the DC of IF amp input must be the same, which is realized by sizing the IF amplifier transistors.
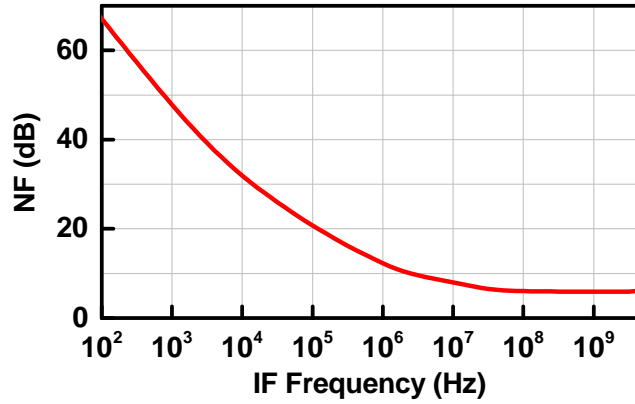
Figure 5.11: Simulated noise profile with RF=28 GHz.
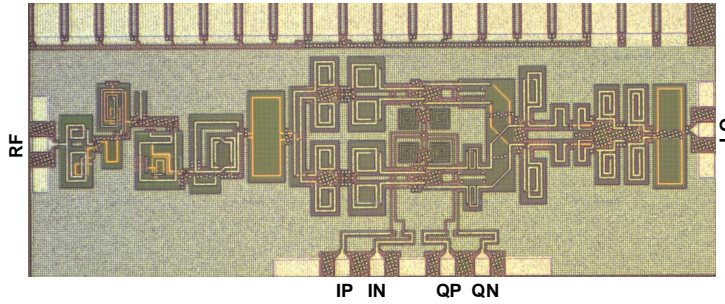
Figure 5.12: Microphotograph of the fabricated IQ receiver chip with core size of 1.8×0.5 mm^2.

The LPF lumped element values can be calculated by the following equations

$$C_1 = \frac{g_1}{R_0 \omega_c} \qquad C_2 = \frac{g_3}{R_0 \omega_c} \qquad L_1 = \frac{g_2 R_0}{\omega_c} \tag{5.5}$$

where g_1, g_2 and g_3 are the lowpass prototype elements, R_0 is the system impedance and $\omega_t extrmc$ is the cut-off frequency. The final C_1/C_2 and L_1 are chosen to be 120 fF and 3 nH, respectively. And the 3 nH inductor is realized by routing at LB/QB/QA layer with a compact size of 60×60 μm^2. Fig. 5.10b presents the simulated LPF and IF amplifier responses together. The peak gain is 7.9 dB with 1-dB/3-dB bandwidth of 5.1/8.1 GHz. S_{21}<-23 dB when frequency is larger than 22 GHz, which means the LO leakage is suppressed at least 23 dB. S_{11} and S_{22} are well matched. The LPF insertion loss is < 0.4 dB when frequency is smaller than 2 GHz. The total simulated IP1dB is -5.4 dBm and can be improved by switching the R_f to a lower value (Fig. 5.10c).

5.2.4   Entire Receiver

The entire receiver one channel gain is 24.5 dB and IP1dB is -27 dB. With frequency moves from 22-44 GHz, the NF has a trend of increasing due to the image folding. The lowest IF frequency is limited by the flicker noise and the simulated noise profile is shown in Fig. 5.11. It can be observed the flicker noise corner is around 50 MHz.

5.3   Measurements

Fig. 5.12 shows the micro-photograph of the fabricated receiver chip. The chip core area is 0.9×1 mm^2. All measurements including NF and linearity were performed using on-chip probing and the Keysight N5247B network analyzer (PNA-X) and signal generator. The total power consumption is 102 mW.

Fig. 5.13a shows the measured conversion gain and input/output matching. The IF is fixed at 2 GHz. The measured IP channel peak conversion gain is 22.3 dB with 3 dB bandwidth of 19.5-42 GHz, which covers the whole millimeter-wave 5G band. The S_{11} is < -10 dB at 19-50 GHz and the S_{22} is < -10 dB at DC-10 GHz. Fig. 5.13b shows the measured NF and IP1dB. The measured single-sideband NF is 5.2-7 dB at 20-45 GHz. When RF frequency is larger than 24 GHz, the image rejection is smaller than 3 dB, the noise at the image band is directly folded into the desired IF, which greatly increase the NF (by 2-3 dB). If the output of the receiver is combined and the image is rejected, the NF will below 5 dB. The measured IP1dB is -26 to -23 dBm at 20-45 GHz with IIP3 of around -15 dBm (measured with Δf=0.1 and 1 GHz).

Fig. 5.14 shows the measured conversion gain error and phase error between the I and Q channels, where the IF is fixed at 1 MHz in order to reduce the effect of connection cables. It can be observed the gain error is <1 dB at 20-45 GHz and it is smaller than <0.3 dB at 26-30 GHz and <0.6 dB at 37-41 GHz. The measured phase error is < 5°at 27-45 GHz. Based on equation (1), if the IQ outputs are combined, the image rejection ratio will be larger than 27 dB at 28-45 GHz.

(a)

(b)
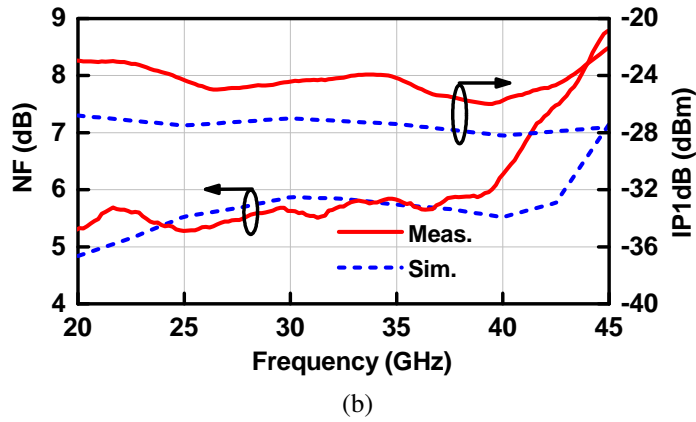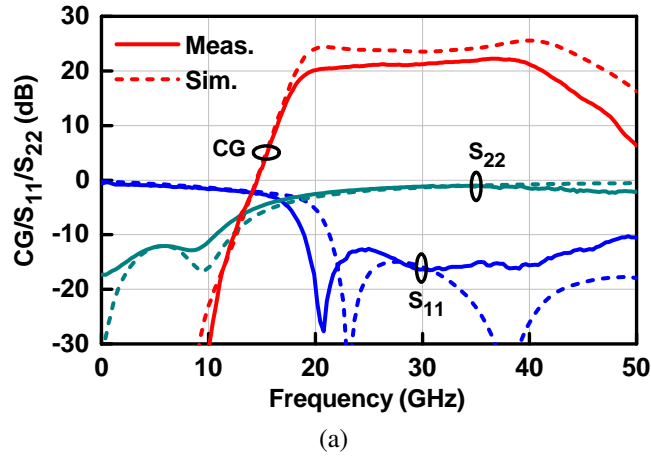
Figure 5.13: Measured and simulated (a) conversion gain and input/output matching; (b) NF and IP1dB.
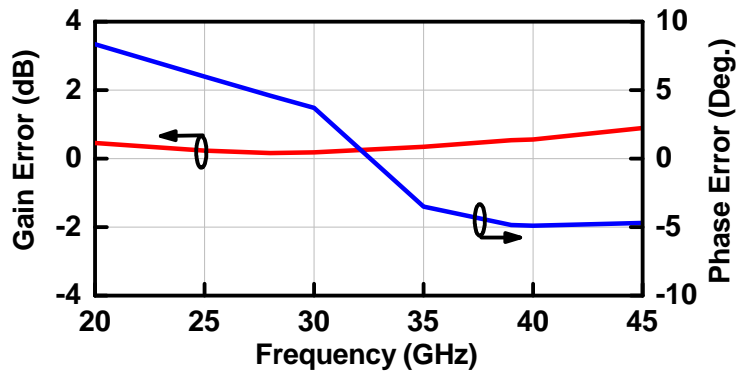
Figure 5.14: Measured gain and phase error between I and Q.

Fig. 5.15 shows the measured conversion gain, NF and IP1dB versus gain control. By turning on the current steering of LNVGA, the receiver conversion gain can realize 7-9 dB control at 20-42 GHz. At the lowest gain state, the NF just increases 1.2 dB, but the IP1dB increases
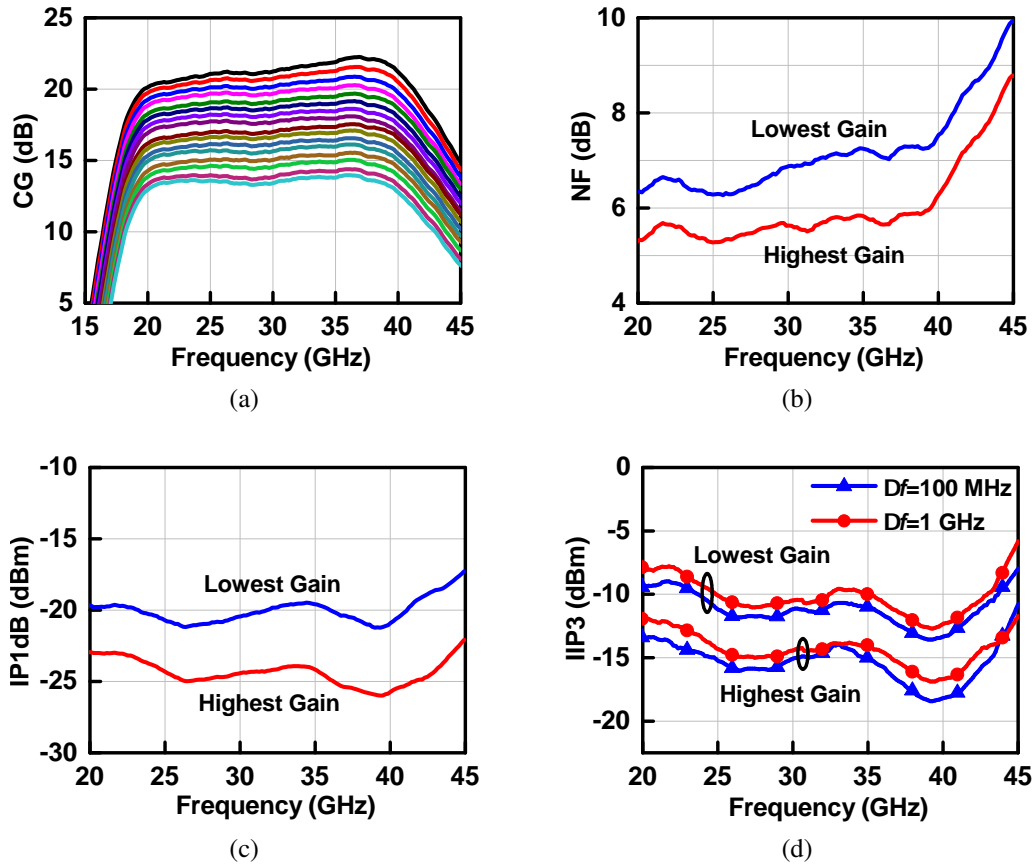
Figure 5.15: Measured (a) CG; (b) NF; (c) IP1dB; (d) IIP3 versus gain tuning.

by 5.2 dB. If more gain and linearity tuning range is required, the IF amplifier can be designed with switched feedback resistors instead of a fixed feedback resistor. Since the amount of IP1dB improvement is larger than amount of NF deterioration, the dynamic range increases with the receiver gain decreasing. Fig. 5.16 shows the measured results when RF is fixed while IF is changed. The measured IF 3-dB bandwidth is 5.7 GHz.

Table 5.2 compares the proposed wideband IQ receiver with start-of-art receivers. The power consumption is not included in the table since the non-core blocks vary in each design. This design has a relative lower gain which is because each channel is a single-end output. If the differential is calculated, the gain can be improved by 6 dB, which is comparable with other designs. As mentioned before, the NF is SSB NF, if the output is combined and the image noise is excluded, the NF will be smaller than 5 dB, which achieves the lowest NF.
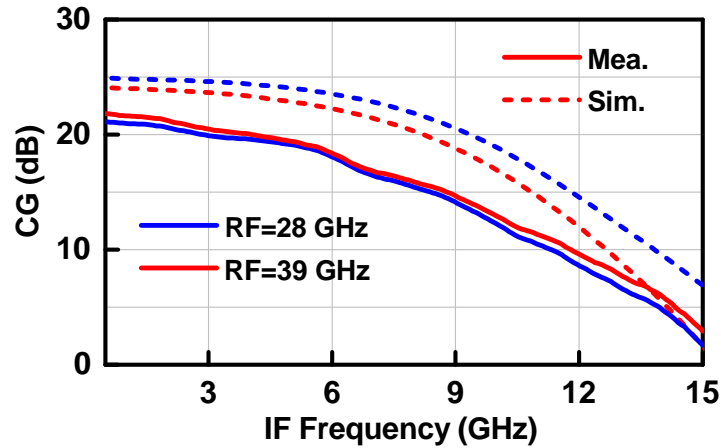
Figure 5.16: Measured and simulated CG versus IF frequency.

Table 5.2: Comparison with Previous Wideband IQ Receivers

Ref.	Tech.	f_0 (GHz)	RF BW (dB)	CG (dB)	NF (dB)	IP1dB (dBm)	LO	Size (mm^2)
[56]	0.12-μm SiGe	25	10-40	36	6.8-9.5	-33	Ex. Se	N.A
[57]	0.13-μm SiGe	35	25-45	21	5-7	-26 to -20	Ex. Se	2.5
[58]	45-nm SOI	34	24-44	35.2	3.2-6.1*	-27	Ex. Diff	0.76
[62]	65-nm CMOS	24	N.A	28.3	5*	-28	Ex. Diff	N.A
[63]	22-nm SOI	28	N.A	37.5	3.5*	-31	Ex. Se	0.1
[64]	65-nm CMOS	28	26.5-32.5	29.5	5.3*	-28	Ex. Se	0.65
This work	22-nm SOI	31	19.5-41	22.3	5.2-7	-26 to -23	Ex.Se	0.9

* NF is measured with image-rejection.

5.4   Conclusion

This chapter presented a wideband IQ receiver that covers 24-42 GHz millimeter-wave 5G band. Three stage 22 dB gain wideband LNVGA ensure low NF for the whole receiver. A modified QAF network is used to generate wideband low mismatch IQ for mixer. The whole

receiver has a measured peak gain of 22.3 dB with 3 dB bandwidth of 22 GHz. And the gain can be adjusted by the LNVGA for 7-9 dB. The measured SSB NF is 5.2-7 dB and the IP1dB is around -25 dBm. The measured gain and phase mismatch is <1 dB and 5°. The wideband responses and low NF makes it attractive for 5G communication.

5.5   Acknowledgment

Chapter 6

Design E-/W-Band LNA in GF 22-nm CMOS FD-SOI and 45-nm CMOS SOI

6.1   Introduction

The rapid scaling of CMOS technology in recent years has enabled low-cost and large-scale millimeter-wave systems, such as 60 GHz phased-arrays, 77 GHz automotive radars, and 94 GHz imaging systems. Advanced nodes of silicon-on-insulator (SOI) CMOS technology in 45-nm RF-SOI, 32-nm SOI and 22-nm fully-depleted (FD) SOI, has resulted in a $f_t/f_{max} > 240$ GHz, which has enabled low power operation at millimeter-wave frequencies.

A high-performance low-noise amplifier (LNA) determines the receiver noise figure (NF) and is an indispensable component in high-sensitivity receivers. Common-source (CS) amplifiers with source degeneration are used extensively at 0.1-30 GHz for simultaneous gain and NF match. However, the degeneration inductor reduces the amplifier gain, which is acceptable up to 30-40 GHz due to the high intrinsic transistor gain. As frequency increases, the common-source is replaced by a cascode amplifier since it results in a higher gain per stage [72]- [73]. At E- and W-band frequencies, multi-stage designs are also used [74–97] at the expense of added power

consumption. Most previous works in *E*- and *W*-band LNAs consume more than 20 mW of dc power to realize around 20 dB gain. Since phased-arrays require a very large number of elements at *E*- and *W*-band (1000-10,000 elements), a savings of 10 mW per LNA will reduce to system power consumption by 10-100 W, greatly reducing the excess generated heat and improving the system performance. Therefore, it is essential to build a low-power LNA while still maintaining a low NF and high gain.

Another important application at *W*-band is imaging systems, where the temperature sensitivity and resolution are related to the receiver NF and bandwidth [86]. For multi-stage amplifiers, the bandwidth is usually limited by the parasitic capacitance at each node, and past publications have proposed various transformer structures for wideband operation [80], [81], [85]. Unfortunately, most of reported bandwidths are smaller than 30 GHz and are achieved at the cost of relatively high dc power.

In this section, we will present high performance *E*- and *W*-band LNAs based on GF 22-nm and 45-nm CMOS SOI. For the *E*-band design, the target is low power consumption (9 mW), high gain (20 dB) and low NF (4.6 dB), while the *W*-band design focuses on wideband applications.

6.2 *E*-/*W*-Band LNA in GF 22-nm CMOS FD-SOI

6.2.1 Technology and Transistor Characterization

The LNAs are implemented in GF 22-nm CMOS FD-SOI process, which provides 10 copper metal layers with an additional 3.4 µm top aluminum metal, as shown in Fig. 6.1a. And Fig. 6.1b presents a cross section of the NMOSFET. The device layer is fully depleted and is located inside a buried oxide (BOX) layer, which isolates the device from the lossy substrate (7 Ω-cm) and also decreases parasitic capacitances. There is also a back-gate (BG) node, which can
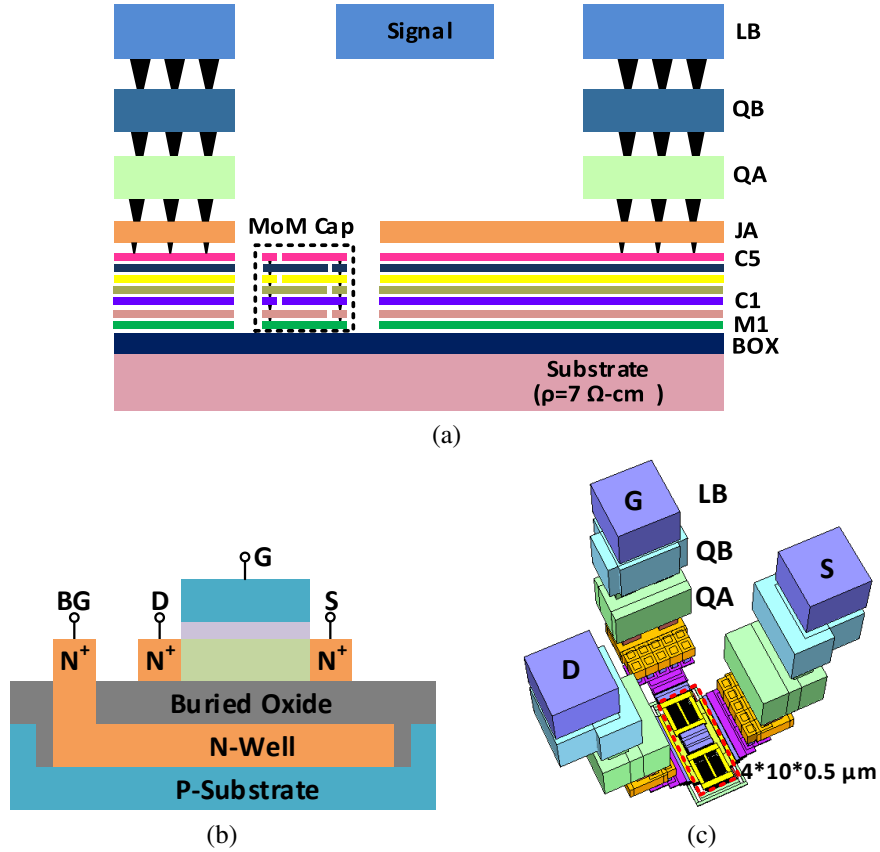
Figure 6.1: (a) 22-nm FD-SOI process stack; (b) Cross section of an n-channel MOSFET; (c) Transistor layout for W=20 μm.

be used to control the threshold voltage. The threshold voltage is expressed as

$$V_{\text{th}} = V_{\text{t0}} + \gamma(\sqrt{|2\phi_{\text{f}} + V_{\text{SB}}|} - \sqrt{2\phi_{\text{f}}}) \tag{6.1}$$

and when V_{BG} is increased, V_{th} decreases, and this allows a reduction of V_{dd} while maintaining the same dc bias current, resulting in low dc power consumption. However, since this was one of the early 22FDX tapeouts and the body-substrate model (capacitance and resistance to substrate) was not valid at mm-wave frequencies, the body is shorted to ground and the body bias was not used.

For LNA design, the first consideration is to realize the lowest possible NF. This 22FDX process provides several types of transistors and the super-low-V-threshold NMOS (slvtnfet) is

Table 6.1: Sheet Resistance and Routing Width for M1-C5

Layer	M1	M2	C1-C5
Sheet Resistance (Ω/sq)	0.616	0.603	0.443
Maximum Routing Width (μm)	1.7	1.7	4.1

(a)

(b)
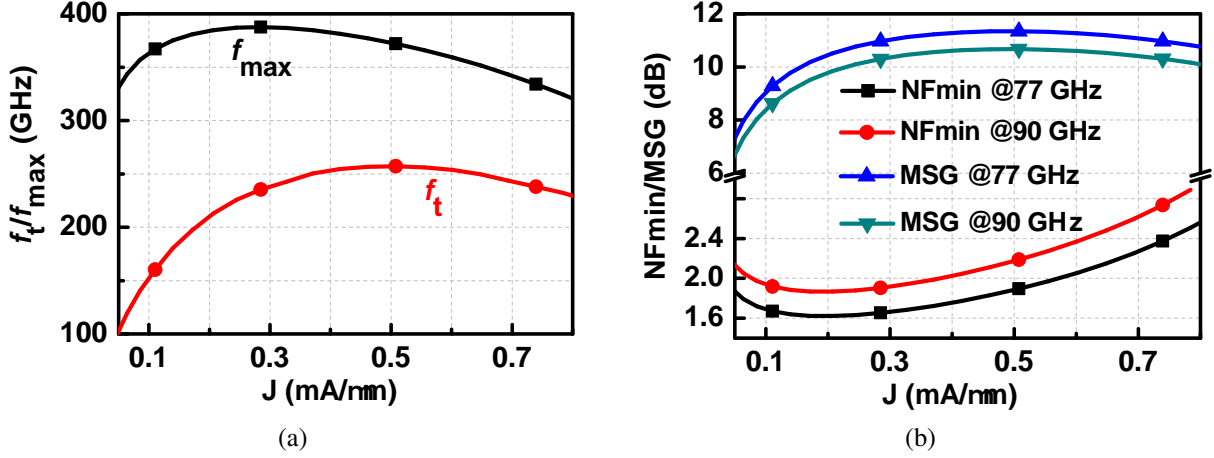
Figure 6.2: (a) 22-nm FD-SOI process stack; (c) Transistor layout for W=20 μm.

used in this design due to its low NF_{min}. The NF_{min} is expressed as [98]:

$$NF_{min} = 1 + 2\pi f K C_{gs} \sqrt{\frac{R_g + R_s}{g_m}} \qquad (6.2)$$

where K is constant value, C_{gs}, R_g, R_s and g_m are the gate-source capacitance, gate resistor, source resistor and transconductance, respectively. To achieve a low NF_{min}, R_g must be reduced to a minimum. Fig. 6.1c presents the layout of a W=20 μm NMOS-transistor, which is realized using four transistor cells each with width of 5 μm composed of 10 fingers (0.5 μm wide). The gates of the four transistors are first connected to C3 and C3-C5 are then used to connect the four transistors together. Since the C3-C5 metal layers have lower sheet resistance and wider allowable routing width than M1, as listed in Table 6.1, the gate resistance can be reduced from 18.5 Ω (for the standard 20×1 μm wide transistor and using M1 to connect 20 fingers) to 10.6 Ω (this design).

The transistor foundry models are based on the layout parasitics up to M1, and the metal parasitics from M1 to C1 are simulated using RC extraction and Caliber (Mentor Graphics) and

from C1 to LB are simulated by using full-wave analysis in EMX (Integrand Software). Fig. 6.2a and b presents the extracted f_t, f_{max}, MSG and NF_{min} versus current density, referenced to the top metal. The maximum f_t, f_{max} are 250/390 GHz. The lowest NF_{min} is 1.6 and 1.85 dB at 77 and 90 GHz, respectively, at a current density of 0.2 mA/μm. The corresponding f_t/f_{max} is 220/380 GHz and the MSG is 10.5 and 9.8 dB at 77 and 90 GHz, respectively. To the author's knowledge, these are very competitive when compared to any silicon or even GaAs technology.

The advantage of this technology can then be summarized as follows: (1) Due to the device scaling and lower parasitic capacitances, this technology has high f_t and f_{max}, which makes it suitable for mm-wave design. (2) Due to the high MSG, this process is suitable for high-gain amplifier design. (3) Due to the low V_{dd} and controllable threshold voltage, this process is ideal for low power design.

For an E- or W-band LNA, as since the input linearity is not a driving factor in the design, the LNA FoM is calculated as [77]

$$\text{FoM} = 20\log_{10}\left(\frac{\text{Gain[lin.]} \times \text{BW[GHz]}}{\text{P}_{dc}\text{[mW]} \times (\text{NF[lin.]-1})}\right) \tag{6.3}$$

Since the transistors in this process provide high gain with low dc power consumption, mm-wave LNAs designed in 22-nm FD-SOI are capable of achieving a very high FoM.

The millimeter-wave inductors are implemented on the LB layer due to its low resistivity. However, metal filling is mandatory from the M1 to the LB layer and with a high density (14%) for QA and QB, and greatly reduces the inductor Q. Fig. 6.3 presents the 3-D structure of a transmission-line inductor with inductance of 50 pH and a trace width of 6 μm (Z_o=75 Ω) and realized by a) LB layer before metal filling; b) LB layer after metal filling; c) QA, QB and LB connect all together after metal filling. For fair comparison, the trace lengths are slightly adjusted to preserve inductance of 50 pH. The simulated inductor Q at 90 GHz decreases from 33.6 to 17.4 after filling by using LB layer only, but building the inductor using QA, QB and LB together

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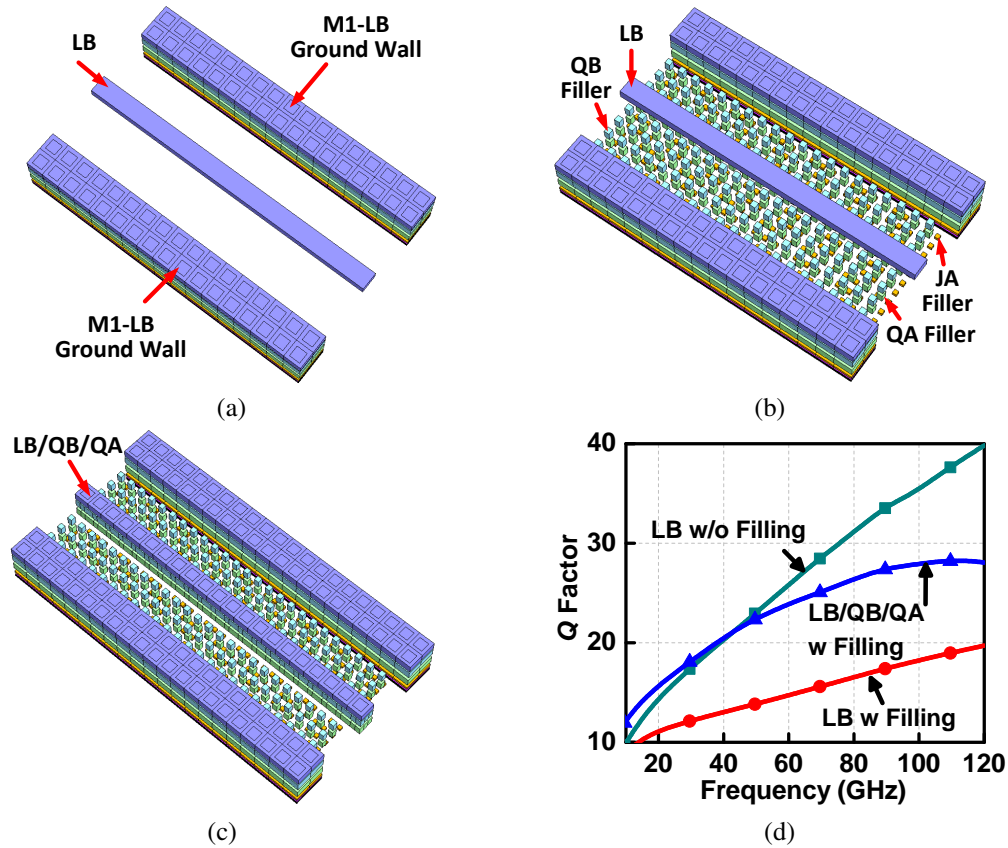
Figure 6.3: A 50 pH transmission-line inductor build using (a) LB without metal fill; (b) LB with metal fill; (c) LB/QB/QA with metal fill; (d) Simulated Q of a 50 pH inductor in 22FDX for different metal-fill cases.

results in a Q of 27.4 at 90 GHz (Fig. 6.3d).

The 22-nm FD-SOI design kit provides metal-oxide-metal (APMOM) capacitors which are based on interdigital fingers with user-selectable layers between M1 to C5. Fig. 6.4 compares two 72 fF capacitors, one built in C1 to C4 metal layers, and the other is a custom MOM cap also built in metal layers C1 to C4. Note that at higher metal layers, the gap between the metals is too large and results in a low capacitance density, and therefore, these are not used. The custom MoM design is around four times larger than the PDK MOM capacitor, and with a 15% lower Q at 90 GHz. Therefore, the PDK APMOM capacitor is used in the LNA designs.
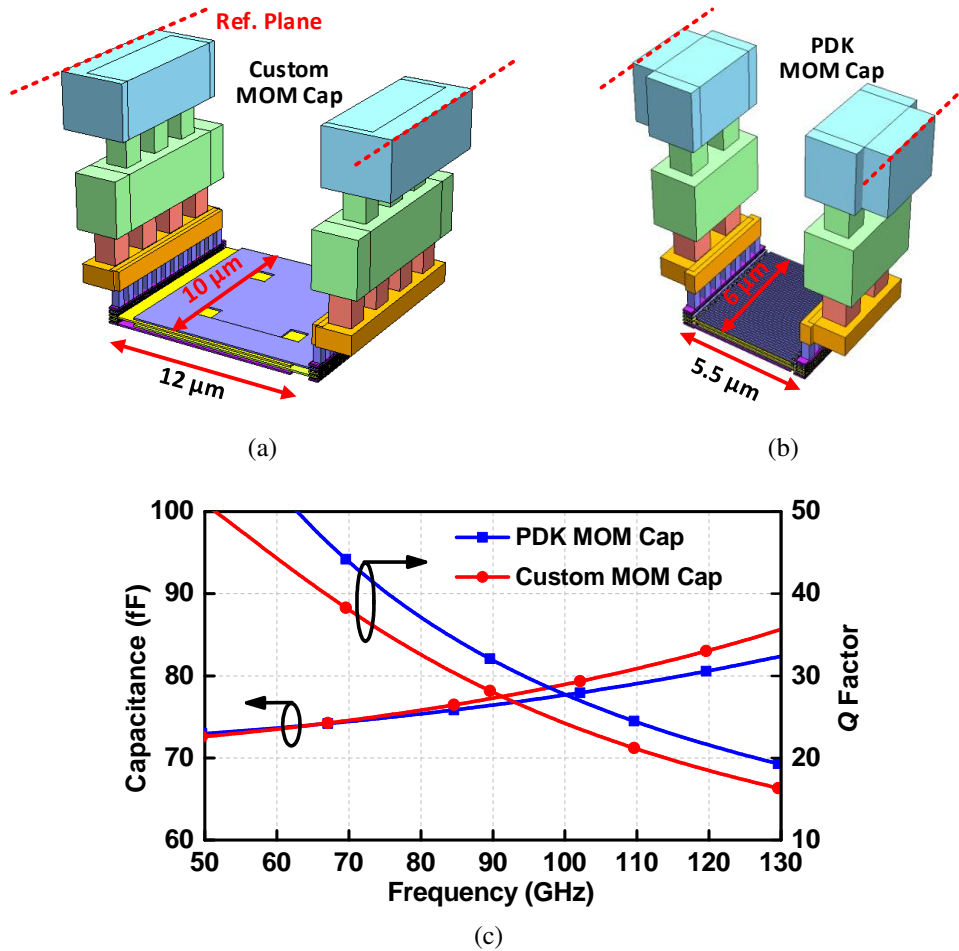
Figure 6.4: 3-D structure of (a) custom MOM capacitor; (b) PDK MOM capacitor; and (c) simulated capacitance and *Q*.

6.2.2 Circuit Design

To realize a high gain for *E*- and *W*-band LNAs, there are two popular topology choices. The first topology is a multi-stage CS structure [88], [92]. Due to its low gain at high frequency, the multi-stage CS topology is often realized as differential CS with neutralization capacitors. The disadvantage of this technique is that the power consumption is doubled due to the differential structure [77–79] and the neutralization capacitors must be very well modeled to avoid stability issues. The second technique is to use a multi-stage cascode structure. But if no gain boosting techniques are adopted, a cascode may still struggle to achieve the required gain per stage,
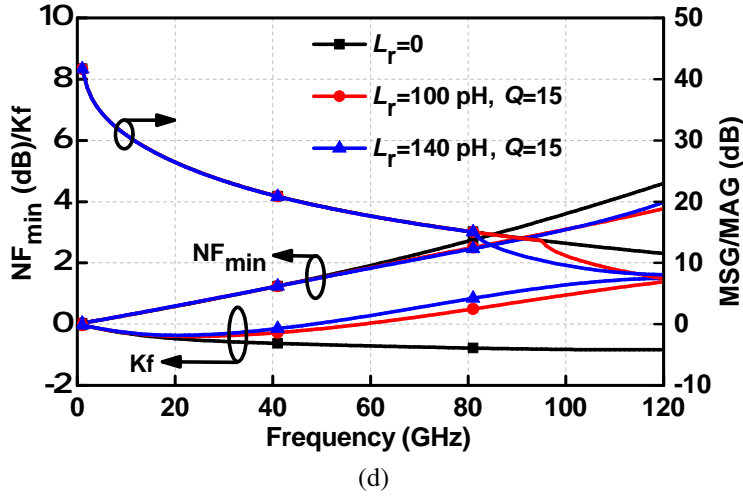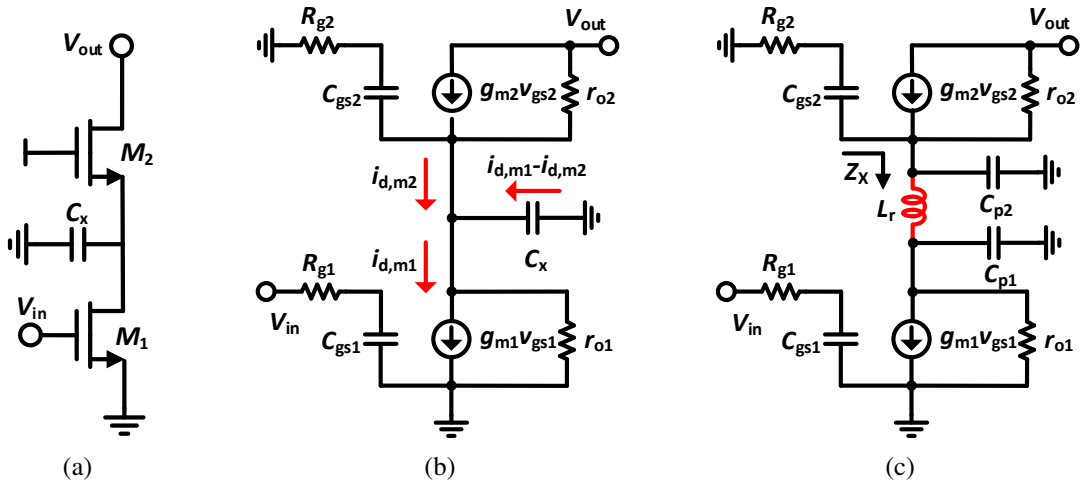
Figure 6.5: (a) Cascode stage; (b) Simplified small signal model of cascode stage without series inductor L_r; (c) with series inductor L_r; (d) Simulated NF_{min}, Kf and MAG/MSG at different L_r value.

and will also require a high dc power [91], [94–96]. In order to realize a high gain but with low power consumption, it is advantageous to choose a cascode structure with gain boosting techniques [81], [84]. The designs proposed in this paper adopt the gain-boosted cascode topology.

Fig. 6.5a presents a cascode amplifier and its simplified small signal model. If there is no parasitic capacitance C_{p1}, C_{p2} (labeled as C_x), the output noise due to the M2 transistor is [81]

$$F_{d2} = \gamma_2 \left(\frac{\omega}{\omega_t}\right)^2 g_{d2} R_s \frac{1}{g_{m2}^2 r_{o1}^2} \tag{6.4}$$

Since $g_{m2}r_{o1}$ is large enough, the effect of F_{d2} is small. However, when C_{p1}, C_{p2} exist, part of the drain current will flow into C_x as

$$i_{d,m2} = \frac{g_{m2}}{\sqrt{g_{m2}^2 + (\omega C_x)^2}} i_{d,m1} \tag{6.5}$$

and the M2 transistor power gain and noise can be calculated as [81]:

$$G_{power} = \frac{1}{4R_{g1}} \left(\frac{\omega}{\omega_t}\right)^2 \frac{g_{m2}^2}{g_{m2}^2 + (\omega C_x)^2} g_{m2} r_{o2} r_{o1} \tag{6.6}$$

$$F_{d2} = \gamma_2 \left(\frac{\omega}{\omega_t}\right)^2 g_{d2} R_s \frac{(\omega C_x)^2}{g_{m2}^2} \tag{6.7}$$

A large C_x results in lower power gain and larger F_{d2}. To suppress the M2 transistor noise, a shunt inductor or series inductor (L_r) is placed between transistors M1 and M2. The impedance seen from Z_x is:

$$Z_x = \frac{1}{sC_{p2}} \| (sL_r + \frac{1}{sC_{p1}}) = \frac{sL_r C_{p1} + 1}{s(C_{p1} + C_{p2} - \omega^2 L_r C_{p1} C_{p2})} \tag{6.8}$$

When the denominator of Z_x is 0, Z_x becomes much larger than the impedance looking up into transistor M2, and this results in the M2 transistor noise circulating in the M2 transistor itself and not present at the output node. Under this condition, L_r is

$$L_r = \frac{C_{p1} + C_{p2}}{\omega^2 C_{p1} C_{p2}} \tag{6.9}$$

Fig. ??d presents the simulated NF_{min} at 90 GHz of a cascode stage with W=20 μm and biased at J=0.2 mA/μm. The NF_{min} is 3.14 dB for L_r =0 pH, and reduces to 2.78 dB when L_r =100 pH is used ($Q = 15$). Note that a L_r up to 100 pH does not change the MSG at 77 and 90 GHz. For L_r=140 pH, the NF_{min} does not change. But the 140 pH inductor enhances the cascode stability factor (K_f) at 90-120 GHz and also affects the MSG/MAG at 90 GHz. Therefore, L_r should not
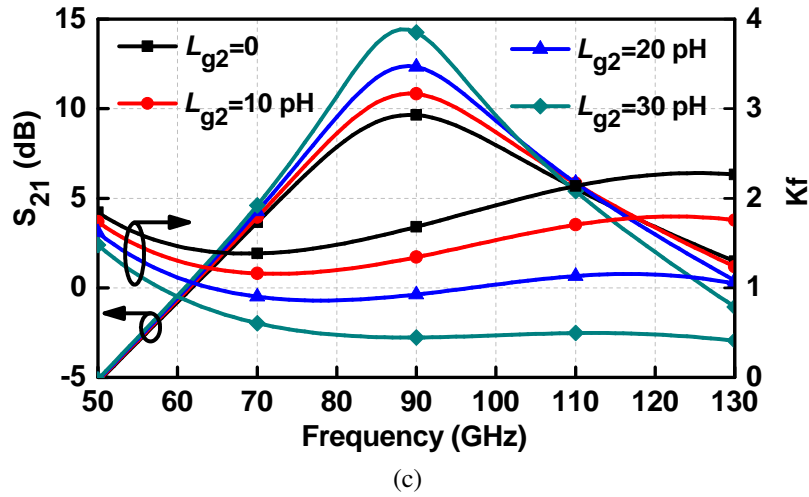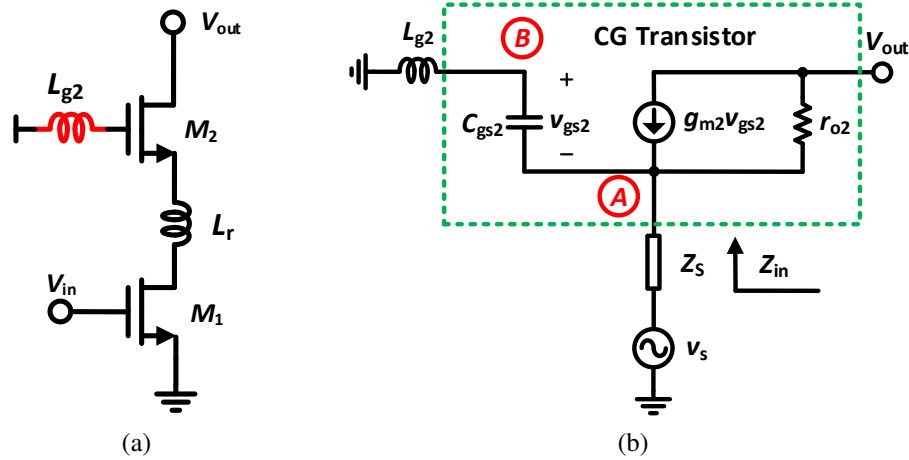
Figure 6.6: (a) Cascode stage with gate inductor at CG transistor; (b) Simplified small signal model; (c) Simulated S_{21} and Kf at different L_{g2} value for a cascode stage.

be too large.

An inductor, L_{g2}, placed at the CG stage is a well-known method to increase the cascode gain (Fig. 6.6a). The voltages at nodes A and B are:

$$V_A = \frac{1 - (\omega/\omega_t)^2}{1 - (\omega/\omega_t)^2 + (g_{m2} + j\omega C_{gs2})Z_s} V_s \tag{6.10}$$

$$V_B = \frac{-(\omega/\omega_t)^2}{1 - (\omega/\omega_t)^2} V_A \tag{6.11}$$

$$\omega_t = \frac{1}{\sqrt{L_{g2}C_{gs2}}} \tag{6.12}$$

As indicated by (11), V_A and V_B are out-of-phase when $\omega < \omega_t$, and V_{gs2} (V_A-V_B) is larger than the case of L_g=0, leading to an enhanced common-gate transconductance. However, a large L_{g2} will result in an unstable design. The admittance Y_{in} is

$$Y_{in} = \frac{g_{m2} + j\omega C_{gs2}}{1 - (\omega/\omega_t)^2} \tag{6.13}$$

and when $\omega > \omega_t$, the real part of the input admittance is negative, which causes stability issues. Fig. 6.6c presents the simulated S_{21} and Kf at different L_{g2} for a cascode stage. The peak gain increases from 9.6 to 10.8 dB for when L_{g2} is increased from 0 to 10 pH. However, when L_{g2} increases to 20 pH, Kf is < 1. This instability can be explained as follows: In the traditional cascode design, the gate of CG transistor is AC shorted (L_{g2}=0) which prevents any output signal leakage to the input through C_{gd}. With the addition of L_{g2} and C_{gd2} form a low-pass filter circuit which provides a low impedance path for the output signal to ground. As L_{g2} is increased, the filter corner decreases and the output signal leaks to the input through C_{gd2} and C_{gs2}, degrading the circuit stability. For a tuned circuit, V_{dd} is usually provided using a drain inductor (L_{d2}) which resonates out the drain shunt parasitic capacitance and peaks the gain at the desired frequency. Thus, L_{g2} and L_{d2} can be designed together to realize a drain-to-gate transformer, (Fig. 6.7). This circuit is described by the following equations:

$$(V_{s2} - V_{in})sC_{gd1} + g_{m1}V_{in} + \frac{V_{s2}}{r_{o1}} = (g_{m2} + sC_{g2})(v_{g2} - v_{s2}) + \frac{v_{out} - v_{s2}}{r_{o2}} \tag{6.14}$$

$$g_{m2}(v_{g2} - v_{s2}) + \frac{v_{out} - v_{s2}}{r_{o2}} + (v_{out} - v_{g2})sC_{gd2} + \frac{(v_{out} - v_M)}{s(L_{d2} - M)} + \frac{v_{out}}{R_L} = 0 \tag{6.15}$$

$$(v_{g2} - v_{s2})sC_{gs2} + (v_{g2} - v_{out})sC_{gd2} + \frac{v_{g2} - v_M}{s(L_{g2} - M)} = 0 \tag{6.16}$$

$$\frac{v_{g2} - v_M}{s(L_{g2} - M)} + \frac{v_{out} - v_M}{s(L_{d2} - M)} - \frac{v_M}{sM} = 0 \tag{6.17}$$

$$M = k\sqrt{L_{g2}L_{d2}} \tag{6.18}$$
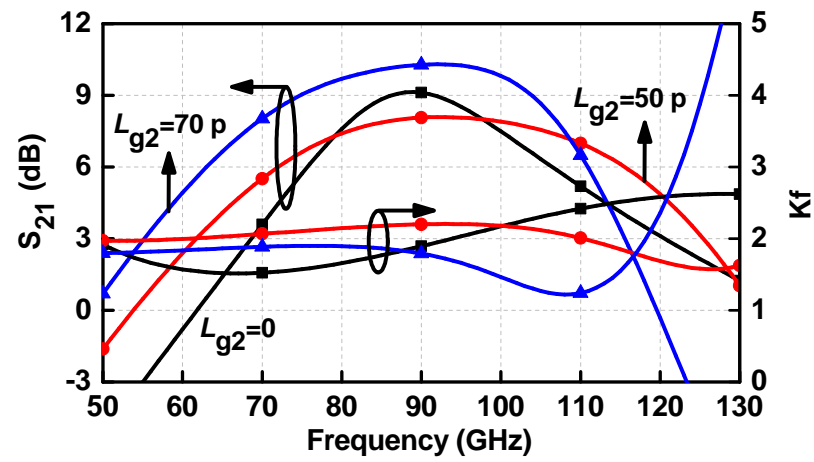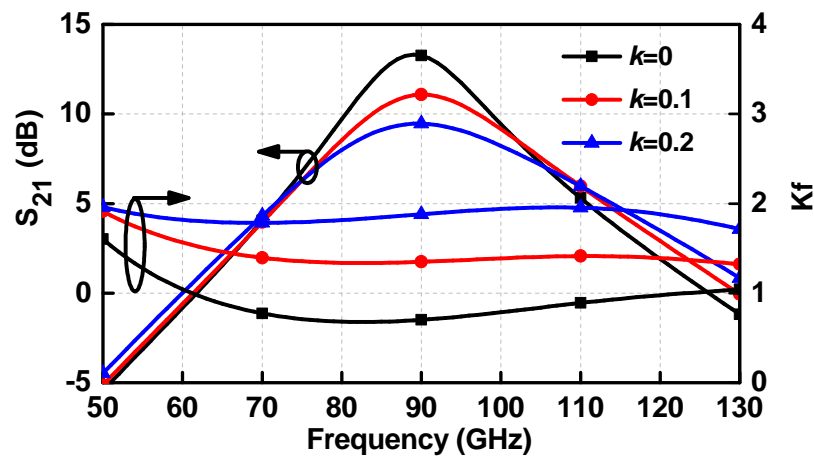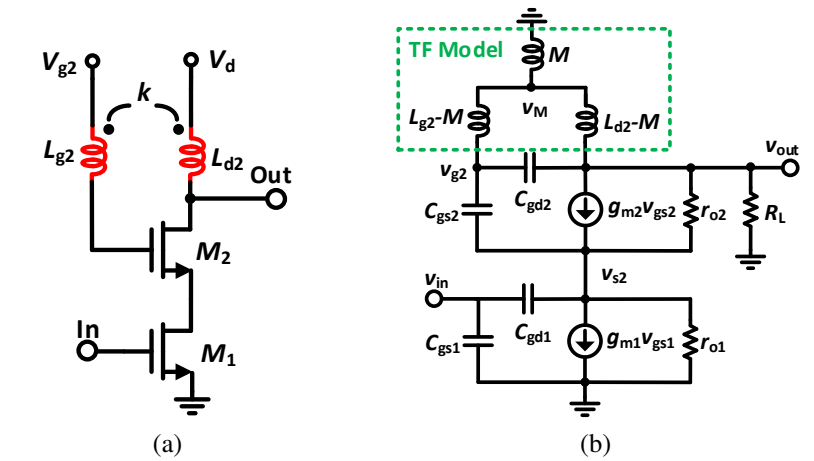
Figure 6.7: (a) Cascode stage with drain-gate transformer; (b) Simplified small- signal model; (c) Simulated S_{21} and Kf for different coupling coefficient value with L_{g2}=30 pH and L_{d2}=70 pH; (d) Simulated S_{21} and Kf for different L_{g2} value with a coupling efficient of 0.3.

For simplified calculations, r_{o1}, r_{o2} and C_{gs1} are ignored, and v_{out}/v_{in} is obtained in equation (6.19).

$$A_v = \frac{g_{m1}R_L s[(L_{d2}L_{g2} - M^2)C_{gd2}C_{gs2}s^3 + (L_{d2}L_{g2} - M^2)C_{gd2}g_{m2}s^2 + C_{gd2}Ms + L_{d2}g_{m2}]}{(g_{m2} + sC_{gs2})[(L_{d2}L_{g2} - M^2)C_{gd2}s^3 + (L_{d2} + L_{g2} - 2M)C_{gd2}R_L s^2 + sL_{d2} + R_L]}$$

(6.19)

For a standard design with no L_{g2} and M, there are three poles: A dominant pole p1 (ω_0=-g_{m1}/C_{gs2}) and two conjugate poles p2 and p3 at higher frequencies. When L_{g2} and M are present, another pole p4 is generated and the positions of p2 and p3 are changed. The non-dominant conjugate poles can be controlled by the transformer parameters (L_{d2}, L_{g2}, M). Due to the conjugate pole (p2 and p3), the roll-of-rate at higher frequency is faster, which is beneficial for a receiver with high out-of-band rejection.

Fig. 6.7c presents the simulated S_{21} and Kf for different coupling coefficient (k) value for L_{g2}=30 pH. When k=0, Kf < 1. By increasing the transformer coupling, the gain drops and the stability is enhanced. The design methodology is therefore to first use a large L_{g2} to increase the cascode gain and then introduce k to stabilize the circuit. The stability enhancement can be explained as follows: The source and drain voltage polarity of the CG transistor is the same while the source and gate voltage polarity is opposite. But the transformer has a positive coupling, which tend to make gate and drain voltage polarity the same. Thus, the voltage difference between gate and source of CG transistor is reduced, which is a negative feedback. The gain is reduced and stability is enhanced.

Fig. 6.7d presents the simulated S_{21} and Kf at different L_{g2} value (k=0.3). It can be seen that with L_{g2}=50 pH, the bandwidth is wider than the case of L_{g2}=0, but the gain is also lower. When L_{g2} = 70 pH, the gain is higher and bandwidth is wider. And in all cases, Kf is > 1. Thus, with changing L_{g2} and k, the desired gain and bandwidth can be realized in a stable cascode amplifier.
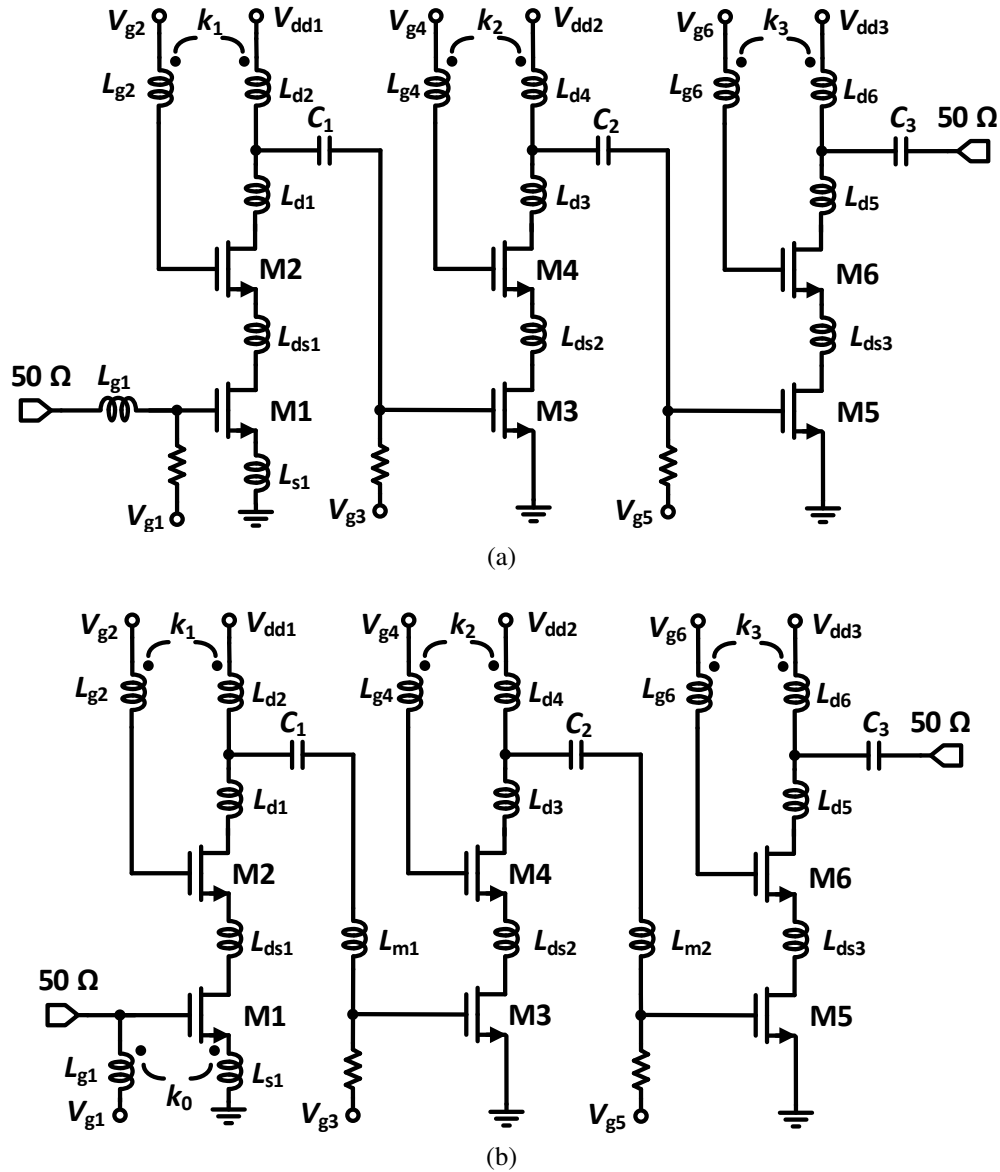
Figure 6.8: Schematic of the 3-stage (a) *E*-band LNA; (b) *W*-band LNA.

6.2.3 Circuit Implementation

Two single-end LNAs (*E*- and *W*-band) are designed using transformer-loaded cascode stages. Both LNAs utilize three cascode stages with input, output and inter-stage matching, but aim at different applications: 1) High gain, low power and low noise at 77 GHz (*E*-band, Fig. 6.8a), and 2) medium gain, wideband and low power at *W*-band (Fig. 6.8b). In both designs, the

Table 6.2: Parameter Value for E-Band LNA (Unit: pH or fF)

L_{g1}	L_{s1}	L_{ds1}	L_{g2}	L_{d1}	L_{d2}	L_{ds2}	L_{g4}	L_{d3}	L_{d4}
100	50	110	50	40	30	110	45	20	45
L_{ds3}	L_{g6}	L_{d5}	L_{d6}	C_1	C_2	C_3	k_1	k_2	k_3
110	45	30	40	72	62	70	0.1	0.1	0.23

Table 6.3: Parameter Value for W-Band LNA (Unit: pH or fF)

L_{g1}	L_{s1}	L_{ds1}	L_{g2}	L_{d1}	L_{d2}	L_{m1}	L_{ds2}	L_{g4}	L_{d3}	L_{d4}	L_{m2}
90	50	110	50	40	30	110	110	45	40	45	110
L_{ds3}	L_{g6}	L_{d5}	L_{d6}	C_1	C_2	C_3	k_0	k_1	k_2	k_3	
110	40	40	40	86	52	70	-0.5	0.25	0.4	0.45	

CS transistors width is 20 μm and the CG transistors width is 32 μm, which is determined by the tradeoff between linearity, gain and power consumption [99].

In both designs, the output matching is realized by a T-shape (L_{d5}, L_{d6}, C_3) matching network since it allows for a larger C_3 to avoid sensitivity to fabrication errors. For the input impedance match, the E-band design employs the classical source- degeneration to realize noise and power matching. By adding L_{s1} (50 pH, Q=24), the input impedance is tuned from (16-j75 Ω) to (55-j42 Ω), and then L_{g1} (100 pH, Q=11.8) is used to compensate the imaginary part. The NF degrades by 0.5 dB due to the finite Q of the matching network. The W-band design employs a transformer between the gate bias inductor and the source degeneration inductor to realize wideband input matching. The matching bandwidth can be controlled by L_{g1}, k_0 and L_{s1} as seen in Fig. 6.9, and a wide bandwidth is achieved with a larger negative k and a larger L_{g1}. However, since the inductance difference between L_{g1} and L_{s1} is large, a k < -0.5 is hard to realize for L_{g1} of 90 pH. Therefore, L_{g1}, k_0 and L_{s1} are chosen to be 90 pH (Q=12.3), -0.5, and 50 pH (Q=17.4), respectively. The NF degrades by 0.6 dB due to the finite Q of the matching network.

The inter-stage matching is realized using series capacitors (C_1 and C_2) for the E-band LNA, and each stage is designed at the same center frequency (Fig. 6.10a). For the wideband W-band LNA, series C-L networks are used to extend the bandwidth as shown in Fig. 6.10b. The combination of the first and third stages results in a flat gain, and the second stage increases the
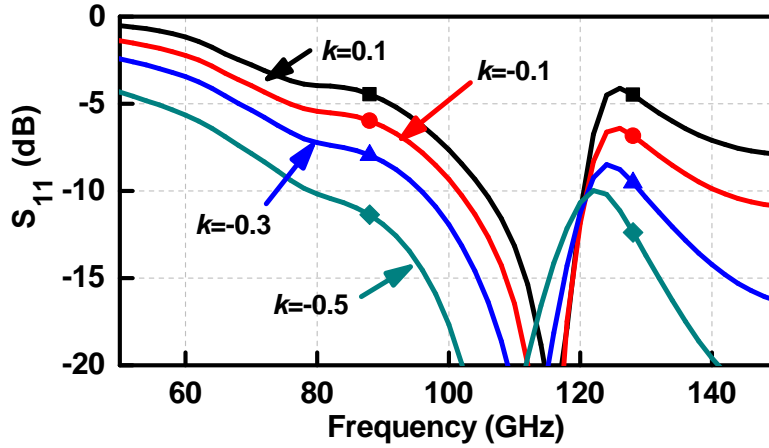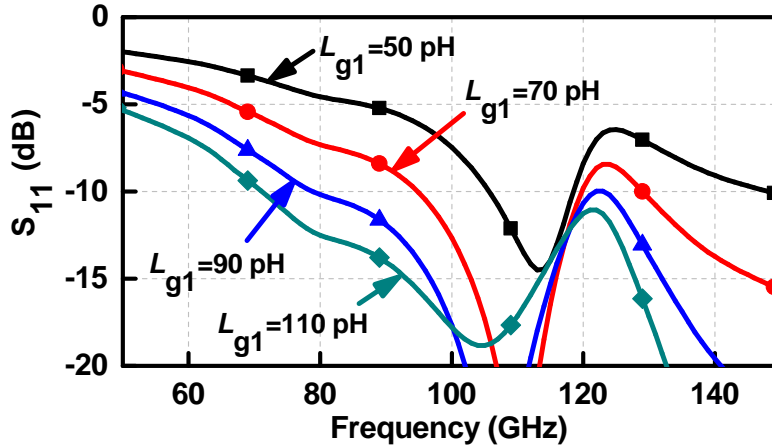
Figure 6.9: Simulated input matching for the *W*-band LNA (a) sweep *k* with L_{g1}=90 pH and L_{s1}=50 pH; (b) sweep L_{g1} with *k*=-0.5 and L_{s1}=50 pH.

overall gain.

The gate-to-drain CG transformers are realized using side-to-side coupling between two-shorted transmission-lines acting as distributed inductors. Fig. 6.11a presents details of the third-stage transformer in the *W*-band LNA. A longer coupling length and smaller coupling gap results in a larger *k*. In order to get a higher *Q*, LB/QB/QA are combined together for a low loss transmission line as discussed in Section II. The simulated transformer parameters are shown in Fig. 6.11b, and L_{g6}=45 pH with *Q*=21, L_{g6}=40 pH with *Q*=23 and *k*=0.23 at 77 GHz. Ground walls from M1 to LB are used to isolate the inductors and transformers and
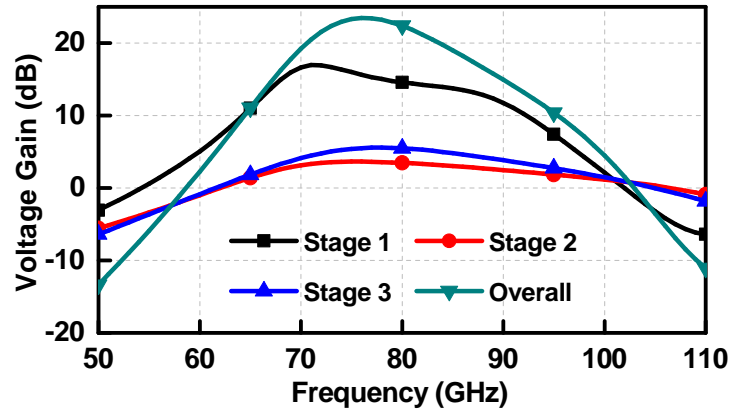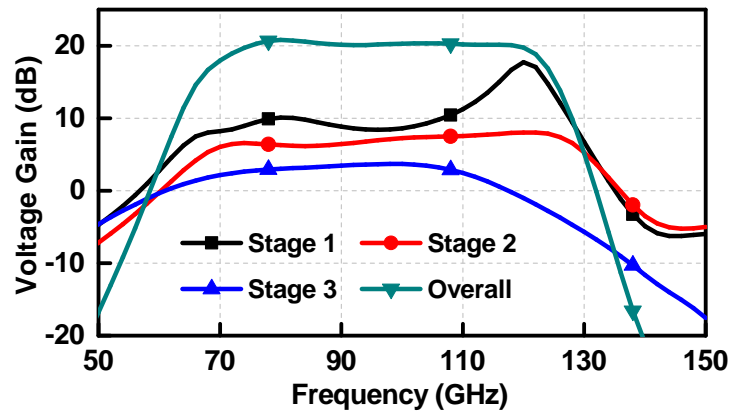
Figure 6.10: Simulated voltage gain of each stage and the whole gain (a) *E*-band; (b) *W*-band.

avoid unwanted couplings. All inductors, transformers and interconnections are simulated using full-wave electromagnetic tools (EMX).

The LNA gain and bandwidth can be easily adjusted by utilizing different transformer combinations. Fig. 6.12 presents first-stage transformer effect on the LNA gain. For the E-band LNA, when k_1 is increased from 0.1 to 0.5, the gain drops from 28.5 to 16.7 dB while the 3-dB bandwidth increases from 5 to 20 GHz. For the *W*-band LNA, when L_{g2} is decreased from 50 pH to 0, the 3-dB bandwidth drops from 58 GHz to 40 GHz. By choosing suitable transformers, the desired gain and bandwidth performance can be achieved. Tables 6.2 and 6.3 list the final optimized parameter values.
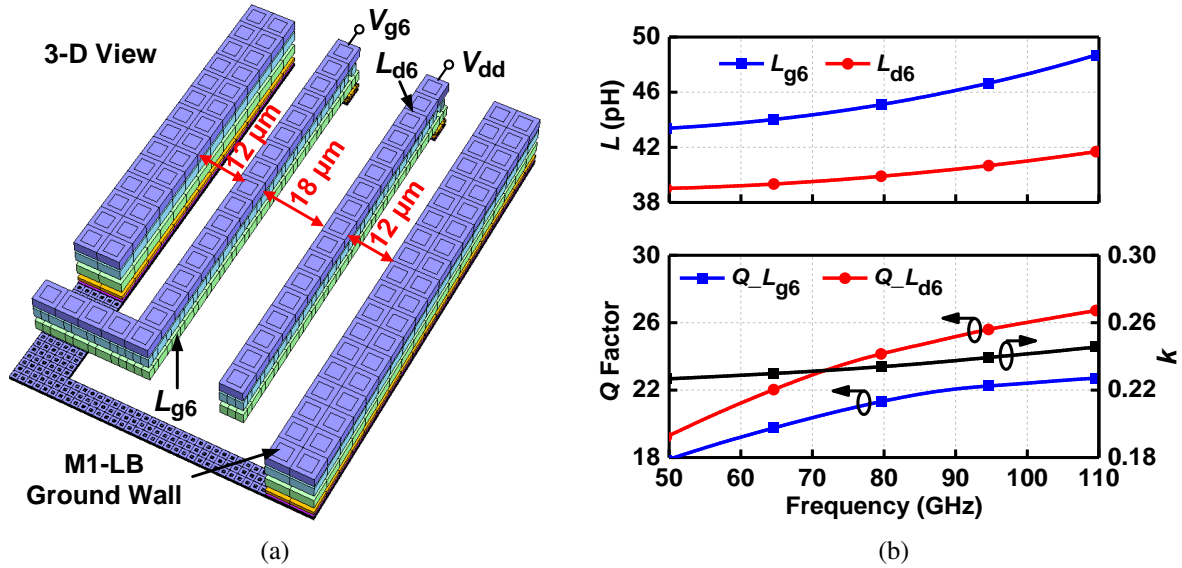
Figure 6.11: (a) 3-D view of third-stage transformer of *E*-band LNA (metal fill is not shown); (b) Simulated inductance, quality factor and coupling coefficient.

6.2.4 *E*-Band LNA Measurement

The *E*- and *W*-band LNAs are implemented in GF 22-nm CMOS FD-SOI (Fig. 6.13), with a size of 0.7 mm × 0.5 mm and 0.75 mm × 0.58 mm, respectively, including pads.

The *E*-band LNA is measured with V_{dd}=1.6 V (3.33 mA/stage, 16 mW total) and V_{dd}=1 V (3 mA/stage, 9 mW total). For V_{dd}=1.6 V, each transistor has a V_{gs} of 0.4 V and a V_{ds} of 0.8 V. For V_{dd}=1 V, each transistor has a V_{gs} of 0.4 V and a V_{ds} of 0.5 V. Fig. 6.14 presents the measured and simulated S-parameters. This is done by using Keysight PNA-X up to 70 GHz with coaxial 1.8 mm GSG probes, and then using a Keysight mm-wave extender with WR10 extenders for the 70-110 GHz range with WR-10 GSG probes. The peak gain is 24 dB and 20 dB with 3-dB bandwidth of 13 GHz and 12 GHz for the high-power and low-power modes, respectively. The measured S_{11} in both cases is < -9 dB from 70 to 110 GHz. The measured reverse isolation is limited by calibration above 70 GHz and is better 35-40 dB. Fig. 6.15 presents the measured Kf and Delta of both cases, showing unconditional stability over all frequencies.

The NF is measured using the hot/cold Y-parameter method. Fig. 6.16a shows the setup.
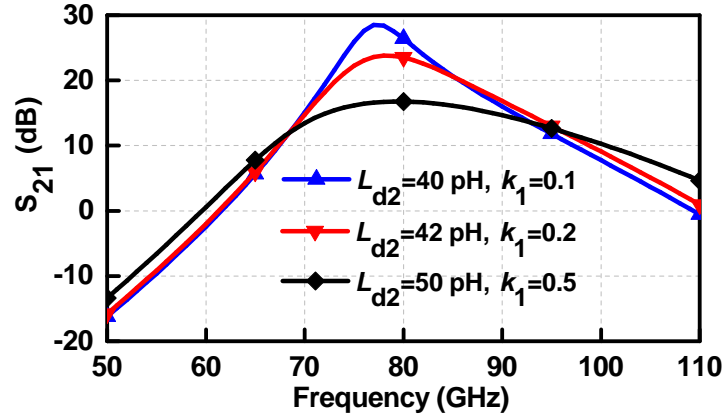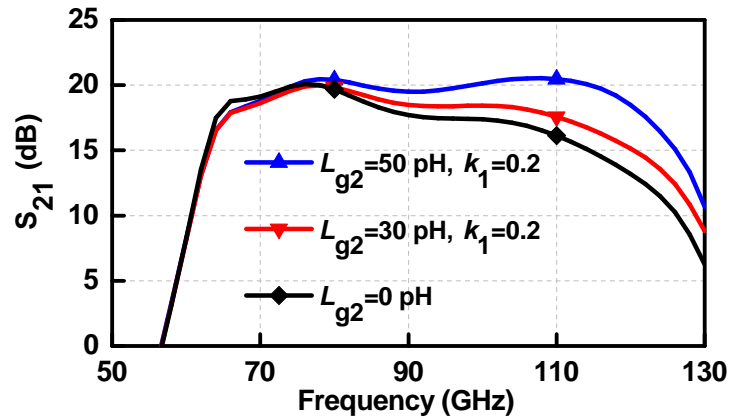
Figure 6.12: Simulated effect of first stage transformer to S_{21} (a) *E*-band LNA with L_{g2}=50 pH; (b) *W*-band LNA with L_{d2}=50 pH.

The noise source is from Quinstar (see Appendix for detailed noise measurements). After the DUT, an external amplifier with 30 dB gain is used to improve the system noise floor and isolates the loss and NF of the down-conversion mixer. A 6 dB attenuator is placed before the LNA and the 30 dB preamplifier to remove any standing waves.

The NF measurement steps are presented below:

Step 1: Use a W-band network analyzer set-up, and calibrate the VNA up to the WR-10 mm-wave extension head using waveguide calibration standards (GSG probe not included). Connect a "Thru" in place of the DUT and measure the Thru loss. The Thru structure includes a pair of waveguide RF probes and two GSG pads, back-to-back, with a very short transmission

(a)   (b)
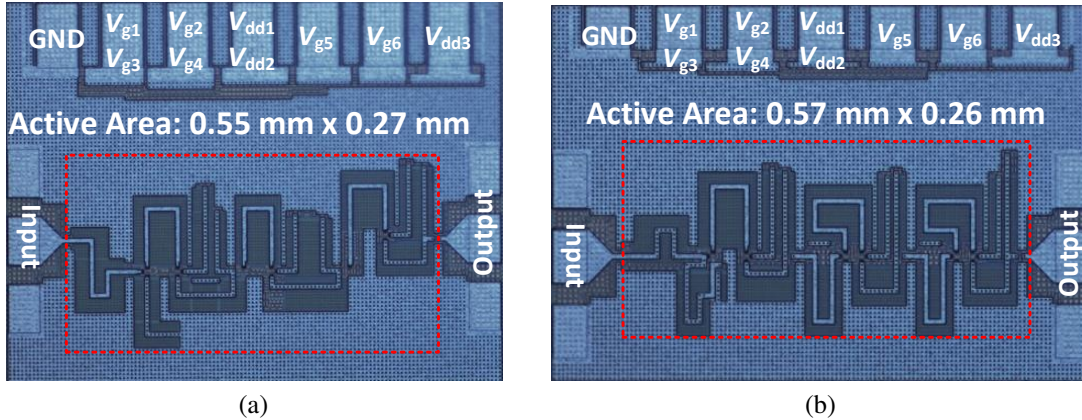
Figure 6.13: Microphotograph of the (a) *E*-band LNA with a chip size of 0.7×0.5 mm^2; (b) *W*-band LNA with a chip size of 0.75×0.58 mm^2.

line. This measured loss is called L$_1$ in dB. We assume that the two probes and two GSG pads are identical, therefore, the loss of the input probe+input GSG pad is (L$_1$/2) in dB.

Step 2: Connect Reference Plane A and B in Fig. 6.16a and perform calibration (no DUT present). The gain and NF of the attenuator, LNA, mixer, and IF amplifier chain are now known.

Step 3: Connect the DUT (LNA) and measure the NF using Fig. 6.16a. This measured NF includes 3 parts: the loss of input probe and input GSG pad, the LNA, and the loss of output GSG pad and output Probe. Since the LNA has a gain >15 dB, the effect of output GSG pad and output probe can be ignored.

Step 4: Calculate the LNA NF by de-embeding the loss of input probe and GSG pad. So the NF$_{\text{LNA}}$=NF$_{\text{total}}$-L$_1$/2.

Fig. 6.16b presents the measured NF with a minimum of 4.6 dB at 77 GHz. Fig. 6.16c presents the measured and simulated output power versus input power. The measured input P1dB is -26.8/-27.4 dBm for P$_{\text{dc}}$ 16/9 mW, corresponding to an output P1dB of -3.8/-8.4 dBm. The linearity is limited by the dc current in the last stage. If higher linearity is required, the bias can be increased at a cost of increasing power consumption. It should be mentioned that, at *E*- and *W*-band range, there are no strong interferers due to the high propagation loss. Therefore, in general, LNA linearity is not an issue. Also, by using a V_{dd} of 1 V instead of 1.6 V, P$_{\text{dc}}$ can be
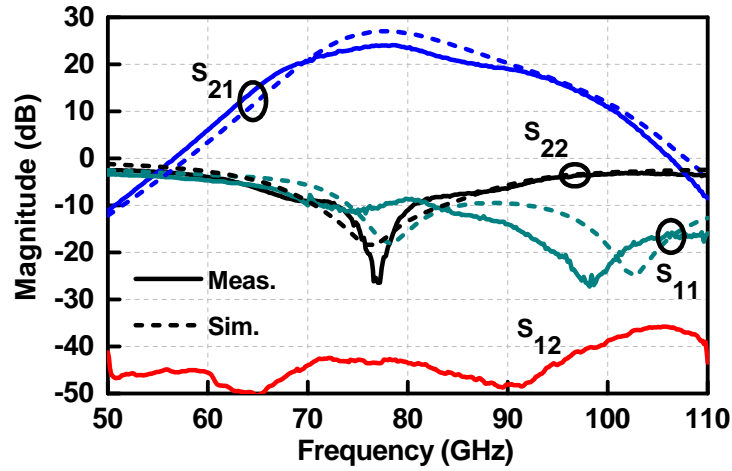
(a)
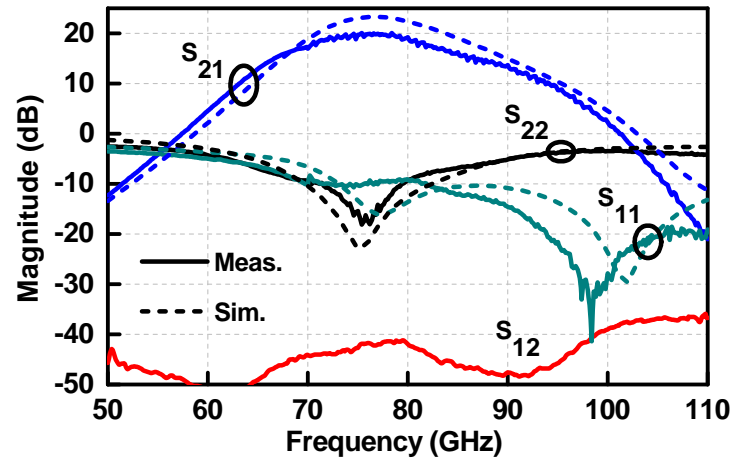
(b)

Figure 6.14: Measured and simulated S-parameters of the *E*-band LNA with (a) 16 mW P_{dc}; (b) 9 mW P_{dc}.
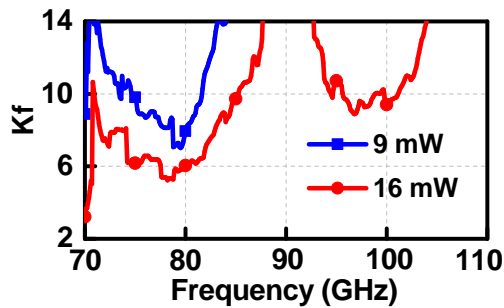
(a)
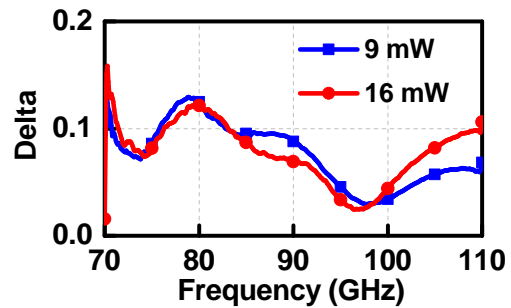
(b)

Figure 6.15: Measured (a) Kf, (b) delta (Δ) for 16 mW and 9 mW P_{dc}.
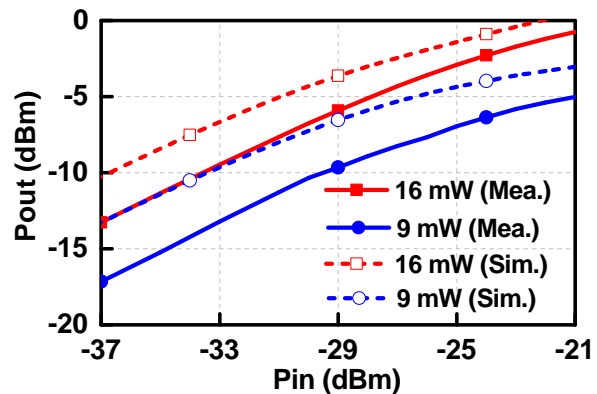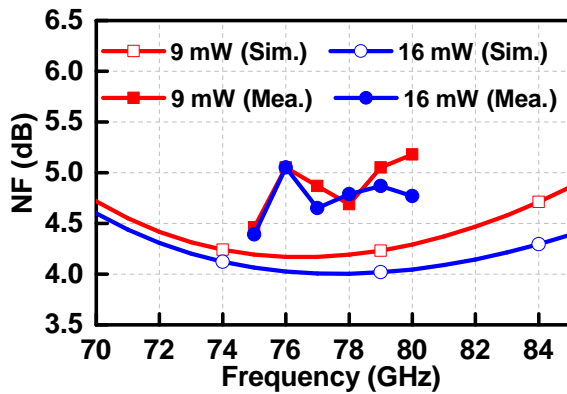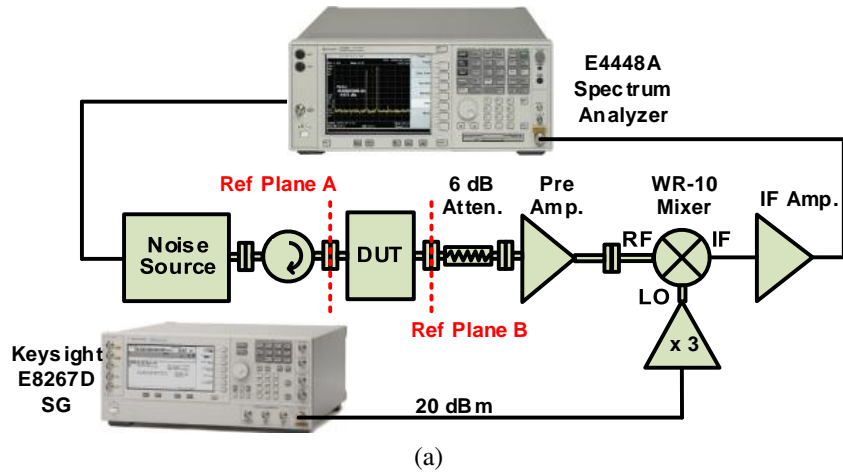
Figure 6.16: (a) NF measurement set up; (b) Measured and simulated NF for P_{dc} of 16 and 9 mW; (c) Measured and simulated output power versus input power for P_{dc} of 16 and 9 mW at 77 GHz.

decreased by 43% with a gain drop of 4 dB and an output P1dB drop of 4.6 dB. But from a FoM perspective, there is slight difference since the P1dB is not considered in the FoM calculation.

6.2.5 W-Band LNA Measurement

Fig. 6.17a presents the measured and simulated S-parameters of the W-band LNA, for a V_{dd} of 1.6 V (3.33mA/stage, 16 mW), V_{gs} of 0.4 V and V_{ds} of 0.8 V. The peak gain is 18.2 dB with a 3-dB bandwidth of 31 GHz. The gain is > 12 dB at 64-112 GHz, showing truly wideband operation. The gain starts to drop at 106 GHz, which may be due to additional parasitic capacitance caused by the stringent metal fills on the lower metal layers which are not fully
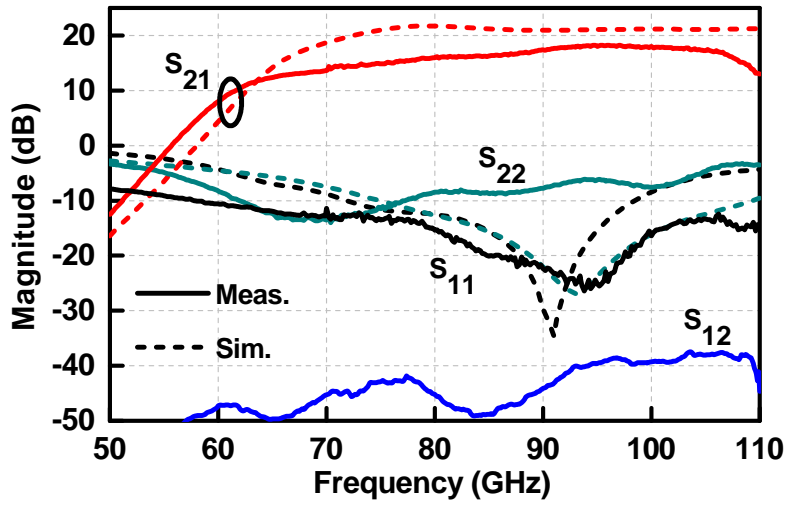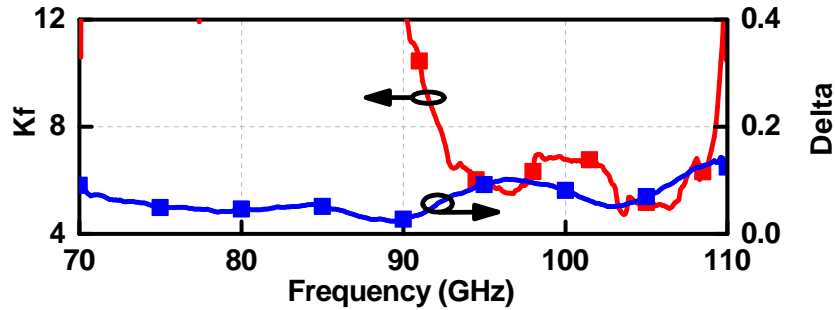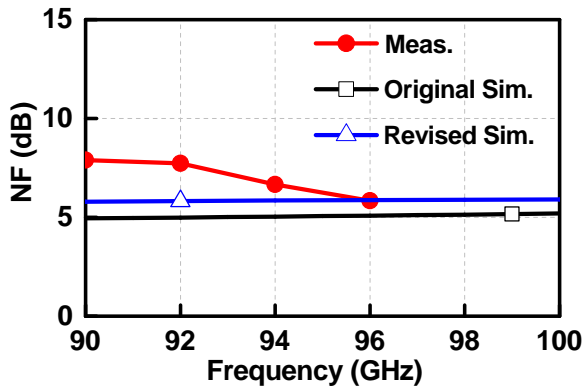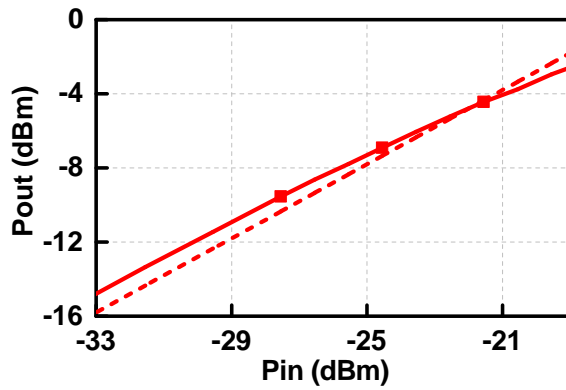
Figure 6.17: (a) Measured and simulated S-parameters; (b) Measured Kf and delta; (c) Measured and simulated NF; (d) Measured linearity at 94 GHz.

considered in the EM simulations. The S_{11} is < -10 dB in the whole band. Fig. 6.17b presents the measured Kf and Δ, which demonstrate that the wideband LNA is unconditionally stable. The

measured NF is 5.8-6.6 dB at 94-96 GHz and agrees well with simulations (Fig. 6.17c, the NF has been re-simulated while taking the decreased gain into consideration). The measured input P1dB is -22.8 dBm at 94 GHz (Fig. 6.17d).

6.3   *W*-Band LNA in GF 45-nm CMOS SOI

A similar *W*-band LNA is also implemented in GF 45-nm CMOS SOI for a technology comparison. The following subsection describe the design of this LNA, which achieves a peak gain of 12 dB and a minimum NF of 4.2 dB with a P_{dc} of 4.7 mW.

6.3.1   Technology and Circuit Design

This circuit is implemented on the GlobalFoundries 45 nm CMOS RFSOI process (45RF-SOI) and Fig. 6.18a presents the metal back-end for Option 18. It provides 7 copper metal layers and one aluminum top-layer. Due to the three thick metals (OA, OB and LD), the inductors implemented on the OB layer achieve high *Q* at *W*-band (a 60 pH inductor has a simulated *Q* of 40 at 90 GHz) and good isolation since a ground via-wall from M1 to LD can be used to reduce the coupling between neighboring inductors. Fig. 6.18b presents the 3-D layout of an NMOS transistor width of 20 μm (20×1 μm). The transistor uses double-gate contact to reduce the gate resistance. The gate, drain, and source connections are built in a stair configuration to quickly separate them and reduce the parasitic interconnect capacitance. Fig. 6.18c presented the simulated NF_{min}, f_t and f_{max} referenced to the top metal versus current density (J). At J=0.15-0.2 mA/μm, the transistor has the lowest NF_{min} (at 90 GHz) and f_t/f_{max}> 180 GHz.

The proposed LNA is shown in Fig. 6.19. In this design, two common-source amplifiers are first used for low noise figure, and are followed by a cascode stage with drain-to-gate feedback transformer, similar as the previous section. The input matching is realized by source-degeneration inductor. For a transistor with *W*=20 μm and biased at 2.2 mA, Z_{opt}=58+j92 Ω and Z_{in}=18-j64 Ω
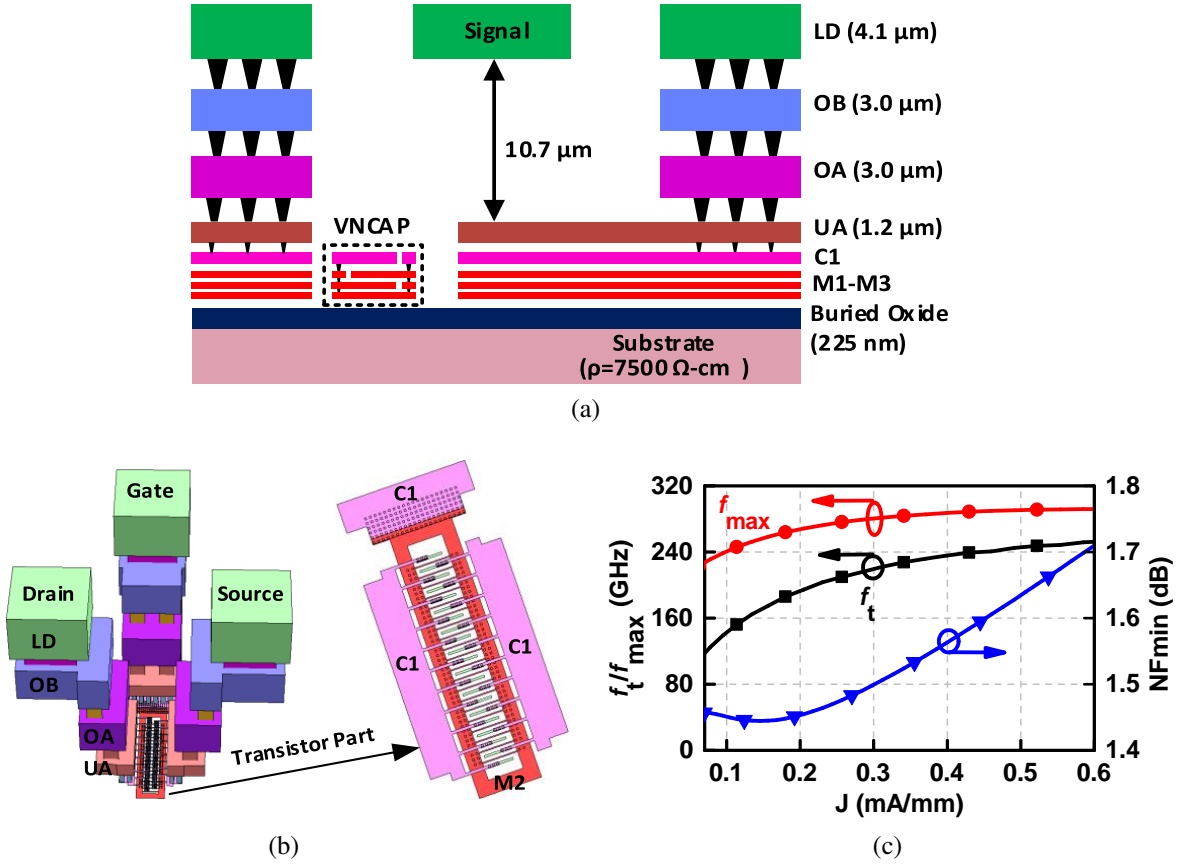
Figure 6.18: (a) Cross section of GlobalFoundries 45 nm CMOS RFSOI metal back-end; (b) Layout of a $W=20\times1$ µm transistor up to LD and C1; (c) Simulated NF_{min} (at 90 GHz), f_t, and f_{max}.

without L_{s1}. By adding a degeneration inductor L_{s1} (60 pH, $Q=40$ at 90 GHz), $Z_{in}=54-j60$ Ω and a series gate inductor L_{g1} (170 pH, $Q=23$ at 90 GHz) is used to S_{11} matching. The inner stage matching is realized by shunt inductors and series vertical capacitor (VNCAP with $Q=40$ at 90 GHz), which provides reasonable gain and noise matching between stages. The last stage is the proposed cascode stage with a higher voltage drive to improve the linearity. At the output port, two series inductor (L_{d3} and L_{d4}) are tapped with a series 50 fF capacitor to complete the 50 Ω match.

A microphotograph of the complete LNA is shown in Fig. 6.20. The chip is 0.6 mm×0.7 mm including all pads. All of the inductors (except L_{g1}) are realized using metal lines (without shield ground underneath) instead of spiral inductors to realize high Q.

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L_{g1}	L_{d1}	L_{s1}	L_{d2}	L_{s2}
170	80	60	70	50
L_r	L_{d3}	L_{d4}	L_{g3}	L_{s3}
120	20	60	60	30
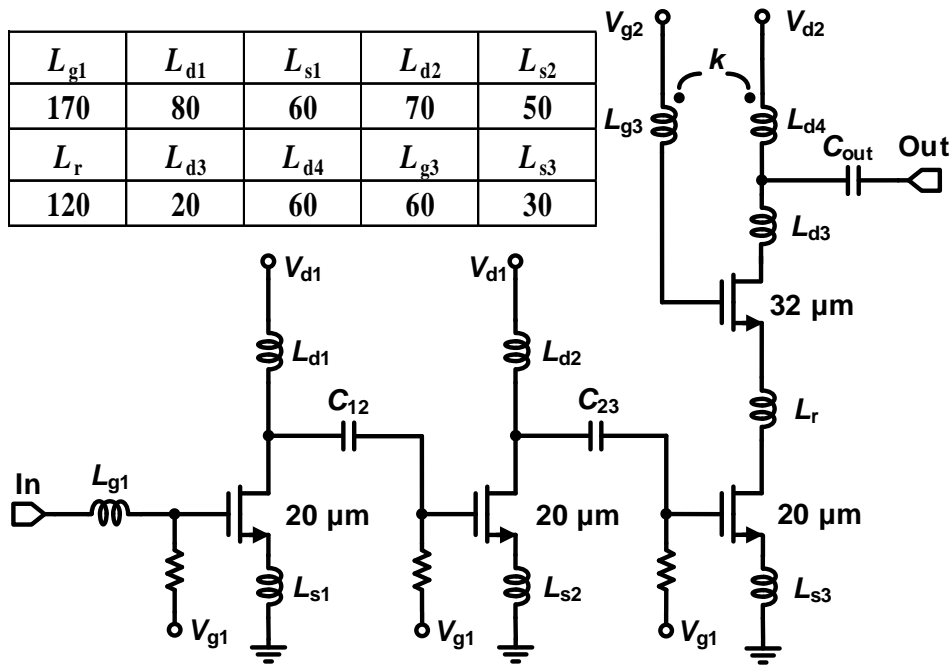
Figure 6.19: Schematic of the W-band LNA. Inductor values are in pH.
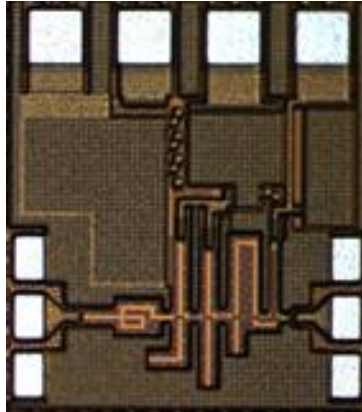
Figure 6.20: Photograph of the fabricated W-band LNA.

6.3.2 Measurement Results

S-parameter measurements are performed on-wafer using WR-10 GSG waveguide probes with 100 μm pitch. Calibration to the probe tips is done using on-wafer short-open-load-thru (CS-5 substrate).

The V_{dd} for the common-source and cascode stages is 0.5 and 1 V, respectively, and the

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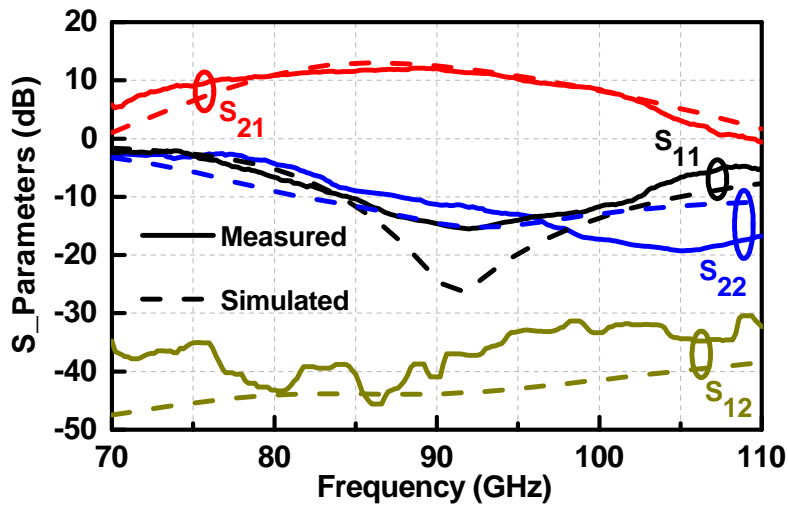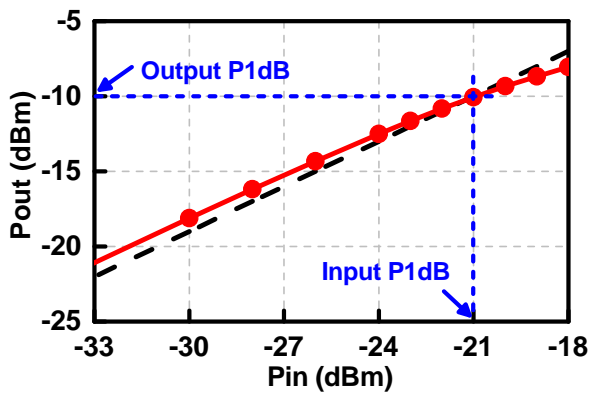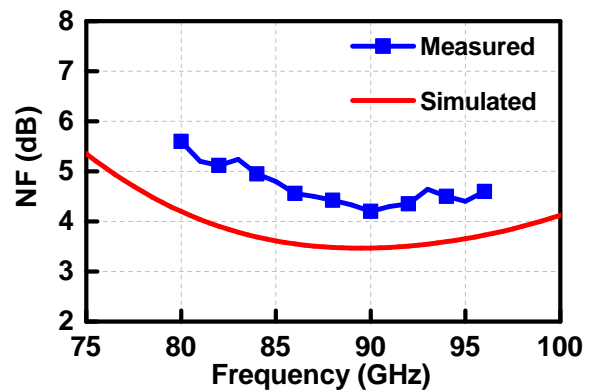
Figure 6.21: (a) Measured and simulated S-parameters; (b) Measured linearity at 90 GHz; (c) Measured and simulated NF.

bias currents are 2.2, 2.2 and 2.5 mA, resulting in a total DC power consumption of 4.7 mW. Fig. 6.21a presents the measured and simulated S parameters. The measured S_{21} has a peak gain of 12 dB at 90 GHz with 3 dB bandwidth of 74-99 GHz. The S_{11} is < -10 dB at 85-102 GHz and S_{22} is < -10 dB at 88-110 GHz. The measured input P1dB is -21 dBm and the corresponding output P1dB is -10 dBm at 90 GHz (Fig. 6.21b). The measured S_{12} is -35 to -40 dB, thereby resulting in a measured Kf ≫ 1.

Fig. 6.21c presents the measured noise figure at 80-96 GHz. The NF is < 4.9 dB at 85-95 GHz with a minimum NF of 4.2 dB at 90 GHz. At 95 GHz, the NF is 4.5 dB.

Table 6.4: Comparison with Previous State-of-the-Art LNAs

Ref.	Tech.	f_0 (GHz)	V_{dd} (V)	Gain (dB)	BW (dB)	NF (dB)	P_{dc} (mW)	IP1dB (dBm)	Area (mm^2)	FoM
[74]	90-nm CMOS	64	1.65	15.5	8	6.5	86	N.A	0.52	-15
[75]	28-nm CMOS	66	2	13.8	18	4	24	-12.5	0.38	7.7
[76]	40-nm CMOS	55	1.2	15	13	3.6	20.4	-25	0.2	8.8
[77]	22-nm FinFET	73.5	1	20	10.4	4	10.8	-22.8	0.54	16.1
[78]	28-nm CMOS	80	0.9	16.5	12	5.2	26	-15.5	0.16	2.5
[14]	45-nm CMOS	83	1	13.5	12	5.7	13.5	-14	N.A	3.8
[82]	90-nm CMOS	78	1	18.8	8.3	7.4	7.2	-30	N.A	7
[84]	65-nm CMOS	77.5	1.8	18.5	30	5.5	27	-15	0.24	11.3
[88]	90-nm CMOS	78.5	1	18.1	8	5.1	8	-22	0.19	14.6
[94]	65-nm CMOS	100	1.8	16.7	21.5	7.2	48.6	N.A	0.29	-2.9
[95]	28-nm CMOS	90	2	32	5	5.3	36	-43.8	0.28	7.3
[96]	65-nm CMOS	84	1	22	20	6.8	21	N.A	0.45	10
This work	22-nm CMOS	77	1	20	12	4.6	9	-27.4	0.35	17
This work	22-nm CMOS	92	1.6	18.2	31	5.8	16	-22.8	0.43	15
This work	45-nm CMOS	86	1	12	25	4.2	4.7	-21	0.42	22.2

6.4   Comparison

Table 6.4 compares the proposed *E*- and *W*-band LNAs with previous LNAs at 60 to 100 GHz. The FoM is calculated using equation (3). The proposed LNAs demonstrate a state-of-the-

art FoM in narrowband (77 GHz) and wideband (70-100 GHz) designs.

6.5   Conclusion

This chapter demonstrates the first 22-nm CMOS FD-SOI LNAs at *E*- and *W*-band. The drain-to-gate transformer-loaded cascode stage is analyzed, and two different three-stage cascode LNAs based on the transformer-loaded cell are designed and implemented. The *E*-band LNA realizes a peak gain of 20 dB with a 3-dB bandwidth of 13 GHz, 4.6 dB NF, and consumes only 9 mW of P_{dc}. The *W*-band LNA has a peak gain of 18.2 dB with 31 GHz bandwidth, 5.8 dB NF, and consumes only 16 mW of dc power. This chapter also demonstrates a *W*-band LNA in 45-nm CMOS SOI with peak gain of 12 dB, NF of 4.2 dB and P_{dc} of 4.7 mW. Both LNAs, wideband and narrowband, in both process achieve state-of-the-art FoM values.

6.6   Acknowledgment

Chapter 6, in full, is a reprint of the material as it appears in the following papers and the dissertation author was the first author.

L. Gao, E. Wagner, and G. M. Rebeiz, "Design of E- and W-band low-noise amplifiers in 22-nm CMOS FD-SOI", *IEEE Trans. Microwave Theory and Techn.*, vol. 68, no. 1, pp. 132-143, Jan. 2020.

L. Gao, Q. Ma, and G. M. Rebeiz, "A 4.7 mW LNA with 4.2 dB NF and 12 dB gain using drain to gate feedback in 45nm CMOS RFSOI technology", in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 280-283, Jun. 2018.

Chapter 7

Designing Wideband Power Amplifiers in 45-nm CMOS SOI

7.1 Introduction

With the development of wireless communication, wideband communication link is becoming desired since it can support high date rate. Wideband power amplifier (PA) as a critical building block in the ultra-wideband transmitter has attracted a lot of attention. Among the wideband power topologies, distributed amplifiers (DA) offer both ultra-wide bandwidth and excellent in-band matching. In [100], a three-stage DA is designed at DC-90 GHz bandwidth in 45nm CMOS SOI using cascode structures. However, it has relatively low gain over the bandwidth. To increase the gain and maintain the bandwidth (BW), a combination of conventional DA and cascade single-stage DA is used [101]. While most DAs are targeted to achieve largest GBW product, their output power are relatively low. The existing high power DAs can be placed in three groups. The first is the use of GaN technology [102], where tens of watts can be achieved using a high-voltage supply. The second is to use non-uniform DAs by tapering the output impedance. However, these DAs tend to have worse in-band gain flatness [103]. Moreover,

since the required inductance per stage reduces quickly, only a limited number of stages can be used. The last method is to use a stacked structure as the single-stage unit [104] [105]. Due to stacking, the power supply can be increased without transistor breakdown. In terms of efficiency, [106] proposed a supply-scaling technique to enhance the efficiency. Since the voltage-swing is accumulated at the drain output, the input stages can be biased at lower power supplies and this improve the DA efficiency. However, this technique requires DC blocks between the stages, which is not suitable for low frequency operation.

In this chapter, a four-stack, four-stage uniform DA is designed. With stacked transistors and a 4.4 V supply, the DA achieves a 1-17 GHz small-signal bandwidth and 19-21 dBm saturated output power. Measured EVM show that this DA can support 30 Gbps data rates using 64-QAM.

7.2 Distributed Amplifier Design

7.2.1 Circuit Design

Fig. 7.1 presents the four-stack four-stage distributed power amplifier. The parasitic capacitance of the NMOS gate and drain are absorbed by the artificial transmission lines (TL). The characteristic impedance of the input and output TLs is chosen to be 50 Ω.

$$Z_0 = \sqrt{\frac{L_g}{C_{g\text{-}p}}} = \sqrt{\frac{L_d}{C_{d\text{-}p}}} \tag{7.1}$$

where $C_{g\text{-}p}$ and $C_{d\text{-}p}$ are the gate and drain parasitic capacitance of the bottom NMOS and the top NMOS transistors. To prevent reflections at the input and output ports, 36 Ω resistors (R_g and R_d) and 10 pF DC block capacitors (C_b) are connected at these ports. The TL group delay (τ_{in}/τ_{out}) and the cutoff frequency ($f_{c\text{-}in}/f_{c\text{-}out}$) are

$$\tau_{in} = \sqrt{L_g C_{g\text{-}p}}, \ \ \tau_{in} = \sqrt{L_d C_{d\text{-}p}}, \ \ f_{c\text{-}in} = \frac{1}{\pi \tau_{in}}, \ \ f_{c\text{-}out} = \frac{1}{\pi \tau_{out}} \tag{7.2}$$
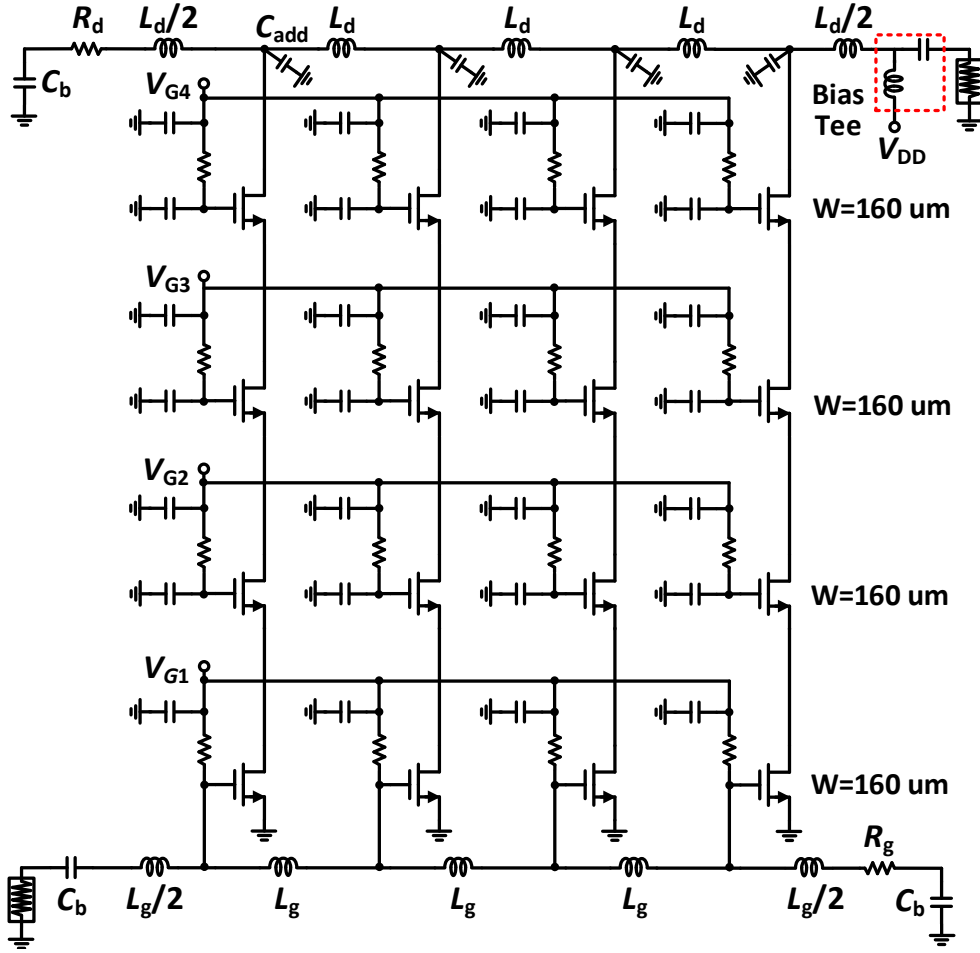
Figure 7.1: Four-stack, four-stage distributed amplifier topology.

To keep a uniform delay, L_g and L_d are set to the same value of 640 pH. Similarly, $C_{g\text{-}p}$ should equal to $C_{d\text{-}p}$. Since the parasitic capacitance at the gate is larger than at the drain, an additional capacitor is placed at the top transistor drain ($C_{add} = 50$ fF).

In theory, the gain of a N-stage distributed amplifier can be expressed as:

$$\text{Gain} = \frac{N \times g_m \times Z_0}{2} \tag{7.3}$$

where g_m is the transconductance of a single amplifier stage. In reality, however, the gain does not increase linearly with the number of stages used due to the TL loss. Therefore, a compromise is made by choosing N=4 to fulfill the overall gain, output power, and PAE requirements. Also,
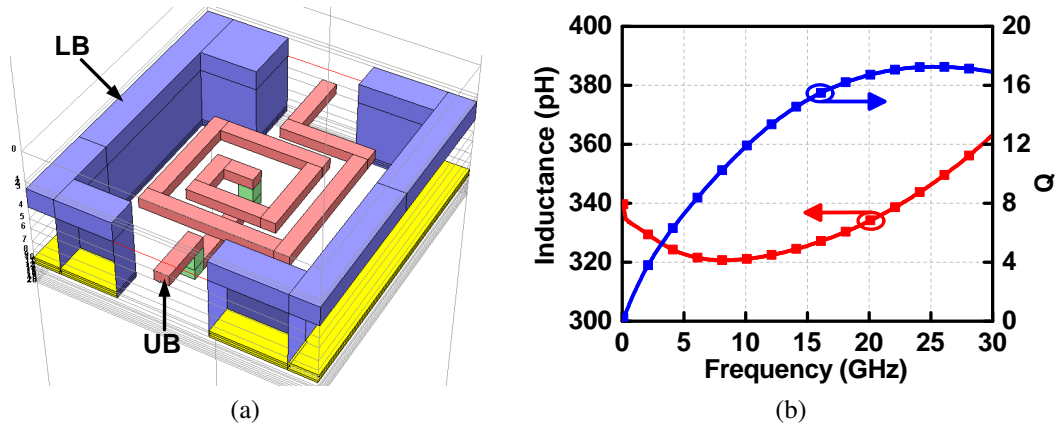
Figure 7.2: (a) Structure of 330 pH inductor; (b) Simulated inductance and quality factor (Q).

larger devices provide higher gm but on the other hand exhibit larger parasitics and limit the DA bandwidth. Therefore, in this design, a 160 μm wide device is used for all transistors as a trade-off between bandwidth and gain.

The DA is implemented in GF 45 nm CMOS SOI, which has a peak f_t/f_{max} of 260/300 GHz referenced to the top metal [14]. The technology provides 11 metal layers and two thick top metal layers (LB and UB). To improve the quality factor, inductors are designed using the UB layer. Fig. 7.2 presents the spiral inductor (L_g/2 and L_d/2) layout and quality factor. The inductors are surrounded by a ground shielding box (LB layer) to minimize the mutual coupling between the different stages. All the inductors and inter-connections are characterized using a 2.5-D EM software (Sonnet), and the mutual coupling between neighboring inductors is taken into account (<-30 dB).

Fig. 7.3a presents a single stage design with four-stack transistors. To maximize the voltage headroom, the transistor gate bias (V_{G1}-V_{G4}) are chosen so that each transistor has the same V_{DS} and V_{GS}. Also, the ac signal needs to be distributed evenly throughout the four transistors. This is achieved by choosing the additional gate capacitors (C_2-C_4), where C_i (i=2, 3, 4) and the gate to source capacitance (C_{gsi}) to form a voltage divider and generate the in-phase voltage swing at the gate and the drain. Fig. 7.3b presents the simulated gate voltage swing of each transistor at input power of 6 dBm (well into compression). Note that V_{gs} or V_{ds} for each
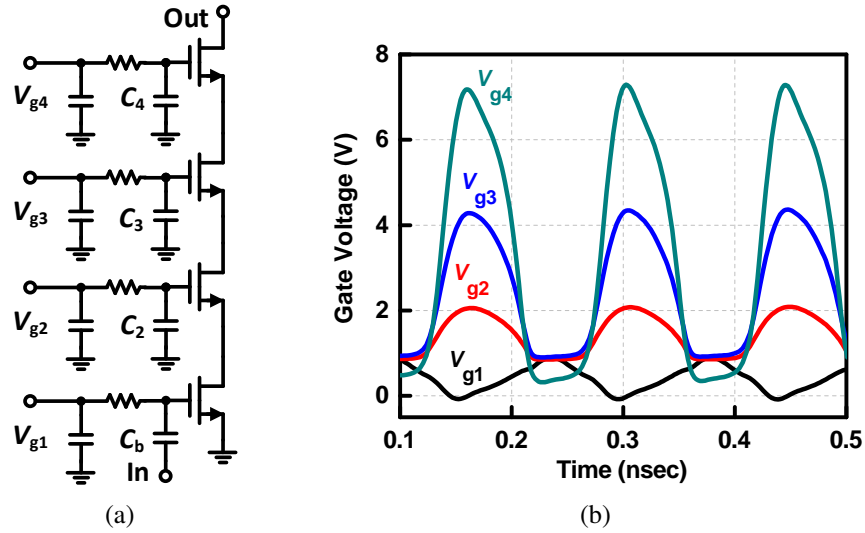
Figure 7.3: (a) Structure of stacked transistors (b) Simulated gate waveforms.
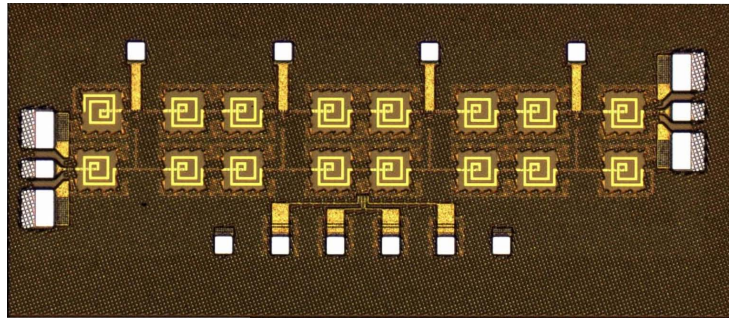
Figure 7.4: Microphotograph of the distributed amplifier.

transistor remains lower than 2.2 V avoiding breakdown.

7.2.2 Measurement

Fig. 7.4 presents a microphotograph of the DA with a size of 1.9 mm × 0.6 mm. All measurements are performed on-chip using GSG probes. The S-parameters, P1dB and the output power are obtained using Keysight N5247A PNA-X. The PNA-X also provides the required bias-tee for the output port.

Fig. 7.5a presents the simulated and measured S-parameters under 4.4 V supply and a bias current of 97 mA. The input and output matching are < -10 dB at 1-20 GHz. The maximum
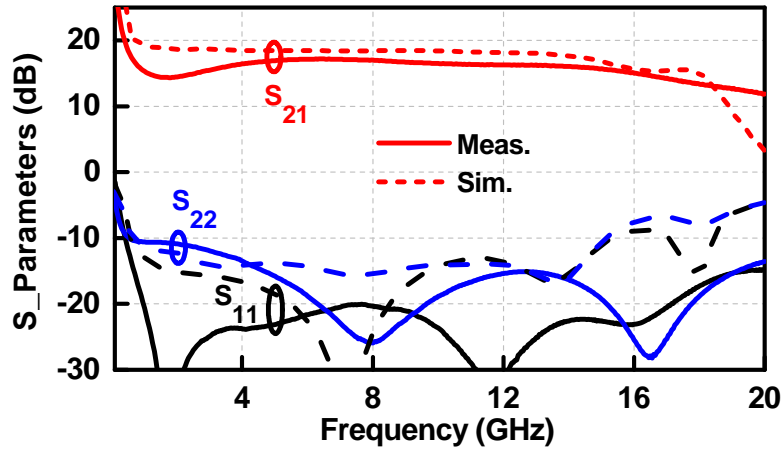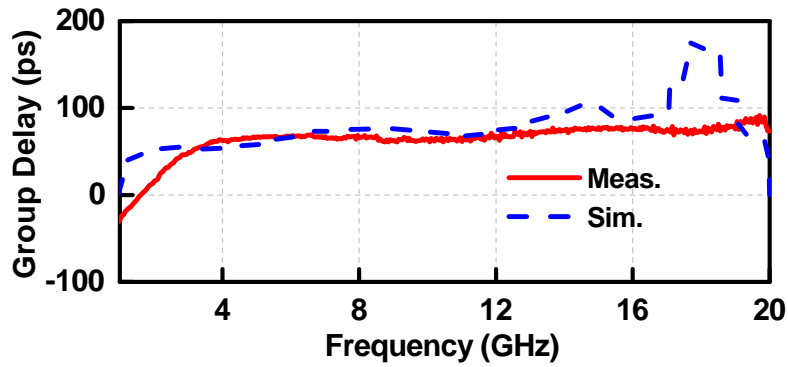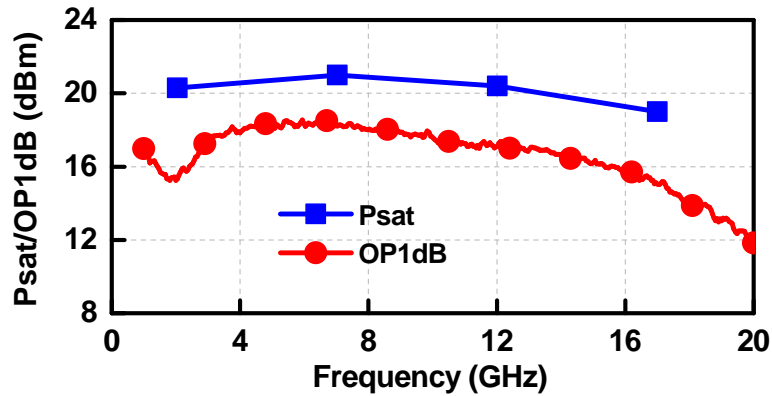
Figure 7.5: Measured distributed amplifier: (a) S-parameters, (b) group delay and (c) OP1dB and Psat.

S_{21} is 17.1 dB with a 3-dB small-signal bandwidth of 1-17 GHz. The measured S-parameters show a high-pass response at 1 GHz due to the DC block capacitor (C_b). The measured NF is
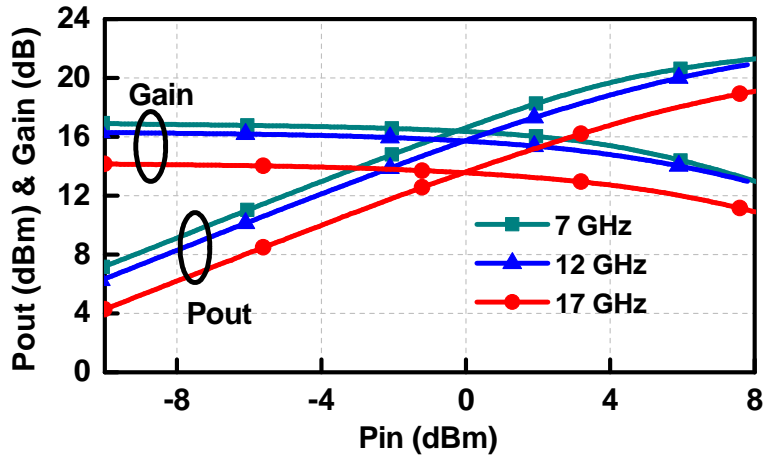
Figure 7.6: Measured gain and output power versus input power.

3.5-7.2 dB at 1-17 GHz. The measured group delay varies by $< \pm 15$ ps at 1-17 GHz (Fig. 7.5b). Fig. 7.5c presents the measured output P1dB and Psat at 2, 7, 12 and 17 GHz.

Fig. 7.6 presents the measured output power and gain versus input power at 7, 12 and 17 GHz. The saturated output power (Psat) is defined as the corresponding output power when the linear gain decreases by 3 dB (P1dB+2dB). Based on this definition, the Psat at 7, 12 and 17 GHz are 21, 20.4 and 19 dBm with a PAE of 19%, 16.3% and 12.2%, respectively. A maximum Psat of 20 dBm with a PAE of 14% is achieved at 17 GHz if this definition is not followed.

Fig. 7.7 presents the Error Vector Magnitude (EVM) measurement setup. A modulated signal is generated by a Keysight M8195A Arbitrary Waveform Generator (AWG) and amplified using a wideband IF amplifier. The output DA signal is directly fed into the Keysight DSO-S 804A real-time Scope for EVM analysis. At -3 dB backoff, the measured EVM for 16 QAM (20 Gb/s) and 64 QAM (30 Gb/s) are 3% and 2.5%, respectively. The DA can sustain a 256-QAM signal with 40 Gbps and 2% EVM (this can be further improved using digital pre-distortion). Note that the 2-7 GHz signal is due to the scope bandwidth limitations (up to 8 GHz). The DA can support a much higher data rate if its full bandwidth is utilized.

Table 7.1 presents a comparison of recent CMOS distributed amplifiers and the proposed amplifier. This work demonstrates the highest output power for a wideband CMOS DA.
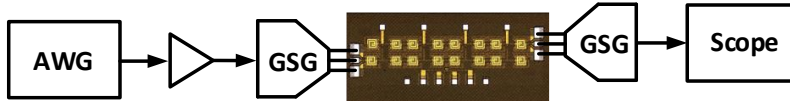
(a)
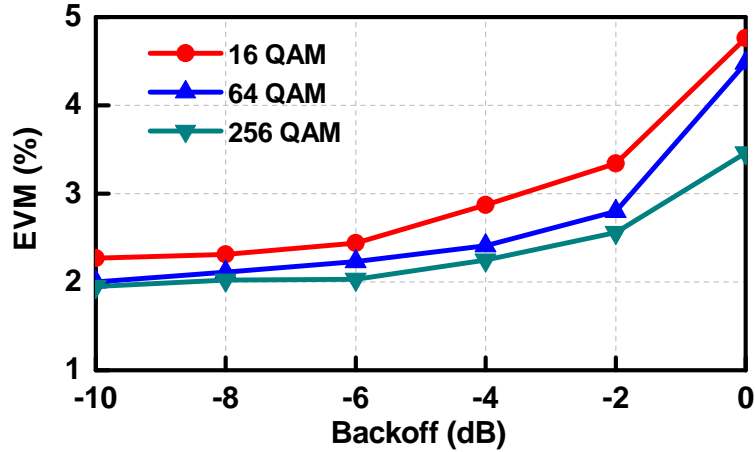
(b)

Figure 7.7: (a) EVM measurement setup. (b) Measured EVM versus modulation scheme and backoff (Carrier = 4.5 GHz, Bandwidth = 2-7 GHz, Symbol Rate=5 Gbaud/s).

Table 7.1: Comparison with Previous Distributed Amplifiers

Ref.	Tech.	BW (GHz)	Psat (dBm)	Gain (dB)	P_{dc} (mW)	Size (mm^2)
[100]	45-nm SOI	DC-92 GHz	N.A	9	73.5	0.45
[101]	0.18-μm CMOS	DC-33 GHz	7.2-12.4	24	238	0.83
[104]	0.13-μm CMOS	2-16 GHz	15.5-18	10	300	0.82
[105]	0.18-μm CMOS	2-22 GHz	12.7-16.7	11.9	260	1.7
This work	45-nm SOI	1-17 GHz	19-21	17.1	427	1.14

7.3   Conclusion

This chapter presented A four-stage four-stack 1-17 GHz distributed amplifier in 45-nm CMOS SOI. The circuit exhibits a maximum gain of 17.1 dB, 19-21 dBm Psat, with a peak PAE of 12.2-19% over the entire bandwidth, and can support complex modulated signals at -3 dB

backoff. Measured results agree well with simulations.

7.4   Acknowledgment

Chapter 8

Conclusion and Future Work

8.1 Conclusion

Increased connectivity is changing the world by new applications of wireless technologies, such as mm-wave 5G and internet of things (IoT). Recent developments CMOS technologies have enabled high-performance phased-array beamformers and transceivers for mm-wave 5G. The wideband phased-array beamformers and transceivers not only meet the requirements of high data-rate transfer but also provide a low-cost solution for multi-band multi-applications. This dissertation described several wideband phased-array beamformers and transceivers for mm-wave 5G application. The following summarizes the key points and results presented in the dissertation.

In chapter 2, a wideband phased array receiver channel that covers the entire 22-44 GHz millimeter wave 5G band in GF 45-nm CMOS SOI has been proposed. The LNA was designed with flat gain in 19-47 GHz with low NF, which ensure the low NF of the overall receive channel. Both the VGA and vector modulator used three-stack amplifier to realize wide bandwidth. The receiver channel has realized a peak gain of 26.3 dB with 3 dB bandwidth of 20.5-44 GHz with NF of 3-3.6 dB. The phase and gain rms error is is < 6° and < 1.9 dB. Both the single blocks and the channel achieve state-of-the-art performance.

In chapter 3, a wideband mm-wave front-end has been proposed. The LNA was realized by two stage cascode amplifier, which achieves 20 dB gain in 20-44 GHz with < 3 dB NF. The SPDT was designed by stacked shunt-series topology, which achieves < 1 dB insertion loss and > 20 dBm IP1dB. The dual-band PA was designed by using switchable load line. These three blocks were then co-optimized in a high-power front-end and resulting in > 18 dBm of output power at 28 GHz and at 36 GHz, including the SPDT switch loss and compression.

In chapter 4, a wideband image rejection receiver that covers the 22-44 GHz millimeter-wave 5G band in 22-nm CMOS SOI has been proposed. The LNA presented a flat gain response at 24-29 GHz and 37-43 GHz with a low NF. A very high tolerance to the out-of-band interferers was observed, which helps to remove the lossy passive filters between the antenna and the LNA. The SSB receiver has a maximum small-signal gain of 28.5 dB and maintains > 24 dB gain at 20-44 GHz with P_{dc} of 70 mW. The receiver NF is < 5 dB over the whole band, with an IRR of > 75 dB by using a IF of 16 GHz.

In chapter 5, a wideband IQ receiver that covers 24-42 GHz millimeter-wave 5G band has been proposed. Three stage 22 dB gain wideband LNVGA was designed to ensure low NF for the whole receiver. A modified QAF network was used to generate wideband low mismatch IQ for mixer. The whole receiver has a measured peak gain of 22.3 dB with 3 dB bandwidth of 22 GHz. And the gain can be adjusted by the LNVGA for 7-9 dB. The measured SSB NF was 5.2-7 dB and the IP1dB was around -25 dBm. The measured gain and phase mismatch is <1 dB and 5°.

In chapter 6, the first 22-nm CMOS FD-SOI LNAs at *E*- and *W*-band has been demonstrated. The proposed drain-to-gate transformer-loaded cascode stage was analyzed, and then two different three-stage cascode LNAs are designed and implemented. The *E*-band LNA realizes a peak gain of 20 dB with a 3-dB bandwidth of 13 GHz, 4.6 dB NF, and consumes only 9 mW of P_{dc}. The *W*-band LNA has a peak gain of 18.2 dB with 31 GHz bandwidth, 5.8 dB NF, and consumes only 16 mW of dc power. This chapter also demonstrates a *W*-band LNA in 45-nm CMOS SOI with peak gain of 12 dB, NF of 4.2 dB and P_{dc} of 4.7 mW. Both LNAs, wideband

and narrowband, in both process achieve state-of-the-art FoM values.

In chapter 7, a four-stage four-stack 1-17 GHz distributed amplifier has been demonstrated in 45 nm CMOS SOI. The circuit exhibits a maximum gain of 17.1 dB, 19-21 dBm Psat, with a peak PAE of 12.2-19% over the entire bandwidth, and can support complex modulated signals at -3 dB backoff.

8.2   Future Work

Both the millimeter-wave beamformers and transceivers presented in this dissertation can be further expanded in a few different ways.

For the millimeter-wave beamformers, they can be improved in the following directions: 1) The VGA can be designed with phase-invariant behavior since it is preferred that the phase and amplitude of each antenna element is controlled independently, which is helpful for phased-array calibration. 2) The chip area can be reduced by changing the inductors to transformers. 3) Add a wideband transmit beamformer channel and put together with the current receive beamformer channel with a wideband SPDT. 4) Build wideband PCB antennas and package the chip on the PCB to realize a complete phased-array beamformer.

In terms of the transmit/receive front-end and receivers, future work can focus on the following directions: 1) Improve the PA gain flatness for the front-end design. The current PA exhibits high output power, but the gain difference between 28 GHz band and 39 GHz band is large, which can be improved by carefully designing the output matching network. Also a stacked switch with 3-4 transistors can be designed to improve the P1dB of the SPDT and therefore improve the Tx output power. 2) Design another IQ mixer for the SSB receiver to down-convert the IF signal to baseband. Also add the LO leakage cancellation circuit, as shown in Fig. 4.2, to complete the receiver. 3) Use polyphase filter to combine the IQ signal for the IQ receiver, which will reject the image and improve the NF.

Finally, the wideband phased-array beamformer and transceiver can be designed together to realize a complete wideband phased-array transceiver system with packaging and insertion in a wideband mm-wave phased-array.

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