Title

A 48-V-to-1-V Switching Bus Converter for Ultra-High-Current Applications

Authors

Zhu, Yicheng
Ge, Ting
Ellis, Nathan M
et al.

Publication Date

2023-06-28

DOI

10.1109/compel52896.2023.10221149

Proceedings of the 24th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2023), Ann Arbor, MI, USA, 25-28 June, 2023

A 48-V-to-1-V Switching Bus Converter for Ultra-High-Current Applications

Y. Zhu
T. Ge
N. Ellis
J. Zou
R. C. N. Pilawa-Podgurski

A 48-V-to-1-V Switching Bus Converter for Ultra-High-Current Applications

Yicheng Zhu, Ting Ge, Nathan M. Ellis, Jiarui Zou, and Robert C. N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Email: {yczhu, gting, nathanmilesellis, jiarui.zou, pilawa}@berkeley.edu

***Abstract*—This paper presents an ultra-high-current switching bus converter with direct 48-V-to-1-V power conversion for next-generation ultra-high-power digital loads (e.g., CPUs, GPUs, ASICs, etc.). In the proposed topology, two 2-to-1 switched-capacitor (SC) front-ends are merged with four 10-branch series-capacitor buck (SCB) modules through two switching buses. Compared to the DC-bus-based architecture, the switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. Through two-phase operation within each SCB module, the switching bus converter extends the maximum duty ratio and achieves a very large SC stage conversion ratio of 20-to-1. Compared to existing 48-V-to-1-V hybrid SC demonstrations, the proposed topology has the lowest normalized switch stress and the smallest normalized passive component volume, showing great potential for both higher efficiency and higher power density than prior solutions. A 48-V-to-1-V hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards. Hybrid gate drive circuitry comprising gate-driven charge pump circuits and cascaded bootstrap circuits was customized for the high-side switches in the SCB modules to overcome the challenge of accumulative voltage drops in the conventional cascaded bootstrap circuit. The hardware prototype was tested up to 1200-A output current and achieved 92.4% peak system efficiency, 87.5% full-load efficiency (including gate drive loss), and 607 W/in^3 power density (by box volume).**

I. Introduction

In recent years, as microprocessors (e.g., CPUs, GPUs, ASICs, etc.) become more computationally powerful, their electric power demands have grown dramatically. The power consumption of next-generation digital loads is expected to reach 1000 W, with core logic voltages below 1.0 V and peak current demand beyond 1000 A. Meanwhile, as modern data centers shift towards the 48-V bus architecture from the legacy 12-V bus architecture, the design of the voltage regulation modules (VRMs) responsible for the 48-V to Point-of-Load (PoL) power conversion is becoming increasingly challenging due to the quadrupled voltage conversion burden. In particular, the continued increase in power levels with maintained or even reduced space for power conversion leads to an ever-increasing demand for higher power density. Moreover, higher power conversion efficiency is required for easier thermal management and reduced electricity consumption of data centers.

The main challenges of 48-V-to-PoL power conversion include: i) high conversion ratio, ii) high output current, iii) high efficiency, iv) high power density, and v) fast transient response. Various solutions have been proposed to address these challenges, and they can be classified into two categories: 1) transformer-based solutions [1]–[3] , and 2) hybrid switched-capacitor (SC) solutions [4]–[14]. As an emerging family of topologies, hybrid SC converters have received increased attention, since they can leverage both the greatly superior energy density of capacitors compared to magnetics [15], [16] and the better figure-of-merit (FOM) of low-voltage switching devices compared to high-voltage devices [17].

This paper presents a high-performance 48-V-to-1-V hybrid SC converter for next-generation ultra-high-current digital loads. In the proposed topology, two 2-to-1 SC front-ends are merged with four 10-branch series-capacitor buck (SCB) modules through two switching buses, achieving a very large SC stage conversion ratio of 20-to-1. Compared to the DC-bus-based architecture, the switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. Through a topological comparison based on the normalized switch stress and the normalized passive component volume, it is shown that the proposed topology has great potential for both higher efficiency and higher power density than prior solutions. A 48-V-to-1-V hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards. Hybrid gate drive circuitry was designed for the high-side switches in the SCB modules to overcome the challenge of accumulative voltage drops in the conventional cascaded bootstrap circuit. The hardware prototype was tested up to 1200-A output current and achieved excellent performance which surpasses existing state-of-the-art solutions.

II. Switching Bus Converter

A. Circuit Topology and Operating Principles

Fig. 1 shows the schematic drawing of the proposed switching bus converter. It comprises two stages: 1) two 2-to-1 SC front-ends as Stage 1, and 2) four 10-branch series-capacitor-buck (SCB) modules (i.e., Modules A-D) as Stage 2. The two stages are merged through four switching buses (i.e., Switching buses A-D). As shown in Fig. 2, the bus voltages v_{swA}-v_{swD} always switch between two different levels. Therefore, this type of intermediate bus is referred to as a *switching bus*.

As can be seen in Figs. 1 and 2, each SCB module consists of five submodules and operates in a two-phase fashion with a 180° phase shift between neighboring branches. The control signals of Modules C and D are 90° phase shifted with respect

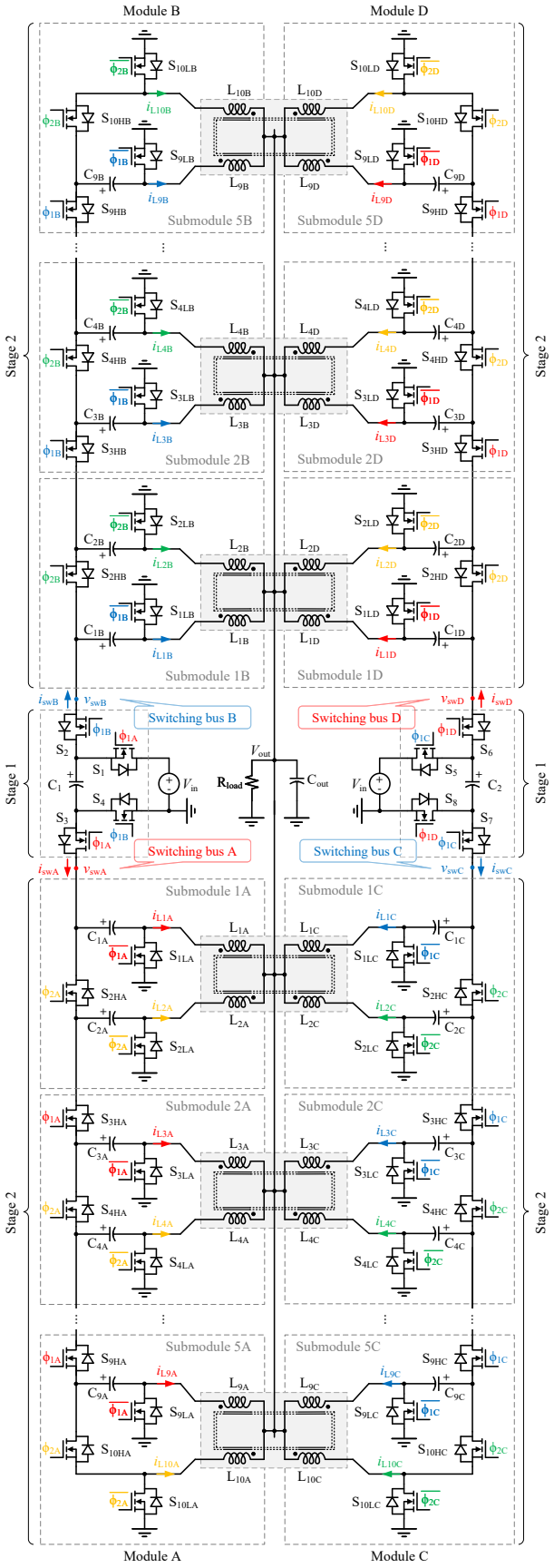


Fig. 1: Schematic drawing of the proposed switching bus converter.

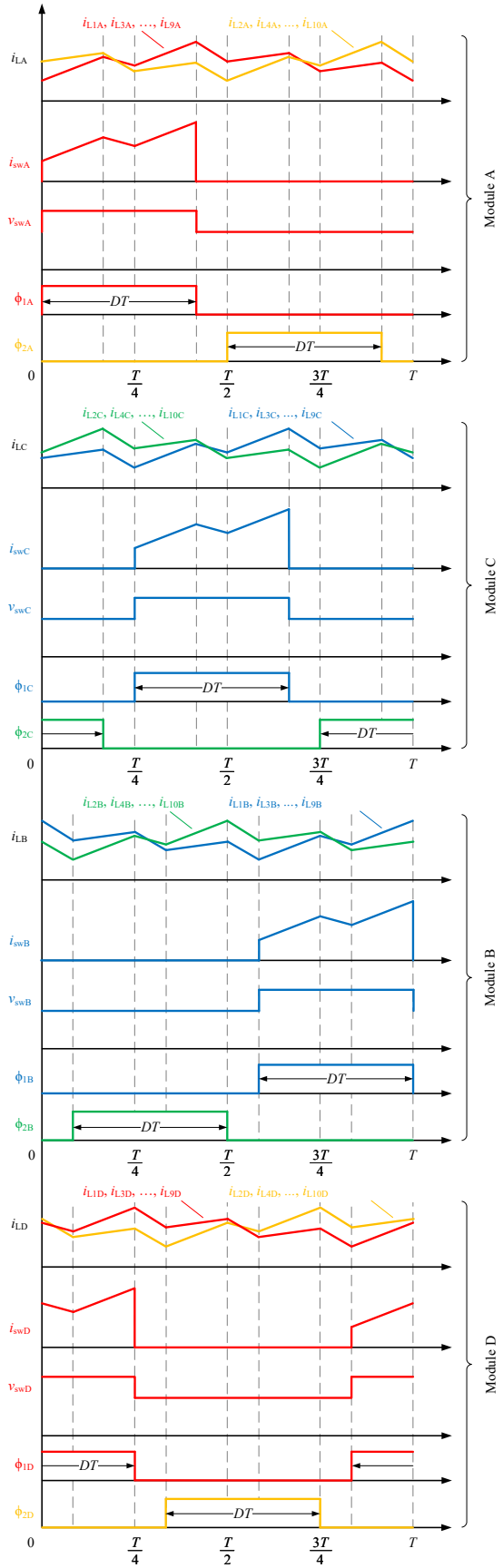


Fig. 2: Key waveforms and control signals.

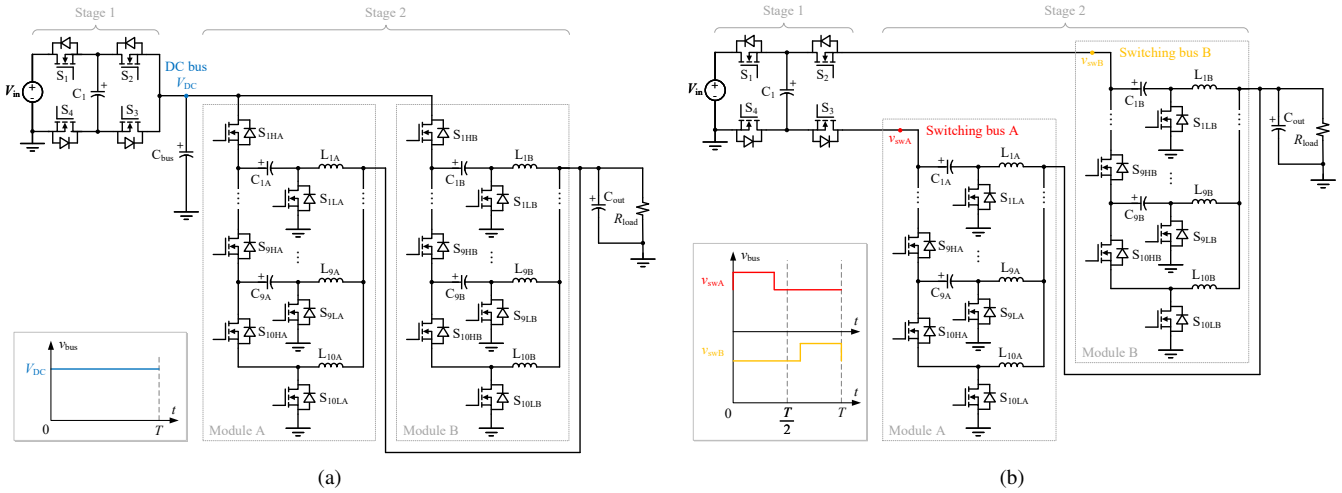


Fig. 3: Comparison between the DC-bus-based architecture and the proposed switching-bus-based architecture. (a) DC-bus-based architecture. (b) Switching-bus-based architecture. Compared to the DC-bus-based architecture, the proposed switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

TABLE I: Topological comparison between this work and existing 48-V-to-1-V hybrid SC demonstrations

Year	Reference	SC Stage Conversion Ratio	Buck Stage Conversion Ratio	Buck Stage Duty Ratio	Normalized Switch Stress	Normalized Passive Component Volume
2020	Crossed-coupled QSD buck [4]	4:1	12:1	0.083	24.2	2.08
2020	DIH [5]	6:1	8:1	0.125	14.7	2.40
2021	CaSP [6]	6:1	8:1	0.125	23.5	2.02
2022 2023	LEGO [7] Mini-LEGO [8]	6:1	8:1	0.125	17.6	2.41
2023	SDIH [9]	6:1	8:1	0.125	14.7	2.40
2022	MLB [10]	8:1	6:1	0.167	23.7	2.03
2022	VIB [11]	8:1	6:1	0.167	14.3	2.07
2023	MSC [12]	8:1	6:1	0.167	15.1	1.95
2022	Dickson^2 [13]	9:1	5.33:1	0.188	14.8	1.90
2023	16-to-1 SBC [14]	16:1	3:1	0.333	10.2	1.69
2023	This work	20:1	2.4:1	0.417	8.99	1.56

to those of Modules A and B so that the four inductors grouped in the gray rectangles are four-phase interleaved with a 90° phase shift and can be implemented as four-phase coupled inductors with higher energy density and faster dynamic response than discrete inductors.

The output voltage of the proposed switching bus converter can be regulated through duty cycle control as

$$V_{\text{out}} = \frac{D}{20} V_{\text{in}}, \tag{1}$$

where V_{in} and V_{out} are the input and output voltages, respectively, and D is the duty ratio with respect to the switching period T as illustrated in Fig. 2.

B. Advantages of the Switching-Bus-Based Architecture

The most straightforward approach to combining two (or multiple) conversion stages is to link them with an intermediate DC bus, as illustrated in Fig. 3(a). This DC-bus-based architecture typically requires a large DC bus capacitor (C_{bus}) to maintain a stiff bus voltage (V_{DC}), which hinders converter miniaturization.

Compared to the DC-bus-based architecture, the proposed switching-bus-based architecture shown in Fig. 3(b) has three advantages that promise higher performance:

- It does not require a large and bulky decoupling capacitor to maintain a stiff DC bus voltage.
- One redundant switch can be removed on each switching bus while two stages are merged together.
- It can ensure complete soft-charging operation for all flying capacitors.

In Fig. 3(b), when Stage 1 and Stage 2 are merged, the original highest high-side switches in Module A ($\text{S}_{1\text{HA}}$ in Fig. 3(a)) is connected in series with S_3 in Stage 1. Similarly, $\text{S}_{1\text{HB}}$ in

Module B is connected in series with S_2. Since the switching buses do not need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, compared to the DC-bus-based architecture, the switching-bus-based architecture enables a reduction in the number of switches.

C. Theoretical Analysis and Topological Comparison

Compared to the conventional multi-phase operation of the series-capacitor-buck (SCB) converter [18], the two-phase operation illustrated in Fig. 2 extends the maximum duty ratio from $\frac{1}{N}$ to $\frac{1}{2}$, where N is the number of branches in the SCB converter. As a result, the upper limit on the number of branches ($N_{\mathrm{m-ph}}$ and $N_{2-\mathrm{ph}}$) in a SCB converter with fixed input and output voltages ($V_{\mathrm{in(SCB)}}$ and $V_{\mathrm{out(SCB)}}$) can be increased:

$$\text{Multi-phase operation: } N_{\mathrm{m-ph}} < \sqrt{\frac{V_{\mathrm{in(SCB)}}}{V_{\mathrm{out(SCB)}}}} \tag{2}$$

$$\text{Two-phase operation: } N_{2-\mathrm{ph}} < \frac{V_{\mathrm{in(SCB)}}}{2V_{\mathrm{out(SCB)}}}. \tag{3}$$

For the proposed switching bus converter shown in Fig. 1, the input and output voltages of the SCB modules in Stage 2 are $V_{\mathrm{in(SCB)}} = 24$ V and $V_{\mathrm{out(SCB)}} = 1$ V, respectively. Therefore, the maximum allowable numbers of branches in the SCB modules for multi-phase operation and two-phase operation are $N_{\mathrm{m-ph(max)}} = 4$ and $N_{2-\mathrm{ph(max)}} = 10$, respectively. Since the switch voltage stress and inductor volt-second stress in a SCB converter decrease as the number of branches increases, a SCB converter with more branches can have less switching device losses and smaller inductor volume. In addition, changing the control scheme of the SCB modules from the conventional multi-phase operation to the two-phase operation can also improve transient response with an extended maximum duty ratio.

To compare the theoretical potential of the proposed topology to that of existing 48-V-to-1-V hybrid SC topologies, this paper uses two metrics for topological comparison. The first metric is the normalized switch stress [16], defined as the total volt-ampere (VA) stress on the switches in a topology normalized by the output power:

$$\text{Normalized switch stress} = \frac{\sum V_{\mathrm{ds}} I_{\mathrm{d(rms)}}}{V_{\mathrm{out}} I_{\mathrm{out}}}, \tag{4}$$

where V_{ds} and $I_{\mathrm{d(rms)}}$ are the peak blocking voltage across and the RMS current through the switches when assuming no capacitor voltage ripple and no inductor current ripple, respectively. A lower normalized switch stress is desirable, as it indicates lower switching losses and lower conduction losses and thus higher efficiency. The second metric used in the comparison is the normalized passive component volume, where the capacitor and inductor volumes are calculated as the peak energy stored in them divided by their volumetric energy density. This metric indicates the total passive component volume needed to meet the given ripple requirements on the inductor currents and capacitor voltages when transferring one unit of normalized power from the input to the output. A smaller normalized passive component volume is desirable,

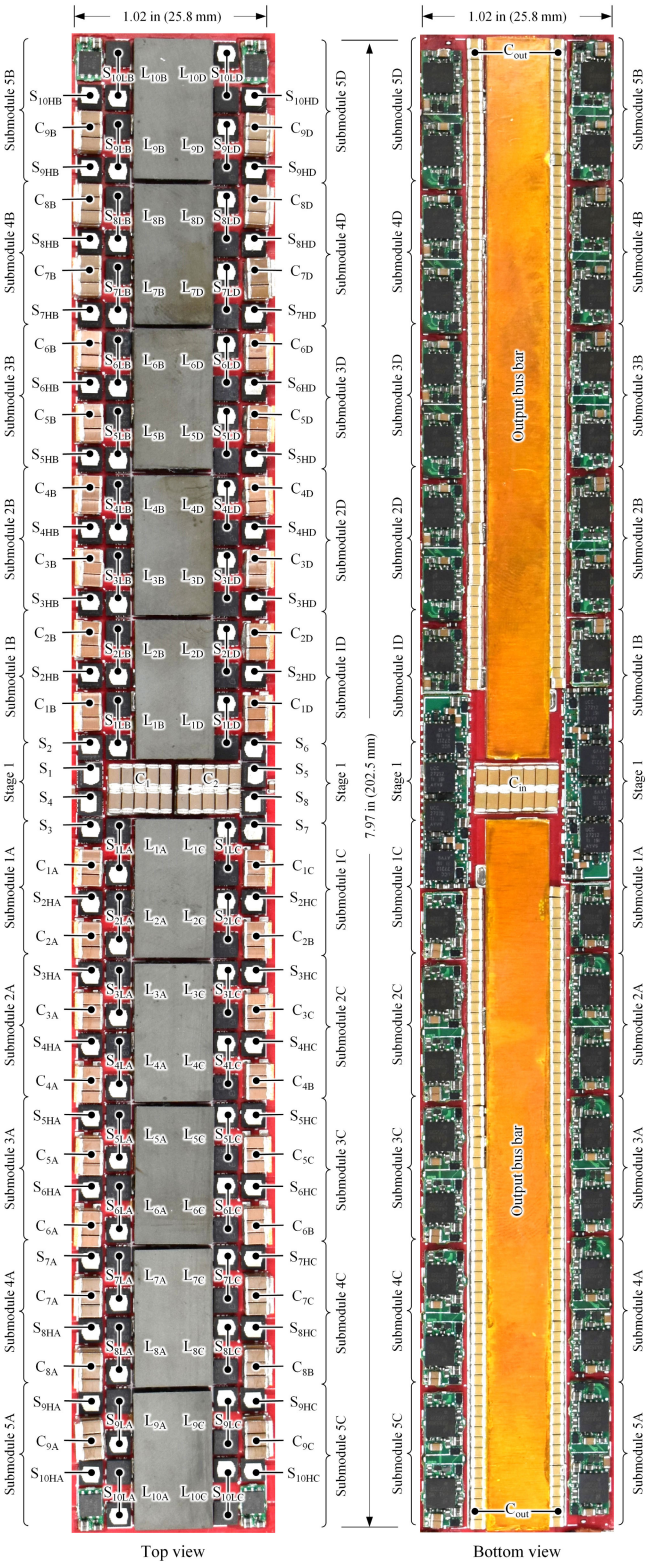
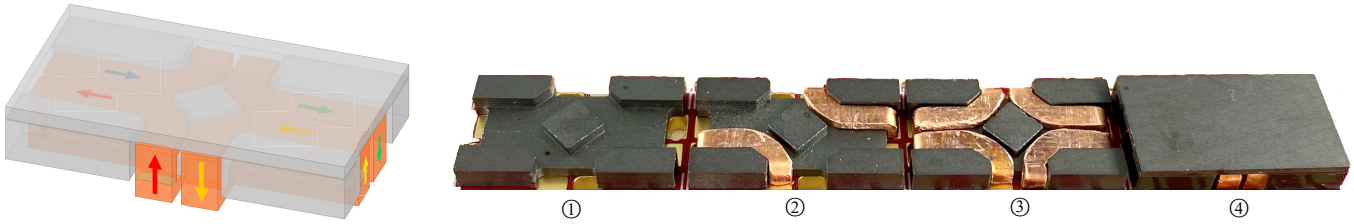


Fig. 4: Photograph of the hardware prototype. Dimensions: $7.97 \times 1.02 \times 0.244$ in^3 ($202.5 \times 25.8 \times 6.2$ mm^3).

TABLE II: Component list of the hardware prototype

Component (X = A, B, C, D)	Part number	Parameters
MOSFET S_{1-8}	Infineon IQE013N04LM6CGSC	40 V, 1.35 mΩ, dual-side cooling
MOSFET $S_{2HX-10HX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 mΩ, dual-side cooling
MOSFET $S_{1LX-10LX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 mΩ, dual-side cooling
	Infineon IQE004NE1LM6	15 V, 0.45 mΩ
Flying capacitor $C_{1,2}$	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 μF*×20 (in parallel)
Flying capacitor C_{1X-6X}	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 μF*×6 (in parallel)
Flying capacitor C_{7X-9X}	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μF*×6 (in parallel)
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 μF*×14 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μF*×248 (in parallel)
Gate driver in Stage 1	Texas Instruments UCC27212	4-A peak source, 4-A peak sink
Low-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source, 5-A peak sink
High-side gate driver in Stage 2	Texas Instruments LM27222	3-A peak source, 4.55-A peak sink

* The capacitance listed in this table is the nominal value before DC derating.



(a) (b)

Fig. 5: Custom four-phase coupled inductor. Dimensions: $18.5 \times 10.5 \times 3.2$ mm^3. (a) 3D view with current paths annotated. (b) Coupled inductor assembly with two pieces of magnetic cores and four pieces of windings: ①→ ②→ ③→ ④ .

as it indicates higher power density.

As listed in Table I, compared with existing 48-V-to-1-V hybrid SC demonstrations, this work achieves the largest SC stage conversion ratio with the lowest normalized switch stress and the smallest normalized passive component volume, showing great potential for both higher efficiency and higher power density than prior solutions. With a larger SC stage conversion ratio, the conversion burden on the following buck stage can be alleviated, enabling buck stage efficiency improvement and inductor size reduction.

III. Hardware Implementation

To validate the functionality and performance of the proposed switching bus converter, a 48-V-to-1-V hardware prototype was built with custom four-phase coupled inductors and gate drive daughterboards. Fig. 4 shows an annotated photograph of the prototype, with the main circuit components listed in Table II. The power board has 6 layers, with 6-oz copper on the two outer layers and 2-oz copper on the four inner layers.

A. Coupled Magnetics

Compared to discrete inductors, coupled inductors can achieve faster transient response without sacrificing steady-state performance [19] and can achieve core volume reduction due to DC flux cancellation [10].

As presented in Fig. 5, a four-phase coupled inductor comprising two pieces of magnetic cores and four pieces of windings was customized and assembled for the hardware prototype. The magnetic cores are fabricated with DMEGC DMR96A Mn-Zn ferrite. The key parameters of the four-phase coupled inductor are listed in Table III.

TABLE III: Key parameters of the four-phase coupled inductor

Parameter	Value
Coupling coefficient	-0.91
Per-phase DC resistance	0.16 mΩ
Equivalent per-phase steady-state inductance*	260 nH
Overall transient inductance (40 phases)	0.80 nH
Height	3.2 mm

* Four-phase average value at $D = 0.417$.

B. Gate Drive Circuitry

As has been mentioned in [14], one practical implementation challenge of the switching bus converter is the gate drive circuitry design for the high-side switches in Stage 2 (i.e., $S_{2HX-10HX}$, X = A, B, C, D). Due to the large number of high-side switches, conventional cascaded bootstrapping suffers from accumulative voltage drops across bootstrap diodes, leading to higher gate drive loss [20]. In [14], the synchronous bootstrap technique [21] was adopted to reduce the voltage drops in the bootstrap circuit by replacing bootstrap diodes with active FETs. Though effective and widely applicable, the synchronous bootstrap circuit has a high component count when implemented with discrete components, which complicates hardware implementation and reduces overall reliability.

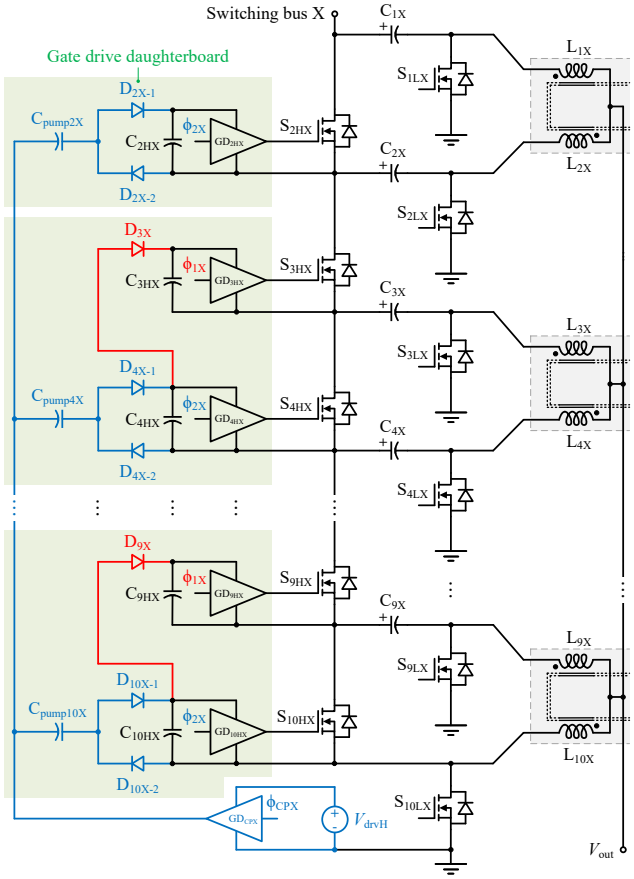


Fig. 6: Gate drive circuitry for high-side switches in Module X (X = A, B, C, D), where switches $S_{2HX,4HX,\cdots,10HX}$ are powered with gate-driven charge pump circuits, and switches $S_{3HX,5HX,\cdots,9HX}$ are powered with cascaded bootstrap circuits. (a) Schematic drawing. (b) Control signals.

This paper proposes custom-designed gate drive circuitry to power the high-side switches in the second stage of the switching bus converter, as illustrated in Fig. 6(a). In the proposed hybrid gate drive circuit, switches $S_{2HX,4HX,\cdots,10HX}$ are powered with gate-driven charge pump circuits [20], and switches $S_{3HX,5HX,\cdots,9HX}$ are powered with cascaded bootstrap circuits. Fig. 6(b) shows the control signals of the proposed hybrid gate drive circuitry. The charge-pump capacitors $C_{pump2X,pump4X,\cdots,pump10X}$ are charged by the flying capacitors $C_{2X,4X,\cdots,10X}$ when $\phi_{CPX} = 0$, and the local decoupling capacitors $C_{2HX,4HX,\cdots,10HX}$ are charged by the added gate driver GD_{CPX} when $\phi_{CPX} = 1$. To ensure proper operation, ϕ_{CPX} must be high when $\phi_{2X} = 1$. Compared to the synchronous bootstrap circuit [21], the proposed hybrid gate drive circuit is simpler and thus easier to implement and mechanically more reliable. In the hardware prototype shown in Fig. 4, the proposed hybrid gate drive circuit is implemented as the green daughterboards mounted on the bottom side of the red power board.

TABLE IV: Key parameters and test conditions of the hardware prototype

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	1.0 V
Maximum tested output current	1200 A (30 A/phase)
Switching frequency	200 kHz
Prototype box volume*	1.98 in^3
Power density by box volume	607 W/in^3

* The box volume is defined as the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry.

IV. Experimental Results and Performance Comparison

The hardware prototype was tested up to 1200-A output current at 1.0-V output voltage, achieving a power density of 607 W/in^3 by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry), as listed in Table IV. As shown in Fig. 7, at 1200-A output current, the highest temperature on the board at thermal equilibrium with air cooling only is 68.1 °C. Given that the coupled inductors are not saturation current limited and the converter is not thermally limited at 1200-A output current, the prototype can handle higher output current. Currently, the 1200-A maximum tested output current is limited by the capability of the DC electronic loads (two Chroma 63203 600-A DC electronic loads) used in this test.

Fig. 8 presents the measured efficiency of the hardware prototype. It achieved 93.8% peak power stage efficiency at 280-A output current and 87.9% full-load power stage efficiency at 1200-A output current. With the gate drive loss included, it achieved 92.4% peak system efficiency at 380-A output current and 87.5% full-load system efficiency.

Table V and Fig. 9 show the performance comparison between this work and the state-of-the-art 48-V-to-1-V works in previous literature. It can be seen that the switching bus converter prototype presented in this paper achieved excellent performance with very high power density and very high efficiency, pushing the Pareto front of Fig. 9 to the upper-right corner.

V. Conclusion

This paper presents a high-performance 48-V-to-1-V hybrid SC converter for next-generation ultra-high-current digital loads (e.g., CPUs, GPUs, ASICs, etc.). The proposed topology comprises two 2-to-1 switched-capacitor (SC) front-ends and four 10-branch series-capacitor buck (SCB) modules, with the two stages merged through two switching buses. Compared to the DC-bus-based architecture, the switching-bus-based architecture does not require DC bus capacitors, reduces the number

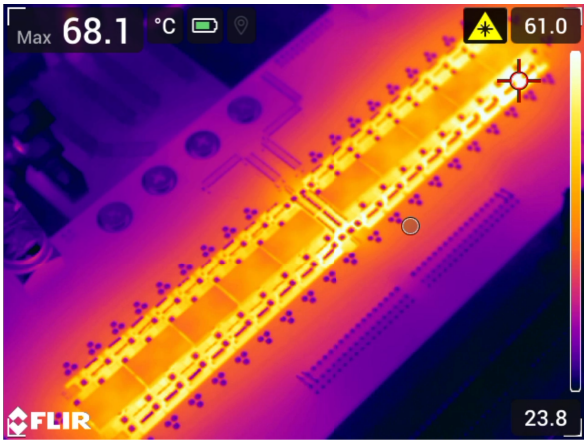


Fig. 7: Thermal image at equilibrium with 220 CFM air cooling only ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 1.0$ V, $I_{\text{out}} = 1200$ A).

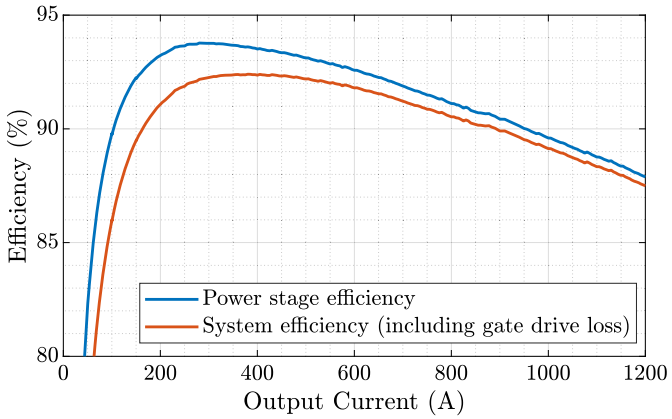


Fig. 8: Measured 48-V-to-1-V efficiency. Peak efficiency: 93.8% at $I_{\text{out}} = 280$ A (92.4% at $I_{\text{out}} = 380$ A including gate drive loss). Full-load efficiency: 87.9% (87.5% including gate drive loss) at $I_{\text{out}} = 1200$ A.

TABLE V: Performance comparison between this work and the state-of-the-art 48-V-to-1-V works

Year	Reference	Output Current	Power Density†	Power Stage Efficiency	System Efficiency‡
2023	This work	1200 A (30 A/phase)	607 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 87.9%	92.4% 87.5%
2023	16-to-1 SBC [14]	500 A (31.3 A/phase)	464 W/in^3 (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2023	MSC [12]	220 A (27.5 A/phase)	607 W/in^3 (by box volume)	Peak efficiency: 92.9% Full-load efficiency: 86.3%	91.1% 85.8%
2023	Mini-LEGO [8]	240 A (20 A/phase)	1390 W/in^3 (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2022	Dickson^2 [13]	270 A (30 A/phase)	360 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [11]	450 A (28.1 A/phase)	232 W/in^3 (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [10]	60 A (30 A/phase)	263 W/in^3 (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	SDIH [9]	105 A (52.5 A/phase)	598 W/in^3 (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2022	LEGO [7]	450 A (37.5 A/phase)	294 W/in^3 (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [4]	40 A (20 A/phase)	150 W/in^3 (by power component volume)	Peak efficiency: 95.1%* Full-load efficiency: 92.7%*	N/A N/A
2020	Sigma [2]	80 A	420 W/in^3 (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

† The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.
‡ Gate drive loss is included in the calculation of system efficiency. *According to direct correspondence with the author.

of switches, and ensures complete soft-charging operation. Through two-phase operation within each SCB module, the switching bus converter extends the maximum duty ratio and achieves a very large SC stage conversion ratio of 20-to-1. Compared to existing 48-V-to-1-V hybrid SC demonstrations, the proposed topology has the lowest normalized switch stress and the smallest normalized passive component volume, showing great potential for both higher efficiency and higher power density than prior solutions. A 48-V-to-1-V hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards. Hybrid gate drive circuitry comprising gate-driven charge pump circuits and cascaded bootstrap circuits is customized to overcome the challenge of accumulative voltage drops in the conventional cascaded bootstrap circuit. The hardware prototype was tested up to 1200-A output current, achieving 92.4% peak system efficiency, 87.5% full-load efficiency (including gate drive loss), and 607 W/in^3 power density (by box volume).

VI. Acknowledgements

The authors would like to thank Infineon Technologies for providing Power MOSFET samples for this work.

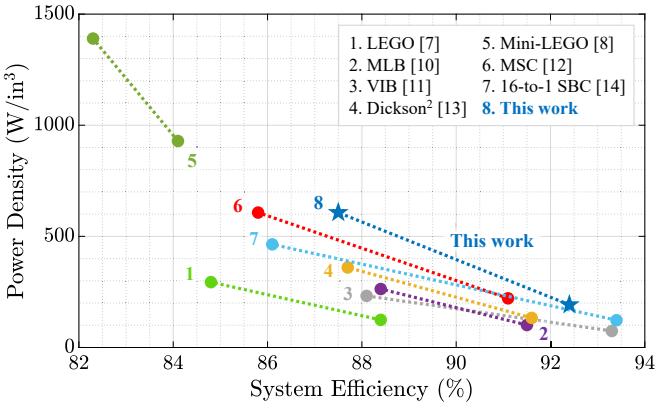


Fig. 9: Performance comparison between this work and the state-of-the-art 48-V-to-1-V works.

REFERENCES

[1] C. Fei, M. H. Ahmed, F. C. Lee, and Q. Li, "Two-Stage 48 V-12 V/6 V-1.8 V Voltage Regulator Module With Dynamic Bus Voltage Control for Light-Load Efficiency Improvement," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5628–5636, 2017.

[2] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-Stage High-Efficiency 48/1 V Sigma Converter With Integrated Magnetics," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 192–202, 2020.

[3] X. Lou and Q. Li, "Multiphase Half-Bridge Current-Doubler Rectifier: A 93.1%-Efficiency Single-Stage 48V Voltage Regulator with 1.04 kW/in3 power density," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1975–1981.

[4] M. Halamicek, T. McRae, and A. Prodić, "Cross-Coupled Series-Capacitor Quadruple Step-Down Buck Converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1–6.

[5] G.-S. Seo, R. Das, and H.-P. Le, "Dual Inductor Hybrid Converter for Point-of-Load Voltage Regulator Modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 367–377, 2020.

[6] Y. Zhu, Z. Ye, T. Ge, R. Abramson, and R. C. N. Pilawa-Podgurski, "A Multi-Phase Cascaded Series-Parallel (CaSP) Hybrid Converter for Direct 48 V to Point-of-Load Applications," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 1973–1980.

[7] J. Baek, Y. Elasser, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, "Vertical Stacked LEGO-PoL CPU Voltage Regulator," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6305–6322, 2022.

[8] Y. Elasser, J. Baek, K. Radhakrishnan, H. Gan, J. Douglas, V. De, S. Jiang, H. K. Krishnamurthy, X. Li, C. R. Sullivan, and M. Chen, "Mini-LEGO: A 1.5-MHz 240-A 48-V-to-1-V CPU VRM with 8.4-mm Height for Vertical Power Delivery," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1959–1966.

[9] N. M. Ellis, R. A. Abramson, R. Mahony, and R. C. N. Pilawa-Podgurski, "The Symmetric Dual Inductor Hybrid (SDIH) Converter for Direct 48V-to-PoL Conversion," *IEEE Transactions on Power Electronics*, doi: 10.1109/TPEL.2023.3259949.

[10] T. Ge, R. Abramson, Z. Ye, and R. C. Pilawa-Podgurski, "Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V Hybrid Switched-Capacitor MLB-PoL Converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1500–1505.

[11] Y. Chen, P. Wang, H. Cheng, G. Szczeszynski, S. Allen, D. M. Giuliano, and M. Chen, "Virtual Intermediate Bus CPU Voltage Regulator," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6883–6898, 2022.

[12] P. Wang, D. Giuliano, S. Allen, and M. Chen, "MSC-PoL: An Ultra-Thin 220-A/48-to-1-V Hybrid GaN-Si CPU VRM with Multistack Switched Capacitor Architecture and Coupled Magnetics," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1967–1974.

[13] Y. Zhu, T. Ge, Z. Ye, and R. C. Pilawa-Podgurski, "A Dickson-Squared Hybrid Switched-Capacitor Converter for Direct 48 V to Point-of-Load Conversion," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1272–1278.

[14] Y. Zhu, T. Ge, N. M. Ellis, L. Horowitz, and R. C. N. Pilawa-Podgurski, "A 500-A/48-to-1-V Switching Bus Converter: A Hybrid Switched-Capacitor Voltage Regulator with 94.7% Peak Efficiency and 464-W/in^3 Power Density," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1989–1996.

[15] J. Zou, N. C. Brooks, S. Coday, N. M. Ellis, and R. C. Pilawa-Podgurski, "On the Size and Weight of Passive Components: Scaling Trends for High-Density Power Converter Designs," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–7.

[16] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and Comparison of Passive Component Volume of Hybrid Resonant Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 903–10 919, 2022.

[17] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020.

[18] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of Double Step-Down Two-Phase Buck Converter for VRM," in *INTELEC 05 - Twenty-Seventh International Telecommunications Conference*, 2005, pp. 497–502.

[19] P.-L. Wong, P. Xu, P. Yang, and F. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 499–507, 2001.

[20] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2020.

[21] N. M. Ellis, R. Iyer, and R. C. Pilawa-Podgurski, "A Synchronous Bootstrapping Technique with Increased On-time and Improved Efficiency for High-side Gate-drive Power Delivery," in *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2021, pp. 462–466.