A High-Speed Multi-Channel Readout for SSPM Arrays

Martin Janecek, Jean-Pierre Walder, Patrick J. McVittie, Bob Zheng, Henrik von der Lippe, *Member, IEEE,* Mickel McClish, Purushottam Dokhale, Christopher J. Stapels, James F. Christian, *Member, IEEE,* Kanai S. Shah, and William W. Moses, *Fellow, IEEE*

***Abstract*—Solid-state photomultiplier (SSPM) arrays are a new technology that shows great promise to be used in PET detector modules. To reduce the number of channels in a PET scanner, it is attractive to use resistor dividers, which multiplex the number of channels in each module down to four analog output channels. It is also attractive to have SSPMs with large pixels (3x3 or 4x4 mm^2). However, large area SSPMs have correspondingly large capacitances (up to 1 nF) and directly coupling them to a resistive network will create a low-pass filter with a high RC time constant. In order to overcome this, we have developed an application specific integrated circuit (ASIC) that "hides" the intrinsic capacitance of the SSPM array from a resistive network with current buffers, significantly improving the rise time of the SSPM signals when connected to the resistive network. The ASIC is designed for a wide range of SSPM sizes, up to 1 nF (equivalent to 4x4 mm^2), and for input currents of 1 to 20 mA per channel. To accommodate various sizes of SSPM pixels, the ASIC uses adjustable current sources (to keep the feedback loop stable). A test ASIC has been fabricated that has 16 input channels, an internal resistor divider array that produces four analog outputs, 16 buffers that isolate the SSPM capacitance from the resistor array, and four output buffers that can drive 100 ohm loads. Thus, detector modules based on SSPMs and this ASIC should be compatible with the block detector readout electronics found in many PET cameras. Tests of this ASIC show that its rise time is <2 ns (and it will thus not significantly degrade the ~7 ns rise time of the SSPM pixels) and that the analog decoding circuitry functions properly.**

***Index Terms*— MPPC, SSPM, SiPM, SPM, G-APD, MRS-APD, ASIC, resistor network, Anger logic, readout time**

I. Introduction

SOLID-STATE Photomultipliers (SSPMs) are a promising technology to replace photomultiplier tubes (PMTs) in Positron Emission Tomograph (PET) detector modules. The SSPM's small size, its insensitivity to magnetic fields, and the potential to be made inexpensively (when mass-produced) are some of the traits that make these devices a very interesting alternative to the current technology of PMTs in PET detector modules [1-4]. These advantages possessed by SSPMs enable the next generation of PET scanners to be made more compact (and in turn, with higher sensitivity and higher resolution) and to be used in conjunction with magnetic resonance imaging (MRI). In addition, the SSPM can possess a high timing resolution (<1ns) [4-7], allowing the SSPM photodetector technology to be implemented in time-of-flight PET [8].

A modern PET scanner contains a very high number of detector channels, and there is therefore a need for a channel reduction scheme. For instance, a PET scanner with 40-cm diameter and 25-cm axial field-of-view, and with 1.5 x 1.5 mm^2 pixels has over 130,000 detector elements. To reduce the number of electronics channels in a PET scanner, it is attractive to use resistor dividers, which multiplex the number of channels for each detector module to four analog output channels [9]. These four channels contain spatial information about where in the detector module an event took place. To directly couple an SSPM to a resistive network is problematic as the intrinsic capacitance of the SSPM and the resistors will produce an RC-circuit, compromising the rise time. This problem is especially problematic for larger SSPM pixels, such as 3x3 or 4x4 mm^2, which can have quite a significant intrinsic capacitance.

The aim of this work is to develop an Application Specific Integrated Circuit (ASIC) that hides the SSPM's intrinsic capacitance from the resistive network with current buffers. This will allow SSPM arrays to be read out without any additional time degradation, while also reducing the number of output channels to four. The ASIC needs to be general in the sense that it needs to accommodate various capacitances up to 1 nF, which is equivalent to 4x4 mm^2 SSPM pixels. This ASIC in combination with an SSPM array should be able to replace the current setup of PMTs and resistive charge-dividing networks used in today's PET detectors, producing a compact and magnetic insensitive photodetector that can be read out at high speeds with a reduced number of output channels. Although each of the building blocks in this ASIC is well-known technology, the ASIC as a whole is a new application that will enable SSPM arrays to replace PMTs in PET detector modules.

We report in this paper on the design requirements of the

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M. Janecek, J.-P. Walder, P. J. McVittie, B. Zheng, H. v. d. Lippe, and W. W. Moses are with the Lawrence Berkeley National Laboratory, Berkeley, CA 94720 USA (phone: 510-486-5579; fax: 510-486-4768; e-mail: mjanecek@lbl.gov).

M. McClish, P. Dokhale, C. Staples, J. Christian, and K. Shah are with Radiation Monitoring Devices, Inc., Waterton, MA 02472 USA (e-mail: kshah@rmdinc.com).

proposed ASIC and the selected architecture for the ASIC design. We then report on basic tests of the manufactured ASIC, both with an electronically "artificial" signal created by an emulator board as well as on basic tests with single SSPM pixels connected to one ASIC channel. Imaging studies with this ASIC are beyond the scope of this article.

II. Background

To create a high-resolution PET detector, the detector module needs to accommodate a large number of SSPM pixels with little dead space in-between each SSPM pixel. This is most easily accomplished by using SSPM arrays instead of single SSPM pixels. Several detector manufacturers now offer SSPM arrays, including Hamamatsu [Japan], Philips [Netherlands], RMD [Watertown, MA], SensL [Ireland], and FBK [Italy]. To reduce the number of output channels on these arrays and to use them as position-sensitive devices, a decoding scheme is needed. Although a simple resistor network directly coupled to the outputs of the SSPM array would allow significant reduction in the number of readout channels, the inherently fast response of the SSPMs would be compromised by several orders of magnitude. Each SSPM pixel has a significant intrinsic capacitance (of hundreds of picofarads), and directly coupling that to a resistive network would create a significant RC circuit, with a degraded readout bandwidth. This is especially problematic for large area SSPMs (>1mm^2), as the pixel capacitance is proportional to the area. To reduce the number of output channels on SSPM arrays, and to use them as position-sensitive devices, several groups are designing Application Specific Integrated Circuit (ASIC) readouts [10-14]. A few of these ASIC designs [10-12] process each signal and are not compatible with the general PET multiplex scheme. The other groups are working on readouts that are designed to work with small SSPM pixels, with capacitances of 50 to 100 pF [13], [14], or smaller. Our ASIC design achieves high performance with much larger devices that have significantly larger capacitance (by a factor of about ten or more), which is more realistic for PET detector modules.

III. Methods

A. ASIC design

The design parameters for the ASIC were determined from SSPM arrays manufactured by RMD, Inc. The operating range of the ASIC is based on a detection of 50 to 1000 scintillating photons per gamma detection event. The number of scintillator photons was calculated by assuming 511 keV gammas impinging onto a LSO crystal (~28,000 photons/MeV), a 75% collection efficiency (emitted optical photons in the scintillator making it to the SSPM detector surface), and a 10% SSPM photodetection efficiency (PDE). The higher photon count occurs when the gamma interaction is a photoelectric effect while the lower number corresponds to the lower range of Compton scatter events. For an LSO crystal, the light pulse has a rise time of <0.5ns [15] and a fall time of ~40ns [16]. To estimate the input signal to the ASIC, this optical pulse is convolved with the impulse response of the SSPM, which is manufacturer dependent. We have in this work tested the ASIC with an SSPM manufactured by RMD, but the ASIC design is designed to work with a range of SSPMs made by various SSPM manufacturers, and thus a range of rise times (of a few ns and slower) and capacitances (100 – 1000 pF per pixel). The RMD SSPM has a rise time of ~7 ns and a fall time of ~45 ns. The surface area of the SSPM pixels was selected to accommodate typical PET scintillator crystal dimensions that are 1x1 to 4x4 mm^2.

For a scintillator light detection of 50 to 1000 photons, that is, when 50 to 1000 micro-cells fire during one gamma interaction, the current from an SSPM pixel was estimated to be 1 to 20 mA. The maximum capacitance was estimated to be 900 pF, which is equivalent to a 4x4 mm^2 SSPM pixel. The total number of input channels was 16, and the output of the ASIC was not allowed to significantly degrade the 7-ns rise time of the input SSPM signal. The ASIC design specifications are summarized in Table I.

TABLE I
ASIC Design Specifications

Maximum Input Current Pulse	20 mA
Maximum Input Capacitance	900 pF
Total Output Noise	1.3% (@ 50 photon det. signal)
Number of Channels	16
Power Consumption - per Channel	12 mW (@ 3.3V excess bias)
Power consumption - Whole ASIC	313 mW (current buffers + amps)

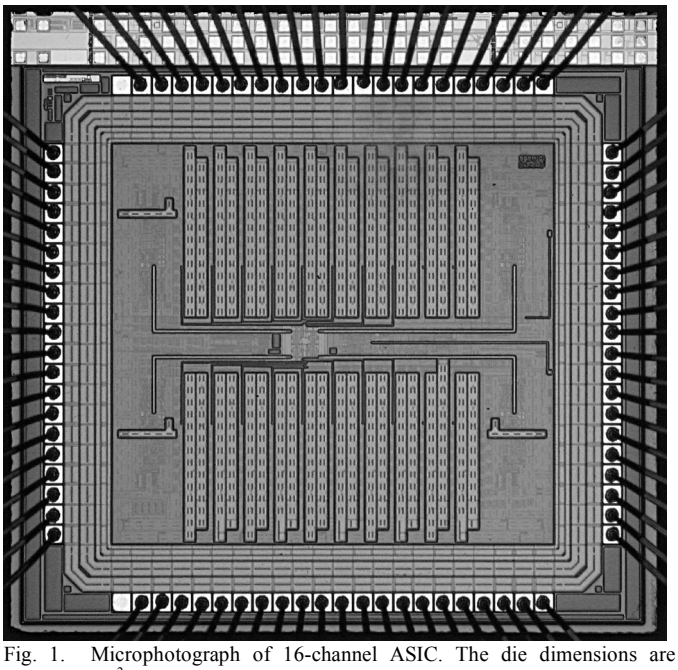

Fig. 1. Microphotograph of 16-channel ASIC. The die dimensions are 2.5 x 2.5 mm^2.

With these design parameters, our IC design team chose a system design based on a design described by Herrero *et al.* [11], though the components in our design were chosen differently. The block diagram of the chip is shown in Fig. 2a, and the schematic of the current-current converter is shown in Fig. 2b.

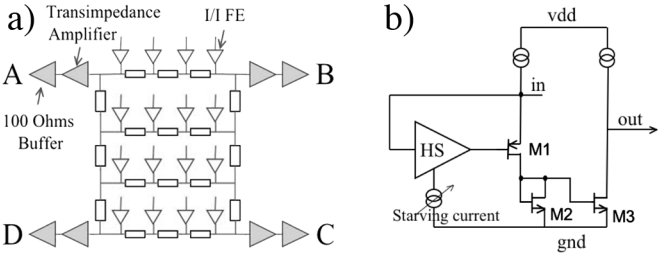

Fig. 2. **a)**: Block diagram of ASIC. Sixteen current-current conveyors (labeled I/I FE) lead the input currents from the SSPM pixels (not shown) to a resistor network, which divides the current to four outputs (labeled A, B, C and D). At each output, a transimpedance amplifier converts the current to a voltage, before the signal is fed to a 100 Ω buffer that drives the line. **b)**: Schematic of the current-current converter. See article text for details.

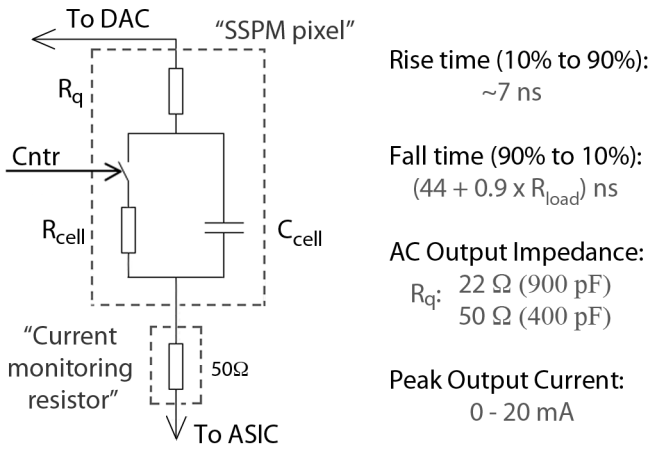

Fig. 3. Schematic of the emulator board circuitry, mimicking an SSPM pixel. To simulate a 900 pF SSPM pixel with a rise time of ~7ns and a fall time of 45ns, we used C_{cell} of 900 pF, R_{cell} of 4.5Ω, and R_q of 22Ω. The corresponding numbers for a 400 pF SSPM pixel were 400 pF, 10Ω, and 50Ω, respectively.

The chip has 16 inputs, where each SSPM-pixel current is coupled through a current-current converter to a resistive network. The resistive network performs a current division between the four outputs (A, B, C, and D). The resulting four multiplexed corner signals are fed through high-speed transimpedance amplifiers that convert the currents to voltages, before the four signals are coupled to output buffers that can drive 100-Ω loads. The 100-Ω load was chosen in order to match the characteristic load of unshielded twisted pair (UTP) cables and to lower the power consumption (compared to 50-Ω buffers). The 16 current-current converters act as shields by preventing the readout front-end electronics – in our case the resistive network – from sensing the capacitance of the SSPM cells, but instead sense the capacitance of the current-current converters, which are four orders of magnitude smaller (assuming an SSPM capacitance of 1 nF).

The current-current converter, which is shown in Fig. 2b, can be viewed as a common gate pass transistor (M1) with a feedback circuit driving the gate of the pass section to improve speed and input impedance. In order to accommodate different number of micro-cells on an SSPM, the first stage transconductance (G_m) of the amplifier, labeled HS (for high-speed) in the figure, is adjustable through a starving current source in order to keep the feedback loop stable. The current-current converter provides a copy of the input current with a ratio of 10:1 (M2, M3) and drives the resistive ladder. The current mirror ratio of 10:1 was chosen to limit the current in the resistive ladder and hence the input voltage to the transimpedance amplifiers. The current attenuation avoids saturation at the output of the current-to-current converter and also helps reduce the power consumption of the four transimpedance amplifiers. This ratio increases the resistive ladder noise contribution referred to the input, which is still below our noise requirements.

The ASIC was designed in Cadence designer software [United Kingdom] and simulated using Eldo Simulator by Mentor Graphics [Wilsonville, OR]. The total output noise (*i.e.*, the quadratic sum of the four corner signals) from these simulations was estimated to be 1.3% rms at an input current of 1 mA (equivalent to a detection of 50 photons), which is equivalent to 0.65 photon rms. As previously mentioned, to accommodate the large variance in input capacitances that the ASIC was designed to work with (up to 4 x 4 mm^2 SSPM pixels), the design requires a starving current source, as shown in Fig. 2b. This design has the tradeoff of a fairly large power consumption of 12 mW per channel, which with 16 input channels and four output line-drivers, results in a total power consumption of 313 mW for the whole chip. The final design was sent to MOSIS (Metal Oxide Semiconductor Implementation Service) for fabrication using the AMS 0.35 μm TSMC CMOS high voltage process.

B. Basic testing of the ASIC

To test the ASIC with various input signals, several emulator boards were designed and manufactured. These boards mimic an SSPM pixel output signal and have the advantage that the signal can be shaped to our specifications, including pulse height, rise and fall times, pulse frequency, and pixel capacitance. The equivalent circuit of an SSPM pixel was mimicked by a capacitor (C_{cell}) in parallel with a switch and a discharge resistor (R_{cell}), all in series with a quenching resistor (R_q), as illustrated in Fig. 3. When the pixel fires, the switch is closed and the charge stored in the cell capacitance discharges through the cell discharge resistor. When the current reaches a threshold, the switch opens, the discharge stops, and the capacitor is recharged through the quenching resistor. By changing the three components (C_{cell}, R_{cell}, R_q), the pixel capacitance and the rise and fall times can be modified. A Digital-to-Analog Converter (DAC) controls the pulse height and the switch is controlled by an FPGA (Field Programmable Gated Array). For the experiments presented here, the components were chosen to mimic SSPM pixels with up to 900 pF capacitance, and to produce ~7 ns rise times and ~45 ns fall times.

For testing, the emulator board output signal was coupled through a 50-Ω resistor (R_{sense}) signal into *channel 0* (unless otherwise specified) input of the ASIC, and *channel A* was used as the output channel (unless otherwise specified). The voltage across the 50-Ω-resistor was used to monitor the input signal. The 50-Ω resistor (in series with R_q and the input resistance of the ASIC, which is between 5 and 10Ω depending on I_{starve}) is in effect placed in parallel with R_{cell} (which is a smaller resistor of 10 Ω) when the switch is closed (i.e., when the signal "rises"). Hence, the impact of placing a 50-Ω resistance in between the emulator board and the ASIC

will produce a degradation of the ASIC rise time by less than 8% (compared to not having it there) for any of the measurements reported on in this paper.

The following tests were performed to evaluate the ASIC: 1) signal output shape, including rise and fall times, 2) gain, 3) electronic noise, 4) input versus output linearity, 5) electronic cross-talk, 6) Anger decoding capability, 7) power consumption, 8) temperature of die, and 9) performance as a function of temperature.

The signal shapes, ASIC gain, and electronic noise were measured with a TDS7404B Tektronix oscilloscope [Beaverton, OR]. The linearity was measured for all four output channels by placing the input current on the closest corner-channel (that is, the current input was on *channel 0* (*3*, *15*, or *12*) when the output voltage was monitored on *channel A* (*B*, *C* or *D*), respectively. The electronic cross-talk was measured on the top row of the ASIC, *i.e.*, channels *0* through *3*. The Anger decoding was performed by injecting various strength signals on one channel at a time and using equations 1a and 1b to calculate the X and Y for that channel.

$$X = \frac{(B+C)-(A+D)}{A+B+C+D}, \quad Y = \frac{(A+B)-(C+D)}{A+B+C+D} \qquad \text{(1a \& 1b)}$$

The resulting XY positions were summarized in a XY plot, which was normalized to the corner channel positions. Each channel was tested with 450 pF and 900 pF emulator boards, as well as various signal strengths. The temperature of the ASIC package was measured using a Raytek Raynger® ST30 PRO infrared thermometer [Fluke Corporation, Everett, WA]. The performance of the ASIC as a function of temperature was performed at three temperatures: at start-up (room temperature), at steady-state (when the ASIC has reached a constant temperature), and at an elevated temperature. The elevated temperature was achieved by blowing hot air onto the ASIC with a heat gun.

C. Testing the ASIC with an SSPM array

The ASIC was also tested with a 6 x 6 pixel SSPM array, as shown in Fig. 4, manufactured by RMD, Inc. Each SSPM pixel measures 1.5x1.5 mm^2, with each pixel containing 30x30 μm^2 micro-cells at a fill factor of 49%, and with a capacitance of 150 pF per pixel. A 3 x 3 x 5 mm^3 LSO crystal was placed on the top left corner of the SSPM array, covering channels 0, 1, 6 and 7, and the crystal was irradiated with 511 keV gammas from a 12 μCi ^{68}Ge point source. The four illuminated channels on the SSPM were connected in parallel, and the resulting output current from the channels was connected through a 10 Ω resistor to the *channel 0* ASIC input. The 10-Ω resistor was used (instead of a 50-Ω resistor) to further reduce the degradation of the rise time. The 10-Ω resistor, which enabled us to measure the current flowing from the SSPM to the ASIC, degraded the rise time of the SSPM and ASIC signals by less than 3%. By connecting four channels in parallel, we effectively created a single SSPM pixel with an intrinsic capacitance of 600 pF. An oscilloscope [DSO7054A, Agilent Technologies] was used to measure the voltages across the 10-Ω resistor and at *output A* on the ASIC. The setup is illustrated in Fig. 5.

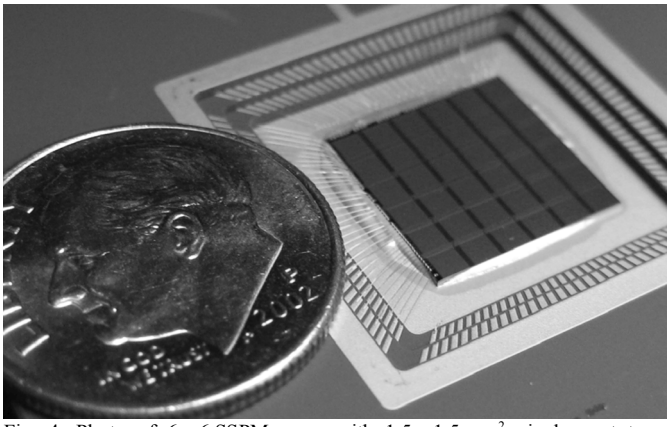

Fig. 4. Photo of 6 x 6 SSPM array with 1.5 x 1.5 mm^2 pixels next to an American dime.

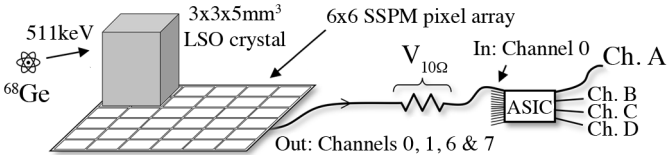

Fig. 5. Setup used to test a single (large) SSPM pixel connected to the ASIC, with the LSO crystal positioned on top of *channels 0, 1, 6, & 7* (which are connected in parallel).

IV. Results

A. Basic testing of the ASIC

As shown in Fig. 6, the signals on the output of the ASIC followed the injected input signal from the emulator boards very well. There is a slight propagation delay (~3 ns) in the output signal compared to the input, and the degradation of the rise and fall times was estimated to be less than 2 ns. The <2 ns impulse response is equivalent to a bandwidth on the current-current converter of at least 175MHz. The unfiltered gain of the ASIC was measured to be ~25 V/A. The electronic noise measurement was below 1 mV (which was limited by our measurement setup), which for a 511 keV gamma-ray detected in a LSO crystal translates to a negligible <1% FWHM to be added (in quadrature) to the ~12% FWHM intrinsic energy resolution of the LSO crystal. As mentioned in Section II.A, the noise is expected to be 0.3 mV rms, which corresponds to 0.65 photons rms.

The measured linearity of the ASIC is shown in Fig. 7, where the output signals' peak-to-peak amplitudes are plotted as a function of input signal peak-to-peak amplitude. There is a slight non-linear effect for large input signals, where the maximum deviation from the linear fit is less than 4% for all channels. This non-linearity for the output signals is small compared to the non-linearity of the SSPM. The number of fired microcells (N_{fired}) in an SSPM is a statistical process based on the probability of detecting randomly distributed photons in a limited number of photosensitive detector elements on a detection surface. This probability can be expressed with the following equation [17]:

$$N_{fired} = N_{cells}\left(1 - e^{-PDE \times \frac{N_{photons}}{N_{cells}}}\right), \qquad (2)$$

where $N_{photons}$ is the number of incident optical photons, N_{cells} is the number of microcells on the SSPM, and PDE is the photodetection efficiency of the SSPM. The linearity of an

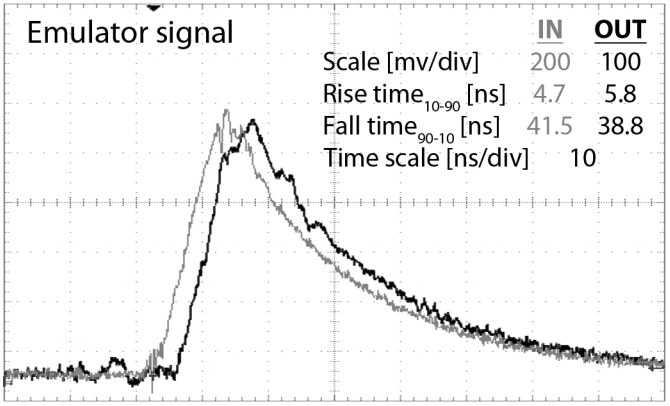

Fig. 6. Oscilloscope image of ASIC output pulse (black curve) versus 450 pF emulator input pulse (gray curve). The emulator board was in this experiment simulating a rise time of ~5 ns. The emulator board signal shows signs of switching noise, which is visible at the start of the rise of the input signal as well at the signal peak, and is also visible in the output pulse. The switching noise is emulator board related and did not affect our measurements.

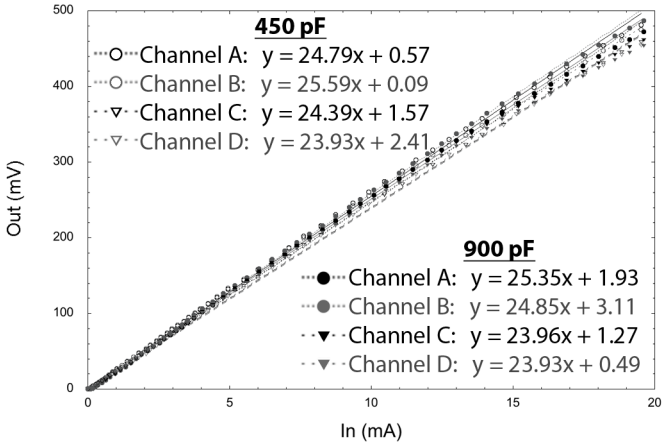

Fig. 7. Linearity plot of the four output signals A, B, C, and D for two capacitive loads. The data has been fitted with linear curve fits, and each curve's equation is displayed for the two emulator boards.

SSPM is thus considered linear only when the term ($-PDE \times N_{photons} / N_{cells}$) can be considered small. In our case we can assume that the maximum number of incident photons onto the SPPM is about 10,000 photons, the number of microcells per pixel to be about 4000, and the PDE to be 10%. With these numbers, we can calculate that we detect about 78% of the photons (i.e., 779 micro-cells fire out of a possible 1000), a number that would decrease for larger photon signals, fewer microcells, or a higher PDE.

The electronic crosstalk of the ASIC is summarized in Table II, and is <6%. The crosstalk was measured to be symmetric, that is, the crosstalk measured on channel *y* when a signal is input on channel *x* is similar to what is observed if the signals were reversed. The crosstalk in these measurements is most likely dominated by the traces on the printed circuit board.

The Anger decoding map is shown in Fig. 8. As can be seen, all channels are consistently falling in their respective location in the XY map, and only a few of the weakest signals are slightly shifted from their nominal location. This minor shift is due to measurement errors of our oscilloscope, as the noise in the oscilloscope probe is no longer negligible at the weaker signal levels. There is also a very minor pincushion effect, which is endemic to a resistor network readout.

TABLE II
CROSS-TALK
(NORMALIZED TO THE OUTPUT SIGNAL ON THE INJECTION CHANNEL)

Channel In \ Channel Out (V)	Ch.	0	1	2	3
	0	1	0.058	0.028	0.016
	1	0.051	1	0.043	0.018
	2	0.028	0.035	1	0.053
	3	0.016	0.016	0.051	1

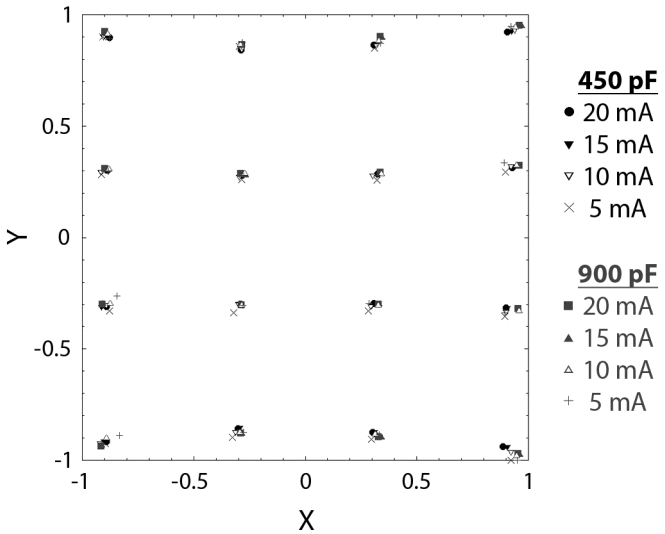

Fig. 8. Anger decoder image of channels 0 (upper left) through 15 (lower right). Two capacitive loads were used, and signal strengths of 5 mA to 20 mA are shown.

The power consumption of the whole ASIC chip, which includes four test structures, was measured to be approximately 360 mW, which is consistent with the simulated results of 313 mW without the test structures. The operational temperature for the ASIC package was measured to be 6ºC above room temperature at steady-state. The ASIC increased its gain by 0.4% per ºC in the temperature range of 25ºC to 45ºC.

B. Testing the ASIC with an SSPM array

Tests with a single SSPM pixel coupled to the ASIC showed similar results to the emulator board tests; the output signal follows the input signal very well and the XY plot showed consistent locations for each channel and good separation between channels. Coupling several pixels in parallel, that is, mimicking larger pixels by increasing the detector surface as well as the capacitance, also produced similar results. In Fig. 9, the input-versus-output signals are shown at 33.7 V bias voltage for a 600 pF SSPM pixel.

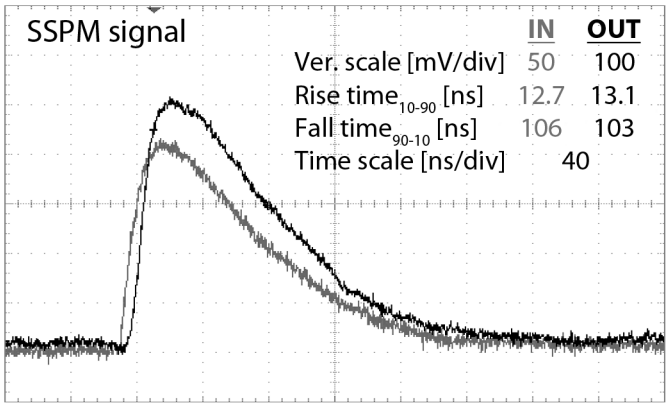

Fig. 9. Oscilloscope image of a single pulse from a 600-pF SSPM pixel (i.e., the ASIC input – gray curve) versus the ASIC output pulse (black curve). The SSPM signal was measured across a 10 Ω resistor. The rise and fall times of the signals are displayed in the legend. Note that the oscilloscope gain is different for the two oscilloscope signals.

V. Discussion

The ASIC was designed to be tunable over a range of SSPM sizes, up to 4 x 4 mm^2. In addition, the speed of the ASIC was designed to not reduce the SSPM readout bandwidth by more than a few percent. These three requirements – large area, flexibility in area, and high timing resolution – resulted in a design that has a fairly high power consumption. The ASIC power consumption in future designs can thus be reduced by reducing: 1) the SSPM area, 2) the range of allowable SSPM areas the ASIC can work with, or 3) the readout speed. Since our goal is to have a general ASIC for SSPM arrays that are compatible with PET detectors, we will look into various ways of reducing the power consumption in the next generation ASIC, however, the high power consumption is a trade-off that we might have to accept.

Our tests of this ASIC show that its rise time is <2 ns, indicating that it will not significantly degrade the ~7 ns rise time of the SSPM pixels. The <2ns rise time degradation should make this ASIC usable in conventional PET systems, where the timing resolution is in the order of a few ns.

VI. Conclusions

An ASIC to read out SSPM pixel array signals has been designed, manufactured, and tested. The ASIC reduces the number of output signals from 16 SSPM pixels down to four, while the SSPMs' intrinsic high timing resolution is maintained. The ASIC uses a charge-division resistive network to decode the channels (*i.e.*, Anger logic), and hides the SSPM capacitance from the resistive network with individual current-current converter between each SSPM and the resistive network. The ASIC allows a wide range of SSPM pixel capacitances (up to 1 nF) to be read out, allowing this ASIC to be used with a wide range of SSPM pixel sizes, up to ~4x4 mm^2. Detector modules based on SSPMs and this ASIC should be compatible with the block detector readout electronics found in many PET cameras.

Our next goal is to develop a 64-channel version of this ASIC. The expected power consumption, with the same architecture, would be 770mW (without line drivers) or 910 mW (with line drivers).

Acknowledgment

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