Title

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A Combined Power Factor Correcting and Active Voltage Balancing Control Technique for Buck-Type AC/DC Grid-Tied Flying Capacitor Multilevel Converters

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***Abstract*—Single-stage Power Factor Correction (PFC) ac-dc rectifiers open a pathway to achieve high power density and efficiency in grid-connected rectifier applications where the target dc voltage is lower than the peak ac voltage (e.g. data center power delivery, LED drivers). Typically in data center and similar applications, a two-stage solution employing a step-up ac-dc stage followed by a step-down dc-dc stage is employed to achieve grid to 48 V conversion. This approach suffers from the efficiency penalty of a cascade of power converters and typically lower power density due to the design of two separate power conversion stages. A single-stage, buck-type PFC rectifier where the output dc voltage is lower than the peak ac voltage circumvents these issues. This work analyzes and develops a single-stage buck-type PFC rectifier utilizing a six-level flying capacitor multilevel (FCML) converter with active flying capacitor voltage balancing and current control to achieve high power density rectification in a single-stage solution. This work is the first to achieve active balancing of capacitors combined with PFC operation in a step-down FCML rectifier.**

I. Introduction

Data centers constitute a relatively large share of global energy usage and this share will likely increase in the coming years [1]. Data center power delivery requires rectification from the incoming mains and successive stages of down-conversion to eventually reach the point of load (e.g. 1, 1.8, or 3.3 V). Conventionally, the rectification stage is implemented with a two-stage solution: the rectifier, which performs Power Factor Correction (PFC), boosts the mains voltage to an intermediate dc voltage higher than the peak of the line (e.g., 400 V for a 240 V_{rms} single-phase ac system) and a second dc-dc stage converts this voltage to a lower dc voltage (e.g., 48 V). As with all two-stage power conversion approaches, the overall system suffers a cascade of efficiency penalties and potentially lower power density due to the design of two separate power conversion stages.

One promising alternative to this conventional architecture is a single-stage conversion architecture [2]–[4]. This architecture directly converts the incoming mains down to a lower voltage (e.g., 48 V) in a single stage rather than increasing the incoming system voltage before subsequently stepping it down. If the power converter used to implement the ac-dc stage is buck-type (i.e. the converter does not operate when $|V_{\text{ac}}| < V_{\text{out}}$), it will be unable to theoretically achieve unity power factor. However, as investigated in [5], extremely high power factors are able to be achieved for conduction angles that are large fractions of the line cycle.

Typically, power converters within the data center or telecom application spaces are held to stringent power density and efficiency standards. To meet these goals, the flying capacitor multilevel (FCML) converter [6] is a very promising topology. The flying capacitors enable a series-connected string of low voltage switches to evenly share the input voltage and thus the converter can employ high figure-of-merit switches. Additionally, the output filter inductor sees significantly reduced volt-second stress, enabling large reductions in the magnetics size compared to a two-level converter. A schematic drawing of a six-level FCML converter with an input synchronous rectifier is shown in Fig. 1.

The ac-dc buck-type PFC application presents a unique challenge for FCML converter control. Since the input voltage of the converter is a rectified version of the grid voltage, the flying capacitors must track this voltage variation (i.e. continually maintain $v_{Ck} = k\frac{v_{\text{in}}}{N-1}$) in order to evenly distribute the voltage stress on the series string of low-voltage switches. Most FCML converter designs employ a passive strategy for balancing the flying capacitor voltages. Typically, the switches in the converter are operated under symmetric phase-shifted PWM (PS-PWM). This modulation scheme uses the same duty cycle for all switching signals and maintains an even phase shift between each signal [6]. This approach relies on the natural circuit dynamics of the FCML converter, such as those investigated in [7]–[11], to converge the flying capacitors to their balanced distribution. Typically, these dynamics are too slow to track the twice-grid-frequency voltage variation. Remedies which sacrifice performance such as operating at an non-ideal switching frequency or choosing unoptimized passive component values have been utilized [4]. This work directly addresses the challenge of flying capacitor voltage tracking at the twice-line-frequency by employing an active

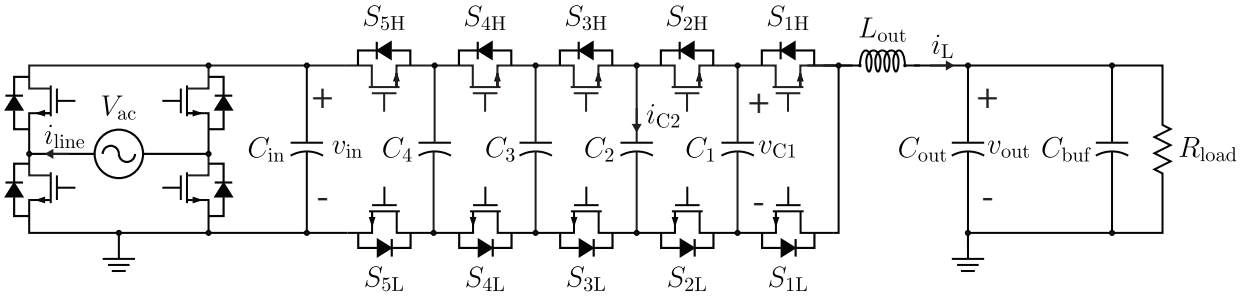

Fig. 1: Circuit diagram of an ac-dc PFC rectifier utilizing a six-level FCML converter with an input synchronous rectifier. C_{out} serves to buffer switching frequency ripple while C_{buf} performs twice-line frequency power buffering.

flying capacitor voltage balancing controller which works in tandem with the inductor current controller. With this control strategy, the switch voltage stress can be minimized and the inductor current can faithfully track the desired reference.

II. Control Law

The derivation of the control law utilized in this work follows that of [12], [13]. However, this work, which operates the FCML converter as a step-down rectifier, requires that the flying capacitor voltages track a U.S. mains twice-line-frequency (120 Hz) large-signal reference and that the inductor current begins and ends at zero current every half-line cycle. These two features force the controller design to depart from these previous works to achieve a satisfactory solution. The controller for this application will be discussed after first analyzing the converter to generate a suitable plant model.

The FCML converter presents an inherent cross-coupling between the inductor current and the flying capacitor voltages. We utilize state space averaging [14] (denoting $\langle x \rangle_0$ the average value of x over a switching period) to analyze the plant and develop a decoupled control law from the plant characteristics. The time-averaged capacitor current $\langle i_{Ck} \rangle_0$ through each capacitor C_k can be expressed as a difference in duty ratios of the adjacent switching signals, q_k, applied to $S_{k\text{H}}$ as in (2). Similarly, the average inductor current can be expressed as a function of switching signals as in (4).

$$C_k \frac{\mathrm{d}}{\mathrm{d}t}\langle v_{Ck} \rangle_0 = \langle i_{Ck} \rangle_0 = \langle (q_{k+1} - q_k) i_{\text{L}} \rangle_0 \tag{1}$$

$$\approx \langle q_{k+1} - q_k \rangle_0 \langle i_{\text{L}} \rangle_0 = \Delta d_k \langle i_{\text{L}} \rangle_0 \tag{2}$$

$$\langle v_{\text{L}} \rangle_0 = \left\langle V_{\text{in}} q_{\text{N-1}} - v_{\text{out}} - \sum_{k=1}^{N-2} (q_{k+1} - q_k) v_{Ck} \right\rangle_0 \tag{3}$$

$$= L_{\text{out}} \frac{\mathrm{d}}{\mathrm{d}t}\langle i_{\text{L}} \rangle_0 \approx V_{\text{in}} d_{\text{N-1}} - \langle v_{\text{out}} \rangle_0 - \sum_{k=1}^{N-2} \Delta d_k \langle v_{Ck} \rangle_0 \tag{4}$$

Linearizing this model, denoting the small signal variables as $\tilde{x}$ and quiescent operating variables as X (i.e. $x = X + \tilde{x}$), about the quiescent point where all flying capacitors are balanced (i.e. $v_{Ck} = k\frac{V_{\text{in}}}{N-1}$) and all quiescent duty cycles are equal (i.e., all $\Delta D = 0$) yields:

$$C_k \frac{\mathrm{d}}{\mathrm{d}t}\langle \tilde{v}_{Ck} \rangle_0 = I_{\text{L}} \Delta \tilde{d}_k \tag{5}$$

$$L_{\text{out}} \frac{\mathrm{d}}{\mathrm{d}t}\langle \tilde{i_{\text{L}}} \rangle_0 = V_{\text{in}} \tilde{d}_{\text{N-1}} - \sum_{k=1}^{N-2} \frac{k V_{\text{in}}}{N-1} \Delta \tilde{d}_k - \langle \tilde{v}_{\text{out}} \rangle_0 \tag{6}$$

Here it can be seen that the average flying capacitor voltages respond only to the differences in adjacent duty cycles while the average inductor current responds to a weighted sum of all duty cycles and the output voltage.

Given this plant model, one control design approach is to apply feedback linearization [15] to decouple the state variables. Feedback linearization simplifies control design by cancelling the inherent state variable cross-couplings, creating multiple Single-Input Single-Output (SISO) systems from the Multi-Input Multi-Output (MIMO) plant. After decoupling the state variables, a single pole integrator response can be chosen for the loop gain corresponding to each state variable. This control strategy results in the closed loop system for each state variable following a first-order, low-pass filter characteristic with a user-definable cutoff frequency. In the Laplace domain we arrive at:

$$\langle \tilde{v}_{Ck} \rangle_0(s) = \frac{I_{\text{L}}}{s C_k} \Delta \tilde{d}_k \tag{7}$$

$$\langle \tilde{i_{\text{L}}} \rangle_0(s) = \frac{1}{s L_{\text{out}}} \left(V_{\text{in}} \tilde{d}_{\text{N-1}} - \langle \tilde{v}_{\text{out}} \rangle_0 - \sum_{k=1}^{N-2} \frac{k V_{\text{in}}}{N-1} \Delta \tilde{d}_k \right) \tag{8}$$

Thus to make the loop gains of the flying capacitor voltage and inductor current systems to be $\frac{\omega_{\text{C}}}{s}$ and $\frac{\omega_{\text{L}}}{s}$, respectively:

$$\Delta \tilde{d}_k = \frac{C_k \omega_{\text{C}}}{I_{\text{L}}} v_{Ck,\text{error}} \tag{9}$$

$$\tilde{d}_{\text{N-1}} = \frac{1}{V_{\text{in}}} (\omega_{\text{L}} i_{\text{L,error}} + \langle \tilde{v}_{\text{out}} \rangle_0) + \sum_{k=1}^{N-2} \frac{k \Delta \tilde{d}_k}{N-1} \tag{10}$$

$$= \frac{1}{V_{\text{in}}} (\omega_{\text{L}} i_{\text{L,error}} + \langle \tilde{v}_{\text{out}} \rangle_0) + \mathbf{B} \vec{\Delta d} \tag{11}$$

The diagonal matrix $\mathbf{B}$ decouples the active balancer controller output from the inductor current loop where each entry in the k-th row is $\frac{k}{N-1}$. Selection of these duty cycles ideally yields $v_{Ck} = \frac{\omega_{\text{C}}}{s} v_{Ck,\text{error}}$ and $i_{\text{L}} = \frac{\omega_{\text{L}}}{s} i_{\text{L,error}}$. Through simulation studies, bandwidths ω_{C} and ω_{L} were chosen to be 3×10^3 and 20×10^3 radians/second respectively. This control architecture is shown schematically in Fig. 2.

As discussed in [12], the desire to mitigate inaccuracies

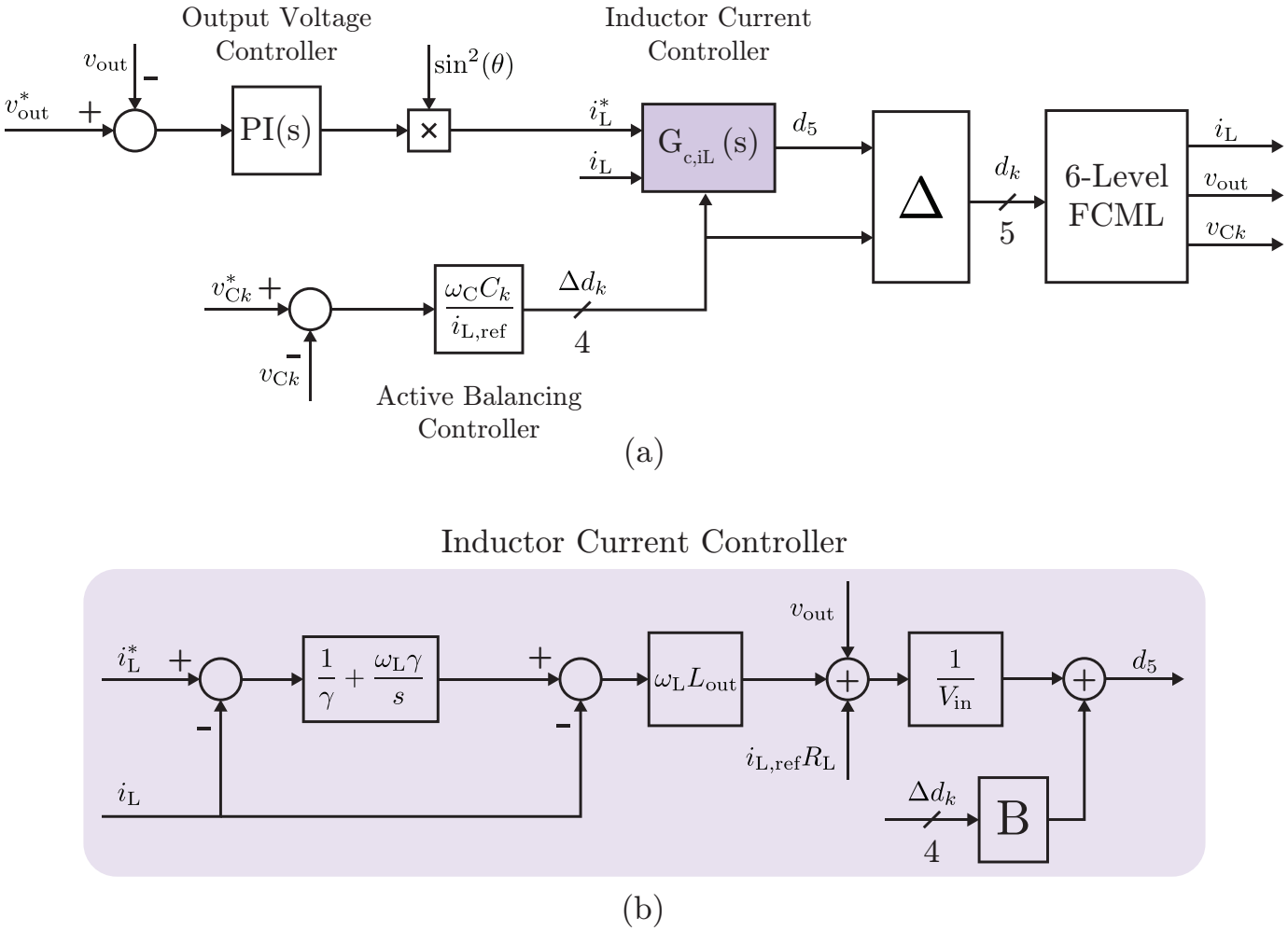

Fig. 2: Block diagram for the implemented combined active flying capacitor voltage balancer and inductor controller for a six-level FCML converter. (a) Overall control structure. (b) Inductor current controller which includes both linearization terms and a PI controller. The Δ block reconstructs the duty cycles from the d_5 and $\vec{\Delta}d$ duties through the following formula: $d_k = d_{k+1} - \Delta d_k$. The **B** block scales the output of the active balancing controller such that the inductor current is unaffected by the active balancer controller as described in (11).

in the plant model and to increase resiliency to disturbances motivate the cascade of a PI controller with the (proportional) feedback linearizing controller described above, as can be seen in Fig. 2(b). In [12], it is recommended to design the PI controller such that the cascade of the PI controller and the feedback linearizing controller yields the same loop gain as the system only with a feedback linearizing controller. This design procedure maintains the same, single-pole response in the overall system as was designed for the feedback linearized plant. In this work, however, we introduce a constant scaling term γ in the design of the controller. In experiment, with $\gamma = 1$ (i.e. that same controller design as in [12]) it was noticed that the inductor current waveform exhibited oscillations at a frequency of around 1 kHz. By reducing γ to 0.25, the zero frequency of the PI controller is reduced and a phase bump is obtained. This increased phase margin virtually eliminated the observed oscillations.

TABLE I: Circuit Parameters

Component	Description	Part Number
$S_{xL,H}$	100V, 1.8 mΩ eGaNFET	EPC2302
C_{fly}	4× 2.2 μF	C5750X6S2W225K250KA
L_{out}	10 μH	IHLP6767GZER100M51
C_{out}	44 μF	C5750C0G2J104J280KC
C_{buf}	54 mF	380LX183M063A082

III. Experimental Results

The aforementioned control structure was tested experimentally using a six-level hardware prototype (Fig. 3), operated at a switching frequency of 100 kHz (i.e., an effective inductor frequency of 500 kHz). The components associated with this hardware prototype are given in Table I. All converter control and switching signal generation was performed by one core of the C2000 F28379D digital signal processor (DSP). The flying capacitor voltages were delivered to the microcon-

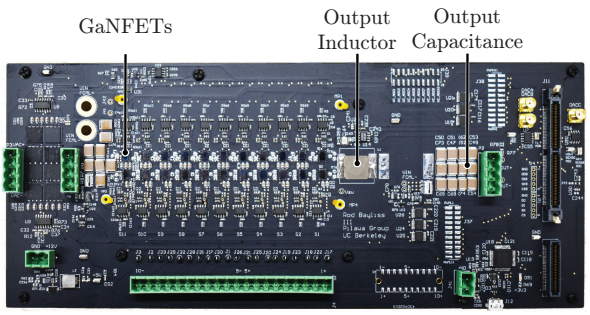

Fig. 3: Photograph of the FCML converter hardware prototype. Circuit parameters are given in Table I.

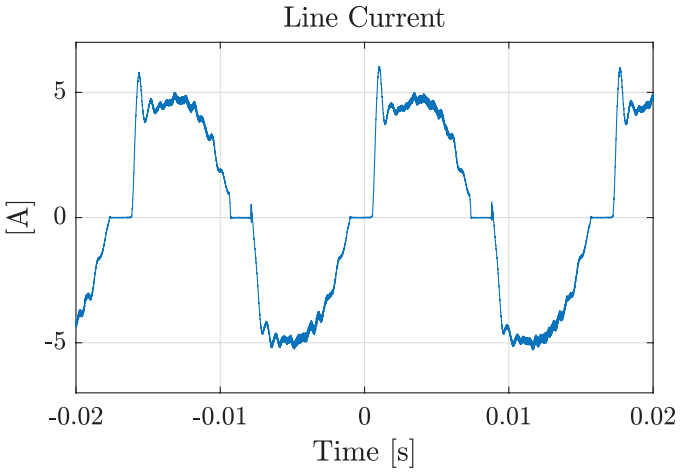

Fig. 4: Measured input current. The measured input current achieves a power factor of 0.9697 with a phase shift of 14.14° as measured by a Keysight PA2201A power analyzer.

troller's onboard ADCs through an analog front end composed of a resistor divider followed by an AD8429 non-isolated instrumentation amplifier. The inductor current was measured through a ground referenced current sense resistor and LT1999 current sense amplifier. The experimental parameters are as follows: $V_{\text{ac}} = 120$ V_{rms}, $V_{\text{out}} = 48$ V and $R_{\text{load}} = 5.3\ \Omega$ yielding an output power of 432 W. A cascaded second order generalized integrator (SOGI) architecture [16], [17] was used to generate the reconstructed and quadrature grid voltages for phase-locking.

Fig. 4 plots the measured converter input current and the measured high power factor of 0.969 reflects satisfactory power factor correction. Fig. 5 shows oscilloscope captures of the flying capacitor voltages while Fig. 6 shows the drain-source voltage stress applied across the switches. Through the developed active balancing control strategy, the flying capacitors are able to track the 120 Hz sinusoidal reference and limit the switch voltage stress.

Finally, Fig. 7 shows the harmonics of the input current plotted against the IEC61000-3-2 Class A limit. All harmonics except for the 17th harmonic pass the harmonic limit. Although these limits are strictly only applicable for equipment operated above 230 V_{rms}, the result provides further validation

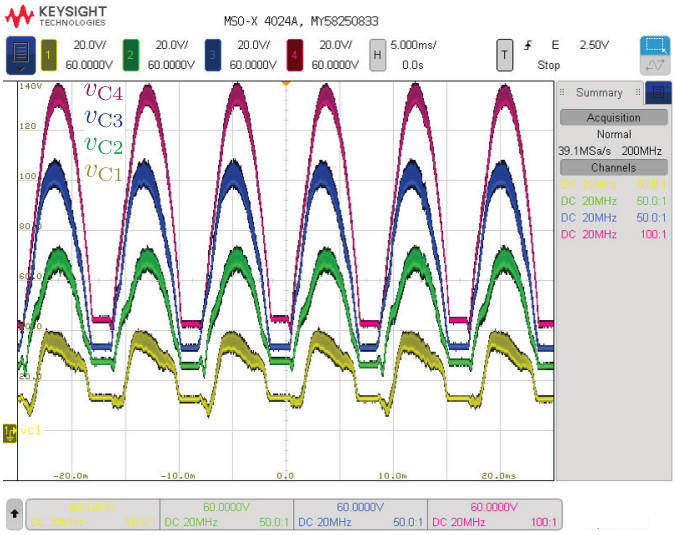

Fig. 5: Measured waveforms of the flying capacitor voltages. The lying capacitor voltages are able to track their reference values sufficiently fast to limit the peak switch voltage stress.

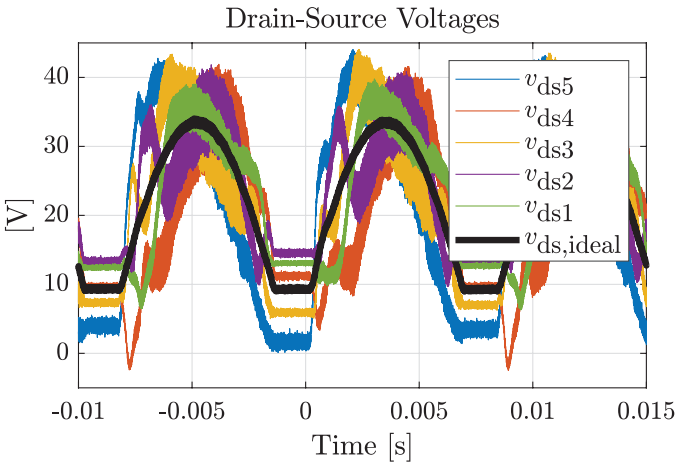

Fig. 6: Measured switch drain-source voltage stress for the operating conditions described in Section III. Ideally the peak switch drain-source voltage is $V_{\text{in}}/(N-1)$ which is achieved when all flying capacitor voltages are at the balanced distribution. The peak drain to source voltage in this experiment was 44.5 V which is 31% higher than the ideal voltage.

of the low harmonic distortion and high power factors able to be obtained by the buck-type PFC approach.

IV. Conclusion

This paper presents a buck-type Power Factor Correction (PFC) ac-dc converter employing a six-level FCML converter. To achieve adequate flying capacitor balancing, an active balancing control strategy was developed and deployed. It is confirmed through hardware validation that the flying capacitor voltages are able to track their ideal, balanced references sufficiently well and high power factor input current (> 0.969) is achieved. This work presents the first implementation of flying capacitor voltage active balancing in a buck-type PFC application, demonstrating excellent control performance.

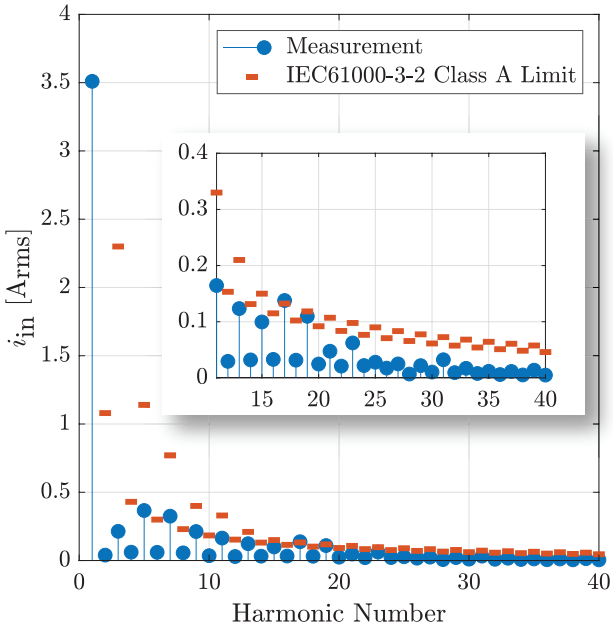

Fig. 7: Measured input current harmonics reported by the Keysight Power Analyzer PA2201A. At an output power of 432 W, all harmonics pass except for the 17th harmonic (1.02 kHz) which is 4% over the limit. Note that the IEC61000-3-2 limits are strictly applicable only for equipment operated an an input voltage above 230 V_{ac} however the comparison is reported here to convey the magnitude of the harmonics relative to industry standards.

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