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Environmental Challenges for 45-nm and 32-nm node CMOS Logic

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Abstract— The objective of this work is to understand the materials and energy requirements, and emissions associated with new semiconductor manufacturing technology nodes. Current and near-future CMOS technologies (for the 45-nm and 32-nm nodes) are investigated using an inventory based on bottom-up process data. The process flow of the CMOS chip is modeled by updating an existing inventory analysis (for 130 nm node devices) to include strained Si channels, metal gates, 10 layers of interconnect and high-k gate dielectrics used in 45-nm and 32-nm CMOS nodes. Conclusions are made concerning emissions of new materials and trends in life cycle energy consumption of logic devices.

Keywords – *Life Cycle Inventory, Life Cycle Assessment, Environmental Management*

I. INTRODUCTION

The semiconductor industry is a large and growing segment of the global economy which, throughout its history, has been challenged by the impacts of its operations on human and environmental health. These challenges have included the hazards of process gases (silane, phosphine, diborane), the release of ozone depleting chloro-fluorocarbons, dumping of untreated fluorine wastes, poisoning of groundwater with mercury, the under-forecasting of facility water demands resulting in serious water shortages (e.g. in Taiwan) and more recently the release of potent global warming perfluorinated gases into the atmosphere. The industry has repeatedly had to make costly changes in the form of process changes and equipment retrofits, materials substitutions, installation of abatement systems or remediation due to these unforeseen problems. Looking into the future, several new environmental questions emerge for the industry, as the range of chemicals used in production expands. Potential environmental impacts associated with novel semiconductor process technologies should be investigated, so that costly manufacturing setbacks can be averted, and to bring quantitative measures of prospective future environmental damages into current manufacturing decision-making.

Maintaining and improving device performance while reducing size and scale of critical device features (in line with Moore's Law) requires an increasingly broader palette of materials. Historically, the range of process materials has expanded only slightly: a short list of only about 12 elements in

the 1980's grew to include tungsten, titanium, copper and tantalum in the 1990's. In the past few years, however, dozens of new elements as well as a broad array of highly tailored compounds have been integrated into the process flow or are being considered as tools to overcome the challenges of current leakage and tunneling, or to build novel geometrical arrangements, in order to achieve ever smaller devices.

Figure 1: Rapid expansion of elements used in semiconductor manufacture. Blue elements represent elements first used in the 1980s. Elements in green, the 1990s, and those in red came into use in the 2000s. Credit: F. Robertson

The result of this material-dependent technology progress is that a larger number, as well as entirely new classes of materials will be emitted into the environment by semiconductor fabs. It is therefore more important than ever to assess the environmental impact of process technologies before they are ramped up into full scale production.

II. METHODS

This paper gives selected results from the 45-nm and 32-nm node technology update to an existing detailed life cycle inventory model of the process flow of a CMOS device [7]. Data are taken from emissions characterization studies and power measurement reports performed at Applied Materials. Emissions characterization is performed using FT-IR and QMS

measurement providing data with an upper bound error of +/- 10%. Power measurement data has an upper bound error of +/- 2.5%.

III. NEW PROCESSES

The 45-nm and 32-nm process flows are a composite of the technology choices of several leading manufacturers [8, 9, 10] as well as industry expectations for near future device scaling [11]. Some logic manufacturers are meeting the 45-nm node through strain engineering alone [10][12], while others are introducing high-k gate dielectrics and metal gates in this generation [15]. Interconnect scaling will proceed at either node with the incorporation of barrier ALD. New process technologies specific to the 45-nm and 32-nm node which involve environmentally significant materials are described as follows.

A. Strained Silicon

Strained Si technology is the enhancement of carrier mobility in the MOS channels through straining of the Si lattice. For PMOS, a layer of Si is epitaxially grown on top of a SiGe layer, to compressively strain the Si channel. The discrepancy in lattice constants between crystalline SiGe and Si causes the epitaxial Si to become axially distorted, enhancing hole mobility in the PMOS channels. Similarly, for NMOS, Si may be subjected to tensile strain through the use of SiN at the channel edge to enhance electron mobility. Higher directional carrier mobility overcomes the limitations of high dose implantation and short channel effects of scaling.

Germane (GeH_4), tetra-chloro-silane (TCS), di-chloro-silane (DCS) and HCl are used in epitaxial growth of SiGe film; Chamber cleaning for silicon and germanium compounds may be achieved using HCl. Emissions from epitaxial SiGe deposition include GeH_4 , SiH_4 , TCS, DCS, HCl and Cl_2 .

B. High-k gate Dielectric

Several options exist for high-k gate dielectrics, with two leading options being HfO_2 and HfSiO_x . Deposition of HfO_2 results in emissions of tetrakis (diethylamido) hafnium (TDEAH), di-ethyl amine (DEA), quaternary ammonium salt ($\text{H}_2\text{NEt}_2^+\text{OH}^-$) and O_2 . HfSiO_x deposition emits TDEAH, tetrakis (dimethylamido) silane (TDMAS), DEA, di-methyl amine (DMA), C_2H_4 , C_2H_2 , CO and CO_2 .

Etching of HfO_2 and HfSiO_x is performed using chlorine chemistries similar to those used for Si etch and these steps produce chlorinated gaseous emissions that are not new to semiconductor facilities. Solid compounds are also produced, including HfCl_4 , which accumulate in pump and abatement lines and which may become suspended in wafer clean wastewater or water waste from point-of-use abatement. An upper bound for these solid emissions, assuming that all chlorine not accounted for in gaseous emissions is converted to HfCl_4 , is 103 kg/year.

C. Metal Gate Electrodes

Gate electrode materials which are potentially compatible with HfO_2 gate oxides include TaN, W and Ru. TaN

deposition results in emissions of NH_3 , DMA and penta-dimethyl amine tantalum (PDMAT). Tungsten deposition processes emit quantities of SiH_4 , WF_6 , SiF_4 , CF_4 , HF and F_2 which may be abated using burn-and-scrub systems. Emissions associated with Ru deposition include bis(2,4 dimethyl pentadienyl) ruthenium (DMRu), CH_3 , CO_2 and CO.

D. Scaling Interconnects (ALD of Barrier)

The thickness of the interconnect barrier layer plays a part in determining interconnect resistivity at a given scale. Atomic layer deposition (ALD) of the TiN barrier layer may be introduced to achieve thinner barriers, decreasing line resistance. Material inputs would be about the same between PVD and ALD, but step duration is lengthened for ALD, with a resultant increased electricity demand.

E. Additional Metal Layers

A typical high performance logic chip at the 45 nm node is designed with 12 layers of interconnect, versus 6 or 8 metal layers of 130 nm and 90 nm devices, and 10 layers for 65 nm devices. Adding each additional 2 metal layers adds 34 steps to the process flow and 82 kWh per wafer in production electricity, as well as 37 kg of total chemical inputs.

F. Shift to Low-k Dielectric

In order to control circuit delay and cross-talk, advanced low-k dielectrics are taking the place of undoped and fluoro-silicate glass as intra-layer and inter-metal dielectrics. Etching these organo-silicates requires fluorinated precursors and results in substantial global warming PFC emissions. Even with the use of lower-emission remote plasma NF_3 clean, the shift to low-k, combined with the increase in the number of metal layers, results in a significant increase in PFC emissions at the 45 and 32 nm nodes. This ongoing trend has been studied in previous literature [16, 17]. PFC emissions from dielectric etch can be effectively abated using point-of-use burn-and-scrub technologies. Using the current life cycle inventory model, the additional two layers of interconnect will produce 33 kgCE/wafer in direct global warming emissions, or 6.7 kg/wafer using combustion and water scrubbing point-of-use abatement.

IV. NEW MATERIALS

TDEAH, TDMAS, DEA, DMA, PDMAT, HfCl_4 , and DMRu would all be new to semiconductor fab emissions. A hypothetical fab producing 300mm, 32 nm node wafers with HfSiO_x gate dielectric, TaN NMOS and Ru PMOS electrodes, operating at 7,500 wafer starts per week, would, without abatement, emit totals of each compound as given in Tables I and II. It is important to note that this process flow is hypothetical and has not been implemented at this time.

TABLE I. SELECTED GASEOUS EMISSIONS FOR 32 NM PROCESS FLOW

Compound	Mass of Gaseous Emissions	
	Per wafer (g)	Per annum (kg)
TDEAH	3.3×10^{-4}	0.13
TDMAS	1.0×10^{-4}	0.04
DEA	4.2×10^{-3}	1.6
DMA	1.5×10^{-2}	5.9
DMRu	27	1.0×10^4

TABLE II. SELECTED SOLID EMISSIONS FOR 32 NM PROCESS FLOW

Mass of Solid Emissions (Upper Bound Estimate)		
Compound	Per wafer (g)	Per annum (kg)
HfCl ₄	2.6×10^{-1}	103
PDMAT	1.2	470

DEA and DMA do not bio-accumulate and both tend to break down in the environment [18-24]. The environmental fate and toxicological effects of TDEAH, TDMAS, DMRu, PDMAT and HfCl₄ are not yet well understood. These emissions could be controlled, and environmental impact drastically reduced, via abatement.

V. LIFE CYCLE ENERGY DEMANDS

Considering the entire life cycle of a CMOS device, although additional steps and lengthened steps may create slight increases to the production energy demand, changes in the use phase power demand of the chip carry much more weight [1]. Increased number of metal layers and higher operational frequencies will increase power consumption, while higher capacitance offered by high-k dielectrics and gate-scaled lower supply voltage will counter this rise [14]. All told, however, 45 and 32 nm node high-performance devices are expected to have slightly (5%) higher power demand than 65 nm node devices [14].

VI. CONCLUSIONS

A bottom-up process model for near-future CMOS fabrication is used to investigate process emissions of concern, as well as to track trends in life cycle electricity use for CMOS devices. New materials appearing among process emissions due to novel process steps include TDEAH, TDMAS, DEA, DMA, PDMAT, HfCl₄ and DMRu. The environmental fate and effect of TDEAH, TDMAS, PDMAT, HfCl₄ and DMRu are of interest as high-k and metal gates are adopted by fabs in the coming years.

We can see shifts in the life cycle energy in both use and production phases. Total production electricity demand for each technology node increases as the process flow expands and individual, steps such as metal barrier deposition, lengthen. Smaller gates and high-k gate dielectric permit lower

achievable standby power and potential decreased electricity use throughout the lifetime of the device, though high performance chips with higher operational frequency will demand roughly the same use phase power as previous generations.

A full cradle-to-gate inventory of material and energy demands, as well as emissions will follow in future work.

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