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Selective Area Doping of GaN by Epitaxial Layer Overgrowth and Its Power Electronic Applications

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Selective Area Doping of GaN by Epitaxial Layer Overgrowth and Its Power Electronic Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials Science and Engineering

by

Jia Wang

2021

ABSTRACT OF THE DISSERTATION

Selective Area Doping of GaN by Epitaxial Layer Overgrowth

and Its Power Electronic Applications

by

Jia Wang

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2021

Professor Ya-Hong Xie, Chair

GaN has wide bandgap, high critical electric field, and high electron saturation velocity, making it an ideal candidate for power switching electronics. However, the development of GaN-based power electronics is still hampered by the high cost of GaN substrate and selective area doping capabilities (especially for *p*-type) to produce laterally patterned *p-n* junctions. Epitaxial lateral overgrowth (ELO) is known to render low-dislocation-density GaN in the overgrown regions (wings) on inexpensive foreign substrates. Furthermore, the combination of ELO (prior to the coalescence stage) and *in-situ* doping process produces the half-core-shell doping profile which has been used in the optoelectronics such as microrod LEDs. However, the application of ELO-GaN has not been explored in the power applications mostly because such doping profile is not configured to withstand high reverse blocking voltage unless the modified structures and methods could be adopted.

In this dissertation, a holistic approach was employed to study the innovative measures either in the material growth or device processing stage to tailor the half-core-shell doping profile produced by the ELO of GaN into the desired selective-area doping profiles for power switching electronics featuring the building block of laterally patterned *p-n* junctions.

For the device processing innovation, the concept of true-lateral device architecture was proposed which consists of fully lateral aligned *p-n* junctions. The general advantages of such device architecture were comprehensively discussed from various aspects. In addition, the low-dislocation density GaN in the wing regions of ELO was fully utilized as an ideal drift layer of a power device. As a result, both power diodes (SBD and PND) and power bipolar transistors (GL-BJT and IGBT) with the true-lateral device architecture were experimentally demonstrated either with superior performance or for the first time, highlighted by the record high critical electric field in a GaN *p-n* junction and the record high current gain of a power bipolar transistor.

Alternatively, for the material growth innovation, the hybrid epitaxy-enabled substrate transfer approach was demonstrated to produce the GaN substrate with repeating laterally patterned *p-n* junctions suitable for a number of advanced electronic devices such as a planar-gate vertical MOSFET. In addition, the selective area doping profiles of the GaN substrate product also rendered a number of state-of-the-art characterization techniques which provided valuable information to study the incorporation and diffusion of dopants (especially for acceptors) in GaN.

With these innovative measures and a deeper understanding of selective area doping of GaN, the potential of epitaxial lateral overgrowth to simultaneously realize the low threading dislocation density and the selective-area doping profile (lateral patterned p-n junctions) was initially and finally unleashed, which may spawn a revival of interest into ELO-GaN to yield unprecedented opportunities in power electronic applications.

The dissertation of Jia Wang is approved.

Hiroshi Amano

Dwight Christopher Streit

Jaime Marian

Kang Lung Wang

Ya-Hong Xie, Committee Chair

University of California, Los Angeles

2021

Dedicated to my parents

for their boundless love and support

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Selected Publications

1. **Jia Wang**, Ya-Hong Xie, and Hiroshi Amano, "High-Gain Gated Lateral Power Bipolar Junction Transistor," *IEEE Electron Device Letters*, vol. 42, no.9, pp. 1370–1373, 2021.

2. *(Editor's Pick)* **Jia Wang**, Guo Yu, Hua Zong, Yaqiang Liao, Weifang Lu, Wentao Cai, Xiaodong Hu, Ya-Hong Xie, and Hiroshi Amano, "Non-polar True-lateral GaN Power Diodes on Foreign Substrates," *Applied Physics Letters*, vol. 118, no.21, 212102, 2021.

3. **Jia Wang**, Shun Lu, Wentao Cai, Takeru Kumabe, Yuto Ando, Yaqiang Liao, Yoshio Honda, Ya-Hong Xie, and Hiroshi Amano, "Ohmic contact to p-type GaN enabled by post-growth diffusion of magnesium," *submitted to IEEE Electron Device Letters*, 2021.

4. **Jia Wang**, Jian Shen, Hua Zong, Shengxiang Jiang, Yuto Ando, Guohao Yu, Weifang Lu, Ting Liu, Wentao Cai, Shugo Nitta, Yoshio Honda, Xiaodong Hu, Ya-Hong Xie, and Hiroshi Amano,

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2. **Jia Wang,** Shengxiang Jiang, Hua Zong, Yaqiang Liao, Ting Liu, Jian Shen, Yuto Ando, Yoshio Honda, Xiaodong Hu, Hiroshi Amano, and Ya-Hong Xie, "Vertical PN Junction-based GaN Power Diode.", Oral presentation at: 2019 51th International Conference on Solid State Devices and Materials (SSDM); Sept., 2019; Nagoya, Japan.

Chapter 1

Introduction

1.1 Background

1.1.1 Power Switching Electronics

With the advent of information era characterized by revolutionary in the silicon (Si)-based computing and communication industries, energy technology is becoming more critical than ever before. The high demands for energy has pushed for increased efficiency in power conversion systems [1], [2]. For one thing, hybrid electric vehicles are becoming cost-effective and popular, and there is growing interest in the development of all-electric transportation to reach a carbon-neutral society. For another, the electricity transmission and distribution infrastructure is amid rapid transformation in its history and a flexible and robust smart electricity grid is needed. Semiconductor switches are at the heart of power conversion systems. In 2020, electricity accounts for 40% of the total energy consumption, whereas more than 30% of electricity undergoes at least one stages of transistor-based power conversion before reaching every household. It is expected that the share would reach 80% by the year of 2030 [3].

This solid-state energy conversion is widely referred to as “power switching electronics”, which constitutes the backbone of electricity transmission, distribution, and processing much like signal electronics is used for constructing the information highway.

Power switching electronics are the major factor that determines the performance, reliability, and cost of the overall power conversion system, which is needed in many applications including electric/hybrid vehicles and power grids. Silicon remains today’s most widely employed power-switching semiconductor material, and some 600 V-class Si-based devices such as super-junction MOSFETs have achieved outstanding performance with the on-resistance as low as 35 $m\Omega.cm^2$

[4], which is approaching the material limit of Si. In order to meet the ever-increasing demand of power conversion, the efficiency of the power switching electronics has to be improved by exploring other semiconductor materials other than Si. The semiconductors having wide-bandgap (WBG) are the ideal choice to satisfy the requirement of power switches which inherently can achieve better voltage blocking capability and current handling capability. The former is often compared by the breakdown voltage (V_{BR}) at OFF-state and the latter one is often compared by the specific on-resistance ($R_{on,sp}$), i.e., the differential resistance of the device in the ON-state multiplied by the device area.

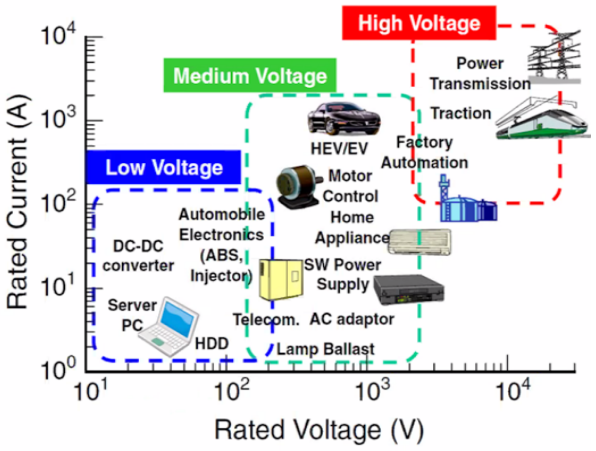

Figure 1.1 A schematic summary of various applications for power switching electronics sorted by the rated voltage (V) and rated current (A) [5].

1.1.2 Critical Electric Field in a WBG Semiconductor

Why could a WBG semiconductor-based power device have higher breakdown voltage and lower specific on-resistance than its Si-based counterpart? The answer can be better illustrated by using the simple model of a one-sided junction, when all the depletion region is considered on the n-side of the junction. Under reverse bias, the electric field ε_c decreases along the junction distance with the slope being proportional to N_d, the net doping concentration in the drift layer. When a Si

diode and a WBG semiconductor diode withstand the same reverse bias, the area of the triangles enclosed by the field (ε)-distance (W) plot in Fig. 1.2 is the same.

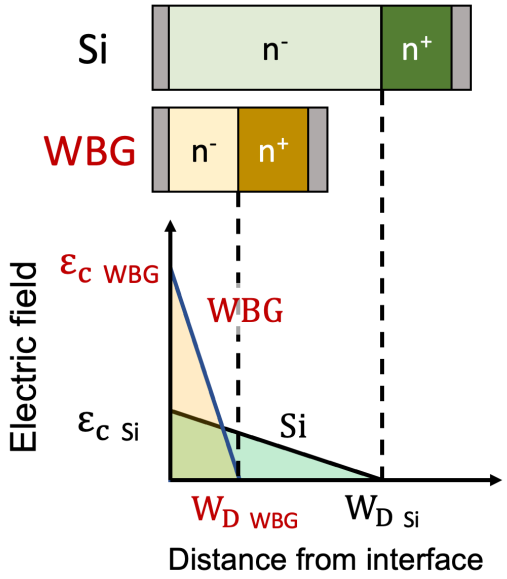

Figure 1.2 Comparison of Si and WBG semiconductor in a one-sided junction model which highlights the merit of a high ε_c.

Because WBG semiconductor can intrinsically tolerate higher critical field ε_c, if under the same breakdown voltage, i.e., when the area of triangles is equal, then the WBG semiconductor can have shorter W_D-thinner depletion region with higher ionized net charge density, which leads to a smaller specific resistance of the drift layer during the ON state. Therefore, WBG can achieve lower specific on-resistance while preserving high breakdown voltage. By the same token, in a p^+-n^- junction diode, the derivation of V_{BR} and $R_{on,sp}$ are as follows:

$$V_{BR} = V_{app} + V_{bi} = \int_{-x_p}^{x_n} \varepsilon \, dx = \frac{x_p^2 e N_A}{2\epsilon} + \frac{x_n^2 e N_D}{2\epsilon} \approx \frac{x_n^2 e N_D}{2\epsilon} \tag{1.1}$$

$$R_{on,sp} = \rho_p x_p + \rho_n x_n = \frac{x_p}{e N_A \mu_p} + \frac{x_n}{e N_D \mu_n} \approx \frac{x_n}{e N_D \mu_n} \tag{1.2}$$

where V_{app} is the applied reverse bias, V_{bi} is the built-in voltage, x_n and x_p are the depletion region thickness on the p-type and n-type semiconductor side.

In general, figure of merits (FOMs) which usually consist of several key material properties are defined and used as benchmark to compare the device performance. In the field of power switching electronic, Baliga's FOM is one of the most commonly used FOMs, which was initially proposed by Dr. B. Jayant Baliga who is best known for his pioneering work in power semiconductor devices [6]. The Baliga's FOM (also written as BFOM or FOM_{Baliga}) can be expressed as follows:

$$FOM_{Baliga} = \frac{V_{BR}{}^2}{R_{on,sp}} = \frac{\varepsilon_c{}^3 \mu_n \epsilon}{4} \tag{1.3}$$

here ϵ is the material's permittivity (dielectric constant), μ_n is the electron mobility (for single-sided junction where n-side is lightly doped), and ε_c is the critical electric field which is defined as the maximum field in a one-sided infinite planar junction at the onset of breakdown. Since FOM_{Baliga} is derive from the model of single-sided junction where only the resistance of quasi-neutral region of the drift layer is taken into the consideration of the specific on-resistance (this is true and mostly accurate when ignoring the effects of high-level minority injection), FOM_{Baliga} should be best understood as the performance limit of a unipolar power device [7].

1.1.3 Material of Choice

We can tell from Baliga's FOM that the critical electric field ε_c-the term in the cubic form in the Baliga's FOM's expression-is the key property for a power semiconductor material. In general, gallium nitride (GaN) and silicon carbide (SiC) are the two most studied WBG materials. If we compare some key material properties of Si, 4H-SiC (the most common polymorph of SiC) and GaN (wurtzite) by using a radial pentagon in Fig. 1.3, we may find out that GaN possesses higher critical field than SiC and Si, making it a good choice for power switching electronics. Specifically, compared to 4H-SiC which features largest bandgap (3.26 eV at 300K) and critical breakdown electric field E_c=2.5–3.0 MV/cm among all the common polymorphs of SiC [8], GaN has higher

breakdown field strength with an estimated value of 3.3–3.7 MV/cm, better on-state performance under higher frequency operation [8]. In terms of avalanche breakdown, the critical field is determined by the width of bandgap. As such, the fact that GaN has wider bandgap than SiC lays the theoretical foundation for the anticipated superior performance of a GaN-based power electronic device [9].

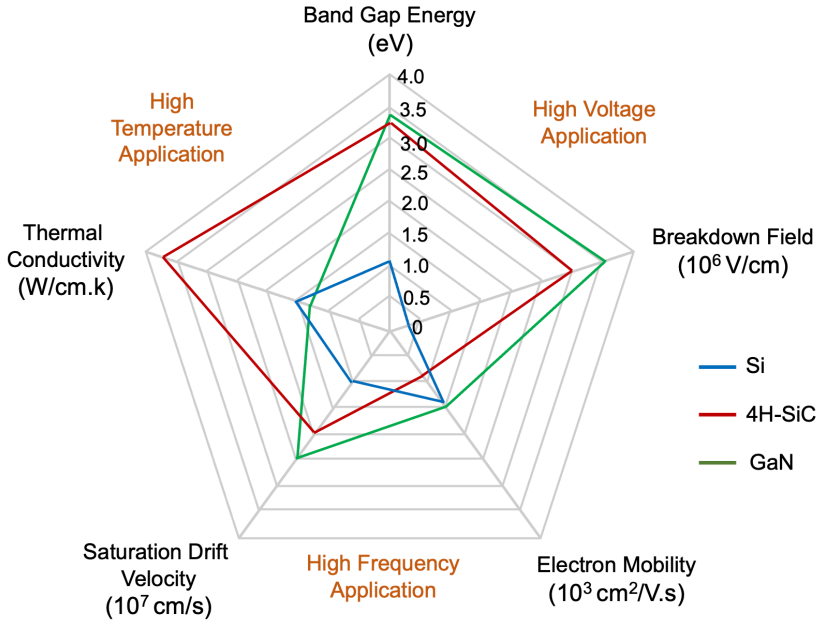

Figure 1.3 A comparison between the key materials properties of Si, 4H-SiC and GaN.

Due to these superior properties, GaN-based power electronic devices are considered to hold the promise of much better performance compared to the Si incumbents and even their SiC rivals in critical factors such as on-state loss, switching loss and the ability to block high voltage in the off-state. Fig. 1.4 summarizes the specific on-resistance and blocking voltage of all the common types of power switches. Despite the theoretical anticipation of superior power performances that GaN should possess over SiC, the de facto applications of GaN and SiC based power electronics as summarized in Fig. 1.5 presents a stark contrast. In other words, even though GaN has a higher limit than SiC, the best reported performance of GaN-based transistors remains inferior to that of

SiC and is significantly below the predicted performance limit. In view of application sorted by voltage ratings, there is a separation line of ~600V in the field of median-and-high frequency power electronics, above which SiC is dominating the status quo-the material of choice for the most demanding power switching applications, i.e., in power grids, whereas GaN-based power transistors have limited market share in low and median power applications with VBR<600 V. Then what is it that causes the discrepancy between theoretical and de facto performances? The answer to this question is crucial which also underlies the motivation of this dissertation, as shall be elaborated in the subsequent section. Secondary to this, one can also observe from Fig. 1.5 that in the low-and-median frequency applications, Si is widespread used throughout the entire voltage rating range. In fact, WBG-based power devices as a whole represents still a very small fraction of power electronic market ($160M: $16B) today and even smaller share (~0.05%) of the total semiconductor market [10].

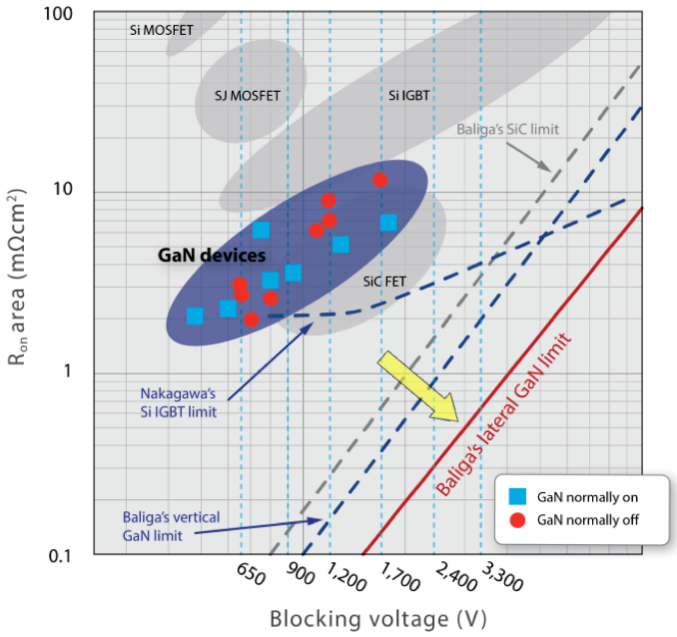

Figure 1.4 The material-limit curves of Si, SiC and GaN and $R_{on,sp}$ versus V_{BR} for all the common types of power switches (the yellow arrow indicates the desired direction) [11].

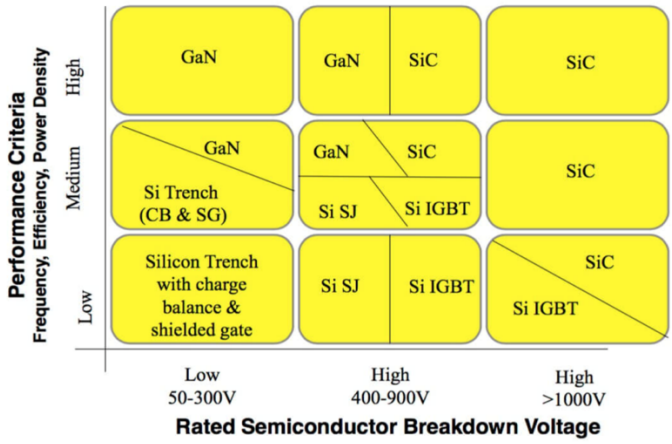

Figure 1.5 Applications of power electronics sorted by voltage and frequency [10].

1.2 Improvement for GaN as Power Switching Electronics

1.2.1 GaN with Low Dislocation Density

Fundamentally, material defects usually account for the deviation from predicted device performance that is based on the abstract physical model with perfect semiconductor material. In terms of WBG materials, if there are numerous states introduced into otherwise forbidden band, the benefits of having a wide bandgap would be seriously compromised. Therefore, it is important to investigate the effects of defects on the device performance. And these defects, shallow or deep in their relative energy level to the band-edge, generally arise from impurity atoms or vacancies (0D), dislocations (1D) or interface/surface and stacking faults (2D). Unraveling their origins is also important to evaluate their relative influences in different WBG materials at material growth or device processing stage. For example, doping is one of the main drawbacks in SiC devices, which in practice can only be achieved by means of ion implantation. However, ion implantation in SiC will heavily damage the lattice and create point defects which are hard to recover despite thermal annealing post-treatment [13]. Worse than SiC, not only is GaN difficult for effective p-type doping, but also it has greater problem in its crystal growth.

Unlike SiC and Si, the growth of bulk crystal of GaN is severely hindered by the extreme high temperature (2225 °C) and high pressure (6.5 GPa) [12] due to the high equilibrium vapor pressure of N_2, making it almost impossible endeavor trying to mass produce crystals of any significant size (e.g., 2-inch diameter) as required by the economy of manufacturing. Consequently, the production of GaN wafers relies entirely on hetero-epitaxy of GaN on foreign substrates such as Si, sapphire and SiC with progressively higher substrate cost. The most widely used growth technique is vapor phase epitaxy (VPE). Probably the most challenging aspect of GaN hetero-epitaxy is the lacking of lattice matched substrates thus the unavoidably high density of dislocations and the associated reliability challenges [13]. For example, sapphire-the widespread employed heterosubstrate today for mass production of white light LED chips, has lattice mismatch of 8% to GaN, leading to a dislocation density of 10^8–10^9 cm^{-2}.

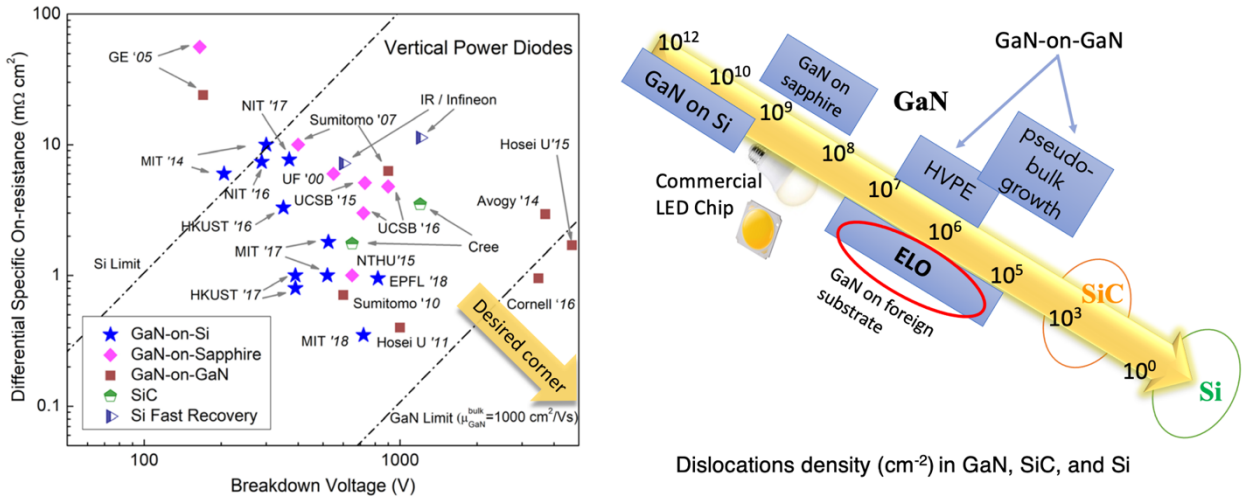

Figure 1.6 The correlation of GaN power device performance (left image from [14]) with dislocation density in GaN material grown on different substrates (right image).

It is believed that the presence of high density of dislocation is the main reason for the degraded breakdown performance in GaN based power electronics. Such correlation might be better revealed in Fig. 1.6 which combines the performance benchmarking of GaN vertical power

diodes fabricated on different substrates with a schematic summary of GaN with varying orders of dislocation density grown on different substrates. As it appears in the right schematic, GaN has typically the highest dislocation density (>10^9 cm^{-2}) on Si due to the largest lattice misfit, followed by the median dislocation density of down to ~10^8 cm^{-2} for GaN on sapphire, and the lower dislocation density GaN in the range of 10^6–10^8 cm^{-2} for GaN-on-GaN substrate prepared by HVPE or pseudo-bulk growth techniques such as ammonothermal or sodium flux method. On the other hand, in the left figure, there is also a similar trend-from the blue stars indicating GaN diodes on Si, to the pink diamonds indicating GaN diodes on sapphire, and finally to the crimson squares indicating GaN diodes on GaN substrate. Such trend pointing to the desired lower-right corner is parallel to the direction of the golden arrow pointing to lower dislocation density. **In some sense, the correlation also represents the interplay the between microscopic defects in the material science domain to the macroscopic performance in the electrical engineering domain.** It was also observed experimentally that dislocation is closely associated with current leakage paths due to deep level traps [15]. The enormous build-up of leakage current causes so-called premature breakdown, which can occur when the critical field and V_{BR} are much less than the predicted values. To date, a couple of leakage mechanisms (trap-assisted space charge limited current and variable range hopping conduction along dislocations) have been invoked for explaining the behavior of GaN devices in the literature [16][17]. It is also known that dislocations tend to be decorated by points defect (vacancy and impurities) because of the interaction of the stress fields generated by the dislocation and point defect (i.e., the cancellation or reduction of stress fields provides driving force for point defects to decorate a dislocation). The trapped electrons hop between deep levels induced by the grouped point defects decorating along threading dislocation then constitute leakage paths under high field.

Therefore, there is a pressing need to minimize the dislocation density in GaN in order to enhance the performance of power devices. As shown in Fig. 1.6, localized dislocation filtering techniques such as epitaxial lateral overgrowth (ELO) or film thickening via halide vapor phase epitaxy (HVPE) have been employed to achieve threading dislocation density (TDD) as low as 10^6 cm^{-2}, which is three orders of magnitude lower than that of the GaN-on-sapphire films used for light-emitting diodes (LEDs) today [13]. The detailed discussion of ELO-the main topic of this dissertation, will be arranged in the next section.

Compared to ELO, thickening has been used more in recent years due to its effectiveness in the reduction of TDD, as most of the commercially available "bulk GaN substrate" (freestanding GaN) are actually derived from thick crystal films grown by HVPE on foreign substrates and subsequently removed from the substrate. In principle, by growing thicker films, the reaction between neighboring dislocations eliminates each other due to the cancelation of stress fields of individual dislocations-a process known as dislocation annihilation. Such reaction between neighboring dislocation causes the reduction of TDD. However, such reduction has a theoretical limit since the probability of dislocation annihilation reduces with increasing film thickness until approaching zero asymptotically. This is fundamentally because the strength of the stress field of individual dislocation decays reciprocally with distance so that the thermal fluctuation will dominate over the weak attraction beyond certain separation distance.

1.2.2 Selective-area Doping Capabilities

In order to improve the performance of GaN-based power devices, with the gradual improvement in the material quality of GaN with low dislocation density over the past decade, doping has resurfaced as another critical bottleneck. In fact, the dislocation density of GaN has reached a low level in the GaN devices fabricated on GaN substrate so that the avalanche

breakdown capability has been demonstrated and the critical E-field approached the material limit of GaN [18]. Nevertheless, on the other hand, the effective p-type doping of GaN still poses the issue. This is fundamentally because that magnesium (Mg) with which the first demonstration of p-type conduction in GaN was realized [19], is still the only dopant available to produce p-type GaN till today [20]. However, because of a high ionization energy (~200 meV), the hole concentration is rather limited in even heavily doped p-GaN due to the incomplete ionization of acceptors [21][22]. In addition, in-situ corporation of Mg impurity during the vapor phase epitaxy is still the dominant methodology for p-type doping of GaN, which would only produce planar and blanket p-type GaN thin film rather than selective-area p-type GaN. Specifically, the ability to obtain selective area p-type doping profile of GaN, or rather, to obtain laterally patterned p-n junctions, is the bottleneck to realize a plethora of power electronics with advanced structures and functions [23]. Figure 1.7 schematically illustrates some of these advanced electronics with laterally-patterned p-n junctions, including junction field-effect transistors (JFETs), p-GaN guard rings for junction termination extension, merged p-n/Schottky (mPS) diodes, planar-gate normally-off vertical MOSFETs [24], super-junction MOSFETs, and current aperture vertical electron transistors (CAVETs) [25].

In principle, in some of these applications, p-type region greatly assists in the edge termination by easing the field crowding at the edge, such as in the cases of guard ring or mPS diodes [26]. Alternatively, p-GaN region may also help reduce the net charge density $|N_D-N_A|$ in the space charge region (depletion region) of the neighboring n-regions in the OFF state so that the reverse blocking voltage is increased due to the reduced slope of the E-field (proportional to $|N_D-N_A|$) along the depletion region [27]. Finally, the p-region will also help decrease the specific on-resistance by high-level minority injection into n-region [6], [28]. Amongst the aforementioned three merits,

the first will help to approach the infinite planar junction-the ideal unipolar model for the Baliga's FOM. And the second and third merits will help go beyond to the performance limit set by the Baliga's unipolar model by achieving the limit-breaking high V_{BR} and limit-breaking low Ron,sp, respectively.

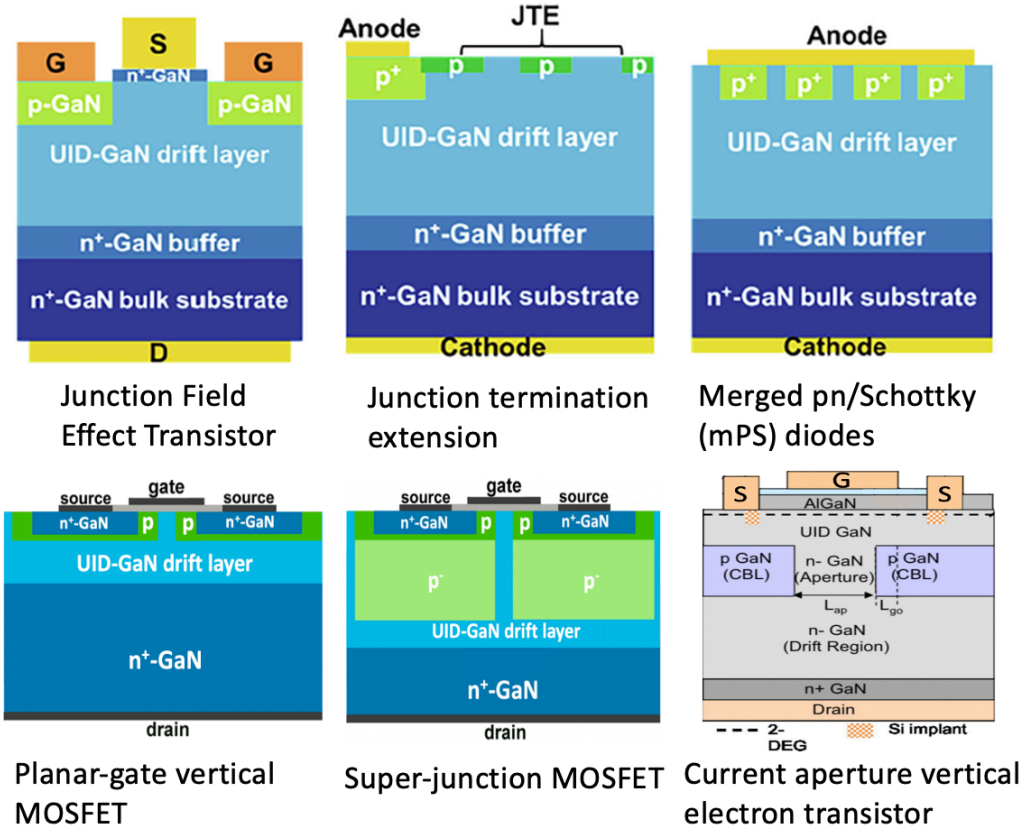

Figure 1.7 Schematic illustrations of several advanced electronics which requires the selective area doping profile characterized by the laterally-patterned p-n junctions [23]–[25], [27]

In reality, although the desired selective-area doping profile featuring laterally-patterned p-n junctions are highly sought after, the current main methodologies, i.e., ion implantation and etch-and-regrowth methods, suffer from various issues. Ion implantation is the dominant technology for doping in Si and quite a lot of research efforts have been devoted to ion implantation of Mg to create p-GaN. However, it is extremely difficult to activate implanted Mg which results in low

activation ratio unless ultrahigh pressure and temperature is employed [29], restricting the yield of the technology. Furthermore, extended defects such as inversion domain with Mg segregation are also among the typical issues in the post-implanted region which are difficult to recover [30]. Alternatively, etch-and-regrowth has been another methodology [31]. As drawn in Fig. 1.8 (right), a trench area is created by dry etch followed by regrowth of p-GaN. However, the unavoidable plasma damage caused to the regrown interface is problematic. The typical issues may include the leakage pathway along the regrowth interface [32] and the notorious and omnipresent Si pile-up which leads to the n^+-GaN sheet along the regrowth interface due to a considerable incorporation of Si atoms [33]. Given that both ion implantation and etch-and-regrowth are faced with various setbacks, a new methodology is strongly desired to realize the selective-area doping capability in GaN.

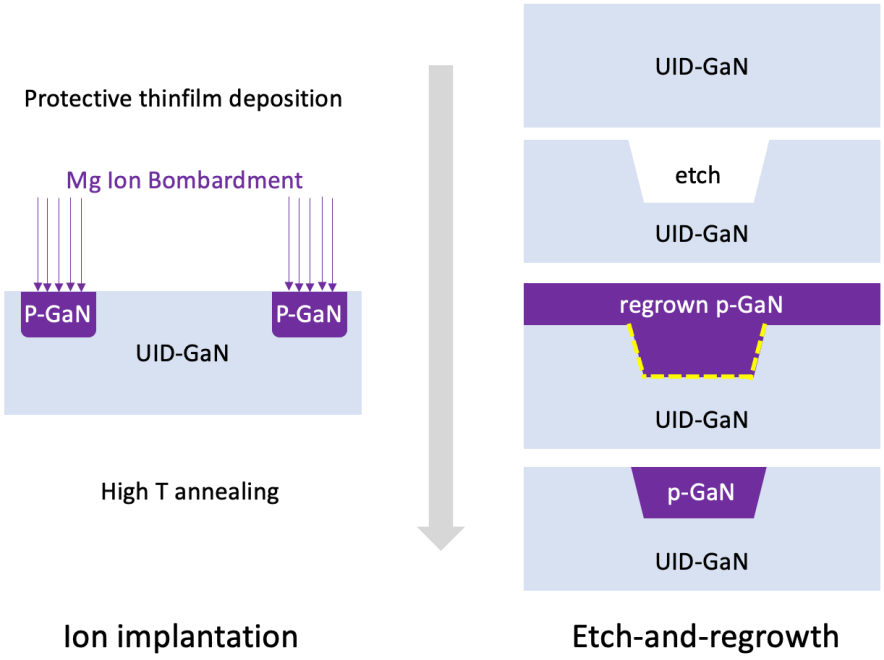

Figure 1.8 Schematic illustration of the ion implantation and etch-and-regrowth methods to create the selective-area p-type region in GaN.

1.3 Epitaxial Lateral Overgrowth of GaN

1.3.1 Dislocation Reduction by ELO

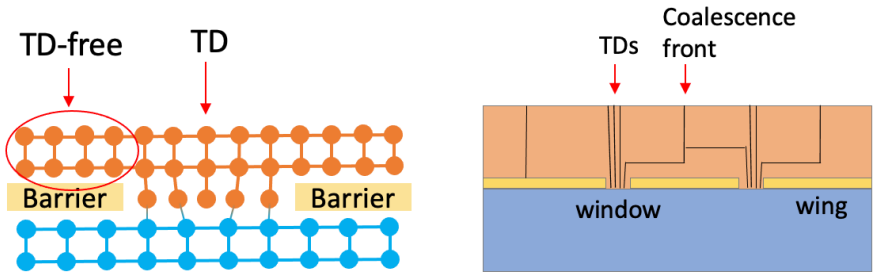

Figure 1.9 Schematic illustrations of the epitaxial layer overgrowth of GaN to reduce the threading dislocation density.

The method of epitaxial lateral overgrowth (ELO) has attracted much interest in the past two decades for obtaining GaN with reduced dislocation density or/and controlled crystallographic planes on the foreign substrate [34]. The original and main purpose of ELO is to reduce the dislocation density. The principle can be briefly illustrated in Fig. 1.9, when the single crystalline GaN indicated by the orange lattice is epitaxially grown onto the foreign substrate in blue having a different lattice constant, misfit dislocation is generated which lies on the interface to relieve the misfit strain beyond the critical thickness of GaN. Then a pair of dislocation lines will adjoin the misfit dislocation at its ends and threads up to the surface, forming two threading dislocations (TDs). Based on this, if a nucleation barrier layer (also referred to as the mask) is deposited to cover part of the foreign substrate onto which GaN cannot nucleate, the GaN directly grown onto the foreign substrate from where there is absence of nucleation barrier (referred to as the window) will then grow laterally over the mask. Such overgrown region (referred to as the wing) is mostly free of threading dislocations (TDs) and the TD-free wing region represents the desired region in the ELO-GaN. Basically, ELO samples contain three areas with different types of defects and densities: the areas grown from the window having high threading dislocation density, the pre-

coalescence laterally overgrown areas containing few bent threading dislocations and occasionally helical dislocations, and areas where two growth fronts meet (coalescence front) having a high dislocation density at the boundary and occasionally voids [35].

1.3.2 Towards Selective-area p-type Doping by ELO

A key difference between the growth of pre-coalescence ELO-GaN from the growth of continuous thinfilm lies in the contrast between 2D and 3D growth mode. The in-situ doping during the 3D growth mode unlocks an additional degree of freedom perpendicular to the basal-plane and naturally leads to the selective-area doping profile in the orthogonal 2D sectional views.

In fact, many research works in the recent decade have been devoted to the creation of 3D doping profile in GaN by using ELO process for optoelectronic applications such as InGaN microrods LED [36]. Following this line of thought, the defining feature of 3D growth mode might also endow the selective-area doping of GaN for power electronics with new opportunities. However, very few research works were available in the literature to have explored the possibility of the 3D growth and doping process enabled by the pre-coalescence ELO-GaN to achieve the desired selective-area doing profile for power electronic applications [37].

The main reason lies in that the 3D growth and doping process would eventually create the half-core-shell doping profile which is not suitable for a power electronic device to withstand high reverse blocking voltage and high current density. As a result, in order to achieve the desired selective-area doping profiles configured for an ideal power switching electronic device, innovative measures need to be taken in either materials growth or device processing stage. This will serve as one of the main topics of this dissertation, therefore it will be discussed in greater detail in Chapter 2.

1.4 Aim of the Study and Outline of the Dissertation

In this dissertation, the main focus was devoted to the innovative measures either in the material growth or device processing stage to tailor the half-core-shell doping profile enabled by the epitaxial lateral overgrowth of GaN into the desired selective-area doping profiles for power switching electronics featuring the building block of laterally patterned p-n junctions. In addition, the potential of the epitaxial lateral overgrowth to produce low-dislocation density GaN in the wing regions was also unleashed by virtue of the special selective-area doping structure-known as the true-lateral device architecture. Taking advantages of the true-lateral device architecture, the excellent electrical performances were demonstrated on a series of power devices from diodes to transistors, highlighted by the record high critical electric field in a GaN p-n junction and the record high current gain of a power bipolar transistor.

In Chapter 1, the background of this dissertation was introduced from a high-level perspective. The directions to improve GaN-a promising candidate for power switching electronics due to the high critical E-field-come from two aspects: reducing dislocation density and achieving selective-area doping capability. With this aim, the purpose to revisit the epitaxial lateral overgrowth of GaN was illustrated, which has strong promise to satisfy the two goals at the same time. Given that the dislocation density reduction by ELO was well established in the past decades, the promise of ELO to achieve the desired selective area doping profile for power devices warrants greater research.

In Chapter 2, the special ELO process employed in this dissertation was introduced and the advantage over conventional ELO was discussed. Then GaN stripe arrays with various half-core-shell doping profiles were grown by a combination of ELO and in-situ doping process. A series of methods of characterization were carried out to reveal the doping structure and also to investigate the planar defects identified in the stripes.

In Chapter 3, a set of device processing measures to tailor the half-core-shell doping structure into the innovative true-lateral device architecture were elaborated, preceded by the discussion of the advantages of the true-lateral device architecture over the true-vertical or quasi-vertical counterpart. Specifically, the converse-piezoelectric effect-induced stress issue associated with the true-vertical or quasi-vertical device structure was discussed. Then, the *p-n* junction diode (PND) and Schottky barrier diode (SBD) with the true-lateral device architecture were fabricated and characterized. The critical breakdown field was extracted and the theoretical critical field under the same condition was calculated by finite element analysis based on the impact ionization model.

In Chapter 4, a novel type of bipolar transistor known as gated lateral power bipolar junction transistor (GLP-BJT) was discussed with TCAD modeling. Then, the prototype GLP-BJT was experimentally demonstrated with the advantage of the true-lateral device architecture to further increase the current gain and breakdown voltage. On the other hand, another important bipolar transistor-insulated gate bipolar transistor (IGBT) was experimentally demonstrated on GaN by virtue of the special advantages of the true-lateral device architecture which otherwise would face formidable challenges to be fabricated.

In Chapter 5, alternative measures from material growth aspect were discussed to turn the half-core-shell doping structure into the desired selective-area doping profile featuring repeating laterally patterned *p-n* junctions on the GaN substrate. Such measures are categorized as a new type of growth and transfer. Material characterization techniques were carried out from different angles to evaluate the special selective-area doping profile. For the device application, the planar-gate vertical MOSFETs were demonstrated on the GaN substrate.

In Chapter 6, the state-of-the-art characterization techniques featuring high spatial resolution were carried out to investigate the elemental, dopant, and carrier distribution of the ELO-GaN

samples with selective-area doping profiles. Then the anisotropic diffusion model of Mg was built and the novel phenomenon associated with the diffusion behaviors of Mg in the ELO-GaN were provided with possible explanations. On the other hand, the application of delta-doping of Mg by diffusion in forming excellent Ohmic contact to *p*-GaN was demonstrated with success. Specifically, the capability to fully recover the Ohmic contact to plasma-damaged *p*-GaN shows a strong promise to address the bottleneck in this field of study, which should also lend a solid hand to greatly enhance the performance of p-n junction diode and bipolar transistors in future work.

In Chapter 7, the conclusion remarks and future outlook were presented.

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Chapter 2

ELO-GaN with Half-Core-Shell Doping Structure

2.1 ELO with Serpentine-Channeled Masks

2.1.1 Overview

The ELO-GaN samples that are employed in this dissertation are mainly grown on the three-layer mask patterned sapphire substrates. As briefly introduced in Chapter 1, the mask material (usually SiO_2, SiN_x) should function as the nucleation barrier to the epitaxial growth of GaN. In a conventional ELO mask structure, a single layer of mask is deposited onto the substrate with periodic openings (referred to as windows) [1]. Instead, the modified mask structure employed in this dissertation features staggered three-layer mask ($Si_3N_4/SiO_2/Si_3N_4$) forming a "Z"-shaped or serpentine-like channel.

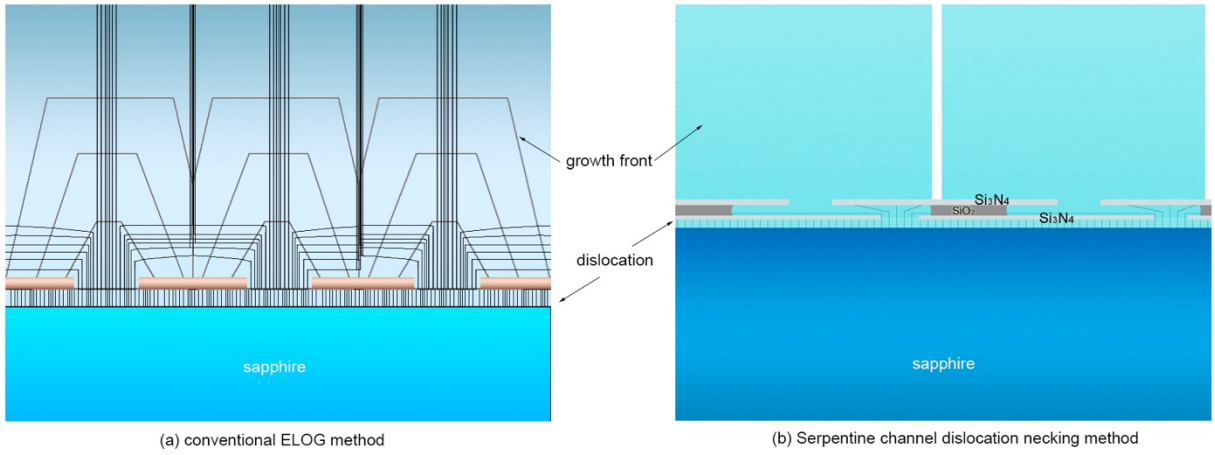


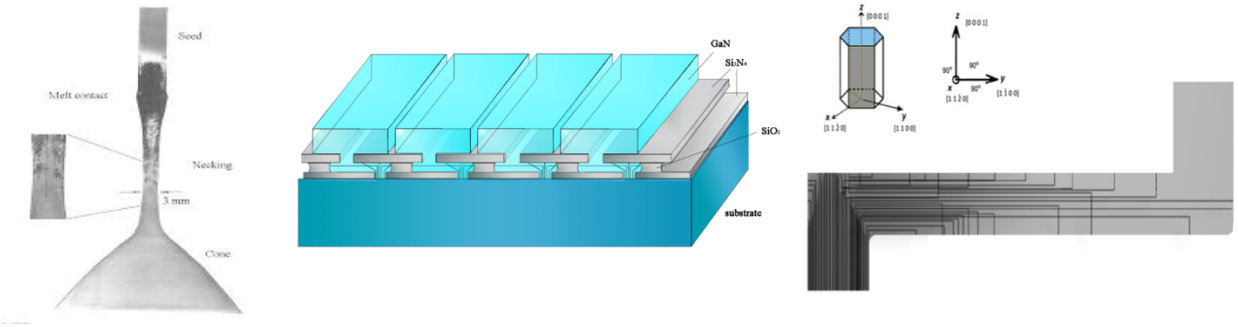
Figure 2.1 Comparison of dislocation reduction in (a) conventional ELO process and (b) ELO process with serpentine-channeled mask.

In general, the guiding principle of ELO is to minimize the crystalline portion of the film-substrate interfacial area and use such interface only for the purpose of enabling epitaxy [2]. This is the same with serpentine-channeled mask, and both of them start by patterning mask onto which

GaN cannot nucleate and only the windows between masks enable the epitaxial growth of GaN, which is also known as the selective area growth (SAG). As shown in Fig. 2.1 (a), in a conventional ELO process, after the growth of GaN from the window, the growth will be switched to the lateral mode by adjusting V/III ratio. A portion of threading dislocations (TDs) will bend due to the image force driving them to thread to the nearest surface. During the lateral growth, the TDs will meander and some may thread to the top surface, causing the remaining TDs in the lateral growth region. At the final stage of lateral growth, the growth fronts will coalesce with each other where numerous new defects are generated such as TDs (1D), stacking faults (2D) and micro-voids (3D). After the coalescence, the vertical growth resumes as the new TDs propagate along with the growth front before threading to the surface of the film. In this way, the dislocations can be reduced in the lateral overgrowth region (wing) but there are still two high-defects regions (i.e., window and coalescence front) per window [3].

In comparison, the ELO process with serpentine-channeled mask can further overcome some of the drawbacks of conventional ELO process by making the most of mask geometry and further filtering the TDs. The benefit of building the serpentine-channel with a length of horizontal part stems from the so-called "dislocation necking" process. As shown in Fig. 2.1(b) and Fig. 2.2 (c), when the growth is switched from vertical to lateral mode in the channel, some TDs are bent in a similar manner to those in a conventional ELO process, the unbent TDs will terminate at the nearest surface of the overhanging Si_3N_4. After the lateral growth is kept for a period of time, the growth is switched from lateral back to vertical mode so that the growth front can emerge from the top window with low dislocation density (the remaining TDs experienced twice bending). The subsequent growth is just the same as a conventional ELO process [4]–[6].

Then, in order to avoid the generation of numerous new TDs and stacking faults upon the coalescence of adjacent islands, the coalescence process could better be forestalled. Fortunately, this is not difficult to achieve since the coalescence process itself, on the contrary, is more difficult to achieve. As it appears, the window region in this modified approach has low dislocation density comparable to the adjacent wing regions, then the size of low dislocation density region is doubled compared to the conventional ELO process.



(a) (b) (c)

Figure 2.2 (a) An X-ray topography image describing the dislocation necking in a silicon boule (image courtesy of Wacker/Siltronic, Germany); (b) Schematic illustration of the GaN grown out of the double-layer mask; (c) Schematic drawing of the dislocation necking in the serpentine channel.

Furthermore, in addition to the dislocation bending during switches between lateral and vertical growth, it is also meaningful to discuss the filtering of dislocation within the lateral channel due to the necking process. Historically, the dislocation necking was originated from the well-known art in manufacturing large-volume dislocation-free silicon crystal (Czochralski method) [7]. As illustrated in Fig. 2.2 (a), a needle-like silicon seed is slowly pulled out of silicon melt. The condition at which the bottom of needle touches the melt is maintained very close to thermal equilibrium so that the melt will slowly solidify on the colder side away from the melt. It is important to note that dislocations glide along certain specific planes and directions in a crystal.

By carefully controlling the rate and the direction of pull-out while minimizing the probability of dislocation threading along the pull-out direction, dislocations will "shoot themselves out" by gliding out of the crystal within the narrow and long neck region. In this manner, as long as the long neck region has high aspect ratio, the final crystal will be completely free of dislocations.

Unlike the bulk growth from melt, one does not have the luxury of creating a vertical neck in the vapor phase epitaxy. Instead, as illustrated in Fig. 2.2 (b)(c), the neck would meander in parallel, rather than perpendicular, to the substrate surface. In analogy to the Czochralski method, the dislocation will be driven out of the parallel GaN neck since the TD gliding direction is out of the c-plane growth direction. As a result, it allows dislocations to be effectively filtered out. As such, the crystal, when growing out of the top mask windows, is entirely relieved of the mismatch strain while featuring low threading dislocation density [6].

2.1.2 MOVPE Growth

The MOVPE growths are carried out in a Veeco K465i GaN MOCVD system, as shown in Fig. 2.3. Both sapphire and Si are used as substrates for epitaxial growths. In the case of Si, AlN buffer layer (150 nm) is deposited to prevent meltback etching of GaN, also the deposition of AlN should precede mask patterning since AlN has no growth selectivity on the SiO_2/Si_3N_4 mask.

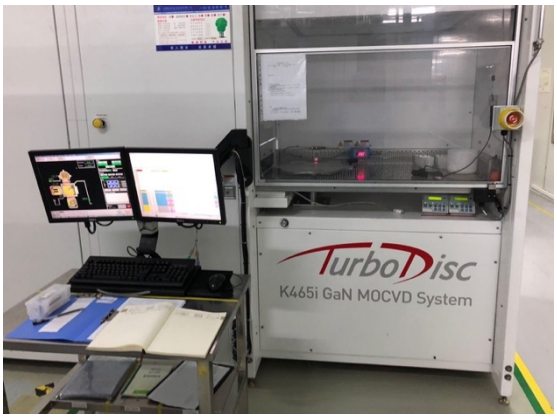


Figure 2.3 Veeco K465i GaN MOCVD system used for growing the ELO-GaN samples.

Table 2.1 The growth recipe for the ELO-GaN with half-core-shell n^+-u-p doping profile (the in-situ doping steps in red box is original contribution from this dissertation).

Step	H_2 (slpm)	N_2 (slpm)	NH_3 (slpm)	Ga (sccm)	Si (sccm)	Mg (sccm)	V/III	Temperature (°C)	Pressure (torr)	Time(min)
Bake	152	0	0	0				1060	100	3
Buffer	150	75	56	50			12000	540	100	20
Channel 1	150	75	56	20			30000	1022	100	126
Channel 2	150	75	56	40			15000	1022	100	62
Ramp	120	38	76	120			6800	1070	100	4
GaN:Si	120	38	76	120	20		6800	1070	100	60–80
UID-GaN	120	38	76	120			6800	1070	100	80–120
GaN:Mg	120	38	76	120		1000	6800	1070	100	25–120
780 °C, N_2 anneal, time: 6 min										
Cooling down: NH_3 135 L, time: 12min										

Table 2.2 The growth recipe for the ELO-GaN with half-core-shell n^+-u doping profile (the in-situ doping steps in red box is original contribution from this dissertation).

Step	H_2 (slpm)	N_2 (slpm)	NH_3 (slpm)	Ga (sccm)	Si (sccm)	Mg (sccm)	V/III	Temperature (°C)	Pressure (torr)	Time(min)
Bake	152	0	0	0				1060	100	3
Buffer	150	75	56	50			12000	540	100	20
Channel 1	150	75	56	20			30000	1022	100	126
Channel 2	150	75	56	40			15000	1022	100	62
Ramp	120	38	76	120			6800	1070	100	4
GaN:Si	120	38	76	120	20		6800	1070	100	60–80
UID-GaN	120	38	76	120			6800	1070	100	80–120
780 °C, N_2 anneal, time: 6 min										
Cooling down: NH_3 135 L, time: 12min										

Table 2.3 The growth recipe for the ELO-GaN with half-core-shell n^+-u-p-n^+ doping profile (the in-situ doping steps in red box is original contribution from this dissertation).

Step	H_2 (slpm)	N_2 (slpm)	NH_3 (slpm)	Ga (sccm)	Si (sccm)	Mg (sccm)	V/III	Temperature (°C)	Pressure (torr)	Time(min)
Bake	152	0	0	0				1060	100	3
Buffer	150	75	56	50			12000	540	100	20
Channel 1	150	75	56	20			30000	1022	100	126
Channel 2	150	75	56	40			15000	1022	100	62
Ramp	120	38	76	120			6800	1070	100	4
GaN:Si	120	38	76	120	20		6800	1070	100	60–80
UID-GaN	120	38	76	120			6800	1070	100	80–120
GaN:Mg	120	38	76	120		1000	6800	1070	100	25–120
GaN:Si	120	38	76	120	20		6800	1070	100	80
780 °C, N_2 anneal, time: 6 min										
Cooling down: NH_3 135 L, time: 12min										

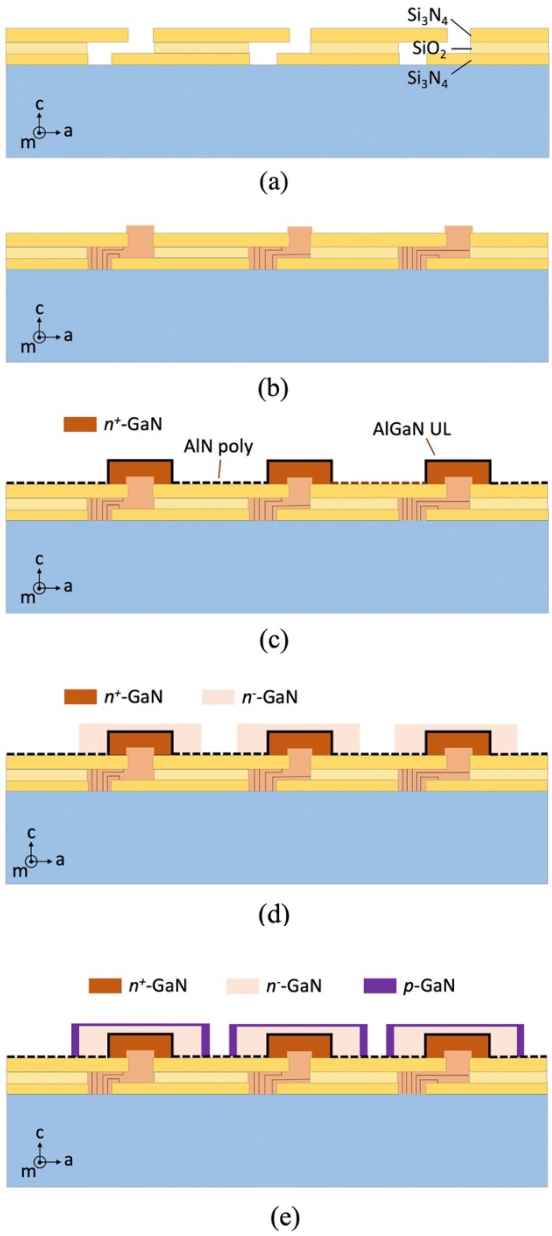


Figure 2.4 Schematic illustrations of the growth of GaN islands with rectangular core-shell doping profile: (a) Serpentine-channeled mask patterned on foreign substrates; (b) The lateral growth of GaN via serpentine-channeled mask; (c) 1st stage lateral overgrowth of n^+-GaN by in-situ doping of Si_{Ga} followed by AlGaN underlayer (UL) to intentionally introduce parasitic poly-AlN on the mask; (d) 2nd stage lateral overgrowth of n^--GaN (for both SBD and PND); (e) 3rd stage lateral overgrowth of p-GaN via in-situ doping of Mg_{Ga} (for PND only).

Figure 2.4 is a schematic illustration of the ELO process of an array of GaN islands combined with in situ doping at the example of the half-core-shell n^+-u-p doping profile [8]. The basic principle of in situ doping is to modulate the flow speed of dopant species at different stages of the ELO process. After the initial tiny GaN island grows out of the windows of patterned mask along $[1\bar{1}00]$, a high flow speed of donor species is supplied, producing a heavily-doped n-type region (in deep-orange), then the donor source is switched off or maintained at significantly low level. The growth parameters such as V-III ratio and pressure are adjusted in favor of lateral growth while an unintentionally doped (UID) or light-doped region is grown (salmon color). At the final stage, the acceptor species is fed into the growth chamber, producing moderate or heavily doped p-type region (violet region). In this way, GaN islands with half-core-shell n^+-u-p^+ (u denotes UID) doping profile are grown. The lateral dimension of each doped region can be well controlled by adjusting the flow duration and growth rate in the MOVPE chamber.

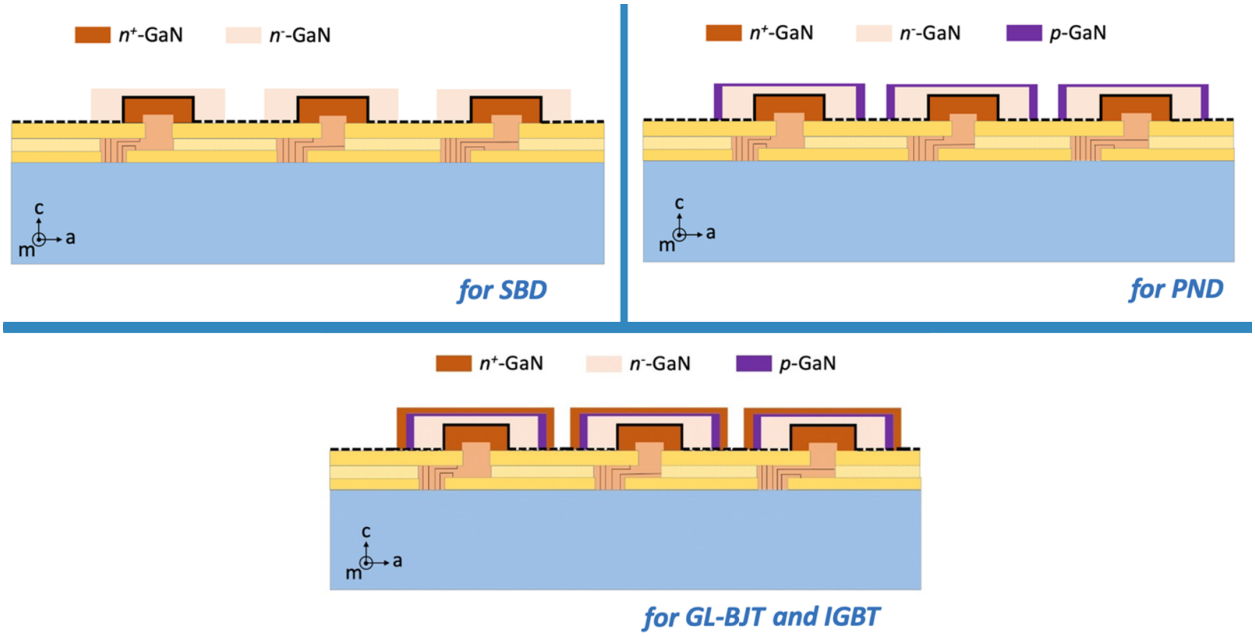


Figure 2.5 Schematics of ELO-GaN island with different types of half-core-shell doping profiles.

A couple of half-core-shell doping profiles of ELO-GaN islands were designed for different device applications. Specifically, after GaN island emerged from the top window region, the ELO process was carried out accompanied by the in-situ n^+/n^- doping for a Schottky barrier diode (SBD) (Fig. 2.5 (upper left)) or $n^+/n^-/p$ doping for a p-n junction diode (PND) (Fig. 2.5 (upper right)), or $n^+/n^-/p/n^+$ doping for transistors like MOSFET, BJT and IGBT (Fig. 2.5 lower). Table 2.1–2.3 summarize the growth parameters during every stage of MOVPE growth. The red boxes correspond to the in-situ doping steps where the growth time in each step determines the lateral width of each doping region. The green lines indicate the position where an AlGaN underlayer is inserted, which will be discussed below.

As an important original contribution from this dissertation, after growing the n^+-GaN core ([Si]~5×10^{19} cm^{-3}), an n^+-$Al_{0.2}GaN$ underlayer (UL) of ~15nm thickness was inserted mainly to form parasitic layer of polycrystalline AlN on the SiN_x mask. This was to suppress desorption of Si from the mask and reduce unintentional incorporation of Si into the subsequent n^-GaN [9]. The AlGaN UL was heavily n-type doped ([Si]>1×10^{19} cm^{-3}) so that the series resistance was made negligible comparing to the overall resistance of the diode, the related resistance calculation will be provided in the next section. Furthermore, low temperature growth of AlGaN UL is preferred to promote the deposition of polycrystalline AlN and to enhance Al incorporation. In addition to suppression of Si desorption from SiN_x mask, AlGaN UL also has some other benefits such as blocking the out-diffusion of O and Si from the n^+-GaN core (0D defect) [10], burial of points defects such as vacancy complexes (0D defect) in the underlying region, and suppression of the formation of dislocations (1D defect) or stacking faults (2D defect) [11], [12].

Impurity incorporation is a series concern especially in power electronics. For example, shallow donors like oxygen and silicon are particularly unwanted in the drift layer to withstand a

high blocking voltage. In order to suppress impurity incorporation during the growth, it is important to control the sidewall facet in the lateral overgrowth of UID-GaN. In principle, subject to the orientation of the mask window and growth parameters such as V-III ratio, pressure, and temperature, the GaN islands with various shape can be obtained. In this regard, the growth front in the *a*-direction should preferably be non-polar plane (*a*-plane) instead of semi-polar planes (i.e. r-plane). That is, a straight-vertical growth front is preferred over an inclined growth front for lower level of impurity incorporation, since it is established in the literature that semi-polar facets (inclined sidewalls) suffer from high concentration impurity of oxygen and carbon due to a high density of surface dangling bonds that tend to incorporate more impurity atoms [13]. The impurity incorporation such as oxygen on the vertical sidewalls ($(11\bar{2}0)$ planes) can be up to three orders of magnitude less than the inclined sidewalls ($(11\bar{2}2)$ planes) [14]. The experimental observation of this phenomenon is also discussed in the Chapter 6. As a result, it is important to keep the sidewalls of GaN islands vertically straight in the lateral overgrowth of GaN, like shown in Fig. 2.6 to have low impurity O incorporation.

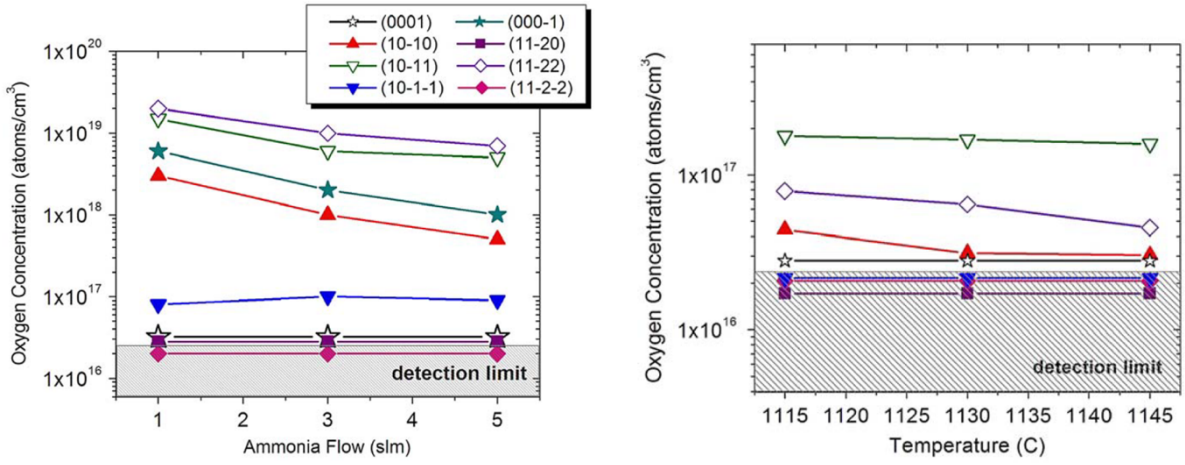


Figure 2.6 The oxygen impurity concentration on different planes of GaN measured by SIMS, whereas other impurities such as carbon also follow the same dependence with oxygen [13].

2.2 Characterization of the ELO-GaN Stripes

2.2.1 Optical Microscopy

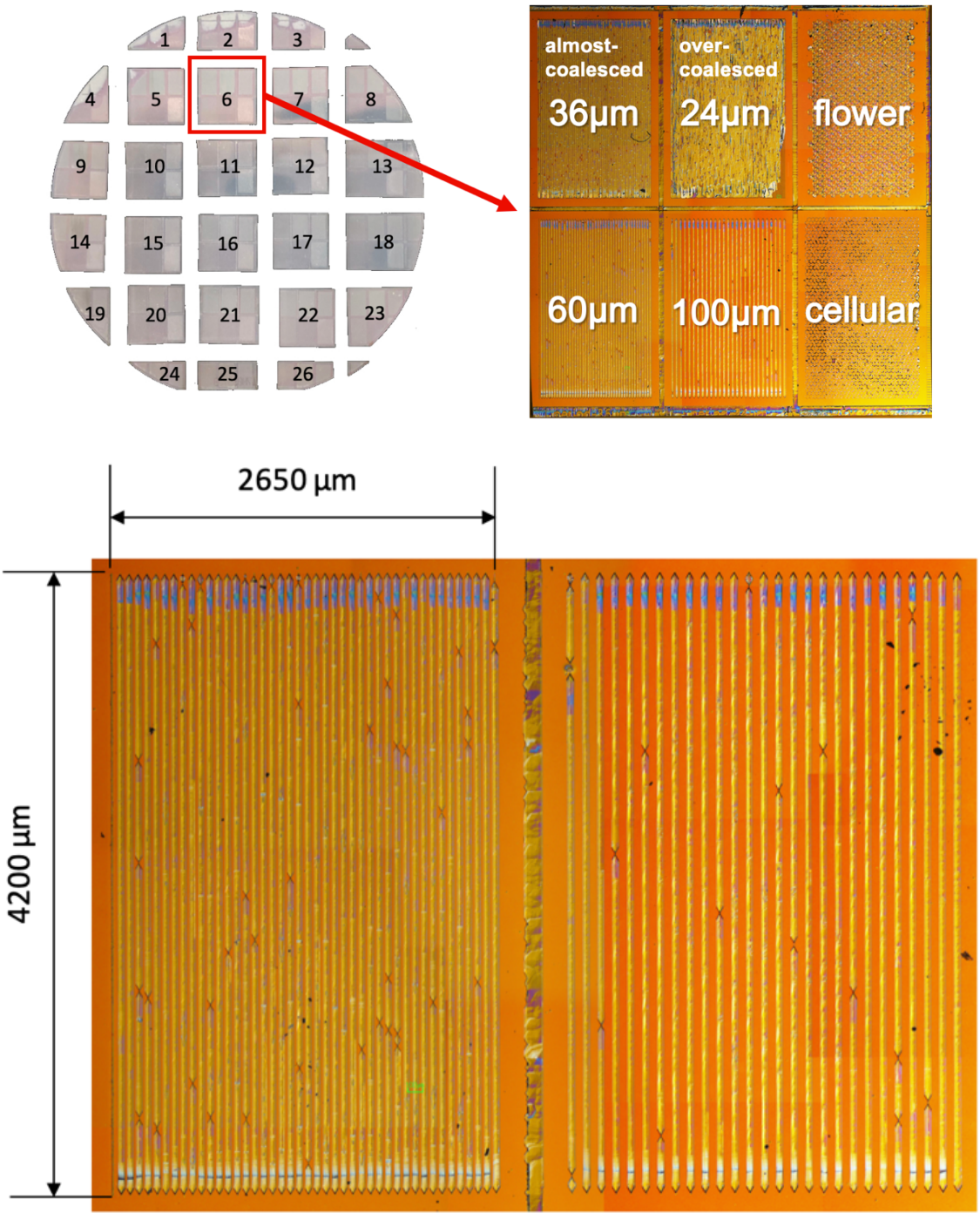


Figure 2.7 The enlarged panorama-view Nomarski optical microscopic picture of as-grown square-shape die with size of 1×1 cm^2.

Figure. 2.7 (upper left) is a real photo of the 2-inch wafer after it was laser cut into 26 dies with the size of each die being ~1 cm × 1 cm except at the edge. The panorama-view of a randomly-chosen die (#6) is presented in a collaged picture consisting of a few Nomarski optical microscopic images, as shown in Fig. 2.7 (upper right), there are six zones in total. The four zones on the left and middle columns with numbered labels are areas with long and narrow stripe-like mask windows. Each GaN stripe in this zone has a length of 4200 μm and width of less than 50 μm. The numbers in the labels indicate the spacing between each stripe-like mask window. For example, 36 μm means that the neighboring mask window has a spacing of 36 μm. In this batch of sample, GaN stripes in the 24 μm-zone have already coalesced into continuous thin film, while those in the 36 μm-zone are just about to coalesce. In comparison, the stripes in the 60 μm-zone and 100 μm-zone are far apart. The 60 μm-zone is preferentially chosen for device fabrication since the wider spacing between neighboring stripes allows for larger contact pads, which also makes it easier for probing during electrical characterization.

2.2.2 Scanning Electron Microscopy

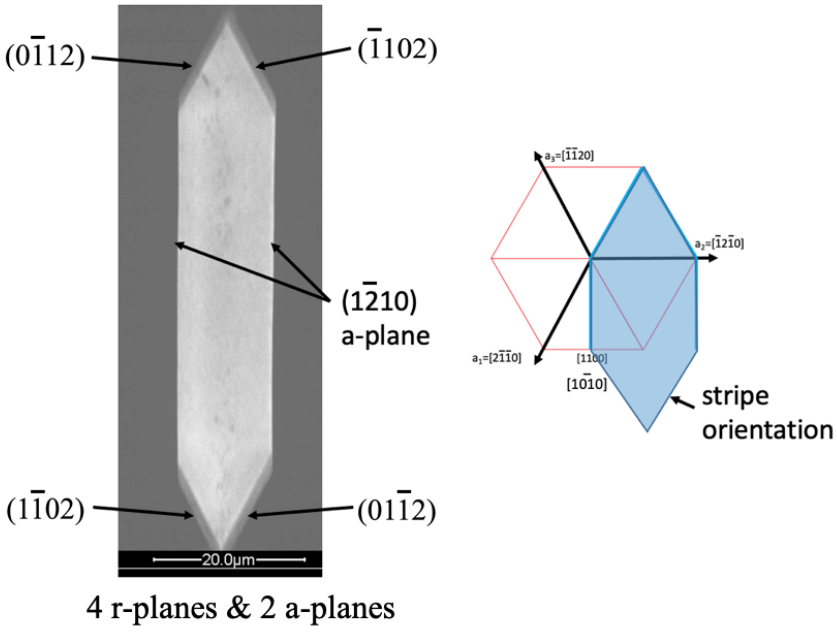


Figure 2.8 The sidewalls of a stripe consist of four r-planes and two a-planes.

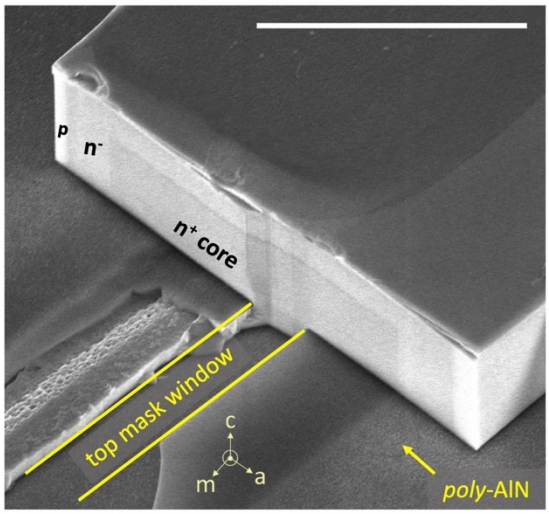


Figure 2.9 The angled-view scanning electron microscopic image shows the rectangular core-shell doping profile of the GaN island and parasitic deposition of poly-AlN on the top SiN_x mask. The boundary of polycrystalline AlN layer on the mask is in line with the inserted AlGaN UL which is sandwiched between the n^--GaN shell and n^+-GaN core. The scale bar is 10 μm.

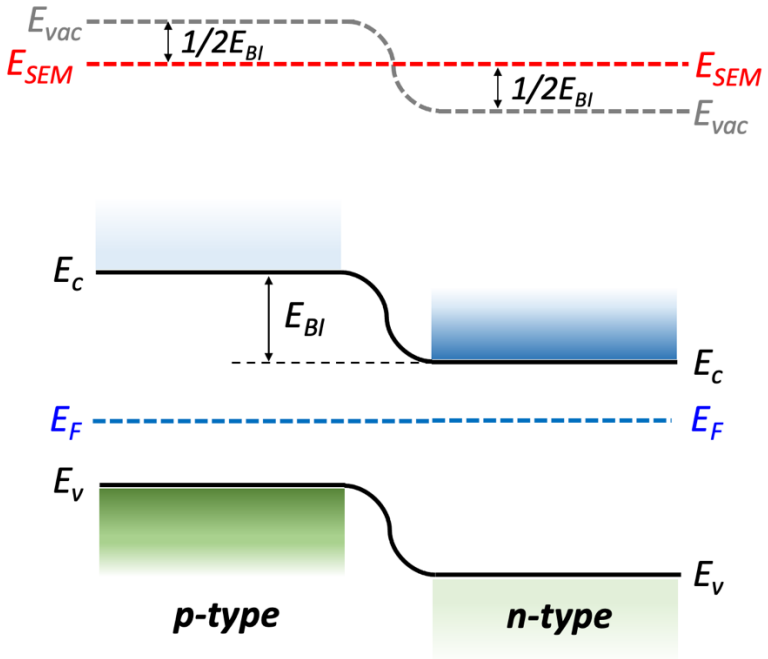


Figure 2.10 The band diagram shows the relative position of the energy levels of SEM detector and SEM vacuum with respect to that of a p-n junction in thermal equilibrium.

The morphology and dopant contrast were observed by using field-emission scanning electron microscopy (SEM) (Hitachi SU9000 and Hitachi SU4300) operated at 10 kV. Figure 2.8 shows a plan-view SEM image of the GaN island grown from a much short window length. The sidewalls of the island consist of four *r*-planes and two *a*-planes. The as-grown island features the same length with that of mask window, implying that the growth along $[1\bar{1}00]$ (radial direction of mask opening) is totally suppressed. The angled-view SEM image of the as-cleaved GaN island (one with the shortest n^--GaN lateral thickness of 2.5 μm) is shown in Fig. 2.9. The rectangular core-shell doping profile of $n^+/n^-/p$ and polycrystalline AlN onto the mask can be clearly distinguished where the shell p-GaN region appears as bright white region due to the dopant contrast of the secondary electron in SEM imaging. The boundary of polycrystalline AlN layer on the mask is in line with the inserted AlGaN UL which is sandwiched between the n^--GaN shell and n^+-GaN core

The dopant contrast is believed to stem from the built-in voltage of the p-n junction [15], [16]. As shown in the band diagram in Fig. 2.10 where E_{vac} is the energy level of vacuum and E_{SEM} is the energy level of SEM detector. In comparison, an extra energy of ½ built-in voltage (E_{Bi}) is required for secondary electrons (SEs) from n-type side to be collected by SEM detector. This leads to higher SE signal yield from the p-type region and as a result, higher brightness in the secondary-electron mode of SEM image. As a result, it is naturally understood that the built-in voltage is also a function of the dopant concentration on the n-type and p-type sides. That is to say, heavily doped p-GaN tends to have brighter region than a lightly doped p-GaN region. Therefore, dopant contrast of secondary electron of SEM imaging is an effective and convenient method to qualitatively characterize the selective-area doping polarity of GaN samples.

2.2.3 Fluorescence Microscopy

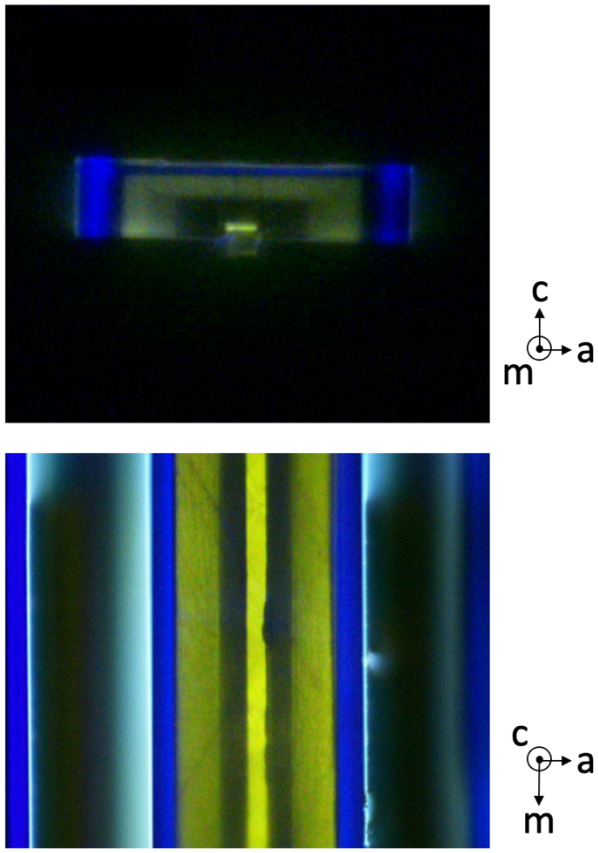


Figure 2.11 The fluorescence microscopic images (upper: cross-sectional view and lower: plan-view) of the as-grown GaN stripe (width: 27 μm) with the half-core-shell n^+-n^--p doping profile.

For direct-bandgap semiconductors like GaN, the information of defects and dopants could also be uniquely given off by a family of luminescence methods such as cathodoluminescence (CL) and photoluminescence (PL), based on the means of excitation source. The fluorescence microscopic imaging was based on the photoluminescence phenomenon. The fluorescence microscopic imaging measurements in this dissertation are performed on an optical microscope (Nikon LV150A) with mercury lamp illuminator (Nikon intensilight C-HGFI, wavelength 380nm). The microscope was not loaded with any filtering lens when the images were taken in the fluorescence mode so that all the colours in the image faithfully represented the in situ "true colours" of corresponding visible light emitted from different doping regions in response of the external

ultraviolet (UV)-light illumination. For example, the blue luminescence from the GaN: Mg region was associated with a broad peak centered at 2.94 eV (equivalent of 422 nm) attributed to conduction band electron-Mg acceptor transition in GaN at room temperature [17].

Figure 2.11 shows the cross-sectional view and plan-view fluorescence microscopic images of the as-grown GaN stripe for PND application. The half-core-shell n^+-n^--p doping profile can be readily observed. The p-region appears as blue color due to the aforementioned blue luminescence and the UID-GaN (n^--GaN) region appears as greenish yellow color due to the yellow-to-green luminescence in the GaN possibly due to carbon impurity or Ga vacancies [18]–[20]. In addition, the n^+-region appears as dark region due to the reabsorption of the yellow-to-green luminescence for the electron transition from shallow donor levels to the conduction band edge.

2.2.4 Cathodoluminescence Microscopy

Similar to photoluminescence (PL), the principle of CL is to subject the sample to a beam of incident electron beam where the acceleration voltage of the beam is on the order of thousands of voltages so that a myriad of electron-hole pairs (also termed as excitons) in the semiconductor material can be generated with energy transferred from the kinetic energy of the incident electrons. These electron-hole pairs will thermally diffuse in a "random walk" manner during their short lifetime before recombining either in a radiative manner by finally emitting a photon whose energy corresponds to the visible light spectrum, or in a non-radiative manner by emitting phonons (i.e., in the form of heat). Since threading dislocations generally serve as the role of non-radiative recombination centers, the dark spots in the luminescence image usually indicate the location of the end of dislocation with high areal resolution determined by the diffusion length of excitons [21]. In this way, TDD is closely associated with dark spot density in the cathodoluminescence microscopic image.

Figure 2.12 are the SEM and corresponding CL images of the selected area of as-grown GaN stripes on Si. The window length is short in this sample so that the GaN stripes appear as short stripe array in each column. As seen from CL image in Fig. 2.12 (c), there is almost no dark point on the stripe, suggesting the stripe has low threading dislocation density. On the other hand, at the position of the align mark region (as shown in Fig. 2.12 (e)) where there is only one layer of mask deposited on the substrate, Fig. 2.12 (d) shows that a dark line exists along the center of each stripe, as a result of the unfiltered dislocation grown out of the window, typical in a conventional ELO. The comparison between (c) and (d) provides a clear proof that the filtering of dislocation is effective in the window region with double-mask bounded serpentine channel, thus revealing the advantage of doubling the width of low dislocation density region per window compared to the conventional ELO process.

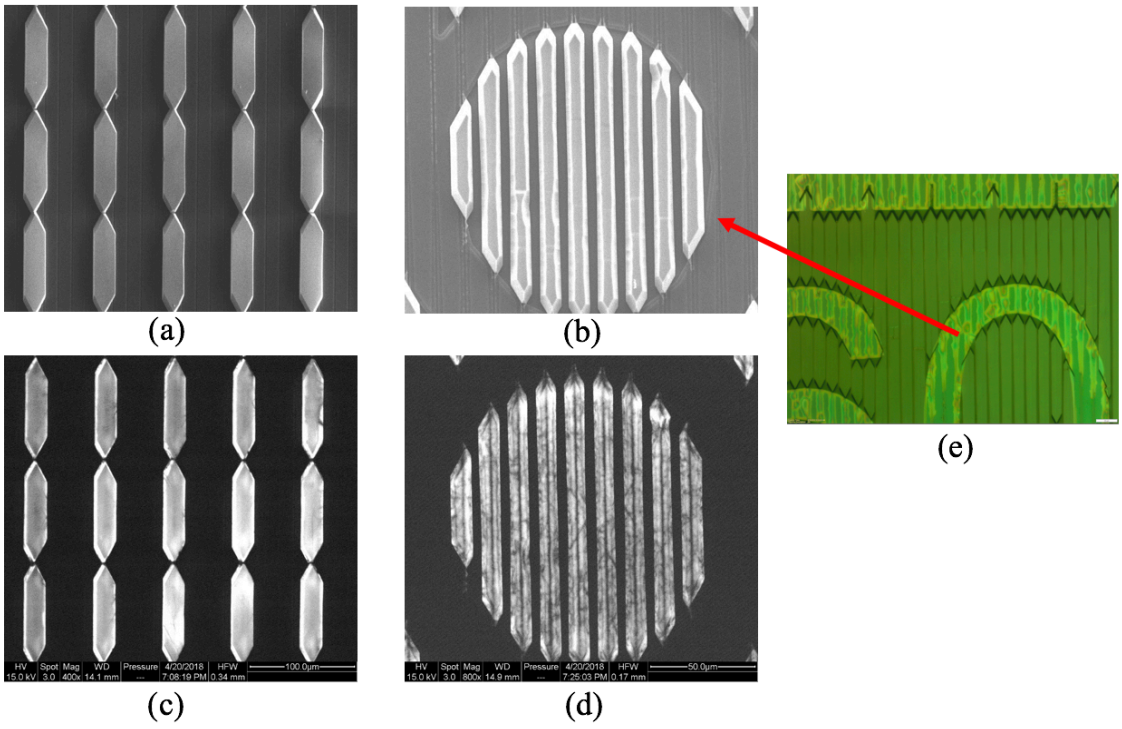


Figure 2.12 The SEM and corresponding CL images of the selected area of as-grown GaN stripes on Si. (a) The SEM image showing the 85 μm-long-stripes and its corresponding CL image (c);

(b) The SEM image showing GaN stripes growing from the aligning mark region (e) where only a single-layer mask is present and its corresponding CL image (d); (e) The optical microscopic image of the zoom-out align mask region compared to (b). (Images from (a) to (d) by courtesy of the collaborators with Peking University).

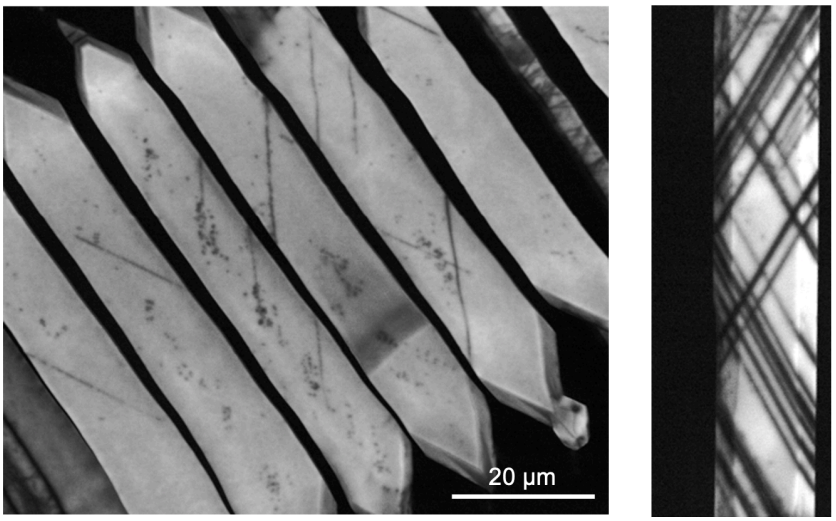


Figure 2.13 (Left) CL image showing the typical issue of "inclined dark line" across a few stripes; (right) high density of dark lines across a stripe.

In addition to dislocation distribution, as the CL images show in Fig. 2.13, there is occasionally an array of straight dark lines crossing the GaN stripes which form a fixed angle of 30° (or 150°) to the radial direction (m-axis) of the stripes (Fig. 2.13 (right). The nature of such straight dark lines could not be well unraveled just from a CL image due to its rather limited depth resolution. The study of such defect is presented in the subsequent section.

2.3 Stacking Faults in the ELO-GaN Stripes

Following the preceding section, in order to unravel the nature of the defect appearing as straight dark line in the CL images, a novel type of photoluminescence microscopy, known as the multiphoton microscopy (MPM), is utilized to obtain the depth profile of such defect [22]. In comparison, multiple-photon photoluminescence (or two-photon photoluminescence in most real

cases) offers depth imaging with much finer resolution. In a two-photo photoluminescence (2P-PL) setup, two photons with the same energy need to be absorbed at the same time in order to excite a valence electron over the band gap. Because the probability of electron transition by simultaneous absorption of two photons is naturally several orders lower than a single photon absorption, the otherwise blurring out-of-focus luminescence associated with a single photon absorption is absent in the 2P-PL where it is much weaker than the strong luminescence occurred at the focal point. As a result, the MP-PL (or 2P-PL) is capable of providing much finer depth-resolution luminescence information [23].

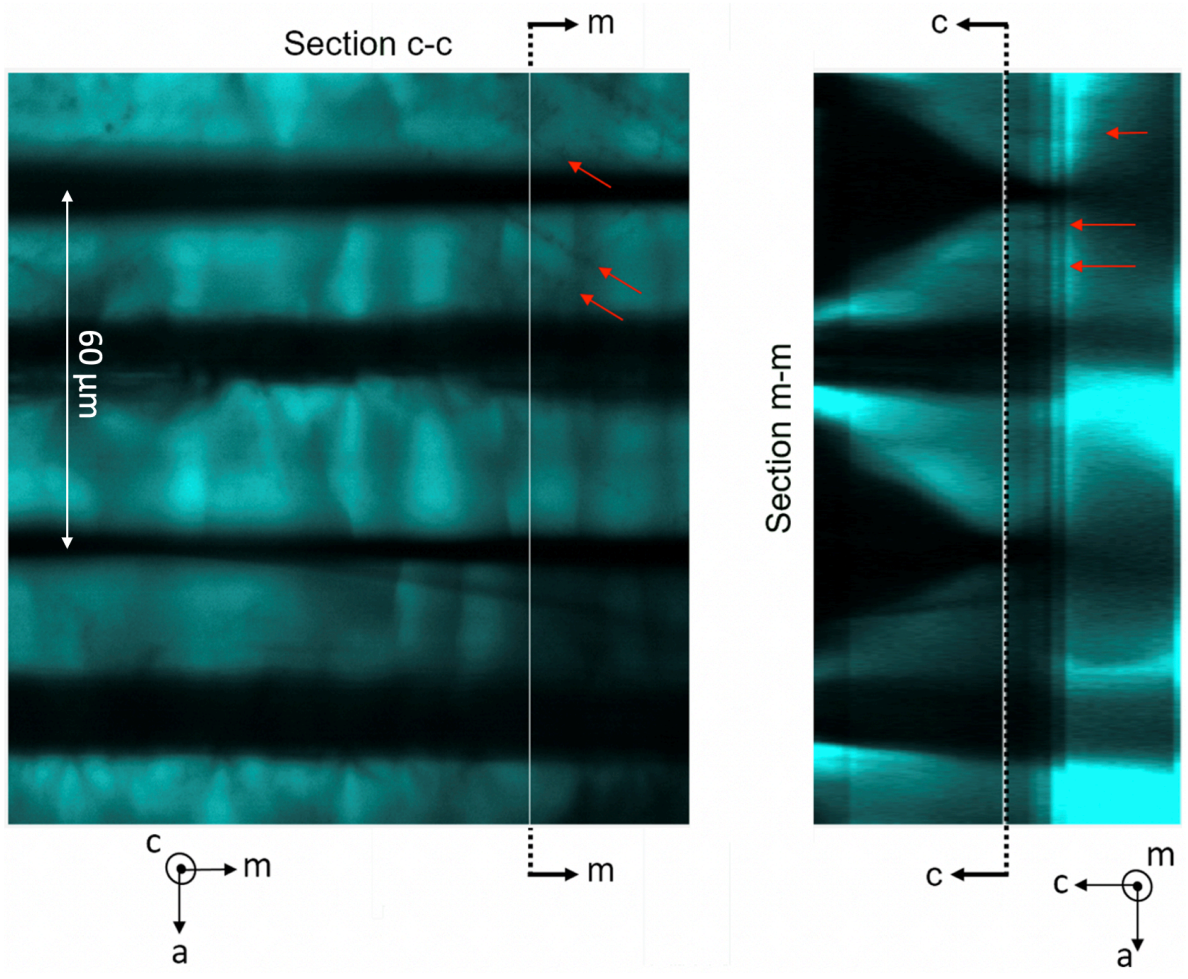


Figure 2.14 The depth-scanning multiple-photon luminescence images (near-band emission). The left presents a cross-sectional c-plane MP-PL image taken at the vertical position (c-axis) indicated

by the dashed line in the right image, whereas the right presents a cross-sectional m-plane MP-PL image taken at the lateral position (m-axis) indicated by the dashed line in the left image, respectively. The array of stacking faults in each image are indicated by the red arrows.

Figure 2.14 shows the depth scanning multiple-photon luminescence images (near-band emission) of the coalesced stripes grown by a hybrid of ELO growths combining MOVPE and halide vapor phase epitaxy (HVPE). The MOVPE growth part is the same as that in this Chapter. The detailed description of the hybrid growth and doping profile related to this unique doping structure will be discussed in Chapter 5 and Chapter 6. The formation of continuous film by the coalescence of stripe arrays and the film thickening process enables the sample to be characterized by MPPL which otherwise would be too thin to collect sufficient number of images due to the depth resolution being ~2 μm. It can be seen that there are periodic parallel dark stripes along m-axis in the left image. Among them, the thinner dark stripes correspond to the tip region of the dark triangles in the right image, suggesting that the dark contrast is due to the p-type GaN where the near-band emission is suppressed by band-to-acceptor transitions. On the other hand, the thicker dark stripes correspond to the coalescence region of the GaN stripes abounded with defects. In addition, some GaN stripe-crossing dark lines can also be observed in the cross-sectional c-plane MP-PL image like those in the fluorescence microscopic image or cathodoluminescence image. Most importantly, the corresponding cross-sectional m-plane MP-PL image helps greatly to unravel the depth profile of these defects which appear as an array of dark lines parallel to the c-axis. The appearance of the defect in the form of dark line in every orthogonal cross-sectional view suggests that it is essentially a planar defect that is parallel to the c-axis and also forms a 30° angle to the m-axis, making it a prismatic stacking fault (PSF) on m-plane. It should also be noted that the presence of PSFs in the ELO-GaN was rarely observed, whereas most of the stacking faults

observed in the literature was basal-plane stacking fault (BSF). Therefore, the formation of such m-plane PSFs in the ELO-GaN stripes along m-axis merits further investigation.

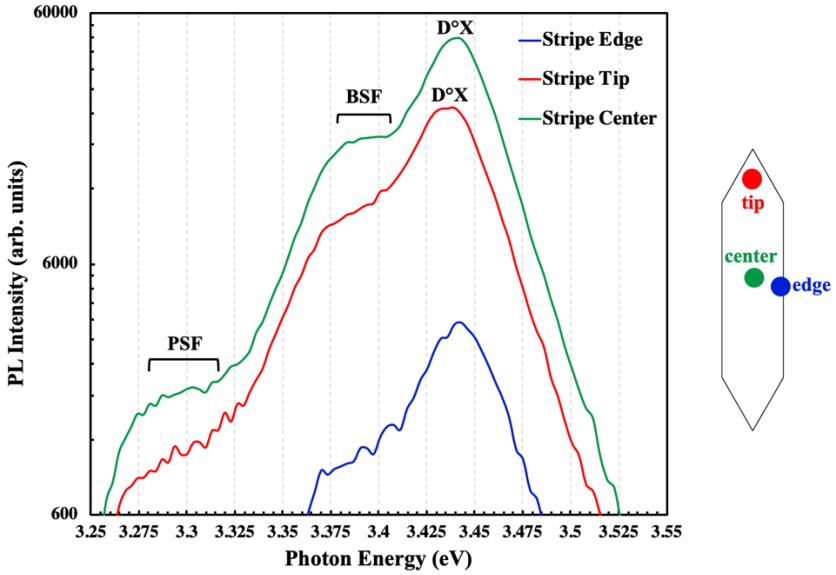


Figure 2.15 Low-temperature PL spectra of the non-doped sample where three kinds of positions are sampled.

In addition to the straightforward evidence provided by the luminescence microscopic imaging, the presence of PSFs can further be supported from the emission spectra analysis. Due to the fact that defects such as stacking fault are optically active, the low-temperature photoluminescence (conventional single-photon luminescence) spectroscopy was carried out at 80 K where the sample being measured was kept and cooled in a liquid nitrogen setting. Figure 2.15 shows the normalized PL spectra for the non-coalesced and non-doped GaN stripes sample. Three kinds of positions on the stripe (stripe edge, stripe tip and stripe center) were sampled. In general, two or three emission bands are found in each position. The near-band edge peak (NBE) near 3.44 eV is associated with donor bound excitons D˚X in GaN and the broad emission band at 3.40 eV is possibly associated with BSFs. In addition, some weak overlapping emission peaks between 3.27-3.33 eV, which are potential due to prismatic stacking fault [24]–[26]. These PL spectra may

further strengthen the evidence of the presence of prismatic stacking faults in the as-grown GaN stripes. For future improvement, to enhance the sharpness of the emission bands and to distinguish individual peaks in the PL spectra, the PL spectroscopy could be carried out in a lower temperature under 10 K (cooled with liquid helium environment).

The presence of the stacking faults were observed to degrade the voltage blocking capability of the true-lateral p-n junction diodes fabricated on the ELO-GaN stripes, as will be discussed in the next Chapter. The reason may be due to the role of prismatic stacking faults as preferential sites for O (a type of shallow donor in GaN material) incorporation, forming a plane of heavily-doped GaN in the otherwise lightly-doped drift region and increasing the leakage current under reverse bias. As a result, it is imperative to reduce the density of the PSFs in the GaN stripes in order to improve the yield of the good-performance devices.

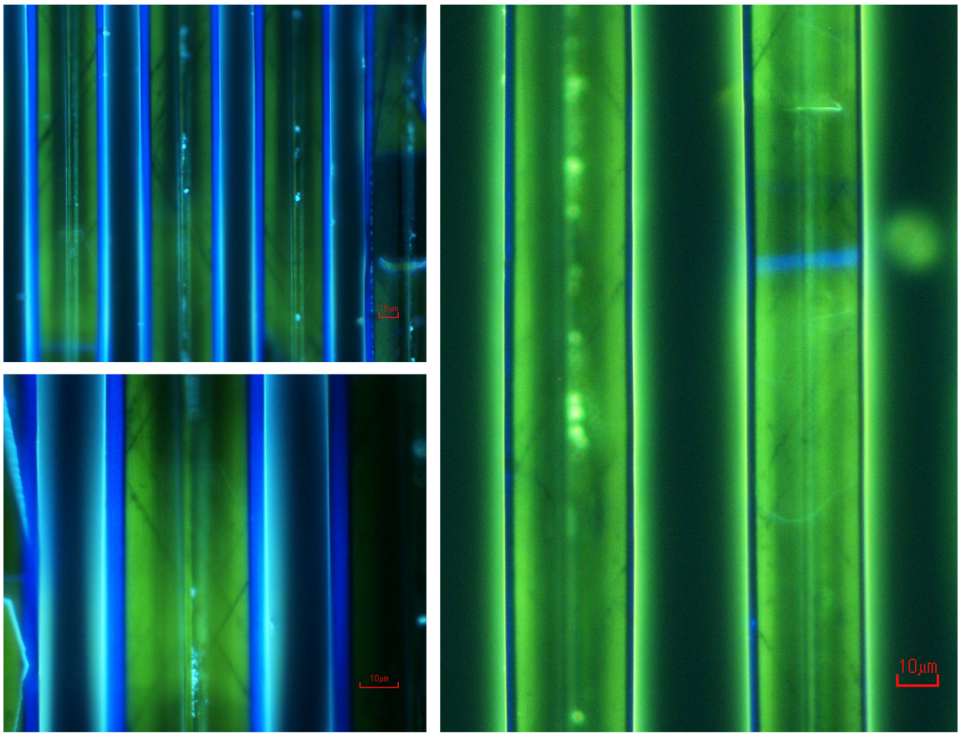


Figure 2.16 The PSFs in the ELO-GaN stripes without the insertion of AlGaN underlayer revealed in a group of plan-view fluorescence microscopic images.

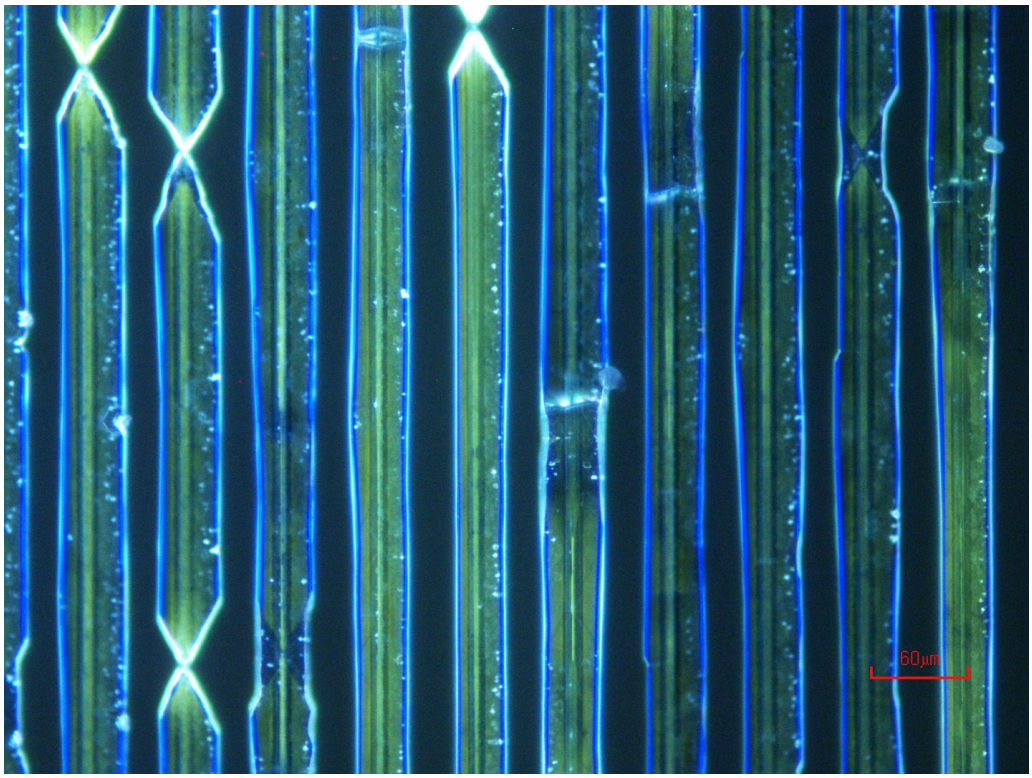


Figure 2.17 The suppression of PSFs in the ELO-GaN stripes with the insertion of AlGaN underlayer observed by fluorescence microscopy.

In an effort to suppress the formation of PSFs in the GaN stripes, it is found that the insertion of AlGaN underlayer also helped reduce the density of the m-plane PSFs in the ELO-GaN stripes, which is consistent with some similar findings in the literature [11], [12]. The GaN stripes grown without and with the insertion of AlGaN underlayer are shown by fluorescence microscopy in Fig. 2.16 and Fig. 2.17, respectively. By comparing the two figures, it is suggested that the insertion of AlGaN heterostructure in GaN lattice may effectively suppress the formation of the m-plane PSFs. Along this line of effort, it is anticipated that the introduction of AlN/GaN super-lattices may further reduce the PSF density in the GaN stripes, which could be potentially utilized in the future growth plans.

2.4 Summary

In this Chapter, the special epitaxial lateral overgrowth method of GaN employed in this dissertation was introduced and the advantages of it over conventional ELO process was discussed. Then GaN stripe arrays with different half-core-shell doping profiles were grown by a combination of ELO and in-situ doping process. A series of methods of characterization were carried out to reveal the doping structure and also to investigate the planar defects present in the stripes. In addition, the modified method was discussed by inserting AlGaN underlayer during the growth of stripes which proved effective to suppress the formation of planar defects and also to suppress the desorption of Si from the underlying SiN_x mask during the growth process due to the intentional deposition of polycrystalline AlN on the mask. The GaN stripes with half-core-shell doping profile laid the solid basis for the subsequent fabrication of power electronic devices including diodes and transistors, which will be further discussed in the subsequent Chapters.

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Chapter 3

True-lateral Diodes on ELO-GaN

3.1 Rational

3.1.1 True-vertical and Quasi-vertical Device Architecture

In order to investigate the true capability of GaN as power devices, pin junction (or p^+-n^- junction) is a preferred structure to extract the preliminary information of critical field, off-state breakdown voltage and on-state resistance. Not only it can be used as a rectifier in the high voltage application, but also it is the building block of many transistors. As such, the success in fabricating a good power p-n junction diode (PND) lays the solid foundation for the potential success in fabricating a GaN MOSFET, BJT or IGBT.

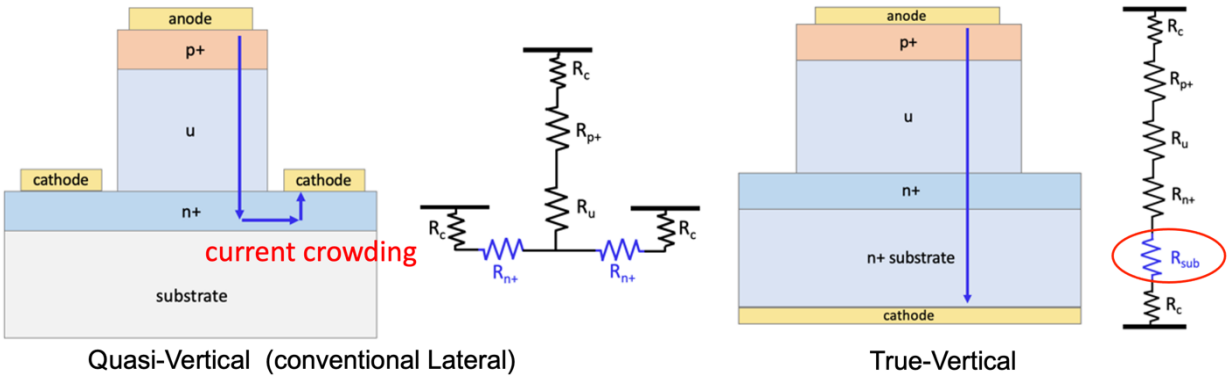


Figure 3.1 Schematic illustrations of quasi-vertical (left) and true-vertical (right) PNDs and their equivalent resistance.

In terms of the device architecture of GaN PND, there are two conventional types: fully-vertical (also called true-vertical) and quasi-vertical (also called "lateral" device) [1]. Figure 3.1 (left) shows a schematic illustration of a quasi-vertical PND, of which p- and n-type contacts are positioned on the same side of the substrate with different height. Therefore, the current flow in such geometry is actually a combination of vertical and lateral components. As indicated by the

blue arrow in Fig. 3.1, as a natural tendency to reduce resistance, most electrons tend to cut the corners in their path. Otherwise, the current from the center of diode would have traversed an excessive long lateral distance to reach the cathode than the current at the edge of anode. As a consequence, the distribution of charge carriers is highly nonuniform as they are preferentially flowing near the vicinity of the anode edge, leading to the so-called "current crowding" issue [2], [3]. The nonuniform high current density also causes excessive joule heating and reliability issues.

Comparatively, in the case of fully vertical device architecture (Fig. 3.1, right), current can flow straight from top anode into bottom cathode without turning directions, allowing it to distribute uniformly. As such, larger current can be handled [4]. This is the reason why a fully-vertical device is much preferred over a quasi-vertical type, and the latter is usually a compromised choice for insulating substrate such as sapphire or AlN buffer layer on Si: the electrically insulating nature makes them inapplicable to fully-vertical architecture [5], [6].

In spite of the overwhelming advantages, the fully vertical device also has a couple of shortcomings. As most of today's fully vertical GaN device is grown on n-type GaN substrate, in addition to the extremely expensive GaN substrate which is 100 times that of sapphire or Si [7], the backside contact, on the albeit heavily-doped substrate, has series resistance R_{sub} of a thick substrate. For a typical value, R_{sub} is 0.45 mΩ.cm^2 for a 400 μm-thick commercial n-GaN substrate with Si concentration of 2×10^{18} cm^{-3}. This is non-negligible for today's state-of-the-art GaN-on-GaN diode featuring $R_{on,sp}$ less than 1.0 mΩ.cm^2.

Besides, the converse piezoelectric effect (CPE)-induced stress may also become a serious issue. This reliability issue has been experimentally identified in the AlGaN/GaN heterojunction-based transistors where micro-cracks are found to be introduced [7]. However, it has not been recognized in the vertical device architecture possibly due to that the study of GaN vertical devices

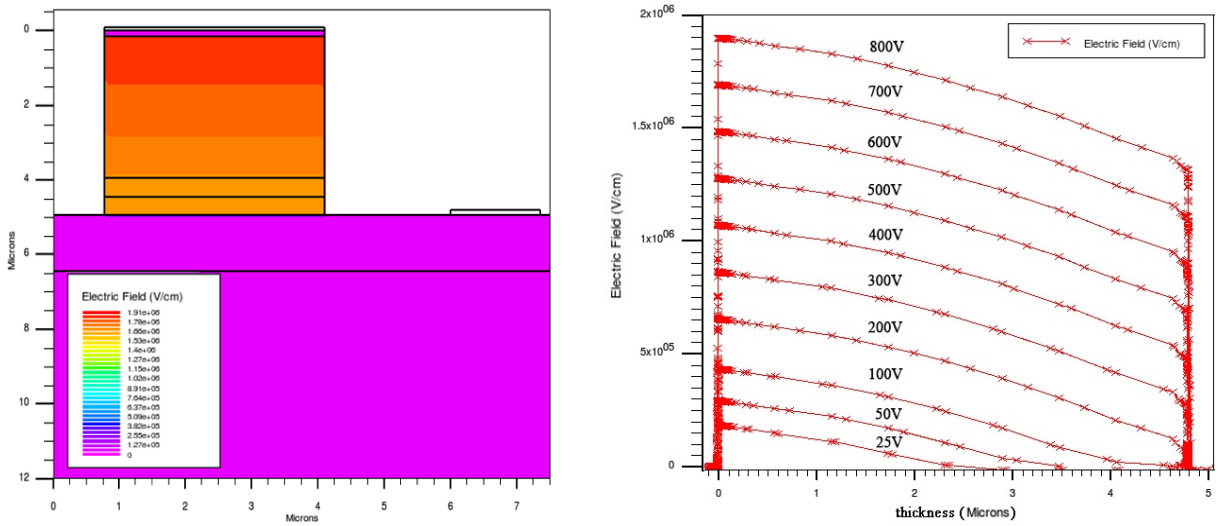
is still in its infancy where the static performance is most often studied. In contrast, the switching performance is not sufficiently investigated especially under the high reverse bias condition, and the latter case is when such reliability issue is expected to occur. The detailed theoretical estimation and FEA modeling of the CPE-induced stress issue in the polar GaN high voltage devices is presented in the following section.

3.1.2 CPE-induced Stress and Reliability Issue

Wurtzite GaN possesses piezoelectricity and converse-piezoelectricity along the c-axis. The former effect is known to contribute to the two-dimensional electron gas (2DEG) in the AlGaN/GaN heterostructure field effect transistor (HEFT) [8] and to motivate non-polar and semi-polar LEDs [9], while the latter effect is non-trivial in the case of high electric field common to a power electronic device. For example, a crack is likely to occur beneath the gate edge on the drain side of the AlGaN/GaN HEFT where the E-field peaks and vertically propagates across the whole AlGaN layer, even during the ON-state after hours of operation [10].

Before the CPE-stress is calculated in the drift layer of PND, it is necessary to identify the case where the CPE stress is significant. Two regimes exist for the distribution of reverse blocking voltage in the drift layer: non-punch-through (NPT) and punch-through (PT) [11]. A NPT design of the drift layer corresponds to the case where drift layer thickness is equal or larger than the parallel plane avalanche breakdown depletion width. Likewise, a PT design corresponds to a drift layer thinner than the parallel plane avalanche breakdown depletion width. The transition from NPT state to PT state occurs when the reverse bias rises beyond a threshold value.

In order to increase the breakdown voltage while not giving rise to $R_{on,sp}$, the PT design is preferred over NPT counterpart. Also, a PT design can give a lower specific drift layer resistance for a given targeted breakdown voltage.



(a) (b)

Figure 3.2 (a) Simulated field distribution in the drift layer under punch-through state and (b) the field distribution in the drift layer under various reverse bias.

Figure 3.2 shows the simulated distribution of electric field across a 4.8-μm-thick drift layer having a gradually changing doping concentration from 10^{16} cm^{-3} (near n^--n^+ interface) to 10^{15} cm^{-3} (near p-n junction). It is seen in Fig. 3.2 (b) that the NPT states correspond to "triangles" while PT states correspond to "trapezoids". The triangle-to-trapezoid transition occurs above 100 V. As reverse bias increases from 100 V to 800 V, the right-leg of the trapezoid also raises.

The following numerical calculation provides an order-of-magnitude estimate of CPE-induced stress. One of the coupled forms of piezoelectricity can be written as:

$$S_{ij} = s_{ijkl} T_{kl} + d_{kij} E_k \tag{3.1}$$

or expressed in an extended form for the 6mm crystal class [12]:

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \begin{bmatrix} s_{11}^E & s_{12}^E & s_{13}^E & 0 & 0 & 0 \\ s_{21}^E & s_{22}^E & s_{23}^E & 0 & 0 & 0 \\ s_{31}^E & s_{32}^E & s_{33}^E & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44}^E & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{55}^E & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{66}^E = 2\left(s_{11}^E - s_{12}^E\right) \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} 0 & 0 & d_{31} \\ 0 & 0 & d_{32} \\ 0 & 0 & d_{33} \\ 0 & d_{24} & 0 \\ d_{15} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{3.2}$$

where S is strain, s is compliance, T is stress, d is piezoelectric coefficient, E is electric field intensity, as a result,

$$d_{33} = (\frac{\partial S_3}{\partial \varepsilon_3})^T \tag{3.3}$$

The values of the d_{33} coefficients for GaN is reported to be 3.1 pm.V^{-1} [13], so $d_{33} = 3.1\ \text{pm.V}^{-1} = 3.1 \times 10^{-10}\text{cm.V}^{-1}$, if the field in the drift layer is assumed to be $2 \times 10^6\ \text{V.cm}^{-1}$, then $S_3 = d_{33}\varepsilon_y = 3.1 \times 10^{-10}\text{cm.V}^{-1} \times 2 \times 10^6\ \text{V.cm}^{-1} 6.2 \times 10^{-4} = 6.2 \times 10^{-4}$.

If the elastic modulus for GaN is 330 GPa [12], the stress corresponds to the strain S_3=6.2×10^{-4} should be $T = S_3 E_{GaN} = 6.2 \times 10^{-4} \times 330\ \text{GPa} = 0.204\ \text{GPa}$. (3.4)

To draw a comparison of such stress to a thermal stress, the thermal expansion coefficient α_a =5.59x10^{-6} K^{-1} for GaN and α = 3.60x10^{-6} K^{-1} for Si, then the value of S_3 will roughly correspond to thermal mismatch induced strain in GaN-on-Si over a temperature difference of 300°C. In addition, considering the CPE-induced strain rate is much larger than thermal stress rate, the actual influence should be much more serious.

As a result, the issue is identified with related to CPE in the high field region of a PND. As shown in Fig. 3.2, when the drift layer is deeply punched through, the sharp drop in electric field across the n^-/n^+ becomes appreciably large, which induces considerable shear stress across the interface. For the commonly used (0001) GaN, there is a tendency for the drift layer to shrink under reverse bias when E-field is along $[000\bar{1}]$ which is restrained by the bulk substrate, thus leading to a tensile stress in the GaN drift layer. This is quite similar to the cooling of GaN on Si, where GaN tends to shrink more than Si thus being under tensile stress.

In order to relieve this issue, the approach of "step-graded doping" can be adopted. This is similar in principle to the practice of "compositionally step-graded AlGaN buffer layer" to relieve the large thermal mismatch between GaN and Si, as AlN has thermal expansion coefficient

between GaN and Si. Likewise, as shown in Fig. 3.3, by inserting step-graded n-type doping buffer layers between lightly doped and heavily doped layers, the high stress across the n^-/n^+ interface can be reduced.

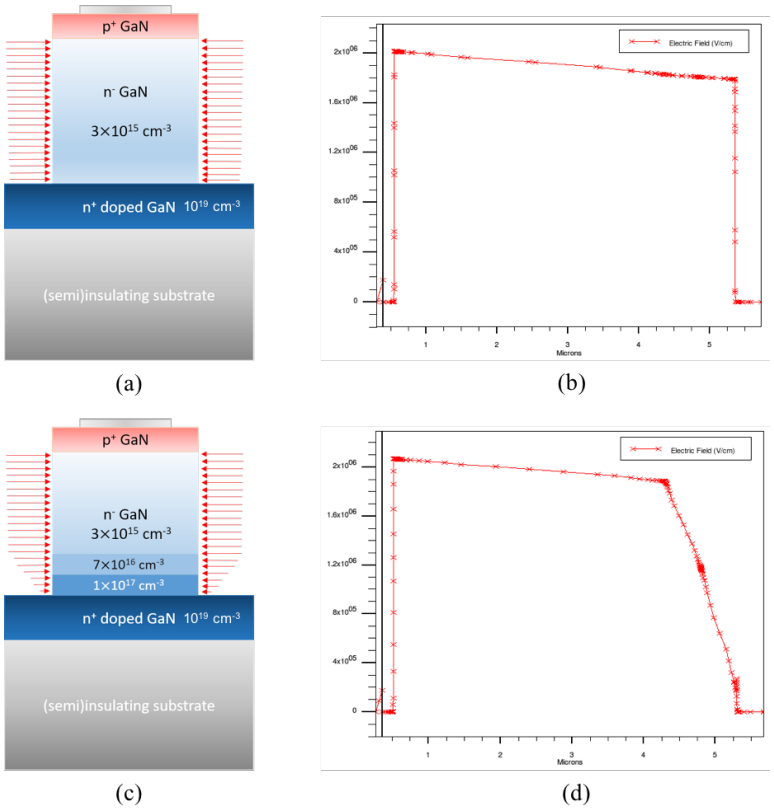
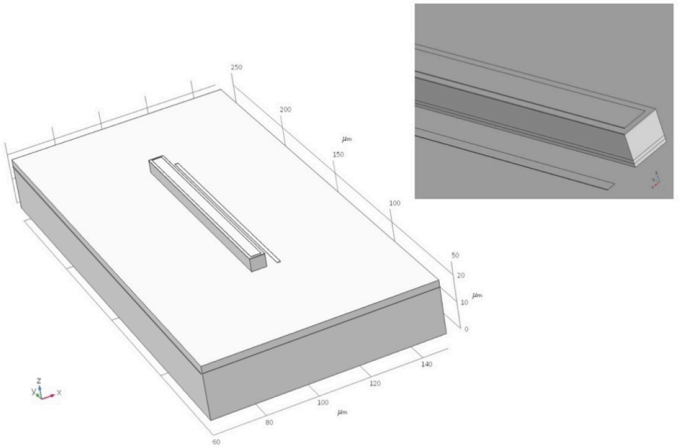


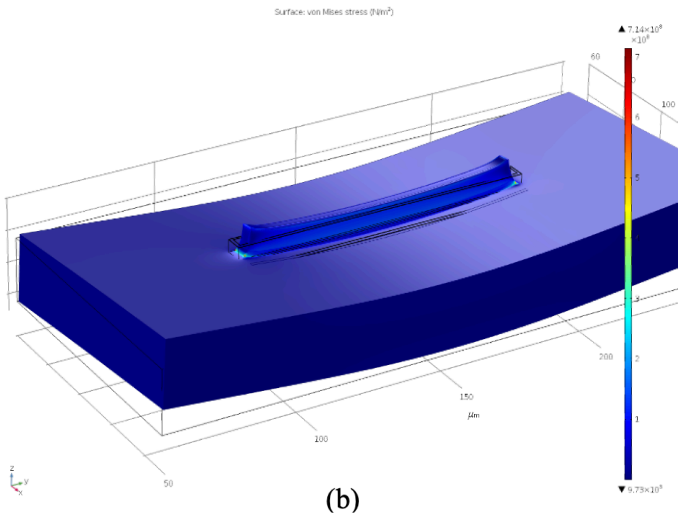
Figure 3.3 The schematic illustration of high-field induced stress in the fully-depleted drift layer. (a) without step-graded doping buffer layer and (b) its corresponding electric field distribution; (c) with step-graded doping buffer layers and (d) its corresponding electric field distribution.

The stress simulation is performed using COMSOL Multiphysics-a commercial FEA software suitable for the study of interdisciplinary physical quantities such as converse piezoelectricity or thermal stress. The modeled PND is on a 100 μm-long-stripe resembling the ELO-GaN island. The n^- drift layer of the diode is 4.8μm with doping concentration of 3×10^{15} cm^3. The stereographic view of the modeled structure (with top and side electrodes) is shown in Fig. 3.4 (a), and the inset shows the structure with step-graded doping buffer layers. Fig. 3.4 (b) shows the simulated stress

distribution of the whole structure without step-graded doping buffer layer. The deformation is shown by a scale factor of 1000, i.e., the strain displayed in the plot is 1000 times of the true strain so that the deformation of diode (GaN) and substrate (single-crystalline Al_2O_3) appear more explicitly. The meshing profile of the mesa-etched diode structure consisting of free triangles with varying density is shown in Fig. 3.5. The interfaces and surfaces have much denser population of meshing nodes so that the accuracy of stress evaluation is enhanced.



(a)



(b)

Figure 3.4 The model of the GaN stripe diode on the sapphire (single-crystalline Al_2O_3) substrate (inset shows the drift layer having step-graded doping buffer layers); (b) The deformation and 3D simulated stress distribution in the structure (deformation scale factor of 1000).

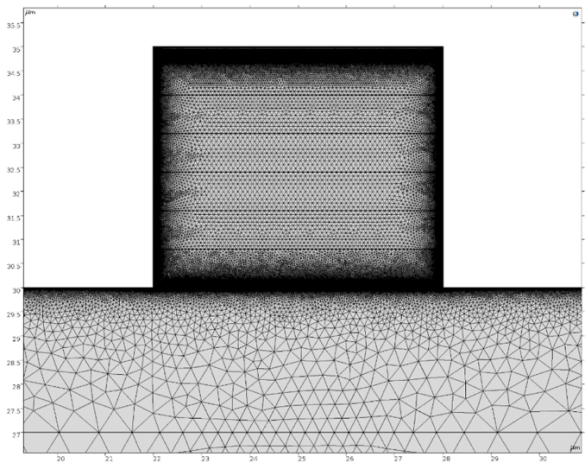


Figure 3.5 The meshing profile of the enlarged diode structure where interfaces and surfaces are densely meshed.

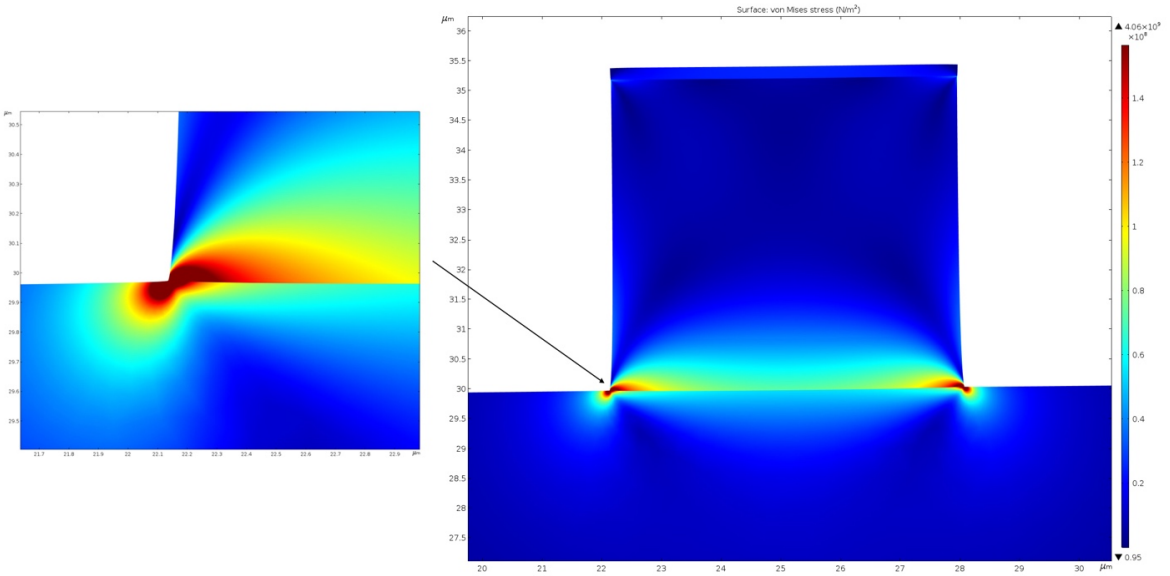


Figure 3.6 The plot of stress distribution in the designed p-n diode without step-graded doping buffer layers (left figure shows the zoom-in image of the peak stress occurring at the mesa edge corners).

The x-z plane view of stress distribution plots without and with step-graded doping buffer layer are shown in Fig. 3.6 and Fig. 3.7, respectively. The scale range in both plots is set to be equal so that the difference in stress distribution can be compared conveniently. As seen in both

cases, the stress peaks at the mesa edge corners. The peak stress is evaluated to be 4.06 GPa (without step-graded doping structure) and 1.08 GPa (with step-graded doping structure), respectively.

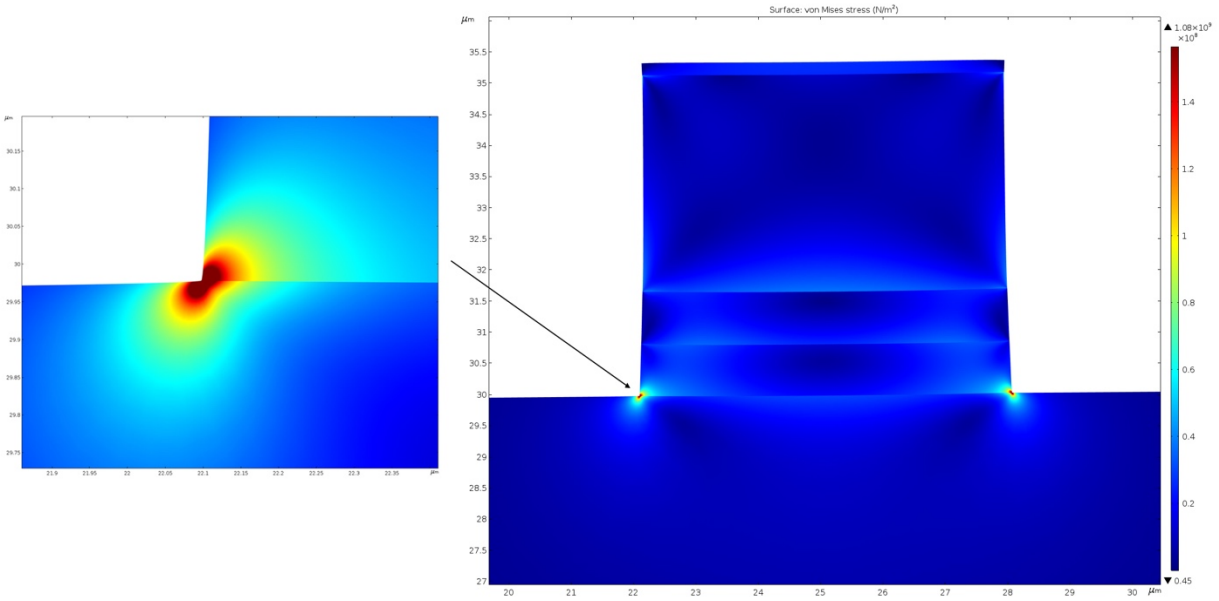


Figure 3.7 The plot of stress distribution in the designed p-n diode with step-graded doping buffer layers (left inset shows the zoom-in image of the peak stress occurring at the mesa edge corners).

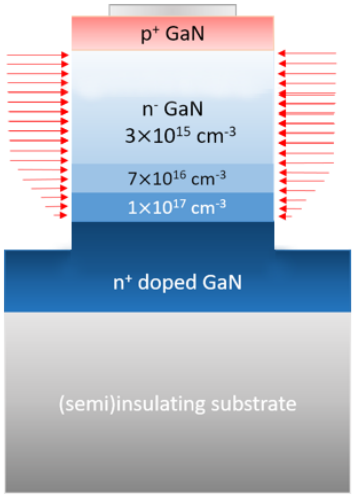


Figure 3.8 The schematic illustration of CPE induced stress by having 1-μm-thick n^+ layer being mesa etched.

As seen in Fig. 3.8, the structure is deeply etched into the heavily doped n^+ layer. By deep-mesa etching, the n^-/n^+ interface can be placed further away from the mesa edge corner. Figure 3.9 shows the simulated result based on the structure in Fig. 3.8. The peak stress occurring at the mesa edge corner further decreases to 0.573 GPa.

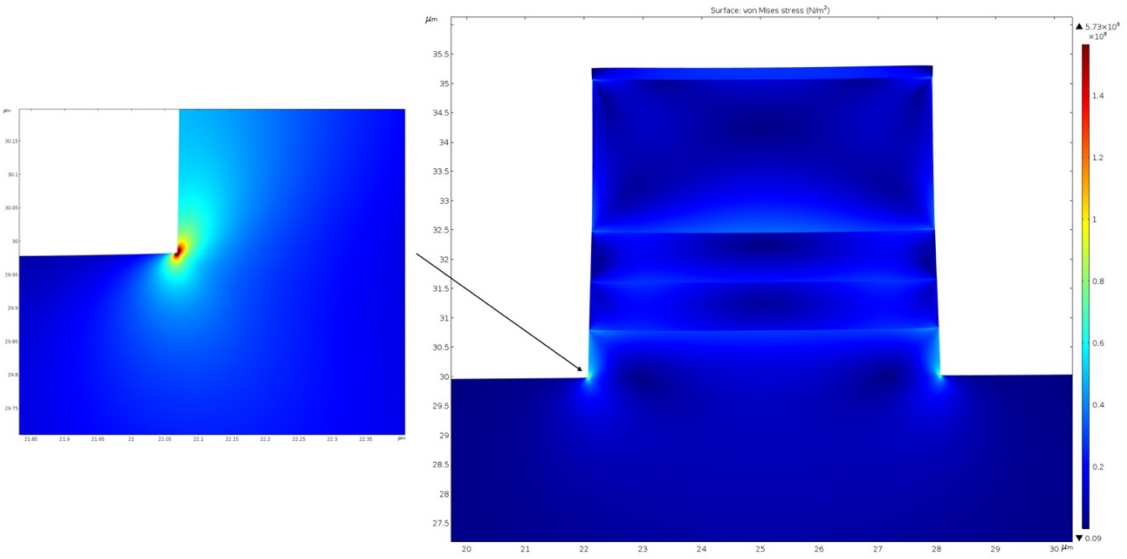


Figure 3.9 The plot of reduced stress distribution in the designed p-n diode with step-graded doping buffer layers and deep mesa etching (left inset shows the zoom-in image of the peak stress occurring at the mesa edge corners).

To conclude this subsection, the COMSOL simulated results show the CPE induced stress in the deeply punched-through drift layer can be relieved by the insertion of step-graded doping buffer layers and a deep mesa etching. In spite of the reduction in the CPE-induced stress, a total elimination of the CPE-induced stress should hinge on the elimination of the CPE itself. Similar to the non-polar GaN LED that fundamentally addresses the quantum confined stark effect (QCSE), a non-polar GaN power device has zero CPE which makes it an ideal solution. This can be readily achieved in the so-called true-lateral device structure, discussed in the subsequent subsection.

3.1.3 True-lateral Device Architecture

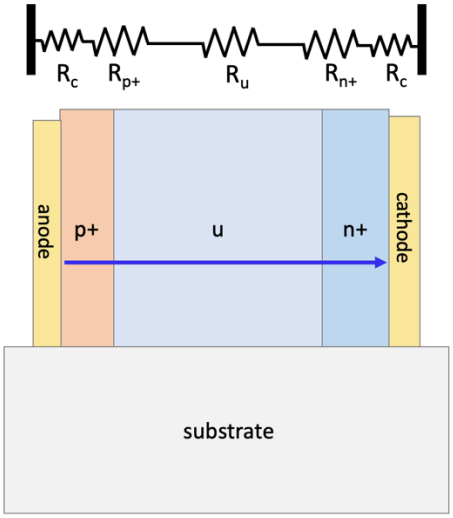


Figure 3.10 Schematic illustration of true-lateral diode architecture and equivalent resistance.

Based on the above-summarized shortcomings of both fully vertical and quasi-vertical p-n diode architectures, we proposed here an alternative type of diode architecture called fully-lateral or true-lateral (in order to distinguish from the conventionally lateral device). Fig. 3.10 is a schematic illustration of the basic device architecture and equivalent resistance. It appears like a 90°-rotated fully-vertical diode so that he current can flow straight from left to right. The fully-lateral architecture feature many advantages that are otherwise unattainable.

Firstly, as revealed in the preceding subsection, the device structure is immune to the CPE. As opposed to vertical structure where the drift layer is along (0001), the true-lateral structure has the drift layer on the non-polar plane (*a*-plane or *m*-plane), the applied E-field along non-polar direction will not induce strain (d_{11} and d_{22} in Eqn. (3.2) are zero). Therefore, the true-lateral p-n junction can intrinsically eliminate the CPE-induced stress and possible reliability issues.

Secondly, with the true-lateral architecture, free charge carriers are allowed to flow in a completely lateral direction between contacts from one sidewall to the other sidewall without the issue of current crowding typical in a quasi-vertical case.

Thirdly, compared to the true-vertical GaN case, the substrate resistance R_{sub} is absent when comparing the equivalent resistance. Therefore, the true-lateral architecture represents the minimum possible resistance to construct and operate the device.

Fourthly, the lateral *p-n* junctions can take special advantage of the epitaxial lateral overgrowth itself. In this case, devices are fabricated on the ELO-GaN islands prior to the coalescence stage which avoids the regeneration of high-defect region. In addition, the drift layer can overlap with low-dislocation-density wing region, allowing itself to withstand higher blocking voltage and approach the intrinsic breakdown strength of the material. It will be discussed to more details in the next section.

Fifthly, if applied in optoelectronic field, the true-lateral structure further helps to improve the external quantum efficiency (EQE). As it appears, the metal contact is switched to sidewall which used to be on top of the active layers, more emitted photons will be extracted from the top direction without being reabsorbed by metal contact. Furthermore, not only metal contact, but also semiconductor layer can reabsorb the emitted photons. For example, the p-GaN in AlGaN-based UV-LED reabsorbs the photons emitted from the AlGaN quantum wells [14]. With the p-GaN no longer being on the top, the light extraction efficiency will be significantly improved. By the same token, a photodetector based on GaN p-i-n junction will also benefit from the fully-lateral architecture leading to higher detection efficiency.

Aside from ECE, the internal quantum efficiency (IQE) may also be improved. Since CPE and direct piezoelectric effect (DPE) are reversible to each other, the immunity to DPE means the device structure will be free of the quantum-confined stark effect), an unwanted effect known to cause non-overlapping of wavefunctions of electrons and holes in the quantum well of a LED due

to the internal electric field induced by lattice mismatch stress [15]. Hence, the IQE of the optoelectronic device will be improved.

Finally, the true-lateral architecture allows for more design space of an optimal packaging in which the pad structure on the insulating substrate could enjoy more freedom in connection to the outer circuit and heat sink. In addition, various types of electronic devices can be invertedly transferred onto the same insulating substrate and easily connected by joining pads together. In this way, the insulating substrate can readily serve as a "breadboard" to support the entire circuit.

3.2 Device Fabrication of the True-Lateral Diodes

3.2.1 Process Flow

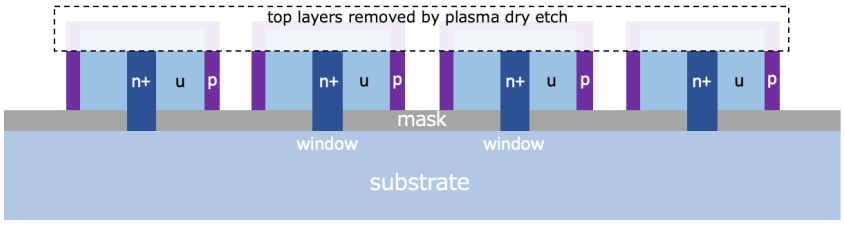


Figure 3.11 Dry etch used to remove the top layers of p-GaN and u-GaN. The removed part is delineated in the black dashed box.

Because the as-grown islands have half core-shell-doping structure, a set of device processing steps are needed to tailor it into the true-lateral device architecture. The removal of top p^+-and u-layers is necessary to obtain a desired lateral junction profile, as shown in Fig. 3.11. These redundant top layers can be removed by methods such as plasma etching. Inductive coupled plasma-reactive ion etching (ICP-RIE) is preferentially chosen to remove these top layers. The damages associated with dry etch is unavoidable, but fortunately the top surface after ICP etch proved to be smooth due to the superior chemical stability of (0001) GaN. Furthermore, in comparison, it is much better than the inevitable damages caused by mesa etch on the sidewall (as they are non-c-planes in most cases) of fully- and quasi-vertical diodes.

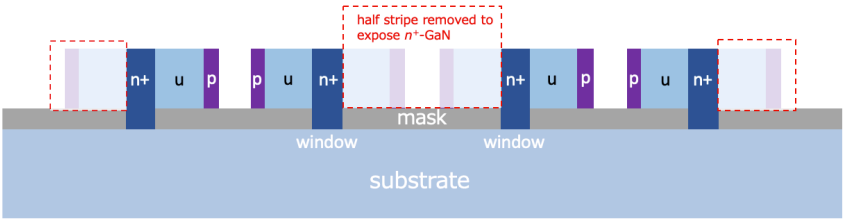


Figure 3.12 Second dry etching used to expose n^+-GaN. The removed part is delineated by the red dashed box.

After removal of top p^+-and u- layers, the island now has laterally symmetrical p-n-p junction profile, of which n^+-GaN is sandwiched in the middle. As such, a second dry etch is needed to expose the sandwiched n^+-GaN as new sidewall. As a result, almost half of the island is removed by selective area dry etching, illustrated in Fig. 3.12. Specifically, the etch is done in a way to produce back-to-back symmetry between neighboring islands. The dry etch-induced damages are on the non-polar plane this time which is less chemically stable than +*c*-plane, but fortunately again, since the newly-exposed sidewall is used for Ohmic contact to n^+-GaN, damages and surface roughness should in turn help reduce the contact resistance. After rapid thermal annealing to activate Mg in p-GaN, the islands with true-lateral doping structure are manufactured.

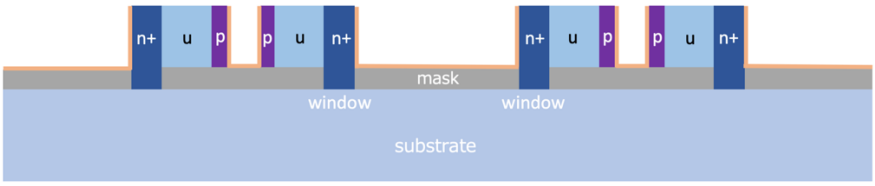


Figure 3.13 Metal contacts deposited onto island sidewalls and metal pads deposited onto the mask (salmon color).

Finally, metallization and post-metallization annealing (PMA) are needed to form Ohmic contacts. Special metallization process, i.e., depositing metals onto the straight vertical sidewalls of each GaN island, is required. The deposition methods can be physical vapor deposition (PVD)

such as electron beam evaporation (EBE) or sputtering, in rare cases the chemical vapor deposition (CVD) is also employed.

As an important detail, in order to ensure that metal layers could be fully and uniformly deposited onto the vertical sidewalls of island usually as high as a few micrometers, either the metal target in a sputtering chamber or the sample itself in an EBE chamber should be tilted enough (~45°) during the deposition process. As Fig. 3.14 depicts, sputtering is preferred over EBE to deposit metal on the vertical sidewall due to the tilted sputtering target and better surface coverage. On the other hand, in the EBE chamber, the possible solution is to place sample on a tilted home-made support. Since the support or sample holder cannot rotate, it needs twice deposition to make sure that metal is deposited on both sides of vertical sidewall, though the effect is still not good as sputtering.

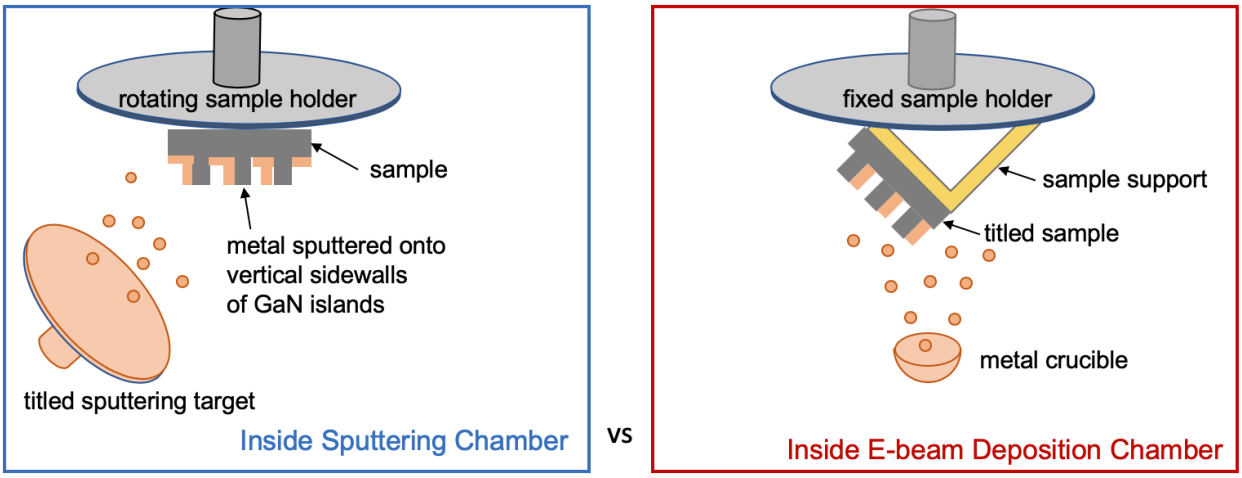


Figure 3.14 Schematic comparison of sputtering vs. e-beam evaporation in the effectiveness of sidewall coverage.

In comparison, the flat pad structure can be easily deposited onto the mask between GaN islands, adjoining the metal contact along the bottom edge of island sidewalls, though sometimes the weak adhesion between metal and dielectric mask often causes delamination of metal pad and special care should be given to it. After PMA to achieve Ohmic contact capability, the true-lateral

device is finally manufactured. Other non-essential processing steps such as passivation and edge termination will be discussed in the subsequent section.

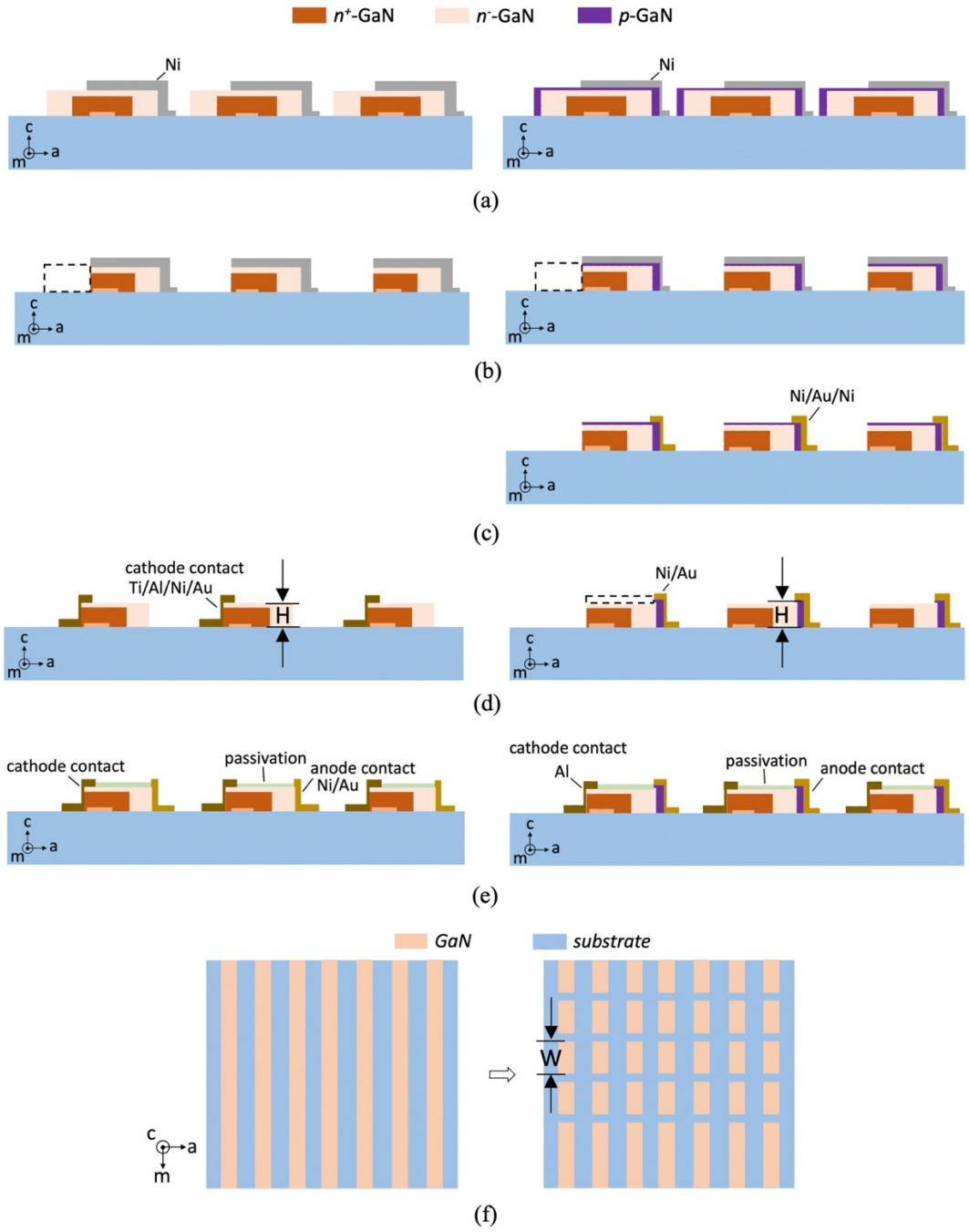


Figure 3.15 Cross-sectional schematic illustrations of the processing of non-polar true-lateral SBD (left column) and PND (right column).

Figure 3.15 schematically summarized the device processing flow implemented to fabricate SBD and PND characterized by the true-lateral p-n and metal-semiconductor junctions. As schematically depicted in Fig. 3.15 (a), after patterning of Ni hard mask to cover roughly half of the stripes, Cl_2-based ICP-RIE was utilized to tailor the shape of ultra-long stripe into shorter island arrays (Fig. 3.15(f)) and also to expose the *a*-plane n^+-GaN as a new sidewall of the island (Fig. 3.15(b)). In this step, the head-to-tail symmetry is achieved as alternative to head-to-head symmetry between neighboring islands in Fig. 3.13. Then, for SBD, Ti/Al/Ni/Au was deposited onto the n^+-GaN sidewall with rapid thermal annealing (RTA) to form the Ohmic contact while Ni/Au was deposited onto the opposed n^--GaN sidewall for the Schottky contact. For PND, Ni/Au/Ni was deposited onto the p-GaN sidewall of the island which serves a dual purpose. On one hand, its serves as hard mask to protect the underlying *a*-plane p-GaN during the second ICP-RIE process where the topmost c-plane p-GaN was removed. On the other hand, it also serves as the p-type Ohmic contact after RTA treatment (Fig. 3.15 (d, right)). It is fortunate that the possible plasma damages caused to the topmost c-plane of the island is less of an issue compared to the otherwise necessary mesa etch where other crystallographic planes of GaN are subject to plasma damages, thanks to the superior chemical stability of +*c*-plane GaN amongst all the crystallographic planes [16]. Afterwards, Al was sputtered onto the n^+-GaN sidewall to form the Ohmic contact. Passivation was achieved by deposition of polyimide and curing process. Figure 3.15(f) shows the plan-view schematic illustration of Fig. 3.15(b) where the ultra-long GaN stripes (left) are tailored into shorter GaN island arrays (right).

Figures 3.16 (a) and (b) are angled-view SEM images of the fabricated PND arrays and the magnified-view of a single PND, respectively. The GaN island has a typical H of 5 μm along c-direction as well as designed W of 100 μm and 200 μm along m-direction (W and H are

schematically indicated in Fig. 3.15 (d) and (f), respectively). As it appears, the fabricated diode is characterized by the true-lateral p-n junction as well as metal contacts formed onto the opposed non-polar sidewalls of the island, making the architecture essentially like a true-vertical diode structure being rotated through a right angle.

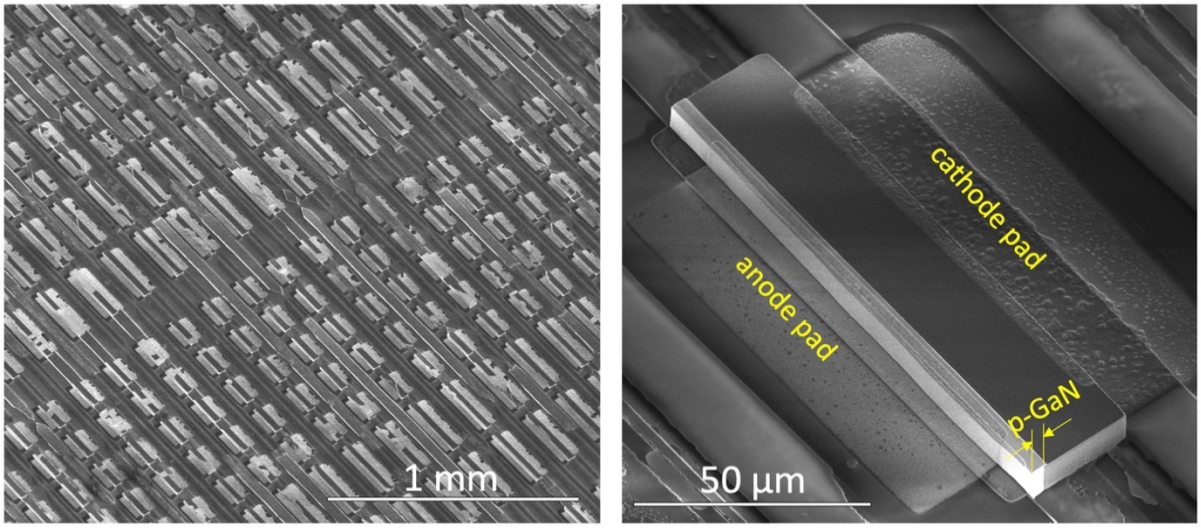


Figure 3.16 The angled-viewed SEM images of (a) the fabricated PND arrays and (b) the magnified view of a single PND.

3.2.2 Edge Termination

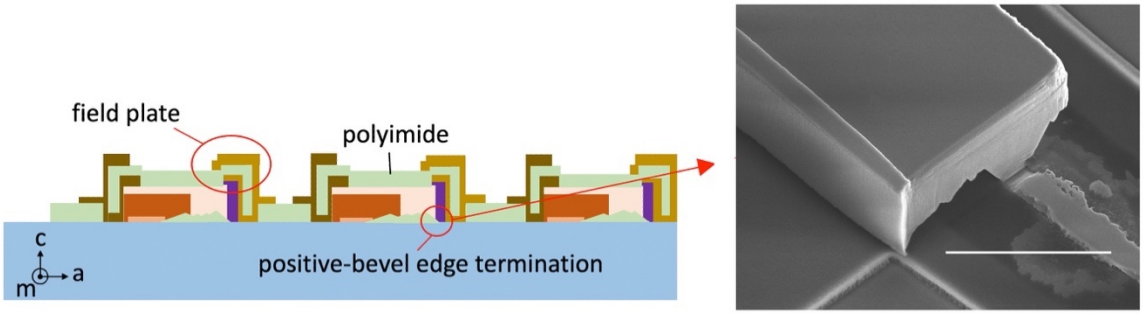


Figure 3.17 (left) The schematic illustration of the field plate and positive-bevel edge termination and (right) the angled-view SEM image of the GaN island where the positive beveled p-n junction as depicted in (left) was created at the -c-plane bottom surface (N-polar) of the island after a 25%

TMAH solution wet etch probably due to more stable N-polar p-GaN than n^--GaN. The scale bar in (right) is 10 μm.

As schematically shown in Fig. 3.17 (left), in order to reduce leakage current and increase breakdown voltage, aside from the passivation by polyimide, field plate and positive beveled p-n junction (a positive bevel angle is defined as one where more material is removed from the edge when progressing from the heavily-doped side to the lightly-doped side of the p-n junction and thus it is preferable for the termination of the single high-voltage junction with high-voltage power rectifiers) [11] were utilized as edge termination schemes to mitigate the electric field crowding and expand the depletion region at the surface. The field plate is wrapping around the three outer surfaces of island (i.e., top +*c*-plane and two opposed m-plane sidewalls). In particular, the positive beveled p-n junction was created at the bottom -c-plane surface (N-polar) of the island after a 25% tetramethylammonium hydroxide (TMAH) solution wet etch probably because of more stable N-polar p-GaN against TMAH etch than adjacent N-polar n^--GaN, as is indicated by the SEM image in Fig. 3.17 (right).

3.3 Device Characterization

3.3.1 TLM Measurement

Transfer-length method (TLM) is a widely-used approach to extract electrical properties such as contact resistance as well as sheet resistance of metal-semiconductor junctions [17]. To apply this method to our sample, the modified TLM is designed and carried out. The cross-sectional view (Fig. 3.18) shows an array of contact pads on the n-GaN and p-GaN indicated by the yellowish-brown and salmon-color, respectively. Five contact pads with different spacings, denoted by L_1, L_2, L_3 and L_4, are presented in the bird's eye-view in Fig. 3.18. In this case, the lateral width of the electrode pad is actually irrelevant in this modified TLM test. Instead, it is the height of adjoining

two diodes, i.e., W, that serves as the defined "width" in the TLM test. This width is needed to calculate the sheet resistance R_{sh} of p-GaN between adjoining contacts according to $\frac{\Delta R}{\Delta L} = \frac{R_{sh}}{W}$ (3.5), which can further extrapolate the concentration and mobility of holes in p-GaN. The transfer length L_T represents the distance beyond which nearly all the charge carrier flows into the electrode. It is half the absolute value of x-intercept. Once L_T is determined, contact resistivity ρ_C is also extrapolated by: $\rho_C = L_T^2 R_{sh}$ (3.6).

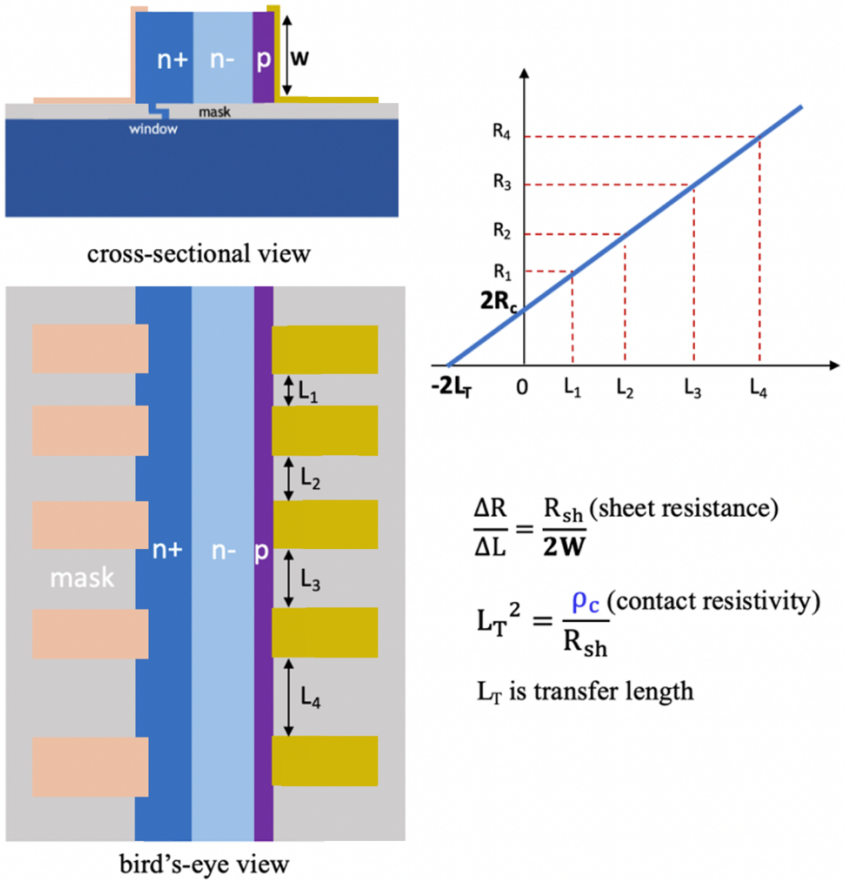
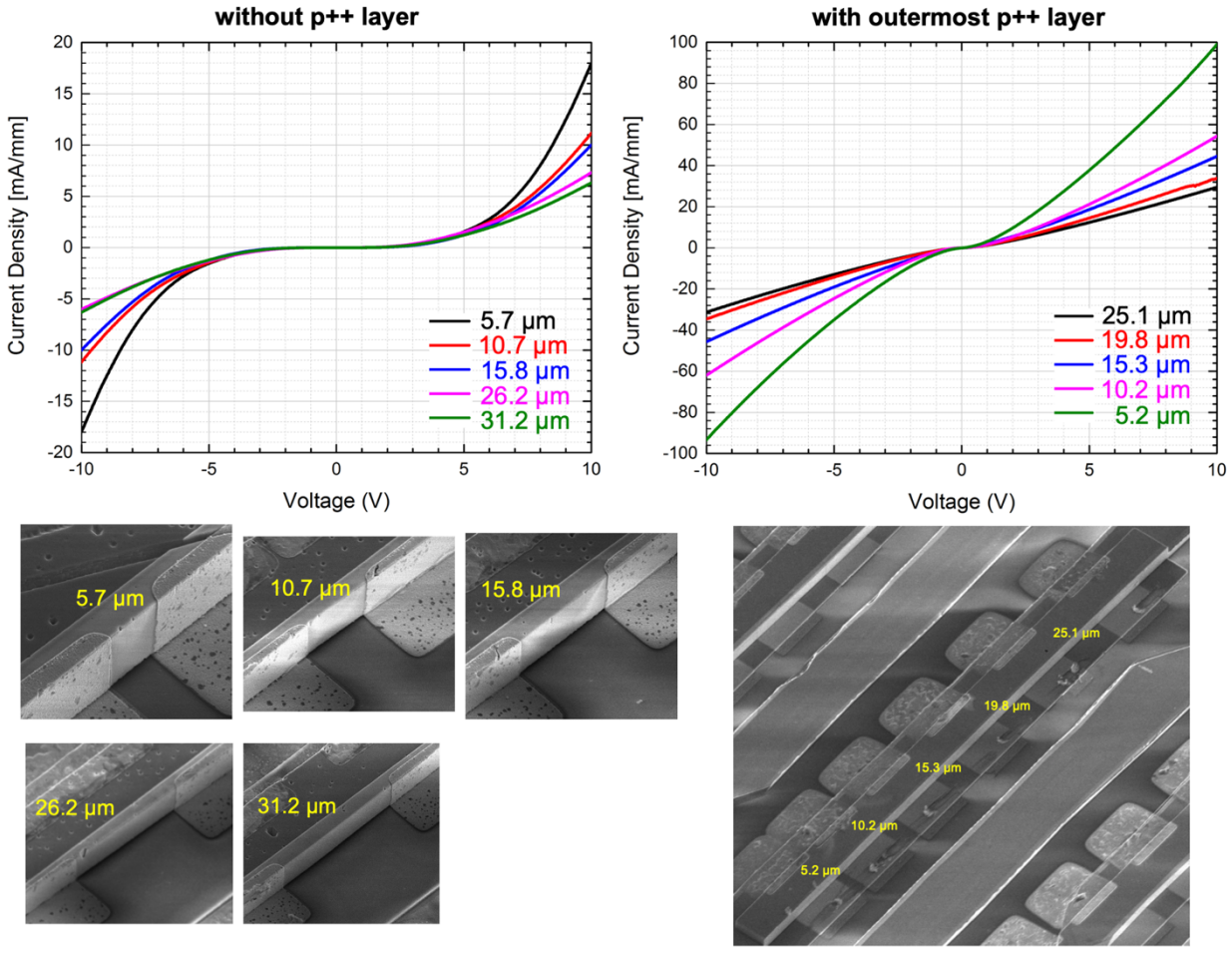


Figure 3.18 Schematic illustrations of modified TLM measurement setup and pattern design.

Fig. 3.19 presents the angled-view SEM images of the TLM test structure and the *I-V* characteristic curves of the TLM test structure from -10 V to 10 V. It can be seen that the outermost p^{++}-GaN contact layer helps improve the Ohmic contact to p-GaN. As plotted in Fig. 2.27, the

extracted differential resistance at different spacings are well aligned on a straight line, indicating that the value of sheet resistance is stable, suggesting that the thickness and doping concentration of p-GaN is uniform. The TLM measurement results for Ohmic contact to p-GaN and n^+-GaN are presented in Fig. 3.20 and Fig. 3.21, respectively. The specific contact resistivity values are comparable to the values of Ohmic contact to +*c*-plane GaN in the literature [18], suggesting that the sidewall contact to non-polar GaN in the true-lateral device architecture is a plausible scheme.



(a) (b)

Figure 3.19 Angled-view SEM images of the TLM test structure for the true-lateral device architecture. The upper images show the superimposed I-V curves of TLM measurements for the Ohmic contact to p-GaN side under different contact spacings.

x-intercept: 4.45 [um]

slope $= \frac{\Delta R}{\Delta d} = \frac{R_{sh}}{W}$ = 2999.9 Ω/ um

W=4.03 um
(measured with angled-view SEM image)

Sheet Resistance:

R_{sh}=12.09 kΩ/□ (or kΩ/sqr)

Transfer Length:

L_T=2.02 um

Specific Contact Resistivity:

$\rho_c = L_T^2 R_{sh}$=4.9×10^{-4} Ω.cm^2

Bulk Resistivity:

$\rho_{sh} = R_{sh} * t$= 12.09kΩ×1.11 μm×10^{-4}cm/μm =1.34 Ω.cm

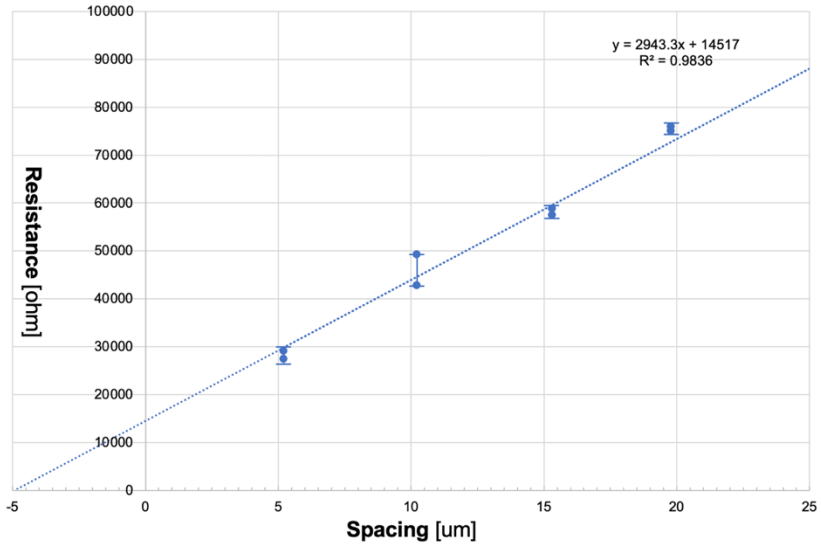


Figure 3.20 The TLM measurement results for Ohmic contact to p-GaN side (with p^{++} contact layer), extracted at ±5V.

x-intercept: 11.4 [um]

slope $= \frac{\Delta R}{\Delta d} = \frac{R_{sh}}{W}$=2.90 Ω/ um

W=4.9+5.1=10.0 um
(measured with angled-view SEM image)

$R_{sh} = \frac{\Delta R}{\Delta t}$. W= 2.90 Ω/μm*10.0μm = 29.0 Ω/□

Sheet Resistance:

R_{sh}=29 Ω/□ (or kΩ/sqr)

Transfer Length:

L_T=5.7 um

Contact Resistivity:

$\rho_c = L_T^2 R_{sh}$=9.4×10^{-6} Ω.cm^2

Bulk Resistivity:

$\rho_{sh} = R_{sh} * t$= 29.0Ω×12 μm×10^{-4}cm/μm =0.035 Ω.cm

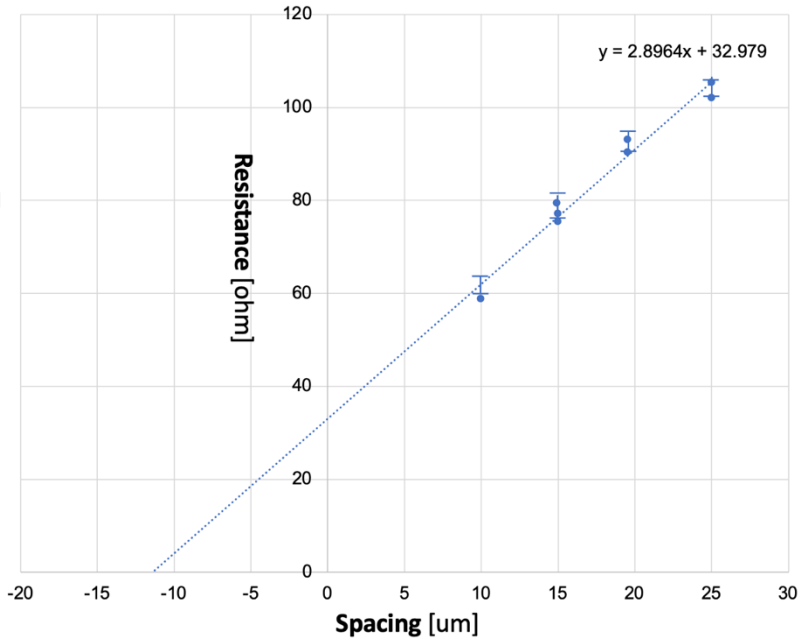


Figure 3.21 The TLM measurement results for Ohmic contact to n^+-GaN side.

3.3.2 Capacitance Profiling Measurement

Similar to the TLM test structure, the C-V measurement setup tailored for the true-lateral diode is depicted in Fig. 3.22.

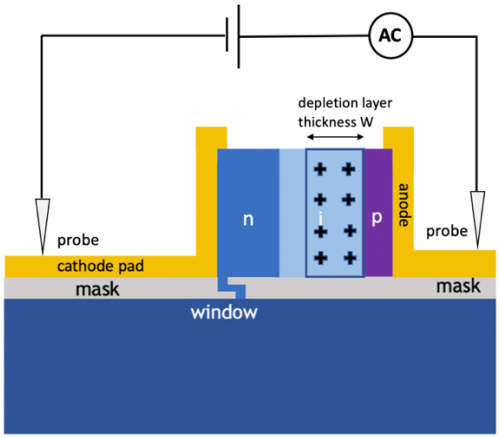


Figure 3.22 The modified setup for capacitance-voltage profiling in the fully lateral PND.

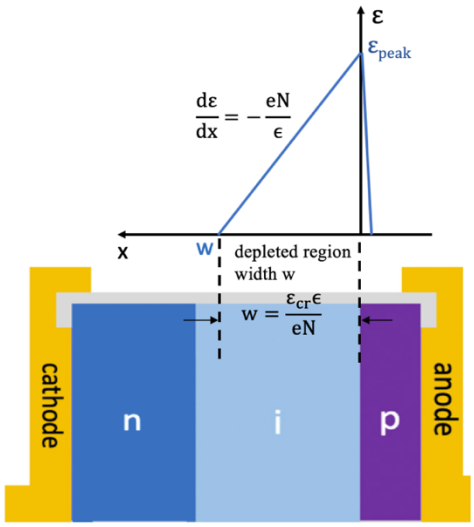


Figure 3.23 The variation of E-field versus depletion region depth in the fully-lateral PND.

As illustrated in Fig. 3.23, the parallel-plate capacitance model works well on the fully-lateral device geometry. Using one-sided junction approximation which is the basis for C-V profiling of diode, it is considered that all the net charges lie in the depletion region of the lightly-doped side, so that [19]:

$$Q_s = qA \int_0^W N_D^+ \, dx \tag{3.7}$$

where A is the cross-sectional area of the diode, to differentiate Q_s by V, we have:

$$C = \frac{dQ_s}{dV} = qA\frac{d}{dV}\int_0^W N_D dx = qAN_A(W)\frac{dW}{dV} \tag{3.8}$$

since $$C = \frac{\epsilon_0 \epsilon_r A}{W} \tag{3.9}$$

by equating the two equations, we have

$$N_D(W) = \frac{C^3}{\frac{q\epsilon_0\epsilon_r A^2 dC}{dV}} = \frac{2}{q\epsilon_0\epsilon_r A^2 \frac{d(\frac{1}{C^2})}{dV}} \tag{3.10}$$

where $W = \frac{\epsilon_0 \epsilon_r A}{C}$

The C-V profiling was measured with Agilent B1505A Power Device Analyzer. Fig. 3.24 (left) is the plot of C-V from 0 to 200 V and Fig. 3.24 (right) is an extrapolated plot of $1/C^2$ versus V based on Fig. 3.24 (left).

The relationship between $|N_D\text{-}N_A|$ versus W(depth) is then plotted according to the above equations as shown in Fig. 3.25. The average net doping concentration of n^--GaN layer is 6×10^{16} cm^{-3}.

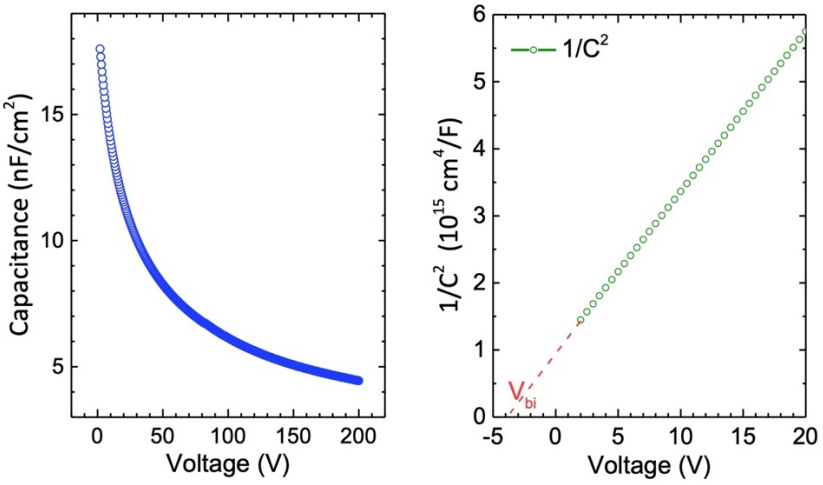


Figure 3.24 (left) C-V characteristics and (right) $1/C^2$ vs. V plot of the a-plane GaN PND.

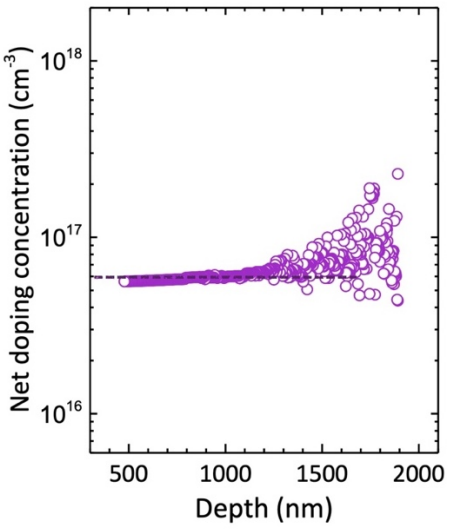


Figure 3.25 Net doping concentration versus depletion depth of the GaN PND.

3.3.3 Forward *I-V* Characteristics

The electrical performances of the *a*-plane GaN SBD on Si and sapphire and the *a*-plane GaN PND on sapphire is measured by Agilent B1505A Power Device Analyzer, respectively. In order to calculate current density, the device area was regarded as the total a-plane cross-sectional area (i.e., W× H where W and H are previously mentioned) of the island based on the structure and nature of the *a*-plane true-lateral diodes.

Before *I-V* measurements, the possible influence of the inserted n^+-AlGaN to the forward *I-V* characteristics should be discussed. The AlGaN underlayer consists of two sublayers: I-10nm $Al_{0.2}Ga_{0.8}N$ with ([Si]=5×10^{19} cm^{-3}) and II-5nm $Al_{0.2}Ga_{0.8}N$ with ([Si]=1×10^{19} cm^{-3}), as shown in Fig. 3.26. The band diagram can be calculated by using TCAD Silvaco.

As shown in Fig. 3.26, the AlGaN barrier of 0.2 eV over 2.5–3 nm is easy for electrons to tunnel through whereas the conduction band offset between the quasi-neutral part of n^+-GaN and n^+-AlGaN is only 0.007 eV, which is even smaller than the built-in potential (0.1 eV) of the n^+-n^-

GaN homojunction in this structure. It can be concluded that the impact of n^+-AlGaN underlayer to the electron flow is negligible.

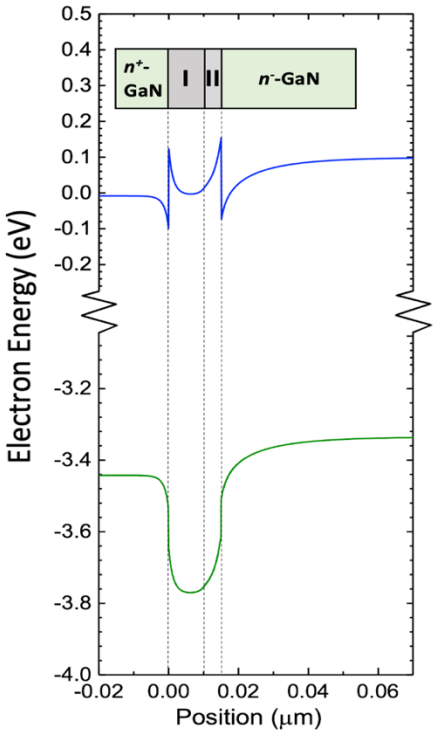


Figure 3.26 The band diagram of the employed n^+-GaN/n^+-$Al_{0.2}Ga_{0.8}N$/n^--GaN heterostructure simulated by TCAD Silvaco.

The forward *I-V* characteristics of the SBD on Si are shown in Figs. 3.27 (a) and (b). The ideality factor is extracted by measuring the $d\log(J)/dV$ of the semilogarithmic J-V plot using the following equation:

$$n = \frac{q}{kT}\frac{1}{d\log(J)/dV} \tag{3.11}$$

where q is the electron charge, k is the Boltzmann constant, T is temperature and J is the current density.

The ideality factor n remains at a plateau of 1.0 (from 1.00 to 1.05) spanning over 7 decades of current (i.e., from $<10^{-7}$ A/cm^2 to 1 A/cm^2), a low turn-on voltage of 0.59 V and a high on/off ratio of over 10^{10} are demonstrated, suggesting that the laterally overgrown n^--GaN has superior

material quality with low TDD due to the ELO process. In addition, the lowered Schottky barrier height of non-polar GaN than that of +*c*-plane GaN also contributes to the observed low turn-on voltage [20], [21] The forward specific on-resistance is calculated to be 0.6 mΩ.cm^2 at 1 kA/cm^2. A further reduction in resistance is expected through device structure optimization, such as shortening the drift layer thickness according to the doping concentration.

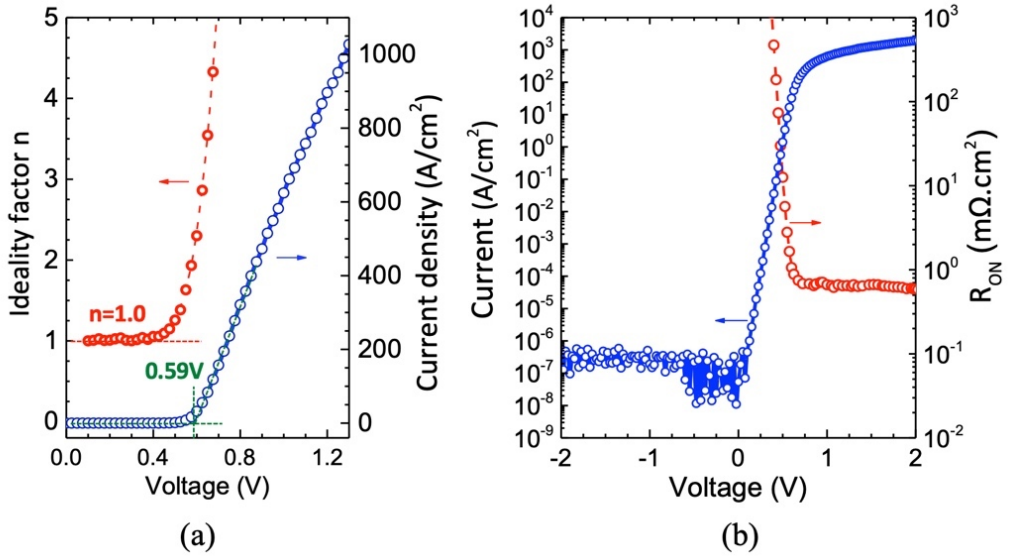


Figure 3.27 Forward I-V characteristics of the GaN SBD: (a) Linear scale showing a turn-on voltage of 0.59 V, the ideality factor n remains 1.0 from 0.10 to 0.42 V corresponding to 7 decades in current; (b) Current density and the specific on-resistance R_{ON} (plotted in semilogarithmic scale) versus forward bias V.

As mentioned previously, the ideality factor n of the SBD remains at a plateau of 1.0 (from 1.00 to 1.05) spanning over 7 decades of current (i.e., from <10^{-7} A/cm^2 to 1 A/cm^2). It is well fitted by Eqn. (3.12) so that the value of J_0 can be extracted to determine ϕ_B by Eqn. (3.13) and (3.14).

$$J = J_0\left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \tag{3.12}$$

$$\phi_B = kT\ln\left(\frac{A^*T^2}{J_0}\right) \tag{3.13}$$

$$A^* = \frac{4\pi e m_n k^2}{h^3} \tag{3.14}$$

Here k and h are the Boltzmann constant and the Plank constant, respectively. A^* is the effective Richardson constant. By using the electron effective mass of GaN $m_n = 0.23m_0$, as a result, A^* is calculated to be 28.9 A.cm^{-2}.K^{-2} [22].

As a result, the barrier height $\phi_B$of the SBD is estimated to be 0.58 eV by Eqn. (3.13) with J_0 =2.1×10^{-4} A.cm^{-2}. This value of ϕ_B is comparable to that reported on the *a*-plane n-type GaN in the literature and consistent with the finding that the Schottky barrier height of *a*-plane n-type GaN is lower than that of +*c*-plane counterpart by around 0.24-0.30 eV [21].

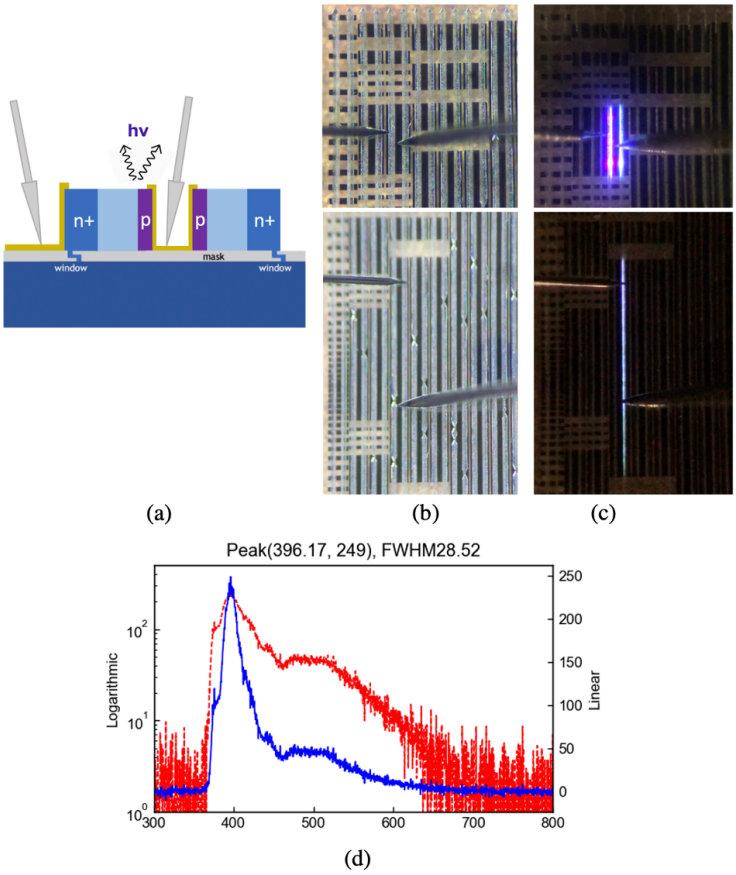


Figure 3.28 (a) *I-V* measurement setup. (b)(c) Microscopic images of the diodes of different lengths before and during the measurement in darkness. (d) The electroluminescence spectrum.

Fig. 3.28 (a) is a cross-sectional schematic illustration of the back-to-back diodes with true-lateral structure, where the two probe tips connected the anode pad and cathode pad, respectively. Fig. 3.28 (b) and (c) are plan-view optical microscopic images of the diodes before (b) and being tested (c), respectively. The diode in the upper-row images has a length of 500 μm and the diode in the lower-row images has a length of 2000 μm. The right images were taken during darkness and the bright violet light can be seen emitted from the p-n junction when the forward bias was applied to the diode. Fig. 3.28 (d) shows the electroluminescence spectrum of the emitted light where the main peak is centered at 396 nm, corresponding to the electron transition between conduction band to acceptor level.

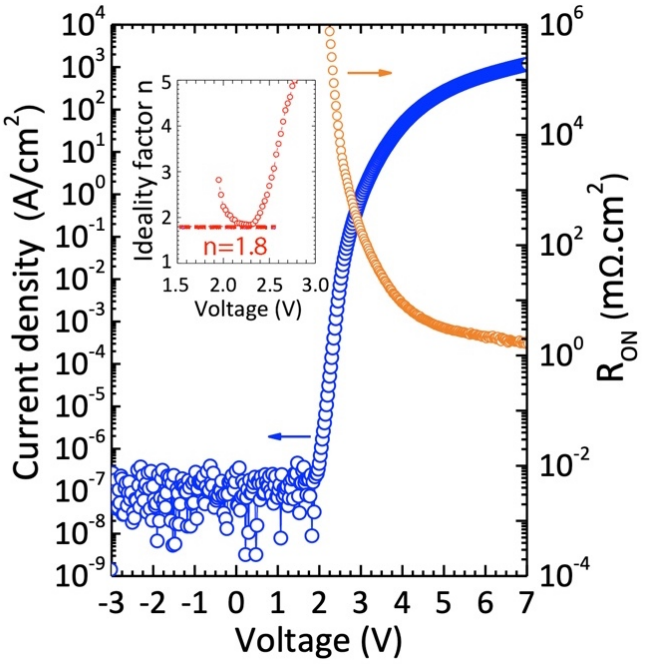


Figure 3.29 Forward *I-V* characteristics of the GaN PND with edge termination: Current density and specific on-resistance R_{on} versus forward bias V (both are plotted in semilogarithmic scale), the inset shows the ideality factor n plotted against V of 1.5-3.0 V.

Fig. 3.29 plots the forward *I-V* characteristics of the GaN PND on sapphire on a semi-logarithmic scale. The forward specific on-resistance is measured to be 1.6 mΩ.cm^2 at 1 kA/cm^2

and a high on/off ratio of 10^{10} is achieved. The lowest ideality factor (n =1.8) is in the lower range of the reported values for a GaN PND which are typically larger than 2 owing to the SRH (Shockley-Read-Hall) recombination and series resistance of p-GaN [23], [24].

3.3.4 Reverse *I-V* Characteristics

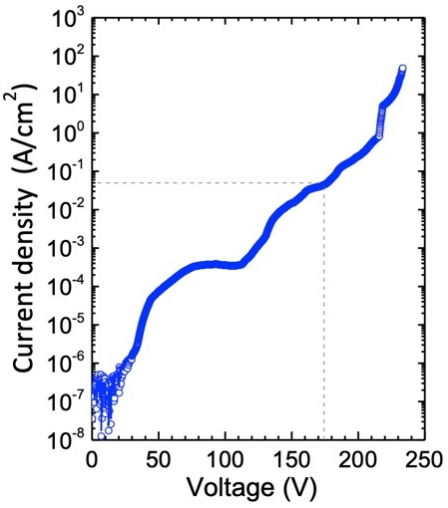


Figure 3.30 Reverse I-V characteristics showing a soft breakdown voltage of 175V occurring at 0.05 A/cm^2.

Figure 3.30 shows the reverse *I-V* characteristics of the SBD and a soft breakdown voltage of 175 V is achieved at leakage current density of 0.05 A/cm^2. The reverse leakage current could be suppressed to increase breakdown voltage with some proper edge termination designs in our future work. The forward and reverse I-V characteristics of the SBD on sapphire displayed similar performance.

For diodes with varied dimensions, 100 μm-long diodes are mainly fabricated in addition to the 200 μm-long diodes on the same sample. However, the long-dimension diodes did not perform as excellent as the short-dimension ones in the reverse blocking characteristics in which considerable leakage current was often observed. The cause is identified to be the prismatic stacking faults (PSFs) present in the stripes grown from the mask-patterned foreign substrates

which appear as the parallel straight black lines across the GaN stripes in the cathodoluminescent images discussed in the preceding Chapter. These observed PSFs are responsible for the enhanced leakage under the reverse bias.

Depending on the distribution of PSFs with average spacing of a few tens of micrometers and extending distance of ~50 μm along stripe, the probability of containing a few of them is very high in the long-dimension devices. In comparison, it is more likely to find some short-dimensional devices where PSFs are absent, in which case the excellent reverse blocking performances were demonstrated.

As longer-dimension device inherently has higher probability of containing a few stacking faults, further improvement in the growth of GaN stripes is needed to effectively suppress the formation of stacking faults and increase the yield of devices with excellent performance.

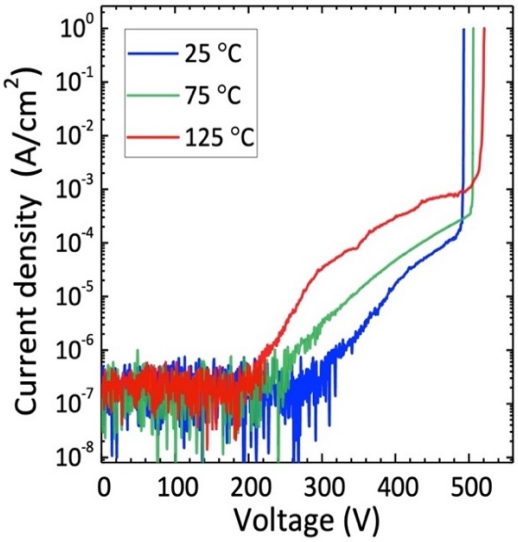


Figure 3.31 Reverse *I-V* characteristics under 25 °C, 75 °C and 125 °C, respectively, the breakdown voltage V_{br} increases from 490 V at 25 °C to 520 V at 125 °C, suggesting impact ionization-induced avalanche multiplication and breakdown.

Figures 3.31 show the champion result of the *I-V* characteristics of the *a*-plane GaN PND on sapphire under reverse bias. Leakage current was below the detection limit at room temperature for at least a reverse voltage of 300 V, and the highest breakdown voltage V_{BR} is measured to be 490 V on the best-performing PND with W=100 μm. The reverse *I-V* characteristics at 75 °C and 125 °C are also plotted in the same figure. Specifically, it is observed that V_{BR} displays a positive temperature dependence, characteristic of avalanche breakdown due to impact ionization multiplication. In addition to the good crystal quality, the high breakdown voltage and low leakage current were achieved in part owing to the aforementioned passivation and edge termination schemes consisting of field plate and the wet-etch induced positive beveled p-n junction.

3.4 Critical Electric Field

3.4.1 Impact Ionization Modeling

As previously explained, it is necessary to carry out a detailed study regarding the dependence of breakdown field on the doping concentration of drift region. Simply put, at high fields, a charge carrier-either an electron or a hole-obtains significant kinetic energy enabling itself to knock a valence electron into the conduction band and produces a pair of electron and hole. This process is called impact ionization. The new pair of electron and hole is again accelerated and then undergoes more collisions, eventually large numbers of electrons and hole pairs are generated, this avalanche-like phenomenon gives sharp rise to the reverse bias current and sets the upper limit to the maximum blocking voltage that a p-n junction could sustain. The peak field occurring at the metallurgical p-n junction during avalanche breakdown, is referred to as the critical E-field $\varepsilon_{\mathrm{crit}}$. Therefore, $\varepsilon_{\mathrm{crit}}$ for impact ionization is closely associated with the bandgap of the material, i.e., the wider bandgap, the higher field needed for impact ionization.

On the other hand, ε_{crit} can also be derived in principle as a function of $|N_d\text{-}N_a|$ based on the model of impact ionization which is described by the following basic integral equations [25]:

$$1-\frac{1}{M_n}=\int_0^{W_d}\alpha\exp\left[-\int_0^{x}(\alpha-\beta)dx'\right]dx \tag{3.15}$$

$$1-\frac{1}{M_p}=\int_0^{W_d}\beta\exp\left[\int_x^{W_d}(\alpha-\beta)dx'\right]dx \tag{3.16}$$

where α and β are the electron and hole impact ionization coefficients, they are defined as the number of electron-hole pairs generated by a carrier per unit distance traveled and they are functions of position and strongly dependent on the electric field which in turn is a function of position and net doping concentration [25]. W_d is the depletion width. M_n and M_p are the electron and hole multiplication factors. Avalanche breakdown occurs when M_n or M_p becomes infinitely large, leading to the integral for electrons or holes being 1.

At higher net doping concentration, the electric field decreases more rapidly along the drift region, and so the impact ionization coefficients α and β also decrease more rapidly, making the values of the definite integrals of $\int_0^{W_d}\alpha\exp\left[-\int_0^{x}(\alpha-\beta)dx'\right]dx$ and $\int_0^{W_d}\beta\exp\left[\int_x^{W_d}(\alpha-\beta)dx'\right]dx$ smaller. As a result, the peak electric field can reach a higher number to keep the same value of integral. That is the reason that higher net doping concentration allows for a higher critical E-field.

Various approaches have been attempted to extract the values of α and β either through experiments or FEA simulations. Specifically, we adopt the values of α and β calculated with Monte Carlo simulation by I. H. Oguzman et al. [26] as follows:

$$\alpha(E)=5.02\times 10^{8}\exp\left(-\frac{3.41\times10^{7}}{E}\right) \tag{3.17}$$

$$\beta(E)=6.80\times 10^{6}\exp\left(-\frac{1.87\times10^{7}}{E}\right) \tag{3.18}$$

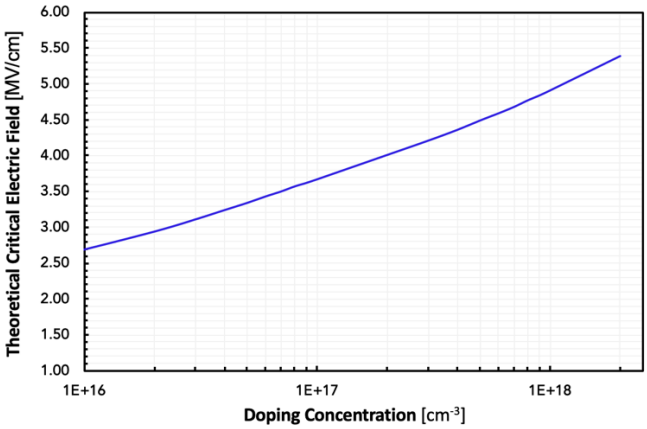


Figure 3.32 Calculated theoretical critical filed versus net doping concentration.

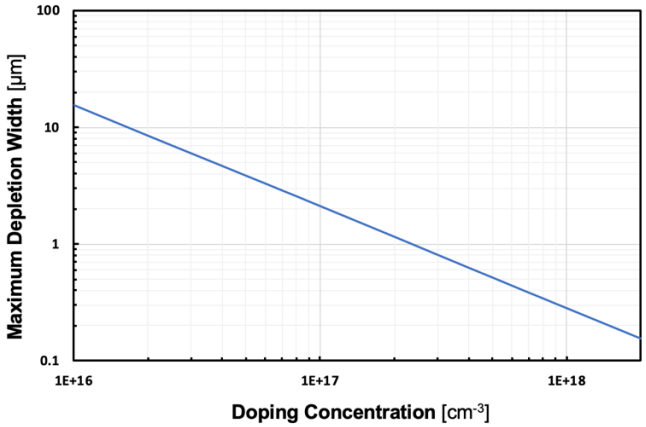


Figure 3.33 Calculated maximum possible depletion width versus net doping concentration.

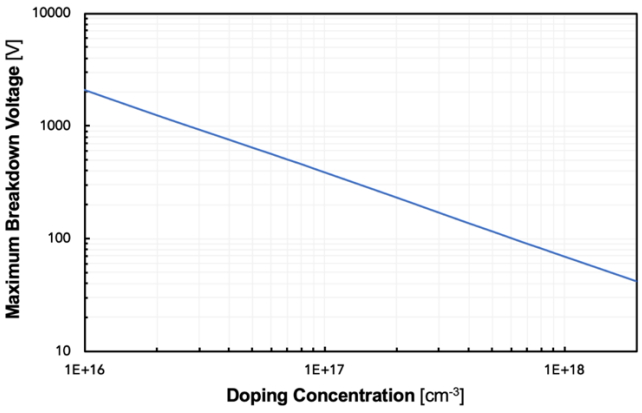


Figure 3.34 Calculated maximum possible breakdown voltage versus net doping concentration.

Since there exists no closed-form solution for the integral, we performed a finite-element analysis to investigate the dependence of critical field with varying net doping concentration. The subsequent plots are drawn based on the 1D-FEA modeling.

It can be seen from Fig. 3.32 that the critical field increases with net doping concentration from 2.7 MV/cm at 1×10^{16} cm^{-3} to 3.7 MV/cm at 1×10^{17} cm^{-3}. Fig. 3.33 shows how the maximum depletion width changes with the net doping concentration. The maximum depletion width sets the boundary between non-punch through (NPT) to punch through (PT) scenarios. When the n^--GaN width is larger than the maximum allowed depletion width, part of the n^--GaN region would never be depleted no matter how large the reverse blocking voltage is applied to. On the contrary, when the n^--GaN is shorter than the maximum allowed depletion width, the depletion width reaches the total thickness of n^--GaN beyond a certain reverse blocking voltage and afterwards it will not increase anymore upon further bias. Fig. 3.34 shows the maximum allowed breakdown voltage that could be achieved at each level of net doping concentration. It is based on the condition that the maximum allowed depletion width is satisfied (NPT state). However, in the case of PT state, the breakdown voltage must be smaller than the NPT state limit.

3.4.2 Critical Electric Field Benchmarking

As shown in the preceding section, the ideal ε_{crit} is not a fixed value. Instead, it is a function of both the net doping concentration and depletion region. Using the one-sided junction model for the p^+-n^- junction diode, critical electric field ε_{crit} at the planar junction interface over a breakdown voltage of V_{br} is then given by:

$$\varepsilon_{crit} = \sqrt{\frac{2e\,|N_d - N_a|\,V_{br}}{\epsilon_0 \epsilon_r}} \quad \text{(non-punch through)} \tag{3.19}$$

or

$$\varepsilon_{crit} = \frac{e|N_d - N_a|W}{2\epsilon_0\epsilon_r} + \frac{V_{br}}{W_d} \quad \text{(punch through)} \tag{3.20}$$

wherein $|N_d\text{-}N_a|$ is the net doping concentration in which N_d and N_a are donor and compensated acceptor concentration in the depletion region on the n^--doped side of the p-n junction. W_d is the depletion width. ϵ_0 is the vacuum permittivity and e is electron charge. The relative permittivity ϵ_r is regarded as 9.5 for $\epsilon_\perp$ and as 10.4 for $\epsilon_\parallel$ [27].

Since V_{BR} is obtained at 490 V at room temperature and $|N_d\text{-}N_a|$ is determined to be 6×10^{16} cm^{-3} as shown in Fig. 3.31, we can calculate the depletion width W_d at breakdown to be 3 μm, which is much shorter than the n^--GaN drift layer thickness of 8-10 μm in this PND, thus fitting into the non-punch through (NPT) scenario. Therefore, ε_{crit} is calculated to be 3.3 MV/cm (note that ϵ_r is 9.5 instead of 10.4 in an *a*-plane p-n junction), making it the record high value of ε_{crit} in GaN devices on foreign substrate. It is worth mentioning that the calculated ε_{crit} from Eq. (3.19) and (3.20) represents the lower-bound based on the parallel-plane (ideal) breakdown voltage model, given that the perfect planar junction could not be achieved, the actual ε_{crit} should have been even higher despite the effective effort to minimize the electric field crowding at the edges in this dissertation [28], [29].

In comparison, the results are benchmarked in the same plot with other values of ε_{crit} and $|N_d\text{-}N_a|$ in the literature [29]–[36]. It should be noted that all the values of ε_{crit} are subject to recalculation based on the varying values of $|N_d\text{-}N_a|$, V_{br} and drift layer width W_d (in the case of PT) reported in each reference and a common value of ϵ_r (9.5 for $\epsilon_\perp$ and 10.4 for $\epsilon_\parallel$). Furthermore, the simulated curve under NPT case in Fig. 3.35 could also well apply to the referenced works under PT case after taking full account of the moderate values of W_d and $|N_d\text{-}N_a|$ in each of these cases [30]–[35].

In addition, the simulated result of ε_{crit} v.s. $|N_d\text{-}N_a|$ assuming NPT case is replotted as the grey dashed line in Fig. 3.35, like that in Fig. 3.32. which could also be interpreted as the performance limit of unipolar power devices in GaN.[37] It can be seen that the critical field has a positive dependence on the net doping concentration, which is partially responsible for the high value of ε_{crit} found in our PND in which the drift layer has relatively high doping concentration.

Therefore, the closeness of each mark in Fig. 3.35 to the simulated GaN limit curve also serves as a good measure of device performance, by which our result on foreign substrate is shown to be comparable to the best results of GaN devices on GaN substrate.

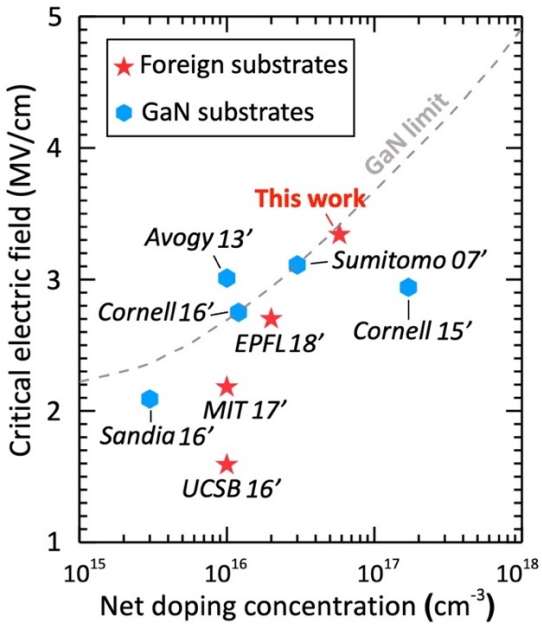


Figure 3.35 Benchmark of critical electric field ε_{crit} versus net doping concentration $|N_d\text{-}N_a|$, where the simulated curve is calculated based on the impact ionization model under NPT case [30]–[35].

3.5 Summary

In brief summary, a new type of diode architecture-fully-lateral GaN diode was proposed and demonstrated for the first time. Compared with quasi-vertical and fully-vertical diodes, the new diode

architecture has a few unrivaled advantages, including the immunity to converse piezoelectric effect-induced stress, minimum possible equivalent resistance, etc. Also, such architecture was capable of unleashing the true potential of ELO by utilizing the low TDD region grown by ELO as the drift layer of a power device and of circumventing the problematic coalescence process of ELO, which might otherwise be inappropriate for power electronics. As a result, power diodes featuring the true-lateral p-n and metal-semiconductor junctions were fabricated on the GaN islands grown on foreign substrates. They were realized based on a hybrid process of epitaxial lateral overgrowth with in situ doping followed by overcoming a set of challenges in the device processing stages. As a result, the good electrical performances were achieved on the fabricated SBD and PND, as were highlighted by the avalanche capability demonstrated in the GaN devices on foreign substrates. This may suggest that the non-polar true-lateral *p-n* junction is a potent building block for high power applications.

3.6 References

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Chapter 4

True-lateral Bipolar Transistors on ELO-GaN

4.1 Introduction

In this Chapter, the true-lateral device architecture featuring fully laterally aligned p-n junctions is employed in the domain of bipolar transistors. The true-lateral p-n junction serves as the building block. Bipolar transistors feature high current and high power handling capabilities than their unipolar FETs counterpart by virtue of the minority carrier injection across the entire p-n junction [1]. They have the intrinsic advantage of going beyond the limit of unipolar Baliga's figure of merit.

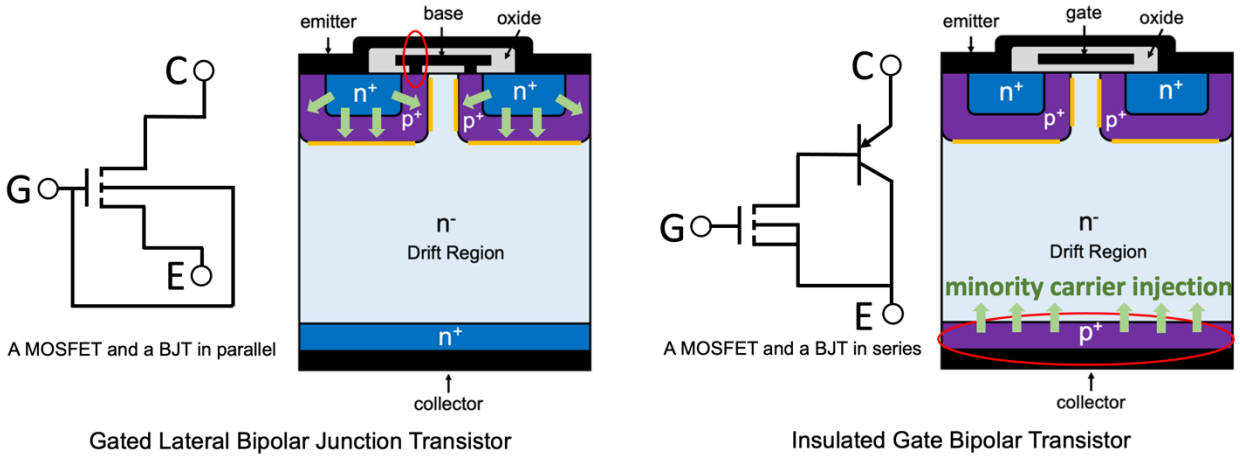

Figure 4.1 Schematic of the structure of a gated lateral bipolar junction transistor and an insulated gate bipolar transistor and their equivalent circuits, respectively.

For bipolar transistors, we invented a prototype gated lateral power bipolar junction transistor (GLP-BJT) and demonstrated a prototype Insulated Gate Bipolar Transistor (IGBT) on GaN by using epitaxial lateral overgrowth to produce the desired selective area doping profile. Before delving into the details of the device fabrication and electrical characterization, it is helpful to start

by introducing and comparing the two devices in general since relatively they are lesser-known than other devices such as a conventional BJT and a MOSFET, especially for a GL-BJT.

Figure 4.1 schematically compares the structure of GLP-BJT and IGBT with their equivalent circuits. Both are fundamentally the hybrid of MOSFET and BJT at the device level. In terms of equivalent circuit, the GLP-BJT on the left is a MOSFET and a BJT in parallel connection and the IGBT on the right is the two in series connection. Structure-wise, both devices resemble the structure of a planar-gate vertical power MOSFET with some modifications. The key distinguishing part in each device from a MOSFET endows themselves with bipolar nature, as is indicated by the red arrows. For a GLP-BJT, part of the metal gate is directly tied with the p-base; for an IGBT, the collector end features a p-n^- junction as opposed to a n^+-n^- junction. Owing to such structural features, during ON-state, minority carriers injection occurs across the p-n junctions indicated by the green arrows, leading to a high current density under high level injection. While during OFF state, the p-n^- junction indicated by the yellow line serves to withstand the reverse blocking voltage in each device. In terms of strength in each device, for GL-BJT, the advantage lies in a high current gain of I_C/I_B which leads to low on-state power dissipation and high-efficiency base drive circuit. For IGBT, it combines the simple gate-drive characteristics of MOSFETs with the high current handling capability of BJT [1]. The detailed discussions will be presented in the following sections.

4.2 Concept of Gated Lateral Power BJT

4.2.1 Tradeoff between Current Gain and Breakdown Voltage

For power BJTs, high current gain is one of the most desirable figures of merit especially under high current condition [2]–[6]. The reason that a BJT was not applied to power application is more specific to Si itself, as Si BJT suffers from the limited safe operating area (SOA) due to the notorious

second breakdown issue [7]. However, such second breakdown is free in wide bandgap material and as a result SiC-BJT emerges as a potent rival against Si IGBT and SiC MOSFET in the power switching market [8]. For switching application, the bottleneck for the SiC-BJT technology is the low current gain especially at high collector current levels which results in a high drive current I_B, high on-state power consumption ($I_B \times V_{BE}$), and high power dissipation in the base drive circuit. A high current gain (>200 [9]) can significantly reduce drive current I_B, therefore it is important for low on-state power dissipation and high-efficiency base drive circuit [10]–[12]. However, both 4H-SiC-based bipolar junction transistor (BJT) and GaN-based heterojunction bipolar transistor (HBT) suffer from a low current gain especially at high collector current levels [4], [8]. To make matters worse, conventional approaches to increase the current gain such as reducing the width and doping level of base region seriously compromise the voltage blocking capability, which accounts for the tradeoff between these two critical metrics of a power bipolar transistor [1], [13].

On the other hand, Gated Lateral BJT has been theoretically and experimentally studied in Si to exhibit high current gain of up to several thousand at low current levels due to the potential barrier modulation by the MOS gate structure over the base region of the lateral BJT [14]–[20]. However, the device was not configured for high power operation. It is thus expected that such a device with modified structure on wide bandgap semiconductor could combine the advantages of high current gain with good current handling and voltage blocking capabilities and hence make possible a Gated Lateral power (GLP) BJT.

4.2.2 Device Structure

The schematic illustrations of the GLP-BJT on GaN island are shown in Fig. 4.2. The island consists of fully lateral GaN n-p-n homojunctions, as seen in the Section A-A, and the p-base region is sandwiched between the n^--collector drift region to the left and the n^+-emitter region to

the right.

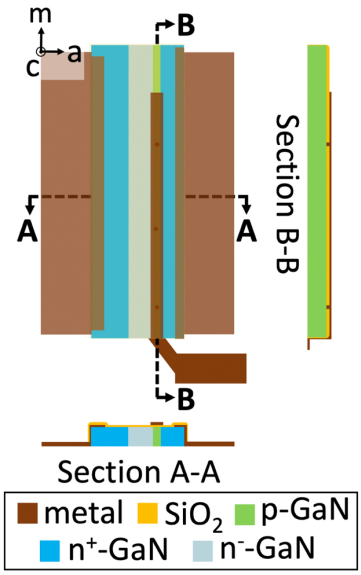

Figure 4.2 Schematic illustrations of device structure (the color of SiO_2 gate oxide is semi-transparent in the top-view illustration to make underlying materials discernable) [21].

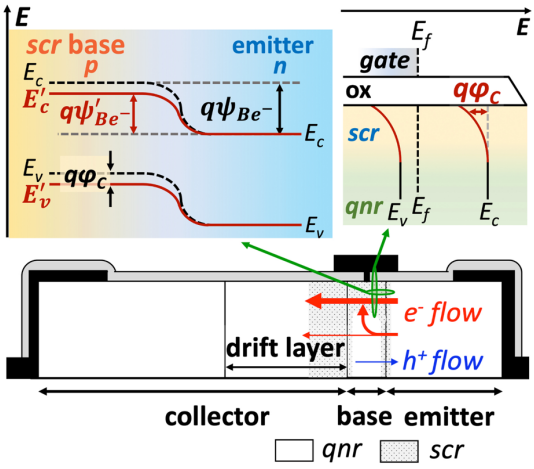

Figure 4.3 The band diagrams across the scr base-emitter junction and the MOS structure in the forward active mode of the device. The electron and hole current components are marked by red and blue arrows, respectively [21].

The device structure is essentially like a power MOSFET in which the gate and p-base region are internally tied. The base region underneath gate oxide is fully depleted changing otherwise

quasi-neutral base region (qnr-base) into space charge base region (scr-base), as depicted in the upper right band diagram in Fig. 4.3. The potential barriers seen by electrons (ψ_{Be^-}) and holes (ψ_{Bh^+}) between the emitter and qnr base under forward bias are dictated by Eqn. (4.1) and Eqn. (4.2), respectively:

$$\psi_{Be^-} = \varphi_{bi} - V_{be} \tag{4.1}$$

$$\psi_{Bh^+} = \varphi_{bi} - \frac{\Delta E_g}{q} - V_{be} \tag{4.2}$$

where φ_{bi} and V_{be} are built-in potential and applied forward bias across the emitter-base junction, respectively. ΔE_g is the narrowing of the bandgap between p-base and n^+-emitter. It is also known that V_{be} serves as the underlying driving force for the high current density in a BJT [13]. As depicted in the upper left band diagram in Fig. 4.3, the barrier for electrons (ψ'_{Be^-}) injected from the emitter into scr base is reduced by a potential of φ_c due to the gate-modulated band bending, as shown in Eqn. (4.3) [15]:

$$\psi'_{Be^-} = \varphi_{bi} - V_{be} - \varphi_c \tag{4.3}$$

As a result, electrons are injected from emitter to scr base more easily due to the reduced barrier, whereas few holes are injected from scr base into emitter. The modulation of potential barriers for electrons and holes to cross the emitter-scr base junction fundamentally increases the current gain in a GLP-BJT. It is worth mentioning that compared to a Si Gated Lateral BJT [14], the fully-lateral n-p-n structure depicted in Fig. 4.3 greatly enlarges the injection area of electrons and eliminates the parasitic vertical BJT, leading to a further increased current gain.

The separation between electrons and holes due to the scr-p base and the resulting effective suppression of recombination is one of key reasons for the high current gain. The scr-p base under the gate oxide provides preferential pathway for electron injection due to the reduced injection barrier, in much the same way as the sub-threshold current in a MOSFET. However, this preferential

pathway is inherently different than "the inversion channel" of a MOSFET under deep depletion mode.

To better compare the difference among conventional lateral BJT, Gated-Lateral BJT and MOSFET, the band diagrams and the associated distribution of electron density are shown in Fig. 4.4. It can be seen that compared to MOSFET, since the p-base and metal are internally tied in a GL-BJT, the Fermi level in the scr p-base underneath the gate oxide is constantly equal to that of gate regardless of the applied bias, as a result, the surface bending at the interface Φ_C is fixed, as opposed to the inversion mode of MOSFET in which the surface potential Φ_s can increase to $2\Phi_B$ (Φ_B is bulk potential) and the Fermi level of p-body and that of the gate varies by $q(V_g-V_b)$. Compared to a conventional BJT, the driving force for electron injection from emitter into scr base is a combination of V_{BE} and Φ_C, whereas the driving force for electron injection from emitter into qnr base is only V_{BE}.

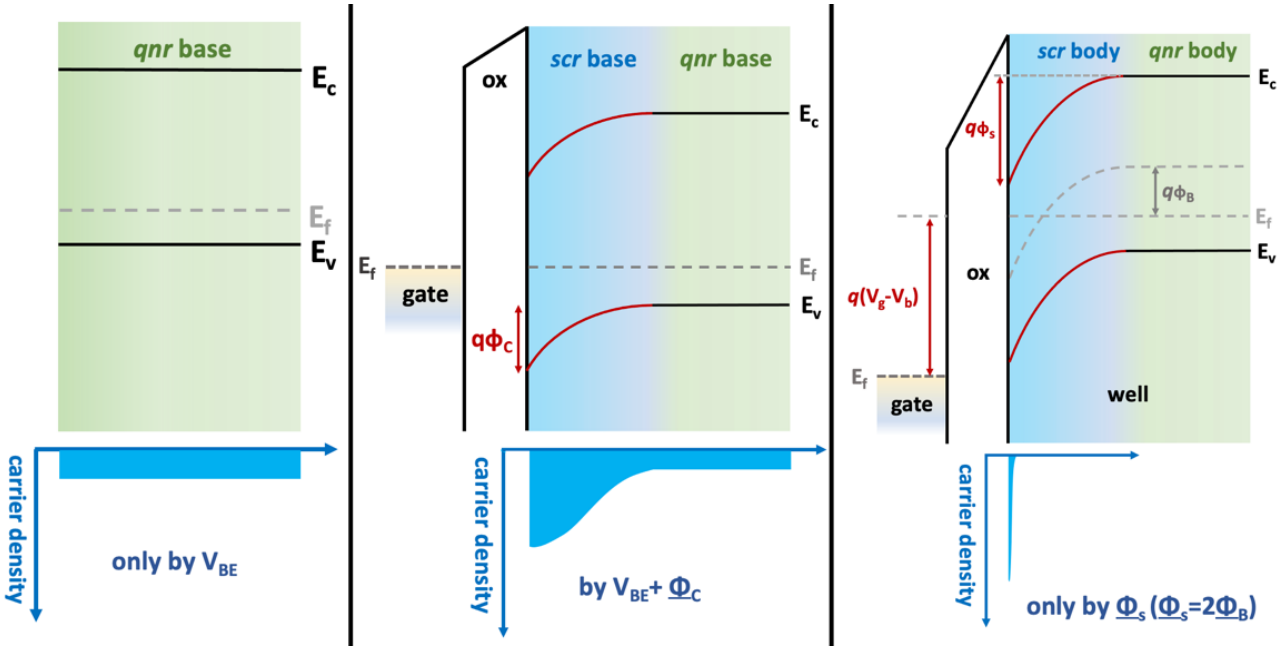

Figure 4.4 The band diagrams and the associated distribution of electron density among conventional lateral BJT, Gated-Lateral BJT and MOSFET.

4.2.3 Device Simulation

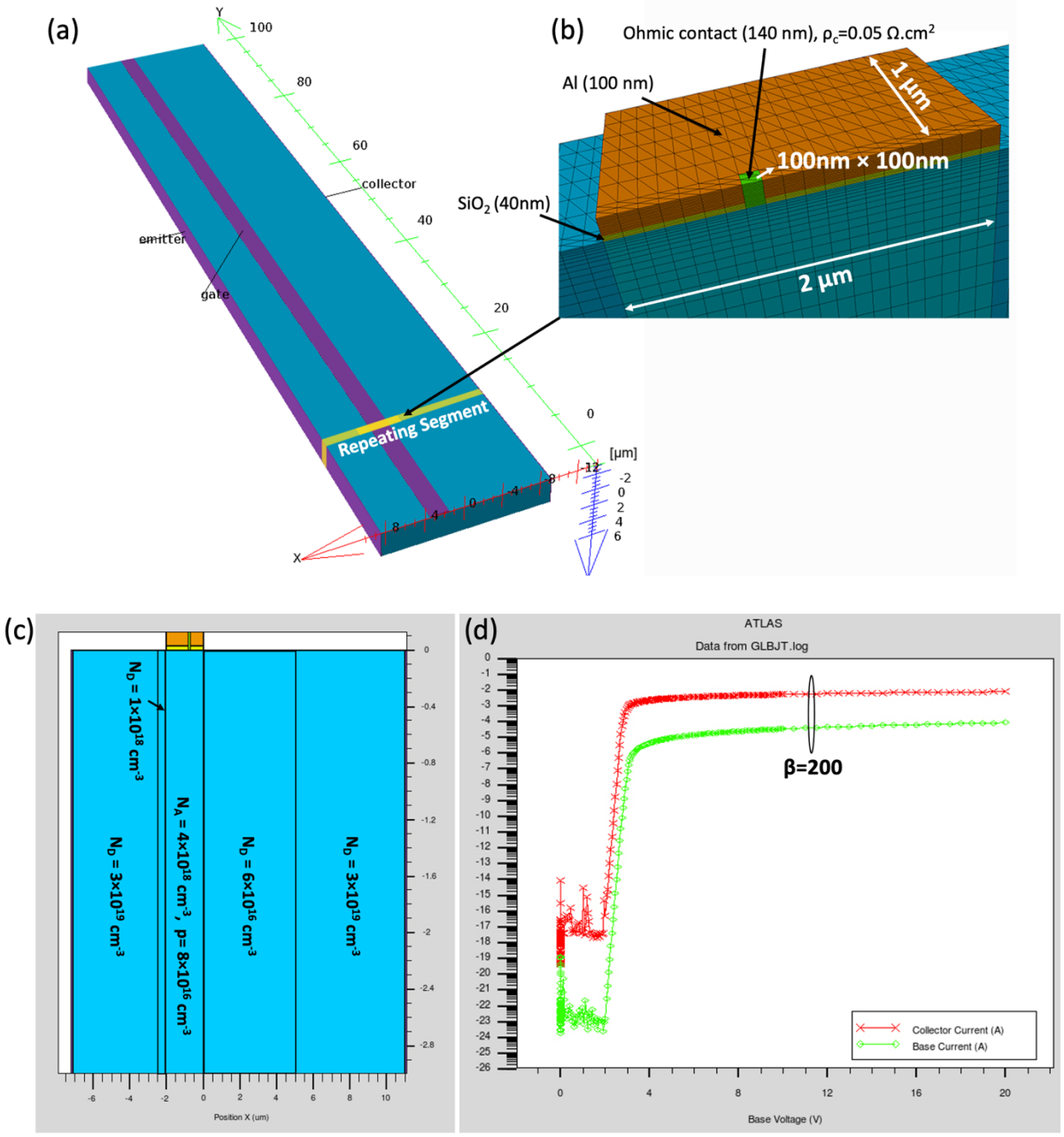

Figure 4.5 TCAD Silvaco simulation results regarding the GLP-BJT on GaN: (a)The simulated 3D structure of the GaN GL-BJT. (b) Zoomed-in view showing detailed information of the gate structure of one repeating segment of the simulated structure. (c) X-Z plane cross-sectional of the simulated structure. (d) The simulated Gummel plot of the device.

In order to qualitatively evaluate the theoretical current gain of the Gated Lateral BJT in GaN, TCAD simulation by Silvaco ATLAS is carried out.

In the simulated structure shown in Fig. 4.5, all the parameters, such as device dimensions and doping concentrations, resemble as much as possible the experimental structure: the p-base region has a width of 2 um, the hole concentration of 8×10^{16} cm^{-3}, and the Ohmic contact (plotted as green area in Fig. 4.5 (b)) has contact resistance of 0.05 $\Omega.cm^2$. To facilitate the calculation, the structure consists of 100 repeating segments along Y-direction (as shown in Fig. 4.5(a)). For each segment, the gate metal (defined in orange color) has area of 2 um (X-direction) × 1 um (Y-direction) and the Ohmic contact (green area) has area of 100 nm (X-direction) × 100 nm (Y-direction) (Fig. 4.5(b)). Other details of the device dimension and doping concentration can be found in Fig. 4.5(c).

It can be seen from the simulated Gummel plot in Fig. 4.5 (d) that a high current gain of ~200 can be achieved from the simulated GaN device. In addition, the current gain can be further enhanced by slightly reducing the p-base region width and the area ratio of Ohmic contact (ratio of green to brown region). In contrast, if the MOS gate structure (brown and yellow) is relaced entirely by the Ohmic contact to p-base region (green) (Fig. 4.5 (b)) as is the case of the lateral BJT, the simulated current gain is less than 5 at the same current level.

Finally, the difference of electron concentration distribution among MOSFET, GLP-BJT and conventional lateral BJT is illustrated by TCAD simulation as shown in Fig. 4.6. Unlike conventional BJT, the scr base underneath the oxide provides preferential pathway for electron injection which leads to different electron distribution in p-base region of the GL-BJT. Compared with the unipolar MOSFET, minority carrier injection occurs throughout the entire emitter-base junction thus giving rise to more uniform electron distribution and good current handling capability. In addition, due to the vertical electric field in the scr base, a significant portion of the

electrons injected into qnr base are attracted into the scr base devoid of holes as is indicated by the red curved arrow in Fig. 4.3, thereby reducing the recombination current and further increasing the current gain of the device. As a result, the simulation result showed that the current gain can increase from less than 5 in the conventional lateral BJT in Fig. 4.6 to a few hundred (>200) in the GL-BJT by virtue of scr-base induced by the MOS gate on top of p-base region.

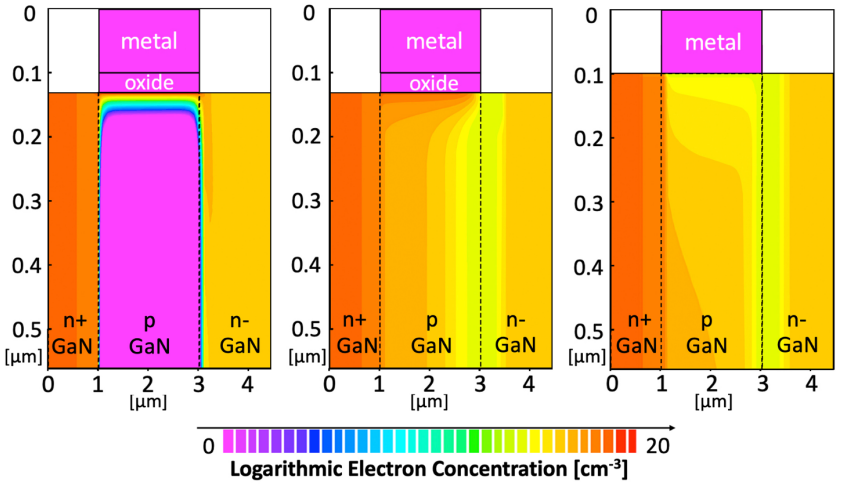

Figure 4.6 Distribution of electron concentration in *n*-channel MOSFET (inversion mode), npn GLP-BJT and conventional npn lateral BJT (both under forward active mode), respectively [21].

Then, to illustrate the extra benefits for the GL-BJT to have fully lateral p-n junctions, which otherwise cannot withstand a high reverse bias due to absence of a drift layer. In this sense, the gated lateral (GL)-BJT with the fully-lateral n-p-n structure becomes a gated lateral power (GLP)-BJT for the first time, as shown in Fig. 4.7. In addition, unlike Si gated lateral BJT [14], there is no parasitic vertical BJT in the fully-lateral n-p-n structure. Furthermore, as seen in the upper image of Fig. 4.7, the injection area for electrons (red line) is much smaller than the injection area for holes (green line) in Si gated lateral BJT, whereas the two areas are equal in the gated lateral power BJT. The last two factors further improves the current gain of the GLP-BJT with fully-lateral device architecture to maintain a high value at high injection current density.

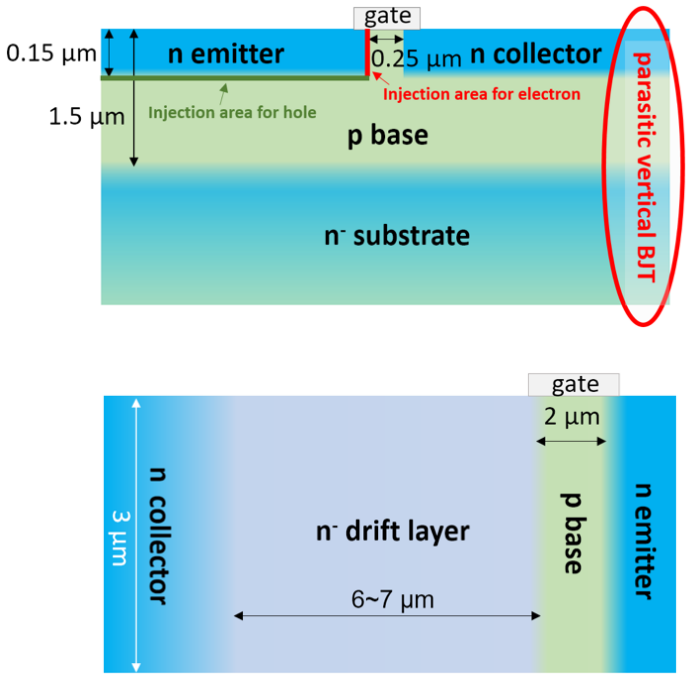

Figure 4.7 The difference between the structures for the conventional gated lateral BJT (in the case of Si) and the gated lateral power BJT (this dissertation).

4.3 Fabrication of Gated Lateral Power BJT

The schematic illustrations of the key growth and process steps are shown in Fig. 4.8 which were similar to the GaN diodes in the preceding Chapter. GaN stripes were grown by metalorganic vapor phase epitaxy on a LPCVD-SiN_x mask-patterned sapphire substrate through a combination of the epitaxial lateral overgrowth with in-situ doping, resulting in the $n^+/n^-/p/n^+$ core-shell doping structure. Then, a double-step Cl_2-based ICP-RIE (ICP power 150W, RF power 30W) was utilized with Ni mask to tailor GaN stripes into arrays of islands characterized by the non-polar *a*-plane lateral n-p-n homojunctions. Here n^+-GaN has [Si]>1×10^{19} cm^{-3}, n^--GaN has $|N_d - N_a| = 6\times16$ cm^{-3} and p-GaN has [Mg] =3–5×10^{18} cm^{-3} which contributes to a calculated hole concentration of 0.7-1.6×10^{17} cm^{-3} (assuming compensated $N_d = 6\times16$ cm^{-3} and acceptor ionization energy $\Delta E_{A,0} = 220$-

245 mV) [22], [23]. The resistivity of p-GaN was measured to be 3.5 Ω.cm by the transfer length method. The calculation of these properties are shown in the next section.

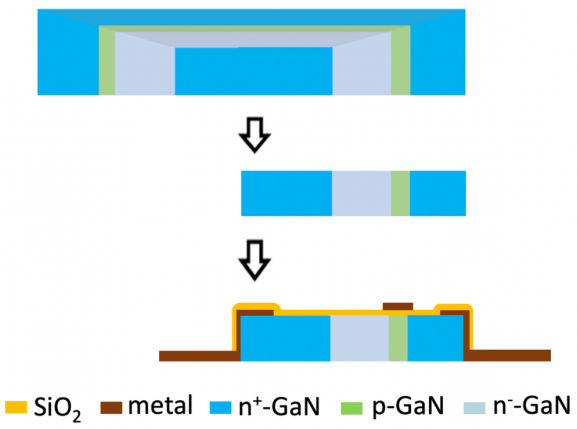

Figure 4.8 Cross-sectional schematics of the key steps of growth and process for the GLP-BJT fabricated on the GaN island [21].

The inverted hexagonal pyramidal pits with $\{10\bar{1}1\}$ facets and 200-400 nm diameter were introduced by ICP-RIE process on the etched top surface of GaN islands (Fig. 4.10). The appearance and diameter of nanopits were modulated by the ICP and RF power of the etching process. SiO_2 of ~40 nm was sputtered as gate oxide (with non-rotating substrate holder) leading to incomplete oxide coverage inside the nanopits. After that, Si (~5 nm) was sputtered followed by thermal annealing (750 °C, 1hr) to render the diffusion of Si atoms as n-type dopant into the surface atomic layers of p-GaN nanopits for an N-P tunnel junction (TJ). After TMAH solution treatment to remove residual Si, photolithography and BOE were used to create openings in the passivation layer followed by sputtering of Ti (20 nm)/Al (150 nm) as collector and emitter contacts/pads and annealing (800 °C, 30s). Then, after photolithography again, Al (180 nm) was sputtered as metal gate and pad followed by annealing (400 °C, 1hr). The metal gate also formed Ohmic contact to p-base via the TJ at the nanopits. Actually, other than Si diffusion-enabled TJ, the Ohmic contact can be alternatively enhanced by the similar diffusion process of deposited Mg

metal into p-GaN with conventional Ni/Au metal contact [24], [25], which will be elaborated in the Chapter 6. In addition, electron beam lithography can be utilized to make orderly nanoholes in the gate oxide instead of randomly-distributed nanopits in the p-base region in order to improve the device yield.

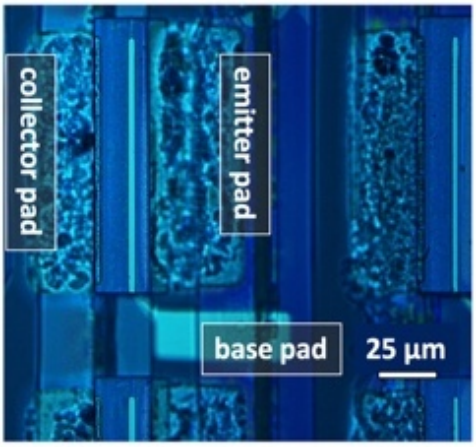

Figure 4.9 Bright-field optical microscopic image of the as-processed devices (mercury lamp was used as illumination source) [21].

The as-fabricated device is shown in Fig. 4.9. The gate, base pad, collector pad, and emitter pad and the ELO-GaN island can be clearly observed. In addition, as can be distinguished in the magnified views due to the secondary electron dopant contrast in Fig. 4.10, the collector drift region has a width of 6–7 µm and is sandwiched between the slightly darker n^+-collector on the left and brighter p-base of ~2 µm width on the right.

Specifically, the incomplete coverage of oxide inside the V-shaped nanopits was intentionally rendered using non-rotating sample holder (shadowing effect) in a sputtering system, where the shadowing effect works. The morphology of the nanopits features inverted hexagonal pyramidal shape and six $\{10\bar{1}1\}$ facets. The appearance and diameter of these pits can be modulated by RF power and ICP power of the ICP-RIE system, as shown in the Fig. 4.11 (right).

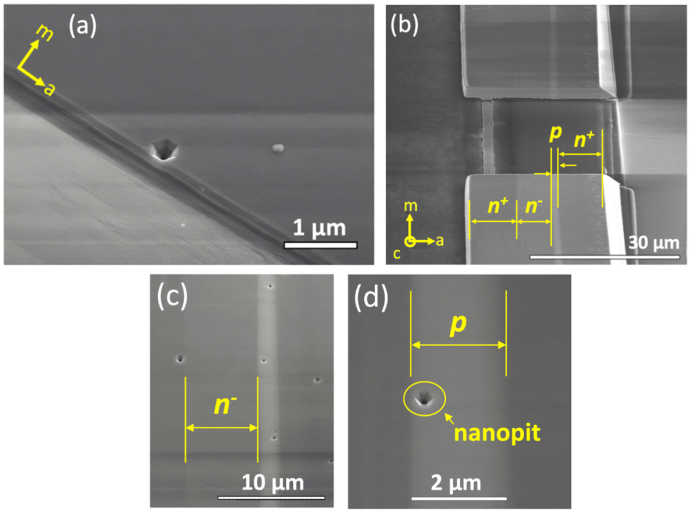

Figure 4.10 Angled-view scanning electron microscopic image of the GaN islands with the lateral n^+-n^--p-n^+ homojunctions before metallization and oxide deposition process: (a) The inverted hexagonal pyramidal pits introduced by ICP-RIE process on the etched top surface of GaN islands. (c)(d) Magnified-views of (b) which reveal the width of n^--collector drift region and p-base region as well as hexagonal nanopit on the surface of p-base region. ((b)(c)(d) are from [21])

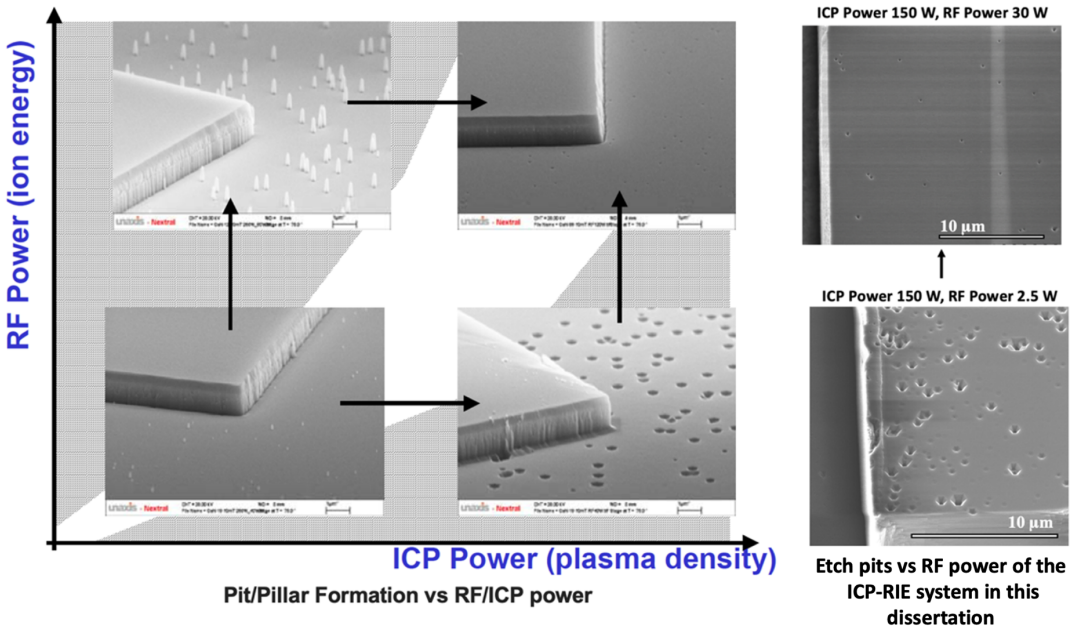

Figure 4.11 The appearance and diameter of these pits can be modulated by RF power and ICP power of the ICP-RIE system (left image from [26]).

4.4 Performance of Gated Lateral Power BJT

The electrical measurements were carried out in the common emitter configuration by an Agilent B1505A semiconductor analyzer. The entire cross-sectional area of the device (i.e., the section B-B in Fig. 4.2) was taken into calculation for current density, which has typical dimensions of 100 um (width) × 3 um (height).

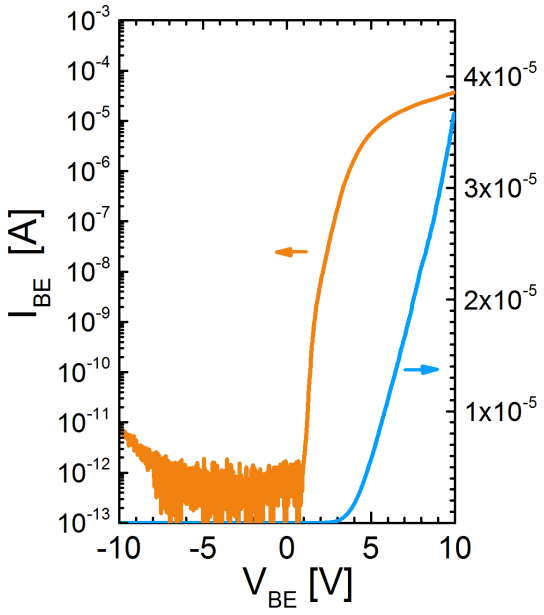

Figure 4.12 Open-collector I-V characteristics of the GaN GLP-BJT.

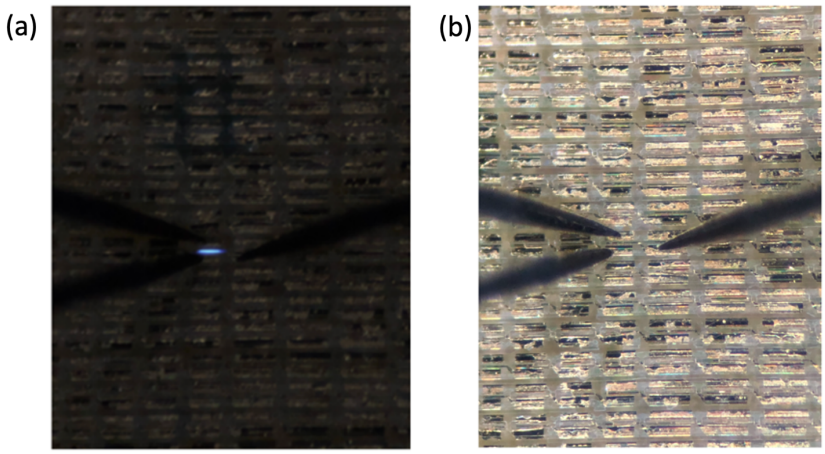

Figure 4.13 (a) Blue electroluminescence during the measurement under dark condition and (b) the same sample area under zero bias under bright condition.

Fig. 4.12 shows the open-collector I-V characteristics which is measured between base and emitter terminals of the device. It can be seen that a good rectifying (on/off ratio>10^7) GaN p-n junction with turn-on voltage of ~4V was demonstrated, which also implied that the Ohmic contact was formed to the p-base. Furthermore, the weak blue luminescence during the measurement shown in Fig. 4.13 could further prove the bipolar action of the device.

A quantitative evaluation of the hole concentration p in the p-base is calculated based on:

$$p + N_{D,compensating} = \frac{N_A}{1+\frac{pg_A}{N_{V,eff}}\exp\left(\frac{\Delta E_A}{kT}\right)} \tag{4.4}$$

$$\Delta E_A = \Delta E_{A,0} - f.\left(N_A^-\right)^{\frac{1}{3}} = \Delta E_{A,0} - f.\left(p + N_{D,comp.}\right)^{\frac{1}{3}} \tag{4.5}$$

$$f = \Gamma\left(\frac{2}{3}\right)\left(\frac{4\pi}{3}\right)^{\frac{1}{3}}\frac{q^2}{4\pi\varepsilon_{GaN}} \tag{4.6}$$

where $g_A = 4$, $\Delta E_{A,0}$ =220–245 mV [22], [23]. It is acceptable to assume that N_A/[Mg]=100% when [Mg] is below the order of 10^{19} cm^{-3}. The unintentionally-doped drift layer has net doping concentration of $|N_D\text{-}N_A|$ of up to 6×10^{16} cm^{-3}, which may be used to estimate the compensating donor. [Mg]=$3–5\times10^{18}$ cm^{-3}.

Since the concentration of hole changes with the independent variables of [Mg], $\Delta E_{A,0}$, and $N_{D,comp.}$. We assume a total of 8 cases (=2^3) where each case is a combination of either upper- or lower-bound value of the three variables, then the following Table 4.1 can be drawn:

Table 4.1 The concentration of hole (p) as a function of [Mg], $\Delta E_{A,0}$, and $N_{D,comp.}$.

Case	[Mg] [cm^{-3}]	$\Delta E_{A,0}$ [meV]	$N_{D,comp.}$ [cm^{-3}]	p [cm^{-3}]
1	3.0E+18	220	0	1.4E+17
2	3.0E+18	245	0	9.2E+16
3	3.0E+18	220	6.0E+16	1.2E+17
4	3.0E+18	245	6.0E+16	6.9E+16
5	5.0E+18	220	0	1.9E+17
6	5.0E+18	245	0	9.2E+16
7	5.0E+18	220	6.0E+16	1.6E+17
8	5.0E+18	245	6.0E+16	1.0E+17

It can be seen that the lower-bound estimate of hole concentration is 6.9×10^{16} cm^{-3} in the case 4 and the upper-bound estimate of hole concentration is 1.9×10^{17} cm^{-3} in the case 5. In fact, the hole concentration of $0.69–1.9\times10^{17}$ cm^{-3} is also a commonly seen range in the p-region of GaN p-n junction. As a reference, the best reported p-n junction diode featuring near-unity ideality factor in the literature also reported a hole concentration of 7×10^{16} cm^{-3} [27].

In addition, the TLM measurement results are shown in Fig. 4.14 which shows the specific contact resistivity is 49 $m\Omega.cm^2$, and the estimated hole concentration is 8.9×10^{16} cm^{-3} in consistency with the theoretical estimate.

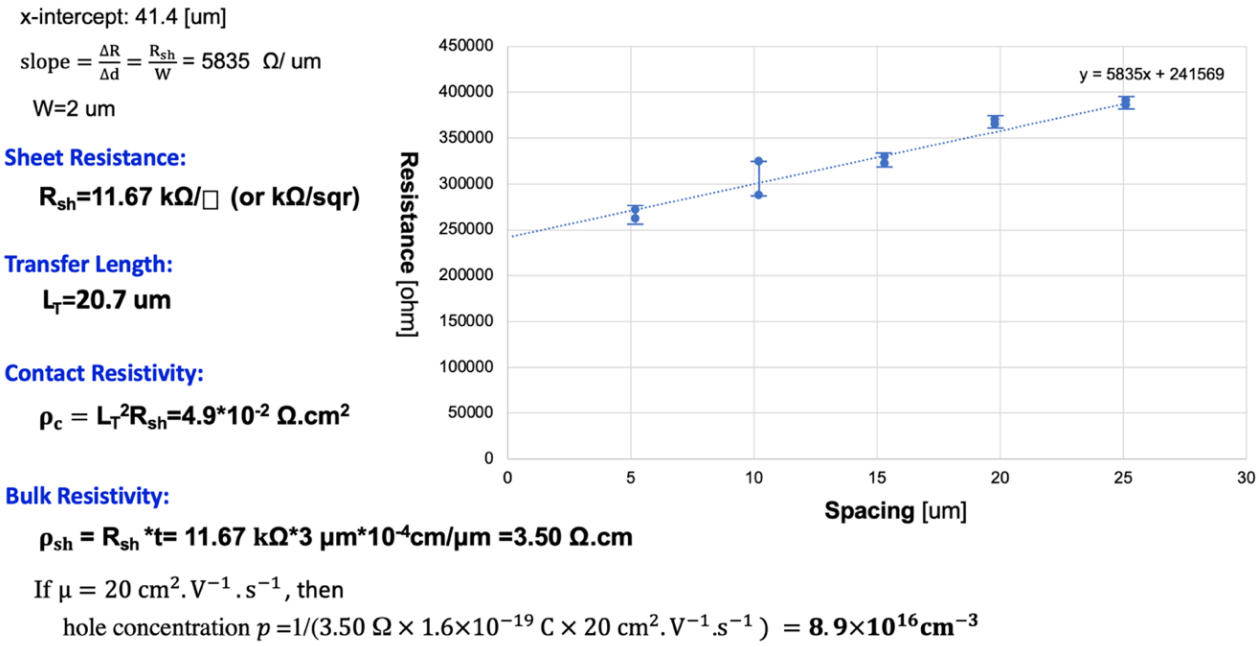

Figure 4.14 TLM results of the Ohmic contact to p-base.

It is based on the above three aspects that we may safely conclude that the base region is p-type and that the Ohmic contact is formed between the metal and p-base.

In general, the "three standard *I-V* plots" of a BJT, i.e., the Gummel plot (combined plot of I_C and I_B versus V_{BE} on a semi-logarithmic scale) measured under V_{BC}=0, the common-emitter output

V_C-I_C characteristics with varying driving current I_B, and the open-base *I-V* characteristics, are commonly accepted to contain all the essential information to evaluate a BJT.

The Gummel plot is shown in Fig. 4.15. I_C was greater than I_B even at low-voltage level, suggesting that the recombination current was suppressed [28]. The current gain β (= I_C/I_B) peaked at 1200 and remained a plateau of around 300 until I_C = 6 mA corresponding to a collector current density J_C of 2 kA/cm^2. Given that the p-base region is ~2 μm wide, a higher current gain is readily accessible should the p-base region be narrowed into sub-micrometer scale.

It should be noted that although the highest current gain reached 1000, it was achieved at low current level (J_c=10 A/cm^2) and low voltage (V_{CE}=3V) corresponding to a DC power density of 30 W/cm^2, making it less significant than the value of 300 achieved at high current level of J_c=2 kA/cm^2 and high power density of 40 kW/cm^2 (V_{CE}=20V) in terms of power handling capability of GLP-BJT which is chosen for benchmarking in Fig. 4.18.

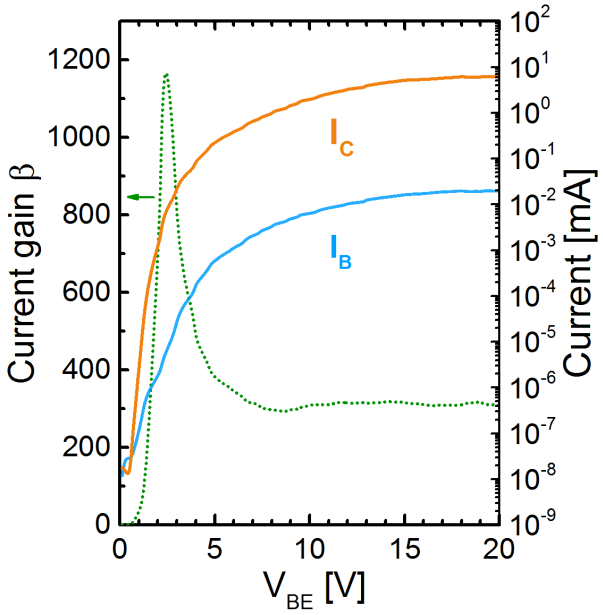

Figure 4.15 The Gummel plot of the GaN GLP-BJT.

The common-emitter output *I-V* characteristics of the GaN GLP-BJT is shown in Fig. 4.16. The input I_B was varied from 0 to 5 μA at a step of 0.5 μA and the output I_C ranged from 0 to 1.5 mA exhibiting a current gain of ~300, which is among the highest values of current gain achieved in power bipolar transistors. Furthermore, the Early effect was not pronounced which embodied an inherent advantage of wide base region [1], [13].

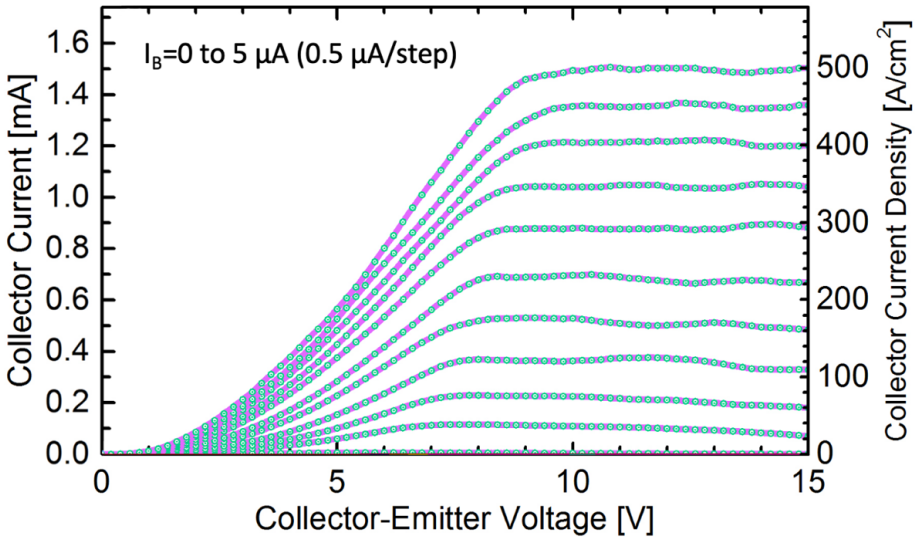

Figure 4.16 Common-emitter output characteristics of the GLP-BJT [21].

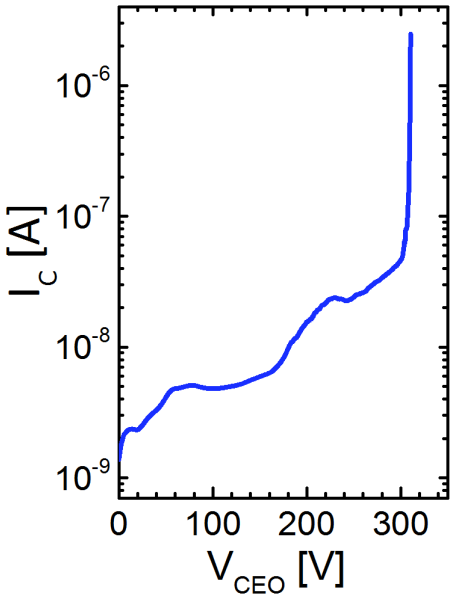

Figure 4.17 Open base blocking I-V characteristics of the GLP-BJT.

Admittedly, the relatively high knee voltage is a typical issue in the GaN-based BJTs or HBTs, the reason is believed to be mostly due to the high base contact resistance [29]. It is known that good p-type Ohmic contact has been a longstanding challenge in GaN devices due to the limited hole concentration. To make the matter worse, since ICP-RIE is necessary in the device fabrication of a GaN-based bipolar transistor, the p-base is subject to plasma-induced surface damages that could introduce nitrogen vacancies as compensating donors which further increase the contact resistance to the p-base region. In spite of this, the knee voltage of ~8 V in this work is among the lower-range values [28], [30] where the lowest report is 6.5 V [29]. This is attributed in part to the moderately acceptable p-base contact resistance (0.05 $\Omega.cm^2$). Fortunately, the effective solution to solving the bottleneck of recovering the plasma etching-damaged p-GaN and obtaining an excellent Ohmic contact is finally found and will be discussed in Chapter 6. This should further help improve the output I-V characteristics of the GaN GLP-BJT in the future research.

The open base *I-V* characteristics was measured on the same device as seen in Fig. 4.17, the open base breakdown occurred at 300–310 V at 0.1 A/cm^2. In principle, the BV_{CEO} is expected to reach 900 V should the doping concentration of n^--collector drift region be reduced below 2×16 cm^{-3} [31]. The breakdown voltage of ~300 V corresponded to a critical E-field of 2.5 MV/cm. This is a high E-field for GaN which implies effective edge termination schemes are needed to alleviate surface field crowding and further enhance the breakdown voltage, as is discussed in Chapter 3 in which a high E-field of 3.3 MV/cm was demonstrated in the lateral p-n diode employing almost the same n- drift region (i.e., doping concentration and drift region thickness) by effective edge termination schemes of field plate and bevel edge termination.

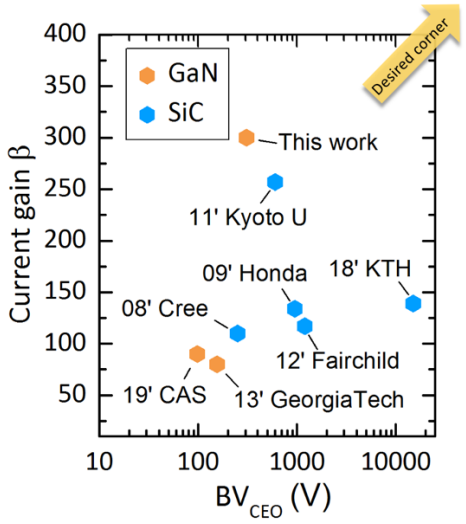

Figure 4.18 Benchmark of common-emitter current gain β vs open base breakdown voltage BVCEO of the GaN-based HBTs and 4H-SiC-based BJTs reported in the literature which satisfied the levels of β > 80 and BVCEO > 50 V [3], [8], [28], [29], [32]–[34]. The arrow indicates the desired corner.

To highlight the potential of achieving otherwise tradeoff metrics of high current gain and breakdown voltage, the combined result is benchmarked in Fig. 4.18 with the state-of-the-art GaN-based HBTs and 4H-SiC-based BJTs which satisfied BV_{CEO} >50V and β >80 [3], [8], [28], [29], [32]–[34]. The current gain at high current and power density levels (β=300), instead of that at low-current level (β>1000), is chosen for the benchmarking. It can be seen that compared to a few existing works in the literature that meet the above-described levels, the GLP-BJT stands out as a competitive candidate to combine the merits of high current gain and high breakdown voltage.

4.5 Insulated-Gate Bipolar Transistor

IGBT was invented by Dr. Jayant Baliga in the last 80s [35] which was considered to be one of the most important breakthroughs in the power switching field. Today Si IGBT still plays the dominant role in the high voltage switching electronics market [36]. For IGBT, it combines the

simple gate-drive characteristics of MOSFETs with the high current handling capability of BJT [1]. Such advantages are highly desired and can further benefit the performance of power switching electronics if a IGBT can be realized on the wide bandgap semiconductor like GaN.

However, there has been no experimental demonstration of GaN IGBT mostly because the difficulty in achieving the doping structure of p-n-p-n and the problematic p-type GaN-an intrinsic issue of GaN material. The difficulty to solve the challenges related to the p-type GaN stems from two aspects: inaccessible p-type GaN substrate and high resistivity p-type GaN. The former one could be possibly solved by finding appropriate p-type doping technology associated with HVPE growth. The second one is related to the low hole concentration even with the highest acceptor doping density and the intrinsic low mobility of holes due to the heavy effective mass.

The relationship between the hole concentration and acceptor concentration (N_A) in GaN can be calculated by combining Eqn. (4.4)–(4.6). The calculated result by 1D-FEA modeling is shown in Fig. 4.19. It can be seen that the hole concentration is only 10^{18} cm^{-3} when the acceptor concentration is 10^{20} cm^{-3}. To make the matter, it is not practical to have acceptor concentration in GaN above 10^{20} cm^{-3} due to the reduced activation ratio (%) of N_A/[Mg]. As a result, it is quite common to see that the acceptor concentration remains almost constant around ~10^{19} cm^{-3} when the [Mg] increases from 10^{19} cm^{-3} to over 10^{20} cm^{-3}-making it an issue known as self-compensation. As a consequence, it is practically hard to produce hole concentration in GaN above 10^{18} cm^{-3} [37]. Furthermore, the mobility of hole decreases with increasing the hole concentration due to increased scattering by ionized acceptors. The low-field hole mobility versus acceptor concentration is also shown in Fig. 4.19 which is modified from the data based on a Monte Carlo approach [38]. It is worth mentioning that the hole mobility in GaN is generally below 10 $cm^2/V.s$ in most real cases. All these factors lead to the low p-type GaN conductivity which is the product of hole mobility,

hole concentration, and the hole charge. For a common case, $p=1\times10^{18}$ cm^{-3}, $\mu_h=6$ cm^2/V.s, then p-type GaN resistivity is $\varrho=1/\sigma=1/qp\mu_h=1/(1.6\times10^{-19}C\times1\times10^{18}$ cm$^{-3}\times6$ cm^2/V.s$)=1.0$ Ω.cm.

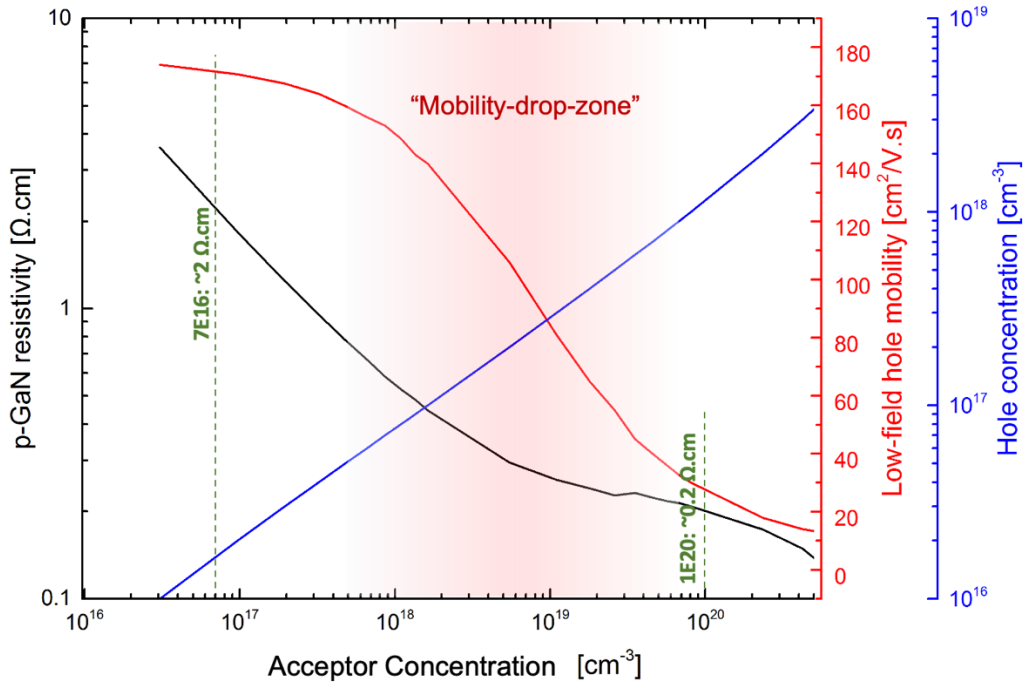

Figure 4.19 Calculated plot of the hole concentration and p-GaN resistivity as a function of acceptor concentration.

Given that the p-type GaN is intrinsically low, imagine that if a p-type GaN substrate could be produced like that of an available n-type GaN substrate today, the substrate resistivity $R_{sub}=1.0$ Ω.cm× 0.04 cm=40 mΩ.cm^2 for a 400 μm-thick commercial p-GaN substrate with hole concentration of 1×10^{18} cm^{-3}. This is an order of magnitude higher than the $R_{on,sp}$ of a unipolar GaN MOSFET capable of withstanding a V_{BR} of over 1200 V, making it unpractical to build a vertical IGBT on the p-type GaN substrate like the structure of a Si IGBT.

On the other hand, the true-lateral device architecture on the ELO-GaN may present unprecedented opportunities towards the realization of structure of an IGBT. The doping structure of n-p-n-p can be realized by growing ELO-GaN pre-coalescence islands with n-p-n half-core-

shell followed by dry etch tailoring. The exposed p-GaN sidewall on one side of the tailored island can readily serve as a pseudo-p-type substrate when the metallization is formed onto it. This will simultaneously address another challenge to reduce the resistance of p-type GaN substrate owing to the thin p-GaN layer (1–2 μm). All of these benefits make the ELO-enabled true-lateral structure a practical and easy solution to addressing the challenge of a GaN IGBT.

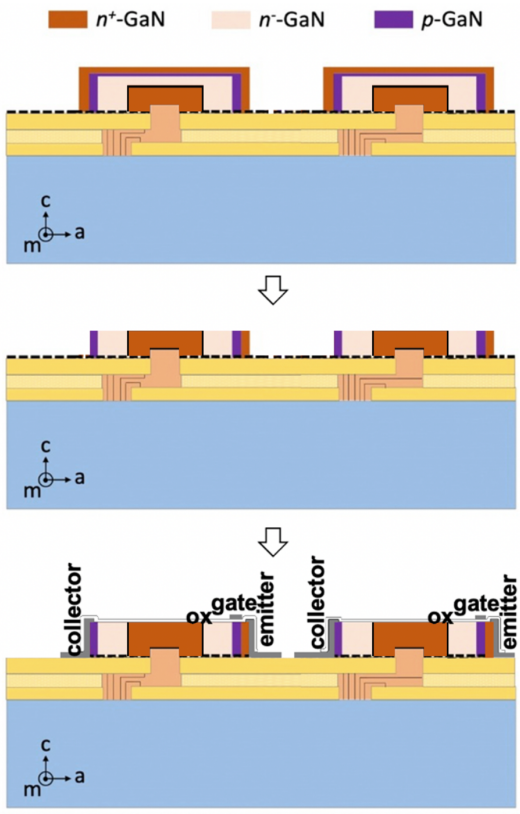

Figure 4.20 Cross-sectional schematics of the key steps in the fabrication of IGBT on the ELO-GaN.

Figure 4.20 shows cross-sectional schematic illustration of the key steps in the fabrication of IGBT structure on the ELO-GaN island. The device has laterally aligned p-n-p-n doping structure, obtained after the dry etching of an ELO-GaN island with half-core-shell n-p-n doping structure. Similar to the GLP-BJT, the metallization is formed onto the opposite sidewalls of the GaN island as collector and emitter, Ni/Au is E-beam evaporated onto the p-sidewall for collector and

Ti/Al/Ti/Au is E-beam evaporated onto the n-sidewall for emitter. SiO_2 is deposited via sputtering onto the top surface of the island for gate oxide. Metal gate (Ni/Au) expands over the p-base sandwiched between the n-regions. Different than the GLP-BJT in which part of the metal gate forms direct contact to the p-base, the IGBT has part of the emitter extending out which forms direct contact to the p-base. The opening in the oxide on the p-base for the direct contact is made by CF_4 RIE. This extended part of the emitter is formed by Ni/Au, which is depicted in the stereographic illustration of the fabricated IGBT arrays in Fig. 4.21. The n^+-emitter and p-base are shorted through emitter metallization to avoid accidental turn-on of the parasitic n-p-n BJT during the OFF state. As a result, the emitter has an "Enter key"-like shape. Finally, all the contact pads are deposited by Al sputtering on the insulating substrate.

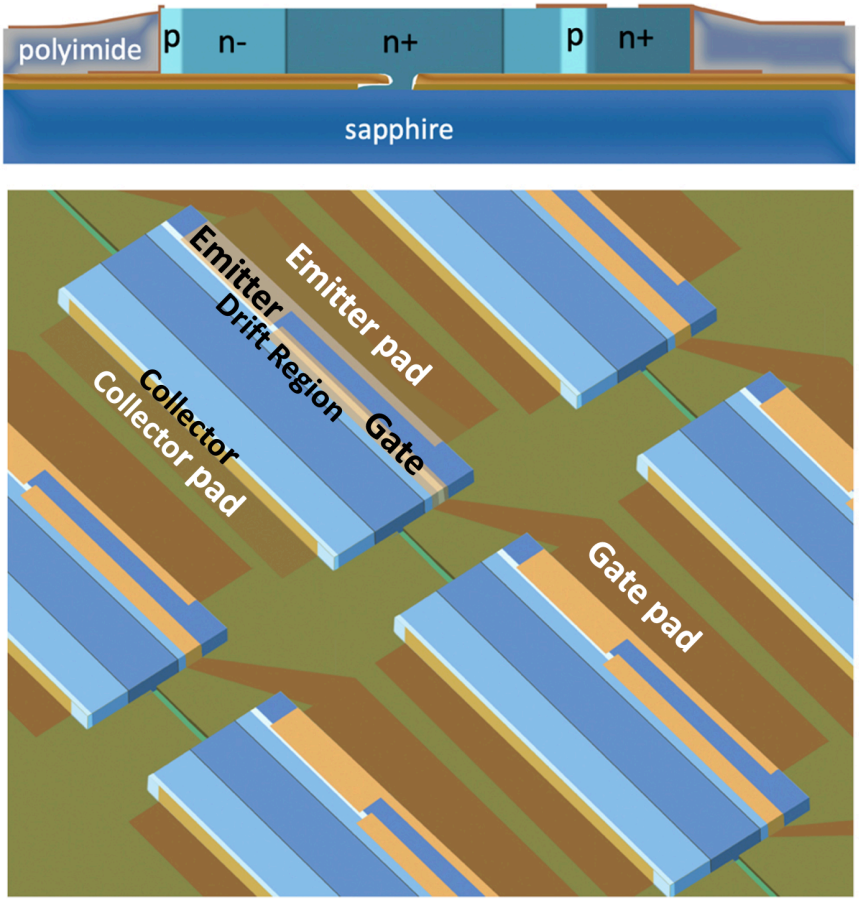

Figure 4.21 Cross-sectional and stereographic illustrations of the IGBT on the ELO-GaN islands.

The p-n-p-n doping structure on the ELO-GaN island before metallization is shown in the angled-view SEM image in Fig. 4.22. The island has a length of 100 μm. The p-sidewall on the left side of the island appears as bright white region which has a width of 1.5–2 μm and can be clearly seen in the inset of Fig. 4.22. In addition, the p-base sandwiched between the two n-regions has a width of 2 μm, as can be seen in Fig. 4.22 as well.

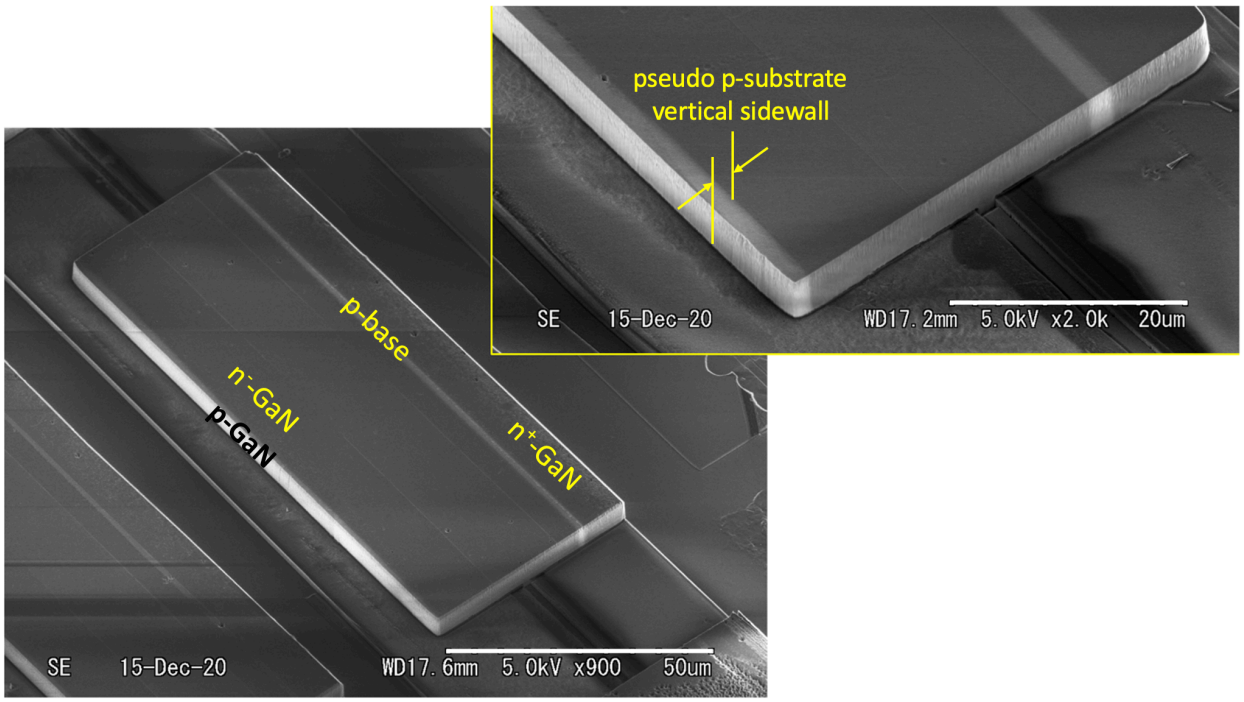

Figure 4.22 Angled-view SEM image of the p-n-p-n doping structure on the ELO-GaN island before the metallization processes, the inset shows the magnified view.

Figure 4.23 shows the plan-view fluorescence microscopic images of the fabricated IGBTs on the ELO-GaN islands with varying lengths. The left column is bright field imaging mode whereas the right column shows the corresponding images in fluorescence imaging mode. The relative position of the metal electrodes in pitch black (including the gate and extended part of the emitter) against the doping regions in colors can be readily observed. The p-base and the n^+-emitter both

appear as blue color mainly due to the incorporation of Mg in the n^+-emitter region as a result of the memory effect of Mg and continuous ELO growth of n-p-n structure.

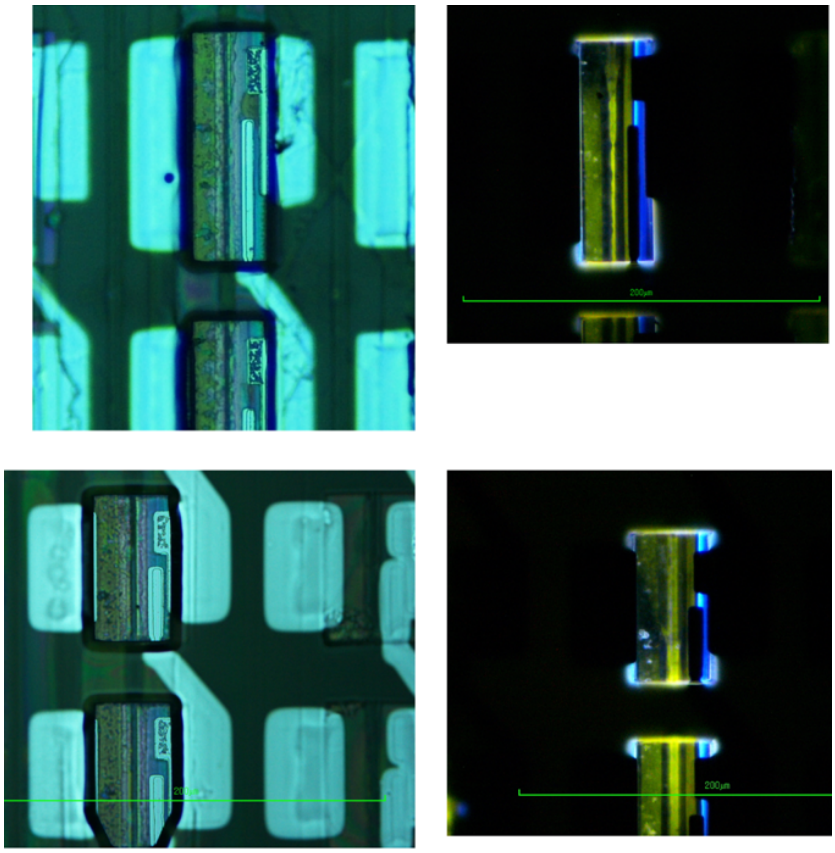

Figure 4.23 Plan-view fluorescence microscopic images of the fabricated IGBTs on the ELO-GaN islands with varying lengths (scale bars are 200 μm).

The three-terminal IGBT being measured for I-V test is schematically illustrated in Fig. 4.24. The corresponding microscopic image for the IGBT arrays being measured is shown on the left. In order to optimize the spatial arrangement for contact pads, the gate pad of an IGBT overlaps with the emitter pad of a neighboring IGBT in the same column. The emitter terminal is grounded.

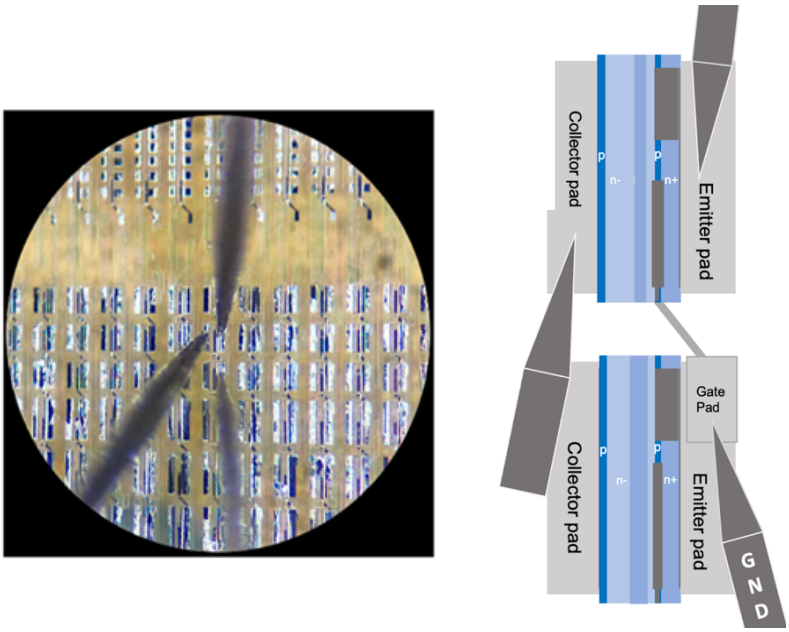

Figure 4.24 Schematic illustration of the IGBT being measured and the corresponding microscopic photo showing the real measurement.

The transfer characteristics and the output characteristics of the prototype GaN IGBT is shown in Fig. 4.25. The collector-emitter current I_{CE} is plotted both in semilogarithmic and linear scale against the gate-emitter bias V_{GE} and the gate leakage current I_G is plotted in semilogarithmic scale against V_{GE} in the same plot. It can be seen from the output characteristics that the collector current I_{CE} has a turn-on voltage between 3–4 V and the linear region of the curve resembles the forward I-V characteristics of a GaN p-n junction, which is a signature of the IGBT output characteristics. It proved that the prototype GaN IGBT is demonstrated. In addition, the non-saturating curves in the saturating region and the relative low density of collector current have do to with the high contact resistance of p-collector which is compromised by the plasma-etching induced damages when the p-sidewall is exposed by dry etching. As a result, in order to improve the performance of the GaN IGBT, this issue should be well addressed, which will be discussed in Chapter 7.

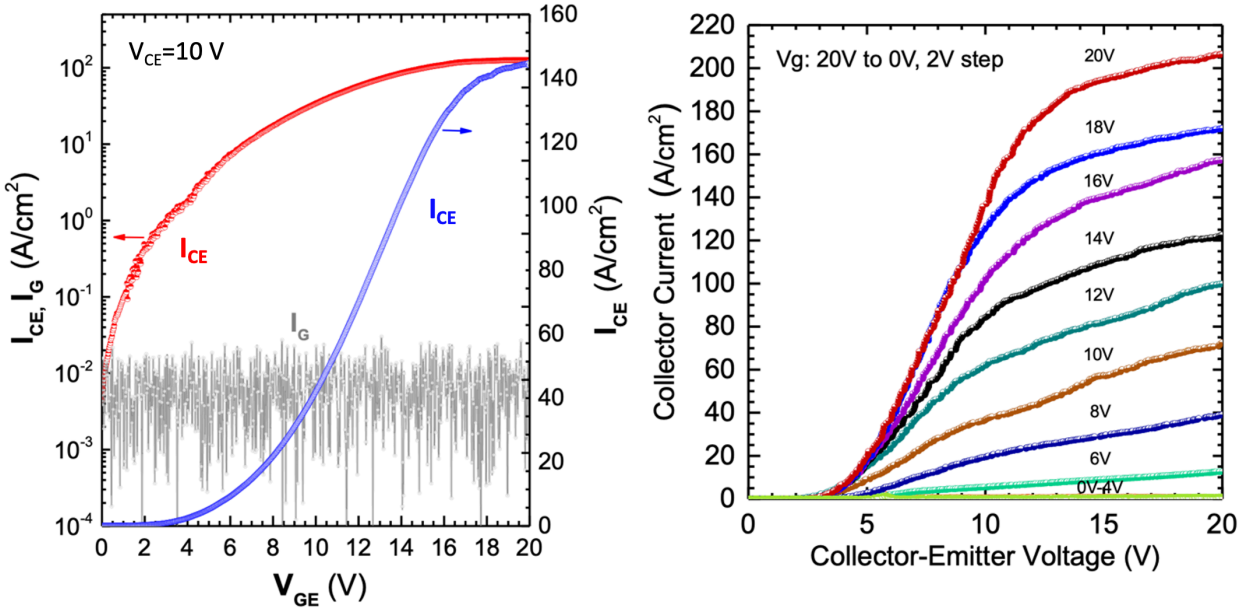

Figure 4.25 The transfer characteristics and the output characteristics of the prototype GaN IGBT, respectively.

4.6 Summary

In summary, both prototype GaN GL-BJT and IGBT were demonstrated using the selective area doping enabled by epitaxial layer overgrowth.

The gated lateral power bipolar junction transistor (GLP-BJT) was first proposed and elaborated from the perspectives of device physics and TCAD modeling. For the n-p-n GLP-BJT on wide bandgap semiconductor, reduced potential barrier are seen by electrons that are injected from n^+-emitter into the depleted p-base region underneath the gate devoid of holes, leading to a high current gain in a Gated Lateral BJT. Meanwhile, it exhibit much higher current and power handling capability than Si-based Gated Lateral BJT due to the intrinsic advantages of GaN. As a result, the fabricated GaN GLP-BJT featured a high current gain of 300 and a base region capable of withstanding high blocking voltage (BV_{CEO} > 300 V) and high critical E-field. These figures of merit thus show strong promise of GLP-BJT in power applications. In this sense, although the

high-gain GLP-BJT was demonstrated on GaN, it also provides new insights to the development of state-of-the-art bipolar transistors based on other wide bandgap semiconductors such as SiC thanks to the good generalizability of this device. Once the bottleneck of achieving high current gain in the wide bandgap semiconductor BJT can be overcome, the true benefits of the bipolar transistors, such as the potential to achieve conductivity modulation, are expected to be fully realized [21].

On the other hand, the prototyping of insulated gate bipolar transistor (IGBT)-another important type of bipolar transistor-was demonstrated on the ELO-GaN islands. There was no experimental demonstration of GaN IGBT whereas the SiC IGBT is also far from commercialization [39]. The true-lateral p-n-p-n structure enabled by the epitaxial lateral overgrowth provides the sole practical solution to realizing a GaN-based IGBT which has been hampered by the issues related to the p-type GaN substrate. Relevant discussion was provided and the prototyping current-voltage characteristics were presented.

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Chapter 5

GaN Substrate with Repeating Laterally Patterned p-n Junctions

5.1 Overview

As mentioned in Chapter 1, in order to achieve the desired selective-area doping profiles configured for an ideal power switching electronic device, innovative measures need to be taken either in the material growth or device processing stage to tailor the half-core-shell doping profile of the pre-coalescence ELO-GaN islands. In Chapter 3 and Chapter 4, the innovative measure in the device processing is employed to render GaN diodes and transistors with fully laterally aligned p-n junctions.

As an alternative approach, in this Chapter, the innovative measure in material growth is discussed to satisfy the purpose of turning the half-core-shell doping structure into the desired selective-area doping profile in a GaN substrate which features repeating laterally patterned p-n junctions. Such measures can also be categorized as a new type of growth and transfer approach named as bottom-up epitaxial layer transfer or epitaxy-enabled substrate transfer.

The concept of the bottom-up epitaxial layer transfer is in contrast to the top-down transfer. In general, top-down epitaxial layer transfer [1], i.e., bonding of host substrate to the epitaxial active layer in a top-down manner and subsequent release of active layer from the parent substrate, has been the dominant methodology with various manifestations such as epitaxial lift-off [2], tape-assisted layer transfer[3], and transfer printing[4]. On the contrary, we may alternatively infer that the host substrate can be in-situ created by the bottom-up deposition or growth as well. In such a case, the integration of epitaxial active layer to the host substrate and separation from the parent substrate makes the whole process a bottom-up epitaxial layer transfer. Compared to the top-down transfer, the bottom-up approach features epitaxial bonding of active layer to the host substrate.

The seamless integration of a specially doped active layer may endow the host substrate with unprecedented functionalities. Like porosity to a native substrate product [5], a large-scale native substrate product with built-in laterally patterned p-n junctions is an appealing functionality especially for a wide bandgap (WBG) due to a rising need for GaN power electronics to have laterally patter p-n junctions[6] to render advanced electronic devices such as normally-off planar-gate vertical field effect transistors, current-aperture vertical electron transistors (CAVETs) [7], and super-junction MOSFETs [8].

Using the bottom-up epitaxial layer transfer approach, the GaN active layer with hundreds or even thousands of repeating laterally-patterned p-n junctions grown from a foreign insulating wafer can be entirely transferred onto a native conducting substrate without using laser radiation [9], [10], sacrificial layer [11] and wet chemical etching [12]. Furthermore, the p-n junctions have significant vertical junction depth that would otherwise be inaccessible by deep ion implantation or diffusion. These unique features also render the effective utilization of a handful of state-of-the-art dopant mapping techniques, whose results are mutually verified, as will be discussed in Chapter 6. Finally, the normally-off planar-gate vertical MOSFETs with good device performance and simpler process flow are fabricated, which highlights the functionality of the GaN native substrate product for the facile fabrication of desired vertical electronic devices.

5.2 Hybrid Epitaxy-enabled Substrate Transfer

5.2.1 General Methodology

The schematic illustrations of the innovative bottom-up epitaxial layer transfer process are shown in Fig.5.1 (a)-(d) and the process consists of the four major steps. Firstly, the mask layer(s) is/are patterned onto a foreign parent substrate to prepare for the epitaxial lateral overgrowth of GaN (Fig. 5.1(a)). Secondly, the first-stage epitaxial lateral overgrowth is carried out with in-situ

doping to generate GaN stripe array with half-core-shell p-n doping geometry (Fig. 5.1(b)). Thirdly, the second-stage epitaxial lateral overgrowth is carried out to achieve the coalescence of stripes and also to generate a native host substrate where a rough surface morphology, or even polycrystalline deposition in the final growth stage, is allowed (Fig. 5.1(c)). Fourthly, the new host substrate is separated from the parent substrate assisted by thermal stress and minor external mechanical force (Fig. 5.1(d)). After separation, the host substrate is flipped-over, and the flat and mirror-like surface can be intrinsically obtained regardless of rough growth morphology on the opposite side, as shown in Fig. 5.1(e). Most importantly, the active layer integrated onto the host substrate has repeating p-n doping pattern, as the inset of Fig. 5.1(e) shows, whose strike-like backbone is copied from the pattern of mask on the parent substrate as depicted in Fig. 5.1(a). Likewise, if the pattern of mask adopts other designs, like hexagonal ring network or flower network shown in Fig. 2.8, the final p-n doping pattern in the integrated active layer would vary accordingly, showing versatility in the described approach.

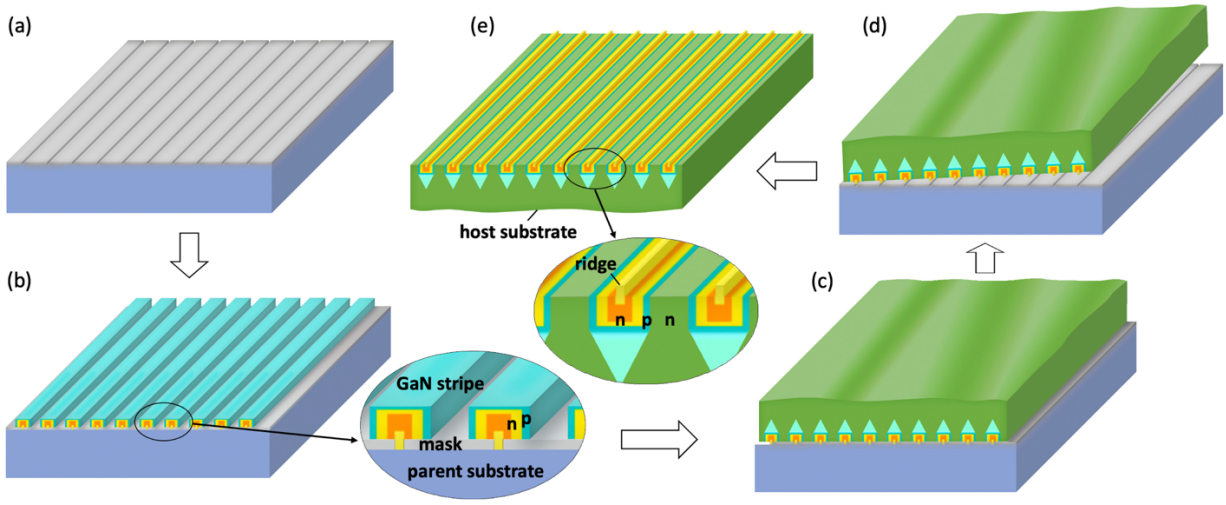

Figure 5.1 Schematic illustrations of the bottom-up epitaxial layer transfer process and the GaN substrate product in a counter-clockwise order.

5.2.2 Growth and Transfer Experiment

Like the preceding Chapters, the mask for the ELO process consists of stacking layers of $SiN_x/SiO_2/SiN_x$ which were deposited by low-pressure chemical vapor deposition (LPCVD) followed by selective dry etching, finally enclosing a serpentine-like channel. The mask has stripe-like openings along $[1\bar{1}00]$ orientation (m-direction) with three types of pitch size (distance between neighboring openings): 36 μm, 60 μm, and 100 μm. The width of opening in the top SiN_x mask is universally 2 μm.

For hybrid epitaxial growth, the two-step epitaxial growth was carried out by combining metalorganic vapor phase epitaxy (MOVPE) and halide vapor phase epitaxy (HVPE)-the two common epitaxial methods for GaN. In contrary to the HVPE-MOCVD sequence commonly employed in a direct bottom-up growth process, we adopted the reversed sequence of MOVPE-HVPE as an inherent requirement of the bottom-up transfer, making it a distinctive feature from a bottom-up epitaxial layer growth. Compared to HVPE, MOVPE can better satisfy the requirement of growing and doping GaN microstructures, such as the GaN micro-stripe array which is the main building block of the active layer. Figure 5.2 shows a set of optical microscopic and scanning electron microscopic images of the GaN samples after the first and second epitaxial growth process.

Similar to the preceding Chapters, a mask-patterned 2-inch sapphire was first loaded into a MOVPE reactor (Veeco). GaN was grown initially inside the channel via geometrically-defined heteroepitaxy. After GaN emerged from the openings of the top SiN_x mask, in-situ intentional doping was carried out along with an anisotropic lateral overgrowth where GaN island lateral extended along a-direction. A gas flow of SiH_4 was fed into the reactor and gradually decreased, forming two main levels of [Si] in the n-type GaN region. Then CP_2Mg was fed into the reactor for Mg incorporation. Finally, GaN microisland array was grown, each of which was characterized

with the half-core-shell p-n doping profile [13], as shown in Fig. 5.2(d). The GaN stripe arrays with different pitch size (36 μm and 60 μm) were achieved, as shown in Fig. 5.2(a) and 5.2(c), respectively. With the same growth time via MOVPE, the inter-gaps (to be filled via HVPE growth) between neighboring stripes were different.

After MOVPE growth, the 2-inch wafer was diced into square pieces of various sizes. After that, the 2nd-stage epitaxial lateral overgrowth and the generation of GaN host substrate was carried out by HVPE which was capable of achieving void-free island (stripe) coalescence and growing thick epi-film for freestanding substrate. Before loading into a home-made 1-inch vertical HVPE reactor, the square samples were subject to an RCA standard cleaning process except using SC1 agent (to avoid damages to the nitrogen-polar surface of GaN). The continuous HVPE growth consisted of two stages: coalescence of islands (continued growth of active layer) and film thickening (generation of new host substrate). Each stage featured different V/III ratios and growth temperature ranging from 950°C to 1080°C. The effectiveness of void-free stripe coalescence via the HVPE can be distinguished by comparing Fig. 5.2(e) and Fig. 5.2(f) where even the disjoints in the GaN stripes could be fully coalesced without leaving voids, otherwise the surface of the corresponding area in Fig. 5.2(f) should have been uneven. After the coalescence stage, the active layer was completely obtained and then integrated into the new host substrate that was bottom-up generated via HVPE growth consisting of a mixture of single-crystalline and polycrystalline GaN, followed by the final transfer stage. After unloading from HVPE reactor, a minor shear stress by a tweezer was applied to separate GaN host substrates entirely from the mask-patterned sapphire substrates.

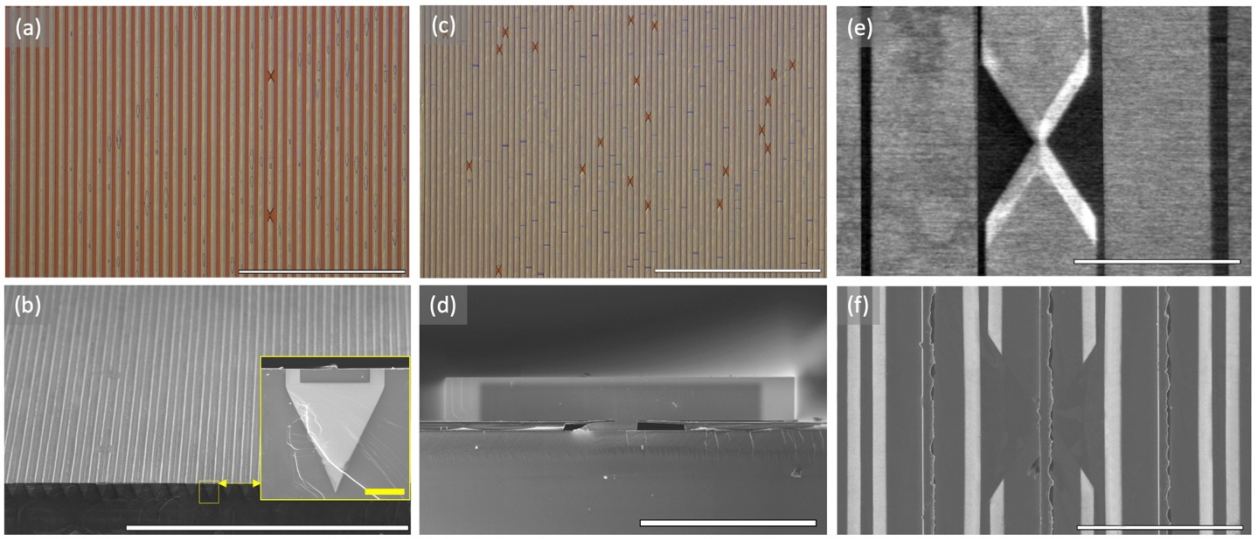

Figure 5.2 A set of optical microscopic and scanning electron microscopic images of the GaN samples after the first and second epitaxial growth process:

(a)Top-view (+c-plane) OM image of the GaN stripe array (pitch size: 60 μm) on the mask-patterned parent substrate after MOVPE stage, scale bar: 1 mm. (b) Angled-view SEM image (scale bar: 1 mm) showing the surface (-c plane) and cross-section (m-plane) of the as-separated (AS)-GaN substrate which has fully integrated the active layer featuring repeating doping profiles (periodicity: 60 μm). The inset shows a magnified cross-sectional view SEM image of a repeating unit of the active layer (scale bar: 15 μm). (c) Top-view (+c-plane) OM image of the GaN stripe array (pitch size: 36 μm) on the mask-patterned parent substrate after MOVPE stage, scale bar: 1 mm. (d) Cross-sectional view (m-plane) of a single GaN stripe on the mask-patterned parent substrate, scale bar: 20 μm. (e) Top-view (+c-plane) SEM image revealing a local disjoint in the GaN stripe on parent substrate after MOVPE stage, scale bar: 50 μm. (f) Top-view (-c plane) SEM image showing the opposite face of the active layer developed from the coalescence of GaN stripes in (e) and transferred to the host substrate, scale bar: 50 μm. The flat surface, the bright white regions indicating p-type GaN as well as the ridge-like surface protrusions can be clearly distinguished.

To investigate the crystallographic and morphological evolution of the GaN stripe array at several growth times during the 2nd stage epitaxial lateral overgrowth (via HVPE) before the coalescence stage, a couple of HPVE growth time-varying experiments (10 min, 30 min, 60 min, and 180 min) were carried out. The SEM and fluorescence microscopic images of the GaN islands were shown in Fig. 5.3. The width of GaN stripe increased with growth time while the ratio of the top plane width over the sidewall width decreased, and parasitic deposition of polycrystalline GaN was observed on the SiN_x mask, as can be seen in Fig. 5.3(a). A set of critical crystallographic planes were identified in the images and indicated by G_1, G_2 and G_3, respectively, as shown in Fig. 5.3(b). The cross-sectional view (m-plane) fluorescence microscopic image of the GaN stripe before growth (0 min) is shown in Fig. 5.3(c), where the outer p-GaN: Mg shell region corresponds to the bright white region in the inset SEM image in Fig. 5.3(b).

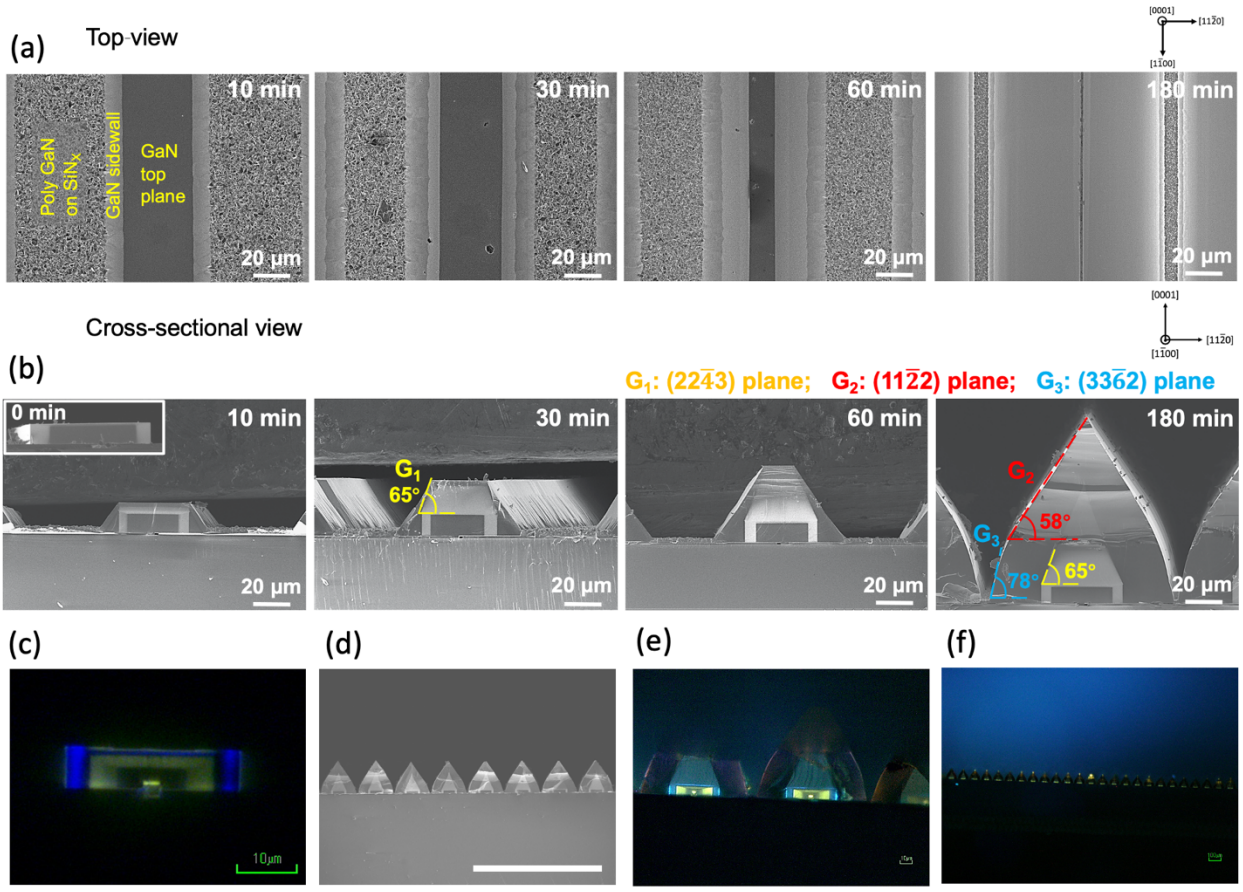

Figure 5.3 Crystallographic and morphological evolution of the GaN stripe array at several growth times during the HVPE process prior to coalescence.

(a) A series of top-view (+*c*-plane) scanning electron microscopic (SEM) images showing the lateral growth of an individual GaN stripe in the array at 10 min, 30 min, 60 min and 180 min, respectively (pitch size: 100 μm). (b) The cross-sectional view (m-plane) SEM images corresponding to the top-view images in (a), the inset of the first image shows the cross-sectional view of the GaN stripe before growth (defined as 0 min). (c) The fluorescence microscopic (FM) image of the GaN stripe before growth. (d) The cross-sectional SEM images of the GaN stripe array (pitch size: 100 μm) after 180 min growth time, scale bar: 300 μm. (d) and (f): The cross-sectional view (m-plane) FM images of the GaN stripe array (pitch size: 100 μm) after 180 min growth time with scale bar of 10 μm and 100 μm, respectively.

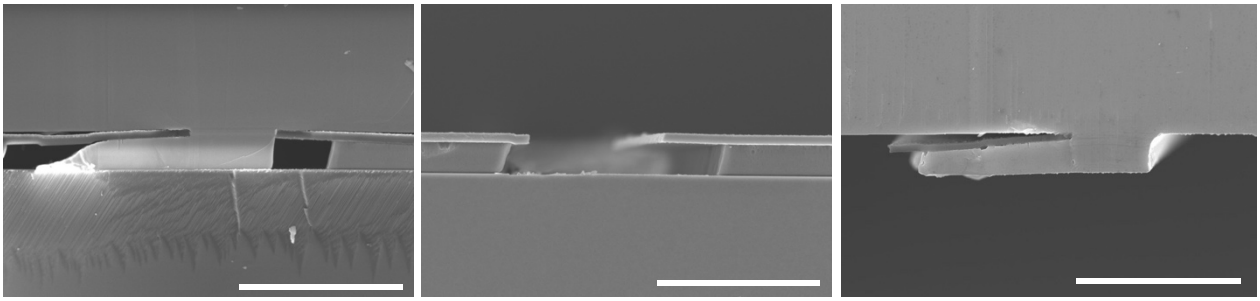

Figure 5.4 Cross-sectional SEM images showing the details of the adjoining part between the GaN active layer and the mask-patterned parent substrate.

(a) GaN root structure buried inside the space enclosed by the mask layers on the parent substrate, scale bar: 5 μm. (b) Mask layers on the parent substrate after the GaN layer was fully detached, scale bar: 5 μm. (c) Cross-section view of the ridge-like surface protrusion on the AS-GaN substrate surface which previously was the GaN root in (a), scale bar: 5 μm.

A set of SEM images in Fig.5.4 offered detailed descriptions of the adjoining part between the GaN active layer and the mask-patterned parent substrate. Before the separation (Fig. 5.4(a)),

the root-like GaN structure was buried inside the space enclosed by the mask layers. The bright region indicated the strong chemical-bonded GaN-sapphire interface. The area ratio of this bonded interface was quite small against the larger GaN-SiN_x mask interface containing air or vacuum gap, which explained the smooth post-separation surface morphology of the GaN layer. After the high-temperature growth, thermal stress built up during cooling provided sufficient driving force to break the limited-area chemical bonded GaN-sapphire interface. As a consequence, after unloading the sample from growth chamber, the GaN active layer-integrated host substrate was able to entirely detach from the parent substrate with minor mechanical force. Furthermore, the shape of surface protrusions faithfully represented the former GaN root buried inside the serpentine-like channel (Fig. 5.4(c)), whereas the $SiN_x/SiO_2/SiN_x$ mask layers remained largely intact except that the suspending end of the top SiN_x layer was carried away by the GaN root as it detached from the host substrate (Fig. 5.4(b)).

The GaN substrates of varying dimensions (2.5mm×4mm×0.45mm, 10mm×10mm×0.40mm, and 16mm×16mm×0.26mm) were completely released from the mask-patterned sapphire substrates (thickness: 420 μm) of equal size, as shown in Fig. 5.5(a), 5.5(b) and 5.5(c), respectively. The largest square size allowed in the 1 inch-diameter growth reactor is 18mm×18mm. It was found that with the thickness of GaN host substrate increased, the degree of transparency decreased due to opaque polycrystalline GaN deposited during HVPE growth. However, the mirror-like surface was invariantly achieved on the integrated active layer side irrespective of large-area polycrystalline GaN and uneven surface on the opposite side. Furthermore, thicker host substrate tends to be crack-free after separation, as seen in Fig 5.5(a) and 5.5(b). These facts proved a good scalability of the method which suggested that a GaN substrate of greater size is readily obtainable in a large-scale growth reactor with just a modicum of effort to optimize growth condition.

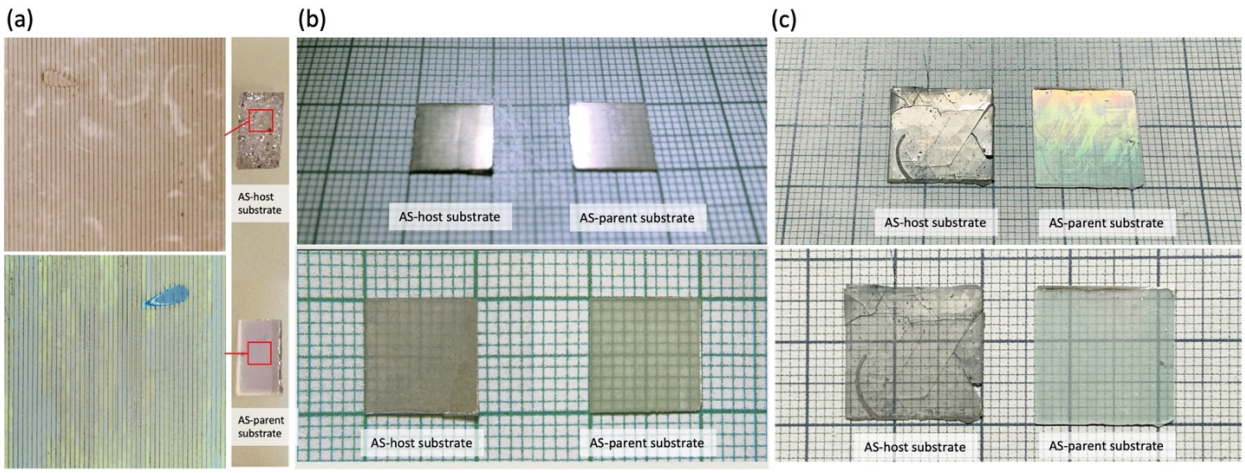

Figure 5.5 A set of real photos showing (a) 2.5mm×4mm×0.45mm, (b)10 mm×10mm×0.40mm, and (c) 16mm×16mm× 0.26mm GaN substrates with integrated active layer that were fully released from the diced mask-patterned sapphire substrates (thickness: 0.42 mm) of equal size. In addition, for (a): Upper left image: the top-view (-c plane) OM image of the AS-face of the active layer-integrated GaN substrate, where the periodic dark lines are the ridge-like surface protrusions and a few cloudy patterns indicate polycrystalline GaN deposited on the opposite side during HVPE stage. Lower left image: the corresponding mirror-symmetrical AS-face (+c plane) of the mask-patterned parent substrate, where the periodic dark lines indicate the corresponding openings in the mask layer. The area range of the above two OM images is 1 mm×1mm.

5.2.3 Repeating Laterally Patterned *p-n* Junctions

The morphology and dopant contrast were observed by using field-emission scanning electron microscopy (Hitachi SU9000 and Hitachi SU4300) operated at 10 kV. The fluorescence microscopic imaging was performed on an optical microscope (Nikon LV150A) with mercury lamp illuminator (Nikon intensilight C-HGFI, wavelength 380nm).

The top view (-c plane) of the AS-active layer surface with selective-area doping profile was revealed by the SEM image in Fig. 5.8(a). The bright white regions were p-type GaN due to the dopant contrast of secondary electron imaging [14], [15]. The repeating unit can be clearly

identified which consists of a pair of regular bright stripes indicating neighboring MOVPE-p-type regions as well as an irregular grey stripe indicating the ridge-like surface protrusion. On the other hand, the same sample was subject to a mechanical polish process to flatten the rough surface on the backside, followed by a chemical mechanical polish (CMP) process to remove the frontside surface protrusions. The surface roughness before and after the CMP process can be seen in Fig. 5.6 (a) and (b), respectively. Also, the surface morphology of the backside of the substrate before and after the mechanical polishing can be compared in Fig. 5.7(a) and (b).

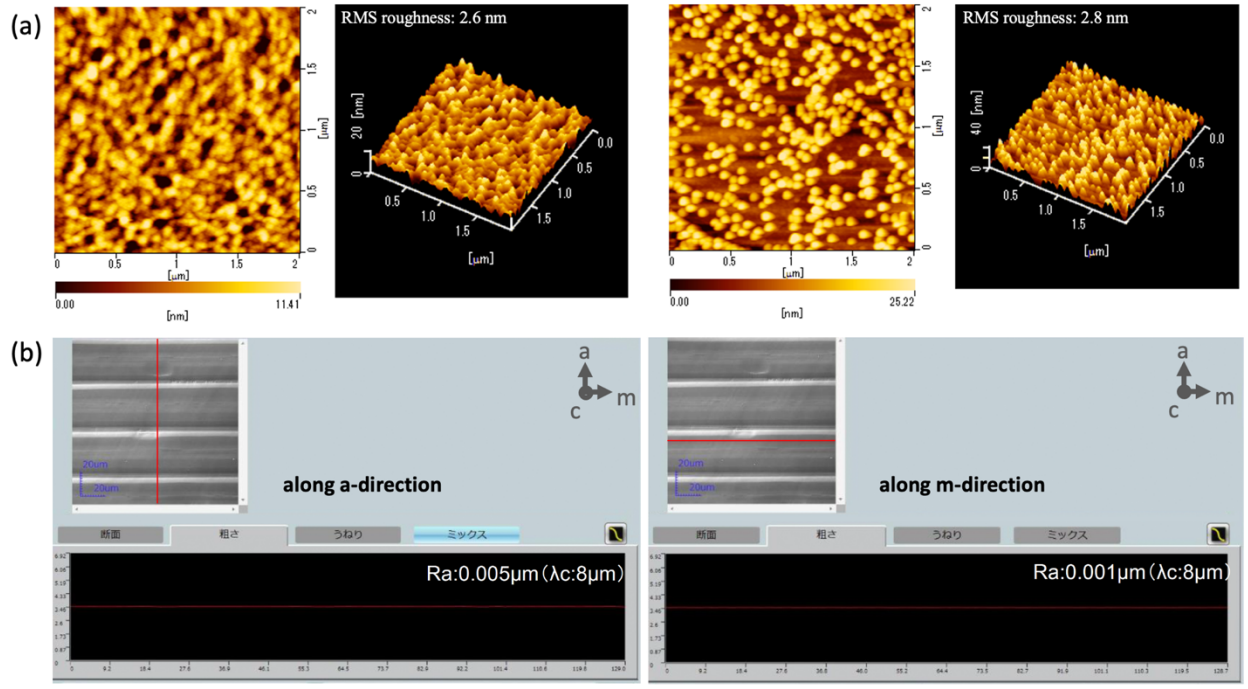

Figure 5.6 (a) The plan-view and 3D-view atomic force microscopic images of the as-separated $(000\bar{1})$ GaN surface, in which two locations were randomly selected. (b) The surface roughness measurement results of the as-chemical mechanical polished $(000\bar{1})$ GaN surface along a-direction and m-direction by confocal laser scanning microscopy.

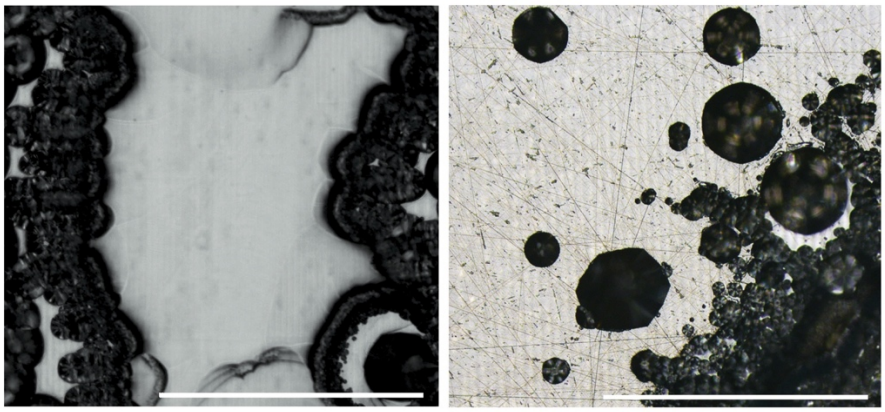

Figure 5.7 The microscopic images of the backside of substrate before and after the mechanical polish process.

(a) The optical microscopic image (scale bar: 1 mm) showing the typical morphology of the backside (0001) of GaN host substrate featuring rough surface and mixture of single-crystalline GaN and poly-crystalline GaN. respectively. The single-crystalline GaN was semi-transparent and the periodic protrusion stripes on the front side ($000\bar{1}$) were viewable and the polycrystalline GaN was opaque. (b) The optical microscopic image (scale bar: 1 mm) showing the backside (0001) of GaN host substrate by mechanical polishing. The surface was flattened and polishing scratches can be observed. The polycrystalline GaN was also heavily n-type doped which imposed negligible influence on the fabrication and performance of the vertical electronic devices.

The top view (-c plane) optical fluorescence microscopic image in Fig. 5.8(b) shows the as-polished active layer surface. On the other hand, the width and relative position of blue stripe pairs in Fig. 5.8(b) exactly match those bright white stripes pairs in Fig. 5.8(a), mutually verifying that these stripe pairs were p-type GaN: Mg regions and confirming that the surface consists of ultra-long repeating laterally-patterned p-n junctions. Furthermore, a few prismatic stacking faults induced during the imperfect MOVPE growth of GaN stripes were also identifiable in the fluorescence image. These features thus demonstrated the effectiveness of fluorescence

microscopic imaging in the dopant mapping with sufficiently good spatial resolution. Lastly, the integrity of the stripe-like doping pattern again proves the perfect bottom-up epitaxial layer transfer process.

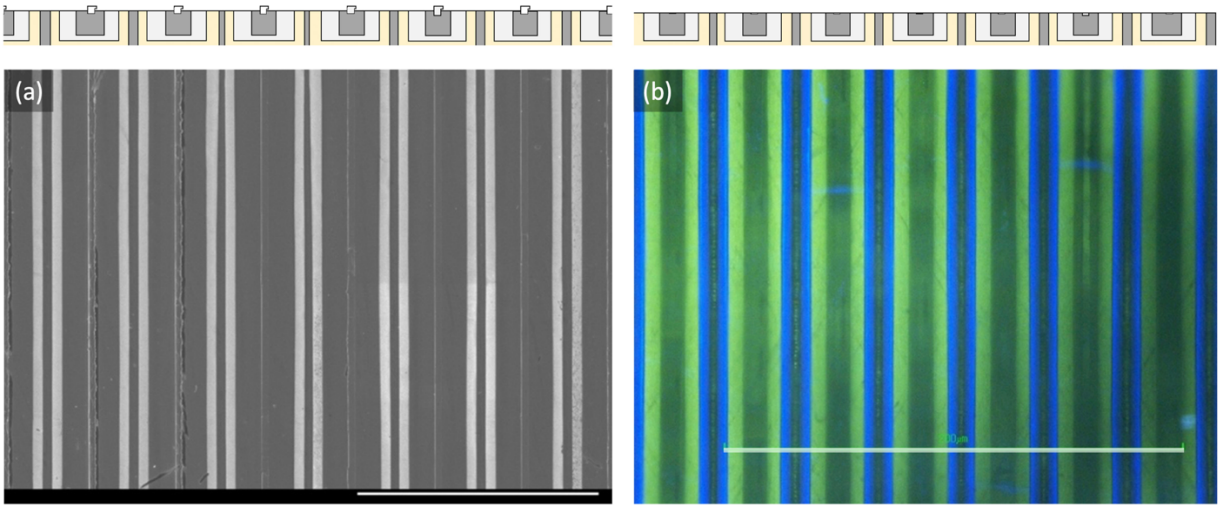

Figure 5.8 Top view (-c plane) scanning electron microscopic image (scale bar: 100 μm) of the AS-GaN substrate. Smooth surface morphology with periodic ridges can be observed and the repeating lateral p-n junctions are revealed due to dopant contrast of secondary electrons. The corresponding cross-sectional schematic is drawn above the SEM image. (b) Top view (-c plane) fluorescence microscopic image (scale bar: 200 μm) of the as-polished GaN substrate surface on which the ridges were removed. The natural color of the emitted visible fluorescent light from different doping regions can be clearly distinguished. The corresponding cross-sectional schematic is drawn above the FM image.

5.3 Normally-off Vertical MOSFETs

5.3.1 Overview

The GaN substrate with integrated active layer featuring repeating p-n junctions enables or facilitates the fabrication of a series of state-of-the-art electronics and optoelectronics. A normally-off vertical power MOSFET is an example whose vertical device architecture can also

comprehensively evaluate both the active layer and bulk GaN substrate. The cross-sectional schematic of the double-gated n-channel vertical MOSFET is shown in Fig. 5.9. Specifically, the demonstration of p-well due to a simple flip-over process of the as-grown half-core-shell p-n structure allows for a standard planar gate architecture preferred over an otherwise recessed-gate architecture.

For GaN MOSFET structure, a trench gate (also referred to as grooved gate) is the only type of gate geometry that has been demonstrated. Fundamentally, it serves as a compromise to allow the gate to access the otherwise buried p-GaN channel. However, the shortcomings of such geometry are apparent. First, the damages caused by dry etch on the trench sidewalls along which leakage paths proliferate, are hard to recover. Furthermore, the induced nitrogen vacancies simply alter the surface p-GaN into n-GaN, which is disastrous for a MOS structure [16], [17]. Plus, the electric field greatly intensifies at the bottom of trench corners where the radius of curvature is small, further adding risks to premature breakdown failures [18]. These reasons make a MOSFET built on vertical p-n junctions less superior than one built on lateral junctions. Once the lateral junction geometry is achieved, the exposed p-GaN would then allow for a much simpler planarized gate without resorting to a troublesome trench. Therefore, ion implantation, a solution considered as closest to realizing vertical p-n junction geometry, has been receiving numerous research interest and efforts in recent years. Despite being promising, currently it is still haunted by serious issues such as lattice damages caused by high-energy ion bombardment and associated point defects. As a result, there has been little report on the successful demonstration of ion implantation-enabled MOSFET in the literature.

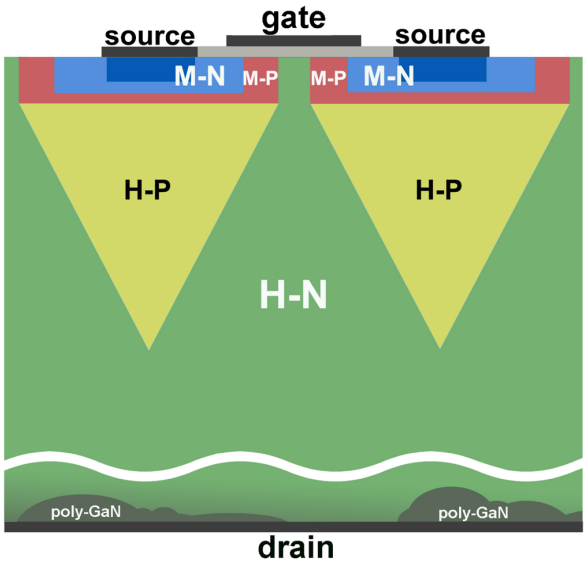

Figure 5.9 Cross-sectional schematic illustration of the structure of a normally-off planar-gate vertical MOSFET fabricated on the GaN substrate.

5.3.2 Device Fabrication

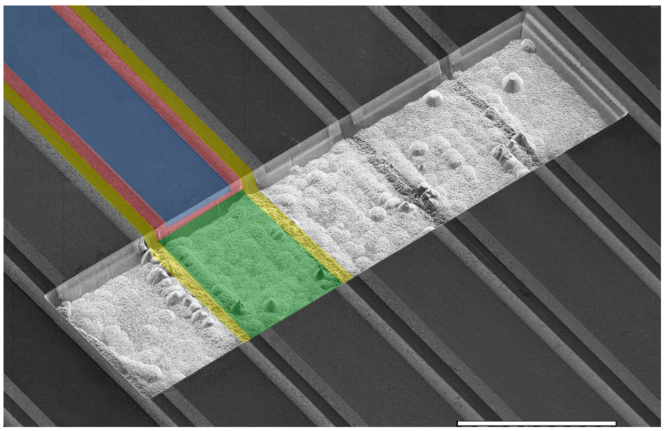

Figure 5.10 The angled-view SEM image (scale bar: 50 μm) showing the doping regions and the trench used for device isolation and pad support before deposition of oxide, metal, and polyimide filling. The MOVPE-n-type, MOVPE-p-type, HVPE-n-type and HVPE-p-type doping regions in a repeating unit are manually coloured in semi-transparent blue, red, yellow, and green, respectively.

After the GaN sample was subject to a simple cleaning process, the square trenches on the sample surface were created via Cl_2-based dry etch in an ICP-RIE system (model: SAMCO RIE-200iP NXT) for isolation where a hard mask consisted of 200 nm Ni was deposited by electron-beam evaporation. In order to isolate devices, the trenches on the nitrogen-terminated sample surface were formed by a combination of dry etch and wet etch. The depth was over 10 μm to ensure the MOVPE-n-type region (source region) was fully exposed and isolated, as shown in Fig. 5.10. Meanwhile, the exposure of previously-buried MOVPE-p-type region also facilitated the subsequent Mg activation. In the final stage of device fabrication, polyimide was filled in the trenches for surface flattening and pad placement.

The sample was then subject to a hot 25% TMAH solution wet etch for plasma damage recovery where the top hard mask of Ni was maintained for N-face GaN protection. After a removal of Ni, the sample was annealed in an RTA furnace (Yonekura MIR-HP) at 850 °C and 1 hr. for Mg activation. A Ti/Al/Ni/Au (20nm/120nm/20nm/200nm) was then evaporated onto the M-N region on the surface as source contact, followed by RTA annealing (in nitrogen, 5 min at 650 °C) to improve n-type Ohmic contact. After that, a SiN_x of ~1-2 nm was deposited via sputtering (ULVAC ACS-4000) followed by a deposition of amorphous Al_2O_3 of 50 nm by atomic layer deposition (ALD). Post deposition annealing was carried out by 450 °C for 1 hr. Wet etch by a dilute HF solution was then used to expose openings for source contacts. A Ni/Au (20nm/100nm) was evaporated onto the oxide as gate metal followed by post-metallization annealing (N_2 atmosphere, 1 hr. at 350 °C). To flatten the trenches for pad placement, polyimide was filled and thermally cured. Ni/Au was evaporated onto the polyimide-flattened trenches for contact pads. Al (thickness ~180nm) was sputtered (ULVAC ACS-4000) onto the flattened backside of the n-type GaN substrate for drain contact.

Figure 5.11 shows a top-view fluorescence microscopic image of the fabricated transistors. The relative position of the metal contacts appearing as pitch black due to complete fluorescence absorption can be distinguished against that of the underlying GaN doping regions in blue- or green-color fluorescence. For each transistor, the metal gate spans over a double-channel consisting of a pair of MOVPE-p-type regions, whereas the source contact pair was deposited on the neighboring MOVPE-n-type regions and adjoined to a large pad on the polyimide-flattened trench. The drain contact was deposited over the entire backside of the n-type GaN substrate.

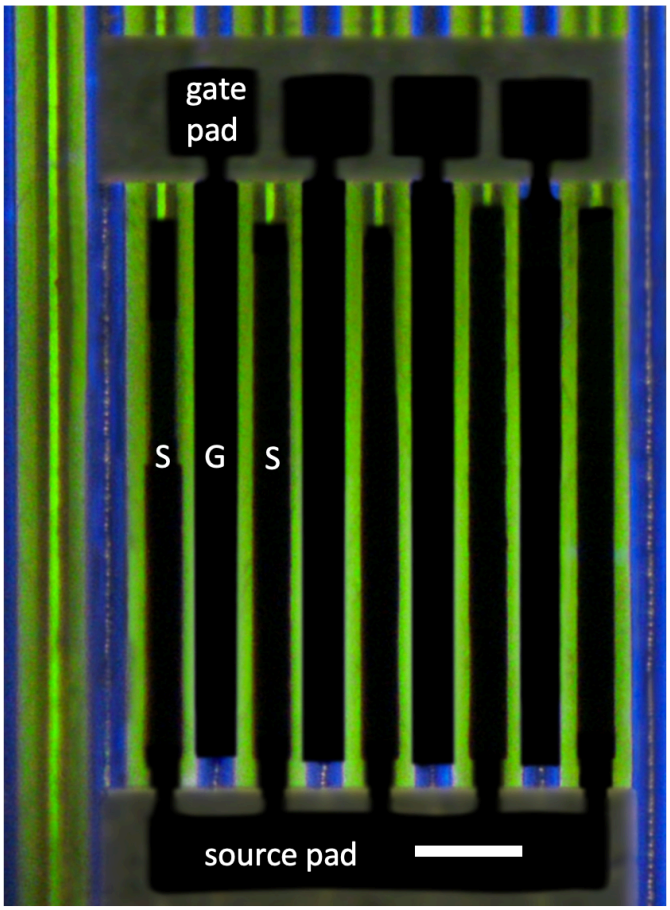

Figure 5.11 Top-view (-c plane) of the fluorescence microscopic image (scale bar: 36 μm) of the MOSFET fabricated on the GaN substrate, where the relative position of metal source, gate and pad (pitch black) against p-type (blue) and n-type (light and dark green) regions can be

distinguished. Gate pad and source pad were deposited on the polyimide-filled trenches, respectively.

5.3.3 Electrical Characterization

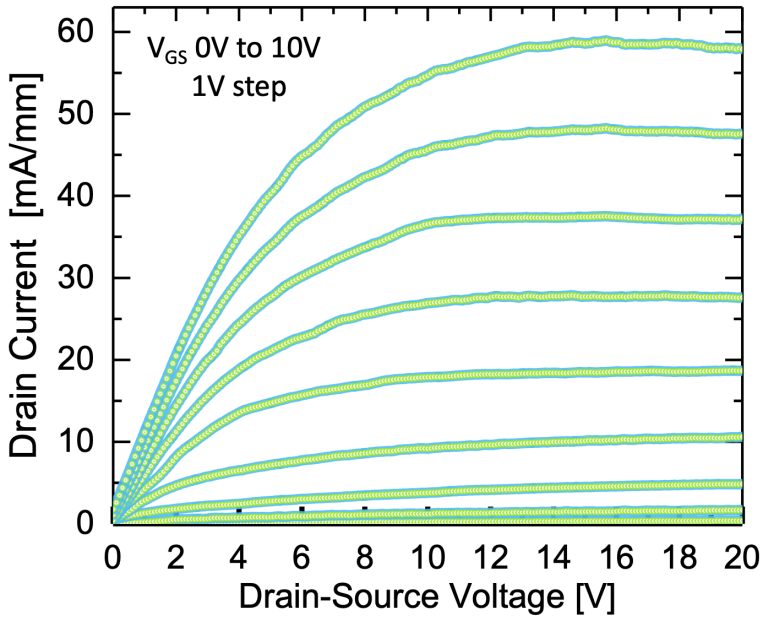

Figure 5.12 The I_{DS}-V_{DS} characteristics of the MOSFET where V_G ranged from 0V to 10V.

The output and transfer characteristic curves of the transistor are shown in Fig. 5.12 and 5.13, respectively. Besides, the extracted field-effect mobility μ_{FE} was plotted against V_G in Fig. 5.14 when a small V_{DS} of 0.5V was applied, based on the following equation [30]:

$$\mu_{FE} = \frac{g_m L}{ZC_0 V_{DS}} \text{ and } g_m = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)\Big|_{V_{DS}=\text{const}} \quad (5.1)$$

where the channel width Z=2×190=380 μm, the channel length L=4 μm, the gate oxide capacitance per unit area C_0 (F/cm^2) = 9 (arb. unit) ×8.854×10^{-14} (F/cm)/50 (nm), and V_{DS}=0.5V, and g_m is transconductance. The peak value of μ_{FE} was found to be 42 cm^2/V. s in Fig. 5.14, serving as a good value among inversion channel mobility of GaN despite conceivably significant Coulomb scattering by the charged Mg and Si ions, which also implied that a further enhancement of μ_{FE} by several times is reasonably expected with lowering [Mg] and compensating [Si] in p-GaN.

To conveniently evaluate the on-off current ratio and threshold voltage, the drain current I_{DS} was plotted in both semilogarithmic and linear scales in Fig. 5.13 and Fig. 5.14, respectively. An on/off ratio of over 10^8 and a threshold voltage of 3.8V were achieved, indicating a good normally-off transistor action. The high on/off ratio suggested that leakage paths were effectively suppressed. The low value of threshold voltage was likely explained by a combination of factors including the compensating donors of Si in p-GaN, the plasma treatment to p-GaN surface along SiN_x sputtering [19], and the intrinsic properties of nitrogen-terminated GaN surface [20].

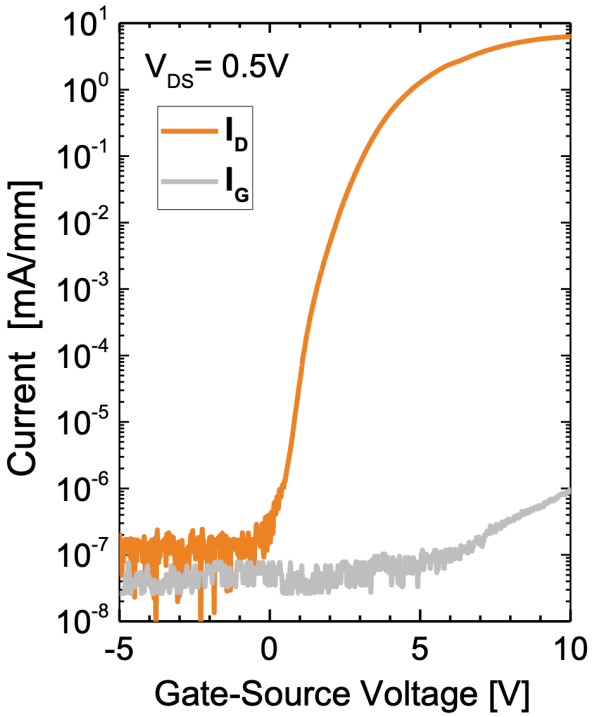

Figure 5.13 The I_{DS}-V_{GS} characteristics of the MOSFET where V_{DS} was 0.5 V, plotted in semilogarithmic scale.

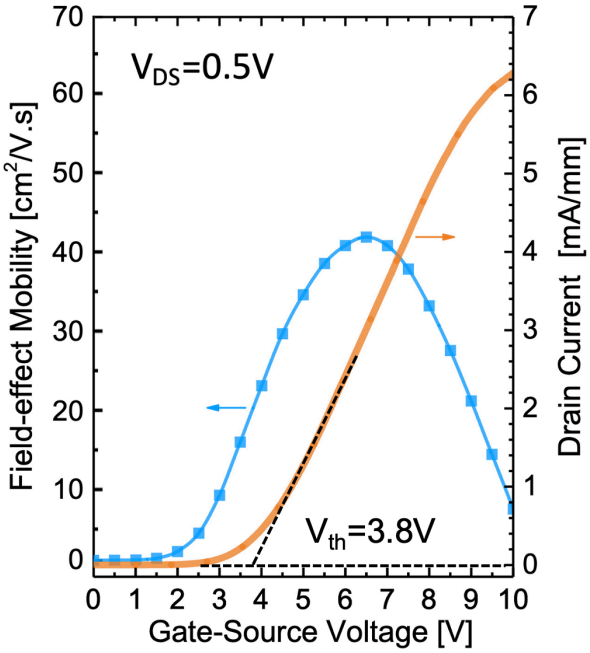

Figure 5.14 The I_{DS}-V_{GS} characteristics and the field-effect mobility μ_{FE}-V_{GS} curve, plotted in linear scale.

Also, the I_{DS}-V_{DS} curves under a set of V_{GS} in the linear region of the MOSFET (V_{DS} less than 5V) were plotted in Fig. 15 with the specific on-resistance R_{ON}-V_{DS} curve. The minimal R_{ON} was found to be 7.8 mΩ.cm² at a V_{GS} =15V and V_{DS} around 2V. The resistance can be further reduced by optimizing the device design, such as shortening the channel length L to commonly-employed sub-micrometer scale to reduce the channel resistance, and narrowing the length of MOVPE-n-type core region (source region) to optimize the effective device area. Despite the design yet to be optimized, the good device operation confirmed the successful integration of selective-area doped active layer into the native conducting substrate by the bottom-up epitaxial layer transfer process. Furthermore, it was also the demonstration of WBG semiconductor electronic device in which the selective-area doping profile was created without resorting to either ion implantation or etch-and-regrowth approach.

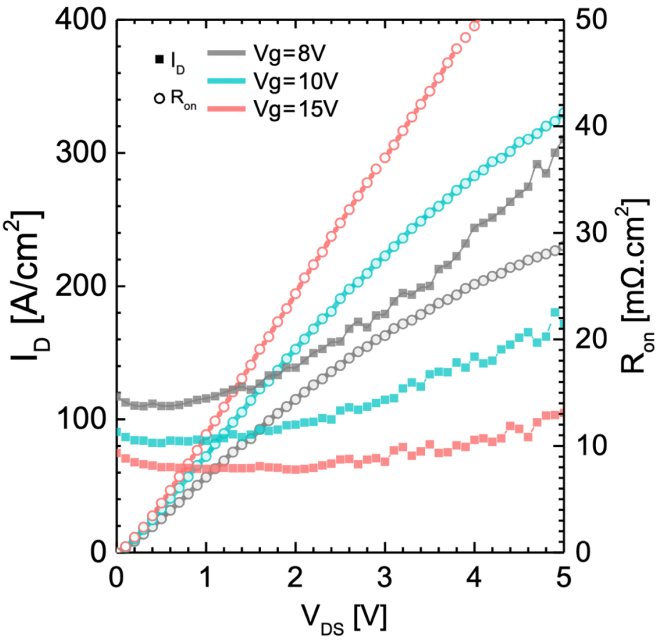

Figure 5.15 The I_{DS}-V_{DS} and R_{ON}-V_{DS} curves under a set of V_{GS} in the linear region of the MOSFET where V_{DS} ranged from 0V to 5V, and the minimal R_{ON} was found to be 7.8 mΩ.cm^2 at V_{DS} around 2V and V_{GS}=15V.

5.4 Summary

In brief summary, in this Chapter, a versatile and scalable bottom-up epitaxial layer transfer approach was discussed as a viable path to simultaneous demonstration of a large-scale native WBD semiconductor substrate as well as the desired functionality of built-in selective-area bipolar doping patterns. Relied on the mere epitaxy growth, the GaN active layer with hundreds of repeating lateral deep p-n junctions was grown from foreign insulating substrate and then seamlessly transferred to native n-type substrate. The substrate has intrinsically mirror-like surface on the active layer side, despite rough surface on the opposite side having mixture of single-crystalline and polycrystalline GaN that did not impede the fabrication or degrade the performance of the vertical devices fabricated on the n-type substrate product. The unique bipolar doping profile rendered the utilization of several dopant distribution mapping techniques of which the

independent results verify each other well. The functionality of such substrate product led to the first demonstration of a MOSFET on the $(000\bar{1})$ GaN as well as the first demonstration of a WBG semiconductor device where the selective-area doping profile was created without ion implantation or etch-and-regrowth approach.

5.5 References

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Chapter 6

Selective-area Doping by Anisotropic Diffusion of Mg

6.1 Quantitative Mapping of Elements, Dopants and Carriers

6.1.1 Challenge for Quantitative Characterization of Selective-area Doping

In the preceding Chapter, selective area doping profile was obtained in the GaN substrate by epitaxy-enabled substrate transfer and in situ doping process. The surface doping profile featuring repeating laterally patterned p-n junctions was qualitatively characterized by scanning electron microscopy and fluorescence microscopy. However, it is also important to quantitatively or semi-quantitatively investigate the distribution, if possible, of the dopant and carrier in order to gain deeper understanding of the incorporation tendency of unintentional impurities and the doping efficiency of intentional donors/acceptors.

However, it is quite challenging to characterize the doping concentration with high spatial resolution [1]. In fact, there is a well-known trade-off between the analytical spot size and the detection range for a characterization technique. Fig. 6.1 summarizes the common characterization techniques by their limitations of the detection range and the analytical spot size [2]. In addition, the fundamental physical limits of the detection range versus analytical spot size under several sampling depths (0.3 nm, 3 nm, and 30 nm) are indicated by a group of parallel solid lines, respectively.

The physical origin of such these limits can be understood in such a way: take the sampling volume of GaN with dimensions of 0.3 nm sampling depth and 100 nm spot diameter for instance, the corresponding sampling volume is 2400 nm^3 which should contain 1.0×10^5 GaN molecules if the density of GaN is taken as 4.4×10^{22} molecules/cm^3, therefore the physical limit of the detection

range should be to detect a single impurity atom in every 1.0×10^{5} GaN molecules, making the detect range limit to be $(1/1.1\times10^{5})\times4.4\times10^{22}\approx4.4\times10^{17}$ cm^{-3}.

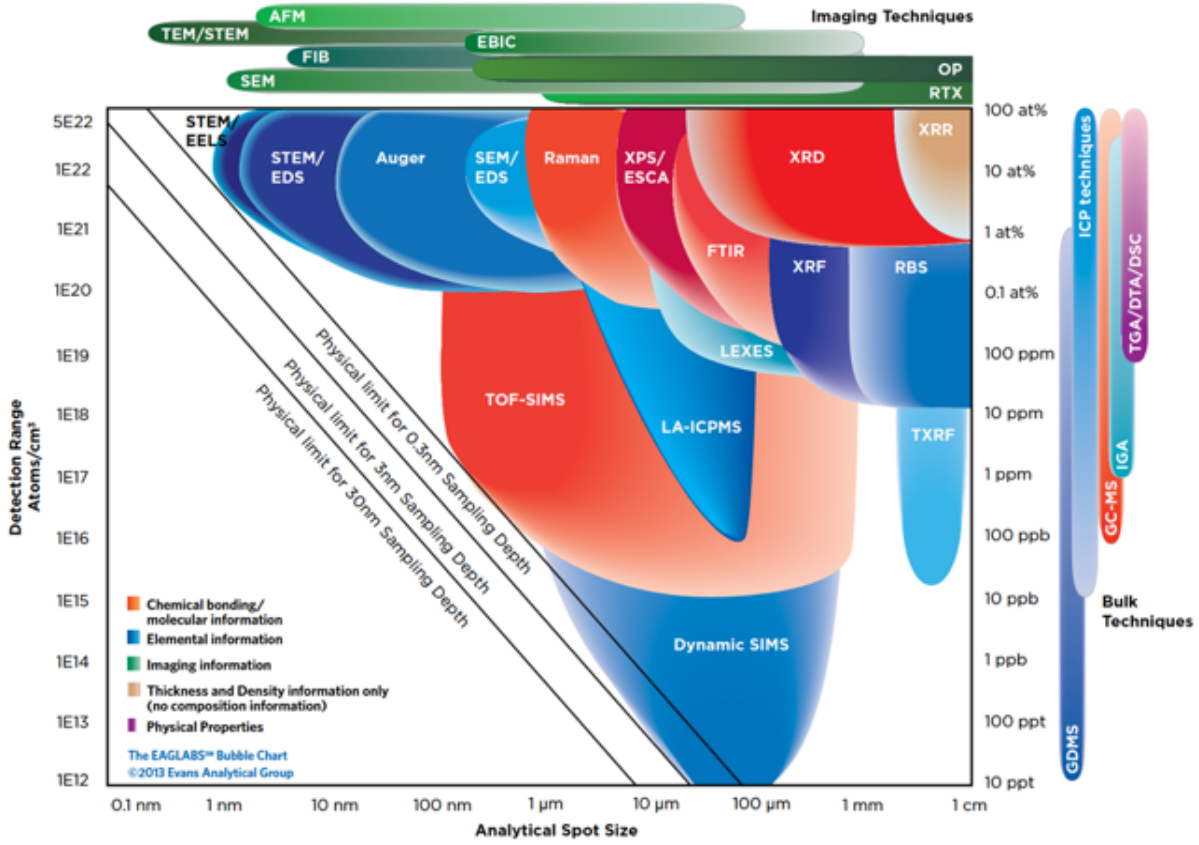


Figure 6.1 A summary of the characterization techniques characterized by their limitations of the detection range and the analytical spot size (image courtesy of Evans Analytical Group [2]).

6.1.2 Cross-sectional Elemental, Dopant, and Carrier Mappings

A two-dimensional dopant and carrier mappings of the selective area doping profile in the GaN substrate obtained by epitaxy-enabled substrate transfer approach were carried out by using scanning non-linear dielectric microscopy (SNDM) and scanning microwave microscopy (SMM) for p-n polarity imaging and carrier concentration imaging, respectively. SNDM and SMM are based on the scanning probe microscopy techniques like atomic force microscopy (AFM) and scanning capacitance microscopy (SCM). SPM measurement is uniquely suited to providing

information about both structural morphology and electronic properties of semiconductor epitaxial layers and device structures with a spatial resolution on the order of ~1–100 nm.

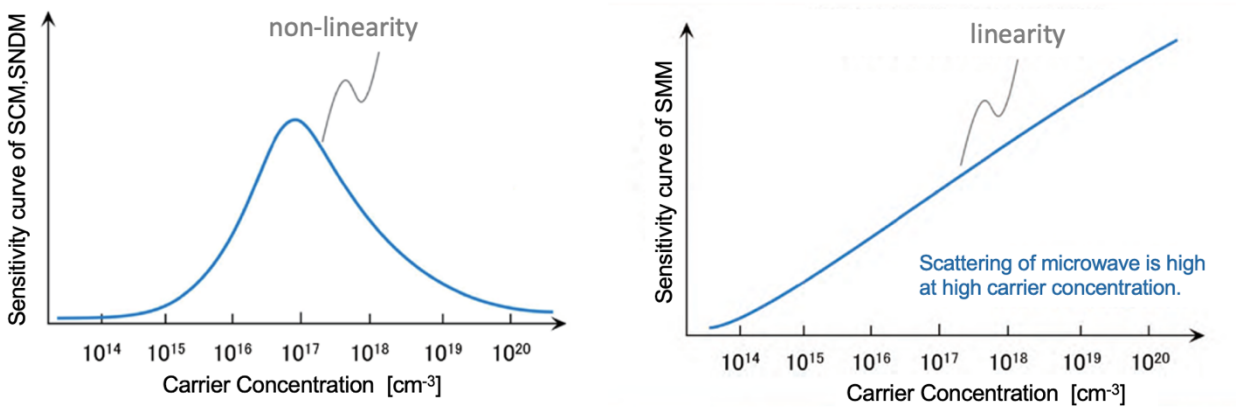


Figure 6.2 The comparison of SNDM (or SCM) and SMM in their sensitivity versus carrier concentration.

Similar but different to SCM which only collects the localized signals of $\frac{\partial C}{\partial V}$ (linear term) related to charged dopant and carrier concentration, SNDM also collects higher-order signals of changes in electrostatic capacitance (non-linear terms like $\frac{\partial^2 C}{\partial^2 V}, \frac{\partial^3 C}{\partial^3 V}\ldots$) right underneath the probe as the resonance frequency of the semi-microwave oscillator approximate 1GHz by FM modulator, while applying an alternating current (V_{AC}) between the probe and sample [3], [4]. In such a way, semiconductor carrier distribution and ferroelectric polarization domain can be observed. Compared to SCM which has a detection range of 10^{15}–10^{20} cm^{-3}, the SNDM has a broader detection range of 10^{14}–10^{20} cm^{-3} due to its higher sensitivity. On the other hand, SMM collects the localized scattered microwave signals of dS_{11}/dV_{tip} related to carrier concentration [5], [6]. In comparison, the SNDM is capable of recognize p/n polarity and has peak sensitivity in the detection of middle-range carrier concentration (~10^{17} cm^{-3}) which decreases toward both heavy- and light-range directions. By contrast, the SMM is incapable of recognize p/n polarity but has

better quantitative analysis capability since the sensitivity and signal intensity has a good monotonous and linear relation with increasing carrier concentration. The sensitivity of SNDM and SMM is compared schematically in Fig. 6.2. Therefore, the two SPM techniques are be complementary to each other. The SNDM and SMM employed in this work feature the detection range of 10^{14}-10^{20} cm^{-3} and 10^{14}-10^{21} cm^{-3}, respectively.

The SNDM was measured on a common platform (Hitachi High-tech AFM5000 II) along with AFM measurement (conductive probe, radius curvature: 20–40 nm) and the SMM is measured in couple with Keysight Technologies 5600LS (Pt Probe, radius curvature: 10 nm).

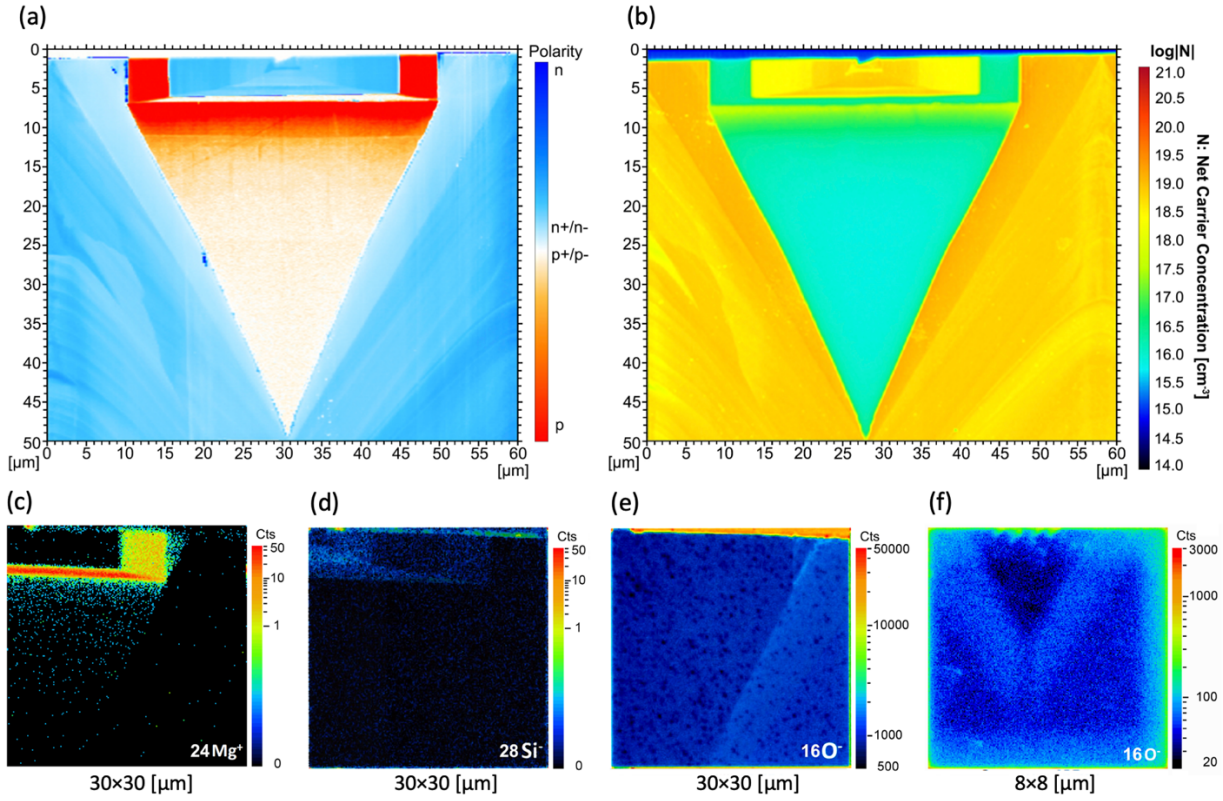


Figure 6.3 Cross-section view (m-plane) of the dopant, carrier, and elemental mappings of a repeating unit in the active layer: (a) scanning non-linear dielectric microscopic mapping showing the polarity (n/p) of the charged dopant species in each doping region. (b) scanning microwave

microscopic mapping showing the absolute carrier (n/p) concentration in each doping region. (c)-(f) NanoSIMS mapping showing the elemental distribution of Mg, Si and O atoms, respectively.

Fig. 6.3(a) and Fig. 6.3(b) show the cross-sectional SNDM and SMM mapping results, respectively. The polarity of the doping regions can be concluded from Fig. 6.3(a) that each repeating unit of the doping profile is characterized by an MOVPE-grown n-type (M-N) core region, surrounded by an MOVPE-grown p-type (M-P) shell region, and an HVPE-grown n-type (H-N) matrix region surrounding the MOVPE-grown square regions and also making up a majority part of GaN substrate. Furthermore, a triangular prism-like p-type (H-P) region beneath each discrete MOVPE-grown region was developed during HVPE growth. The carrier concentration of each region can be revealed in Fig. 6.3(b). It is seen that both M-N and H-N regions are heavily n-type doped with electron concentration above 10^{18} cm^{-3}. The M-P region has hole concentration mostly in the range of 5×10^{16} to 1×10^{17} cm^{3} and the H-P region has a hole concentration mostly around 1×10^{16} cm^{3} except that in the narrow area adjacent to M-P region the hole concentration experienced a diffusion-induced large gradience from 10^{18} cm^{-3} to 10^{16} cm^{-3} within a vertical distance of 5-6 μm.

In addition to the dopant and carrier mapping results, the two-dimensional elemental mapping and one-dimensional line scanning were carried out by CAMECA NanoSIMS 50L. Cs^{+} and O^{-} primary ion beams were used for the detection of C, O, Si (negative secondary ion) and Mg (positive secondary ion), respectively. NanoSIMS (Nanoscale secondary ion mass spectrometry) is an analytical instrument manufactured by CAMECA which operates on the principle of dynamic secondary ion mass spectrometry. The NanoSIMS is used to acquire nanoscale resolution measurements of the elemental and isotopic composition of a sample and the NanoSIMS is able to create nanoscale maps of elemental or isotopic distribution, parallel acquisition of up to seven

masses, isotopic identification, high mass resolution, subparts-per-million sensitivity with spatial resolution down to 50 nm, making it approach the physical limit described in Fig. .6.1

To our best knowledge, there has been no report of NanoSIMS mapping for characterizing the doping of semiconductor in the literature in spite of a number of studies existed in the domain of materials science [7]. Fig. 6.3 (c)-(f) show the cross-sectional NanoSIMS mapping results of Si, Mg and O. In addition, the quantitative line scanning results of these elements can be found in Fig. 6.4 and Fig. 6.5. It can be confirmed that the dominant n-type dopant species in the M-N and H-N regions are Si_{Ga} and O_N, respectively, since the shape of distributions of Si and O well matches the corresponding M-H and H-N regions in Fig. 6.3(a) and Fig. 6.3(b). By the same token, the p-type dopant species in the M-P and H-P regions is Mg_{Ga}. The incorporation of Si in the MOVPE-grown region mainly came from the intentional introduction of dopant precursor SiH_4. In addition, it was also from the desorption of Si from the SiN_x mask during MOVPE growth, and this unintentionally doping source was responsible for the presence of Si in the M-P region. Instead, the incorporation of Si into HVPE-grown region was below the detection limit of NanoSIMS, most probably due to the deposition of polycrystalline GaN which covered the SiN_x mask (as shown in Fig. 5.3(a) in Chapter 5) and suppressed the desorption of Si into vapor phase during HVPE growth. The undetectable Si in the HVPE-grown region also accounted for the higher hole concentration in the small part of H-P region adjacent to M-P region than in the M-P region due to the compensating donor effect of Si in p-type GaN. Rather than Si, the high electron concentration in the H-N matrix region came from O-an impurity species commonly associated with HVPE (O is a rare impurity for MOVPE)[8]. The NanoSIMS mapping results also served as the first-time utilization of SIMS imaging technique for dopant distribution of a semiconductor material.

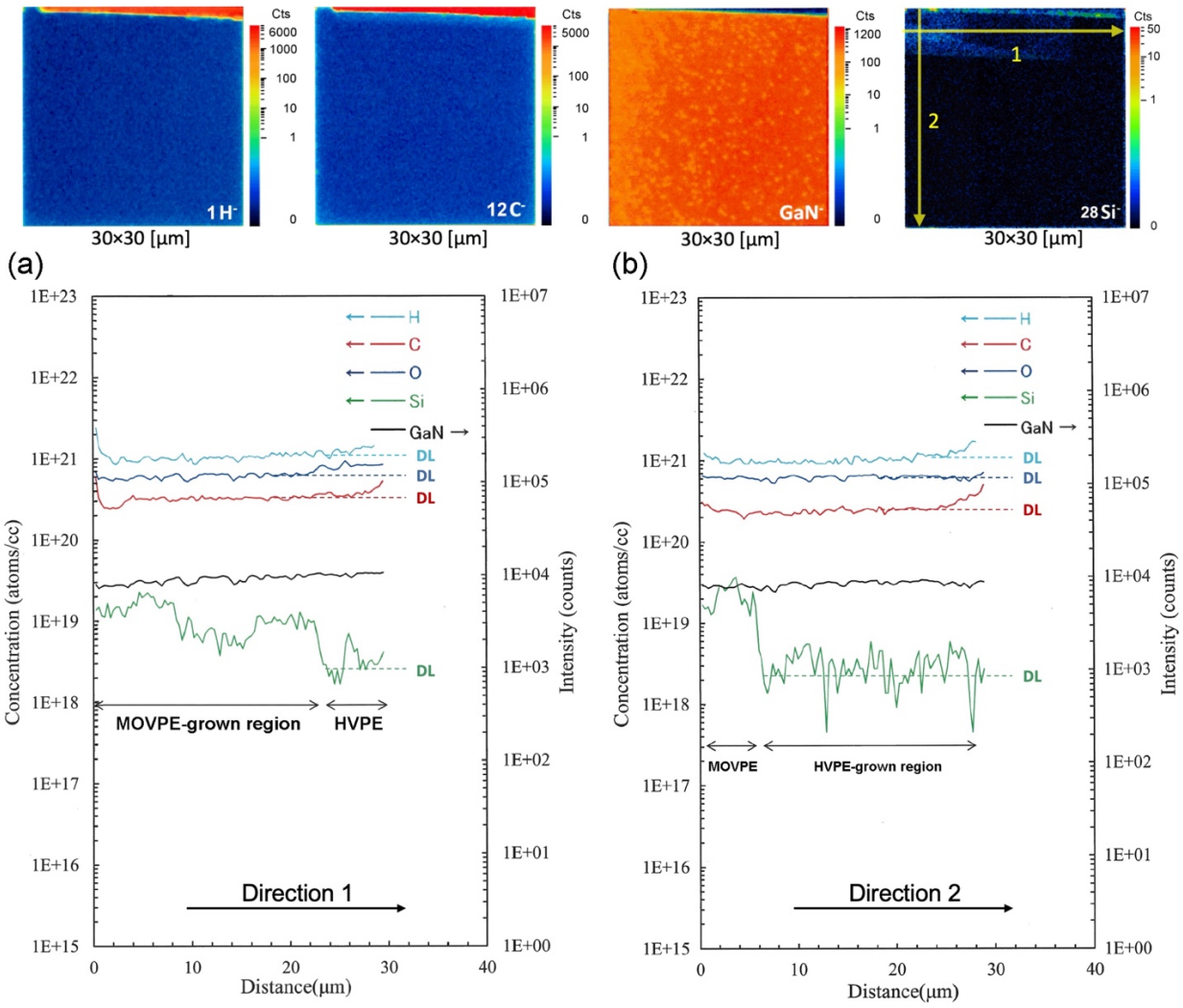


Figure 6.4 NanoSIMS mapping results of distribution of H and C, and the line scanning results of H, C, O and Si (the NanoSIMS mapping results of O and Si are shown in Fig. 6.3). Cs^+ primary ion beams were used for the detection of C^-, O^-, and Si^- secondary ions. (a) and (b): The line scanning results of H, C, O, and Si along the direction 1 (horizontal) and the direction 2 (vertical) indicated in the top right NanoSIMS mapping image (30 μm×30 μm), respectively. The scanning length is 30 μm. The detection limit (DL) of H, C, O elements are high due to the microscale sampling length and small atomic mass, so the concentration of H, C, O could not be detected. Si

has relatively lower detection limit (2-3×10^{18} cm^{-3}) and the concentration of Si in the MOVPE-grown region is detected whereas that in the HVPE-grown region is below the detection limit.

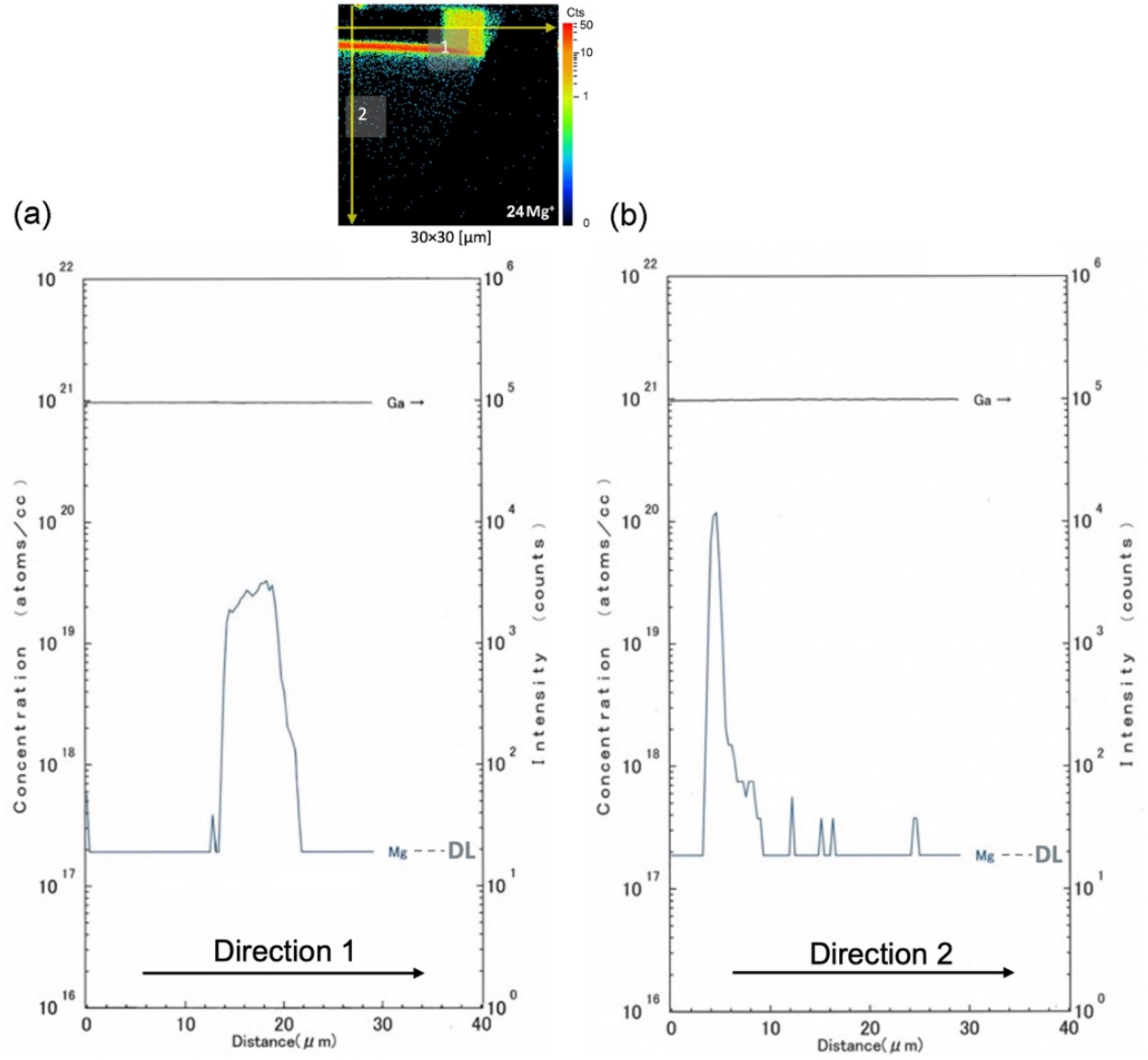


Figure 6.5 The line scanning results of Mg. O^- primary ion beams were used for the detection of Mg^+ secondary ions. The line scanning results of Mg along the direction 1 (horizontal) and direction 2 (vertical) indicated in the top NanoSIMS mapping image (30 μm×30 μm), respectively. The scanning length is 30 μm. Different levels of Mg incorporation in the M-P regions grown

along c-plane and a-plane are observed. The concentration of Mg above the detection limit (DL) of 2×10^{17} cm^{-3} in the H-P regions due to diffusion can be quantitatively revealed.

Fig. 6.3(c) also suggested that the Mg incorporated in the M-P region experienced a self-redistribution during the subsequently lateral overgrowth stage, most probably by diffusion since the home-made HVPE reactor has a strictly Mg-free environment before loading of the sample which was subject to the standard RCA cleaning (except using SC1 agent) before HVPE growth. The redistribution of Mg was apparently crystallographically defined, leading to the triangular prism-like H-P region bordered by (0001) and two $(22\bar{4}3)$ planes. Meanwhile, the time-of-flight (TOF) SIMS was also carried out to investigate the [Mg] in the H-P region (scan direction perpendicular to the page). The results and measurement condition is shown in Fig. 6.6, showing that the [Mg] in the upper triangular p-GaN region is 7×10^{16} cm^{-3}.

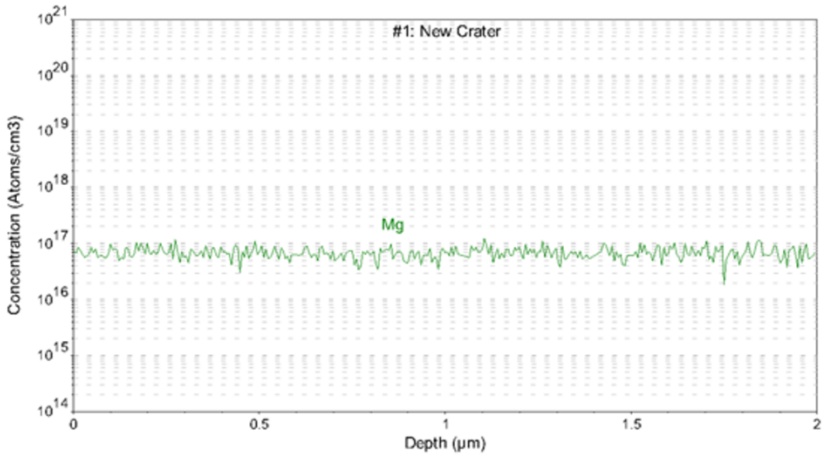


Figure 6.6 Time-of-Flight (TOF) SIMS result (scan direction perpendicular to the page) showing that the [Mg] in the upper triangular p-GaN region is 7×10^{16} cm^{-3}.

The fact that the lightly-doped H-P region further extended the p-n junction length by over 40 μm might show great promise in the design and application of state-of-the-art power electronics such as superjunction-based transistors, should the unintentional [O] in the H-N region were significantly reduced. The diffusion behavior of Mg along both c and a direction will be discussed in detail in the following section.

The hole concentration p, the acceptor concentration N_A, the compensating donor concentration $N_{D,\,comp}$ are internally tied by the principle of charge neutrality:

$$p + N_{D,comp}^{+} = n + N_A^{-} \tag{6.1}$$

It is reasonable to assume that n is negligible and the compensating donor is completely ionized. Then we have:

$$p + N_{D,comp} = \frac{N_A}{1+\frac{pg_A}{N_{V,eff}}\exp\left(\frac{\Delta E_A}{kT}\right)} \tag{6.2}$$

g_A is the effective degeneracy for the acceptor state:

$g_A = 2$ for heavy hole VB only,

$g_A = 2\sim4$ for heavy hole VB + light hole VB

$g_A = 4$ for weighing equally heavy hole VB and light hole VB

Here we adopted $g_A = 4$ throughout the calculation.

Furthermore, the ionization energy decreases with increasing the ionized acceptor as [9], [10]:

$$\Delta E_A = \Delta E_{A,0} - f.\,(N_A^{-})^{\frac{1}{3}} = \Delta E_{A,0} - f.\left(p + N_{D,comp}\right)^{\frac{1}{3}} \tag{6.3}$$

whereas $\Delta E_{A,0}$ =245 ± 20 mV [11] and

$$f = \Gamma\left(\frac{2}{3}\right)\left(\frac{4\pi}{3}\right)^{\frac{1}{3}}\frac{q^2}{4\pi\varepsilon_{GaN}} \tag{6.4}$$

Using the above equations, we may calculate the concentration of acceptor N_A based on the measured hole concentration. The compensating donor concentration is set at 2 $\times 10^{16}$ cm^{-3}. We used finite-element analysis to calculate N_A since there is no analytical solution to solve together Eqn. (6.2), Eqn. (6.3), and Eqn. (6.4). The calculated N_A is plotted in Fig. 6.7.

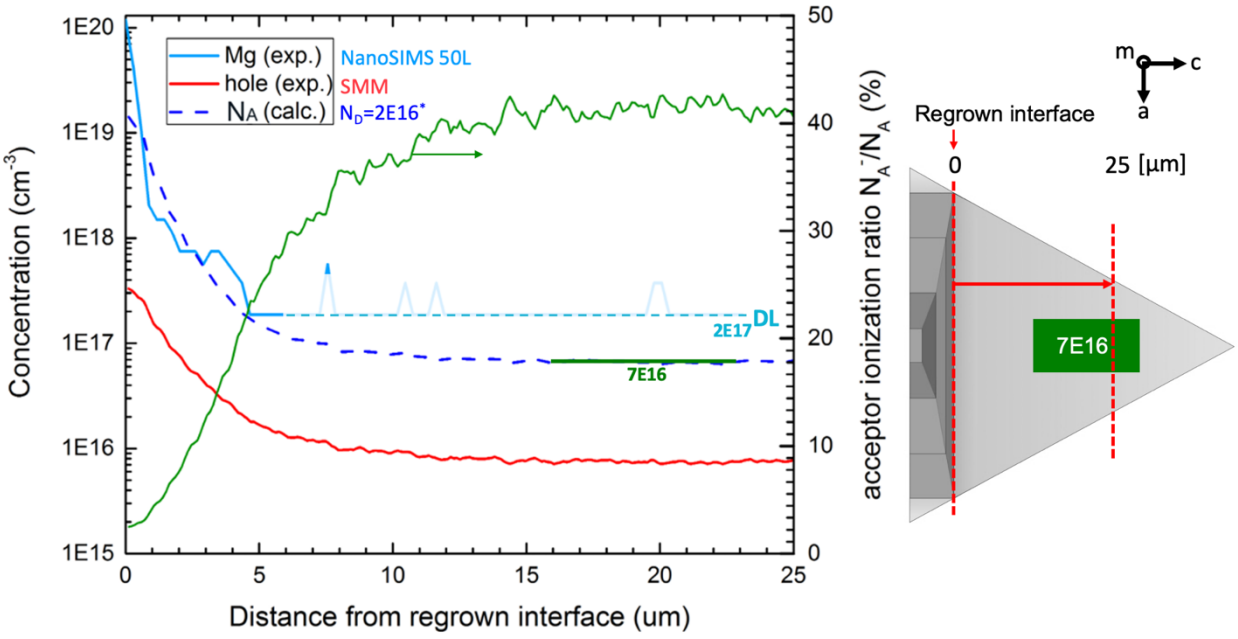


Figure 6.7 The distribution of [Mg] from the regrown interface measured by NanoSIMS 50L, the distribution of hole concentration measured by SMM and the distribution of acceptor concentration N_A calculated by the finite-element method with the compensating donor $N_{D,\,comp}$ at 2 $\times 10^{16}$ cm^{-3}. The regrown interface and the line scan path are indicated in the schematic illustration on the right.

It can be seen that the calculated N_A in the upper triangular region is reaching a plateau of 7 $\times 10^{16}$ cm^{-3}, which matches well with the value of [Mg] measured by the TOS-SIMS in Fig. 6.6. This is consistent with the fact that N_A=[Mg] in the lightly-doped p-GaN. The ionization ratio of acceptors (N_A^-/N_A) is around 30% in the lightly-doped p-GaN ($N_A \sim 10^{17}$ cm^{-3}) which decreases to 9% in the medium-doped p-GaN ($N_A \sim 10^{18}$ cm^{-3}) and further decreases to less than 3% in the heavily-doped p-GaN ($N_A \sim 10^{19}$ cm^{-3}). Furthermore, the ionization ratio should be slightly lowered

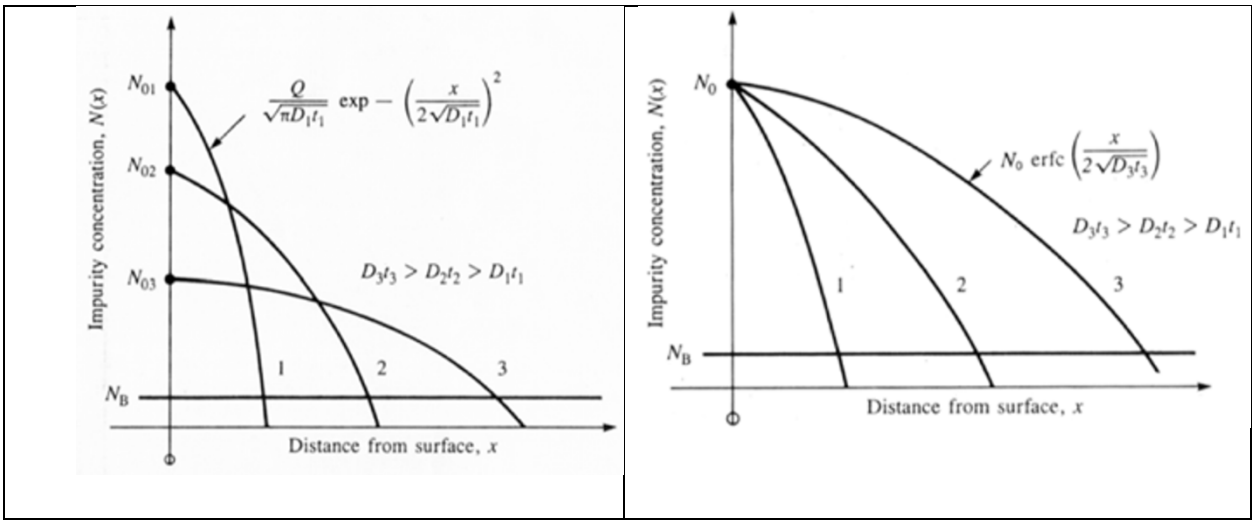
in the absence of the compensating donors. In the heavily-doped p-GaN ([Mg]~10^{20} cm^{-3}), the activation ratio of N_A/[Mg] drops considerably which is a common issue in the p-type doping of GaN due to segregation of Mg. The FEA-calculated N_A well matches the [Mg] measured by NanoSIMS and TOF-SIMS, suggesting a good correlation between the experimental data obtained with SMM and NanoSIMS results.

6.2 Modeling of Anisotropic Diffusion of Mg in ELO-GaN

In order to model the out-diffusion behavior of Mg from the M-P region during HVPE growth stage, let us first review the two important diffusion models that describe the dopant diffusion depending on the source type of dopant: limited source diffusion and constant source diffusion. The former type does not hold fixed surface concentration whereas the latter type has fixed surface concentration.

Table 6.1 Comparison of the limited source diffusion and the constant source diffusion [12].

Limited Source Diffusion Solutions	**Constant Source Diffusion Solutions**
Total dopant is fixed	Unlimited dopant
Surface dopant falls with time while dopant goes deeper	Surface concentration is fixed for all diffusion time
$N(x,t) = [\frac{Q}{\sqrt{\pi Dt}}]\exp[-(\frac{x}{2\sqrt{Dt}})^2]$	$N(x,t) = N_0 \mathrm{erfc}(\frac{x}{2\sqrt{Dt}})$
Often behave as constant source first (high concentration very shallow), then drive in deeper using limited source.	Total impurity concentration $Q = \int_0^\infty N(x,t)dx = 2N_0\sqrt{\frac{Dt}{\pi}}$



The measured diffusion profile of [Mg] along c-axis and a-axis can be fitted as a sum of several different diffusion models, referred to as the first, second and third order. The fitting results of [Mg] along c-axis are shown in Fig. 6.8.

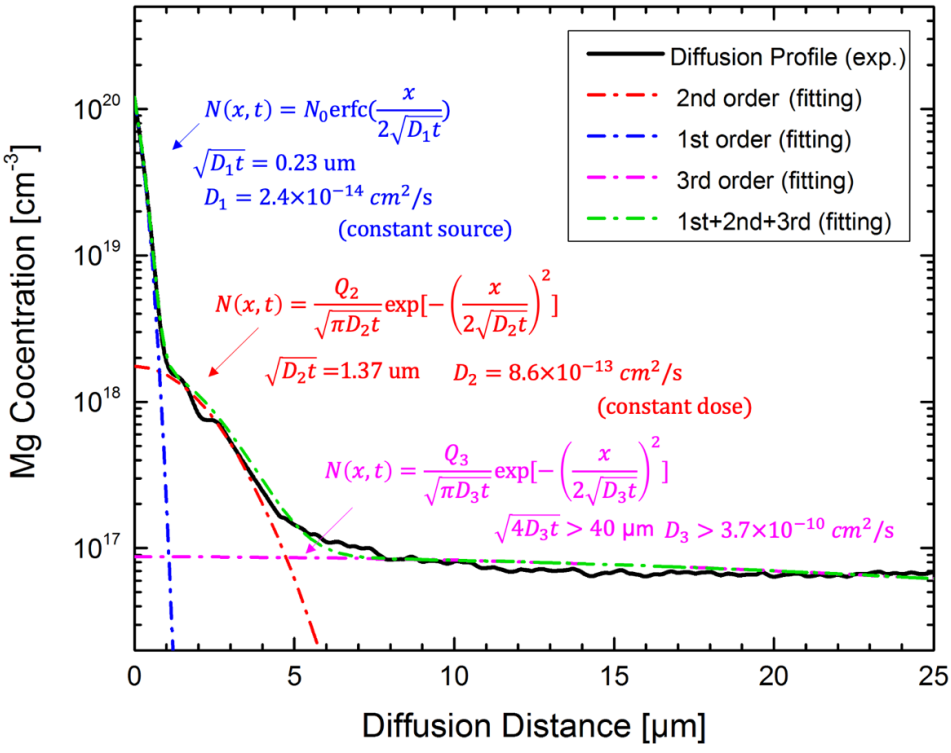


Figure 6.8 The measured diffusion profile of [Mg] along *c*-axis and the fitting results.

The first order diffusion is constant source diffusion and the second and third diffusion are limited source (constant dose) diffusion. It is reasonable to regard the surface of M-P region as

unlimited dopant source in the initial range which accounts for the first-order diffusion. For the second-order diffusion which was experienced by a few percentages of the total diffused Mg atoms, the diffusivity D_2 is higher than that of the first-order diffusion by a factor of 30–40, implying that these Mg atoms may have different chemical environments (e.g., unpassivated Mg atoms versus passivated Mg atoms by H atoms). Furthermore, there is a long-range third-order diffusion having 2–3 orders of magnitude higher diffusivity than the previously-described second order diffusion, suggesting that the in-situ surface diffusion during the HVPE growth might be responsible for the high diffusivity in the third-order diffusion.

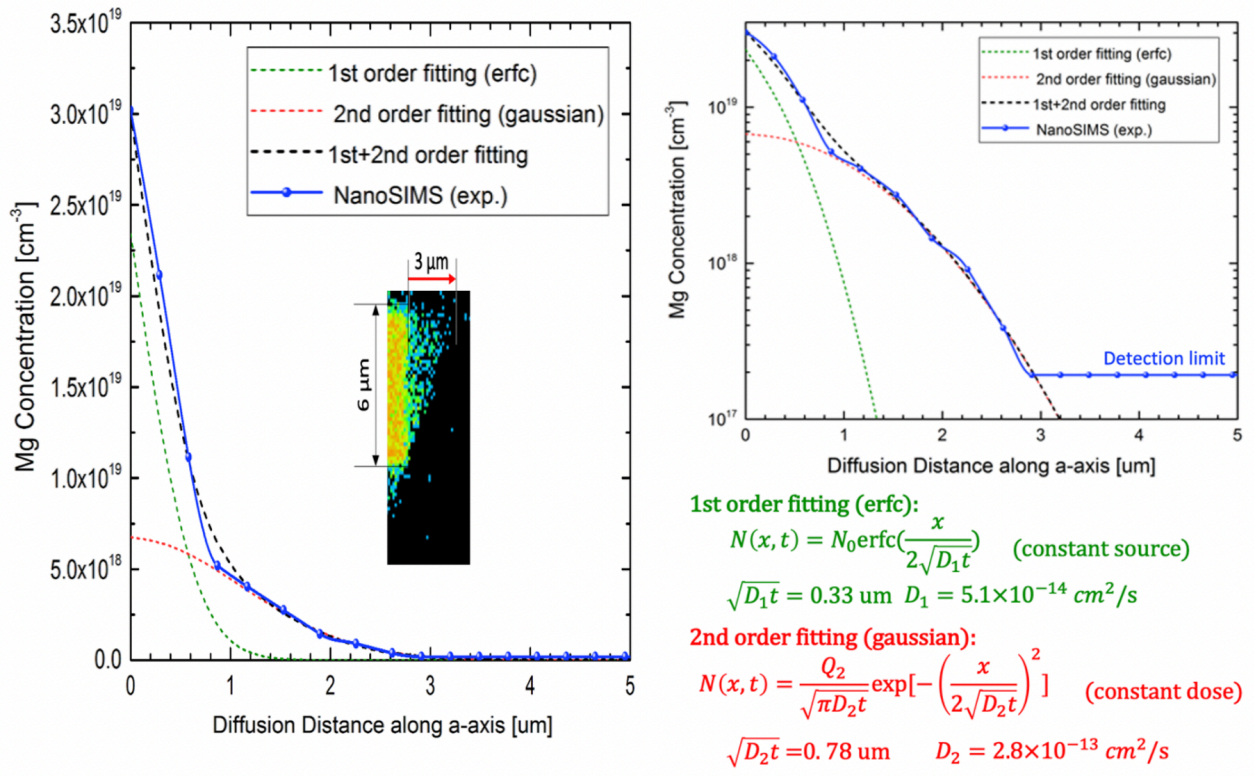


Figure 6.9 The measured diffusion profile of [Mg] along *a*-axis and the fitting results.

Likewise, the fitting results of [Mg] along *a*-axis are shown in Fig. 6.9 which consist of similar first-order (constant source) and second-order (constant dose) diffusion. The diffusivity of the second-order diffusion $D_{2,a}$ is 4–5 times higher than that of the first-order diffusion $D_{2,a}$.

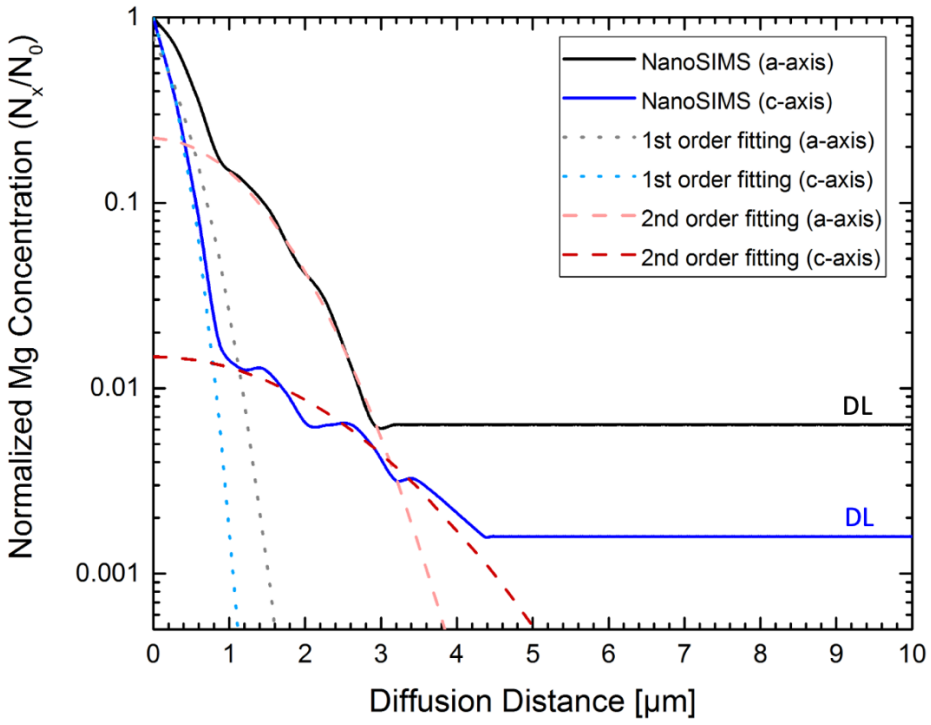


Figure 6.10 Comparison between the normalized diffusion profiles of [Mg] along *c*-axis and *a*-axis and their fitting curves.

Figure 6.10 compares the diffusion profile of [Mg] along c-axis and a-axis and their fitting curves, respectively. To better compare the results, the [Mg] are normalized in the both cases. It is interesting to observe that although $D_{1,a} > D_{1,c}$, $D_{1,a} < D_{2,c}$. In another words, the first-order diffusion of [Mg] along a-axis was faster than that along c-axis, but the second-order diffusion of [Mg] along a-axis was slower than that along c-axis. This implied that the diffusion along a-axis saw the diffusion barrier at the boundary of the triangle which limited the range of second-order diffusion range. Such barrier should have played the same role in limiting the diffusion range of the third-order diffusion along c-axis, as schematically depicted in Fig. 6.11.

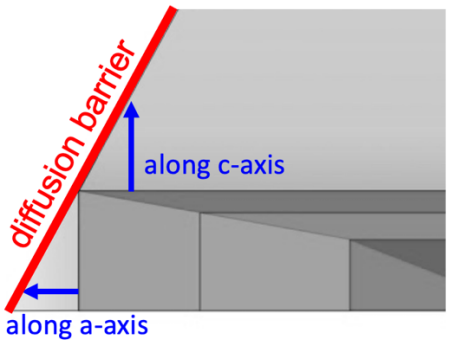


Figure 6.11 Schematic illustration of the diffusion barrier (in red line) at the boundary of the triangle which limited the diffusion of Mg along a-axis (2nd order diffusion) and along c-axis (3nd order diffusion).

In addition, the fitting parameters of the diffusion modeling in Fig. 6.8 may also be used to estimate the distribution of [Mg] along c-axis at different stage (varying with t) during HVPE growth using Eqn. (6.5).

$$N(x,t) = N_0\,\mathrm{erfc}\left(\frac{x}{2\sqrt{D_1 t}}\right) + \frac{Q_2}{\sqrt{\pi D_2 t}}\exp\left[-\left(\frac{x}{2\sqrt{D_2 t}}\right)^2\right] + \frac{Q_3}{\sqrt{\pi D_3 t}}\exp\left[-\left(\frac{x}{2\sqrt{D_3 t}}\right)^2\right] \qquad (6.5)$$

t=10min, 30min, 60min and 6hrs

The results are shown in Fig. 6.12. It can be seen that the plateau [Mg] (the flattening part of the [Mg] curve) decreased from 9×10^{17} cm^{-3} at 10 min to 1×10^{17} cm^{-3} at 30 min as the size of the height of the trapezoidal island increased. The third-order diffusion was able to follow the growth front at different intermediate growth stage possibly due to the nature of fast surface diffusion. Then, the appearance of the hump in the 6-hour-diffusion curve (green) compared to the 30-min-diffusion and 60-min-diffusion curves suggested that the much slower second-order diffusion has gradually become dominant.

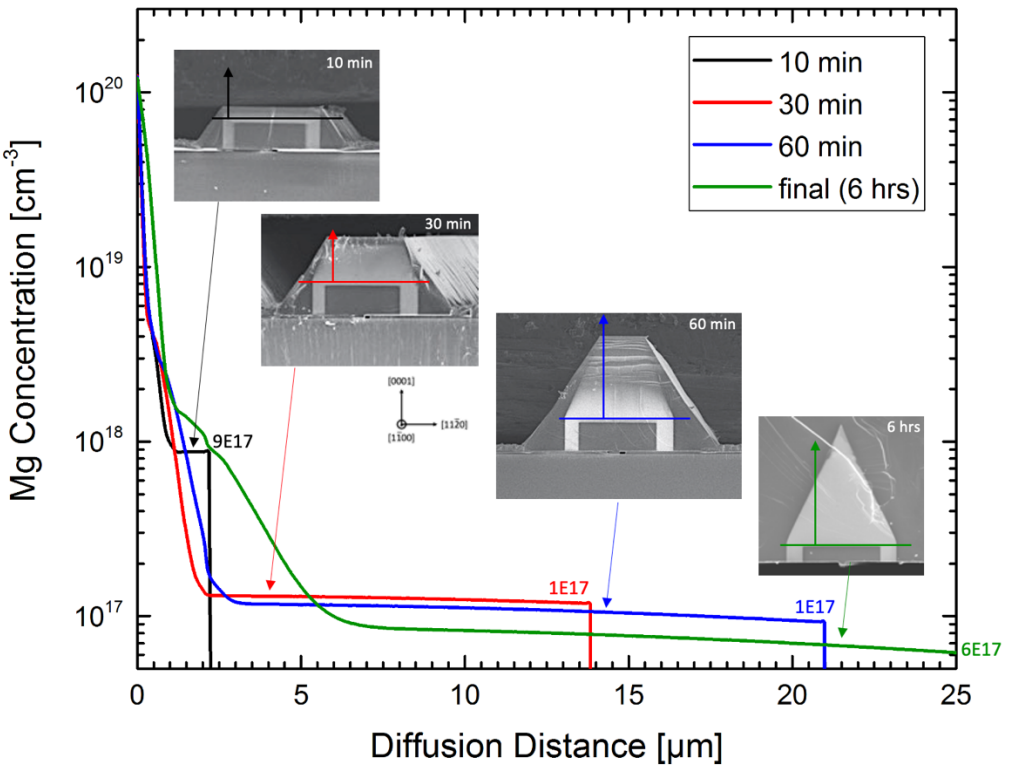


Figure 6.12 The estimated distribution of [Mg] (starting from the regrown interface and diffusing along c-axis) during different stage (t=10min, 30min, 60min, and 6 hours).

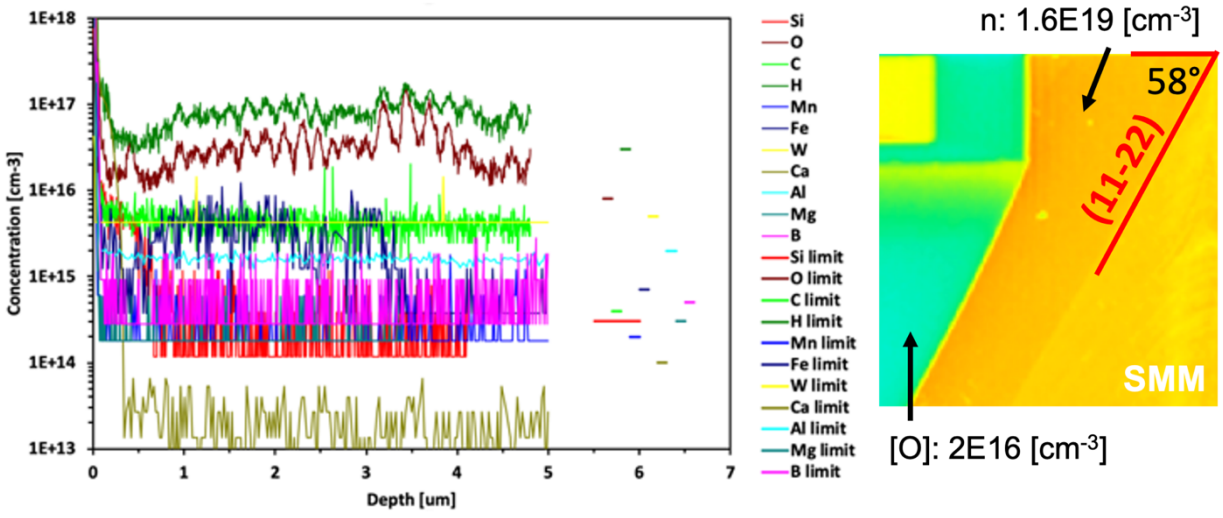


Figure 6.13 The dynamic SIMS result of a reference sample grown along c-plane by the same HVPE reactor showing the concentration of oxygen impurity [O] =2 $\times 10^{16}$ cm^{-3}, which may be used to estimate the [O] in the triangular region when the growth was along *c*-plane.

The anisotropic incorporation of impurity on different GaN crystallographic planes can be revealed in the SMM and SIMS mapping results. The dynamic SIMS result of the reference sample grown along c-axis in the same HVPE growth reactor in Fig. 6.13 shows that the concentration of oxygen impurity [O] is around 2×10^{16} cm^{-3} whereas the [Si] is below the detection limit of 3×10^{14} cm^{-3}. This is consistent with the [O] as compensating donor in the lightly-doped p-type triangular region. On the other hand, the n-type GaN grown by HVPE has high electron concentration of over 1×10^{19} cm^{-3}. Since Si impurity is absent in HVPE, O is the main shallow-donor species in the H-P region. As such, the impurity concentration of [O] is on the orders of several 10^{19} cm^{-3} in the GaN grown on $(11\bar{2}2)$ plane, making a difference of over three orders of magnitude compared to the [O] on c-plane. In addition, the crystallographic dependence of oxygen incorporation can be also revealed by the yellow contour lines in the SMM mapping result in the H-N region, suggesting that different levels of [O] were incorporated onto a series of high-index crystallographic planes.

6.3 Delta-doping of Mg for Ohmic Contact to p-type GaN

6.3.1 Rational

As mentioned in the preceding Chapters, since the first demonstration of p-type conduction [13], magnesium (Mg) is still the only dopant available to produce p-type GaN until today [14]. However, because of a high ionization energy (~200 meV), the hole concentration is rather limited in even heavily doped p-GaN [11], [15]. Furthermore, the common and unavoidable plasma etching process easily introduce N-vacancy as compensating donor which reduces the hole concentration of the surface p-GaN and makes it act like lightly-doped p-GaN, leading to the increased difficulty of obtaining Ohmic contact to p-GaN [16]–[18]. As a result, a good Ohmic contact to p-GaN has become the bottleneck to improve the performance of related electronic devices such as merged PiN Schottky diode, p-n junction diodes, bipolar transistors (HBT, GL-

BJT, and IGBT) and p-channel unipolar transistors (MISFET and HEMT) [19]–[23].

Doping by the post-growth diffusion is a common practice in semiconductors like Si which produces a decaying dopant profile where the top of semiconductor was saturated with the dopants under constant source diffusion. Such heavily-doped semiconductor surface makes it desired to satisfy the only practical regime to realize a Ohmic contact by approximation to the field-emission-enabled carrier transport across the metal-semiconductor junction [24], [25].

Post-growth diffusion by thermal annealing of Mg with high temperature and long time was reported to render p-GaN region in a undoped GaN which also incorporated the Ohmic contact to p-GaN [26]. However, the quality of the Ohmic contact was not quantitatively evaluated. Nor is there any study on the Ohmic contact formation to p-GaN with lower annealing temperature. Since the restoration of Ohmic contact to plasma-treated p-GaN is naturally expected in the device processing stage, the post-growth diffusion of Mg with low annealing temperature and short time, if feasible, could exhibit good compatibility to a broader range of device processing means.

In this section, excellent Ohmic contact to p-GaN by post-growth diffusion of Mg at lower temperature and shorter time even on the plasma-etched p-GaN. The results suggested that the Mg annealing condition of 550°C, 10 min was the optimum condition to form the Ohmic contact to p-GaN with minimum contact resistance and least influence on the distribution of [Mg] in the bulk p-GaN. Furthermore, the superior performance of a p-n junction diode with the same treatment further highlighted the benefit of Ohmic contact to p-GaN enabled by the post-growth diffusion of Mg.

6.3.2 Experiments

The epi-layers consisting of 400 nm p-type GaN with [Mg]= 1×19 cm^{-3} and 2 μm n^--type GaN with $|N_d - N_a|$= 4×16 cm^{-3} were grown by metal-organic vapor phase epitaxy (MOVPE) on the

~400-μm-thick 2-inch n^+-GaN substrate having free electron of ~10^{18} cm^{-3}. The top p^+ contact layer was not grown. The wafer was diced into dozens of small samples.

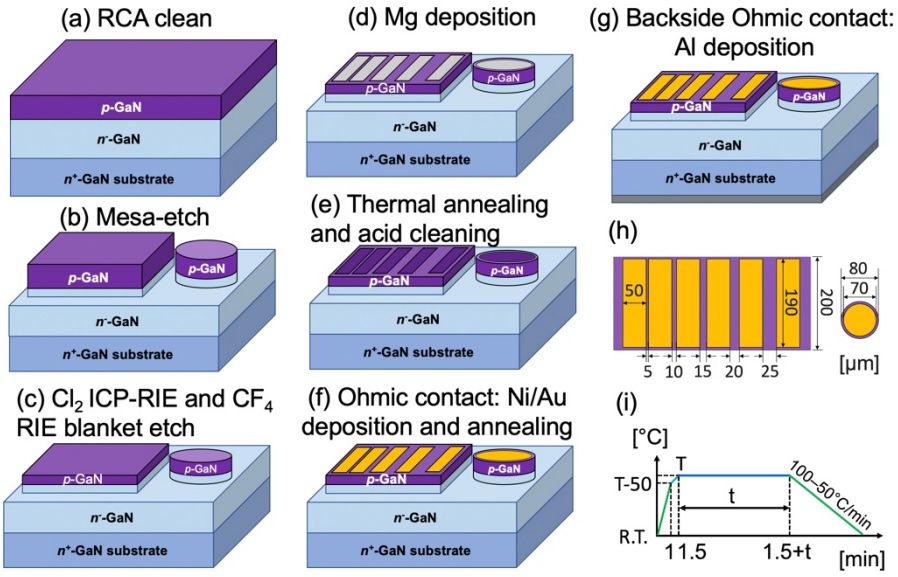


Figure 6.14 (a)–(g) Schematic illustrations of the key steps of the fabrication flow for the p-GaN TLM test structure and p-n junction diode with plasma- and Mg-treatment. (h) Schematic plan-view of the TLM test structure and the mesa structure and anode of p-n junction diode. (i) Thermal cycle for all the annealing process mentioned in this letter with the defined variants of temperature (T) and time (t).

Fig. 6.14 (a)–(g) schematically illustrates the key steps in the fabrication flow for the p-GaN TLM test structure and p-n junction diode. Four paths are divided among the samples: I (blank): a-b-f-g; II (with the Mg-treatment only): a-b-d-e-f-g; III (with the plasma-treatment only): a-b-c-f-g; IV (with the dual plasma-Mg-treatment): a-b-c-d-e-f-g. As shown in Fig. 6.14 (b), the Cl_2-based ICP-RIE was used for mesa etch (etching depth: ~800 nm, hard mask: ~3 μm photoresist), including the TLM test structure and the circular vertical p-n junction diode (PND) next to it (Fig. 6.14 (h)). For path III and IV designed to evaluate the effect of post-growth diffusion of Mg on the plasma-treated p-GaN, part of the samples were subject to the plasma-treatment including Cl_2 ICP-

RIE (ICP power: 150 W, bias power: 30 W, etching time: 30 s) followed by CF_4 RIE (bias power: 100 W, etching time: 2 min) to represent an etching condition to fully damage p-GaN (Fig. 6.14 (c)). The etched samples were then bathed in hot TMAH solution for 10 min to smoothen the mesa sidewalls. After that, all the samples were annealed with T= 700 °C and t= 10 min in N_2 for p-GaN activation. Then, Mg (50 nm) was sputtered onto the p-GaN except the blank samples as shown in in Fig. 6.14 (d), followed the heat treatment process in N_2 with the variants of T and t defined in Fig. 6.14 (i). All the Mg-treated samples were cleaned by the SC2 solution (HCl: H_2O_2: H_2O=1:1:4) at 80 °C for 10 min to remove the residue Mg and possible acid-soluble Mg compounds (Fig. 6.14 (e)). Finally, Ni (20 nm)/Au (150 nm) was E-beam evaporated onto the exact same region with Mg (the alignment precision was within 1 μm) onto all the samples, followed by thermal annealing with T= 525 °C and t= 5 min in O_2 (Fig. 6.14 (f) and (h)). Al (~180 nm) was sputtered onto the backside of all the samples as cathode for the PNDs (Fig. 6.14 (g)).

6.3.3 *I-V* Measurement Results

Fig. 6.15 (a) is the *I-V* characteristic (contact spacing: 15 μm) of the sample underwent path I and path II (with varying T and t). It can be seen that both the path I-sample (blank) and the path-II-samples (T=400 °C and 500 °C) did not exhibit Ohmic behavior. Furthermore, as it appeared, the 500 °C sample had the highest resistance, followed by the 400 °C sample and the blank sample, successively. This could be explained by the parasitic alloyed region (chemically inert, insoluble in acids or alkalis) formed by interdiffusion of Mg and Ga (or GaN) on top of the p-GaN which was thickened and coarsened with increasing T from 400 °C to 800 °C. The results suggested that the alloyed layer on top of semiconductor was not responsible for the Ohmic contact to p-GaN and also conversely added to the specific contact resistivity. In strong contrast, the samples with 550 °C, 600 °C, and 700 °C exhibited excellent Ohmic behavior with fully linear *I-V* characteristics

whereas the 800 °C sample had slightly degraded linearity. The transition between non-Ohmic to Ohmic occurred within 500 °C–550 °C, which was further revealed in Fig. 6.15 (b) with finer steps of T. When T increased from 500 °C to 550 °C, the linearity of the *I-V* curves gradually strengthened. Furthermore, although the sample with 500 °C and 10 min showed non-Ohmic behavior, the sample with 500 °C and 60 min showed quasi-linear Ohmic behavior with comparable linearity between that of 525 °C, 10 min and 535 °C, 10 min. This proved that no specific value of T was essential to initialize the Ohmic contact when t was variant, which further suggested that the diffusion of Mg in GaN-a physical process-was the cause due to the formation of the p^+-GaN layer upon reaching the threshold diffusion length as a function of both T and t.

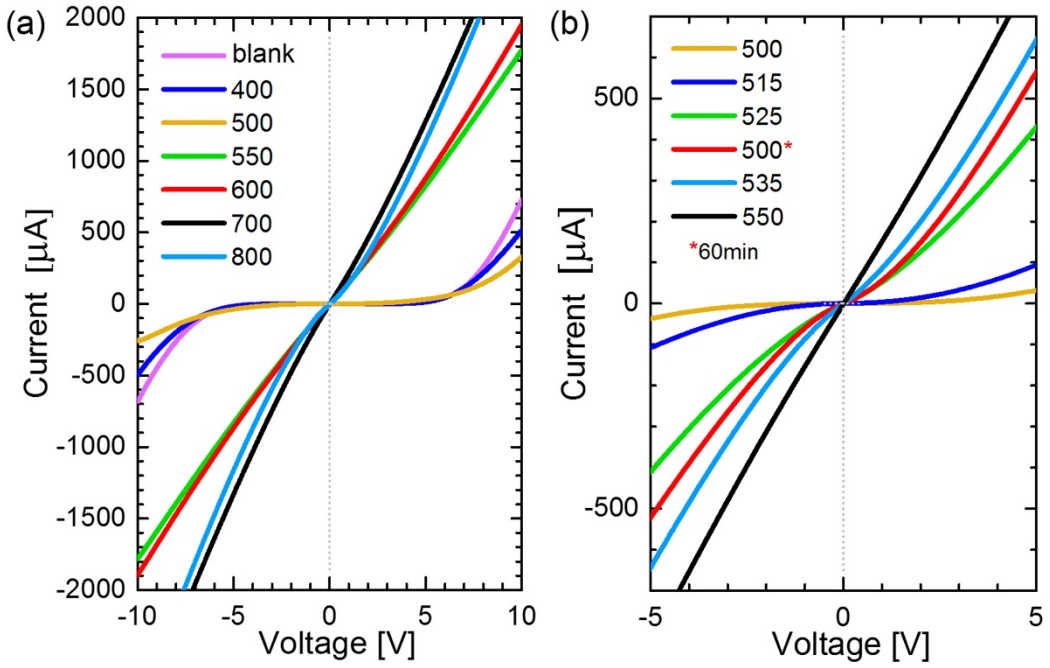


Figure 6.15(a) The *I-V* characteristics (contact spacing: 15 μm) of the blank sample and path II-samples with varying T (from 400 °C to 800 °C) and t= 10 min in the Mg-treatment process. (b) The I-V characteristics (contact spacing of 15 μm) of the path II-samples with T from 500 °C to 550 °C, t= 10 min and T= 500 °C, t= 60 min.

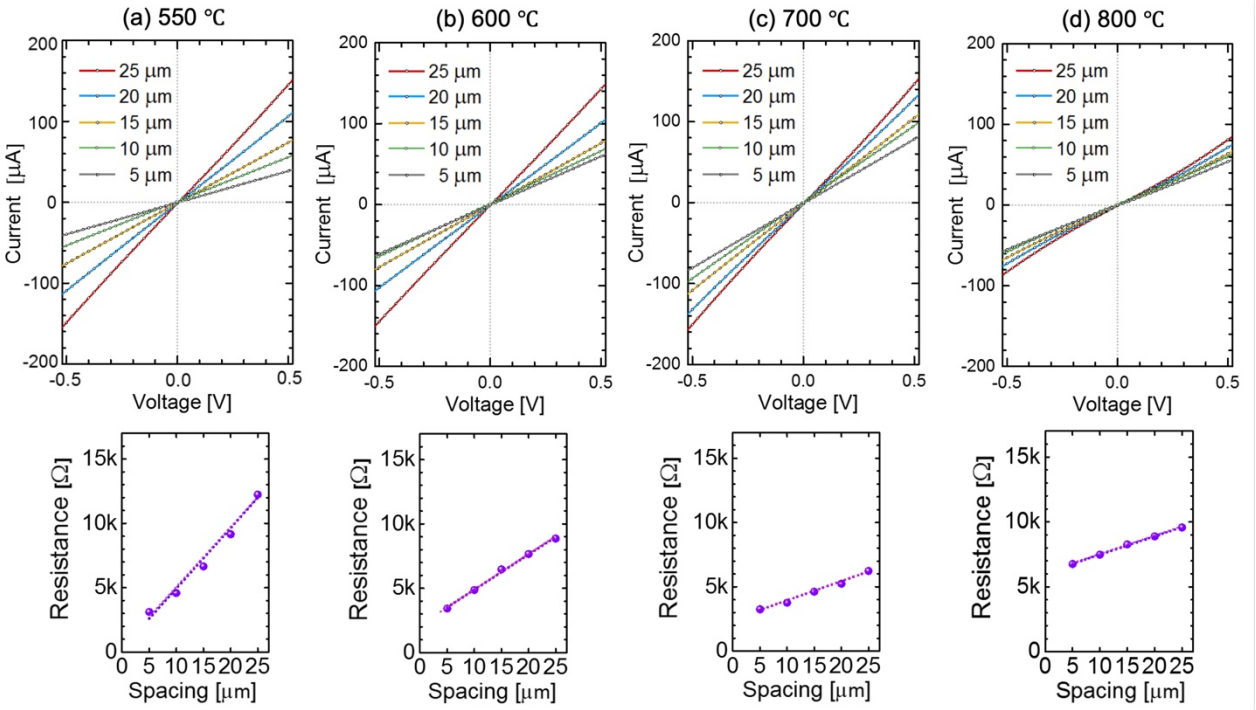


Figure 6.16 (a)-(d) The TLM results of the path-II samples with Mg-treatment (T=550 °C, 600 °C, 700 °C, 800 °C) and t=10 min.

Table 6.2 Summary of the sheet resistance and the specific contact resistivity under different annealing temperatures.

Temperature	550 °C, 10 min	600 °C, 10 min	700 °C, 10 min	800 °C, 10 min
Sheet resistance	89.3 kΩ/sq	51.9 kΩ/sq	28.3 kΩ/sq	25.3 kΩ/sq
Specific contact resistivity	6.37×10^{-5} Ω.cm^2	8.13×10^{-3} Ω.cm^2	1.82×10^{-2} Ω.cm^2	1.47×10^{-1} Ω.cm^2

Figure 6.16 compares the TLM results (extracted at V=± 0.025 V) of the path-II samples with T=550 °C, 600 °C, 700 °C, and 800 °C and Table 6.2 summarizes the sheet resistance and the specific contact resistivity under these conditions. It is concluded that the sheet resistance decreased with the temperature whereas the specific contact resistivity increased with the temperature. The diffusion of Mg altered the previous distribution of [Mg] in the bulk p-GaN when more Mg diffused into p-GaN at higher temperature, thus giving rise to the hole concentration and decreasing the sheet resistance. On the other hand, the concomitant thickening of the parasitic Mg

alloyed region on top of p-GaN gave rise to the specific contact resistivity in the same manner as in the non-Ohmic range (400 °C to 500 °C) where the diffusion length was insufficient form the thin p^+-GaN layer. The counteracting effects of the Mg alloyed region and of the Mg diffusion-enabled p+-GaN region leads to 550 °C being the optimum temperature to reach the minimum contact resistance with the least influence on the distribution of [Mg] in the bulk p-GaN, and the latter feature is important for the device applications where a uniform and moderately-doped p-GaN is preferred.

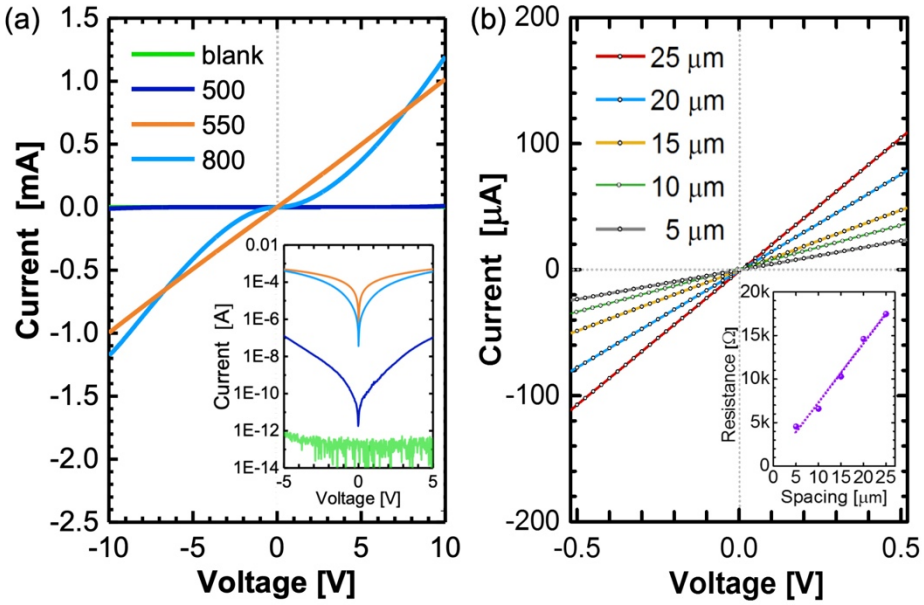


Figure 6.17(a) The *I-V* characteristics (contact spacing of 15 µm) of the plasma-treated samples with Mg-treatment (varying T and t= 10min) and without Mg-treatment (blank sample). (b) TLM result of the plasma-treated sample with Mg-treatment (T= 550°C and t= 10min).

Figure 6.17 (a) compares the *I-V* results of the TLM test samples underwent path III and path IV with varying T. It can be seen that the plasma-treated sample exhibited undetectable current within ±5V (R>1TΩ), proving that the Ohmic contact to p-GaN was considerably compromised by etching-induced damages. Then, after Mg-treatment at 550 °C (10 min), the ideal Ohmic contact with fully linear *I-V* curve was restored, resembling that of the path II-sample with 550 °C in Fig.

6.16. As shown by the TLM result (extracted at V=± 0.025 V) in Fig. 6.17 (b), the sheet resistance was 128.6 kΩ/sq and the specific contact resistivity was 2.1×10^{-4} Ω.cm^2. Since the plasma etching by Cl_2 ICP-RIE thinned the p-GaN by a thickness of ~120 nm (etching rate: 4 nm/s, etching time: 30s), the ratio of the increased p-GaN sheet resistance (128.6 kΩ/89.3 kΩ=144%) matched the ratio of the reduced p-GaN thickness (400 nm/280 nm=143%) very well, which proved a good repeatability of the experiments.

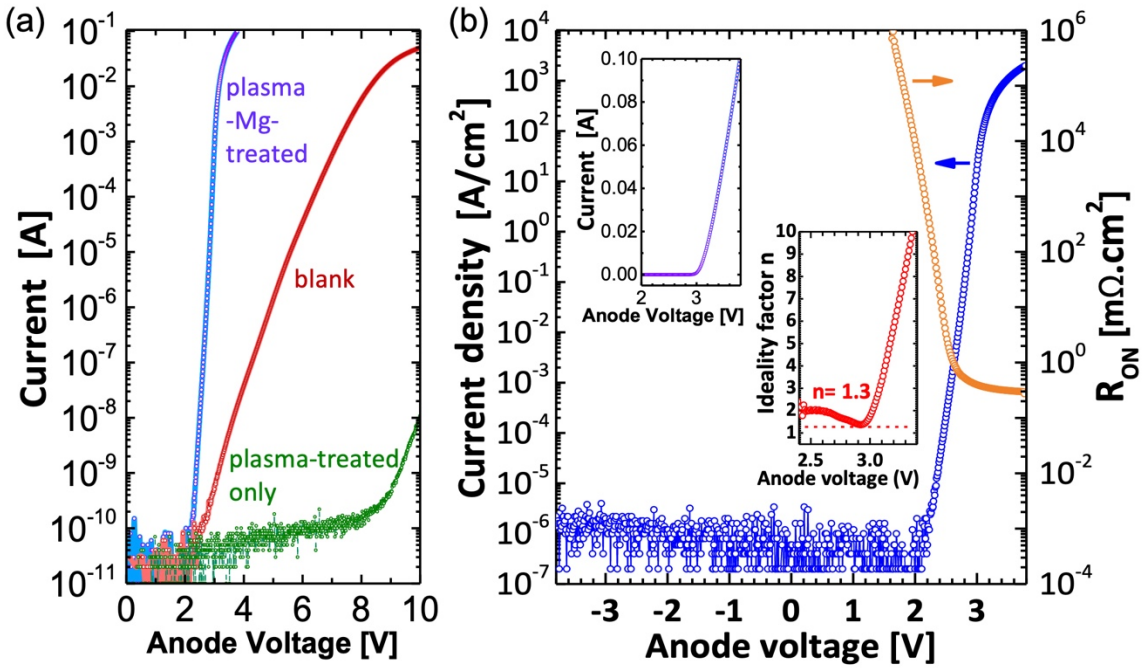


Figure 6.18 (a) The semilogarithmic forward *I-V* characteristics of the PNDs (blank sample), with plasma-treatment and with plasma-Mg-treatment, respectively. (b) The current density and on-resistance-voltage characteristics of the plasma-Mg-treated PND in (a). The insets show the linear I-V and ideality factor (IF)-V plots, respectively.

Fig. 6.18 (a) compares the *I-V* characteristics of the PNDs underwent path I (blank), path III (plasma-treated only), and path IV (dually plasma-Mg-treated, T=550 °C), respectively. It can be seen that the path IV-PND exhibited drastically improved current compared to the path I-PND and the path III-PND. As shown in Fig. 6.18 (b), a low turn-on voltage of 3V, a low ideality factor (IF)

of 1.3 at around 2.9 V, and a high current density J of 1kA/cm^2 at 3.5 V (mesa area is taken as device area, diameter: 80 μm) corresponding to $R_{on,sp}$=0.30 mΩ.cm^2 at 3.5 V were obtained on the plasma-Mg-treated PND which were among the best reported values for GaN PNDs, owing to the excellent Ohmic contact formed onto p-GaN [27], [28]. This also proved that the post-growth diffusion of Mg was highly effective to restore the ideal Ohmic contact to the plasma-etched p-GaN.

6.4 Summary

In brief summary, the state-of-the-art characterization techniques featuring high spatial resolution were carried out to investigate the elemental, dopant, and carrier distribution of the ELO-GaN samples with selective-area doping profiles. The anisotropic diffusion model of Mg was built and the novel phenomenon associated with the diffusion behaviors of Mg in the ELO-GaN were provided with possible explanations.

On the other hand, the application of delta-doping of Mg by diffusion at low temperature and short time in forming excellent Ohmic contact to p-GaN was demonstrated with success. Specifically, the capability to fully recover the Ohmic contact to plasma-damaged p-GaN shows a strong promise to address the bottleneck in this field of study, which should also lend a solid hand to greatly enhance the performance of p-n junction diode and bipolar transistors in future work.

6.5 References

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Chapter 7

Conclusion and Future Outlook

7.1 Concluding Remarks

To conclude this dissertation, a holistic approach is adopted to explore the possibility of using epitaxial lateral overgrowth to tackle with the persistent issue of producing laterally patterned p-n junctions in GaN to improve the performance of GaN-based power switching electronics devices. The process of combining ELO in the pre-coalescence stage with in-situ doping produces ELO-GaN island arrays with half-core-shell doping profile.

The innovative measures are taken in device processing or material growth aspect to tailor the half-core-shell doping structure into the desired selective-area doping structure, thus yielding unprecedented opportunities in the power electronic applications.

For the device processing innovation, the true-lateral device architecture is built which consists of fully lateral aligned p-n junctions. Both diodes (SBD and PND) and bipolar transistors (GL-BJT and IGBT) with the true-lateral device architecture are demonstrated either with superior performance or for the first time, owing to various aspects of the advantages of the true-lateral device architecture.

For the material growth innovation, the epitaxy-enabled substrate transfer approach is demonstrated to produce the GaN substrate with repeating laterally patterned p-n junctions which makes it ideal for the planar-gate vertical MOSFET or even superjunction MOSFET.

As a result, the potential of epitaxial lateral overgrowth to simultaneously realize the low threading dislocation density and the selective-area doping profile (lateral patterned p-n junctions) is initially and finally unleashed. This may spawn a revival of interest into ELO-GaN for power electronic applications.

7.2 Future Outlook

7.2.1 Improvement of V_{BR}

Despite the initial success in obtaining the record high breakdown field in the fully lateral p-n junction, it should be noted the breakdown voltage is not high. The reason lies in the high impurity incorporation in the UID-GaN region serving as the drift layer of the power devices. The future work will try out different measures to reduce the net doping concentration $|N_d\text{-}N_a|$ of the drift layer. In addition to the optimization of AlGaN underlayer and poly-AlN deposition to suppress the desorption of Si from SiN_x mask, the effect of n^+-core region of the GaN islands on the Si incorporation in the n^--GaN (UID-GaN) should also be investigated. Speaking of which, for the proposed doping structure of IGBT on ELO-GaN, the design of n^+-core region is not necessary and could be saved, as shown in Fig. 7.1. In this way, all the possible Si source is minimized for the growth of n^--GaN (UID-GaN). It will allow one to see the lowest possible incorporation of donor-like impurities in the MOVPE growth chamber.

In addition, the more important and fundamental parameters to significantly increase the breakdown voltage is to reduce the doping concentration $|N_d - N_a|$ in the n^- drift region, according to Eqn. (7.1) [1]:

$$V_{BR} = \frac{\epsilon_0 \epsilon_r {\varepsilon_{crit}}^2}{2e\,|N_d - N_a|} \tag{7.1}$$

Specifically, if $|N_d - N_a|$ can be modified from the current level of 6×16 cm^{-3} to the median level of 2×16 cm^{-3} in the literature, the breakdown voltage can reach over 900 V [2]. This could be possibly achieved by optimizing MOVPE growth parameters and minimizing possible Si and O incorporation into UID-GaN. Ultimately, by reducing $|N_d - N_a|$ to the lowest level of 1-2×15 cm^{-3} reported for GaN, the breakdown voltage can be improved to a few thousand volts [3], in that case, the width of drift region should also increase accordingly to avoid deep punch-through. In fact, ultra-

low $|N_d - N_a|$ is also the underlying reason for the much higher BV_{CEO} in SiC-based BJTs, as can be seen in Fig. 4 of the manuscript where the device demonstrating highest BV_{CEO} of 15 kV has $|N_d - N_a| \sim 1\times10^{14}$ cm^{-3} [4].

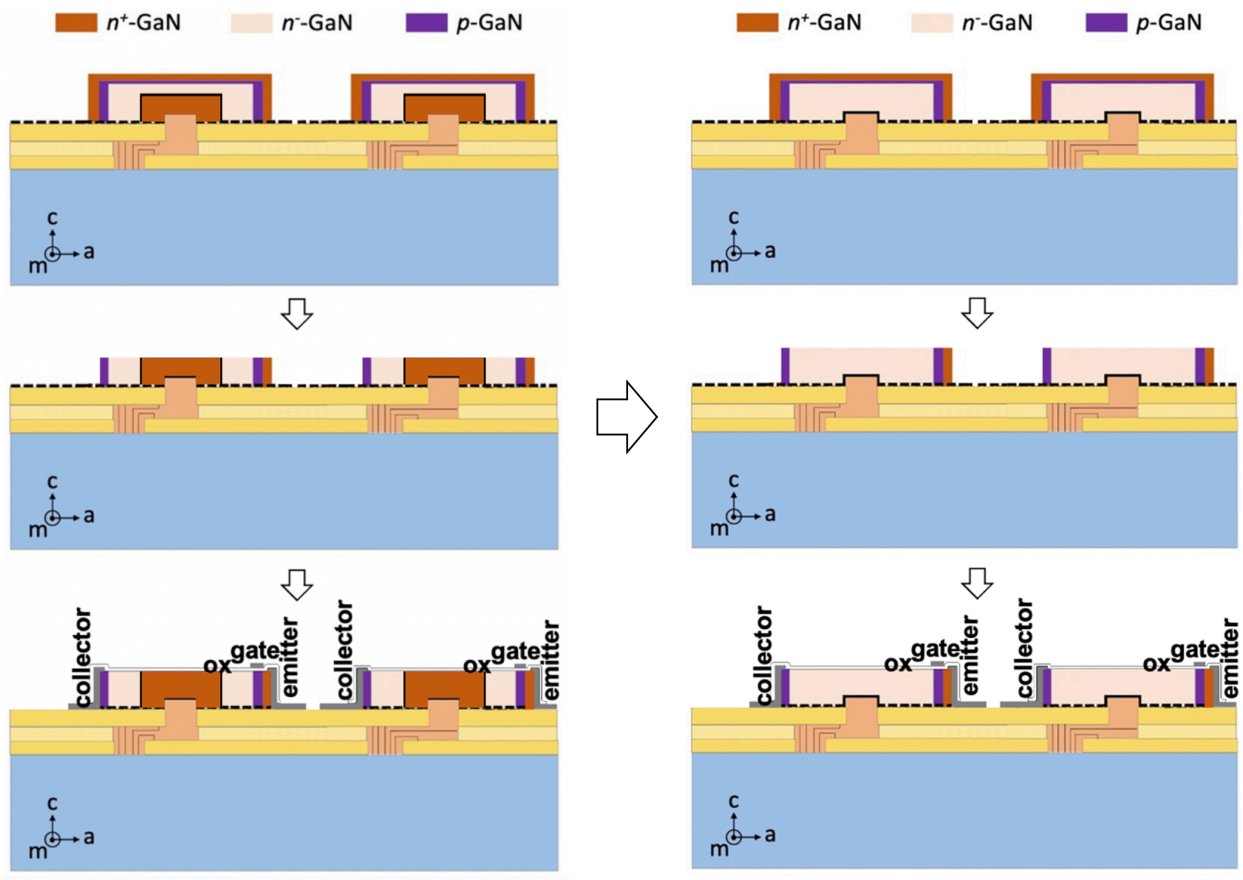

Figure 7.1 Modified doping sequency by removing unnecessary n^+-core in the ELO-GaN island for IGBT structure.

Furthermore, the compromised option should be explored by modulate the incorporation amount of C which acts as compensating acceptor to counteract the donor-like impurities such as Si, O, and nitrogen vacancy (V_N) [5]. If $|N_d\text{-}N_a|$ can be reduced to 1–2×10^{15} cm^{-3}, the expected breakdown voltage can reach over 5 kV. Then the thickness of the drift region needs to be scaled up correspondingly. Fortunately, this is not difficult to obtain by ELO process when the thick drift layer only requires a wide ELO-GaN island depicted in Fig. 7.2, as opposed to the conventional

drift layer in a true-vertical or quasi vertical device which needs to overcome considerable stress built in the thick GaN epi-film.

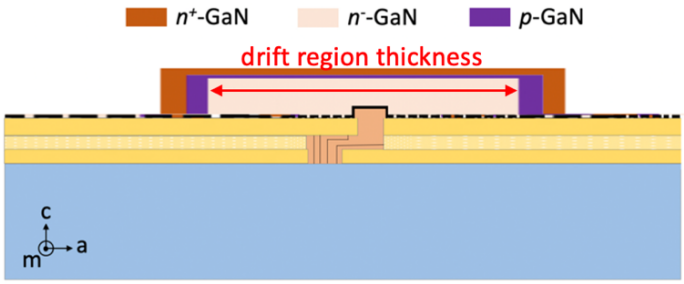

Figure 7.2 Thickening of drift region by extending the lateral dimension of n^--GaN region of the ELO-GaN island grown over the mask.

7.2.2 Reduction of $R_{on,sp}$

It is equally important to reduce the on-resistance of the devices, which should become the intrinsic advantage of bipolar transistors provided that the bottleneck of Ohmic contact to plasma-damaged p-GaN is addressed. It is fortunate that a versatile and highly effective approach has been demonstrated in Chapter 6 to enable the delta-doping of Mg at the metal-semiconductor junction interface by post-growth diffusion of Mg by low temperature and short time annealing. As shown in Fig. 7.3, after p-sidewall of the GaN island is exposed by dry etching, the unavoidable plasma etching-induced damages could be recovered by sputtering of metallic Mg onto the vertical sidewall followed by thermal annealing.

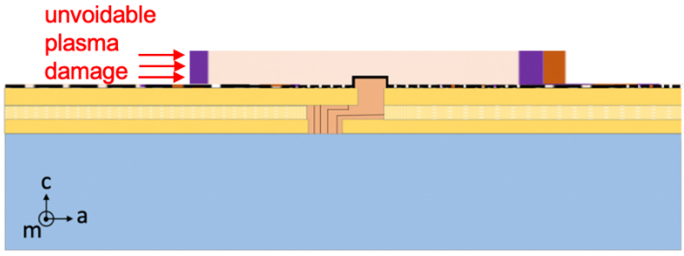

Figure 7.3 The p-GaN sidewall exposed by dry etch and the associated damages by plasma to be recovered by deposition of Mg and thermal annealing.

By the same token, the Ohmic contact to p-GaN in the GLP-BJT can also be greatly enhanced by the aforementioned approach to improve the current density of the device. Speaking of GLP-BJT, for the Ohmic contact region between metal gate to the narrow p-base, electron beam lithography can be utilized to make orderly nanoholes in the gate oxide instead of randomly-distributed nanopits in the p-base region in order to improve the device yield.

Once the excellent Ohmic contact is formed onto p-GaN, it is anticipated that the conductivity modulation-one of the most intriguing aspects of a bipolar transistor like IGBT [1]-could be realized in GaN and the unipolar Baliga's FOM limit could be superseded [6]. It is worth mentioning that realization of conductivity modulation naturally requires that the net doping concentration of n^--region should be sufficiently low, which goes back to the discussion in the preceding sub-section.

7.2.3 Substrate Transfer and Monolithic Integration Platform

After addressing the issues to improve the performance of individual devices, the focus will be turned to realizing another combined advantage of the ELO-GaN islands with fully lateral device architecture which lies in the feasibility to realize a platform of monolithic integration of a full spectrum of electronic devices onto a single insulating substrate.

For the advantage of ELO, compared to the continuous thin film, the ELO-GaN islands can be easily transferred onto the host substrate due to the limited ratio of contact area to the parent substrate.

For the advantage of fully lateral device architecture, the ELO-GaN island with fully lateral doping structure features horizontal symmetry. After the top face of the island is bonded to the new substrate, the small bottom area is detached from the parent substrate and the island transfer is completed. With horizontal symmetry, the flipped-over structure of the island on the new

substrate is identify to the previous structure, facilitating the subsequent device processing including metallization on the sidewalls of the island.

In such a way, a full spectrum of devices from a number of parent substrates, from core devices to peripheral circuits for the driving, control, sensing and protection module, can be successively transferred onto a single new substrate where each device is individually addressable. Figure 7.4 schematically illustrates the monolithic integration of four different types of GaN devices (SBD, PND, MOSFET, GL-BJT, IGBT, etc..) with fully lateral doping structure from parent substrates onto a single substrate. The host substrate needs to be insulating, so that the contact pads can be flexibly designed and deposited onto the surface to connect arbitrarily devices of interest, making essentially the substrate a "breadboard" which shows great promise to achieve unprecedented versability and flexibility in the monolithic integration, which is desirable to create more on-chip functionality, enhance robustness and facilitate the miniaturization of the entire power conversion system [7]. Furthermore, the substrate should preferably possess excellent thermal conductivity, making SiC or diamond good alternatives. In this way, the substrate can better serve as an ideal platform towards monolithic integration of power conversion system.

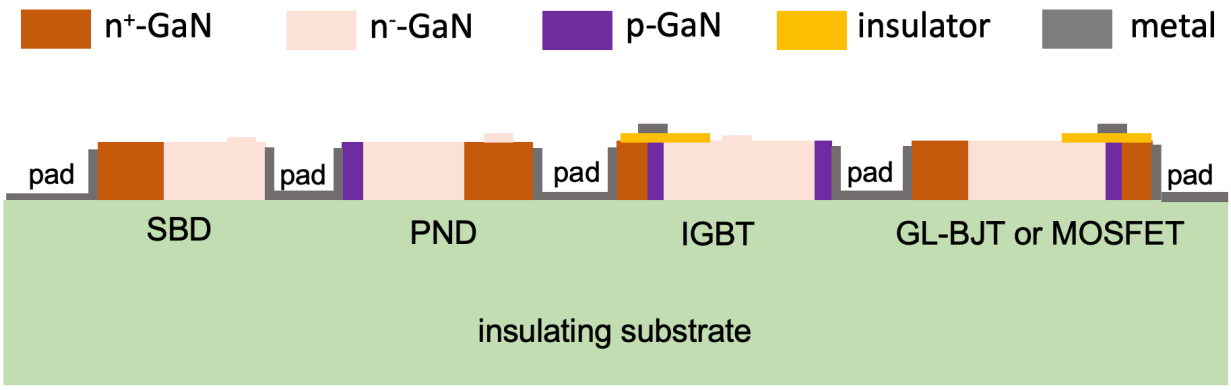

Figure 7.4 Monolithic integration of a number of different GaN devices (SBD, PND, MOSFET, GL-BJT, IGBT, etc..) by successive transfer of the flipped-over ELO-GaN islands with various

fully lateral doping structures from parent substrates onto a single insulating substrate preferably with excellent thermal conductivity and device processing on the new substrate.

7.3 References

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