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Design and Optimization of a Composite Heat Spreader to Improve the Thermal
Management of Three-Dimensional Integrated Circuits

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Mechanical Engineering

by

Andisheh Tavakoli

March 2022

Dissertation Committee:
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The Dissertation of Andisheh Tavakoli is approved:

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Committee Chairperson

University of California, Riverside

Dedicated to

To my parents, whose courage gave me a chance for a better life

ABSTRACT OF THE DISSERTATION

Design and Optimization of a Composite Heat Spreader to Improve the Thermal
Management of Three-Dimensional Integrated Circuits

by

Andisheh Tavakoli

Doctor of Philosophy, Graduate Program in Mechanical Engineering
University of California, Riverside, March 2022
Dr. Kambiz Vafai, Chairperson

The present study documents the optimal distribution of a limited amount of high thermal

conductivity material to enhance the heat removal of 3D integrated circuits, ICs,

numerically. The structure of the heat spreader is designed as a composite of high thermal

conductivity (Boron Arsenide) and moderate thermal conductivity (copper) materials. The

volume ratio of high conductivity inserts to the total volume of the spreader is fixed. For

the configuration of the inserts two categories are considered, namely ring type and blade

type. For the former, various patterns of the single and double ring inserts are studied; while

for the latter, three main configurations including radial, one level of pairing, and two levels

of pairing are examined. To examine the impact of adding high conductivity inserts on the

cooling performance of the heat spreader, a detailed analysis is performed to find the

optimal geometry for each category. An approach is implemented to find the structures

corresponding to the lowest maximum temperature of the 3D IC while the ratio of the

Boron Arsenide volume to the whole heat spreader volume is fixed. Four different

boundary conditions are examined to seek their impact on the optimal configuration of the inserts. For the double ring insert layout, the optimal distribution of the high-conductivity material between the inner and outer rings is found. The results show that for the optimal conditions, the maximum temperature of the 3D IC is reduced up to 10%. For the blade inserts, the results show that for the constant temperature, variable temperature, and convection heat transfer boundary conditions at optimal conditions, the maximum temperature of the whole structure can be reduced to 13.7, 11.9, and 13.9%, respectively; while the size of the heat sink, and heat spreader is mitigated by 200%.

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Chapter 1

Introduction

With the advances in the electronic industry, the vital role of thermal management has become more critical. By miniaturizing the electronic components, the density of electronic pieces per volume is risen steeply. As such, the conventional methods cannot properly address the generated high heat fluxes for these devices.

Thermal management is the key point for the advancement of the microelectronic components [1-8]. As the number of devices mounted on a single chip is increasing, the appropriate thermal management is becoming of paramount concern. Thermal issues have a crucial impact on the functionality and reliability of the electronic systems.

Recent advances in the electronics industry have paved the way for various innovative schemes to be proposed and implemented to overcome the overheating issues [9-11]. For example, Sparrow et al. [12] analyzed the fluid flow and heat transfer in cold plates to improve the thermal management of electronic equipment. In their work, they considered periodic variations in the stream direction. Azari et al. [13] tried to model analytically the hotspots of a nonuniform heated body when rectangular microchannels were invoked to dissipate the generated heat. In another work, Colla et al. [14] utilized nano-phase change materials to mitigate the high temperatures resulting in the electronic parts. Gielen and Baelmans [15] analyzed the thermal management and the cooling of the electronic components based on the second law of thermodynamics.

It should be noted that thermal management is vital in the design of 2D and 3D ICs technology since the thermal conductivity of dielectric materials is low which results in

thermal hotspots throughout the component. Most of the research to overcome this issue has been done by devising innovative designs for the heat sinks. [16-22]. For instance, conductive heat tree structures at micro and nanoscales have been generated for cooling electronic disc-shaped pieces in Daneshi et al [23]. In their work, tree shape conduction paths of highly conductive materials in radial pattern, structure with one level of pairing, tree with loop architectures, and combination of branching and loops were generated and optimized for cooling the electronic devices.

The increased power density in 3D ICs results in ever more crucial thermal issues that directly affect their performance. With 3D IC we can achieve circuit performance and on-chip integration of analog, digital, and mixed-signal circuits simultaneously [24]. Resistive-capacitive delay is one of the drawbacks of the 2D ICs. To overcome this issue 3D architecture can be utilized [25]. Another advantage of this system is its suitability for usage for System-on-a-Chip designs [24]. There is limited number of investigations for the thermal aspect of 3D ICs [26].

Tavakkoli et al. [27] mentioned that by increasing the junction temperature as high as 10 oC, the clock buffer performance deteriorates around 1.2%. This matter shows the significance of reducing the temperature of hot spots in electronic circuits. Most of heat generation throughout the integrated circuit is due to transistor switching. In 3D ICs there are several layers including device layers mounted over each other. Generally, all the device layers should be electrically insulated from each other using some special dielectric layers. However, these dielectric layers deteriorate the cooling of the structure due to their low thermal conductivity [28, 29]. Therefore, removing the generated heat is more crucial

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in 3D ICs where the overheat can degrade the device performance, reduce the reliability of the chip by raising the junction leakage and electromigration failure [30]. It is also notable that the effective operating speed of electronic components is higher at lower temperatures [31].

To increase the heat transfer area between the die and the heat sink, a heat spreader is utilized [26]. The architecture and the heat spreader material and different layers as well as the specification of the heat sink affect the heat dissipation of the 3D IC remarkably [32]. Highly conductive inserts have been used extensively to enhance the thermal dissipation potential of different electronic devices. For example, Rocha et al. [33] developed an analytical solution for a circular electronic piece embedded by highly conductive radial inserts. They optimized the architecture of the configuration.

In their subsequent work, they optimized the configuration for circular inserts numerically [34]. da Silva et al. [35] used constructal theory to optimize the configuration of an incomplete insert with high thermal conductivity to cool a circular disk. The inserts were extended from the perimeter towards the center of the disc, without meeting each other at the center of the disc.

A constructal design for the architecture of high conductivity inserts, HCI's, for thermal management of triangular electronic pieces has been done by Ghodoossi and Egrican [36]. Sharifi et al. [37] used an incomplete insert with a variable cross-section to enhance the heat dissipation capability of the electronic component. They optimized the profile of the cross-section for the inserts in both radial and dendritic designs. Nazari et al. [38] optimized

the configuration for highly conductive inserts in circular electronic pieces numerically. They found the optimal arrangement based on both thermal and mechanical points of view. Tavakkoli et al. [27] performed a detailed comprehensive study on the thermal issues in 3D integrated circuits. They analyzed the effect of the size of different parts of the 3D IC's such as substrate, heat sink, device layer; and the pitch and arrangement of core processors and TSV's as well as the variation of thermal conductivity and heat dissipation of the processors. In their further research, Tavakkoli et al. [32] investigated the thermophysical and geometrical effects of the die, device layer, heat sink, and heat spreader on the thermal performance of 3D IC's. Their findings can be used to design and optimize the 3D IC structures. Wang et al. [39] studied the hotspots of multilayer 3D IC's. In their work, they examined the impact of thermal properties and geometric features.

The review of the open literature shows that there has been quite a number of investigations devoted to analyzing and optimizing the cooling schemes for electronics pieces. However, most attention has been placed on the improvement of the heat sinks; while less work has been directed towards the redesigning and optimization of the structure of the heat spreader to enhance its thermal conductance using high conductivity inserts. Therefore, in the present study, a specified amount of Boron Arsenide, BAs, with thermal conductivity of 1300 W/mK, is distributed as rings and straight blades to decrease the hot spot temperatures throughout the whole IC structure. For this purpose, single and double ring; radial, one-level of pairing, and two-level of pairing straight blade configurations are proposed and optimized. Also, the location of rings and the number of blades at each stage is optimized. Pursuing a parametric study, the architecture of these structures is optimized. Invoking this

innovative method, the size of the heat sink, and heat spreader can be shrunk to the size of the device layer which can be as much as 200%. This is very beneficial when there are space limitations.

Chapter 2

Design and Optimization of Ring Shape Inserts

2.1. Abstract

This study establishes a numerical investigation of the optimal distribution of a limited amount of high thermal conductivity material to enhance the heat removal from 3D integrated circuits, IC. The structure of the heat spreader is designed as a composite of high thermal conductivity (Boron Arsenide) and moderate thermal conductivity (copper) materials. The volume ratio of high conductivity inserts to the total volume of the spreader is set at a fixed pertinent ratio. Two different boundary conditions of constant and variable temperature are considered for the heat sink. To examine the impact of adding high conductivity inserts on the cooling performance of the heat spreader, various patterns of the single and double ring inserts are studied. A parametric study is performed to find the optimal location of the rings. Moreover, the optimal distribution of the high-conductivity material between the inner and outer rings is found. The results show that for the optimal conditions, the maximum temperature of the 3D IC is reduced up to 10%; while at the same time, the size of the heat sink, and heat spreader can be diminished by as much as 200%.

2.2. Problem statement

The heat generated throughout the device layers is transferred via conduction to the heat sink through the heat spreader. For a typical situation, the heat sink and the heat spreader are larger than the electronic component. The schematic of a typical generalized

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three-dimensional IC structure is illustrated in Figure 2.1. This structure is composed of a substrate, thermal interface material (TIM), die, device layer, heat spreader, and heat sink. The device layers are mounted between the TIM layer and the silicon die. Various electronic subsystems are located on the device layer like processor, memory, sensor. It should be noted that heat generation merely occurs inside the device layer. The thermal interface material is used to enhance conductive heat transfer between the device layers and the die so that the insulating effect of the air cavities created at the contact surface of the two solid layers is minimized.

Thermal interface material layer comprised of C4 bumps is used to connect the silicon substrate and the die closest to it, while micro-bump TIM layers are utilized for bonding the device layers with the layer above it. The heat generated in each CPU due to transistor switching is conducted through the layers to the package and then dissipated to the ambient via convective heat transfer.

The nominal values for different components of the 3D IC considered in this study are given in Table 2.1, which have been extracted from Ref. [27]. Silicon is the preferred material used for fabricating electronic chips due to its stability, abundance, and ease of fabrication, while copper is preferred for manufacturing the heat sink and the heat spreader components due to its superior thermal conductivity. The TIM layers, which provide electrical insulation and mechanical support for the bonding of active device layers, are typically made out of composites with high volume fractions of thermally conductive fillers such as Aluminum Oxide. As mentioned earlier, in this work, the variation of pertinent components utilized in the 3D architecture and the generated heat is given in Table 2.1.
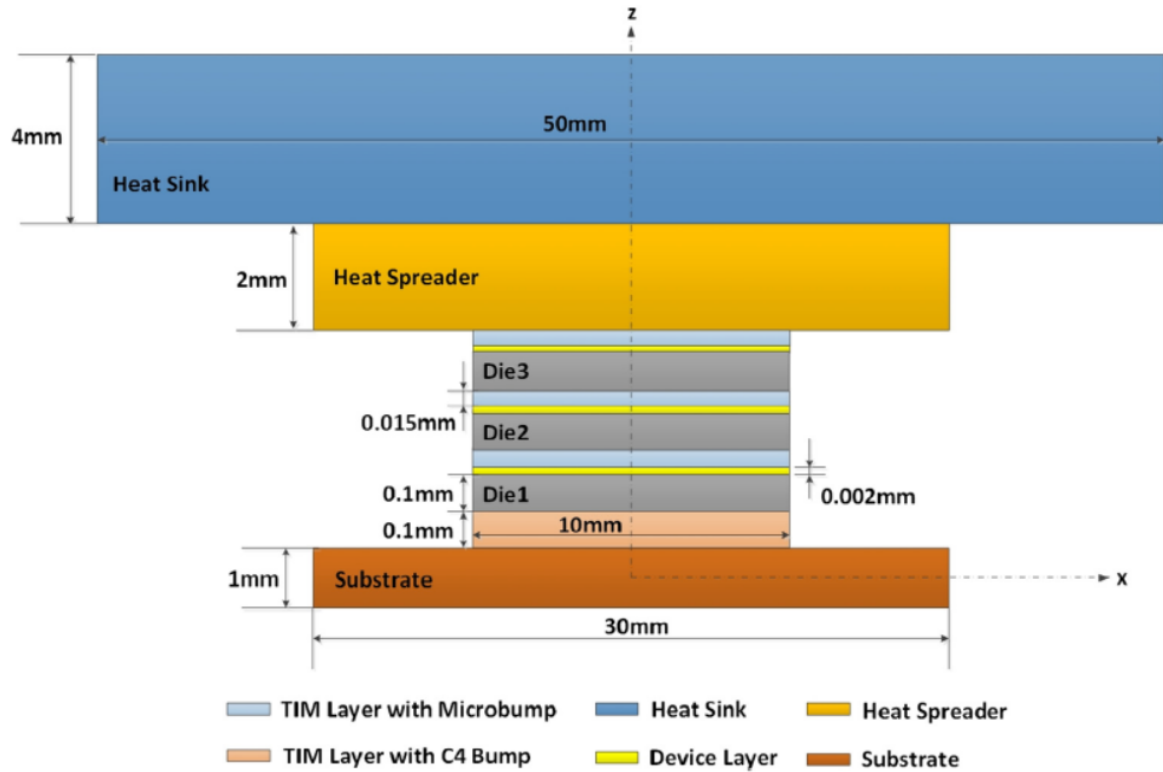
Figure 2.1. Schematic view of the nominal 3D ID structure

The size of the heat spreader and heat sink are typically larger than other layers to extend

the surface area exposed to the cooling fluid and consequently to enhance the heat transfer to the

ambient fluid. However, if there is a space constraint, their cooling performance will be impaired.

As expected, our simulations show that restricting the diameter of the heat spreader decreases the

cooling capability of the heat sink. To overcome this problem, in the present study, we use a rather

limited and practical amount of a high conductivity material to boost the thermal conductance of

the heat spreader. Therefore, this study aims to seek an optimal distribution of the limited amount

of high conductivity materials through the heat spreader to enhance the heat removal of the circular

3D integrated circuits.

Table 2.1. The nominal specifications for different layers for the 3d IC considered in the present study [27]

Layer	Parameter	Nominal value	Unit
Heat spreader	Material	Cu	---
	Diameter	10, 30	mm
	Thickness	2	mm
Chip	Diameter	10	mm
	Number of layers	3	---
TIM layer with microbump	TIM material	Thermal grease	---
	Thermal conductivity	5	$W(mK)^{-1}$
	Thickness	15	μm
TIM layer with C4 bump	TIM material	Thermal grease	---
	Thermal conductivity	5	$W(mK)^{-1}$
	Thickness	100	μm
Die	Material	Si	---
	Thickness	100	μm
Device layer	Material	Si	---
	Thickness	2	μm
Core processor	Material	Si	---
	Total power of cores in each layer	90	W
	Cores per layer	4	---
	Diameter	1	mm
	Thickness	2	μm
Substrate	Material	Si	---
	Diameter	30	mm
	Thickness	1	mm

For this purpose, the impact of adding high-conductivity inserts, various patterns of single and double ring styles on the cooling performance of the heat spreader are studied. This includes, first a parametric study to find the optimal location of the rings. Next, we turn our attention to finding the optimal distribution of the high-conductivity material between the inner and outer rings. Throughout this analysis, the volume ratio of the high conductivity inserts to the total volume of the heat spreader is fixed at 20%. We have shown that changing the percentage

of the high conductivity material does not change the characteristic of the results illustrated in this work.

To analyze the heat transfer throughout the IC, we have considered two thermal boundary conditions at the heat sink. A constant temperature (15 °C) and one which is based on a linearly variable temperature [38]. The purpose is to show the impact of the type of the boundary condition on the performance and optimal structure of the highly conductive inserts for the 3D IC. Each of these B.C.s has a physical counterpart. For example, considering a coolant with a typical inlet temperature and depending on the strength of convective heat transfer coefficient we can have approximately either a constant temperature or a variable temperature B.C. However, as the boundary conditions are presented in non-dimensional form, the values of those conditions do not impact the non-dimensional results achieved in this study. Effectively, we have shown that regardless of the type of the boundary condition, the improvements that we have established based on our proposed design reduce the hotspots.

The heat Spreader material is copper with k=401 W(mK)$^{-1}$, while the high conductivity material is taken as Boron Arsenide with thermal conductivity of 1300 W(mK)$^{-1}$. In this investigation, the high conductivity inserts are taken as rings. A 3D view of a 3D IC using a single ring is shown in Fig. 2.2. Also, when we use a double ring configuration, the high conductivity material is split between the rings equally unless mentioned otherwise. The thickness of the inserts is similar to that of the heat spreader.

Figure 2.3 illustrates the proposed design for the present study. This figure represents a composite having a double layer HCI.
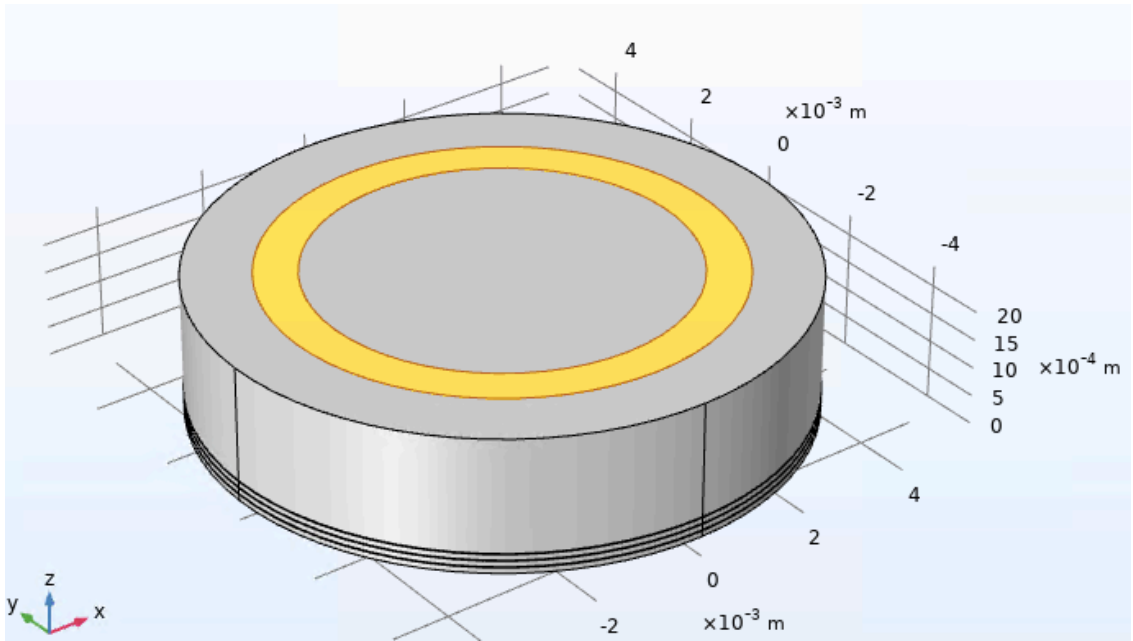
Fig. 2.2. A 3D view of the 3D IC using a single ring
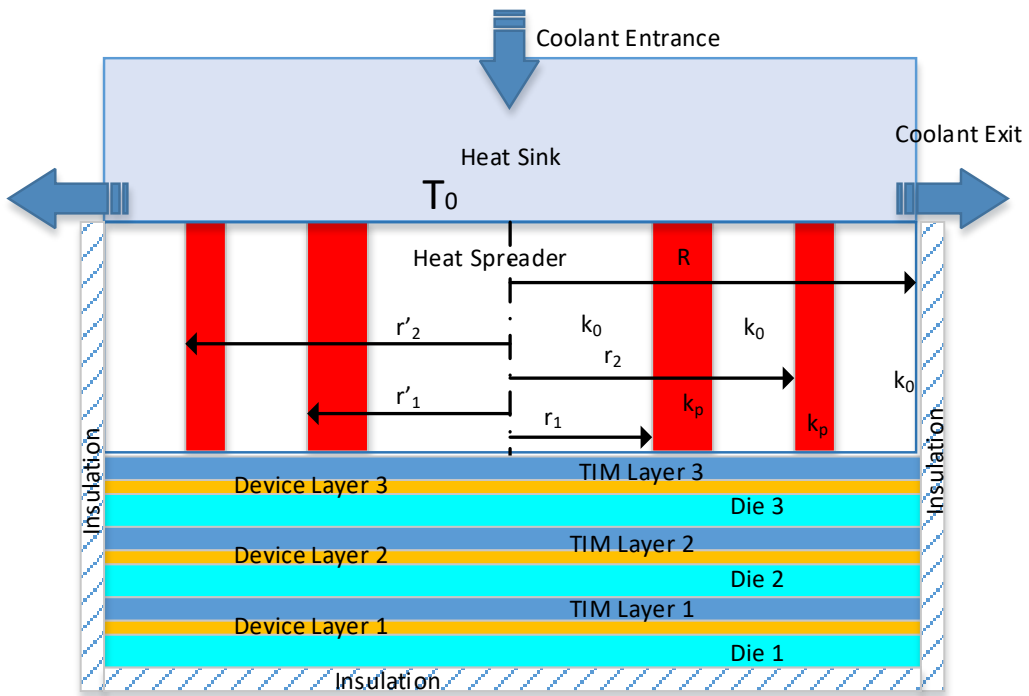
Figure 2.3. Schematic of a 3D IC structure with two-layers of high-conductivity inserts within the heat spreader

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2.3. Modeling and Analysis

2.3.1. Governing equations

The energy transport throughout the 3D IC is via conduction with convection at the outer boundaries. The three-dimensional, steady-state governing equations in the cartesian coordinate system can be written as

$$\frac{\partial^2 T^*}{\partial x^{*2}} + \frac{\partial^2 T^*}{\partial y^{*2}} + \frac{\partial^2 T^*}{\partial z^{*2}} + \dot{q}_g^* = 0 \tag{2.1}$$

where $\dot{q}_g^*$ denotes the volumetric heat generation inside each piece. This term is non-zero in the heat generating layers. The nondimensionalized coordinates, volumetric heat generation, and temperature and coordinates are

$$x^* = \frac{x}{H}, \quad x^* = \frac{y}{H}, z^* = \frac{z}{H}, \tag{2.2}$$

$$\dot{q}_g^* = \frac{\dot{q}_g H^2}{k(T_{max,0} - T_0)} \tag{2.3}$$

$$T^* = \frac{T - T_0}{T_{max,0} - T_0} \tag{2.4}$$

The boundary condition for the lower boundary of the substrate of the 3D IC is effectively akin to an adiabatic condition due to the low thermal conductivity. Two boundary conditions for the heat sink are considered as:

First B. C.: $T_0 = 15 \ [°C]$ (2.5)

Second B. C.: $T_0 = 10\left(\frac{r}{R}\right) + 15 \ [°C]$ (2.6)

where in the non-dimensional form, they can be written as

First B. C.: $T_0^* = 0$ (2.7)

Second B. C.: $T_0^* = \frac{10r^*}{T_{max,0} - T_0} = \frac{10r^*}{62.7 - 15} = 0.21r^*$ (2.8)

There is natural convection around the 3D IC. The B.C. at the peripherical surface of the IC is stated in the following non-dimensional form:

$$\frac{\partial T_s^*}{\partial n} = -Bi(T_s^* - T_\infty^*) \tag{2.9}$$

where n is the normal unit vector and Bi is the dimensionless Biot number defined as:

$$Bi = \frac{hR}{k} \tag{2.10}$$

and T_∞ is the ambient temperature ($T_\infty = 300K$).

To model the natural convection around the 3D IC, the continuity, Navier-Stokes, and energy equations are solved. These equations are given below in Cartesian coordinates.

Continuity equation:

$$\frac{\partial u^*}{\partial x^*} + \frac{\partial v^*}{\partial y^*} + \frac{\partial w^*}{\partial z^*} = 0 \tag{2.11}$$

x-momentum conservation equation

$$Re_H \left(u^* \frac{\partial u^*}{\partial x^*} + v^* \frac{\partial u^*}{\partial y^*} + w^* \frac{\partial u^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial x^*} + \left(\frac{\partial^2 u^*}{\partial x^{*2}} + \frac{\partial^2 u^*}{\partial y^{*2}} + \frac{\partial^2 u^*}{\partial z^{*2}} \right) \tag{2.12}$$

y-momentum conservation equation

$$Re_H \left(u^* \frac{\partial v^*}{\partial x^*} + v^* \frac{\partial v^*}{\partial y^*} + w^* \frac{\partial v^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial y^*} + \left(\frac{\partial^2 v^*}{\partial x^{*2}} + \frac{\partial^2 v^*}{\partial y^{*2}} + \frac{\partial^2 v^*}{\partial z^{*2}} \right) \tag{2.13}$$

z-momentum conservation equation

$$Re_H \left(u^* \frac{\partial w^*}{\partial x^*} + v^* \frac{\partial w^*}{\partial y^*} + w^* \frac{\partial w^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial z^*} + \left(\frac{\partial^2 w^*}{\partial x^{*2}} + \frac{\partial^2 w^*}{\partial y^{*2}} + \frac{\partial^2 w^*}{\partial z^{*2}} \right) \tag{2.14}$$

energy conservation equation:

$$Pe_H \left(u^* \frac{\partial T^*}{\partial x^*} + v^* \frac{\partial T^*}{\partial y^*} + w^* \frac{\partial T^*}{\partial z^*} \right) = \left(\frac{\partial^2 T^*}{\partial x^{*2}} + \frac{\partial^2 T^*}{\partial y^{*2}} + \frac{\partial^2 T^*}{\partial z^{*2}} \right) \tag{2.15}$$

2.3.2. Non-Dimensionalization

The governing equations were nondimensionalized as follows:

$$u^* = \frac{u}{u_m} \quad v^* = \frac{V}{u_m} \quad w^* = \frac{w}{u_m} \quad p^* = \frac{pH}{\mu_f u_m} \quad Re_H = \frac{\rho_f u_m H}{\mu_f} \quad Pe = \frac{\rho_f C_{p,f} u_m H}{k_f} \tag{2.16}$$

To extend the application of the results of this study, the following dimensionless variables are defined and used in this study.

$$r^*=r/R;\ z^*=z/L;\ \phi = \frac{V_{HCI}}{V_{Spreader}}\ ;\quad P = \frac{V_{HCI1}}{V_{HCI2}} \tag{2.17}$$

where, r^*, z^*, ϕ, and P are dimensionless radius, dimensionless height, volume fraction, and volume ratio, respectively. Volume ratio shows how much HCI is allocated to the inner and outer rings, in the double-ring configuration. The value of the volume fraction is fixed at 0.2 throughout this study.

Dimensionless Temperature is defined as

$$T_{max}^* = \frac{T_{max}-T_0}{T_{max,0}-T_0} \tag{2.18}$$

Where, T_0 designates the minimum temperature of the heat sink (Temperature of the Heat Sink Center, 15°C), T_{max} is the maximum temperature of the 3D IC with composite heat spreader (with high conductivity insert), and $T_{max,0}$ is the maximum temperature of the 3D IC with plain heat spreader (without high conductivity insert). This dimensionless variable shows the effectiveness of utilizing HCI in cooling the 3D IC. According to this definition, T_{max}^* is always less than unity.

2.3.3. Numerical simulation

Ansys CFX commercial software is used for simulation. Convergence is achieved when the residuals of energy equations become less than 10^{-8}. To check the grid independence, the number of grids is doubled until a deviation of less than 1% is observed in the minimum temperature for the last two sets of grid distributions. Four grid distributions have been

created for this study which are shown in Table 2.2. The minimum temperature of the 3D

IC is selected as the criterion to find the appropriate grid distribution. This parameter is the

most sensitive factor to grid changes as well as it is more liable to mesh sizing for the

second boundary condition. In Table 2.2, ΔT_{min} is equal to the difference of the minimum

temperature of the IC predicted by the mesh setup in a given row and the minimum

temperature computed from the coarser grid in the prior row. Based on the data shown in

Table 2.2, Grid set #3 is selected for our simulations.

Table 2.2. Study of the independence of the results from the solution grid

Grid Case no.	Number of cells	T_{min}	ΔT_{min}
1	33765	15.70	---
2	63615	15.49	0.21
3	126400	15.34	0.15
4	239294	15.29	0.05

2.3.4. Validation

A cylinder with L/D=0.5 is considered for which the bottom and peripheral surfaces are

held at $T_\infty = 40°C$ and the top surface is kept at $T_0 = 15°C$. An analytical solution is

available for this problem, which is used as a criterion for the accuracy and validity of the

numerical method.

The analytical solution for this problem can be stated as [40]:

$$T(r,z) = T_\infty + 2(T_0 - T_\infty)\sum_{n=1}^{\infty}\left(\frac{\sinh\lambda_n z}{\sinh\lambda_n L}\right)\frac{J_0(\lambda_n r)}{(\lambda_n R)J_1(\lambda_n R)} \qquad (2.19)$$

where λ_n are roots of the equation $J_0(\lambda_n R) = 0$; r is the radial distance measured from the

center, and Z is the altitudinal distance measured from the bottom surface.

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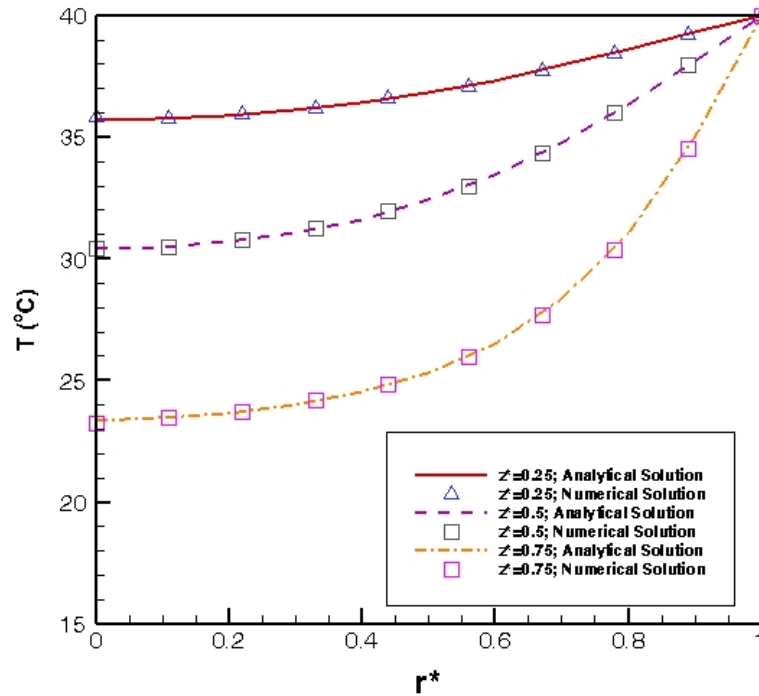
Figure 2.4. Comparison of the numerical temperature predictions with analytical results

Figure 2.4 illustrates the comparison between the current numerical results and the analytical counterparts at three dimensionless heights: z*=z/L=0.25, 0.50, 0.75. As can be seen, an excellent agreement is observed.

2.4. Results and discussion

To show the significance of the present work, the following cases (without HCI) are first investigated.

   a) A 3D IC with a heat spreader diameter of 30 mm for constant boundary condition.

   b) A 3D IC with a heat spreader diameter of 10 mm (equal to the diameter of the main piece) for the same boundary condition.

The results show that for the first and second boundary conditions, the maximum temperatures for case b are 1.1 ºC and 8.6 ºC higher than that of the case a, respectively.

This highlights the importance of invoking the proposed configuration especially when the size of the heat sink has to be limited.

In our analysis, the configuration for the high conductivity inserts (HCI) is taken as a ring. First, all of the HCI is lumped onto a single ring. Having examined different locations of the ring, the temperature distribution and max temperature of the 3D IC are obtained.

Next, the same volume of HCI is divided equally into two rings and following a similar procedure for the first step, the architecture/location of the rings are determined. Finally, for each heat sink boundary condition, the optimal distribution factor for every optimized location is found.

Figure 2.5 illustrates the dimensionless maximum temperature, T^*_{max}, of the IC structure utilizing a single layer of high-conductivity insert for both B.Cs. From this figure, it is evident that there are optimum locations for high conductivity inserts for both types of boundary conditions. However, these locations do not coincide.

When the high conductivity insert is located at the center, the hotspots appear at the edge of the setup. Since the volume of the HCI is fixed, the radial ring thickness decreases when we move away from the center. As the high conductivity ring approaches the hot spot there is an optimum point that when the ring passes that point, the hotspot relocates towards the inner part. These aspects are clarified in Figs. 2.6-2.8.
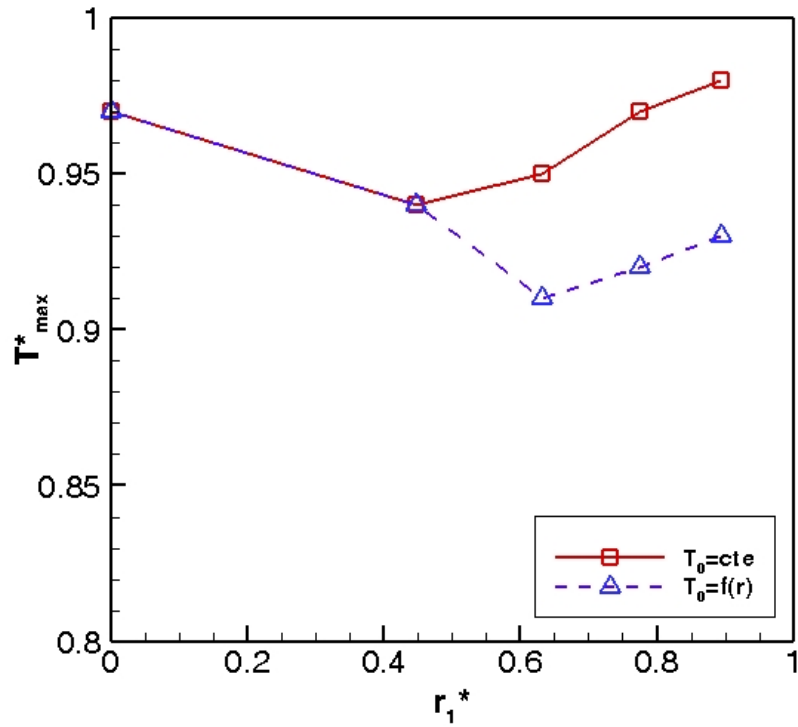
Figure 2.5. Maximum temperature of the IC structure for the two boundary conditions utilizing a single layer of the high-conductivity insert
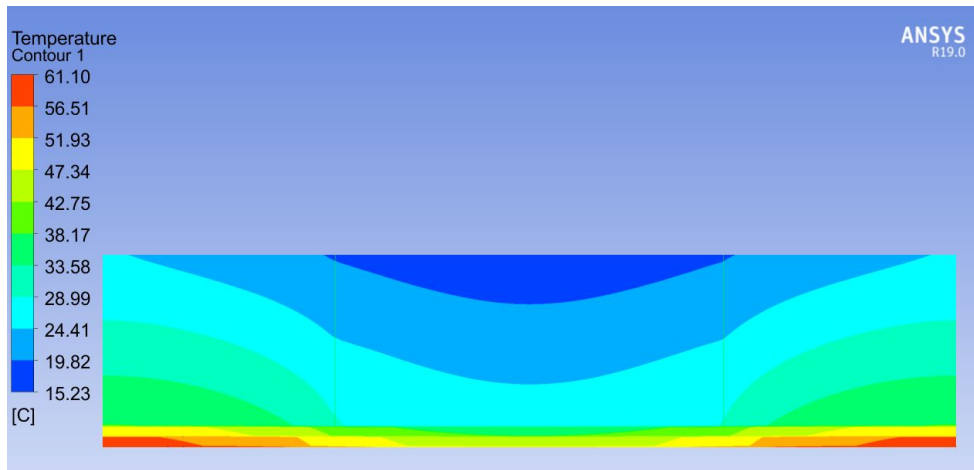
Figure 2.6. Temperature counters of the IC structure using a single layer of the high-conductivity insert for $r^*_1=0$ and $T_0=f(r)$
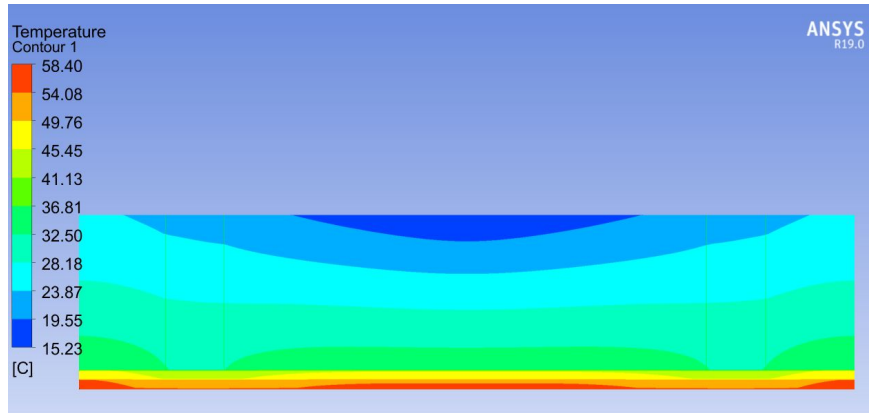
Figure 2.7. Temperature contours for the IC structure utilizing a single layer of high-conductivity insert for r^*_1=0.632 and T_0=f(r)
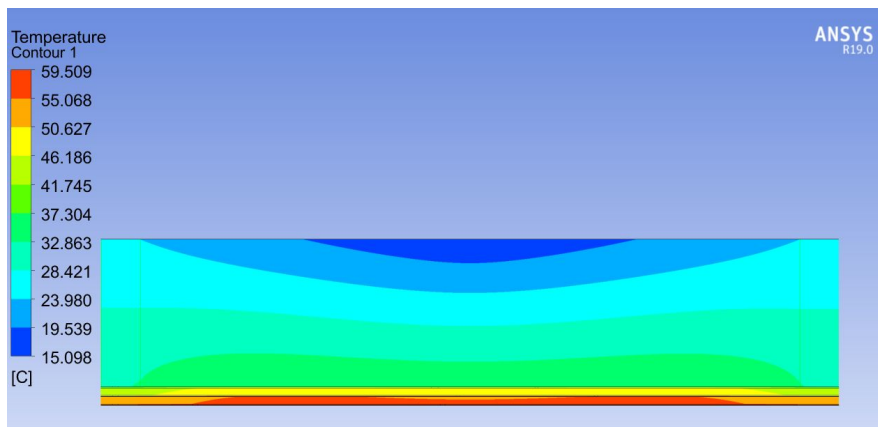
Figure 2.8. Temperature contours for the IC structure using a single layer of high-conductivity insert for r^*_1=0.894 and T_0=f(r)

It should be noted that the locations of the extrema depend on the heat sink boundary condition. That is, when there is a constant temperature B.C for the heat sink, the optimum point for the inserted ring resides closer to the center. This is because the heat sink temperature at the outer part of the piece for the second B.C.is higher than that of the first boundary condition which in turn results in a lower temperature gradient at those parts. As such, by moving the high conductivity ring closer to the edge, this lower temperature gradient is compensated by the higher thermal conductivity. As expected, the value of the

maximum temperature is different for the two boundary conditions. However, the value of the dimensionless maximum temperatures is the same for both B.Cs.. For instance, when the high conductivity insert is located at the center, the max temperature would be 53.85°C and 63.10°C for the first and second B.C respectively. While the value of the dimensionless Max. temperature is 0.97 for both boundary conditions. The dimensionless maximum temperature indicates the effectiveness of utilization of the high conductivity insert in cooling the 3D ICs. For the optimized conditions, the dimensionless maximum temperatures are 0.94 and 0.91, for first and second B.Cs., respectively. Whereas, the dimensionless maximum temperature for plain heat spreader (without high-conductivity insert) of triple diameter (30 mm) is 0.97. This highlights the significant role of HIC in cooling the 3D ICs.

To have a better insight into the impact of high conductivity insert on the temperature distribution throughout the 3D IC, the temperature contours for different configurations of the structure including single HCI are shown in Figs. 2.6-2.8. Figure 2.6 represents the temperature contours of the IC structure utilizing a single layer located at the center of the piece based on the second heat sink B.C. This figure indicates that the hotspot location is at the edge of the piece. Further, the sharp variation in contour slope designates the change in the thermal conductivity.

Figure 2.7 shows the temperature contours of the IC structure with a single layer of high-conductivity insert for $r_1^* = 0.632$ based on the second boundary condition for the heat sink. This contour corresponds to the optimum configuration of a single ring spreader. In this situation, the distribution of the temperature for the IC is more uniform than the other

configuration. It should be noted that we have nearly two hot spots for this case. One is located at the edge while the other is located at the center of the IC. The advantage is that the hot spot temperature has been reduced.

Figure 2.8 shows the temperature contours for the IC structure with a single layer of high-conductivity insert located at the outermost radius of the spreader for the second boundary condition. The location of the hotspots is moved close to the central part. The maximum temperature does not exactly occur at the center since the temperature of the heat sink experiences its minimum at the coolant entrance (center of the heat sink). This is not the case for the first B.C. due to the constant heat sink temperature since the temperature increases with distance from the high conductivity ring.

Figure 2.9 presents the maximum temperature of the IC structure invoking two layers of the high-conductivity insert when the external ring location is pinned at the edge of the spreader. The result shows that for the first B.C., the optimized location for the first ring is at the center. This means that the farther away these two rings are, the better cooling performance is achieved.

Regarding the second B.C., there is a fixed ring at the outer edge. If the second ring is too close to the center, it will deviate from the optimal conditions since the temperature gradient is maximum at the center. That is, in going from the center towards the perimeter, the temperature gradient is reduced while the equivalent thermal conductivity is enhanced. Therefore, the optimal conditions occur when the internal ring is dislocated from the center of the heat spreader.

Figure 2.9. Maximum temperature of the IC structure for the two boundary conditions using two layers of high-conductivity insert for r'$_2$=R.

Based on the result shown in Fig. 2.9, the next step in improving the configuration is by fixing the location of the internal HCI at the center of the spreader. Figure 2.10 shows that the maximum temperature of the IC structure with two layers of the high-conductivity insert when the internal HCI is fixed in the center of the spreader, while the outer ring location is varied to yield the optimal configuration. The behavior of the dimensionless maximum temperature for both boundary conditions is similar. However, the effectiveness of utilizing HCI is better for the first B.C. For both B.Cs, the optimal structure is achieved when the second ring is located at $r_2^* = 0.774$.

Figure 2.10. Maximum temperature of the IC structure for the two boundary conditions using two layers of high-conductivity insert for $r_1=0$.

Figure 2.10 is based on the second B.C. as compared to Fig. 2.9. For both configurations, the internal ring is located at the center, while the location of the outer one is different. Figure 2.10 demonstrates that the location of the outer ring observed in figure 2.9 (which had been fixed) is not optimal; that is if we let the structure morph, the optimal location of Fig. 2.10 will be obtained.

Two opposite effects emerge when dislocating the outer ring towards the perimeter. First, the distance between the HCI ring increases which tends to make the temperature distribution of the IC structure more uniform. Second, the radial thickness of the outer ring is reduced which leads to attenuated thermal conduction. These two contradicting features produce an optimal location for the outer ring.
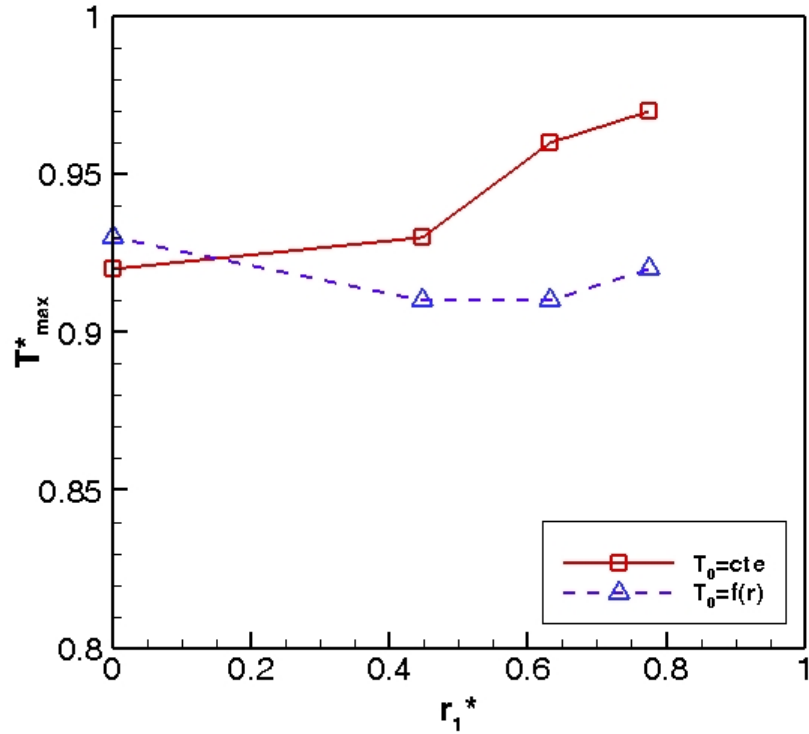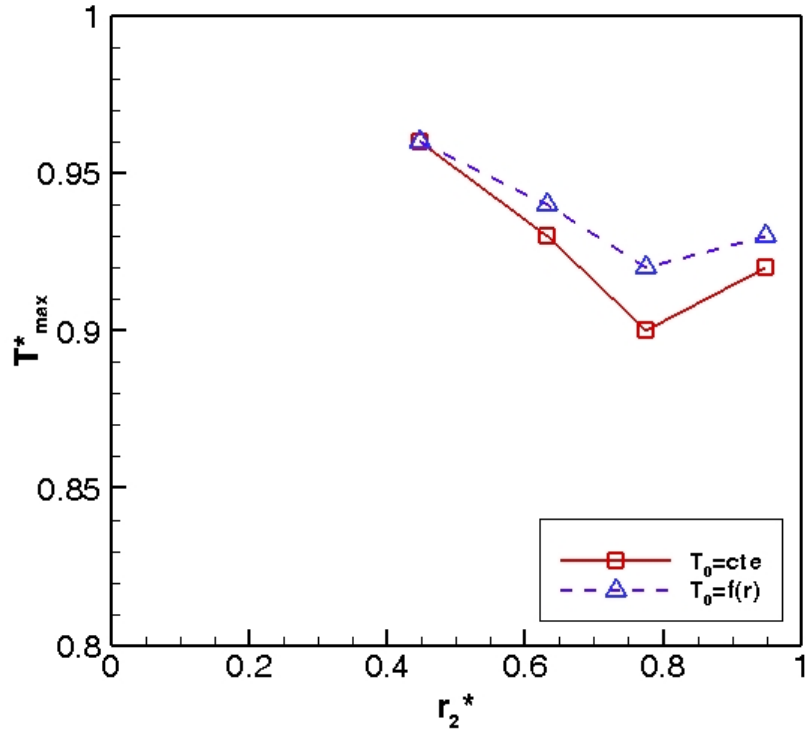
Figure 2.11. Maximum temperature of the IC structure for the two boundary conditions using two layers of high-conductivity insert for $r_1=0.25r_2$.

Figure 2.11 displays the maximum temperature of the IC structure with two layers of high-conductivity inserts for $r_1 = 0.25r_2$. It is observed from this figure that the best location for the outer ring is the same for both boundary conditions at $r_2^* = 0.774$. The spacing between the successive rings is:

$$\Delta r = r_2 - r_1 = r_2 - 0.25r_2 = 0.75r_2 \qquad (2.20)$$

Therefore, the spacing between the rings increases as the outer ring radius increases, which has a favorable effect; since it tends to make the temperature more uniform. On the other hand, similar to Fig.2.10, higher values of r_2 lead to thinner HCI rings which deteriorates the cooling efficacy. This means that an optimal location for the rings does exist. Also seen in this figure is the behavior of the second B.C. As it can be seen, when r_2 surpasses the

optimum point of $r_2^* = 0.774$, T_{max}^* does not vary remarkably. For this Boundary condition, the temperature gradient is reduced as we move towards the edge. Hence, it is better to bring the ring closer to the edge. In Figure 2.10, it is seen that the curve before the optimum point is steeper than the curve after that which implies that the effect of distancing the rings is more pronounced at lower values of the rings' radii.

Figure 2.12 presents the maximum temperature of the IC structure invoking two layers of high-conductivity inserts for $r_1 = 0.50r_2$. It is interesting to note that both curves are optimal in a range of ring radii rather than a single specified radius. Therefore, an optimum design exists. It is also seen that the effectiveness of using HCI as a heat spreader is not sensitive to the boundary condition for an optimal situation.

Figure 2.12. Maximum temperature of the IC structure for the two boundary conditions using two layers of high-conductivity insert for r₁=0.50r₂.
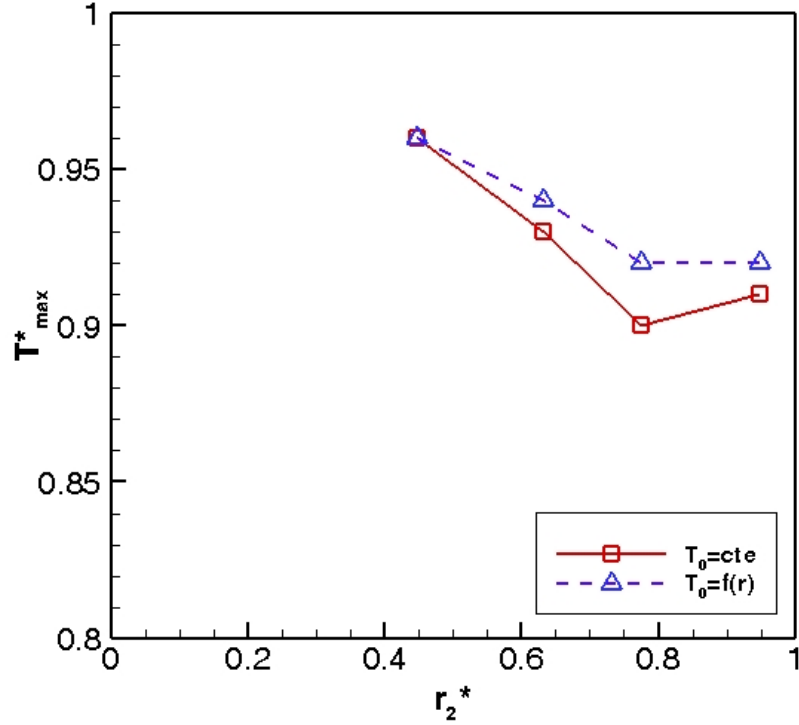
Figure 2.13. Maximum temperature of the IC structure for the two boundary conditions using two layers of high-conductivity insert for $r_1=0.75r_2$.

Next, the correlation between the locations for the two rings is taken as $r_1 = 0.75r_2$, which means the successive rings reside closer to each other. Therefore, if the rings are not placed far enough from the center, they would be merged. Thus, we cannot convey this condition for low values of r_1 and r_2. The results for this case are shown in Fig 2.13.

Since the values of r_1 and r_2 are beyond a threshold, the impact of distancing the rings is less than the effect of reducing the thickness of the rings. Therefore, for the first B.C., an ascending trend is observed when r_1 and r_2 are increased. On the contrary, for the second boundary condition, as the temperature gradient plays a role in the thermal conduction, a minimal value for T_{max}^* is obtained concerning r_1 (or r_2).

Finally, the optimal configuration of the composite heat spreader obtained is adopted for further optimization for the volume ratio. The optimal configurations for the first and second B.C. are as follows;

$$r_1^* = \begin{cases} 0.194 & first\ B.C \\ 0.580 & second\ B.C \end{cases} \tag{2.21}$$

$$r_2^* = 0.774 \qquad Both\ B.Cs \tag{2.22}$$

Having fixed the locations of the rings, the maximum temperature of the 3D IC is achieved for various volume ratios. The results are illustrated in Fig 2.14.
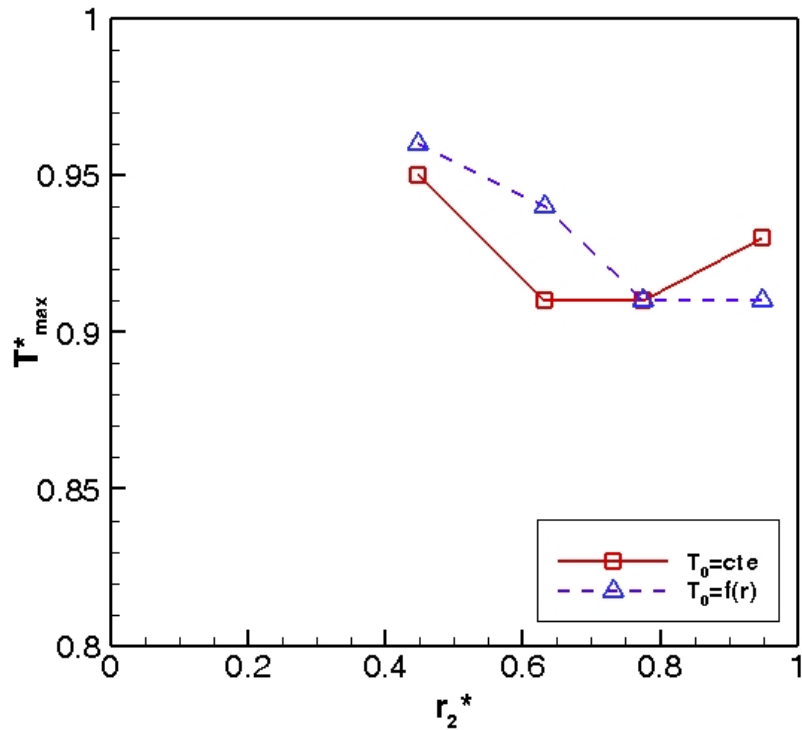

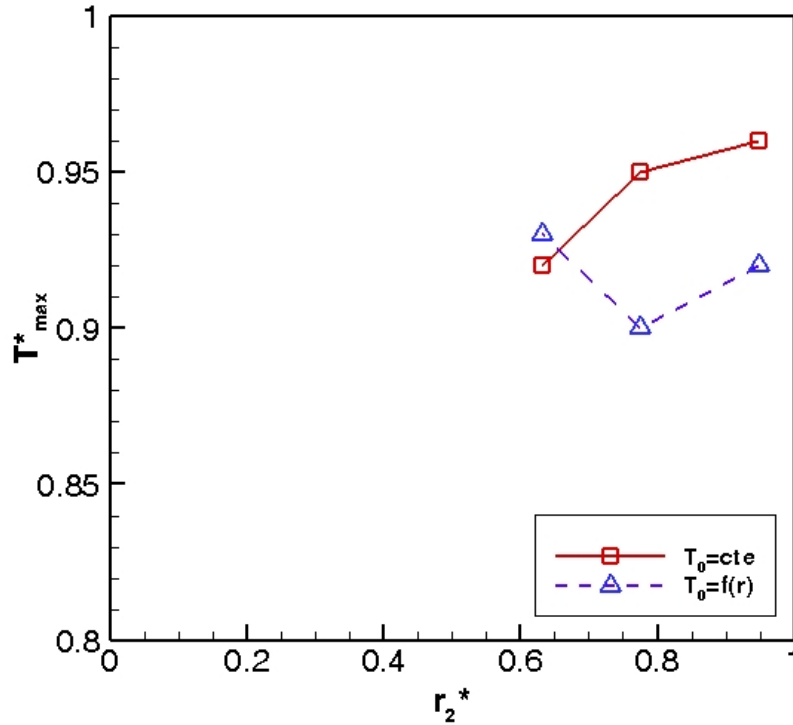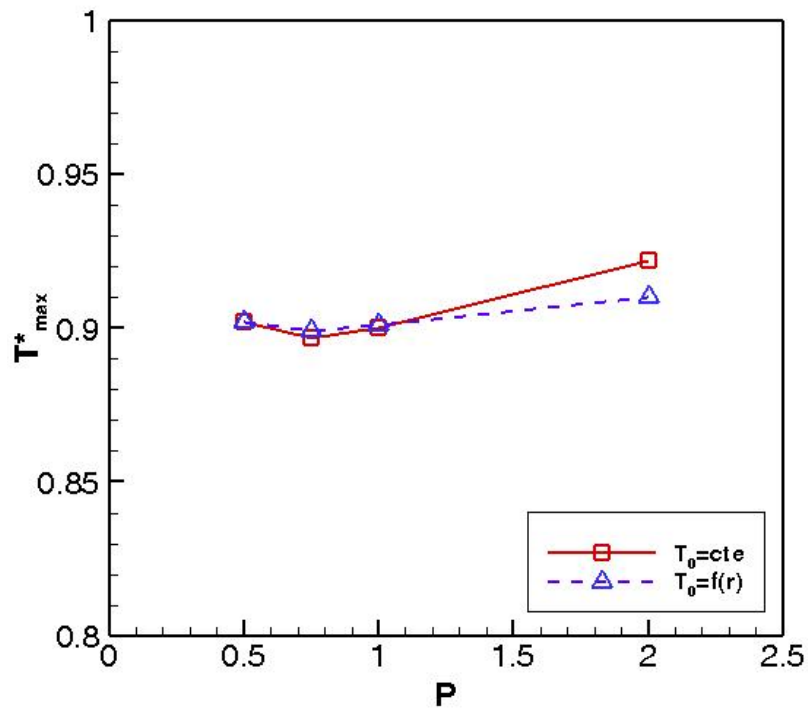Figure 2.14. Maximum temperature of the optimal IC structures for the two boundary conditions using two layers of high-conductivity inserts with different volume ratios.

According to this figure, there exists a volume ratio for which the configuration is optimized, again. This optimal volume ratio is 0.75 for both B.Cs. That is to achieve the most optimum cooling of the 3D IC, we need to allocate more HCI to the outer rings. As the outer ring has a larger inner radius, if we want to have a balanced thickness over the rings, more HCI should be allotted to the outer ring. If the amount of HCI for the outer ring exceeds a limit, again the balance between the rings will be violated which will lead to an attenuated result. The final optimal results for the aforementioned B.C.s are:

$$r_1^* = \begin{cases} 0.194 & 1^{st}\ B.C \\ 0.580 & 2^{nd}\ B.C \end{cases} \tag{2.23}$$

$$r_2^* = 0.774 \qquad P = 0.75 \tag{2.24}$$

This means that for this final optimal condition, the dimensionless maximum temperature is reduced by more than 10% which corresponds to more than a 4°C decrease in the maximum temperature of the 3D IC.

Chapter 3

Geometrical Optimization of Blade Type Boron Arsenide Inserts

3.1. Abstract

This investigation is aimed at the design and optimization of Boron Arsenide insert structures embedded in the heat spreader of a 3D IC. The inserts are distributed in three main configurations: radial, one level of pairing, and two levels of pairing. The considered heat spreader is constituted of a composite of copper and highly conductive blades made of Boron Arsenide with high thermal conductivity. The structures corresponding to the lowest maximum temperature of the 3D IC while the ratio of the Boron Arsenide volume to the whole heat spreader volume is fixed, are established. Four different boundary conditions are examined to seek their impact on the optimal configuration of the inserts. The results show that for the constant temperature, variable temperature, convection heat transfer boundary conditions at optimal conditions, the maximum temperature of the whole structure (the structures have not been defined) can be reduced by 13.7, 11.9, and 13.9%, respectively; while the size of the heat sink, and heat spreader is mitigated 200%.

3.2. Problem statement

In 3D ICs thermal energy is generated in the thin device layers. This energy needs to be removed by conducting through the heat spreader and onto the heat sink. A typical 3D IC is composed of the heat sink, heat spreader, die, thermal interface material (TIM),

substrate, and the device layer. Table 3.1 presents the specification of a typical 3D IC which has been considered in the present study. This table is prepared based on ref. [4]. More details regarding 3D IC's, are provided in references [4& 9].

Table 3.1. The nominal specifications for different layers for the 3D IC considered in the present study [27]

Layer	Parameter	Nominal value	Unit
Heat spreader	Material	Cu	---
	Diameter	10, 30	mm
	Thickness	2	mm
Chip	Diameter	10	mm
	Number of layers	3	---
TIM layer with microbump	TIM material	Thermal grease	---
	Thermal conductivity	5	$W(mK)^{-1}$
	Thickness	15	μm
TIM layer with C4 bump	TIM material	Thermal grease	---
	Thermal conductivity	5	$W(mK)^{-1}$
	Thickness	100	μm
Die	Material	Si	---
	Thickness	100	μm
Device layer	Material	Si	---
	Thickness	2	μm
Core processor	Material	Si	---
	Total power of cores in each layer	90	W
	Cores per layer	4	---
	Diameter	1	mm
	Thickness	2	μm
Substrate	Material	Si	---
	Diameter	30	mm
	Thickness	1	mm

The heat spreader size is usually larger than the device layers to facilitate the heat transfer; however, this impedes the accommodation of the 3D ICs at micro applications where the available space is restricted. Our previous study has shown that limiting the diameter of the heat spreader weakens the cooling potential of the heat sink. To tackle this issue, a special amount of a high conductivity material is utilized. For this purpose, 20% of the volume of the heat spreader is allocated to Boron Arsenide which is a high conductivity material with thermal conductivity of 1300W/mK; while the remaining part of the heat spreader is occupied by copper with thermal conductivity of 400W/mK.

We have observed that increasing the percentage of the high conductivity material beyond 20% does not affect the pattern of the optimal configuration of the high conductivity inserts remarkably.

This study aims to find the optimal configuration of the high conductivity inserts throughout the heat spreader. For this purpose, three main structures are considered: radial, one level of pairing and two levels of pairing. In all of the configurations, the thickness of the inserts is the same as the thickness of the heat spreader.

In the radial configuration, inserts reside as straight blades connecting the center of the heat spreader to its perimeter as shown in Figure 3.1. This figure shows a radial configuration for 16 inserts. To optimize this configuration, the number of blades is doubled while their thickness is halved. This procedure is continued until its effect on the maximum temperature of the 3D IC is negligible.
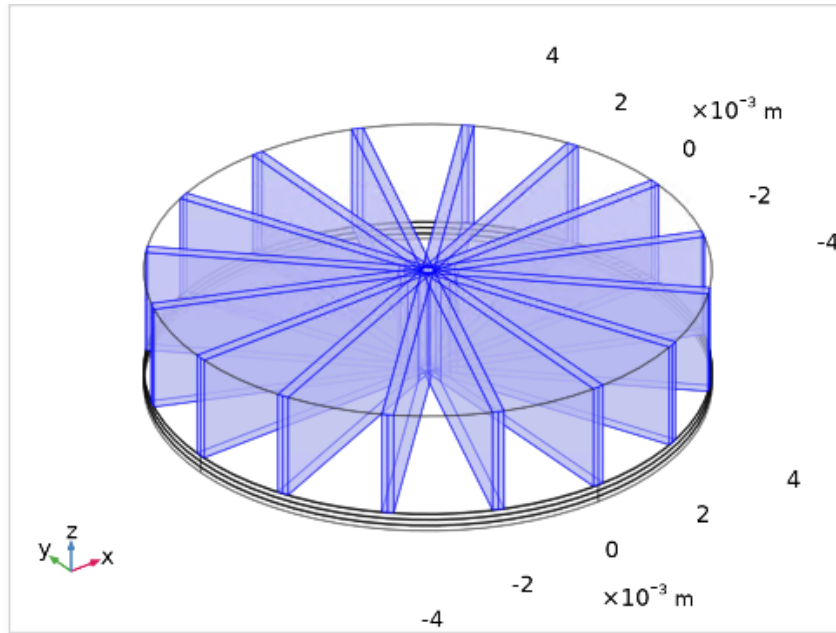
Figure 3.1. Schematic of a radial configuration with 16 blades

For the one level of pairing configuration, the radial inserts break into outer inward and inner outward incomplete blades inside the heat spreader. Figure 3.2.a illustrates this configuration for 16 inner blades (N_1=16) and 16 outer blades (N_2=16); while figure 3.2.b shows the case for N_1=16and N_2=32. Thus, the angular location of these two sets of inserts can vary independently: providing one more degree of freedom for the optimization process. The location of this breakout is another degree of freedom.

For the two levels of pairing structure, the breakout occurs twice: giving two more degrees of freedom for the optimization. Figure 3.3.a illustrates this configuration for 16 inner blades ($N_1 = 16$), 16 middle blades ($N_2 = 16$), and 16 outer blades ($N_3 = 16$); while figure 3.3.b shows the case for $N_1 = 16$, $N_2 = 16$, and $N_3 = 32$.
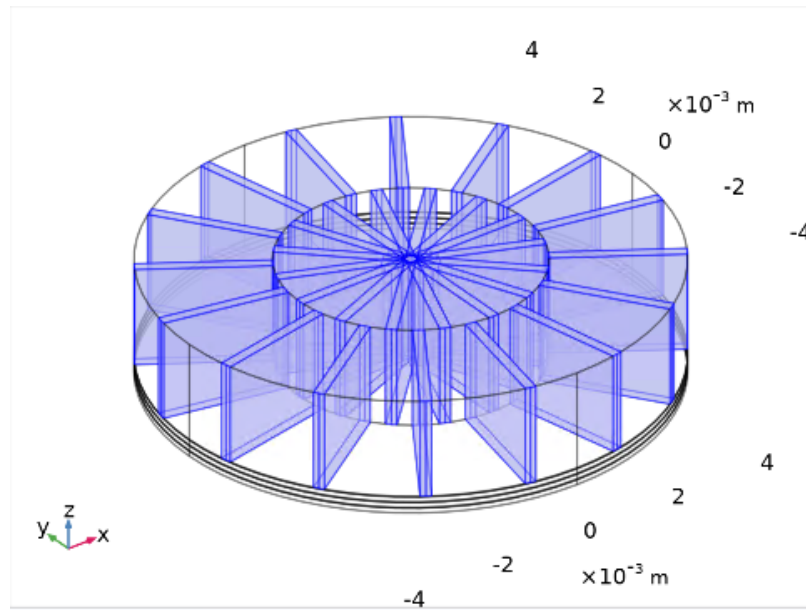
(a)
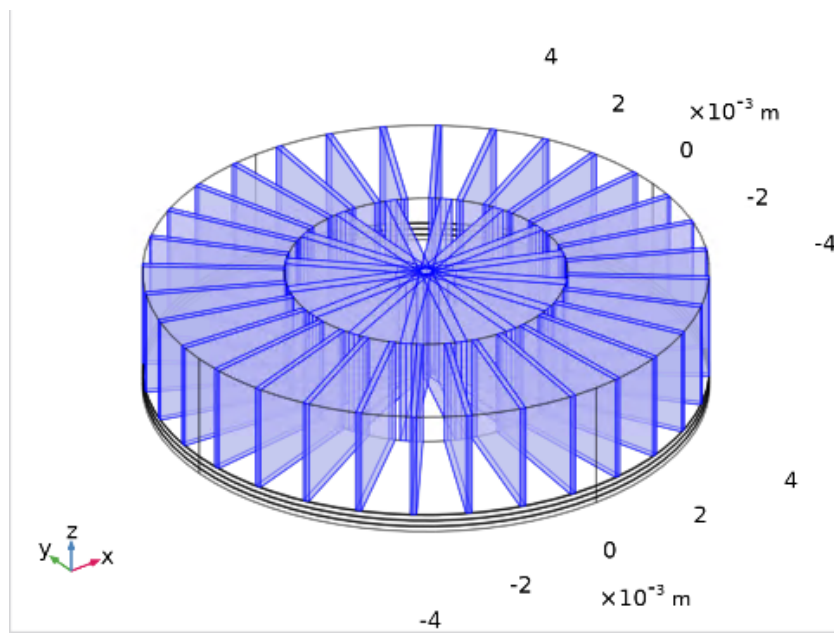
(b)

Figure 3.2. Schematic of one level of pairing configurations with $N_1 = 16$ and a) $N_2 = 16$, b) $N_2 = 32$

We would like to see examine various aspects of these configurations. For example, we want to see of increasing the degrees of freedom, can significantly enhance the heat transfer.

For the heat sink, four distinctive boundary conditions are considered: namely, constant temperature (15 ºC) [15], linear variable temperature (between 15 ºC at the center and 25 ºC at the edge), convection heat transfer with $h = 100 \frac{W}{m^2 K}$ and convection heat transfer with $h = 80 \frac{W}{m^2 K}$. The chosen variety of the boundary conditions will enable us to examine their impact on the performance and optimal structure of the highly conductive inserts for the 3D IC. Each of these B. C's has a physical counterpart. Moreover, as the boundary conditions are presented in non-dimensional form, the absolute values of the temperature at the boundary do not impact the non-dimensional results achieved in this study.

3.3. Modeling and Analysis

3.3.1. Governing equations

Heat is generated throughout the device layers of a 3D IC and is dissipated at the heat sink with convection at the outer peripheral boundaries. The thermal energy is transmitted throughout the different layers and the heat spreader of the 3D IC via conduction. The underlying problem in the present research is three-dimensional and steady state. Therefore, the governing equation for the conduction part in the cartesian coordinate system is,

$$\frac{\partial^2 T^*}{\partial x^{*2}} + \frac{\partial^2 T^*}{\partial y^{*2}} + \frac{\partial^2 T^*}{\partial z^{*2}} + \dot{q}_g^* = 0 \qquad (3.1)$$
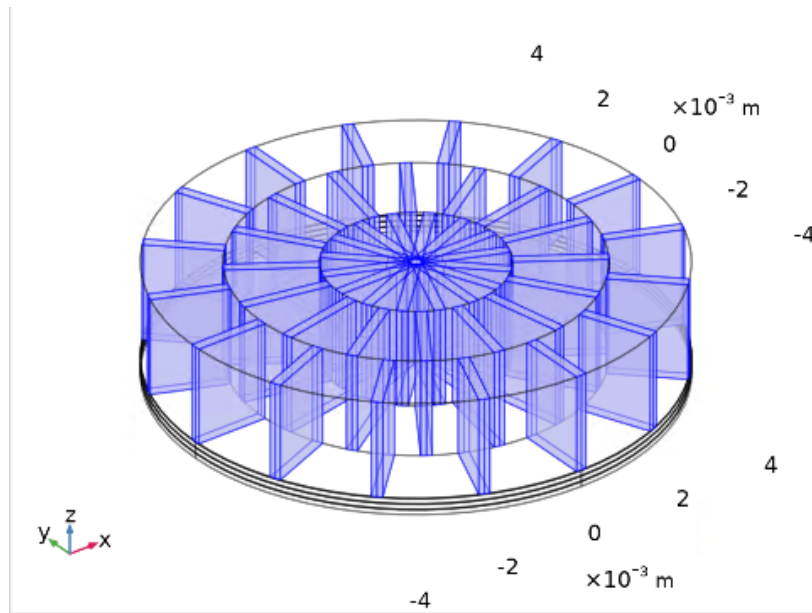
(a)
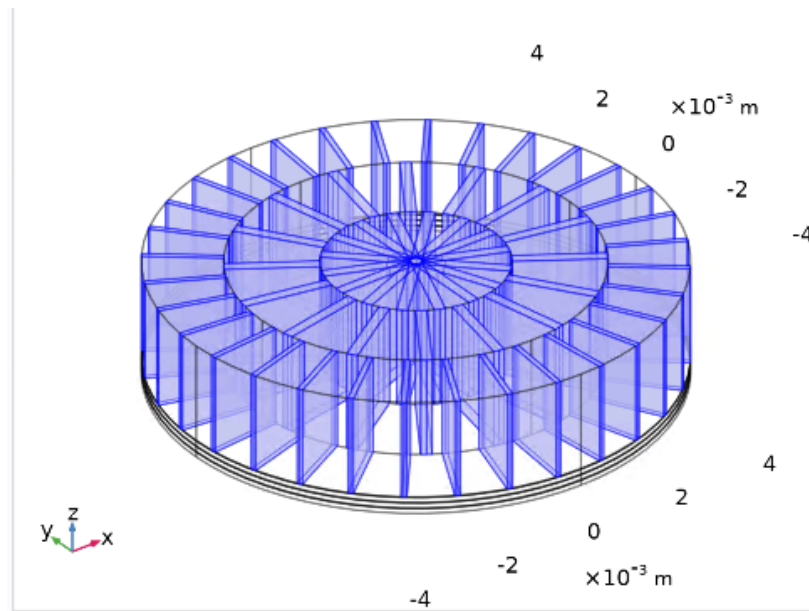
(b)

Figure 3.3. Schematic of two levels of pairing configurations with $N_1 = 16$, $N_2 = 16$, and a) $N_3 = 16$, b) $N_3 = 32$

where $\dot{q}_g^*$ designates the volumetric heat generation inside each piece. This term is only non-zero in the device layers where heat is generated. The nondimensionalized coordinates, volumetric heat generation, and temperature and coordinates are:

$$x^* = \frac{x}{H}, \quad y^* = \frac{y}{H}, z^* = \frac{z}{H}, \tag{3.2}$$

$$\dot{q}_g^* = \frac{\dot{q}_g H^2}{k(T_{max,0}-T_0)} \tag{3.3}$$

$$T^* = \frac{T-T_0}{T_{max,0}-T_0} \tag{3.4}$$

Where, T_0 designates the minimum temperature of the heat sink (Temperature of the Heat Sink Center), and $T_{max,0}$ is the maximum temperature of the 3D IC with plain heat spreader (without high conductivity insert).

The thermal boundary condition for the external surface of the substrate is adiabatic. For the heat sink, four distinctive boundary conditions are considered.

First B. C.: $\quad T_S = 15 \ [°C]$ $\hspace{4cm}$ (3.5)

Second B. C.: $T_S = 10\left(\frac{r}{R}\right) + 15 \ [°C]$ $\hspace{3cm}$ (3.6)

Third B.C.: $\quad q" = h(T_S - T_0) \hspace{1cm} h = 100 \ kW/m^2 \ K$ $\hspace{1cm}$ (3.7)

Fourth B.C.: $\quad q" = h(T_S - T_0) \hspace{1cm} h = 80 \ kW/m^2 \ K$ $\hspace{1.2cm}$ (3.8)

where in the non-dimensional form they can be written as:

First B. C.: $\quad T_S^* = 0$ $\hspace{5cm}$ (3.9)

Second B. C.: $T_S^* = \frac{10r^*}{T_{max,0}-T_0} = \frac{10r^*}{62.7-15} = 0.21r^*$ $\hspace{1.5cm}$ (3.10)

Third B.C.: $\quad T_S^* = T_C^* + \frac{q"}{h(T_{max,0}-T_0)}$

$$= T_C^* + \frac{3437.75 kw/m^2}{100 kw/m^2 k(55.22-15)K} = T_C^* + 0.85 \tag{3.11}$$

Fourth B.C.: $\quad T_S^* = T_C^* + \frac{q"}{h(T_{max,0}-T_0)}$

$$= T_C^* + \frac{3437.75 kw/m^2}{80 kw/m^2 k(63.81-23.59)K} = T_C^* + 1.07 \tag{3.12}$$

Where T_S and T_C are the surface temperature and coolant temperature, respectively, while R is the radius of the heat spreader.

There is natural convection around the 3D IC. The B.C. at the peripherical surface of the IC is stated in the following non-dimensional form:

$$\frac{\partial T_S^*}{\partial n} = -Bi(T_S^* - T_\infty^*) \tag{3.13}$$

where n is the normal unit vector and Bi is the dimensionless Biot number defined as:

$$Bi = \frac{hR}{k} \tag{3.14}$$

and T_∞ is the ambient temperature ($T_\infty = 300K$).

To model the natural convection around the 3D IC, the continuity, Navier-Stokes, and energy equations are solved. These equations are given below in Cartesian coordinates.

$$\frac{\partial u^*}{\partial x^*} + \frac{\partial v^*}{\partial y^*} + \frac{\partial w^*}{\partial z^*} = 0 \tag{3.15}$$

$$Re_H \left(u^* \frac{\partial u^*}{\partial x^*} + v^* \frac{\partial u^*}{\partial y^*} + w^* \frac{\partial u^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial x^*} + \left(\frac{\partial^2 u^*}{\partial x^{*2}} + \frac{\partial^2 u^*}{\partial y^{*2}} + \frac{\partial^2 u^*}{\partial z^{*2}} \right) \tag{3.16}$$

$$Re_H \left(u^* \frac{\partial v^*}{\partial x^*} + v^* \frac{\partial v^*}{\partial y^*} + w^* \frac{\partial v^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial y^*} + \left(\frac{\partial^2 v^*}{\partial x^{*2}} + \frac{\partial^2 v^*}{\partial y^{*2}} + \frac{\partial^2 v^*}{\partial z^{*2}} \right) \tag{3.17}$$

$$Re_H \left(u^* \frac{\partial w^*}{\partial x^*} + v^* \frac{\partial w^*}{\partial y^*} + w^* \frac{\partial w^*}{\partial z^*} \right) = -\frac{\partial p^*}{\partial z^*} + \left(\frac{\partial^2 w^*}{\partial x^{*2}} + \frac{\partial^2 w^*}{\partial y^{*2}} + \frac{\partial^2 w^*}{\partial z^{*2}} \right) \tag{3.18}$$

While the energy conservation equation for the fluid domain is

$$Pe_H \left(u^* \frac{\partial T^*}{\partial x^*} + v^* \frac{\partial T^*}{\partial y^*} + w^* \frac{\partial T^*}{\partial z^*} \right) = \left(\frac{\partial^2 T^*}{\partial x^{*2}} + \frac{\partial^2 T^*}{\partial y^{*2}} + \frac{\partial^2 T^*}{\partial z^{*2}} \right) \tag{3.19}$$

The governing equations are nondimensionalized as follows:

$$u^* = \frac{u}{u_m} \quad v^* = \frac{V}{u_m} \quad w^* = \frac{w}{u_m} \quad p^* = \frac{pH}{\mu_f u_m} \quad Re_H = \frac{\rho_f u_m H}{\mu_f} \quad Pe = \frac{\rho_f C_{p,f} u_m H}{k_f} \tag{3.20}$$

Also, the following dimensionless parameters help us to extend the results of this study to other geometries.

$$r^* = r/R; \ z^* = z/L; \ \phi = \frac{V_{HCI}}{V_{Spreader}}$$ (3.21)

where, r^*, z^*, and ϕ are dimensionless radius, dimensionless height, and volume fraction, respectively. The value of the volume fraction is fixed at 0.2 throughout this study. Maximum dimensionless temperature is

$$T_{max}^* = \frac{T_{max} - T_0}{T_{max,0} - T_0}$$ (3.22)

Where, T_{max} is the maximum temperature of the 3D IC structure with heat spreader having high conductivity inserts. In fact, this dimensionless parameter presents the effectiveness of utilizing Boron Arsenide HCI in cooling the 3D IC. It is notable that T_{max}^* is always less than unity.

3.3.2. Numerical simulation

COMSOL Multiphysics software is used for the numerical simulation of the governing equations. Convergence is achieved when the overall residual for energy equation become less than 10^{-8}.

To check the grid independence, we used two grids with 246,896 and 824,452 cells and compared the minimum and maximum temperatures of the 3D IC for all the boundary conditions. The results are presented in Table 3.2. In this table, ΔT_{min} is equal to the absolute difference between the minimum temperature of the IC predicted by the finer mesh and the minimum temperature computed for the coarser grid in the prior row. A

similar definition can be applied to ΔT_{max} . Based on the data shown in Table 3.2, Grid set

#1 is appropriate and is selected for further simulations.

Table 3.2. Study of the independence of the results from the solution grid

Boundary Conditions	Grid Case No.	Number of cells	T_{min}	T_{max}	ΔT_{min}	ΔT_{max}
First B.C.	1	246896	15.000	55.217	---	---
	2	824452	15.000	55.214	0.000	0.003
Second B.C.	1	246896	15.519	62.649	---	---
	2	824452	15.307	62.649	0.212	0.000
Third B.C.	1	246896	14.996	55.216	---	---
	2	824452	14.998	55.214	0.002	0.002
Fourth B.C.	1	246896	23.590	63.811	---	---
	2	824452	23.592	63.809	0.002	0.002

3.3.3. Validation

To validate the numerical method a cylinder with L/D=0.5 is considered where the top

surface is kept at $T_0 = 15°C$, while the bottom and peripheral surfaces are held at $T_\infty = $

40°C. This analytical solution [40] for this problem given below is considered as a basis

for evaluating the accuracy and validity of the numerical method

$$T(r,z) = T_\infty + 2(T_0 - T_\infty) \sum_{n=1}^{\infty} \left(\frac{\sinh \lambda_n z}{\sinh \lambda_n L} \right) \frac{J_0(\lambda_n r)}{(\lambda_n R)J_1(\lambda_n R)} \qquad (3.23)$$

where λ_n are roots of the equation $J_0(\lambda_n R) = 0$; r is the radial distance measured from the

center, and z is the altitudinal distance measured from the bottom surface.
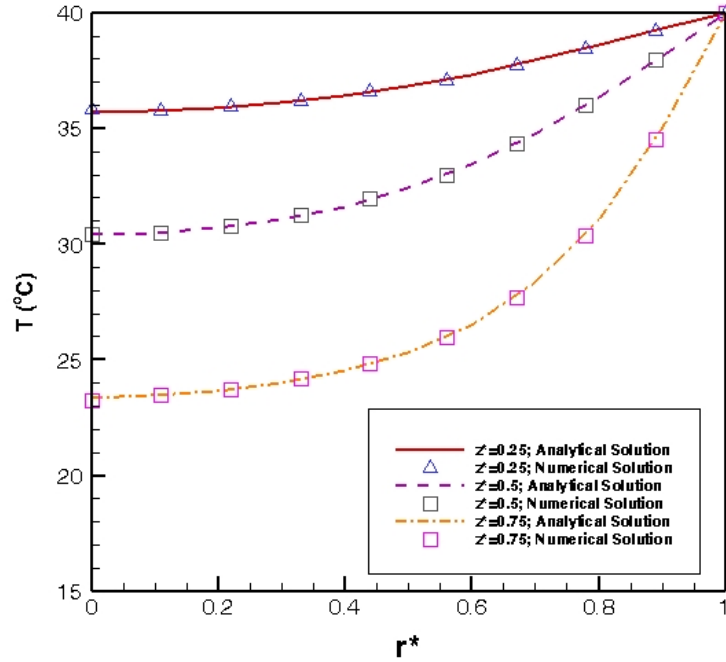
Figure 3.4. Comparison of the numerical temperature predictions with analytical results

Figure 3.4 represents the comparison between the numerical results of the present study and the analytical results from Eq. (3.22) at three dimensionless heights: $z^* = \dfrac{z}{L} = 0.25, 0.5, 0.75$. An excellent agreement is observed.

3.4. Results and discussion

In our research investigation, high conductivity Boron Arsenide are taken as straight blades embedded in the heat spreader of a 3D IC. The blades are configured in three distinctive architectures, namely radial, one level of pairing, and two levels of pairing. First, all of the HCI is distributed among similar blades connecting the center of the heat spreader to its periphery. Keeping the volume fraction fixed at 20%, the number of blades is doubled by halving their thickness. For different cases, the temperature distribution and the maximum

temperature of the 3D IC are obtained. This procedure continues until the change in the maximum temperature of the 3D IC is negligible.

Next, the optimal condition achieved earlier will be used as the basis to find the optimal architecture for the one and two levels of pairing cases. For these cases, the optimal configuration will be determined by varying the number and the thickness of the inner, middle, and outer inserts, independently. It should be noted that all of these parametric studies and optimizations will be carried out for all of the heat sink's imposed boundary conditions.

It is noted that for both the convective heat transfer boundary conditions the coolant temperature is considered as -19.38°C. This is the temperature of the cooling fluid that conveys a constant temperature of 15°C at the heat sink boundary of the plain heat spreader (heat spreader without HCI) when h=100 kW/m^{2}K. In the other words, when there is no HCI in the heat spreader, the convective heat transfer boundary condition of the heat sink with h=100 kW/m^{2}K and coolant temperature -19.38°C is equivalent to the first boundary condition of the heat sink.

3.4.1. Radial inserts

Figure 3.5 illustrates the impact of varying the number of radial inserts embedded in the heat spreader on the dimensionless maximum temperature of a 3D IC for all four heat sink boundary conditions. It should be noted that despite the variation in the number of inserts, the volume fraction of HCI is fixed; that is when the number of the blades is doubled their thickness is halved. As is evident from this figure, for all the boundary conditions when

the number of inserts is increased the maximum temperature of the piece decreases. However, this decline is not remarkable after surpassing 16 inserts. Therefore, using more than 16 radial HCI is not recommended due to more complexity induced in setting up a higher number of HCI blades. This matter is also independent of the heat sink boundary condition. As such, a structure consisting of 16 HCI blades will be used for additional optimization in the upcoming sections.

From Fig. 3.5 it is also seen that the highest effect of incorporating 16 radial HCIs belongs to the constant temperature boundary condition (first boundary condition). To have a better insight on the impact of incorporating HCI on the thermal management of the 3D IC structure the temperature contour for the fourth B.C. at the lowest level which possesses the highest temperature values is illustrated in Fig. 3.6. From this figure, it is clear that the hot spots reside on the edge of the heat spreader because the space between blades is larger at the heat spreader periphery. Therefore, to remove these hot spots, in the next stage we will use one level of pairings for the HCIs in a manner that the outer inserts be located at the current hot spots.
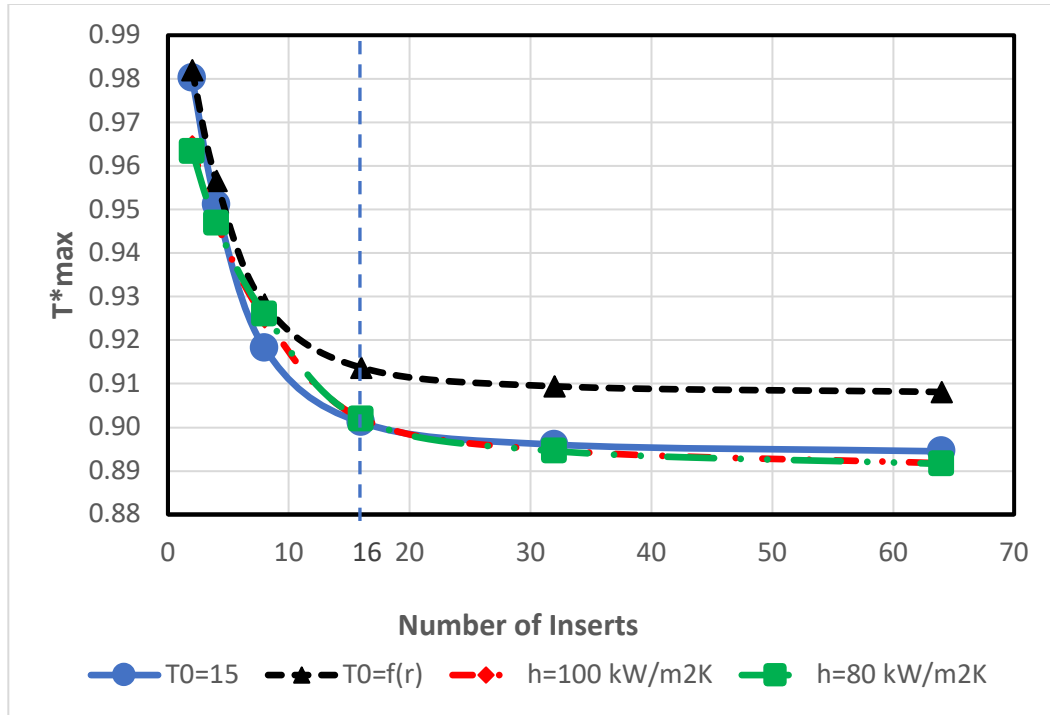
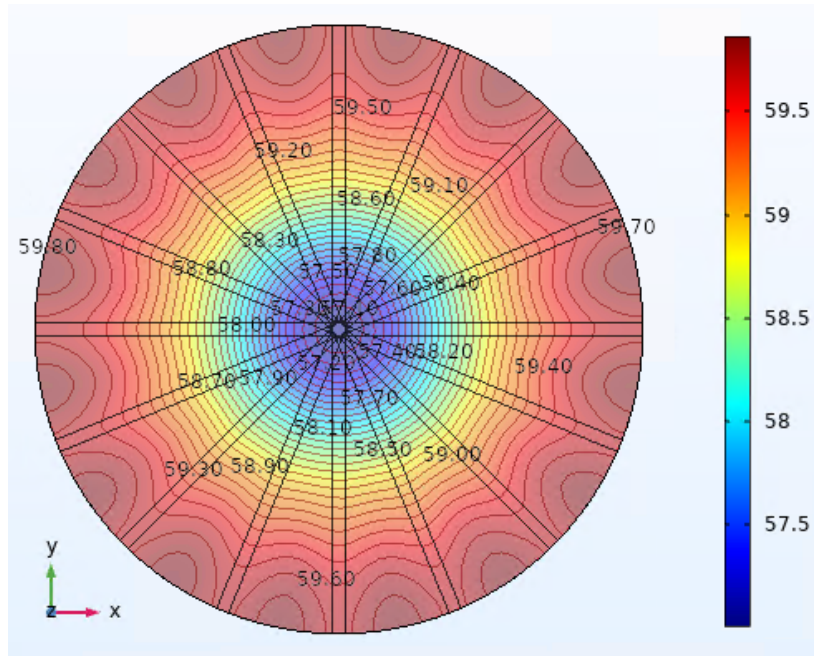Figure 3.5. Variation of T*_{max} with the number of inserts for radial configuration.

Figure 3.6. The contour of temperature at the lowest level of 3D IC for radial configuration with 16 blades for fourth B.C.

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3.4.2 One level of pairing

The effect of the length of the inner and outer inserts on the heat spreader with one level of the pairing of HCI is shown in Fig. 3.7. In this figure $r_1^* = r_1/R$, where r_1 is the length of the inner insert and R is the radius of the heat spreader. This figure is plotted for a similar number of inner and outer inserts ($N_1 = 16, N_2 = 16$). It is seen that for all the B.Cs, there are optimum values for the length of inner and outer inserts. It should be noted that the optimal value for all boundary conditions occurs at $r_1^* = 0.94$. However, as expected, the dimensionless maximum temperature values at the optimum location are contingent on the boundary condition.
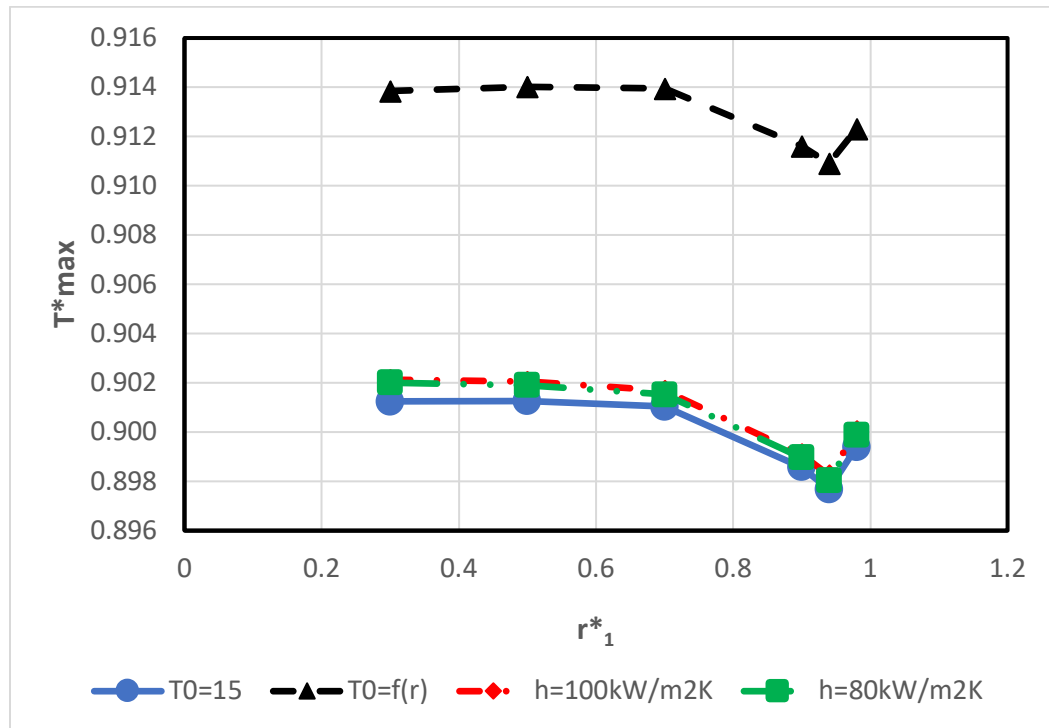

Figure 3.7. Variation of T*max with the dimentionless length of inner inserts for one level of pairing configurations with $N_1=16$, $N_2=16$

Figs. 3.8a, 3.8b and 3.8c demonstarte the justification for the existence of the optimum values for the length of the inner and outer inserts, for $r_1^* = 0.90, 0.94$, and 0.98, respectively. These figures contain the temperature contour at the hottest level of the 3D IC for the fourth B.C.. From figure 3.8a, it is observed that the hot spots reside at the edge of the heat spreader between the outer HCI blades. As can be see the effect of the inner HCIs on the hot spot location is not remarkable. Upon further examination of Fig. 3.8b it can be seen that by extending the inner inserts more towards the periphery, the hot spots are relocated towards the outer short inserts. Due to an increase in the length of inner inserts, the contribution of these inserts in transferring heat is increased while on the other hand, the length of the outer inserts is decreased which mitigates the role of these inserts in dissipating the heat. This figure displays the optimum case. That is by increasing the length of inner inserts and reducing the length of outer inserts this phenomenon will be boosted as seen in Fig. 3.8c. Accordingly as can be seen, the maximum temperature has been increased compared to Fig. 3.8b while the locations of the hot spots are not changed. As we have seen the hot spots are located at the edge of the heat spreader and usually between the outer inserts. Thus, one way to suppress the hot spots is distributing more HCI blades in the outer region. The variations of the dimensionless maximum temperature of 3D IC for $N_1 = 16$ and $N_2 = 3$ for different heat sink B.Cs are shown in Fig. 3.9. It is evident from this figure that when the number of outer blades is doubled (their thickness is halved) the trend of variations of T_{max}^* with r_1^* will be different. That is the variation is strictly monotonical. This behavior is also valid for all other heat sink B.C.s considered in this work.
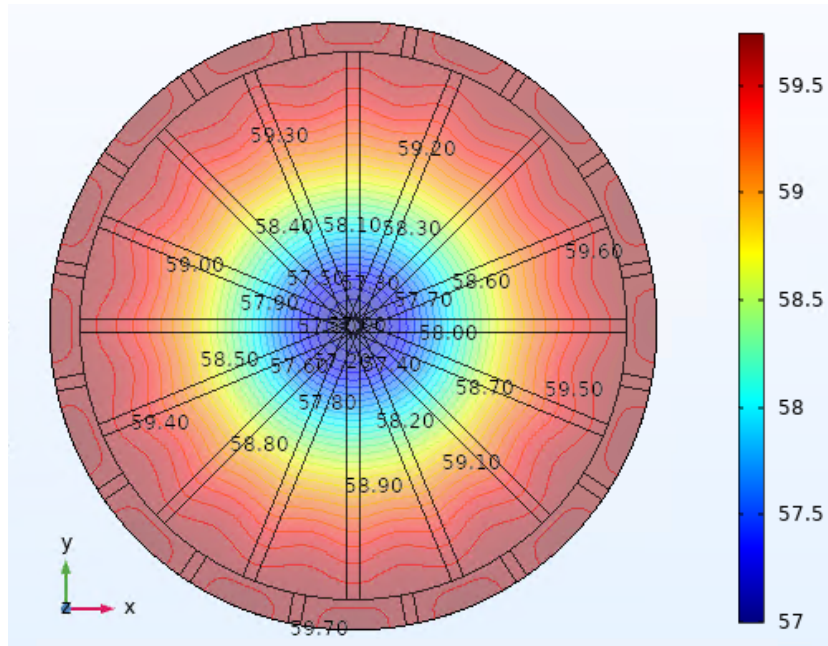
(a)
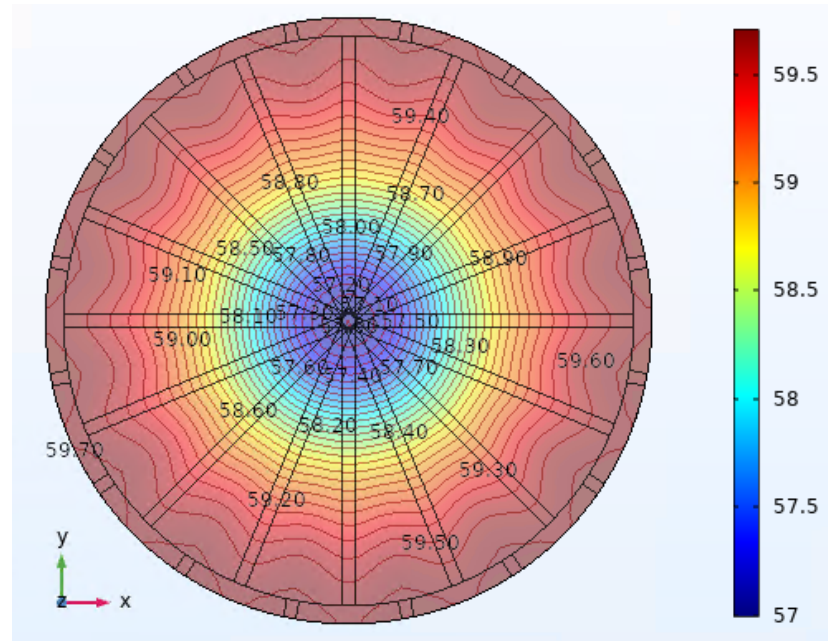
(b)
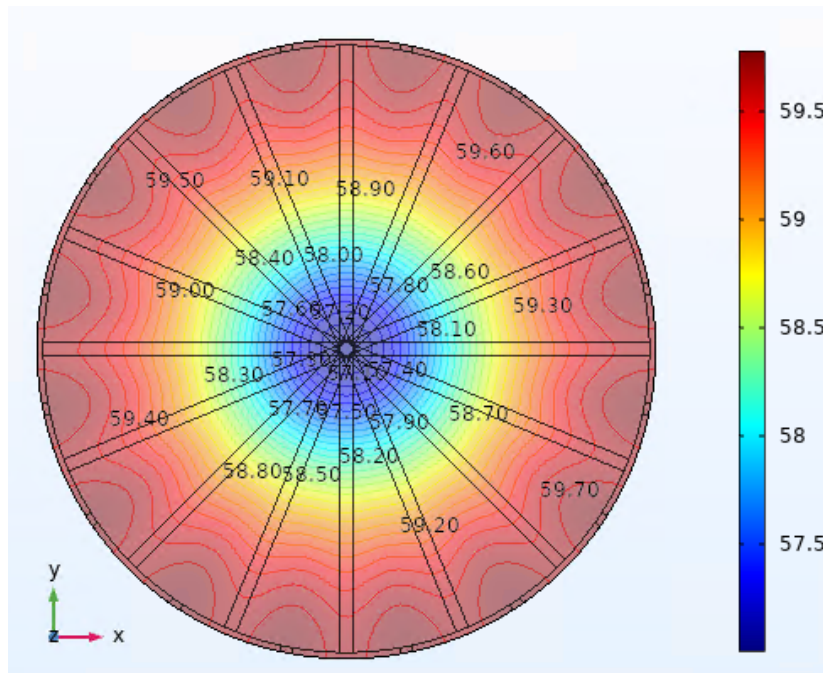
(c)

Figure 3.8. The contour of temperature at the lowest level of 3D IC for one level of pairing configuration with $N_1 = 16$, $N_2 = 16$ for fourth B.C. at a) $r*_1 = 0.90$, b) at $r*_1 = 0.94$, and c) at $r*_1 = 0.98$

To explain this behavior, the temperature contours at the lowest level of the 3D IC (corresponding to the fourth B.C.) for $r_1^* = 0.70$, and 0.98 are represented in Figs. 3.10a and 3.10b, respectively. From Fig.3.10a it is seen that for $r_1^* = 0.70$ the hot spots reside between consecutive outer blades. However, by increasing the length of internal inserts for $r_1^* = 0.98$, the impact of internal inserts dominates the effect of outer short inserts, 3.10b. This leads to eliminating the hot spots located on the trajectory of the internal inserts; while the hot spots resided between the adjacent pair of blades are worsen due to the reduction in their lengths.
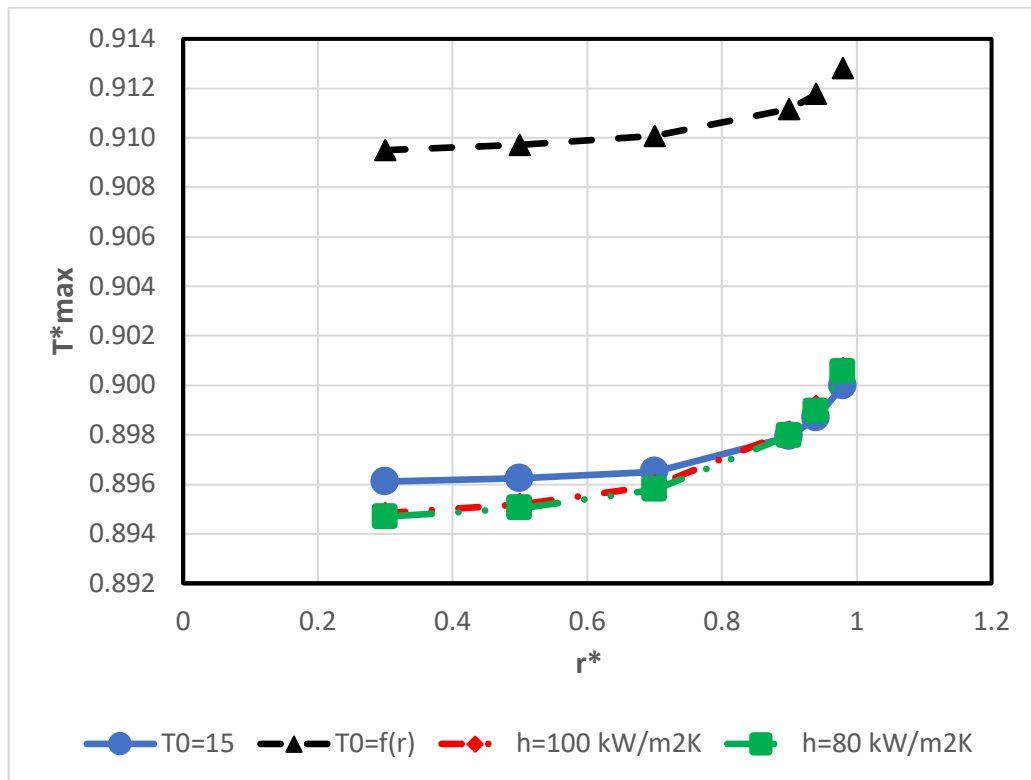

Figure 3.9. Variation of T^*_{max} with the dimentionless length of inner inserts for one level of pairing configurations with $N_1=16$, $N_2=32$
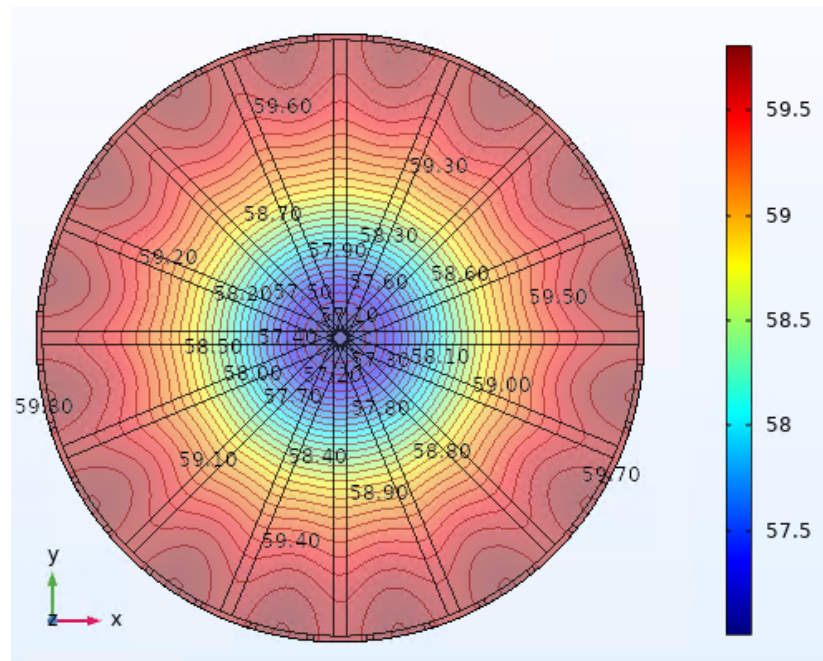
3.4.3. Two levels of pairing

To arrive at more optimum conditions, another level of pairing is considered for the HCI configurations shown in Fig. 3.3. This adds two more degrees of freedom, i.e., the number and the length of the second level inserts to the optimization procedure. Throughout this section the length of internal and middle inserts are assumed to be equal, while the length of the outer insert can be changed independently.

Figure 3.11 presents the effect of the length of various inserts of a heat spreader with two levels of pairing on the maximum dimensionless temperature of a 3D IC. In this figure $r_2^* = r_2/R$, where r_2 is the length of the inner and middle inserts (the radial location of the middle insert tips) and R is the radius of the heat spreader. In this figure, the number of inner, middle, and outer inserts are equal $N_1 = N_2 = N_3 = 16$. From this figure it can be seen that there are optimum values for the HCI inserts lengths at which the maximum temperature of the 3D IC is minimized. It is interesting to note that this optimum location $(r_2^* = 0.94)$ is independent of heat sink boundary condition. It should also be noted that the dimentionless maximum temperatures corresponding to B.C's 1, 3, and 4 are close to each other and exactly coincide at the optimal condition; while the values corresponding to B.C. 2 are totally different. Moreover, it is observed that although the temperature distribution of a 3D IC is strictly dependent on the convective heat transfer coefficient at heat sink, the dimentionless maximum temperature is not sensitive to that factor.
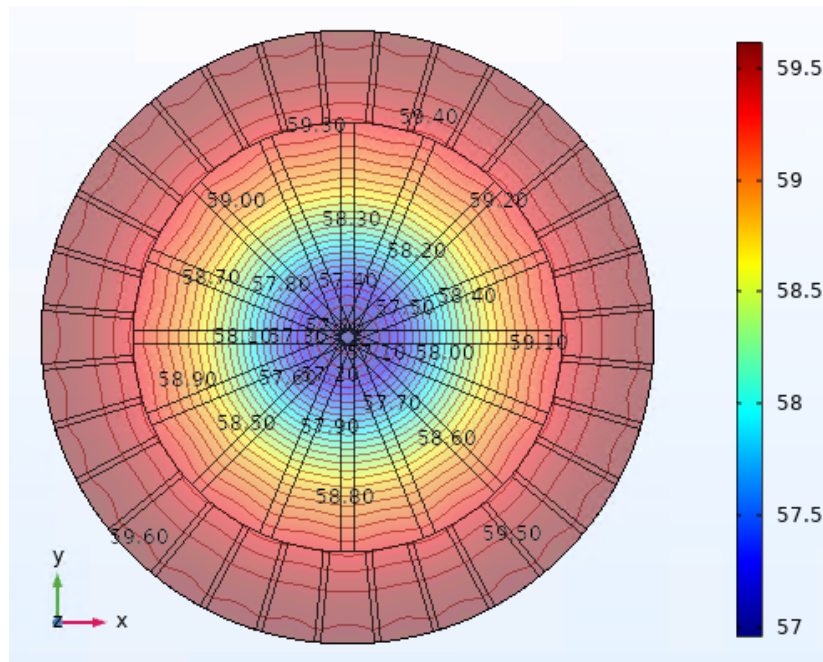
(a)

(b)

Figure 3.10. The contour of temperature at the lowest level of 3D IC for one level of pairing configuration with $N_1 = 16$, $N_2 = 32$ for fourth B.C. at a) $r*_1 = 0.70$, b) $r*_1 = 0.98$

Figure 3.11. Variation of T^*_{max} with r^*_2 for two levels of pairing configurations with $N_1=16$, $N_2=16$, and $N_3=16$

As the hot spots occur at the edge of the heat spreader, the inner inserts do not affect the optimal configuration. That is, the length of the outer inserts defines the optimal points. Therefore, the justification for the existance of the optimal values of different blades is simillar to that of one level of pairing case (Fig. 3.8). To have a better insight, Figs. 3.12a-c (corresponding to Fig. 3.8a-c for one level of pairing) are provided.
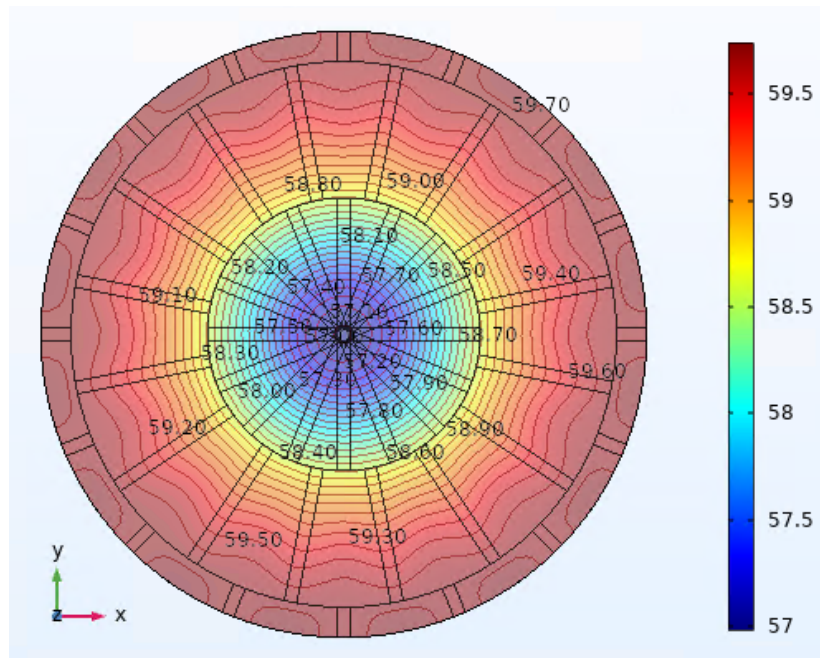
(a)
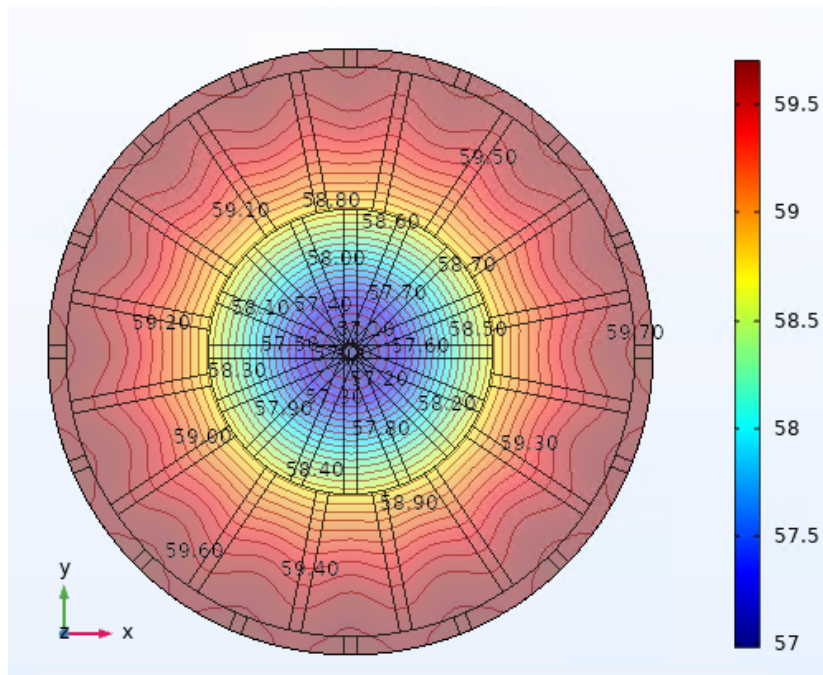
(b)

(c)

Figure 3.12. The contour of temperature at the lowest level of 3D IC for two levels of pairing configurations with $N_1 = 16$, $N_2 = 16$, and $N_3 = 16$ for fourth B.C. at a) $r^*_2 = 0.90$, b) at $r^*_2 = 0.94$, and c) at $r^*_2 = 0.98$
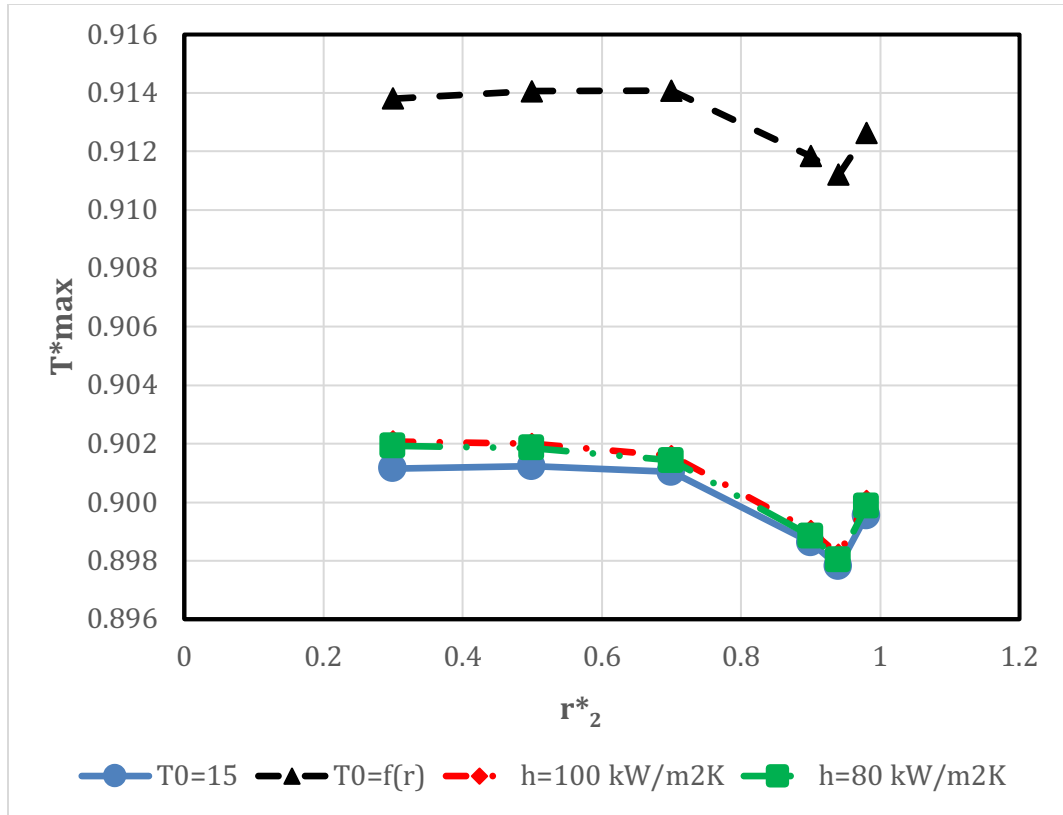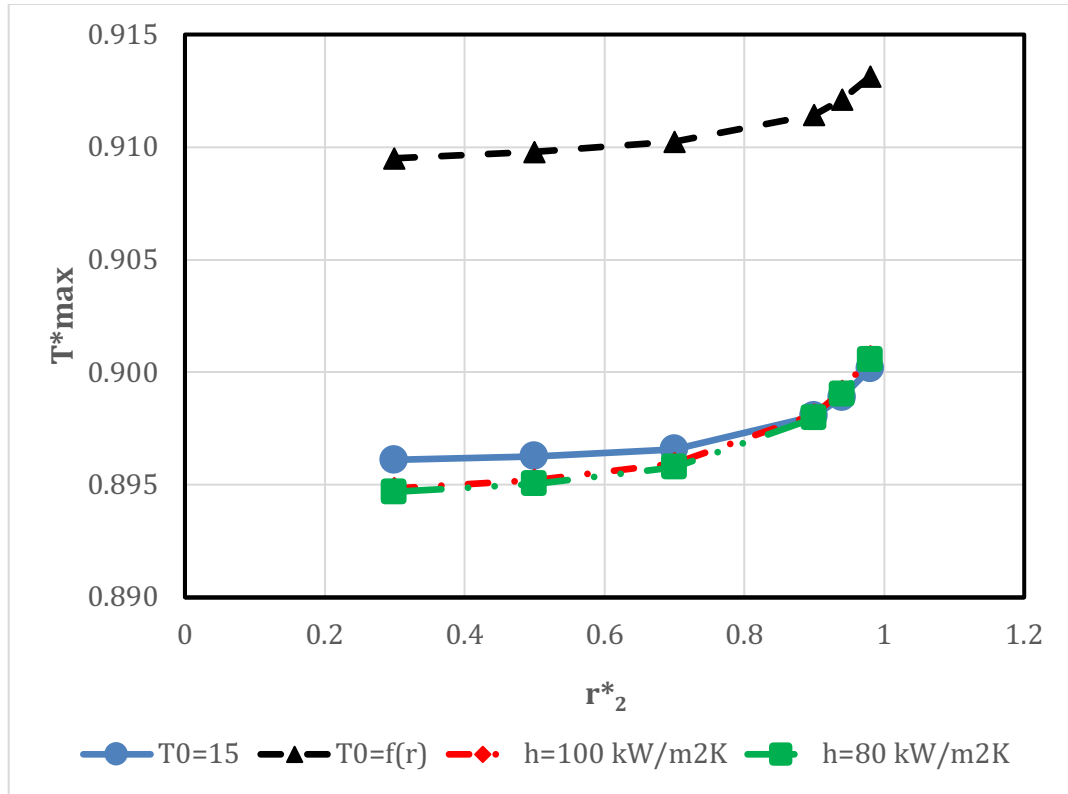
Figure 3.13. Variation of T*max with r*2 for two levels of pairing configurations with
N_1=16, N_2=16, and N_3=32

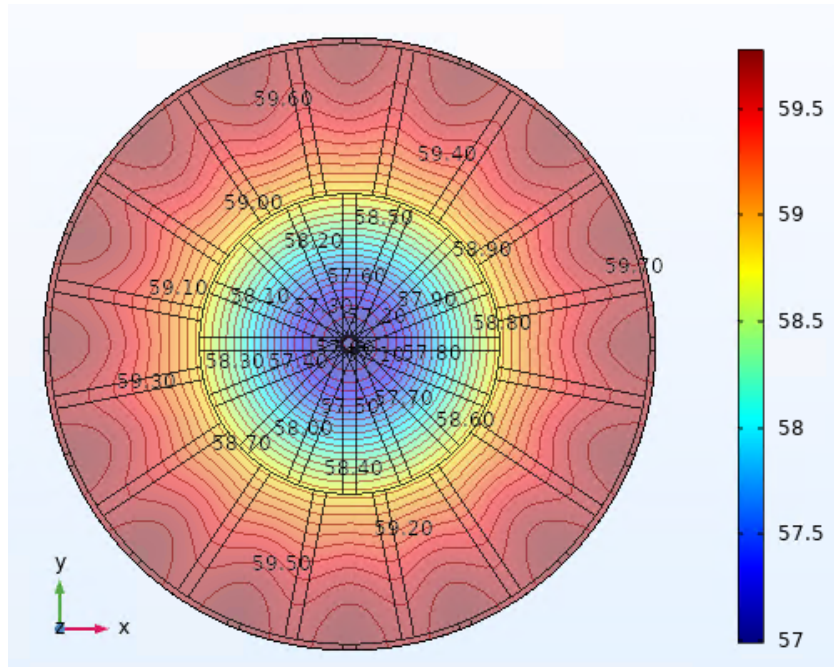Figure 3.13 shows how the maximum temperature of the 3D IC varies with the length of HCI inserts for $N_1 = N_2 = 16$, and $N_3 = 32$. Here again the dimentionless maximum temperature for B.Cs, 1,3, and 4 are so close to each other ;while for the second boundary condition it is remarkably higher. The reason is that the hotspot occures at the edge of the heat spreader where the temperature of the heat sink for the second B.C. (25°C) is much higher than the other boundary condition cases. From this figure, it is evident that when the length of the outer inserts is reduced (r_2^* increases) the maximum temperature rises for all the B.Cs monotonically. The reasoning is simillar to what was discussed in Fig. 3.9. Because the internal HCI blades do not affect the temperarue distribution near the periphery

of the heat spreader; that is the hot spot location and thus the optimal configuration is not contingent on the architecture of the internal blades. Similar to Fig. 3.9 when there are 32 outer inserts, reducing the length of those inserts, reduces the number of hotspots by half and hence their temperature will rise.

Simillar behavior is observed in Fig. 3.14 which has been plotted to show the effect of the length of different blades on the maximum temperature of 3D IC when the number of outer blades is increased to 48 (the number of inner and middle inserts is fixed at 16). Comparing this figure to Fig. 3.13 it is seen that the asending trend of the curves is intensified. It should be noted that using higher number of outer inserts makes the temperarute distribution at that part more uniform. However, by increasing r_2^* the length of outer insert is reduced leading to diminishing its effect on the heat dissipation and pronuncing the role of the middle inserts in heat conduction. Thus, the hot spots will be concentrated at the edge of the heat spreader between the middle inserts. In this case the number of hot spot location is reduced to 1/3, hence the temperarure of the hot spot is increased.

Next, the number of both middle and outer insert is increased to 32; while the number of inner inserts is kept fixed at 16. The variation of the maximum temperature for different B.C's for this case is illustrated in Fig. 3.15. For this configuration, the temperature distribution at the horizontal plane is so uniform that by changing the length of different inserts its uniformity is not affected considerably, as seen in Fig. 3.16, which also shows that the highest temperature occurs around the periphery of the heat spreader. Therefore, no discernable change is obserevd in Fig. 3.15. Next, we doubled the number of outer inserts $N_1 = 16, N_2 = 32$, and $N_3 = 64$. The results are shown in Fig. 3.17. For this

situation the temperature distribution will be more uniform at the outer ring where the highest temperatures occur. According to Fig. 3.17, increasing r_2^* , slightly increases the maximum temperature. Because the hot spots reside at the edge of the heat spreader. Increasing r_2^* leads to a reduction in the length of the outer blades which in turn, raises the hot spot temperature. However, due to the high number of outer inserts, the growth in the hot spot temperature is not sharp.
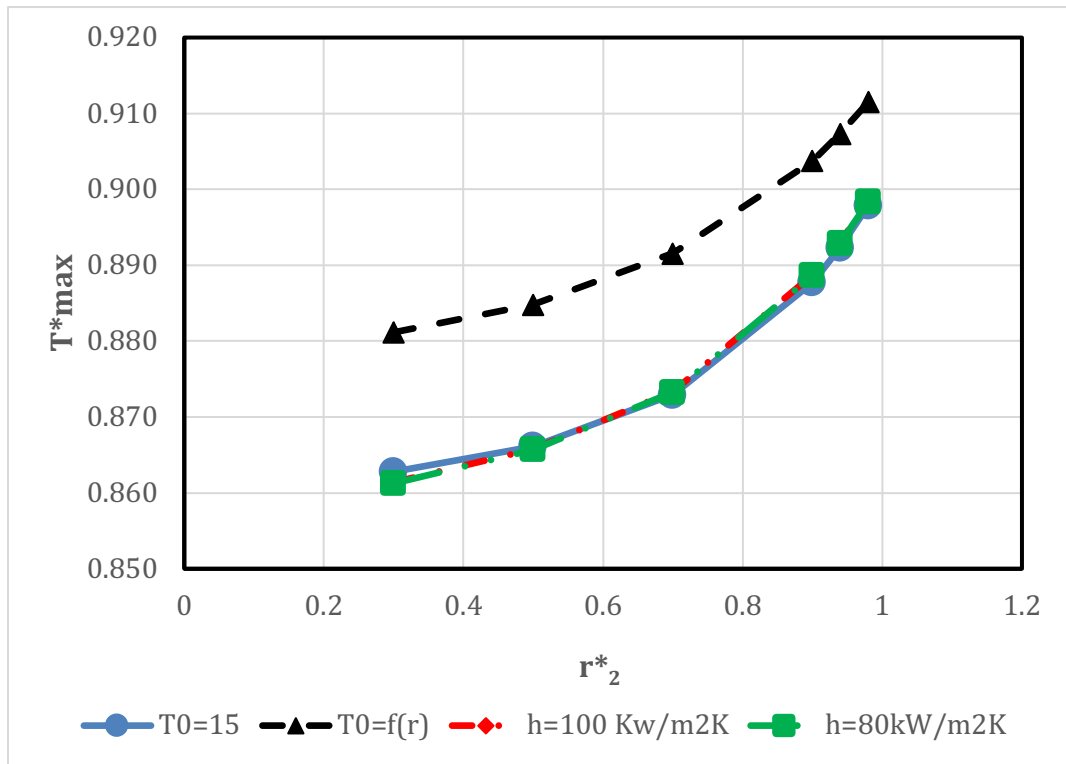
Figure 3.14. Variation of T^*_{max} with r^*_2 for two levels of pairing configurations with $N_1=16$, $N_2=16$, and $N_3=48$
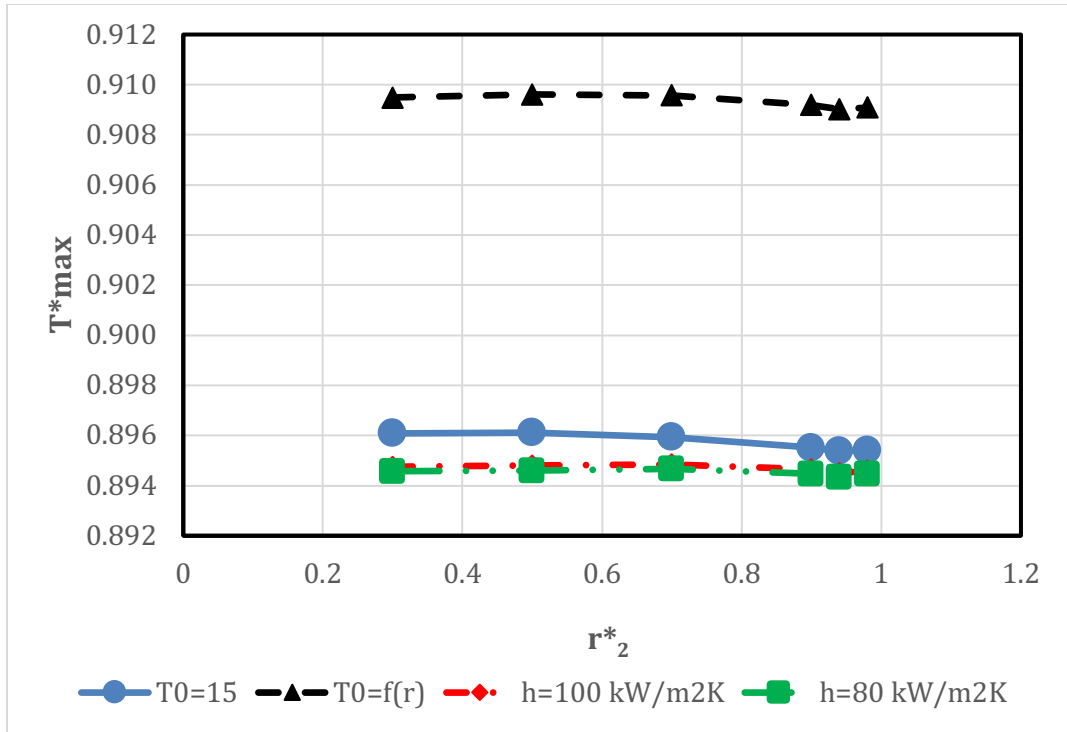
Figure 3.15. Variation of T^*_{max} with r^*_2 for two levels of pairing configurations with $N_1=16$, $N_2=32$, and $N_3=32$
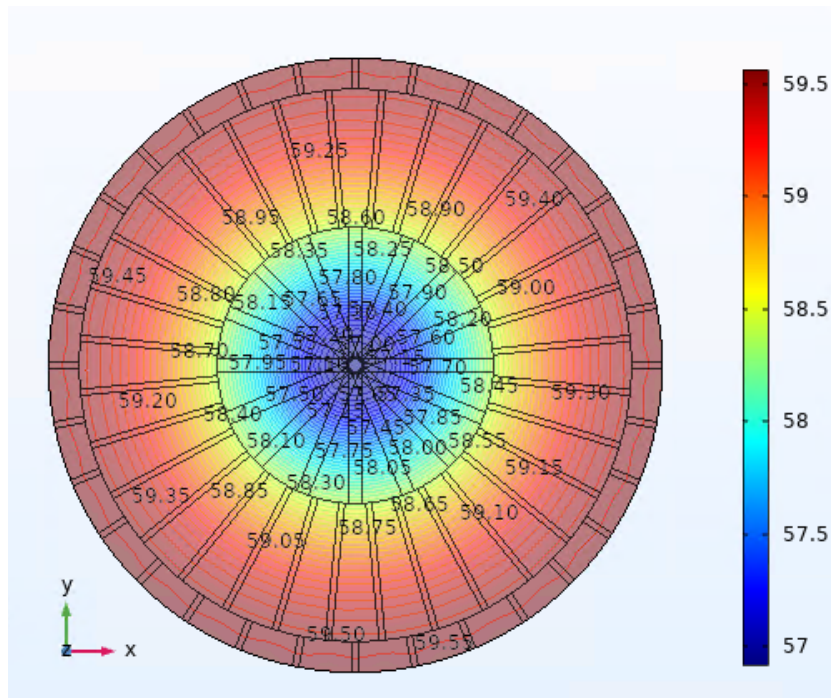
Figure 3.16. The contour of temperature at the lowest level of 3D IC for two levels of pairing configurations with $N_1 =16$, $N_2 =32$, and $N_3 =32$ for fourth B.C. at $r^*_1 =0.90$
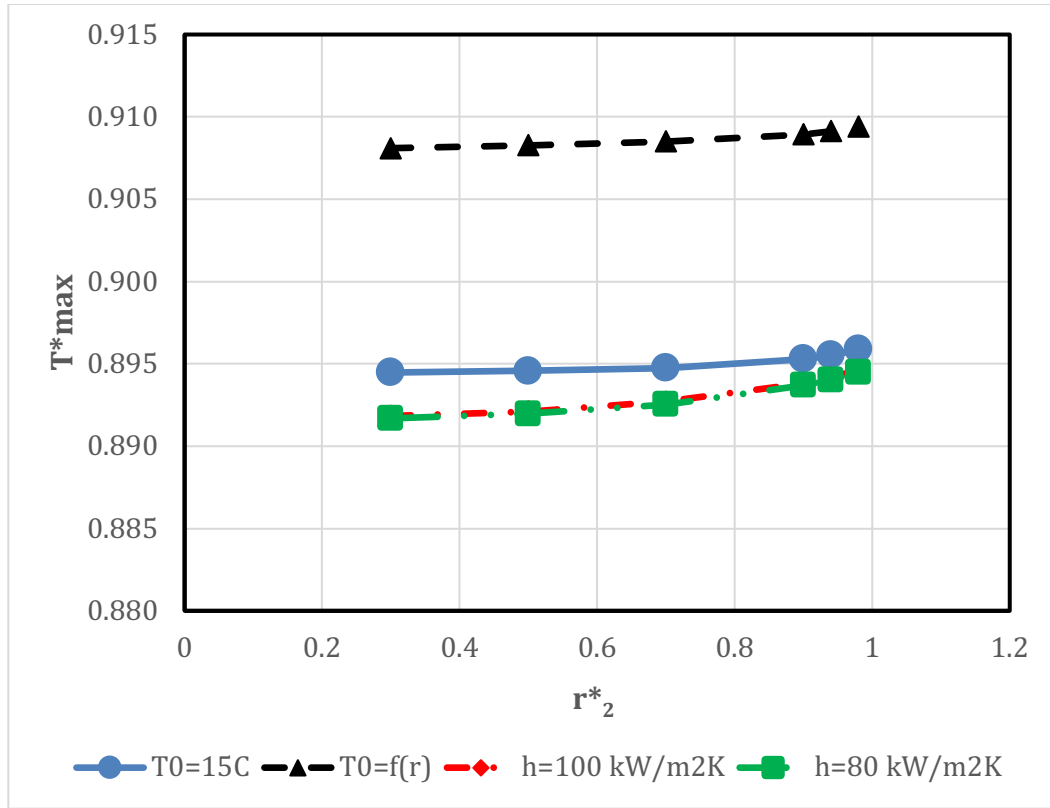
Figure 3.17. Variation of T*$_{max}$ with r*$_2$ for two levels of pairing configurations with
N$_1$=16, N$_2$=32, and N$_3$=64

3.4.4. Comparision of various configurations

Comparing various radial, one level of pairing and two levels of pairing configurations, it is observed that the case for two levels of pairing with $N_1 = 16$, $N_2 = 16$, and $N_3 = 48$ yeilds the optimal condition. This optimal is independent of the heat sink boundary condition. For the optimal condition, the dimensionless maximum temperature of 3D IC for the first to the fourth B.C's are 0.863, 0.881, 0.861, and 0.861, respectively, which are corresponding to 5.52, 5.66, 5.58, and 5.58°C reduction in the maximum temperature of the 3D IC structure compared to the same case without incorporating the HCI.

Chapter 4

Summery and Conclusions

A computational investigation is performed to find the optimal configurations for distribution of a finite amount of Boron Arsenide throughout the heat spreader of the 3D IC structure to substantially reduce the magnitude of the hot spot temperatures. The architecture under consideration includes the ring-shape and straight-blade configurations. The ring-shape architecture includes single-layer and double-layer patterns while the straight-blade one is composed of radial, one-level of pairing and two-level of pairing layouts.

For the ring-shape configuration, an optimization procedure is followed for finding the proper locations for the rings as well as achieving the best distribution for the high conductivity material between the rings. For this part, the following results are achieved.

- The results show that there exist optimum locations for placing the HCI rings.

- For the single ring configuration, the dimensionless maximum temperatures at optimized conditions are 0.94 and 0.91, for first and second B.Cs., respectively.

- For two-ring configuration, it is seen that the farther away the rings are, the better cooling performance is achieved.

- For both B.Cs, when the inner ring is pinpointed at the center of heat spreader, the optimal structure is achieved when the second ring is located at $r_2^* = 0.774$.

- When $r_1 = 0.25r_2$, it is concluded that the best location for the outer ring is the same ($r_2^* = 0.774$) for both boundary conditions.

- For $r_1 = 0.50r_2$, it is notable that both boundary conditions have optima in a range of ring radii rather than a single specified radius.

- When $r_1 = 0.75r_2$, for the first B.C., an ascending trend is observed when r_1 and r_2 are increased. On the contrary, for the second boundary condition, a minimal value for T^*_{max} is obtained concerning r_1 (or r_2).

- There is an optimal value (P=0.75) for the allocation of the HCI material to the rings.

- The final optimal results are: $r_1^* = 0.194$, and 0.580, for the first and second B.C.s, respectively; $r_2^* = 0.774$, and $P = 0.75$.

- It is found that for the final optimal condition, the dimensionless maximum temperature of the 3D IC could be lowered by more than 10%.

For the straight-blade configuration, all the simulations are carried out subjected to four different boundary conditions. For this section, the following results are obtained.

- For these cases, the optimal configuration will be determined by varying the number and the thickness of the inner, middle, and outer inserts, independently.

- For radial configuration, for all the boundary conditions when the number of inserts is increased the maximum temperature of the piece decreases. However, this decline is not remarkable after surpassing 16 inserts.

- Therefore, using more than 16 radial HCI is not recommended due to more complexity induced in setting up a higher number of HCI blades.

- For one-level-of-pairing layout, for all the B.Cs, there are optimum values for the length of inner and outer inserts.

- The optimal value for all boundary conditions occurs at $r_1^* = 0.94$.

- For two-level-of-pairing, there are optimum values for the HCI inserts lengths at which the maximum temperature of the 3D IC is minimized.

- The optimum location occurs at $r_2^* = 0.94$ which is independent of heat sink boundary condition.

- It is found that the best results are achieved when the high conductivity material are distributed in two levels of pairing configuration with $N_1 = 16$, $N_2 = 16$, and $N_3 = 48$.

- The results show that when operating at the optimal condition, incorporating BAs inserts can reduce the dimensionless maximun tempereture of 3D IC structure as much as about 14%.

- The performance of the optimal blade-type insert case (14% reduction in maximum temperature) is superior comparing to the performance of the optimal ring-type insert case (10% reduction in maximum temperature).

- It should be mentioned that the achieved results are dimensionless; therefore, they can be scaled up or down to meet the practical limitations.

Nomenclature

c_p specific heat at constant pressure $[\text{J}\,(\text{kg}\cdot\text{K})^{-1}]$

h   convective heat transfer coefficient $[\text{W}\,(\text{m}^2\cdot\text{K})^{-1}]$

H   Heat spreader height [m]

k   thermal conductivity $[\text{W}\,(\text{m}\cdot\text{K})^{-1}]$

L   length [m]

n   normal coordinate

Nu   Nusselt number $[\,\text{h}\cdot\text{H}\,/\,\text{k}_f\,]$

p   pressure [Pa]

P   volume ratio

$\dot{q}_g$ volumetric heat generation rate $[\text{W}\ \text{m}^{-3}]$

r   Radial distance [m]

r_1 Inner radius of internal ring [m]

r_2 Inner radius of external ring[m]

R   Radius of the heat spreader

Re_H Reynolds number $[\,\rho_f \text{u}_m \text{H}/\mu_f\,]$

T   temperature [K]

T^* Dimensionless temperature, $[T^* = \frac{T-T_0}{T_{max,0}-T_0}]$

u   x-component of velocity $[\text{m}\ \text{s}^{-1}]$

v   y-component of velocity $[\text{m}\ \text{s}^{-1}]$

w   z-component of velocity $[\text{m}\ \text{s}^{-1}]$

x, y, z   Cartesian coordinates

Subscripts

f   Fluid

e   entrance

m   mean

max   maximum

o   outlet

s   solid

H   Characteristic Length

∞   Ambient Condition

Superscripts

*   dimensionless

Greek Symbols

μ dynamic viscosity $[\,(\text{N}\cdot\text{s})\ \text{m}^{-2}]$

ρ density $[\text{kg}\ \text{m}^{-3}]$

$\varnothing$ volume fraction

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