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***Abstract*—As a result of their soft-charging and soft-switching capabilities, resonant switched-capacitor (ReSC) converters can achieve higher efficiencies and power densities than pure switched-capacitor (SC) converters. However, the terminal capacitors (i.e, the input and output capacitors) still consume a large volume in ReSC converters and represent the new bottleneck for converter miniaturization. Theoretically, when the terminal capacitances are reduced, an optimum clocking scheme that preserves multi-resonant operation can be calculated. In practice, this optimal operating point may not be precisely obtained due to circuit parasitics, passive component tolerance and derating. This paper demonstrates a closed-loop hysteretic control method that can dynamically track the zero current switching (ZCS) operating point and allow for a reduction in terminal filtering capacitors via multi-resonant operation. A 48-to-24-V ReSC converter prototype is designed and constructed to verify the effectiveness of the proposed control method. The controller is demonstrated to successfully track the ZCS operating point, enabling over 70% reduction in terminal capacitor volume. In the case of reduced terminal capacitances, the controller achieves up to 44% reduction in power loss compared with the conventional open-loop control without ZCS autotuning.**

I. Introduction

By adding a small resonant inductor to pure switched-capacitor (SC) converters, the primary passive component volume (i.e., the total volume of the flying capacitors and the inductor) of a resonant switched-capacitor (ReSC) converter can be significantly reduced while preserving efficiency [1]. In fact, due to the soft-charging of flying capacitors [2], [3], resonant switched-capacitor (ReSC) converters can achieve minimal conduction losses at relatively low switching frequencies compared with pure switched-capacitor (SC) converters [4]–[6]. Furthermore, by using a zero current switching (ZCS) scheme, most of the voltage-current overlap loss during switching transitions can be eliminated.

As illustrated in Fig. 1, practical implementations of ReSC converters require large input and output capacitors ($C_{\rm in}$ and $C_{\rm out}$) to stabilize the terminal voltages. Given that these terminal capacitors need to be much larger than the flying capacitor $C_{\rm fly}$, they typically consume a large volume and have become a new bottleneck for converter miniaturization. Although it is desirable to reduce the size of terminal capacitors, when the terminal capacitance is reduced to the same order of magnitude as the flying capacitance in a 2-to-1 ReSC converter, the switching frequency of the converter diverges from $\frac{1}{2\pi\sqrt{LC_{\rm fly}}}$ and the inductor current waveform during both

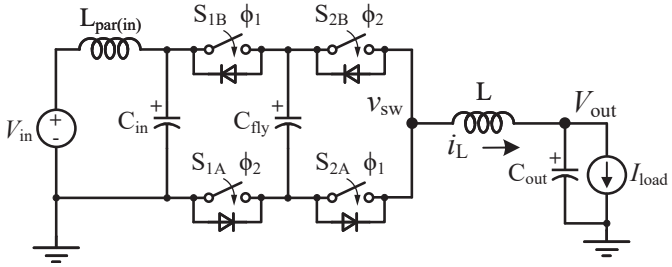


Fig. 1: Schematic of the 2-to-1 ReSC converter used in this work. Parasitic input inductance $L_{\rm par(in)}$ is modeled to allow a finite input capacitance to be assessed.

phases is no longer symmetric. As a result, the conduction loss can only be minimized when the switching frequency is very high (incurring significant switching losses) or when the converter is operating precisely at multi-resonance with dissimilar phase durations [7], [8]. Theoretically, when the input or output capacitance is not sufficiently large, the multi-resonant compensation control (MRCC) proposed in [8] can be used to determine the optimum operating point. However, in practice, it is challenging to achieve and maintain such precise ZCS tuning using solely phase duration estimates: parasitics, inductor dc bias, and passive component tolerance all serve to affect the converter's resonant behavior. Moreover, commonly used high density Class II multilayer ceramic capacitors (MLCCs) deviate significantly in value with voltage bias, age and temperature [9].

Despite these challenges, demonstrations of closed-loop control and accurate sensing that accounts for component mismatch and variation have been lacking. Recently, [10] demonstrated an active digital ZCS controller applied to the switched tank converter (STC) [11]. In this paper, a closed-loop digital control method that can dynamically achieve zero current switching (ZCS) is studied and tested on a 48-to-24-V ReSC converter. When cascaded, this topology has demonstrated excellent performance for 48-to-12-V power conversion in data centers [12], [13].

Using feedback from the voltage deviation observed on the internal switch node ($v_{\rm sw}$ as shown in Fig. 1) during the deadtime interval, the state of the turn off current (above or below 0 A) at the end of each phase can be assessed. The duration of each phase is then gradually adjusted by

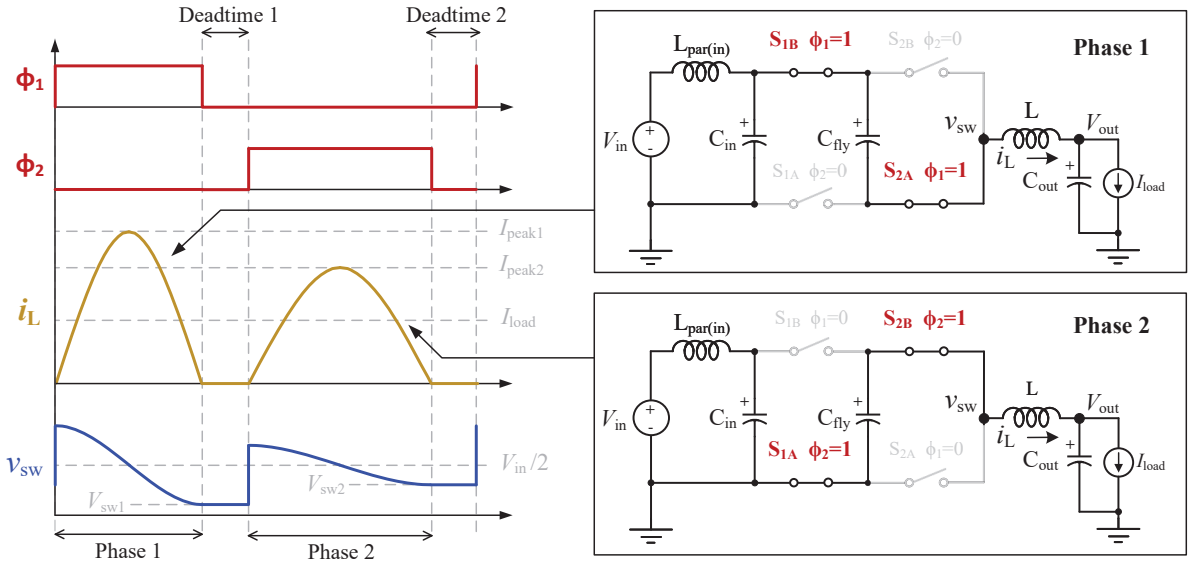


Fig. 2: Key waveforms of ideal ZCS operation. The duration of phase 1 is equal to T_1 and the duration of phase 2 is equal to T_2.

the controller until the voltage deviation of $v_{\rm sw}$ during the deadtime is minimal, indicating that the turn off current is close to 0 A. Each phase is adjusted independently, allowing the proposed control method to achieve ZCS tuning in multi-resonant operation, thereby enabling terminal capacitances to be reduced without compromising the soft-switching operation of the converter.

The remainder of this paper is organized as follows. Section II describes ZCS operation in the presence of finite terminal capacitance. Section III outlines the proposed hysteretic control scheme using a single voltage comparator. Section IV details a hardware prototype exemplifying intended operation, and Section V concludes this work.

II. Theory of ZCS Operation

A. Switching Sequence and Multi-Resonance

Figure 2 shows the switching scheme, output inductor current waveform $i_{\rm L}$, and switch node voltage $v_{\rm sw}$ in the case of ideal ZCS operation. There are two main phases separated by deadtimes. $\rm S_{1B}$ and $\rm S_{2A}$ are conducting during phase 1, while $\rm S_{1A}$ and $\rm S_{2B}$ conduct in phase 2. The duration of the deadtime, typically between 10-100 ns, is negligible compared with the main phase durations and scaled up in Fig. 2 for better visibility. Here, the parasitic input inductance $L_{\rm par(in)}$ is assumed to be large—carrying a constant current $I_{\rm in}$—with minimal impact on circuit dynamics.

As discussed in [7], the effective capacitance observed by the output inductor L during phase 1 is

$$C_{\rm eff1} = \frac{1}{\frac{1}{C_{\rm in}} + \frac{1}{C_{\rm fly}} + \frac{1}{C_{\rm out}}}, \tag{1}$$

and the effective capacitance during phase 2 is

$$C_{\rm eff2} = \frac{1}{\frac{1}{C_{\rm fly}} + \frac{1}{C_{\rm out}}}. \tag{2}$$

For most converters, $C_{\rm in}$ and $C_{\rm out}$ are chosen to be much larger than $C_{\rm fly}$, resulting in $C_{\rm eff1} \approx C_{\rm eff2} \approx C_{\rm fly}$. However, when $C_{\rm in}$ and $C_{\rm out}$ are reduced to a value of the same magnitude as $C_{\rm fly}$, the mismatch between $C_{\rm eff1}$ and $C_{\rm eff2}$ will induce noticeable multi-resonant operation as seen in Fig. 2. Due to the steady-state charge balance constraint on $C_{\rm fly}$, in addition to $C_{\rm eff1}$ being smaller than $C_{\rm eff2}$, the peak inductor current during phase 1 will be larger than that observed during phase 2 as per the following equations:

$$T_1 I_{\rm peak1} = T_2 I_{\rm peak2} \tag{3}$$

yielding

$$I_{\rm peak1} = I_{\rm load}\frac{\pi(T_1+T_2)}{4T_1} \tag{4}$$

$$I_{\rm peak2} = I_{\rm load}\frac{\pi(T_1+T_2)}{4T_2} \tag{5}$$

where T_1 and T_2 are the respective durations of phase 1 and phase 2 in ideal ZCS operation, and $I_{\rm peak1}$ and $I_{\rm peak2}$ are the corresponding peak inductor currents.

B. Switch Node Voltage

With ideal ZCS, the switches will be turned off precisely at 0 A. There is no energy stored in the output inductor at the beginning of the deadtime; there will be negligible current flow in the circuit and energy exchange between components. As a result, from the beginning to the end of the deadtime, the switch node voltage will remain constant as shown in Fig. 2.

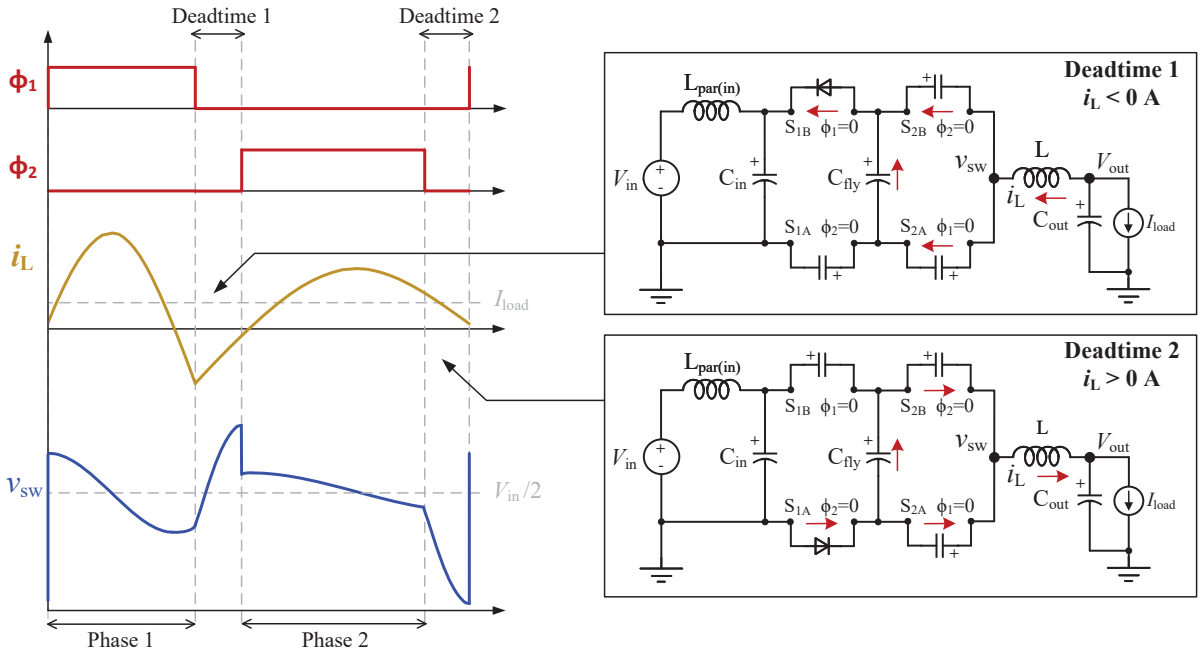


Fig. 3: Key waveforms of partial ZCS operation when i_{L} is negative during deadtime 1 and positive during deadtime 2.

During deadtime 1:

$$v_{\mathrm{sw}}(t) = V_{\mathrm{sw1}} = V_{\mathrm{C_{in-end1}}} - V_{\mathrm{C_{fly-end1}}} \tag{6}$$

and during deadtime 2:

$$v_{\mathrm{sw}}(t) = V_{\mathrm{sw2}} = V_{\mathrm{C_{fly-end2}}} \tag{7}$$

where $V_{\mathrm{C_{in-end1}}}$ is the voltage across C_{in} at the end of phase 1, and $V_{\mathrm{C_{fly-end1}}}$ and $V_{\mathrm{C_{fly-end2}}}$ are the voltages across C_{fly} at the end of phase 1 and phase 2, respectively.

C. Input and Flying Capacitor Voltage Ripple

To estimate $V_{\mathrm{C_{in-end1}}}$, $V_{\mathrm{C_{fly-end1}}}$, and $V_{\mathrm{C_{fly-end2}}}$, the net deviation in voltage across C_{in} and C_{fly} over the duration of each phase must be assessed. For the input capacitance C_{in}, this is dissimilar to the peak-to-peak voltage ripple, as it experiences its peak voltage strictly within the interval of phase 1. By instead constraining consideration to the main phases' boundaries, straight-forward charge conservation can be used. Considering phase 2 and leveraging the assumption of constant current I_{in} in $L_{\mathrm{par(in)}}$, the per phase voltage ripple across C_{in} can be expressed as:

$$\Delta v_{\mathrm{C_{in}}} = \frac{Q_{\mathrm{in},2}}{C_{\mathrm{in}}} = \frac{I_{\mathrm{in}} T_2}{C_{\mathrm{in}}} \tag{8}$$

where $Q_{\mathrm{in},2}$ is the total charge conveyed by the constant current I_{in} in $L_{\mathrm{par(in)}}$ during phase 2. As the ReSC converter provides a fixed 2-to-1 voltage step down, $I_{\mathrm{in}} = \frac{I_{\mathrm{load}}}{2}$ following the principle of energy conservation. Therefore, $\Delta v_{\mathrm{C_{in}}}$ can be expressed as a function of load current:

$$\Delta v_{\mathrm{C_{in}}} = \frac{I_{\mathrm{load}} T_2}{2C_{\mathrm{in}}} \tag{9}$$

Additionally, since the average voltage on C_{in} equals V_{in},

$$V_{C_{\mathrm{in-end1}}} = V_{\mathrm{in}} - \frac{\Delta v_{\mathrm{C_{in}}}}{2} \tag{10}$$

Leveraging charge balance on C_{fly}, the per phase voltage ripple across C_{fly} can be expressed as:

$$\Delta v_{\mathrm{C_{fly}}} = \frac{Q_{\mathrm{load},2}}{C_{\mathrm{fly}}} = \frac{Q_{\mathrm{load},1}}{C_{\mathrm{fly}}} = \frac{I_{\mathrm{load}}\,(T_1 + T_2)}{2C_{\mathrm{fly}}} \tag{11}$$

where $Q_{\mathrm{load},1}$ is the total charge conveyed by the output inductor current i_{L} during phase 1 and $Q_{\mathrm{load},2}$ is the total charge conveyed by the output inductor current i_{L} during phase 2. Noting that C_{fly} admits charge during phase 1 and releases charge during phase 2,

$$V_{\mathrm{C_{fly-end1}}} = \frac{V_{\mathrm{in}}}{2} + \frac{\Delta v_{\mathrm{C_{fly}}}}{2} \tag{12}$$

$$V_{\mathrm{C_{fly-end2}}} = \frac{V_{\mathrm{in}}}{2} - \frac{\Delta v_{\mathrm{C_{fly}}}}{2} \tag{13}$$

Finally, combining from (6), (10), and (12) for V_{sw1}, and (7) and (13) for V_{sw2}, yields

$$V_{\mathrm{sw1}} = \frac{V_{\mathrm{in}}}{2} - \frac{\Delta v_{\mathrm{C_{fly}}}}{2} - \frac{\Delta v_{\mathrm{C_{in}}}}{2} \tag{14}$$

$$V_{\mathrm{sw2}} = \frac{V_{\mathrm{in}}}{2} - \frac{\Delta v_{\mathrm{C_{fly}}}}{2} \tag{15}$$

where (9) and (11) can further be used to relate voltage ripple to I_{load}.

$$V_{\mathrm{sw1}} = \frac{V_{\mathrm{in}}}{2} - \frac{I_{\mathrm{load}}(T_1 + T_2)}{4C_{\mathrm{fly}}} - \frac{I_{\mathrm{load}} T_2}{4C_{\mathrm{in}}} \tag{16}$$

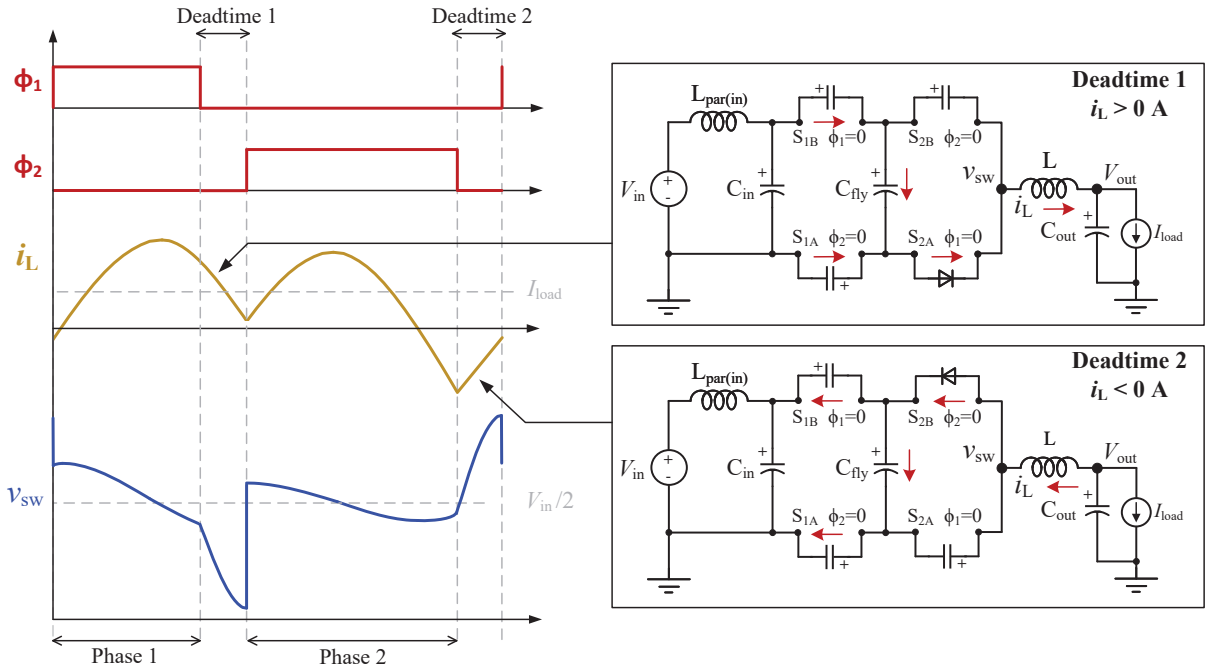


Fig. 4: Key waveforms of partial ZCS operation when i_{L} is positive during deadtime 1 and negative during deadtime 2.

$$V_{\mathrm{sw2}} = \frac{V_{\mathrm{in}}}{2} - \frac{I_{\mathrm{load}}(T_1 + T_2)}{4C_{\mathrm{fly}}} \tag{17}$$

D. Imperfect ZCS Operation

In the case of partial ZCS, there will be current flow during the deadtime and the output inductor can interact with the parasitic output capacitance (C_{OSS}) of the MOSFETs and their body diodes. The inductor current can charge or discharge the C_{OSS} of affected switches, causing an increase or decrease of their drain to source voltages and a subsequent voltage deviation at the switch node. Since the flying capacitor and terminal capacitors are typically orders of magnitude larger than the MOSFETs' C_{OSS}, they can be considered as constant voltage sources during the deadtime intervals.

Figures 3 and 4 show the inductor current waveform, the switch node voltage, and deadtime interactions for partial ZCS cases in the 2-to-1 ReSC converter. During deadtime 1 in Fig. 3, the inductor current is below 0 A. The switch $S_{1\mathrm{B}}$ being previously on, its C_{OSS} remains discharged and the negative inductor current will immediately flow through its body diode. The negative current will increase the charge stored in the C_{OSS} of switch $S_{2\mathrm{A}}$ causing the switch node voltage to rise above V_{sw1}. Similarly during deadtime 2 in Fig. 4, the inductor current is negative and will flow through the body diode of $S_{2\mathrm{B}}$. The negative current will increase the charge stored in the C_{OSS} of switch $S_{1\mathrm{A}}$ also causing the switch node voltage to rise above V_{sw2}.

During deadtime 2 in Fig. 3, the inductor current is above 0 A. The switch $S_{1\mathrm{A}}$ being previously on, its C_{OSS} remains discharged and the positive inductor current will immediately flow through its body diode. The positive current will discharge the C_{OSS} of switch $S_{2\mathrm{A}}$ causing the switch node voltage to fall below V_{sw2}. Similarly during deadtime 1 in Fig. 4, the inductor current is positive and will flow through the body diode of $S_{2\mathrm{A}}$. The positive current will discharge the C_{OSS} of switch $S_{1\mathrm{A}}$ also causing the switch node voltage to fall below V_{sw1}.

This circuit analysis demonstrates that the change in switch node voltage during the deadtime can indicate the direction of the turn off current. In ideal ZCS operation, the switch node voltage will stagnate at V_{sw1} during deadtime 1, and V_{sw2} during deadtime 2. When v_{sw} deviates from V_{sw1} in deadtime 1 or V_{sw2} in deadtime 2, it can be deduced that the converter is not operating with ideal ZCS.

III. Feedback Control Method

A. Digital Voltage Sensing

As described in Section II, at the end of each phase, the measured switch node voltage, with respect to V_{sw1} and V_{sw2} is indicative of the polarity of the turn off current. This principle enables digital voltage sensing to be used for autotuning of ZCS. Voltage sensing is preferred over current sensing as it typically incurs less losses and volume usage. The digital nature of this sensing method reduces the impact of noise and parasitics on the reliability of the control. Figure 5 shows a simplified schematic of the control network that is used to sense v_{sw}. A resistor divider comprising R_{s1} and R_{s2} scales the switch node voltage down to be compared with a precise voltage reference. An additional parallel capacitor divider, C_{s1} and C_{s2}, provides an enhanced frequency response for high bandwidth tracking. Following the flow chart shown in Fig. 6, a voltage comparator compares v_{sw} with the given threshold during each deadtime, and incrementally adjusts each phase

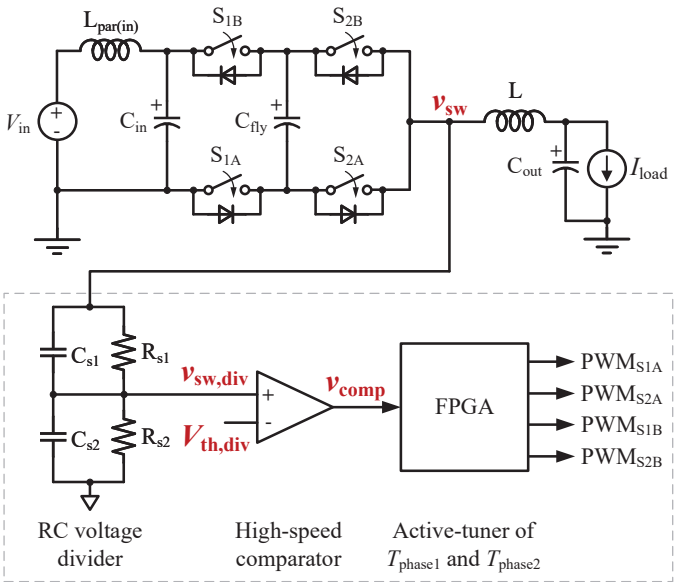


Fig. 5: Block diagram of the proposed topology and control network.

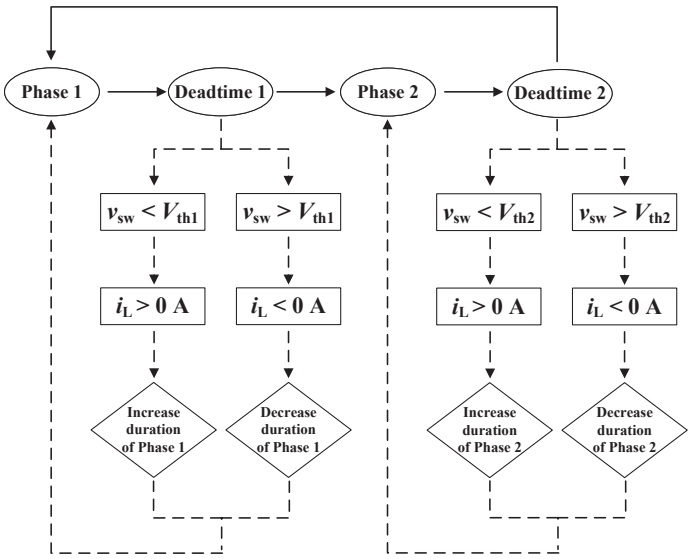


Fig. 6: Flowchart of the proposed control scheme.

duration by a small fixed time step until both phases converge to the desired ZCS operating point.

B. Threshold Voltage and Convergence

If the input capacitor and flying capacitor voltage ripple are neglected, the threshold voltages for deadtime 1 and deadtime 2, V_{th1} and V_{th2}, can be set equal to $\frac{V_{\mathrm{in}}}{2}$. However, as discussed in Section II, in the case of ideal ZCS, $v_{\mathrm{sw}} = V_{\mathrm{sw1}}$ during deadtime 1, and $v_{\mathrm{sw}} = V_{\mathrm{sw2}}$ during deadtime 2. V_{sw1} and V_{sw2} are load dependent and decrease from $\frac{V_{\mathrm{in}}}{2}$ as the inductor current increases. Hence, for the controller to converge closer to the ideal ZCS operating point, it is preferable to estimate and use V_{sw1} and V_{sw2} as threshold references for the comparator instead of $\frac{V_{\mathrm{in}}}{2}$. Using the proposed control method, and as is typical with hysteretic control, the controller will oscillate between a few states having converged. The smaller the time step used to adjust phases 1 and 2 during the deadtime, the closer these oscillating states can be to a 0 A turn off current.

IV. Hardware Prototype and Experimental Results

A prototype was designed and built to verify the proposed feedback control method. Annotated photographs of the hardware prototype are shown in Fig. 7. The MOSFETs and output inductor are on the top side of the board (left), and the gate drive circuitry is on the bottom side (right). The sensing circuitry, including the RC divider for voltage sensing of the switch node and a high-speed comparator (AD8611), is highlighted in Fig. 7. A list of the electrical components used for the power stage and control circuitry is provided in Table I.

Although Sections II and III discuss the need for separate voltage references to adjust the duration of phase 1 and phase 2, this would translate into either using double the sensing circuitry in hardware or implementing a multiplexed voltage reference. Thus, both for simplicity and to minimize the size of the added volume from the control components, a single voltage comparator and threshold voltage is used. For the following experiments, the threshold voltage is selected as the average of V_{sw1} and V_{sw2}.

$$V_{\mathrm{th}} = \frac{V_{\mathrm{sw1}} + V_{\mathrm{sw2}}}{2} \tag{18}$$

To compute the expected value of V_{sw1} and V_{sw2}, T_1 and T_2 are estimated assuming the converter operates as an ideal LC resonant tank:

$$T_1 \approx T_2 \approx \pi\sqrt{LC_{\mathrm{fly}}} \tag{19}$$

Per the equations in Section II, a load point and the value of C_{in} are also required to estimate V_{sw1} and V_{sw2}, and therefore to calculate V_{th}.

Figure 8 displays the key measured waveforms that verify the convergence process towards multi-resonant ZCS operation. To assess the performance of the control with finite terminal capacitance effects, only part of the terminal capacitors listed in Table I is implemented for this test. The input and output capacitances were reduced to 44.5 μF and 73.2 μF from their full value of 150 μF and 229 μF respectively (after dc bias derating). This represents a 73.3% reduction in input capacitor volume and a 74.1% reduction in output capacitor volume for this prototype. Given the flying capacitance is 27.0 μF (after dc bias derating), C_{in} and C_{out} were reduced to be of the same order of magnitude as C_{fly}. Using the derated values for C_{in} and C_{fly}, the inductance L (180 nH as listed in Table I), and the expected load current of 10 A, the calculated V_{th} is 22.6 V. The RC divider ratio for the switch node voltage sensing being 11:1, the reference voltage $V_{\mathrm{th,div}}$ used at the comparator input is $V_{\mathrm{th,div}} = \frac{V_{\mathrm{th}}}{11} = 2.05\,V$. The initial switching frequency and duty cycle for the convergence test

TABLE I: List of the power stage and control circuitry components

Component	Part number	Parameters
MOSFET $S_{1A,1B,2A,2B}$	Infineon IQE013N04LM6ATMA1	40 V, 1.35 mΩ
Flying capacitor C_{fly}	TDK C2012X5R2A475K125AC	X5R, 100 V, 4.7 μF*×18 (in parallel)
Inductor L	Coilcraft XGL6030-181MEC	180 nH, 1.0 mΩ, 43 A
Full input capacitor C_{in}	TDK C3216X6S2A106K160AC	X6S, 100 V, 10 μF*×16 (in parallel)
	TDK C5750X7S2A226M280KB	X7S, 100 V, 22 μF*×12 (in parallel)
Full output capacitor C_{out}	TDK C3216X5R1V226M160AC	X5R, 35 V, 22 μF*×12 (in parallel)
	TDK C5750X7R1V476M230KC	X7R, 35 V, 47 μF*×12 (in parallel)
Gate driver	Analog Devices LTC4440-5	High-side gate driver, 80 V
Bootstrap diode	Infineon BAT6402VH6327XTSA1	Schottky diode, 40 V
High speed comparator	Analog Devices AD8611	4 ns single-supply comparator
Resistor divider	Vishay MCT06030D1501BP100	Thin Film, 1.5 kΩ, 0.1 W
	Vishay MCT0603MD1502BP100	Thin Film, 15 kΩ, 0.125 W
Capacitor divider	Kyocera AVX 06031A101FAT2A	C0G, 100 V, 100 pF
	Kyocera AVX 06035A102FAT2A	C0G, 100 V, 1000 pF
Voltage reference for threshold	Linear Technology LT1790ACS6-5	Low dropout voltage reference

* The capacitance listed in this table is the nominal value before dc bias derating.

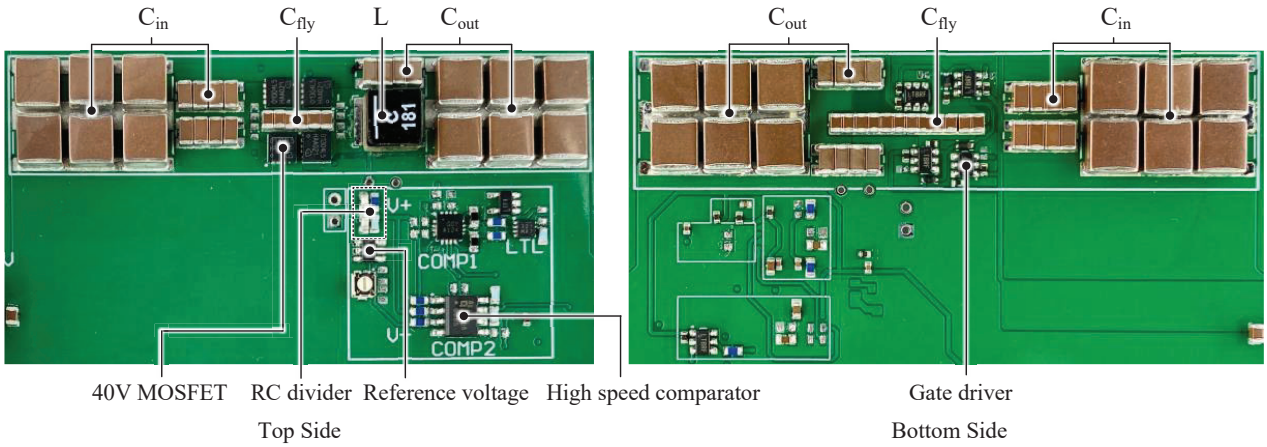


Fig. 7: Photographs of the constructed hardware prototype.

are selected to generate turn off currents distant from the 0 A crossing. Before enabling the control, the turn off current after phase 1 is approximately -12.5 A, whereas it is 9.0 A after phase 2. In the converged state, the inductor current waveform shows that multi-resonant ZCS operation was achieved. The voltage spikes at the switch node during the deadtime are significantly attenuated, demonstrating that the turn off current became negligible. Figure 9 shows the progressive change of the phase durations for the experiment conducted in Fig. 8. The control scheme is enabled at $t = 0\,s$ and, using a time step adjustment of 5 ns, it converges to its final state after approximately 4 ms.

In Fig. 10, the measured load efficiency curves for the hardware prototype are plotted. Owing to the need for high accuracy measurements, a Yokogawa WT5000 was used for all efficiency measurements. Two cases are shown: (a) using the full terminal capacitances of $C_{in} = 150\,\mu$F and $C_{out} = 299\,\mu$F, and (b) using the reduced terminal capacitances of $C_{in} = 44.5\,\mu$F and $C_{out} = 73.2\,\mu$F. For each case, the efficiency of the converter when the phase durations are determined by the controller is compared with the efficiency of the converter when the phase durations are set according to equation (19). As stated in section II, when C_{in} and C_{out} are large, the phase duration estimate made in (19) is satisfactory. Hence, in Fig. 10(a), both efficiency curves follow similar trends. The efficiency using the ZCS autotuner is still marginally higher as it allows for better soft switching operation given equation (19) cannot account for passive component tolerance and circuit parasitics. When C_{in} and C_{out} are reduced, the estimate in (19) can no longer ensure ZCS operation and the efficiency using the ZCS autotuner is significantly higher as shown in Fig.10(b).

Table II lists the full load efficiencies of the 2-to-1 ReSC converter with different terminal capacitances and with or without the proposed ZCS autotuning method. In the case of reduced terminal capacitances, ZCS autotuning can allow for up to 44% reduction in power loss at full load compared with open-loop control. In addition, using the ZCS autotuner,

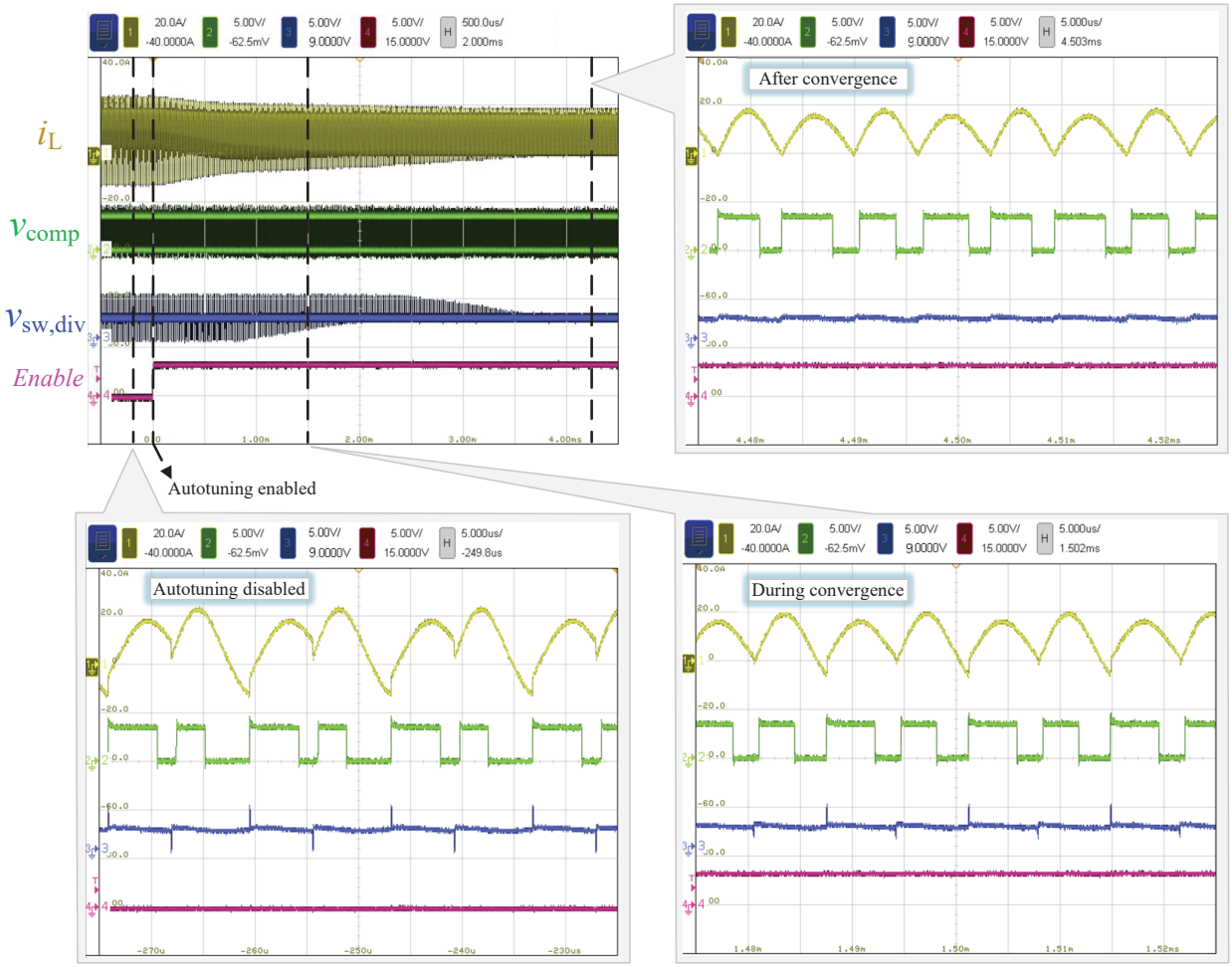


Fig. 8: Measured inductor current i_{L}, comparator output v_{comp}, RC divided switch-node voltage $v_{\mathrm{sw,div}}$, and control *Enable* signal demonstrating the convergence towards multi-resonant ZCS operation. This test was conducted with reduced terminal capacitances (C_{in} = 44.5 μF, C_{out} = 73.2 μF) and a load current of 10 A.

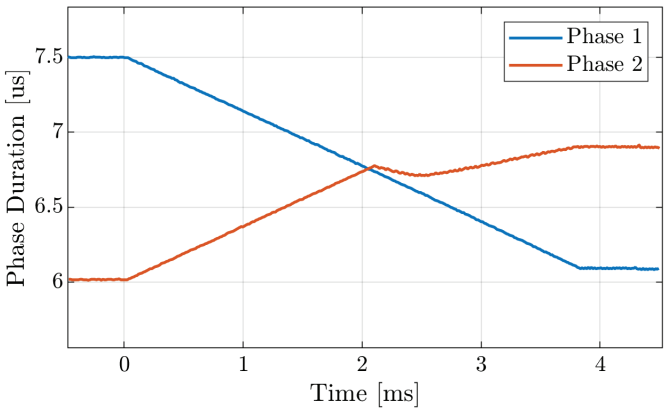


Fig. 9: Convergence process of phase durations after the activation of ZCS autotuning at $t = 0\,s$.

the full load efficiency of the converter is 98.7% with the full terminal capacitances and 98.5% when it is reduced. The proximity of these values demonstrate that, with the proposed control technique, the total terminal capacitor volume can be reduced by more than 70% with marginal effect on efficiency.

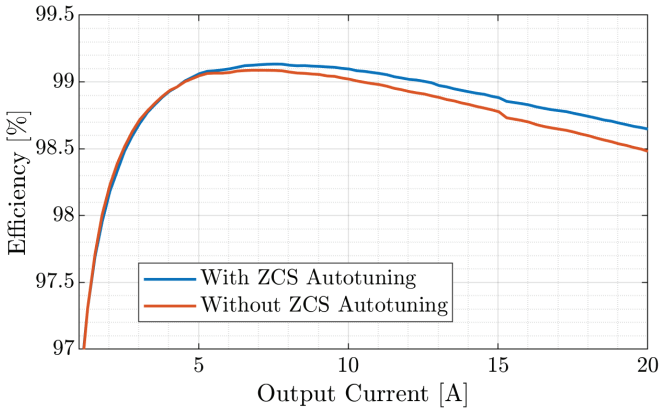
V. Conclusion

With reduced terminal capacitances, a ReSC converter can no longer achieve symmetric resonant operation with ZCS at the LC tank resonant frequency, leading to higher conduction and switching losses. Theoretically, an optimum operating point can still be determined to ensure multi-resonant operation with ZCS. However, in practice, the optimum switching frequency and duty ratio cannot be precisely calculated due to circuit parasitics and component tolerance and derating (with voltage bias, temperature, and age). To preserve the efficiency while combating these non-idealities, this paper proposes a closed-loop hysteretic control technique that can dynamically track an optimum operating point and achieve ZCS by modifying the phase durations. The proposed control technique is implemented on a 48-to-24-V ReSC converter prototype for experimental verification. Using the ZCS au-

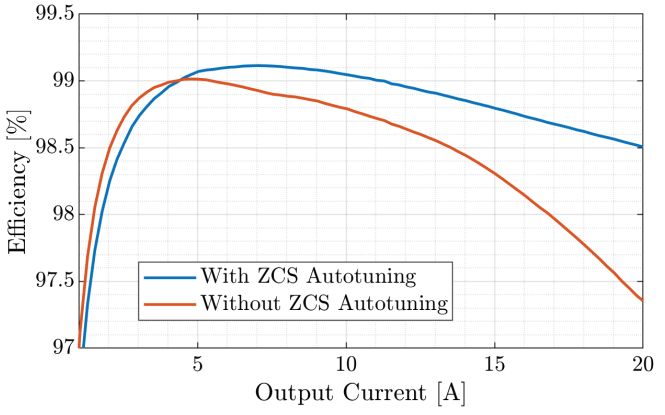
TABLE II: Full load efficiency comparisons

C_{fly} [μF]*	C_{in} [μF]*	C_{out} [μF]*	Total terminal capacitor volume [mm^3]	Control method	f_{sw} [kHz]	D	Full load efficiency	Power loss reduction by ZCS autotuner
27.0	150	299	1974	Without ZCS autotuning† With ZCS autotuning	72.2 73.9	0.50 0.483	98.5% 98.7%	13.3%
27.0	44.5	73.2	520	Without ZCS autotuning† With ZCS autotuning	72.2 77.0	0.50 0.469	97.3% 98.5%	44.4%

* The capacitance listed in this table is the value after dc bias derating (extracted from component datasheet).
† Without ZCS autotuning, phase durations are set per equation (19).



(a)



(b)

Fig. 10: Measured efficiency curves with both autotuning control enabled and disabled: (a) the full terminal capacitance is used (C_{in} = 150 μF, C_{out} = 299 μF), (b) the terminal capacitance is reduced (C_{in} = 44.5 μF, C_{out} = 73.2 μF). Without ZCS autotuning, phase durations are set per equation (19).

totuner, over 70% reduction in terminal capacitance volume was achieved with no compromise on the peak efficiency and only a 0.2% decrease in full load efficiency. Moreover, both with large and reduced terminal capacitances, the proposed feedback controller improves the efficiency of the converter compared with open-loop control. In the case of reduced terminal capacitances where the resonant frequency of the converter significantly deviates from $\frac{1}{2\pi\sqrt{LC_{\text{fly}}}}$, the controller allows for up to 44% reduction in power loss.

REFERENCES

[1] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 903–10 919, 2022.

[2] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, 2015.

[3] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, 2012.

[4] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, Jun 1995, pp. 1215–1221 vol.2.

[5] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 841–851, March 2008.

[6] R. C. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*. IEEE, 2008, pp. 4008–4015.

[7] Y. Zhu, Z. Ye, and R. C. N. Pilawa-Podgurski, "Modeling and analysis of resonant switched-capacitor converters with finite terminal capacitances," in *2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*, 2021, pp. 1–6.

[8] Y. Zhu, Z. Ye, T. Ge, and R. C. N. Pilawa-Podgurski, "Multi-resonant compensation control for terminal capacitance reduction in resonant switched-capacitor converters," in *2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*, 2021, pp. 1–6.

[9] J. Xu, L. Gu, and J. Rivas-Davila, "Effect of class 2 ceramic capacitor variations on switched-capacitor and resonant switched-capacitor converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2268–2275, 2019.

[10] T. Urkin, G. Sovik, E. E. Masandilov, and M. M. Peretz, "Digital zero-current switching lock-in controller ic for optimized operation of resonant scc," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5985–5996, 2020.

[11] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5048–5062, 2018.

[12] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946–4958, 2020.

[13] T. Ge, Z. Ye, and R. C. Pilawa-Podgurski, "A 48-to-12 v cascaded multi-resonant switched capacitor converter with 4700 w/in^3 power density and 98.9% efficiency," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 1959–1965.