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# Charged Particle Detection using a CMOS Active Pixel Sensor

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Abstract--Active Pixel Sensor (APS) technology has shown promise for next-generation vertex detectors. This paper discusses the design and testing of two generations of APS chips. Both are arrays of 128 by 128 pixels, each 20 by 20 µm. Each array is divided into sub-arrays in which different sensor structures (4 in the first version and 16 in the second) and/or readout circuits are employed. Measurements of several of these structures under Fe<sup>55</sup> exposure are reported. The sensors have also been irradiated by 55 MeV protons to test for radiation damage. The radiation increased the noise and reduced the signal. The noise can be explained by shot noise from the increased leakage current and the reduction in signal is due to charge being trapped in the epi layer. Nevertheless, the radiation effect is small for the expected exposures at RHIC and RHIC II. Finally, we describe our concept for mechanically supporting a thin silicon wafer in an actual detector.

#### I. INTRODUCTION

MODERN collider detectors frequently need to measure a Wvertex that has an origin away from the collision point. Vertex detectors provide tracking information to decide whether a track comes from the primary vertex or from a secondary decay [1]. With impact resolution in the tens of microns, they can identify particles with  $c\tau$  of 100's of microns. Consequently, they are ideal to detect mesons with charm or bottom quarks, which have these decay properties.

#### A. Previous Vertex Detectors

Vertex detectors have been successfully constructed using silicon strip detectors. These are placed so the strips are at small angles to one another, providing a measure of the track position along the strip. Other vertex detectors make use of a pixel structure. Such pixel detectors have the advantage of simultaneously measuring all three space point coordinates. They do not have the hit ambiguity problem of strip detectors. In addition, the small pixel size provides excellent spatial resolution. For example, the SLD collaboration built a vertex detector [2] based on CCD technology [3]. As the detector is in a low radiation environment, CCDs could be used at this accelerator. CCDs require that the charge be transferred from one pixel to another. Charge in the end row of a pixel chip, for example a  $1000 \times 1000$  array, must be transferred through more than 1000 pixels before being digitized. Therefore, any small loss in charge transfer produces large signal loss and signal sharing.

Because of the high radiation environment and need to have the vertex detector in the trigger, CCDs are not the appropriate choice [4] at LHC (Large Hadron Collider) at CERN. At the LHC, the three major experiments [5] decided to use a hybrid technology where the sensor is bump bonded to a read-out chip. The hybrid technology has the disadvantage that the pixel size is much greater than a CCD pixel and that two chips have to be assembled. The two chips and their interconnection are much thicker than can be done in CCD technology.

#### B. APS Radiation Detectors

Through research by the LEPSI/IReS group [6], Active Pixel Sensors (APS) [7] have recently emerged as a competitor to CCDs and the hybrid technology for charged-particle pixel detectors. The CMOS section for an APS chip has three layers. The top layer of the device has an n+ diffusion / n-well surrounded by a p-well region. Below it is a more lightly doped ( $p^-$ ) epitaxial (epi) silicon layer and then the p+ wafer silicon. As most of the epitaxial region is field free, electrons and holes diffuse in the epitaxial region.

Electric fields develop at the interfaces where the doping levels change, so that electrons in the epitaxial layer are reflected at the p-well and p+ interfaces. At the epi and n-well interface, the electric field pulls the electrons into the n-well. Since the capacitance of this diode is quite small, the voltage changes significantly for a small amount of collected charge (~30  $\mu$ V/e). The voltage, on this reverse biased floating diode formed by the n-well and p<sup>-</sup> epitaxial layer, is read out when a column and row line addresses the pixel.

When a charged particle traverses the APS sensor, it creates electron-hole pairs in the epi layer. As the epi region can be much thicker than a conventional APS diode, a greater amount of charge can be liberated and collected. Because the epi layer is field free, the holes produced by the charged pair diffuse until they reach the  $p^+$  substrate, while the electrons diffuse until they reach a pixel's  $n^+$  diode. Because of this phenomenon, hits spread out over several pixels, while CCDs tend to collect the charge in one or two pixels.

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APS detectors can be built with thin wafers and with small pixels just like CCDs. Unlike CCDs, charge is directly read out from each pixel without shifting through the rest of the detector. In principle, APS detectors can operate in much higher radiation environments than CCDs. Furthermore, as they can be built in standard CMOS, features such as ADCs and zero suppression can be put in the periphery of the chip. For example, to make a high-speed APS sensor, [8] put an ADC on each pixel.

#### C. STAR with a New Inner Vertex Detector

The STAR Collaboration [9] is examining whether APS technology is appropriate for an inner vertex detector [10]. That detector is currently running at RHIC (Relativistic Heavy Ion Collider), which is operated by Brookhaven National Laboratory. The focus of the detector is to study collisions between circulating Au beams at 100 GeV·A. Initial measurements at this energy have been completed. As there have been recent technical progress with vertex detectors, it is now conceivable that detailed measurements on charmed quarks can be made.

Simulations show that the STAR detector could detect charmed particles but not produce differential cross sections. The STAR detector does contain a vertex detector called the SVT (Silicon Vertex Tracker). The SVT uses three layers of silicon drift detectors to measure the position of a track. These detectors are relatively thick (a few percent of a radiation length), far (> 6 cm) from the interaction point, and have a predicted position resolution of 20  $\mu$ m. To study the physics of charm, a high-resolution inner vertex detector is needed in STAR.

We have been simulating a hypothetical vertex detector with thickness of 80  $\mu$ m and resolution of 4  $\mu$ m. There are two cylindrical detectors at radii of 2.8 cm and 3.82 cm away from the interaction point. Inside the detector, there is Be beam pipe with a radius of 2.2 cm. Simulations show that with such a detector an invariant cross section from the D<sup>0</sup> meson can be measured. What follows in this paper is our work to investigate whether an APS detector is appropriate for accelerator experiments.

#### II. CHIP CONFIGURATIONS

Two CMOS radiation sensor ICs, APS-1 and APS-2, have been designed, fabricated, and tested. Each prototype sensor array includes 128 by 128 pixels with a pixel size of 20 by 20  $\mu$ m. Each array is about 2.5 mm on a side. Both chips were designed in a standard TSMC digital 0.25  $\mu$ m CMOS process that includes an 8-10  $\mu$ m epitaxial layer. The layouts of the chip and some previous results with a 1.5 GeV electron beam have been discussed in [11].

The circuit to read out the diode is shown in Fig. 1. In this paper, we will discuss our design APS-2, which has 16 test structures. We will concentrate on four standard APS configurations that have 1, 2, 3 or 4 pickup diodes. In general,

we have found similar results when comparing APS-1 to APS-2.



Fig. 1. The circuit diagram shows the main APS pixel circuit that is reported in this paper. For the case where there are two to four diodes in a pixel, the sensor consists of multiple diodes that are connected in parallel.

The LEPSI/IReS group [12] has modeled the charge diffusion process for standard APS geometries. In their simulation, they compared the charge collected in a pixel with a 1-diode and another with a 4-diode configuration. They modeled the charge collection in a single pixel and with a  $2 \times 2$  and a  $3 \times 3$  pixel sum and then obtained good agreement with detailed measurements. To analyze the results of our detector, we will analyze single pixel hits and also various pixel sums.

#### III. TESTS WITH FE<sup>55</sup>

To record the data from the APS chip, we built a test DAQ board to digitize and store the data. The output of the APS went to an ADC, which digitized the data at 0.4 MHz into 16 bits. All data presented below are taken at room temperature. We use the correlated double sample method to remove and reduce fixed pattern and reset noise by subtracting subsequent frames. As the chip is not reset in between reads, the difference is simply the integrated charge in the diode, and reset noise is canceled. Fig. 2 shows a typical spectrum from Fe<sup>55</sup>. To create this histogram, we use a very simple algorithm that looks for the highest ADC value and then sum over a square array of pixels, for example  $5 \times 5$  pixels, such that the peak pixel is at the center of that array. After making that sum, we zero those pixels and then repeat the procedure. We stop looking for hits when the highest pixel is less than a pre-determined threshold. A more sophisticated algorithm could produce better results, which might enhance the performance on the detector. For instance, if the shape of the charge distribution were included, then the full signal could be found in fewer pixels. This

algorithm would decrease the number of channels included in the sum and thus reduce the noise.



Fig. 2. This is a histogram of a typical ADC spectrum for summing  $5 \times 5$  pixels. The curve shows the fit to the 5.9 keV x-ray line. This plot has a high pedestal because the data were taken at low rates.

Similarly, we also do sums of  $3 \times 3$  (9 pixels) and  $7 \times 7$  (49 pixels). To sum 4 pixels, we take the  $3 \times 3$  array and then find the highest  $2 \times 2$  sum that contains the center pixel. We take the highest 4-pixel array and then find the highest 3 pixels to find the 3-pixel sum. We use a similar method to find the 2-pixel sum. Monte Carlo studies have shown that the 2, 3, and 4 pixels sums are biased because they are susceptible to noise fluctuations. As the noise is comparable to the charge collected in the outside pixels, the algorithm tends to pick those pixels where the noise is larger. Consequently, the 9 pixel sums are a more accurate measurement of the energy of an event than the fewer pixel sums. The counts with higher ADC values are produced by pileup events. The reconstruction algorithm is very simple and does not reject those events.

The diffusion of the electrons in the epitaxial layer can be studied by comparing different numbers of pixel sums. Fig. 3 shows the measured charge for various sums. The single pixel sum shows a peak at 5.9 keV. This peak is produced when the  $\gamma$ -ray converts near the n<sup>+</sup> diode and all the charge is collected. If the x-ray does not convert near the diode and coverts in the epi layer, the charge diffuses in the epi layer. The various pixel sums show the extent of diffusion. These data show that a 5 × 5 array captures most of the charge but not all.



Fig. 3. Various  $Fe^{55}$  spectra for different pixel sums. The top curve is for a single pixel. The other curves represent a square pixel array centered on the highest pixel. Each graph has a label that indicates the square pixel sum area. The insert in the top graph shows the 5.9 keV peak at a higher scale. The x-axis shows the number of ADC counts. The  $Fe^{55}$  peak can be seen in each sum. It varies from about 60 counts in the upper plot to around 260 in the 9 × 9 pixel sum.

We define signal to noise, as the mean charge in the Fe<sup>55</sup> peak divided by  $\sigma_1\sqrt{n}$ , where *n* is the number of pixels summed and  $\sigma_1$  is the sigma of the noise for a single pixel. Fig. 4 shows this ratio for different number of diodes attached to the standard APS configuration. From these data, we conclude that the single diode structure has slightly better over-all signal to noise ratio then the other configurations. It is apparent that the extra charge collected by the diodes has less of an effect than the increased capacitance of the diodes. The data presented in this figure have the one diode near the other transistors of the APS circuit. We found that if we centered the diode in the middle of the pixel, the signal to noise ratio is worse. This reduction occurs because the extra capacitance of the longer trace reduces the measured voltage.



Fig. 4. Signal to Noise for different diode configurations. The symbol for the 1, 2, 3, and 4 diode sums are respectively open diamond, closed triangle, open square and closed circle.

#### IV. RADIATION EFFECTS

To determine the effect of radiation, we exposed the chips to 55 MeV protons at the Lawrence Berkeley Laboratory 88" Cyclotron. Each APS chip was mounted in a chip carrier. The center of the chip was about 2.38 cm away from the beam center. The intensity of the beam was monitored by the standard 88" beam diagnostics in beam line 3B. The diagnostic program measures the fluence in protons/cm<sup>2</sup>. To scale from the low energy proton exposure to that of RHIC, we used the NIEL scaling hypothesis that is described in [13].

Table I shows the exposures for the various chips. We use the conversion that 1 rad =  $6.7 \times 10^6$  protons/cm<sup>2</sup>. We assume that a RHIC year provides collisions for a continuous total of 20 weeks and that RHIC II has a luminosity 40 times RHIC.

We measured the leakage currents before and after the radiation exposure. The leakage current before the exposure was approximately the same for each chip.

TABLE I RADIATION EXPOSURE FOR TEST AT THE 88" CYCLOTRON. RHIC EXPOSURE IS THE EQUIVALENT NUMBER OF YEARS ASSUMING NOMINAL OPERATING CONDITIONS. RHIC II IS THE PROJECTED RADIATION DOSE FOR THE NEW MACHINE THAT IS 40 TIMES THE LUMINOSITY OF RHIC.

Exposure	Proton Flux (x10 <sup>12</sup> cm <sup>2</sup> )	Equivalent Dose (krad)	RHIC Exposure (y)	RHIC II Exposure (y)
1	0.144	21	18	0.5
2	0.485	72	62	1.5
3	0.96	143	122	3.1
4	3.02	451	385	9.6
5	9.88	1475	1259	31.5

The mean leakage current is subtracted when extracting the signal for a hit. So leakage current only becomes an issue, when the shot noise from the accumulated leakage charge between pixel reads becomes significant compared to other noise sources. The leakage charge is a product of leakage current and readout time, so that increasing the readout speed or reducing the temperature can control the leakage current generated shot noise. Increased leakage current, however, requires a more frequent reset to keep the diode voltage in the correct operating range.

The time to read each pixel was 2.56  $\mu$ s and the total time measured for the leakage current was 2.63 ms. The maximum speed of the APS chip is about 1 Mpixel/s, which, if used, would reduce the measured leakage charge.

We can then see the radiation exposure's effect on signal and noise on the performance of the chips. Fig. 5 shows the results. To determine the Fe<sup>55</sup> peak, we use the same technique as previously described. We were able to measure a clear peak for all exposures except the highest at  $1.0 \times 10^{13}$  p/cm<sup>2</sup>. The data show a decrease in pulse height and a gradual increase of noise.



Fig. 5. The top graph shows the Fe<sup>55</sup> signal as a function of fluence, while the bottom graph shows the increase in noise.

Radiation induced bulk damage in the epi layer can explain some of the loss of signal. The traps can capture the diffusing electrons and prevent them from being collected by the APS diode. To determine where the charge is lost, we measured the response to Fe<sup>55</sup> of an irradiated detector. Figs. 6a-b show the results of an unexposed detector, while 6c-d show one that exposed to 143 krad. Both Figs. 6a and 6c demonstrate that the 5.9 keV x-ray peak occurs at the same place. Therefore, the basic CMOS operation is not compromised and the gain in the diode is not affected. However, Figs. 6b and 6d show there is a shift in the  $5 \times 5$  pixel sum for the irradiated chip. This shift occurs in the charge collected from the epi layer, and therefore it implies that charge is lost in the epi layer. The LEPSI/IReS group has made similar measurements [14] with neutron radiation. Their conclusions for the effect of radiation damage are consistent with ours.



Fig. 6. Comparison of a detector that was exposed to 143 krad of 55 MeV protons to an unexposed detector. Graph a) shows the single pixel charge collected for an unexposed chip, while b) shows the sum for a 5 × 5 array. Similarly, c) shows the single pixel charge for the irradiated detector and d) the 5 x 5 pixel sum. The vertical line shows the location of the  $F^{55}$  5.9 keV x-ray, The peak position of the 5.9 keV peak is in the same location for a) and c), while the charge collected through the epi-layer, as shown in the 5 × 5 sum is different. The higher energy 6.5 keV Fe<sup>55</sup> line can be seen in a) and not c) because a) has an order of magnitude more events. These plots were taken at a higher rate than the other Fe<sup>55</sup> data, so there is a more significant pileup effect. The 5 × 5 sums have a minimum seed value of 20.

To study the source of the noise, we calculated the contribution caused by the shot noise of the leakage current. We then subtract the shot noise and plot the residual noise. These results are shown in Fig. 7. As the residual noise is roughly constant with leakage current or radiation fluence, the increase in noise can be attributed mostly to shot noise. As the leakage charge decreases with readout speed, reading the chips faster would result in less noise. Once again, the extra leakage current is only important, if the shot noise exceeds the other contributions. In this figure, we have converted the scale into electrons. To do this, we assume all of the charge of the Fe<sup>55</sup> is collected by in the 5.9 keV peak. This corresponds to 1638 electrons.

It is clear that this increase in noise and reduction of signal might restrict the use of APS technology. To explore its use in a potential accelerator environment, we examine the impact of its use at RHIC. Exposure #1 is the estimated equivalent of 18 years at RHIC, while the exposure #2 is projected to be equivalent to 1.5 years at RHIC II. These data show that the reduction on performance of the chip is relatively small. As mechanical supports could be designed so that the silicon can

be replaced each year, the detector need only last one year in an accelerator environment until a convenient accelerator maintenance period occurs. From these tests, we have a strong indication that APS technology can withstand the radiation environment of RHIC.



Fig. 7. This upper line shows the variation of noise with leakage current. The lower line is the result when the shot noise is subtracted. The y-axis is in units of electrons.

#### V. MECHANICAL DESIGN

Because we want to minimize the mass of the detector, we have had some sample wafers thinned to 50  $\mu$ m and are currently developing methods for handling and supporting the thinned silicon strips under tension. As the p<sup>+</sup> substrate only provides mechanical support for the device, it is possible to remove it and have the same sensitivity to charged particles. In fact, it is common, in astrophysical CCD applications, to remove this substrate [15] and sometimes even remove part of the epi layer so that the back of the chip can be illuminated.



Fig. 8. The right picture shows the mechanical concept for mounting three ladders of silicon. The darker shaded area represents the silicon, while the lighter shaded region that extends past the silicon is the aluminum-Kapton cable.

Our concept for a detector support is illustrated in Fig. 8. In this design 10 cm silicon detector strips or ladders and aluminum Kapton flex cables are supported under tension by the gray structures at either end. The ladders, consisting of five  $1.6 \times 1.6$  cm CMOS chips, are shown in darker shading. The flex cables are shown in lighter shading. As shown in the left side of the figure, there are two detection layers, one at an inner radius and one at an outer radius. The 24 ladders are

arranged in modules of 3 ladders as shown on the right side of the figure. The detector unit is supported at one end only so that the whole assembly can be easily removed and replaced should the primary beam stray.

#### VI. SUMMARY

Our results show that APS technology is very promising for developing a vertex detector. Our chips can detect particles from x-rays to electrons. Unlike CCDs, charge for APS chips diffuse to several pixels. Consequently, the intrinsic signal to noise is less for APS chips, as many pixels need to be summed as charge diffuses in the epi layer. Radiation tests show that the APS technology should be radiation resistant under nominal RHIC operating conditions. When RHIC II becomes operational, there would be only a small decrease in signal and increase in noise over a three-year exposure. Mechanical prototypes are under construction and will soon be studied to ascertain a practical method of supporting very thin silicon.

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