UNIVERSITY OF CALIFORNIA, SAN DIEGO

Digital Signal Generation for Wireless Communication Systems

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electrical Circuits and Systems)

by

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The dissertation of Jeremy Rode is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2010

Dedication

To my parents and Dr. Nibbles

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Chapter 3, in part, is a reprint of the material as it appears in the *2008 IEEE MTT-S International Microwave Symposium Digest*. The author of this dissertation was the primary investigator and primary author for this publication. The amplifier used for the measurements used active devices from a CMOS chip designed by Tsai-P Hung.

Chapter 4, in part, is a reprint of the material as it appears in "Transmitter architecture using digital generation of RF signals" in the *2003 IEEE Radio and Wireless Conference Proceedings*. The author of this dissertation was the primary investigator and primary author for this publication. Parts of this chapter are also a reprint of the material as it appears in a chapter entitled "Adaptive Circuit Approaches for Microwave Transmitters" inside the edited book, *Multifunctional Adaptive Microwave Circuits and Systems*. The author of this dissertation was the primary investigator and primary author for the parts used from this publication. The data from the hardware measurements in section 6 was originally used in "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters" in *2007 IEEE MTTS-S International Microwave Symposium Digest*.

In chapter 5, the amplifiers used for measurements were based off a design first used in "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters" in *2007 IEEE MTT-S International Microwave Symposium Digest*.

Chapter 6, in part, the amplifier used for measurements was based off a design first used in "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters" in *2007 IEEE MTT-S International Microwave Symposium Digest*.

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ABSTRACT OF THE DISSERTATION

Digital Signal Generation for Wireless Communication Systems

By

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Doctor of Philosophy in Electrical Engineering (Electrical Circuit and Systems)

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Professor Peter M. Asbeck, Chair

Radio Frequency (RF) transmitters have long been realized by analog circuitry particularly at the front-end that interfaces with the antenna. Migrating wireless transmitter functions from analog to digital circuitry can bring many benefits such as lower cost, lower power, and higher integration while eliminating some of the drawbacks of analog circuitry such as sensitivity to temperature and processing variation. The objective of this dissertation is to investigate and analyze techniques used to implement wireless transmitters with digital circuitry. Several different transmitter designs addressing different wireless standards are presented, which serve to show the advantages of the digital approach, highlight major obstacles to its success with emphasis on the

issues unique to digital transmitters, and introduce novel analysis and simulation techniques leading to new designs addressing the obstacles identified.

The dissertation begins by summarizing barriers to digital transmitter implementation, and introducing new metrics to facilitate comparative evaluation. In-band power ratio is discussed, a novel metric useful for the prediction of relative efficiency of switching amplifiers driven with different quantization algorithms.

The transmitter system examples begin with a low-power standard with relatively low signal accuracy requirement (ZigBee) where a novel quantization algorithm driving a CMOS amplifier highlights the digital transmitter benefits of simplicity, high integration, and low total transmitter power.

The dissertation then discusses more complex, higher-power systems (CDMA and WCDMA) to highlight the major obstacles to a cellular-handset-class digital transmitter. Novel optimizations of a delta-sigma modulator's digital implementation and noise transfer function design allow the modulator to operate quietly in the receive band, while retaining realistic clock frequencies and word lengths.

Through laboratory measurements, analysis, and fixed-time-step simulations developed in this work, a set of nonlinearities is discovered that is inherent to types of switching amplifiers driven by aperiodic broadband signals. The cause of these nonlinearities is presented, and validated by an amplifier redesign reducing these nonlinearities by more than an order of magnitude.

A variation on a well-known digital encoding algorithm, band-pass pulse width modulation, is shown to achieve amplifier efficiencies better than delta-sigma, without exciting broadband noise from amplifier nonlinearities. Novel digital-to-time circuit

topologies and frequency domain simulations are presented to attain the high accuracy time resolution needed to achieve pulse width modulation at high frequencies. Laboratory measurements are provided showing the efficiency and noise advantages of this design.

A digital polar amplification system is presented highlighting novel digital drive algorithms. A general study on broadband noise generated by polar amplifier systems is undertaken with simulation and analysis. Unique time-domain properties of polar broadband noise, due to common impairments such as time misalignment, are presented and analyzed. A pre-distortion technique is presented that can reduce the broadband noise in polar amplifiers though the addition of simple DSP operations.

Lastly, a novel all-digital frequency synthesis algorithm is presented along with hardware measurements.

Chapter 1

Introduction

1. Wireless Communication Systems

The explosive growth in functionality of modern wireless mobile devices has largely been driven by advances in digital signal processing and microprocessors implemented in digital CMOS circuitry. For the last few decades, computers and the driving force behind them, digital CMOS manufacturing, have been following an exponential growth in inexpensive functionality, commonly referred to as Moore's Law. However, many components of wireless communication systems, especially those near the antenna, are still implemented with purely analog circuits.

A major component that remains an analog circuit is the transmitter. This dissertation presents methodologies for digital implementation of transmitters. The following sections of chapter 1 introduce wireless transmitters, discuss the differences between traditional analog transmitters and the proposed transmitter design methodology, and then present the benefits of digital implementation. The chapter concludes with a presentation of the goals of this dissertation and a summary of its organization.

2. Transmitters for Wireless Communication Systems

A wireless transmitter fundamentally takes a signal (or data) and formats it to enable transmission over the air using electromagnetic radiation for reception by a receiver. In the case of the familiar FM radio system, an audio signal is transmitted to multiple receivers, with the transmitter encoding the audio data into a format suitable for

radio frequency (RF) transmission. This is the process of modulation. This signal is also translated to a higher frequency (by mixing or upconversion), amplified, and launched into an electromagnetic wave at the antenna. Both the transmit frequencies and power levels can vary by many orders of magnitude, depending on the specific application.

The transition from input data to transmitter begins with baseband processing to format the data. Since these signals are relatively low frequency, and free of any carrier, they can be easily implemented digitally (although they are still done in analog circuits in some legacy systems). Digital baseband signal generation will be briefly covered in the following section, as baseband signal generation methods affect the key signal properties in digital transmitters.

2.1. Baseband Signal Generation

Baseband signal generation applies digital modulation to a carrier signal to map the transmit data stream to changes in the amplitude and phase of the carrier signal. The details of the different standards are beyond the scope of this dissertation, except for one example used to introduce baseband concepts: quadrature phase-shift keying (QPSK). In QPSK, a commonly used digital modulation, data bits are mapped to four levels of carrier phase shift according to the equation:

$$S(t) = \sqrt{2}\cos\left(\omega_c t + (2i+1)\frac{\pi}{4}\right), i = 0,1,2,3 \quad (1)$$

S(t) is the normalized amplitude QPSK modulated signal, ω_c is the carrier frequency in radians per second, and i corresponds to the transmitted symbols. To facilitate time-sampled representation, transmitters typically break the baseband signal representation

into to two orthogonal basis functions, describing the signal as a sum of sine and cosine functions:

$$S(t) = I(t)\cos(\omega_c t) + Q(t)\sin(\omega_c t) \tag{2}$$

Thus the signal in (1) can be represented by two carrier-free lower frequency signals, I(t) and Q(t) in (2), referred to as the in-phase and quadrature signals respectively.

The I and Q signals are commonly visualized on a constellation diagram, a two dimensional plot with I on the x-axis and Q on the y-axis. The constellation diagram of QSPK, with the data to symbol mapping annotated is given in Figure 1.

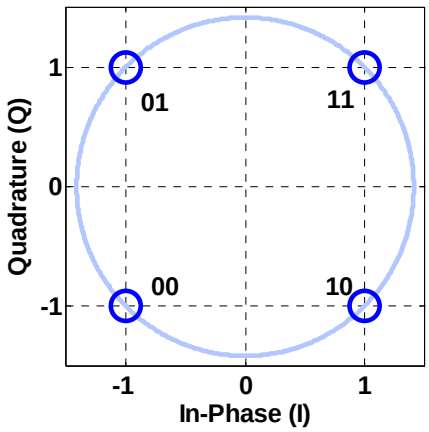

Figure 1: Example QPSK constellation diagram annotated with Gray code symbol mapping and the unit circle.

The digital data is mapped to corresponding points on the constellation diagram at instants of the time set by a sampling rate, referred to as the symbol time. The symbol rate is set by the data rate divided by the bits per symbol of the system. (So far, the signal has not been defined by the transmitter at any other point in time.)

The signal trajectory between the symbol times has a profound effect upon both out-of-band spectral characteristics and the amplitude of the signal between the symbols. The time-varying signal amplitude at the symbol rate will be referred to as the envelope

of the signal, to differentiate this amplitude variation from the instantaneous amplitude variation of a sinusoidal carrier signal.

This leads to a alternate representation of communication signals commonly used, a polar representation where E(t) is the envelope or signal magnitude, and θ is the signal phase shown below:

$$S(t) = E(t)e^{j\omega_c t+\theta(t)} \tag{3}$$

Both the time varying amplitude and the polar representation of a communication signal are important factors in signal amplification.

Using a signal trajectory following the unit circle on the constellation diagram will maintain constant envelope amplitude, but will increase the bandwidth of the resulting signal, reducing its spectral efficiency. In a transmitter, the transition trajectory is set by a pulse shaping filter that defines the baseband signal for all times other than the symbol times. In effect, the filter is taking each symbol (a pulse) and shaping the transient response of the pulse.

A common pulse shaping filter is a raised-cosine filter, a sinc function with a roll-off factor applied to truncate its impulse response. The impulse response of an example raised-cosine pulse shaping filter is given in Figure 2, below:

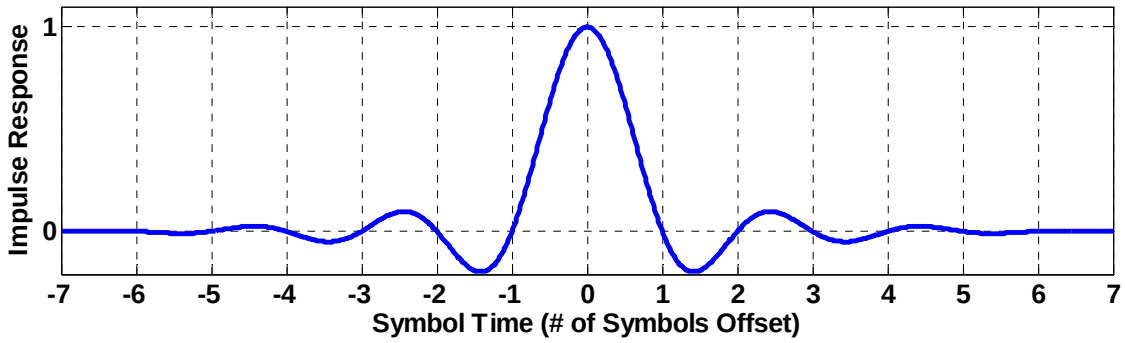

Figure 2: Raised cosine filter impulse response (roll-off factor = 0.22).

The pulse shaping is achieved by convolving both the baseband signals with the above impulse response at an elevated sampling rate. Ideally the signal values at the symbol times remain unchanged, and thus the impulse response of the filter is zero at all other times.

Filtering results in a signal trajectory describing a path on the constellation diagram between the previously specified symbols. An example of a QPSK trajectory is created by taking four symbol transitions and applying the pulse shaping filter described in Figure 2. This is added to the constellation diagram in Figure 1, resulting in Figure 3, shown below:

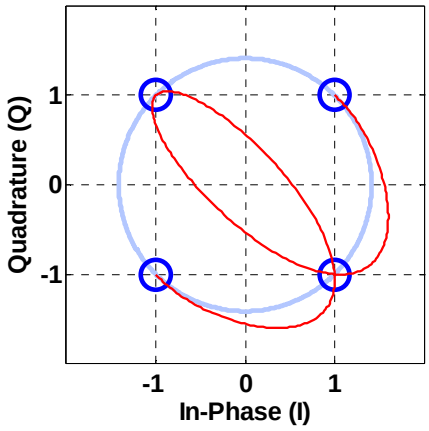

Figure 3: Example I/Q signal trajectory from a 11 10 01 10 00 data stream.

Filtering also has the side effect of increasing the necessary word-length of the digital value used to represent the signal. Prior to the pulse shaping filter, a two-bit signal sampled at the data rate was sufficient to represent the incoming data. Post filtering, both the word-length and sampling rate of the signal are significantly increased.

At this point, classical transmitter designs diverge from the designs to be presented in this work. Classical designs will first be briefly covered, and then digital designs will be presented, while contrasting the differences.

2.2. Classical Transmitters

The block diagram of a commonly used classical transmitter design is given in Figure 4, below:

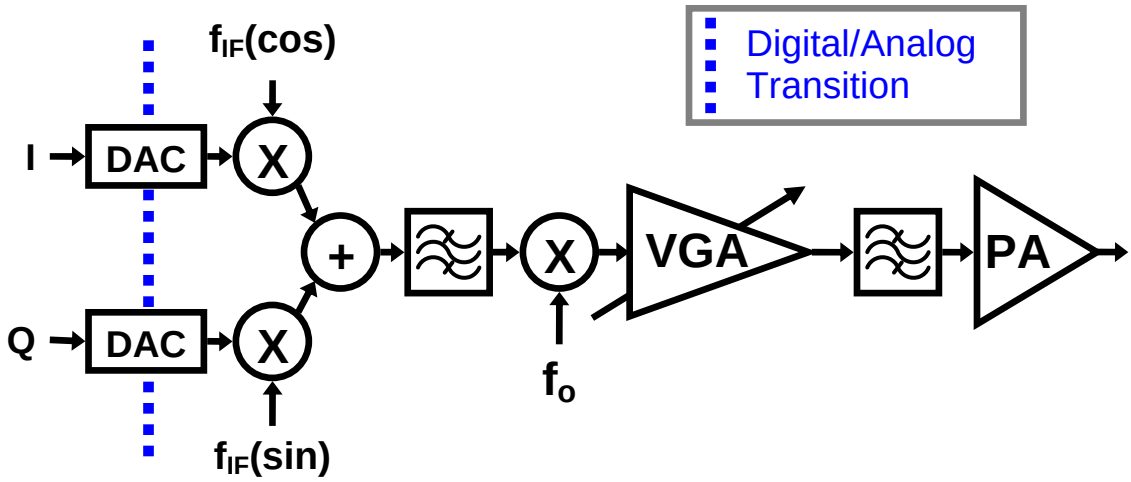

Figure 4: Block diagram of a heterodyne transmitter.

The block diagram begins with the two baseband I/Q signals, from the last section, converted from a digitally represented number to a corresponding analog voltage level by a pair of digital-to-analog converters (DACs). The blue dotted line denotes the

transition from the digitally represented signals to signals represented by continuously varying voltage (analog domain). The line is for comparison with the digital transmitter to be introduced.

The two analog baseband signals are mixed (multiplied) by a sine and cosine function respectively and summed. Referring to equations (1) and (2), this operation results in an output of the desired signal, a phase modulated carrier signal.

The resulting signal, referred to as an intermediate frequency (IF), is spectrally identical to the final signal, save for having a lower frequency. This signal is typically filtered in the IF, as a greater amount of filtering can be achieved, for a given filter quality, at lower frequencies. The IF signal is then mixed again to upconvert it to the final transmit frequency. The signal is then amplified through an amplifier, or chain of amplifiers, depending on the power level required.

The example of Figure 4 shows a pair of amplifiers, the first of which is commonly referred to as a driver amplifier and a final amplifier, commonly referred to as a power amplifier (PA). Here the driver amplifier is a variable gain amplifier (VGA), which is used to vary the output power of the transmitter. A variable output power is becoming a common feature in transmitters, as any power transmitted in excess of the level needed to produce the required signal to noise ratio at the receiver wastes energy and causes unnecessary interference.

2.3. Digital Transmitters

In the last transmitter example, all of the functions except for the baseband pulse shaping filter occurred in the analog domain. This is in contrast with the focus of this work, a digital transmitter. A block diagram of a digital transmitter is shown below:

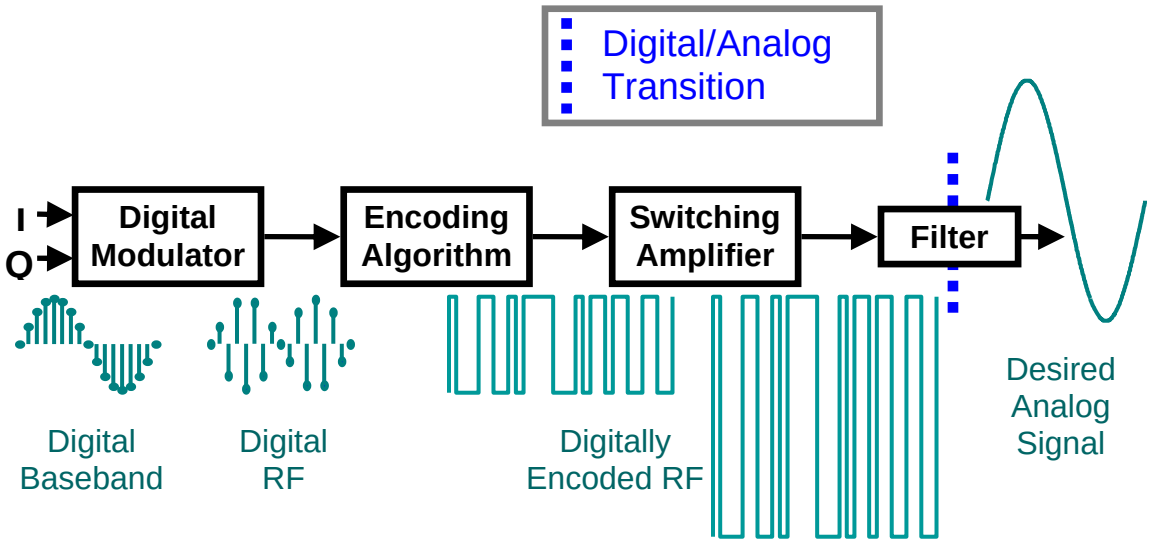

Figure 5: Block diagram of a digital transmitter. Shown with exaggerated example waveforms.

The digital transmitter starts with the identical I/Q inputs as the previous transmitter example. Instead of converting the digital signal to a varying voltage level, the signal representation is maintained as a digital value. The sampling rate of this digital signal is increased in rate, in this representative example, to a multiple of the desired transmit frequency. The signal is also mixed (multiplied) digitally with sine and cosine functions to upconvert it to the desired transmit frequency.

In this digital transmitter example, the signal is subsequently run though an encoding algorithm that maps (quantizes) the high numerical precision digital signal to

two states. The resulting signal is a digitally encoded RF signal consisting of the desired signal and added error resulting from the mapping operation, referred to as quantization noise. Encoding algorithms typically control the properties of this quantization noise such that virtually all of the added noise is at a different frequency than the desired signal. Quantization is necessary to format the digital signal to directly drive a switching amplifier.

The signal is then amplified by a switching amplifier. A switching amplifier is a system where the active devices are held either in the fully on, or fully off position, similar to the operation of a switch. Ideally, the devices are never held in a partially on or partially off state; the devices in a switching amplifier are only allowed to rapidly transition through the partially conducting states. This allows for high efficiency amplification, as devices dissipate the least amount of power when held in the full on or full off state.

Lastly the signal is filtered to remove the unwanted quantization noise added by the encoding step. At this point the signal is transitioned from the digital domain back into a continuously varying analog voltage. As this is the last step in the transmitter, this type of transmitter is referred to as a digital transmitter.

2.4. Digital Encoding / Quantization

As stated before, the quantization algorithm maps the many-state digital signal into a few-state signal suitable for driving a switching amplifier. The quantization algorithm exploits the narrowband nature of the desired signal by controlling the frequency distribution of the added error signal. Quantization algorithms for the

modulator will be referred to as low-pass or band-pass depending on whether the added quantization noise falls spectrally above, or both above and below the desired signal, respectively. The transfer function that describes this property is referred to as a noise transfer function (NTF). The NTF is the inverse of the desired modulator transfer function, i.e., a band-pass modulator has a band-stop NTF.

Waveforms of a common quantization algorithm, delta-sigma (sometime referred to as ΔΣ, sigma delta, or ΣΔ), encoding a two-tone signal are given below:

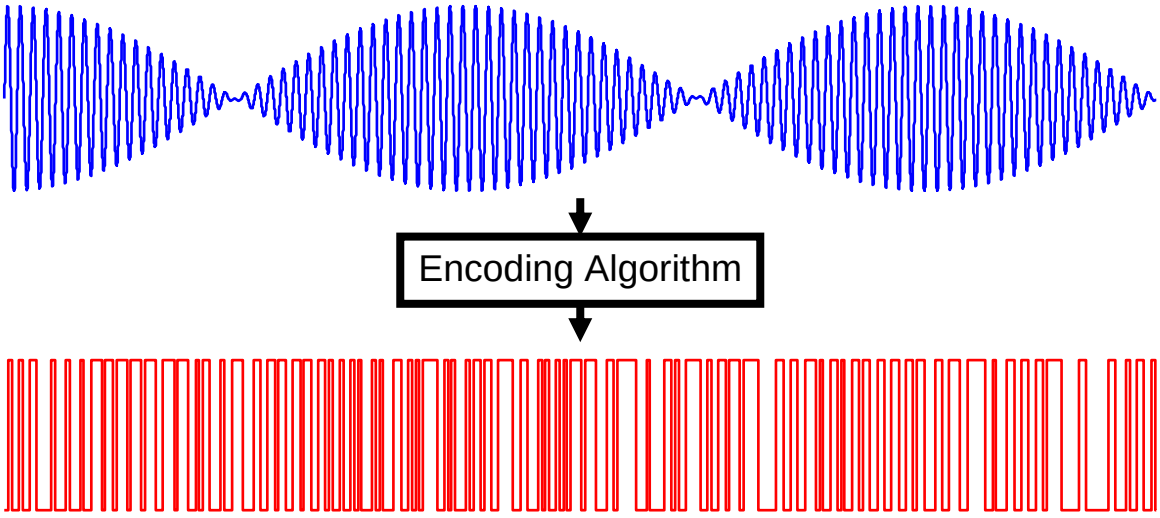

Figure 6: Example waveforms of an encoding algorithm quantizing a two-tone signal. Input at the top, and output at the bottom.

The top signal is a two-tone signal, a sum of two sine waves that differ slightly in frequency. Due to a variety of properties, and ease of generation, a two-tone signal is a commonly used test sequence in RF engineering. The bottom shows the two-tone signal encoded by a band-pass delta-sigma modulator. It is difficult to visually determine that the input signal is contained in the encoded bit stream.

Using a Fourier transform to bring the above signals in the frequency domain verifies that the two-tone signal is still present, despite being visually buried. The magnitude of the discrete time Fourier transforms (referred to as a spectrum or power spectral density, PSD), of the above signals are shown below:

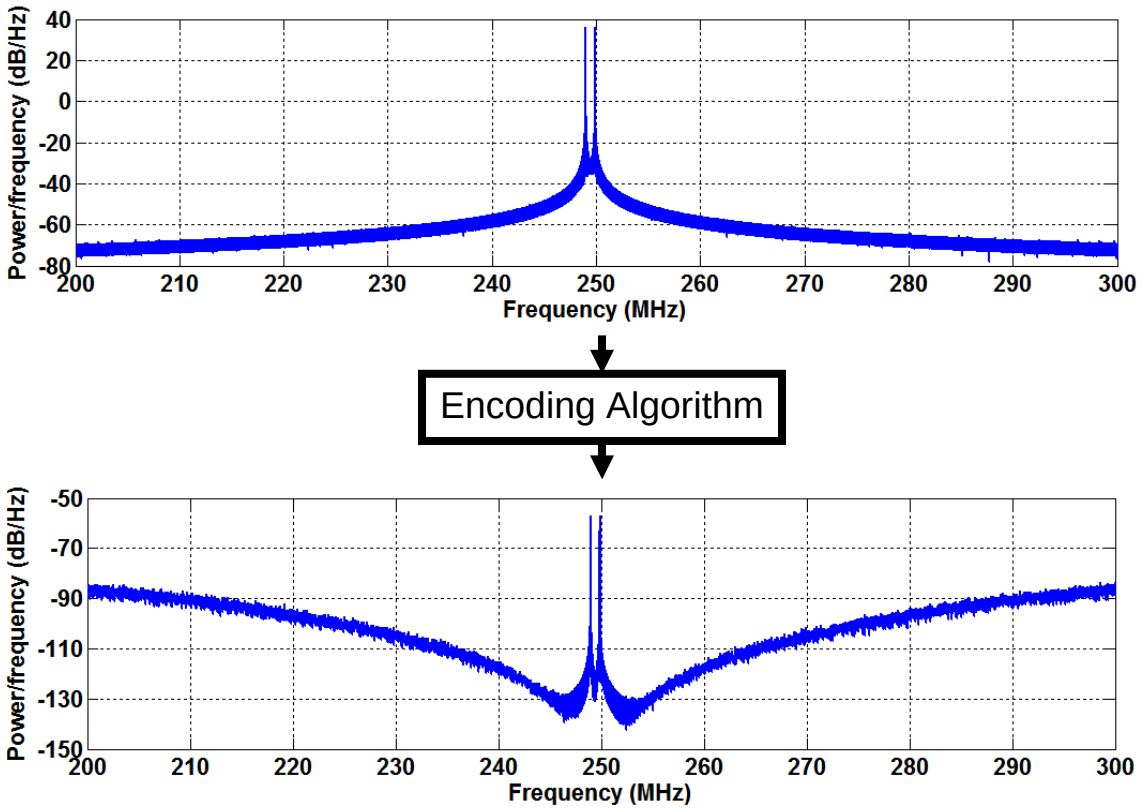

Figure 7: Computed spectra of the signals from Figure 6. Input at the top, and output at the bottom.

The Fourier transform reveals that the two-tone signal is still present, and can be recovered by filtering with a filter with the inverse transfer function of the NTF, here a band-pass filter.

2.5. Transmitter Figures of Merit

The major figures of merit (FOM) used to evaluate the performance of transmitters fall into three basic categories: power, accuracy, and purity. These figures of merit will be extensively used throughout the work, and will be briefly introduced here.

The power FOM category includes the maximum and minimum RF power the transmitter can deliver and how much supply power is required in the creation of the RF signal. The drain efficiency (DE) is the RF output power expressed as a ratio to the DC supply power used. An additional measure, power-added efficiency (PAE), results from subtracting the RF input power from the output RF power and expressing this as a ratio to the power used. These definitions are blurred slightly by a digital transmitter, which begins with digital bits and ends in a relatively high power RF signal, so more appropriate measures will be introduced in chapter 2.

The power FOM serve to determine the relative range of the transmitter based on the power, and the amount of battery life expected based on the power consumed. The amount of heat dissipated is also determined by the power efficiency. Efficiency numbers are typically expressed in percent, and power is typically expressed in watts, milliwatts (mW), or decibels relative to 1 mW (dBm). The ratio of the maximum to minimum RF power transmitted is referred to as dynamic range or power control range and is typically expressed in decibels. High dynamic range leads to more efficient spectral use, since mobile units in urban environments can lower their transmit power enabling smaller co-channel network cells, while still being able to operate in larger urban cells.

FOM in the accuracy category measure how accurately the transmitter reproduces the intended signal. The major FOM used in this work is error vector magnitude (EVM). The complex baseband communication signal is represented as a vector on a Cartesian plane, with the x-axis (real axis) for the in-phase and the y-axis (imaginary axis) for the quadrature signal. At the sampling time, the desired ideal signal vector is subtracted from the actual transmitted signal vector. Typically the resultant square of the error is normalized to the signal power and the root mean square (RMS) is taken. This subtraction and normalization results in a unitless RMS EVM expressed typically in percent.

The accuracy FOM category gives insight into the spectral efficiency of the transmitter. Noise degrades the accuracy of the signal, as does passage through a transmitter with a high EVM. The signal from transmitters with lower EVM can tolerate more noise and are still recoverable by a receiver.

Lastly, the purity FOM categories provide measures of how much RF power the transmitter generates at unintended frequencies. Spectral purity measurements include adjacent channel power ratio (ACPR), adjacent channel leakage ratio (ACLR), harmonic levels, spurious emissions, and receive band noise. The adjacent or alternate channel figures measure the relative levels of interference a user on an adjacent or alternate channel would experience from the operation of the transmitter in question. This is typically expressed as a unit-less power ratio relative to the transmit power: decibels relative to carrier (dBc). Different standards have varying ways of calculating these powers, i.e., different integration bandwidths, and offsets. At lower powers this

specification can transition to an absolute power level independent of in-band signal power.

Spurious noise is typically noise generated at frequencies out of the transmit band the system is intended to operate on. The levels are specified as an absolute power per frequency (expressed in power spectral density, dBm/Hz). Receive band noise is a special case of spurious noise arising in full-duplex wireless systems (systems that transmit and receive simultaneously). Spurious noise from the transmitter that falls in the receive channel can interfere with the receiver (self-interference). Due to the extreme sensitivity of modern receivers, the maximum noise generated by the transmitter in the receive band can easily be ten orders of magnitude less than the transmit power.

3. Migrating from Analog to Digital

With the advance of modern CMOS processes into multi-gigahertz clock frequencies, migrating RF transmitter blocks to CMOS circuits has become feasible. Transitioning analog circuits to monolithic CMOS is not straightforward. Traditional analog designs suffer when directly translated into submicron CMOS circuitry. Major problems for submicron CMOS transmitter design include: low voltage operation affecting analog headroom, impedance matching for output power, and area-hungry low-Q inductors.

Many of the disadvantages of analog circuitry in submicron CMOS can be overcome by migrating analog transmitter functions to digital equivalents. Digital circuit implementation provides many advantages over analog, including ease of testability and decreased sensitivity to temperature, processing, and aging effects. Digital circuits are

more adaptable, allowing changes with a simpler design cycle, or in some cases, their functionality can be changed on the fly (in programmable or "software radio" systems) [1]. A major additional advantage of digital circuits is that they can be readily incorporated into CMOS-based systems-on-chips and can better take advantage of process geometry shrinks than their analog counterparts.

There are many promising opportunities for the implementation of wireless transmitters with entirely digital circuit approaches. Digital architectures have advantages not only in increasing integration, decreasing size and lowering cost, but can also help reduce power dissipation. One of the most power hungry components of a transmitter is the power amplifier. Digital techniques allow the PA to be driven with signals comprising distinct quantized amplitude levels. These distinct levels facilitate the driving of switching amplifier architectures. In low RF output power applications, the amplification stage might consist solely of a large inverter stage implemented on the digital chip, creating a whole transmitter system-on-a-chip.

4. Goals of Dissertation

The goal of this work is to study techniques allowing the implementation of digital wireless transmitters meeting the relevant specifications of a contemporary communication standard without sacrificing the power or integration benefits of digital design approaches. Development of fully specification-compliant digital transmitters that outperform analog transmitters is a very challenging goal considering the present state of the art. The contributions of this dissertation are to identify major obstacles to successful

digital transmitter implementations, to analyze these obstacles, and to identify novel solutions that bring digital implementations closer to engineering use.

5. Organization of Dissertation

With the exception of chapters 2 and 8, this work is organized around chapters dedicated to a specific communication standard paired with an encoding algorithm.

5.1. Communication Standards Chosen

The work begins with analysis of ZigBee, a low-power wireless personal area network (WPAN) standard. Novel digital transmitter designs, using current CMOS technology, are presented that have both better performance (especially lower power) and better anticipated economics from migration to CMOS integrated designs.

The communication standards for the later designs were chosen specifically because their implementation entirely in the digital domain is extremely difficult, yet the payoff is large. These communication systems have modulations with a time-varying envelope that traditionally preclude the use of a switching amplifier. The digital transmitter designs targeting the more complex cellular handset standards will serve to both illuminate the obstacles and to show the analysis and innovations required to enable a digital transmitter.

5.2. Chapter Organization

The second chapter serves to familiarize the reader with the key issues prevalent in all of the digital transmitter designs. Concepts are introduced that will further the understanding of subsequent chapters. Novel figures of merit are introduced, including

in-band power ratio, a metric useful for predicting amplifier efficiencies with different drive signal encodings.

The third chapter is dedicated to analyzing the advantages a digital transmitter design brings to a ZigBee/802.15.4 system, a half-duplex communication system with a several milliwatt power output, and a low peak-to-average ratio (around 2-3 dB). A novel digital encoding algorithm is introduced reducing the total transmit power, while simultaneously allowing the transmitter to be fabricated entirely in a low voltage digital CMOS process.

The fourth chapter looks at new digital designs for a transmitter meeting the challenging set of specifications corresponding to code division multiplexing (CDMA) cellular handset standard. The chapter takes a design route, previously published by members of the UCSD engineering department [2], using a delta-sigma modulator to encode the signal. The chapter highlights the design differences between the delta-sigma modulator used for driving a PA and that of more traditional delta-sigma systems for oversampling based analog-to-digital and digital-to-analog conversion. The chapter introduces new logical optimizations to improve the design of the digital logic enabling the delta-sigma algorithm to run at muli-gigahertz clock rates. Lastly, experimental results are shown, which demonstrate the presence of a unique nonlinearity arising from interactions in switching amplifiers with tuned loads driven with non-periodic signals.

The fifth chapter is dedicated to the identification, analysis, simulations, and discussion of solutions to the nonlinearity identified in the previous chapter. A non-traditional time domain methodology to simulate the amplifier with aperiodic drive is developed, capturing the nonlinearity to an extent not possible with many standard

simulation techniques. Test signals are presented that quickly distinguish this nonlinearity from more traditional slew rate impairments that can also affect amplifiers driven with delta-sigma signals. Lastly, an amplifier redesign, with measurements, is presented to validate the above analysis and simulation.

The sixth chapter is dedicated to pulse width modulation (PWM), a technique commonly used for low frequency switching power systems, such as DC/DC converters and amplifier systems. A straightforward modification to this modulation technique is presented that transforms PWM from a low-pass modulation to a band-pass modulation. This low-pass to band-pass modification allows PWM (now band pass PWM, or BPPWM) to reproduce communication signals with clock rates equal to that of the transmit frequency. Unique issues pertaining to the digital generation of both PWM and BPPWM, where digital transitions are no longer aligned to the transitions of the digital timing clock, are addressed in the simulation with a frequency domain technique. A novel circuit is presented which is based on a delay locked loop (DLL) that serves as a digital-to-time converter, generating time-accurate digital transitions unaligned with a timing clock. Lastly, amplifier measurements are presented that demonstrate the benefits of RF BPPWM transmitter systems over delta-sigma systems.

The seventh chapter introduces a digital variation of the polar transmitter. The polar technique, also referred to as envelope elimination and restoration (EER), is an increasingly relevant amplifier topology enabling efficient amplification of high peak-to-average power ratio (PAPR) signals. The chapter deals with a relatively slowly varying voltage mode class-D (VMCD) amplifier supplying a current to a rapidly varying current mode class-D amplifier (CMCD). This pair of amplifiers takes advantage of the band-

limited properties of communication signals, mapping the fast and slow varying parts of the signals to different amplifiers that can each deal efficiently with the different types of signals. The chapter presents a completely digital driven version of this technique, with a unique voltage-to-current conversion provided by an inductor between the two amplifiers. Algorithms are presented that work around some of the issues of a digital polar amplifier, while preserving their amplifier efficiency.

The eighth chapter is dedicated to a novel all-digital frequency synthesis algorithm. Frequency synthesis is the process of generating a varying reference clock from a fixed reference source. This synthesized source can be rapidly tuned to different frequencies, typically corresponding with the different channels used by a wireless communication standard, to increase capacity. Frequency synthesis is not traditionally considered part of the transmitter per se, as frequency synthesis is also required by a receiver, but is a requirement for a complete transmitter design. This chapter will present an algorithm to generate an arbitrary frequency from a fixed frequency reference using only digital components. This algorithm highlights the advantages of a quantization technique, developed in other work at UCSD [3], which is superior to delta-sigma when subjected to nonlinearities. Measurements are introduced and compared to known art in frequency synthesis.

In the ninth and final chapter, the results of this work are summarized. Future directions in digital transmitter work are suggested.

6. References

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[3] A. Swaminathan, A. Panigada, E. Masry, I. Galton, "A Digital Requantizer With Shaped Requantization Noise That Remains Well Behaved After Nonlinear Distortion" in *IEEE Transactions on Signal Processing*, vol. 55 iss. 11 pp. 5382-5394 November 2007.

Chapter 2

Digital Transmitter Design Issues and Metrics

1. Introduction

Although many parallels can be drawn between digital and traditional transmitters, digital transmitters have unique advantages and disadvantages with unique trade-offs. This chapter introduces metrics that were developed in this dissertation to evaluate the performance of digital transmitter systems and amplifiers. Metrics were developed both to create fair comparisons between digital transmitter systems and traditional analog systems, and also to evaluate the relative performance of digital transmitter subsystems. Design challenges specific to digital transmitters are also summarized.

A new metric is introduced in this chapter: in-band power ratio, which is useful in comparing the expected efficiency of amplifiers driven by different encoding algorithms, without necessitating laboratory measurements.

2. Design and Measurement Challenges

2.1. Digital Amplifier Testing

The drive conditions of digitally driven amplifiers in highly integrated CMOS systems are difficult to replicate in a laboratory environment. In an integrated system, the RF switching amplifier is driven by the digital logic gates of the encoding system. In higher RF power systems, a driver or chain of drivers is necessary to switch the larger

gate capacitance of the higher power output devices. When the system resides entirely on a CMOS chip, the electrical lengths of the lines between the encoder, driver, and amplifier can be made significantly smaller than the all pertinent wavelengths, including the carrier frequency and higher order harmonics.

In laboratory experiments involving digital transmitters, switching amplifiers under test are driven by a signal source far removed from the amplifier, and typically matched to a 50 Ω source impedance. At the frequencies set by the communication standards examined in this work, it is impossible to reduce the electrical length between the source and the device under test (DUT) without putting the signal generation on-chip. Integrating the signal generation on-chip complicates the design and necessitates fabrication of separate chips for each significantly different test, an unrealistic approach. In this dissertation the signal generation is physically separated from the amplifier systems necessitating impedance matching strategies for testing.

The amplifier input signal generated by the source must be transmitted though a variety of connectors and electrical structures before reaching the gates of the amplifier DUT. In order to achieve proper device switching, the rapid transients of the digital drive signal must be preserved, precluding any use of resonant impedance matching circuitry. In addition, for accurate power output measurements input RF power from the signal generator must not leak through to the output. This is especially important for the low power systems work presented in this dissertation.

In order to preserve the high speed signal characteristics, while preventing both power leak-though and standing waves on the input of the amplifiers under test, a resistive match is placed as near as possible to the amplifier input, typically on-chip. The

matching resistor reduces the reflected power back to the source and minimizes the possibility of input power leaking through to the output.

As already discussed, this resistive match isn't needed in the final integrated design. Unfortunately, the resistive match required in the laboratory setting leads to difficulty in some of the metrics traditionally used to define amplifier gain, as it heavily penalizes metrics such as power-added efficiency (PAE) that account for traditional amplifier gain. For this reason, three gain independent efficiency measurements are used: Drain efficiency, two-stage efficiency, and system efficiency, all of which are defined in section 3.

2.2. Switching Amplifiers and Aperiodic Drive

Traditional switching amplifiers are typically designed to amplify signals with high levels of periodicity. In this case, amplifier analysis and testing using periodic drive signals accurately predicts actual amplifier performance. As switching events of the amplifier occur at the same point in the matching structure resonances, understanding the drain waveforms is fairly straightforward, as steady-state analytical models apply.

However, when aperiodic drive signals are substituted, amplifier waveforms become more complex, as switching events can occur at different points in the matching structure resonances. Amplifier switching in and out of phase with the resonant structures can cause unexpected behavior that is dependent on the exact switching sequence. An example of an aperiodic signal drive causing unexpected amplifier behavior is a switching event in a voltage mode class-D, occurring at the current peak of the output series resonance. This switch at the peak causes reverse current to flow

through the pull-up device back to the DC supply. As most realistic DC supplies can only source current, the reverse current charges the supply, causing a rise in the supply voltage. This introduces a memory effect, as the next switching event will introduce a higher than expected supply to the amplifier output.

Interactions similar to this example are a major difference between traditional periodic switching amplifier design and the designs presented in this work. Many of the simulation tools used to design switching amplifiers fail to capture these complex interactions and incorrectly predict amplifier performance. Fixed time-step simulation techniques are introduces that address these issues.

3. Figures of Merit and Metrics to Address Digital Amplifier Design

3.1. Drain Efficiency

Drain efficiency (DE) is the ratio of desired RF output to consumed DC power in an amplifier. One major caveat in the use of DE in digital transmitters is the quantization noise in digital transmitters, extra output power in digital transmitters that is not typically significant with most traditional analog transmitters. It is important to ensure that the RF output power measurement only takes into account power in the desired band of operation. Use of a standard power meter at the output of a digital transmitter can give optimistic results compared with a more accurate measurement using a spectrum analyzer to integrate across the transmit band.

One of the major advantages of DE is that it can be used to directly compare the efficiencies of digitally driven switching amplifiers to traditional analog amplifiers. However, DE gives an unfair advantage to the switching amplifier, as a switching

amplifier of equivalent power will normally demand a drive signal larger than that of an analog amplifier. Nonetheless, this metric will still be extensively used, as it easily measured, offers insight into power efficiency, and does not rely on driver chain power dissipation estimates when the amplifier is outside of its target drive environment. Extending the efficiency measure to encompass more of the transmitter system is necessary for a more realistic efficiency metric, the subject of the rest of section 3.

3.2. Multistage Efficiency and Power-Added Efficiency

Power-added efficiency (PAE) is a commonly used metric in analog amplifiers. PAE is defines as the in-band RF power output subtracted from the RF input power, with the difference in a ratio to the DC power consumed. The closest metric to PAE for switching amplifiers in lab setups suffering from the input matching issues described previously is two-stage or multistage amplifier efficiency. Multistage amplifier efficiency is the RF power output over all of the DC power consumption necessary to both operate the amplifier and the drivers necessary to charge and discharge the gate capacitance of the power amplifier devices. This is a more realistic metric to judge switching amplifier power performance, especially where the output drive from standard size digital logic gates is not strong enough to directly drive the PA.

3.3. System Efficiency

Digital amplifier system efficiency is the ratio of the in-band RF output power of the system to the power required to generate this RF signal all the way from baseband I/Q signals. This metric can be used to very accurately compare digital transmitters with

traditional designs. As shown in chapter 1, Figures 1-2, a digital transmitter design is radically different from its analog counterpart. The most accurate power efficiency comparison takes into account not only all of the power necessary both to run the RF power amplifier chain, but also all of the power required in data conversion and frequency conversion chain.

System efficiency has a major drawback in that power consumption of all the transmitter blocks is not always known. Literature describing traditional transmitter systems does not always include the power dissipation of the entire system. Even when provided, the system power dissipation published for integrated RF systems can include a variety of additional circuitry implementing a host of different functions, such as frequency synthesis, receivers, or media access control. Also, laboratory systems can use signal sources in place of an up-converter chain, so that amplifiers can be tested decoupled from the entire transmitter system. System efficiency calculations of laboratory setups often have to rely on estimated or simulated power dissipation of transmitter functions implemented by test equipment.

3.4. In-Band Power Ratio for Digital Amplifiers

In-band power ratio is defined as the ratio of the desired signal power to the total power in an encoded RF signal. The total power in an encoded communication signal is made up of the desired signal with added quantization noise. Using the delta-sigma encoded two-tone example from chapter 1 section 2.3, Figure 1 shows the spectrum of the encoded two-tone signal with the desired signal and the quantization noise annotated.

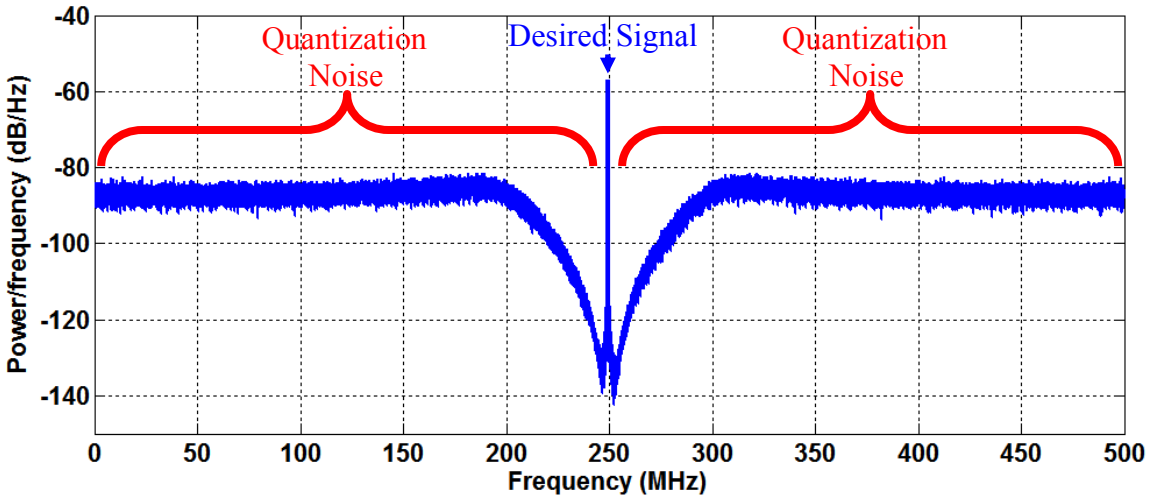

Figure 1: Spectra of two-tone from chapter 1, Figure 4, zoomed out to the Nyquist frequency and marked to illustrate in-band power ratio.

The in-band power ratio here can be calculated by power averaging the spectral power of the two-tone signal, and dividing it by the total signal power. The total signal power is the desired signal plus the quantization noise where the power density is integrated out to the Nyquist frequency for the clock rate used.

In-band power ratio is an excellent comparative predictor of digital amplifier performance in systems dominated by losses related to switching. Switching losses include capacitive charging and discharge loss, crowbar/shoot-through currents during switching, and out-of-band losses due to finite resonator Q. In-band power ratio, as an efficiency predictor, does not account for in-band dissipative losses such as the on resistance of switching devices, and losses in the resonator/matching circuitry. This is due to most of the dissipative losses being proportional to output power, and the switching losses being proportional to the number of transitions. The number of transitions generated by band-pass wideband noise shaping algorithms tend to be very similar, as the noise spectrally falls equally above and below the desired signal.

All of the coding algorithms used in this work shape the added quantization noise, and over the long term change states with the same probability, independent of signal and encoded in-band power. Figure 2 shows the transition probability of two of the encoding algorithms used in this work.

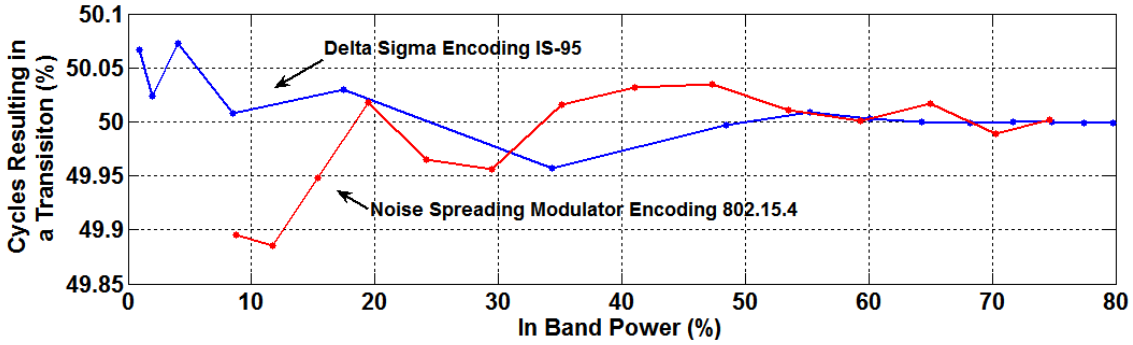

Figure 2: Switching probability of different encoding algorithms encoding different communication standards to be used in this work (IS-95 CDMA and ZigBee/802.15.4). Shown across the entire back-off range of in-band power, including tunings that cause limit cycles. The values are normalized to a $F_S/4$ modulator clock frequency.

Switching probabilities and thus switching losses are relatively constant over different coefficient settings, and even across different band pass noise shaping encoding algorithms. This is even true for delta-sigma modulators in moderate limit cycles as shown in to the right of Figure 2.

With constant switching losses, increasing the in-band power of an encoded signal causes the power output of the amplifier to increase until the amplifier approaches the limit of its constant wave (CW) efficiency. It is not possible to encode narrowband signals having a nonzero peak-to-average power ratio (PAPR) at anywhere near 100% in-band power without severe distortion. Systems encoding signals with high peak-to-average power ratio (PAPR) will be fundamentally limited to a lower maximum in-band power ratio than for systems encoding a signal with a lower PAPR. This is similar to

analog systems that need to be operated at back-off powers to prevent clipping high PAPR signals.

Unlike the other metrics discussed, in-band power ratio is not a useful measure for traditional analog transmitter, but is extremely useful in comparing different encoding algorithms. As the same switching amplifier can typically be driven with a variety of different encoding algorithms, such as delta-sigma or pulse width modulation, a figure of merit predicting the efficiency of an amplifier with different drive encodings can avoid unnecessary laboratory measurement.

In-band power was developed over the course of this work, and has also been developed in parallel by others working with digital amplifiers in [1]-[2]. The work in [1] refers to in-band power ratio with the term "coding efficiency."

4. Conclusion

Digital transmitters are distinct systems from the analog systems they replace. A new framework of metrics facilitates the comparison between the proposed digital transmitters and classical systems. A new metric, in-band power, was developed that predicts digital amplifier efficiency across different encoding algorithms.

5. References

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[2] T. Johnson, R. Sobot, and S. Stapleton, "Measurement of Bandpass Sigma-Delta Modulator Coding Efficiency and Pulse Transition Frequency for RF Class D Power Amplifier Applications," in *Electrical and Computer Engineering, 2006. CCECE '06. Canadian Conference on*, pp. 2314-2317, May 2006.

Chapter 3
ZigBee (802.15.4) Transmitter Demonstration

1. Introduction

A low-power digital transmitter design is presented highlighting the system integration and efficiency benefits brought by digital transmitter designs. A novel low-complexity quantization algorithm is introduced that can achieve efficient amplification while meeting spectral and accuracy specifications. The low-complexity algorithm saves power in the digital logic implementation allowing for low overall transmitter power dissipation.

2. ZigBee (802.15.4)

ZigBee addresses an important application space in the spectrum of wireless technologies by providing a low-cost, low-power, high-reliability, low-data-rate wireless communication standard. ZigBee with its MAC/PHY layer, as defined by IEEE 802.15.4 [1], has a large range of potential uses, extending from industrial control to home automation to consumer electronics to patient monitoring.

The major goals of a ZigBee transmitter design are to minimize cost, power dissipation, and size. A single-chip submicron CMOS solution is ideal to meet all of these goals. This work focuses on creating a CMOS ZigBee transmitter with state-of-the-art efficiency that can be entirely integrated into a modern CMOS process.

RF transmitter chains, combined with a power amplifier (PA), have long been realized by analog circuits, and often require fabrication in specialty device technologies.

With the advance of modern CMOS processes into multi-gigahertz clock frequencies, migrating these RF blocks into CMOS circuits has become feasible.

The transition to monolithic CMOS is not straightforward. Traditional analog designs suffer when directly translated into submicron CMOS circuitry. Major problems for transmitter design include: low voltage operation affecting analog headroom, output power, and area-hungry low-Q inductors.

Many of these issues can be addressed by focusing design on the strength of CMOS: digital circuitry. The goal of this work is to implement a transmitter entirely in digital circuitry, using a switching power amplifier as a one-bit power digital-to-analog converter, thereby pushing the digital-analog barrier as far out as possible.

3. Quantization Algorithm

3.1. Motivation

802.15.4 specifies a direct sequence spread spectrum (DSSS) with binary phase-shift keying (BPSK) utilizing a raised cosine pulse shaper. The signal has a time varying envelope passing though zero, with a peak-to-average (PAR) ratio of about 1.7 dB. This non-constant envelope modulation makes the use of high-efficiency nonlinear switching amplifiers difficult.

A popular method for driving switching amplifiers with non-constant-envelope signals [2]-[6] is to quantize an upconverted digital RF signal using a quantization algorithm (usually a band-pass delta-sigma modulator) to obtain a one-bit over-sampled sequence. This one-bit signal includes components of the original signal and also

modulator-added quantization noise, which is typically shaped out of the frequency band of interest.

A major side benefit of these digital drive systems is the elimination of the digital-to-analog converter (DAC). The power saved by DAC elimination can offset the addition of thousands of digital gates in modern CMOS. Also DAC designs in CMOS do not readily migrate across different processes, but digital algorithms can easily be resynthesized into different digital processes.

3.2. Noise Spreading Algorithm

Noise spreading is a coding method designed for simplicity, low power, and high in-band power ratio. The algorithm directly quantizes the desired value with an added dither. A block diagram of the algorithm is shown in Figure 1.

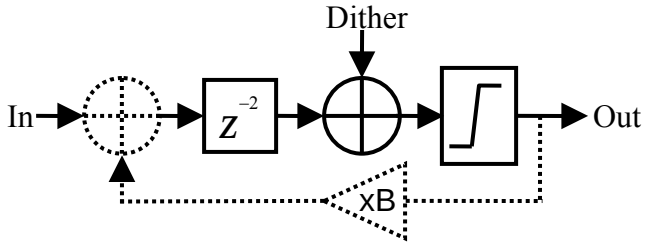

Figure 1: Block diagram of the direct quantization algorithm with optional power control feedback show in dashed lines.

The dither decorrelates the quantization noise from the input signal with no spectral shaping. The algorithm spreads the noise evenly across the band. In our implementation, the dither signal has a triangular probability density function (PDF), and is scaled to have its maximum swing match the input signal. The signal is generated by a

pair of linear feedback shift registers (LFSR), producing uniformly distributed pseudorandom numbers which are added together to create a triangular PDF sequence.

Algorithmic simplicity is important for total transmitter efficiency, as the hardware implementing these functions runs at a high clock rate.

3.3. In-Band Power Ratio

Digital power amplifier efficiency is affected by both design details of the amplifier and the in-band power ratio [3]-[5] of the quantization algorithm. The in-band power ratio is defined as the ratio of the desired in-band signal power to the power of the entire pulse train. For a given encoding algorithm, there will be a tradeoff between in-band power ratio, adjacent channel power ratio (ACPR), and error vector magnitude (EVM) [4]. As will be shown later in the chapter, the presented algorithm can achieve in-band power ratios in the eighty percent range with an EVM of less than five percent.

3.4. Algorithmic Power Control

With minimal additions, shown in Figure 1 as dotted lines, the noise spreading algorithm can be expanded to contain algorithmic power control. Algorithmic power control allows a digital radio to lower the output power of a transmitter with no changes in supply voltage, as the digital system cannot otherwise implement a variable gain amplifier. Eliminating variable amplifier supply simplifies system design by eliminating costly DC/DC converters. In the case presented here, algorithmic power control is can be used to meet power control recommendations contained in the 802.15.4 specifications [1] with a fixed voltage supply to the amplifier.

To achieve power reduction, the loop decreases the in-band power ratio by adding more quantization noise, similar to an analog amplifier running at back-off, causing the efficiency to decrease. This added noise will be shaped spectrally out-of-band due to the noise transfer function created by the added delay path. This effect increases as the back-off is increased, as a pair of poles in the noise transfer function move along the real axis, away from the origin as the B constant is increased. This can be seen in the noise transfer function (NTF) of the modulator:

$$NTF(z) = \frac{1}{1 - Bz^{-2}} \tag{1}$$

The transmitted signal is also slightly suppressed at high B values, as can be seen by the signal transfer function (STF) of the noise spreading modulator.

$$STF(z) = \frac{z^{-2}}{1 - Bz^{-2}} \tag{2}$$

High B values uncover the two zeros located at the origin, shaping the noise both towards zero frequency and the Nyquist frequency. Graphically, this is shown in Figures 2 and 3:

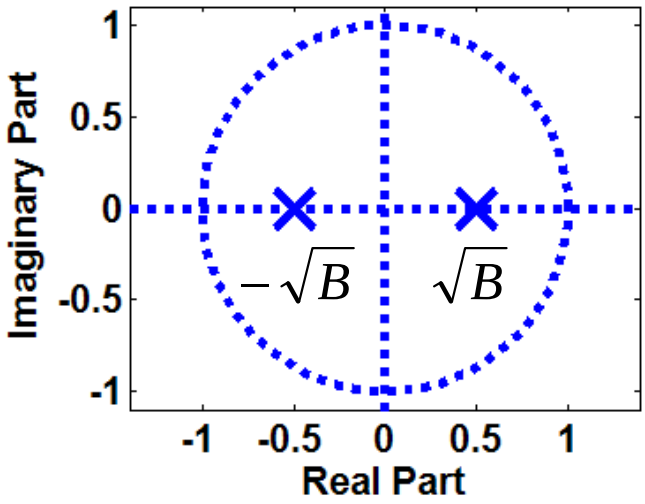

Figure 2: Z-plane plot of noise transfer function of the noise spreading algorithm

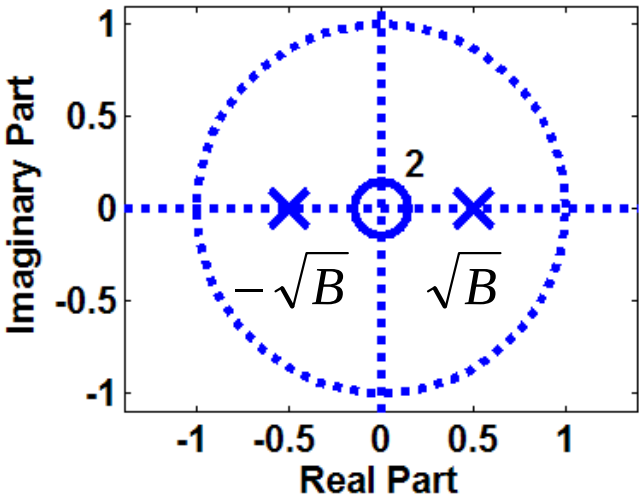

Figure 3: Z-plane plot of signal transfer function of the noise spreading algorithm.

3.5. Power Consumption

Power consumption for the noise spreading algorithm is expected to be much lower compared to an equivalent delta-sigma modulator. Power savings are due to the minimalist design, requiring fewer and simpler digital blocks. Periodicity and the resulting spurious tones are avoided, even when using a narrow word-length data path.

Also, the feedback path passes though the quantizer, and thus the feedback value is bounded. Unlike delta-sigma systems, overflows can be avoided by design, and the adders do not require additional logic to saturate on overflow. The ability of the noise spreading modulator to operate at very narrow word lengths reduces the static power dissipation of the digital logic required to implement the DSP functions.

The power reduction realized by moving to a simpler algorithm than delta-sigma has an effect on the system efficiency, especially for a low power transmitter. Delta-sigma modulators have many adders and possibly multipliers, all having word lengths in excess of 8-bits. Eliminating these gates running at very high speed, reduces system dissipation by tens of milliwatts and leads to large increases in system efficiency for a several-milliwatt class transmitter. Power consumption will be analyzed in detail for the specific implementation used in this work in section 4.4.

4. The 802.15.4 / Zigbee Transmitter

4.1. Transmitter Architecture

The overall transmitter architecture is shown in Figure 4. Similar to the quantization algorithm, the frequency plan is designed for simplicity and low power. All of the complex filtering is done at baseband frequencies. High-speed upsampling operations are implemented as zero-order-hold functions, which are nearly computation-free. The final signal is represented at the Nyquist frequency, keeping clock rates as low as possible. For high frequency transmitters, it is possible to further upsample the one-bit output of the modulator, saving logic power at expense of the noise-spreading properties.

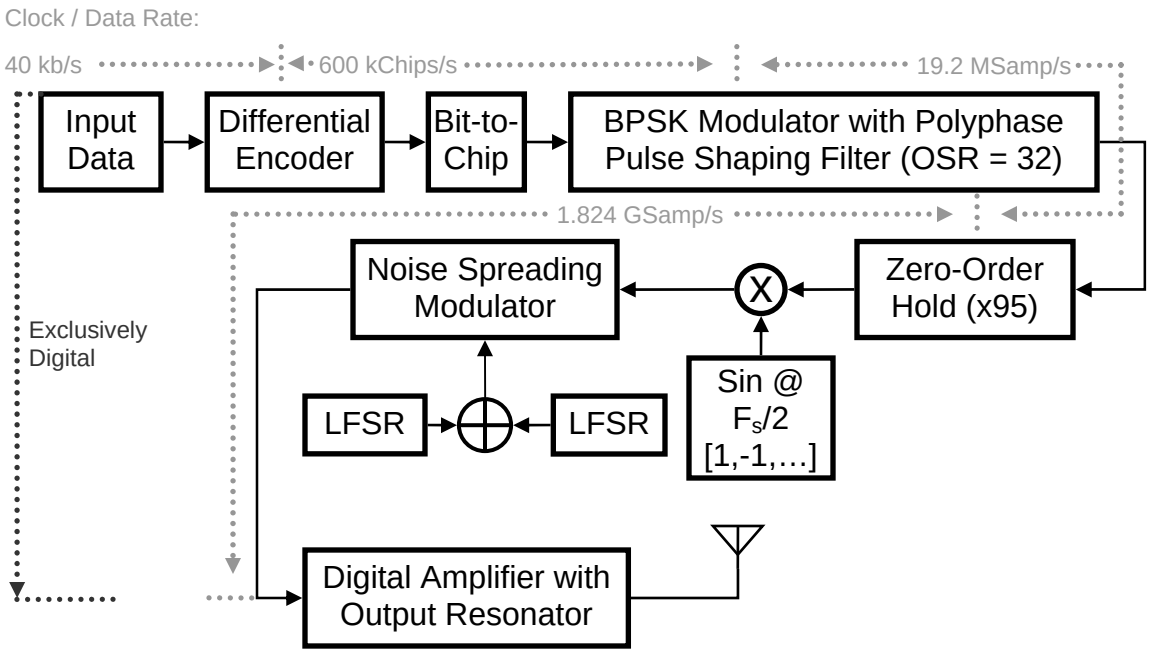

Figure 4: Block diagram of proposed transmitter architecture.

Simulations indicate a five-bit word length is sufficient to satisfy the 802.15.4 transmit relative spectral mask of -20 dBc and the absolute transmit mask of -20 dBm [1] for transmit powers less than a watt.

4.2. Simulation Setup

The ZigBee transmitter system has been simulated in both MATLAB and C code. The ZigBee PHY was modeled in MATLAB up to a digital IF signal. The IF signal was then passed on to an algorithm written in C code, modeling the noise spreading modulator. The resulting output was then brought back into MATLAB for analysis.

Analysis included power spectral density with relative and absolute spectral masks, in-band power ratio, and EVM. The first two simulations are straightforward but the EVM calculation has some computationally intensive algorithms that are made

greatly more efficient by using a custom algorithm that is a variation of the Newton-Raphson successive approximation.

The PHY specification defines EVM as [1]:

$$EVM \equiv \sqrt{\frac{\frac{1}{N}\sum_{j=1}^{N}(\delta I_j^2 + \delta Q_j^2)}{S^2}} \tag{3}$$

S is the magnitude of the ideal constellation point and (δI_j, δQ_j) is the error vector. The simulation includes a down converter and receiver to recover the signal in order to compute the error vector magnitude. Unfortunately the process of down converting the signal causes delays, and the timing needs to be realigned to compute an accurate error. Realigning the signal and normalizing the amplitude for the lowest possible magnitude typically involves a very computationally intensive two-dimensional cross-correlation or a linear search.

Newton's method of successive approximation is an iterative method for approximating roots of real-valued functions. Assuming the misalignment is less than a chip, the alignment is very similar to finding the local minima of a polynomial with imaginary roots.

Starting with Newton's method finding the roots of the error vector magnitude as a function an offset of X samples f(X_n):

$$X_{n+1} = X_n - \frac{f(X_n) \times (X_n - X_{n-1})}{f(X_n) - f(X_{n-1})} \tag{4}$$

Using an unmodified Newton's method formula alone will result in the approximation hovering around the local minima. Modifying Newton's method slightly, to subtract the lowest value found thus far, causes the approximation to converge rapidly.

$$X_{n+1} = X_n - \frac{[f(X_n) - \min(f(X))] \times (X_n - X_{n-1})}{f(X_n) - f(X_{n-1})} \quad (5)$$

Convergence of this algorithm causes a divide-by-zero condition, so the algorithm can be halted on the divide-by-zero, or when two successive approximations are equal. For reasonable initial values for the derivative, the algorithm converges to the accuracy of a double precision floating point number in four iterations.

4.3. Simulation Results

Simulations show that the noise spreading transmitter meets all of the spectral mask requirements at full algorithmic power, as well as the near spectral requirements through a 15 dB algorithmic back-off. Figure 5 shows the near-band spectral performance for the transmitter running at full power:

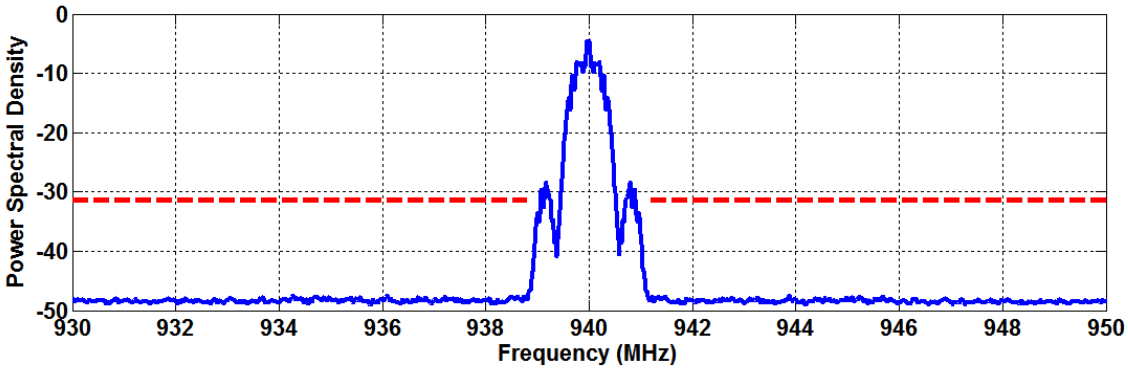

Figure 5: Simulated PSD of the ZigBee signal. The spectral mask is shown in dashed red.

For the full power case, the relative spectral mask is met through the band, including past the Nyquist frequency. In a high algorithmic back-off case, the spectral mask is more difficult to meet due to the increased amount of quantization noise. A spectral simulation of high back-off results in the following spectra:

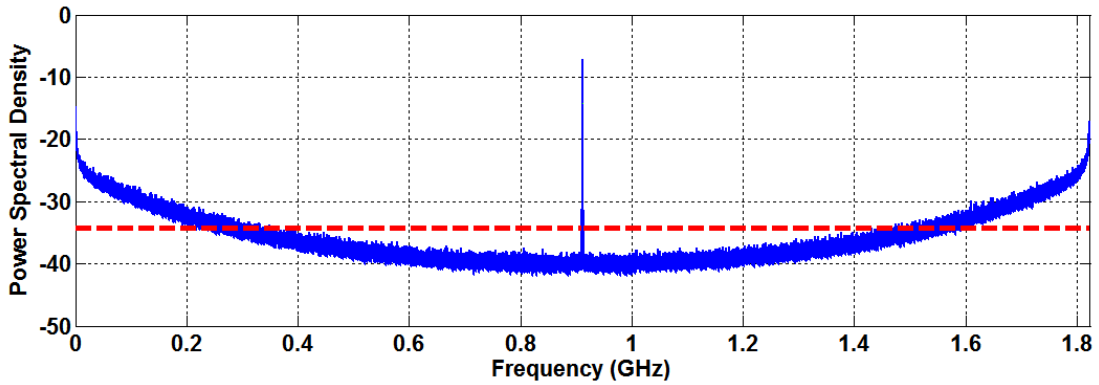

Figure 6: Simulated wideband PSD of noise spreading algorithm in high algorithmic power back-off. The spectral mask is shown in dashed red.

The relative spectral mask requirements are violated at the edge of the band in the high back off case, but this is not expected to be the case with an amplifier containing an output resonator, as the output resonator should present an open circuit to the amplifier at frequencies far from its resonance.

The error vector magnitude of the transmitter was simulated though the range of the algorithmic power control, which is shown in Figure 7:

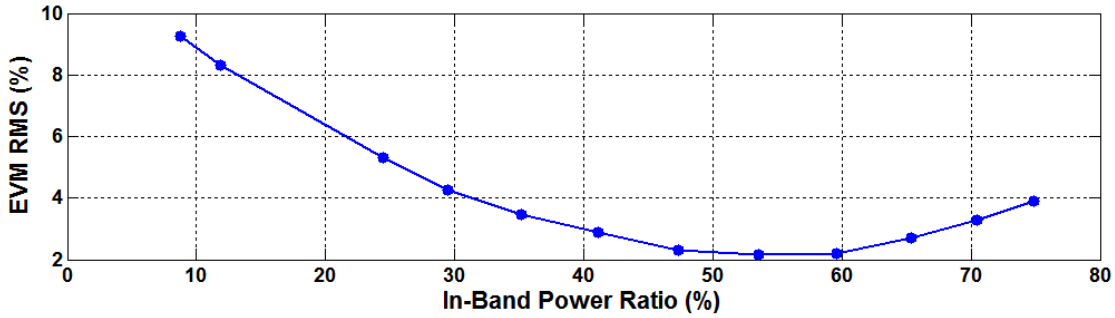

Figure 7: Simulated EVM vs. algorithmic power back-off.

The simulation shows the algorithm is comfortably lower than the 35% maximum given by the specification.

4.4. Transmitter Architecture Power Dissipation Simulation

The power dissipation expected from the digital logic implementing the noise spreading modulator, starting at the baseband and ending at the two one-bit amplifier drive signals, is simulated. As the gate library provided could not meet the clock timing at the sample rate, the circuit was parallelized by a factor of two. The functionality described in Figure 1, sans power control feedback, was implemented in VHDL for logic synthesis and power simulation. The block diagram of the functionality implemented in VHDL is shown below.

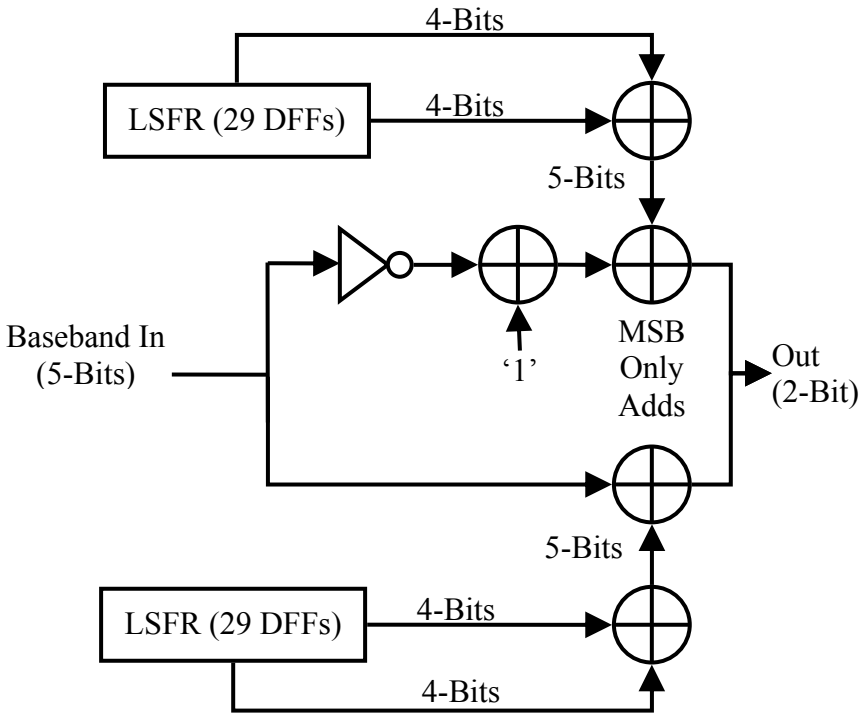

Figure 8: Block diagram of the digital functionality implemented in VHDL.

Dither is implemented by a maximal one-to-many Galois linear feedback shift register (LSRF) with a word length of 29-bits. The word length was chosen to minimize the number of taps and corresponding XOR gates, and to limit the spurious tones caused

by the sequence repeating. Two four-bit sequences from the LSFR are added together to form a pseudo-random number with a triangular probability density function. The VHDL code written to implement the above functionality is provided in appendixes A and B.

The VHDL system was then synthesized and optimized with Synopsis Design Compiler using the A18 ASIC, release d16, gate libraries provided by Jazz Semiconductor. This digital gate library is targeted to the same 0.18 um CMOS process that the amplifier is fabricated in. The synthesized design is shown below in Figure 9, below. The LSFR and final adders are shown as boxes to simplify the fairly complex schematic.

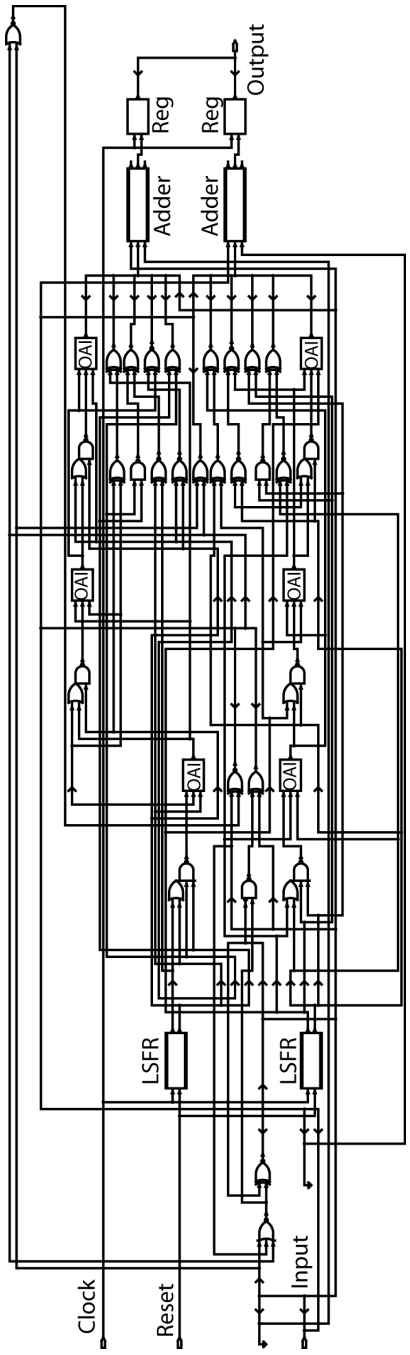

Figure 9: Synthesized schematic of noise spreading modulator.

The power dissipation simulation results in between 4.4 mW and 5.3 mW of power necessary to run two copies of the digital logic at 915 MHz with a supply voltage of 1.8 V, with the higher dissipation number having excess timing slack.

Since the design with a clock rate at half the sampling rate has insufficient timing slack to be run at the lower supply voltages of around one volt, a one quarter sampling rate design was also synthesized. This design could successfully meet timing down to the lower supply voltages. The power dissipation estimate of the one-quarter-rate noise spreading modulator was 4.45 mW.

All of the subsequent system efficiency calculations assume 6 mW of power dissipation. This includes the above simulated logic, clock tree overhead, and any multiplexer or signal retiming necessary before amplification. These power consumption numbers are dramatically reduced by employing a more modern CMOS processing technology expected in a highly-integrated digital transmitter design. As will be presented, even with the higher power consumption overhead, the digital transmitter system still exceeds the system efficiency of a comparable analog transmitter.

4.5. The Voltage-Mode Class-D CMOS Amplifier

To verify experimentally the waveform simulations and efficiency predictions of this chapter, and of several later chapters, measurements were made on an experimental power amplifier constructed from the active devices first designed in [4]. A new PCB was designed along with a lumped-element matching network. The experimental voltage mode class-D (VMCD) amplifier was constructed in a 2 V maximum, 0.18 μm CMOS process. A pair of driver amplifiers was used as a first stage. One of the driver amplifiers drives the PMOS of the final stage amplifier, and the second driver drives the NMOS of the final stage. Figure 10 shows the complete schematic of the amplifier, and Figure 11 shows the CMOS die implementing the amplifier. Both drivers have

asymmetrical pull-up/pull-down devices to minimize the overlap of the on-times of the two devices in the VMCD. Minimizing the turn-on overlap reduces the shoot-through current of the amplifier leading to higher efficiency [4].

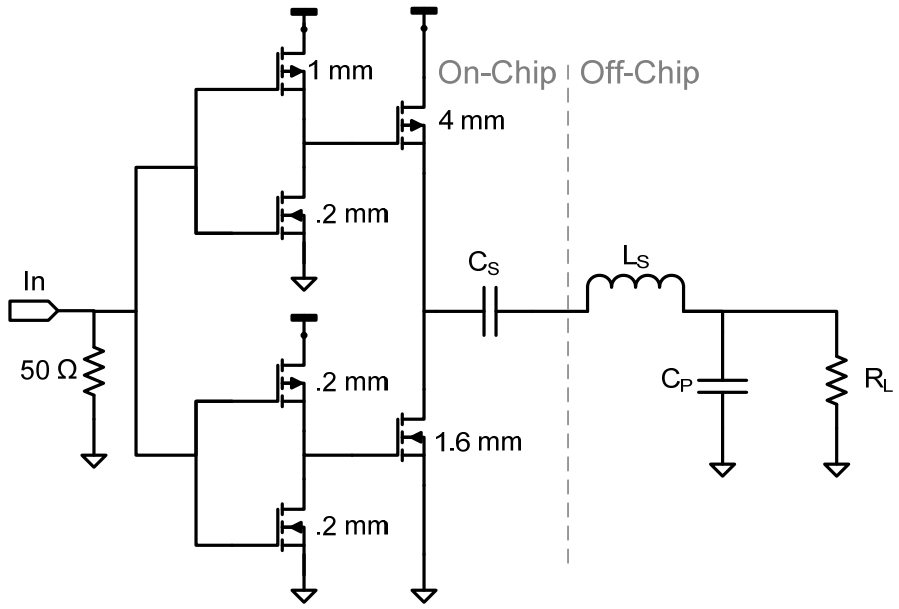

Figure 10: Schematic of the CMOS VMCD amplifier. Supply decoupling capacitors omitted. All transistor lengths are the 0.18 µm minimum.

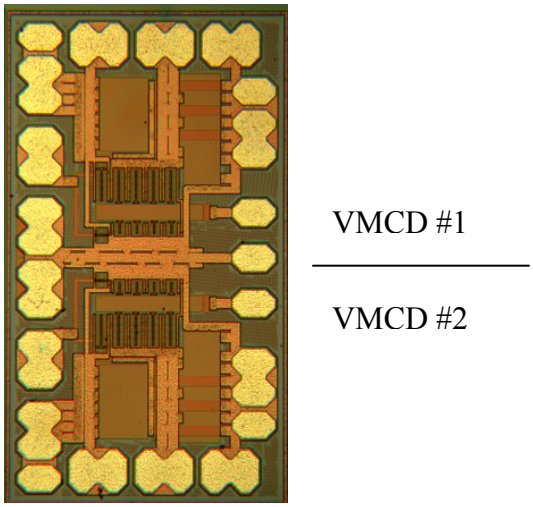

Figure 11: Die photograph of the dual VMCD amplifier chip.

The input to the pair of driver amplifiers is terminated in a 50 Ω resistive match to minimize reflections in the input broadband digital signal, and to ensure that the measured output power is solely from the CMOS amplifier. In the particular chip used, two VMCD amplifiers and corresponding drivers were included on each die. Only the top amplifier was used in the following experiments.

Two off-chip components were used: an inductor comprised of a bond-wire in series with two turns of wire, and a surface mount capacitor. The inductor serves both as part of the resonator and as part of the L match to the output at 50 Ω. The capacitor is solely for the purpose of matching to 50 Ω.

5. Measurements

5.1. Measurement Setup

The system model of the transmitter was used to calculate a 12-Mbit digital transmit pattern, which was subsequently loaded into an Agilent 81134A pulse pattern generator. The pulse pattern was then played back through the prototype amplifier. An Agilent N9020A MXA spectrum analyzer was used for both channel power and spectral measurements. No filters were used between the amplifier and the spectrum analyzer.

5.2. VMCD Square Wave Measurement Results

To verify the functionality of the VMCD amplifier and for tuning, square waves were used in the initial testing. The efficiency and fundamental RF power vs. DC supply voltage is shown in Figure 12:

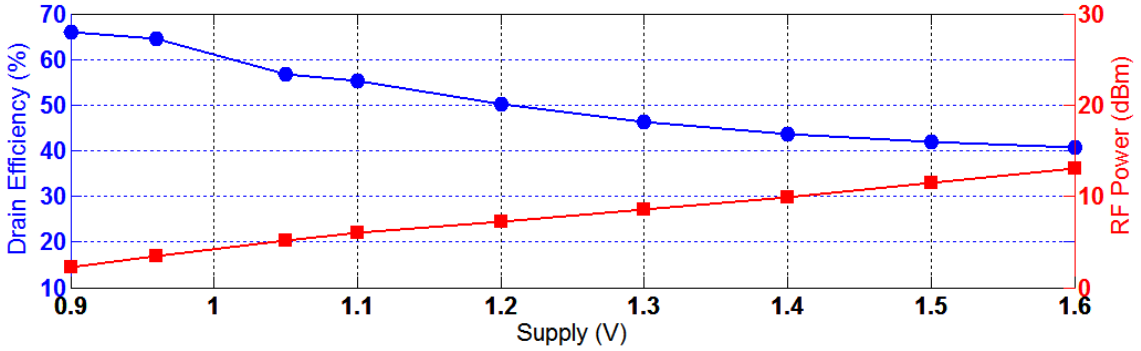

Figure 12: Measured square wave drain efficiency (blue with circle markers) and RF Power (red with square markers) vs. supply with a 935 MHz square wave drive signal.

To verify the tuning of the output resonator, the supply voltage was fixed and the square wave frequency was varied. The efficiency and output power are shown in Figure 13:

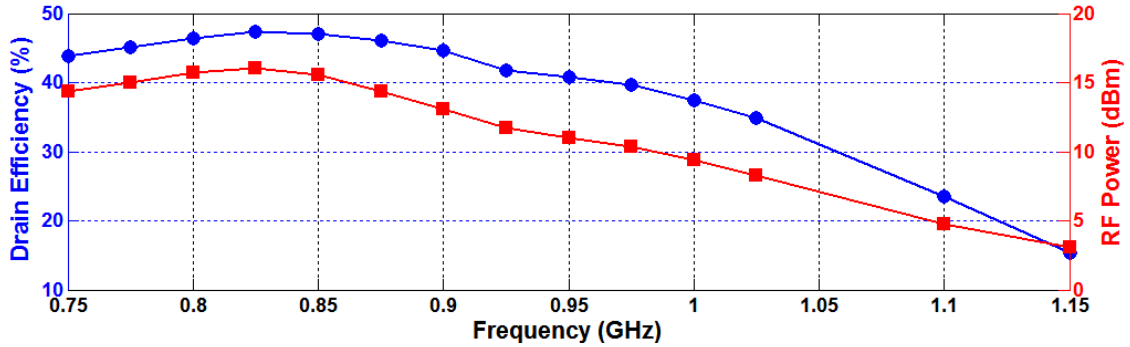

Figure 13: Measured square wave drain efficiency (blue with circle markers) and RF power (red with square markers) vs. Frequency with a 1.5 V supply.

5.3. ZigBee Power Measurement Results

Figure 14 shows the power output of the VMCD with different supply voltages. Down to a 0.9V supply, the amplifier provides more than a milliwatt of RF power, the standard power for ZigBee systems. The power measurements were performed by the channel power integration routine provided by the spectrum analyzer. This is particularly

important for digital amplifier systems because of the relatively large amounts of out-of-band power compared to traditional linear amplifiers.

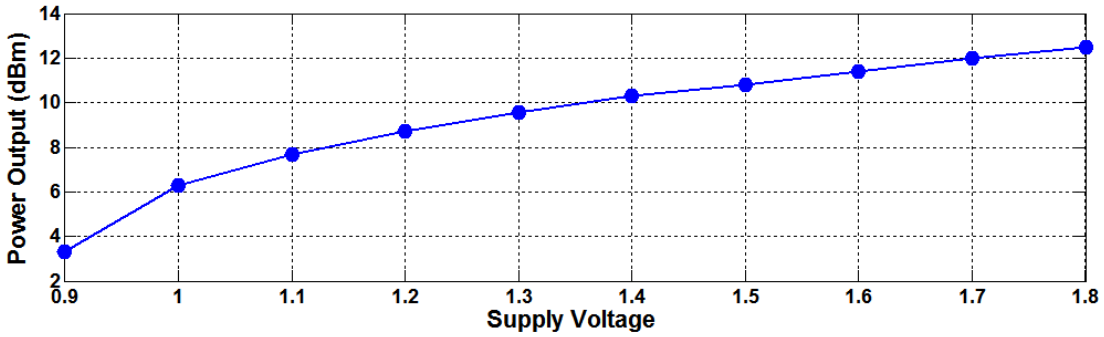

Figure 14: Measured 802.15.4 / ZigBee power output power vs. supply.

The top line in Figure 15 shows the drain efficiency of the final amplifier stage. Power-added efficiency is not shown, as it is difficult to define for a digital amplifier; the voltage of the drive and output signal are the same. Cabling losses of 0.3 dB were accounted for in the efficiency calculations.

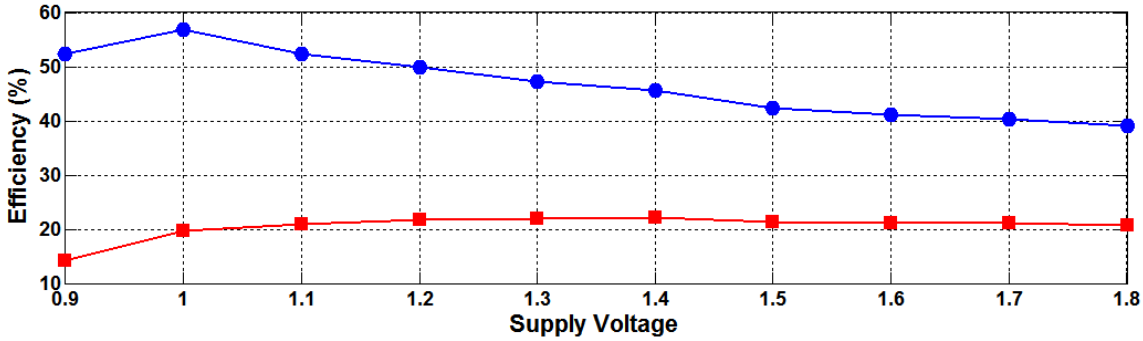

Figure 15: Measured 802.15.4 / ZigBee drain efficiency (top with circle markers) and system efficiency with supply (bottom with square markers).

The bottom line in Figure 15 shows system efficiency, a hybrid between simulated and measured data. System efficiency sums all of the power used, including that of the driving stages and that of the estimate of the power dissipation of the digital logic necessary to implement the necessary DSP functions in the block diagram,

presented in section 4.4. Another milliwatt was allocated for the fixed frequency reference, bringing to total estimated overhead of this transmitter to 6 mW. The estimated power dissipation is significantly smaller than the measured power amplifier dissipation numbers at the higher supply voltages where the system would be expected to operate. For the system efficiency numbers presented here, the sensitivity to inaccuracies in the simulated power dissipation of the digital logic is small.

The amplifier efficiency was also measured for algorithmic back-off, shown in the following plot:

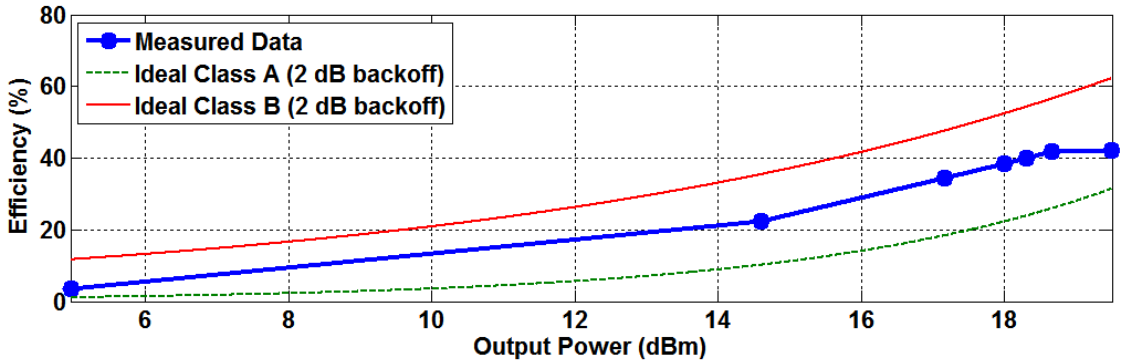

Figure 16: Measured ZigBee drain efficiency with algorithmic power back-off compared to two ideal efficiencies for classical analog amplifiers.

The curve is very similar to a classical amplifier in back-off. The amplifier efficiency degrades as the in-band power ratio is reduced. Scaling the voltage to lower the RF transmitter power is a more efficient method, but adds the complexity of conversion circuitry.

5.4. Spectral Measurement Results

The spectrum of the output was also measured and results are displayed in Figures 17 and 18. The output spectrum easily meets both the absolute and relative PSD masks

near the transmit band [1]. In Figure 17, only the relative mask is shown because the relative mask is the more difficult standard to meet at transmit powers lower than about 100 mW.

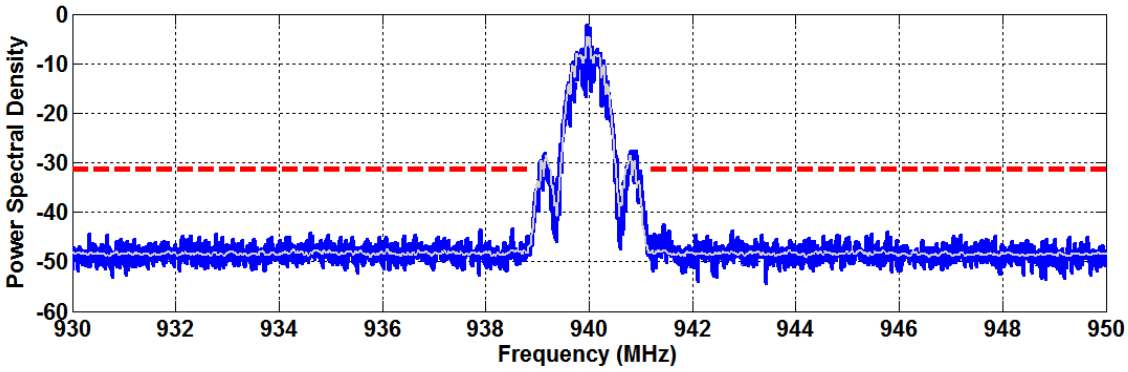

Figure 17: In-band measured output spectrum at 1.5 V supply with 802.15.4 relative PSD mask (RBW = 10 kHz). Shown with the simulated spectrum overlaid in light gray.

A full spectral sweep of the output is shown in Figure 18. The FCC spurious emission mask is also drawn. Due to the presence of harmonic power and low frequency quantization noise, the system does not meet the emission limits at the output directly from the amplifier.

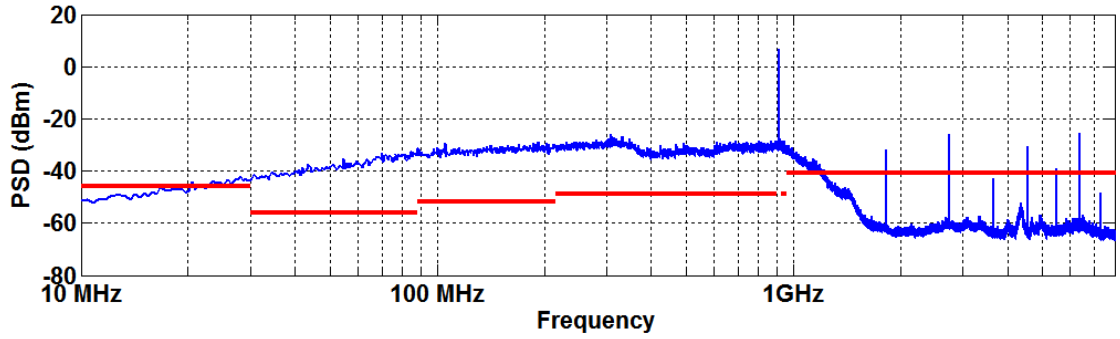

Figure 18: Full measured output spectrum at 1.5V supply with FCC spurious emission limits. (RBW = 100 kHz).

To show that these limits can be met by the addition of a filter or an antenna that attenuates signals out of band, an elliptical filter frequency transfer function was applied to the spectrum in Figure 18. This is shown in Figure 19, where the transfer function of a fourth order band-pass filter was added to the spectra of Figure 18 by multiplying the transfer function of the elliptical band-pass filter with a 912 MHz center frequency, an 18 MHz 3 dB bandwidth, and a 37 dB out-of-band rejection.

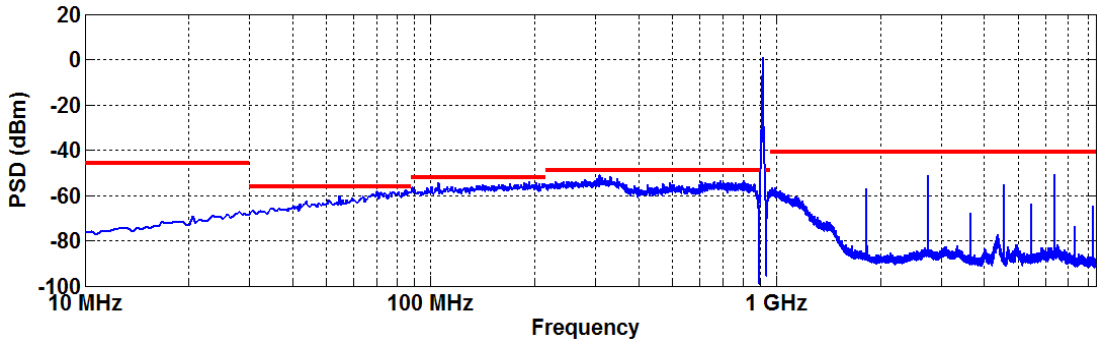

Figure 19: Above measured spectrum with modeled second order elliptic output filter applied.

The spurious mask is an absolute limit, so the transmitter can also be brought to compliance by reducing the output power.

6. Comparison with Traditional Transmitters

6.1. System Efficiency

Table 1 compares system efficiencies of this work with another experimental system and two commercial parts:

Table 1: Comparison of efficiencies

Reference:	RF Power:	System Efficiency:
This Work[1]	10.8 mW	22%
[7] [2]	10 mW	13%
[8][2]	1.4 mW	4%
[9][3]	1 mW	1.5%

Note 1: Includes digital logic estimate.
Note 2: Includes VCO / PLL.
Note 3: Includes VCO / PLL and some MAC functionality.

Comparisons are made difficult by the fact that RF power is significantly lower in references [8] and [9], and thus transmitter efficiency is more affected by the power-dissipation overhead of the transmitter upconversion chain. The power level in [7] closely matches that of this work. For a more detailed comparison, every relevant specification provided in [7] is compared with this work in table 2 below.

Table 2: Detailed comparison of this work with [7].

	This Work	[7]
RF Power Output	10.8 dBm	10 dBm
Frequency	940 MHz	914 MHz
RF Supply Voltage	1.5 V	3 V
Supply Current	34.4 mA	20.3 mA
Efficiency sans VCO	22%	16%
2nd Harmonic	-28 dBm	-23 dBm
3rd Harmonic	- 22 dBm	-24 dBm
Spurious Emissions (Except Harmonics)		
30 – 1000 MHz	-30 dBm	-36 dBm
2 – 12.75 GHz	-60 dBm	-30 dBm

6.2. External Components

The following block diagram compares the off-chip components required by both this work and [7]:

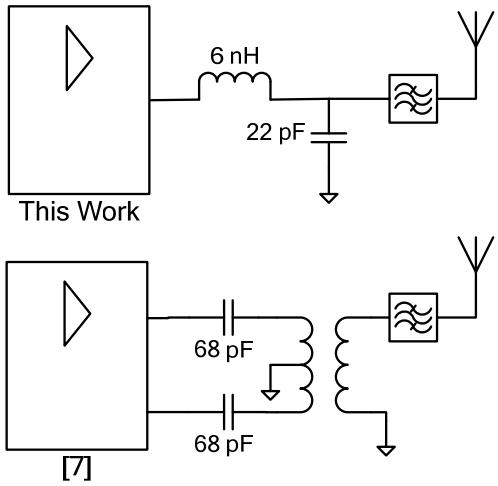

Figure 20: Schematic of external RF components required by proposed transmitter (top) versus [7] (bottom).

Both systems require a band-pass filter to meet FCC spurious requirements at higher power levels. The system in [7] requires a balun (that is typically integrated with the filter) and two DC blocking capacitors. This work requires an inductor (which can be implemented by a bond wire) and a shunt capacitor for matching. The chip in [7] requires two power supplies one at 3 V and another at 1.8 V, making implementation more difficult in modern, low voltage CMOS.

7. Conclusion

802.15.4/ZigBee is an excellent application for digital transmitter design, as a highly integrated design is key to reducing unit cost, a critical issue for ZigBee radios. Also, unlike many CMOS designs, this transmitter will scale very well with digital technology generations. Power dissipation of the DSP and driver amplifiers will markedly drop. RF output power output is sufficient down to a 0.9V supply, meaning a direct scaling to submicron CMOS is possible. CV^2 scaling from 0.18 μm to 95 nM CMOS technology node suggests that a doubling of transmitter efficiency is plausible.

8. Acknowledgments

Some of the material presented in chapter 3 is previously published in [10]. The author of this dissertation was the primary investigator and primary author for [10]. Tsai-P Hung designed the CMOS chip used in the VMCD amplifier during the course of [4]. The author would like to thank him for the use of extra chips.

9. Appendix A: VHDL Source Code

9.1. Top-level VHDL Source Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity zigmod is
    Port ( chip_in : in std_logic_vector(4 downto 0);
           clock   : in std_logic;
           reset   : in std_logic;
           outv    : out std_logic_vector(1 downto 0) );
end zigmod;

architecture Behavioral of zigmod is

 signal rnd1, rnd2, rnd3, rnd4      :  std_logic_vector(3 downto 0);

 component lfsr
    Port (
      clock     : std_logic;
      reset     : std_logic;
      data_out1 : out std_logic_vector(3 downto 0);
      data_out2 : out std_logic_vector(3 downto 0) );
  end component;

begin
  LFSR_1 : lfsr
    port map (clock  => clock,
              reset  => reset,
              data_out1 => rnd1,
              data_out2 => rnd2 );

  LFSR_2 : lfsr
    port map (clock  => clock,
              reset  => reset,
              data_out1 => rnd3,
              data_out2 => rnd4 );
```

```
    process (clock)
     variable chip_mod          :  std_logic_vector(4 downto 0);
     variable pre_out           :  std_logic_vector(5 downto 0);
     variable rnd               :  std_logic_vector(4 downto 0);
    begin
    if rising_edge(clock) then
        chip_mod := unsigned(not chip_in) + 1;
        rnd := unsigned('0' & rnd1) + unsigned('0' & rnd2);
        pre_out := unsigned('0' & rnd) + unsigned('0' & chip_mod);
        outv(0) <= pre_out(5);
     end if;
    end process;

    process (clock)
     variable chip_mod          :  std_logic_vector(4 downto 0);
     variable pre_out           :  std_logic_vector(5 downto 0);
     variable rnd               :  std_logic_vector(4 downto 0);
    begin
    if rising_edge(clock) then
        chip_mod := chip_in;
        rnd := unsigned('0' & rnd3) + unsigned('0' & rnd4);
        pre_out := unsigned('0' & rnd) + unsigned('0' & chip_mod);
        outv(1) <= pre_out(5);
     end if;
    end process;
end Behavioral;
```

9.2. LFSR VHDL Source Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity lfsr is
    Port (
      clock     : std_logic;
      reset     : std_logic;
      data_out1 : out std_logic_vector(3 downto 0);
      data_out2 : out std_logic_vector(3 downto 0) );
end lfsr;

architecture Behavioral of lfsr is

  signal lfsr_reg : std_logic_vector(28 downto 0);

begin

process (clock)
  begin
    if rising_edge(clock) then
      if reset = '0' then
        lfsr_reg <= lfsr_reg(27 downto 0) & '1';
      else
        lfsr_reg <= lfsr_reg(27 downto 0) & (lfsr_reg(28) xor
lfsr_reg(27));
```

```
      end if;
      data_out1 <= lfsr_reg(14) & lfsr_reg(21) & lfsr_reg(5) &
lfsr_reg(3);
      data_out2 <= lfsr_reg(25) & lfsr_reg(10) & lfsr_reg(19) &
lfsr_reg(19);
    end if;
  end process;
end Behavioral;
```

10. References

[1] IEEE Std. 802.15.4™-2003.

[2] A. Jayaraman, et al., "Linear high-efficiency microwave power amplifiers using bandpass delta sigma modulators," in *IEEE Microwave Guided Wave Letters*, vol. 8, iss. 3, pp. 121–123, March 1998.

[3] T. Johnson and S. Stapleton, "RF Class-D Amplification with Bandpass Sigma–Delta Modulator Drive Signals," in *IEEE Transactions on Circuits and Systems,* vol. 52 iss. 12, pp. 2507-2520 December 2006.

[4] T. Hung, J. Rode, L. Larson, P. Asbeck, "Design of H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters", in *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, iss. 12, pp. 2845–2855 December 2007.

[5] M. Iwamoto, et al., "Bandpass delta-sigma class-S amplifier," in *IEEE Electronics Letters*, vol. 36, iss. 12, pp. 1010-1012, June 2000.

[6] J. Sommarek, et al., "Comparison of different class-D power amplifier topologies for 1-bit band-pass delta-sigma D/A," in *2004 Proc. Of Norchip Conf.*, pp. 8-9, November 2004.

[7] ATMEL "AVR Low Power 700/800/900 MHz Transceiver for IEEE 802.15.2-2006, IEEE 802.15.4c-2009, Zigbee, 6LoWPAN, and ISM Applications" Rev. 8168C-MCU Wireless-02/10 February 2010.

[8] N. Oh, S. Lee and J. Ko, "A CMOS 868/915 MHz Direct Conversion ZigBee Single-Chip Radio," in *IEEE Communications Magazine*, December 2005.

[9] ZMD "ZMD44102 Data Sheet and User Manual" Version 1.1 August 2006.

[10] J. Rode, T. P. Hung, and P. M. Asbeck "An All-Digital CMOS 915 MHz ISM Band 802.15.4 / ZigBee Transmitter with a Noise Spreading Direct Quantization Algorithm" in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2008.

Chapter 4

CDMA / QPSK Delta-Sigma Digital Transmitter Demonstration

1. Introduction

The goal of this chapter is to present work on the feasibility of a delta-sigma driven cellular-handset-class digital transmitter. Improvements and design tradeoffs in all aspects of the digital transmitter are explored. The chapter begins with a description of the overall envisioned digital transmitter system. Simulations are presented, detailing the performance of the delta-sigma based transmitter with emphasis on both RF signal properties and on the digital logic required to implement the delta-sigma modulator. New techniques are introduced to achieve delta-sigma noise shaping with the lowest possible hardware complexity and power dissipation. Delta-sigma modulator noise transfer function (NTF) designs are simulated and measured. These NTF designs reduce the quantization noise produced in the receive band, a necessarily quiet band for frequency division full-duplex communication. Measurements from a digital transmitter experimental setup are presented, highlighting the efficiency benefits of digital transmitter designs. Lastly, wide-band spectral degradation from amplification of the aperiodic delta-sigma signal is quantified.

2. CDMA / QPSK

A code division multiple access (CDMA) system using quadrature phase-shift keying (QPSK) was chosen because it is representative of the difficulties encountered in

designing a switching amplifier based system to meet system requirements of modern wireless systems. Some of the exacting standards are very difficult to meet with a highly integrated digital transmitter design. The major obstacles for a cellular digital transmitter that are discussed in this chapter include: 1) RF output power levels not easily achievable with the supply voltages of digital CMOS processes. 2) Strict adjacent channel power ratio (ACPR) requirements and the need to keep the receive band extremely quiet to avoid self-jamming in full duplex. (Both problems are exacerbated by the presence of delta-sigma quantization noise.) 3) Wide RF output power dynamic range requirements demanded by power control. 4) An efficient transmitter chain, despite having a saturated power amplifier (and often having zero voltage gain).

3. System Description

Figure 1 illustrates a block diagram of the proposed all-digital transmitter:

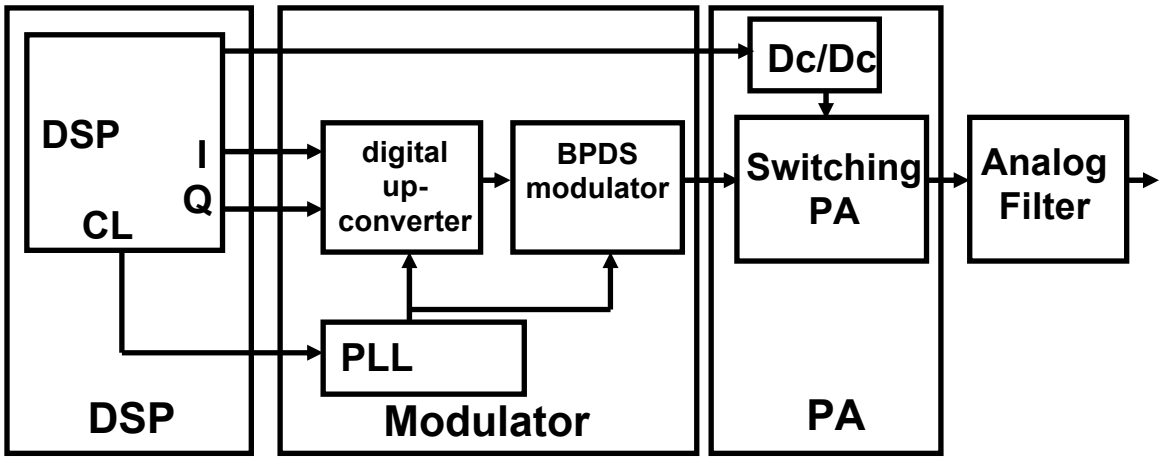

Figure 1: System block diagram for the all-digital transmitter.

3.1. Baseband

The signal used in the following simulations is an offset QPSK signal that closely approximates the IS-95 CDMA uplink waveform. The baseband I/Q signal is generated from a standard pulse shaping finite impulse response (FIR) filter fed by random chips, using conventional discrete time digital signals with large word length. This baseband I/Q signal is similar to that of other standard transmitters, except that the baseband sampling frequency is chosen to be higher than typically used. A higher baseband sampling frequency is used to keep the signal images resulting from the subsequent unfiltered zero-order hold (ZOH) upsampling operations from falling in undesired locations. The representative spectrum of the baseband signal is shown in Figure 2:

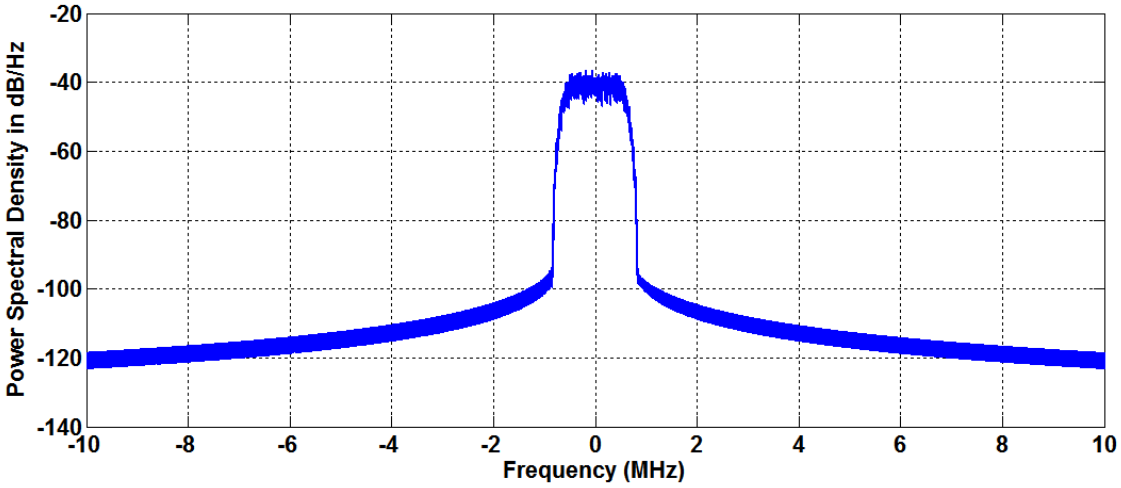

Figure 2: Spectrum of complex baseband signal comprised of random QPSK chips filtered with a raised cosign filter. The signal chip rate and bandwidth are 1.25 MHz and the sampling rate is 80 MHz.

3.2. Upsampling

ZOH upsampling operations are chosen because they are very easy to implement, and are much more power and gate area efficient than the more traditional zero-stuffing

followed by a FIR filter upsample operation. The major disadvantage of unfiltered ZOH upsampling is that the signal aliases are only lightly attenuated by a sinc function, rather than a FIR filter. For a narrowband signal, which is common in communication signals, the images fall in the local maxima of the sinc, resulting in relatively small image attenuation. Fortunately, this signal subsequently passes through a delta-sigma modulator that adds quantization noise to the signal. This quantization noise is shaped by a band-pass noise transfer function (NTF) of the delta-sigma modulator. In order for the signal images generated from an unfiltered ZOH upsample operation not to affect the output spectrum, the images must fall at or below the power levels of the quantization noise.

For example, if the final RF spectrum shows that images from the second upsampling to RF are still present in the delta-sigma modulated signal, the baseband sampling rate may be set at too low a value. The spectrum of Figure 4 (in the next section) shows such vestigial images. The images can easily be reduced by increasing the baseband sampling rate, and commensurately decreasing the ZOH upsampling factor. This change pushes the signal images further out of band. At some point the images will become lost in the quantization noise subsequently generated by the delta-sigma modulator.

3.3. Frequency Translation

The representative final sampling frequency used here is 3.2 GHz, chosen to correspond to a RF frequency of 800 MHz. The signal is then modulated in quadrature, using the following function:

$$y(n) = x_i(n) f_1(n) + x_q(n) f_2(n) \tag{1}$$

where:

$$f_1(n) = \{1,1,-1,-1,...\} \tag{2}$$

$$f_2(n) = \{-1,1,1,-1,...\} \tag{3}$$

The simple form of the local oscillator (LO) signals results from the sampling frequency being exactly four times higher than the desired carrier frequency. The sequences in (2) and (3) are easily implemented. The representative spectrum of the upconverted signal is shown in Figure 3:

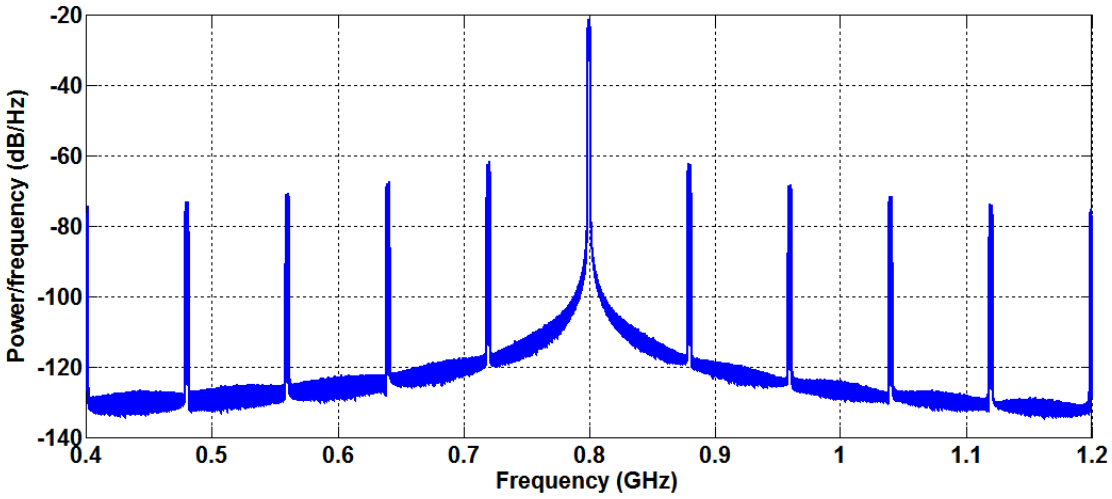

Figure 3: Simulated spectra of the signal immediately before delta-sigma modulation. Sampling is at 3.2 GHz and scaled to correspond to a 33 dBm transmit power. The noise floor is due to the spectral leakage of the Hamming window used.

The unconverted signal is then converted to a one-bit value through the use of a band-pass delta-sigma modulator. (A detailed block diagram of the band-pass delta-sigma modulator will be introduced later in Figure 9.) The ability to use a fast binary sequence to represent a complete, high dynamic range CDMA signal is surprising, but a

one-bit second-order band-pass delta-sigma modulated signal has been experimentally shown to exceed CDMA IS-95 requirements [2].

The spectrum of the output signal from the delta-sigma modulator is indicated in Figures 4-5. On a large frequency scale the quantization noise is apparent, but the noise is removed from the communication band of interest:

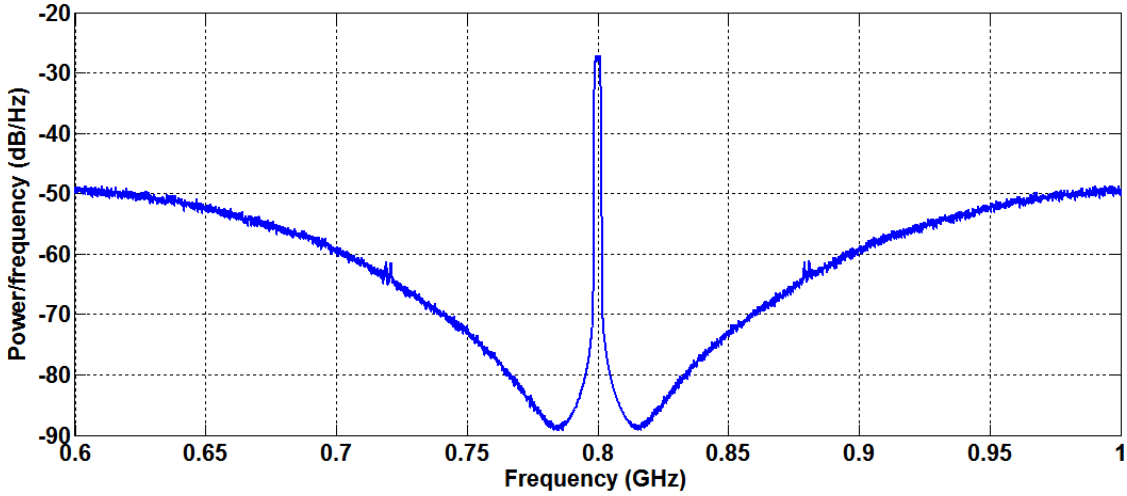

Figure 4: Simulated wide-band spectrum of delta-sigma modulated signal at a sampling rate of 3.2 GHz.

On a frequency scale comparable to the CDMA transmit band, the noise floor is low because of the spectral noise shaping achieved in the delta-sigma modulator. The following Figure also shows the approximate ACPR limits for CDMA signals in adjacent channels (assuming full transmit power).

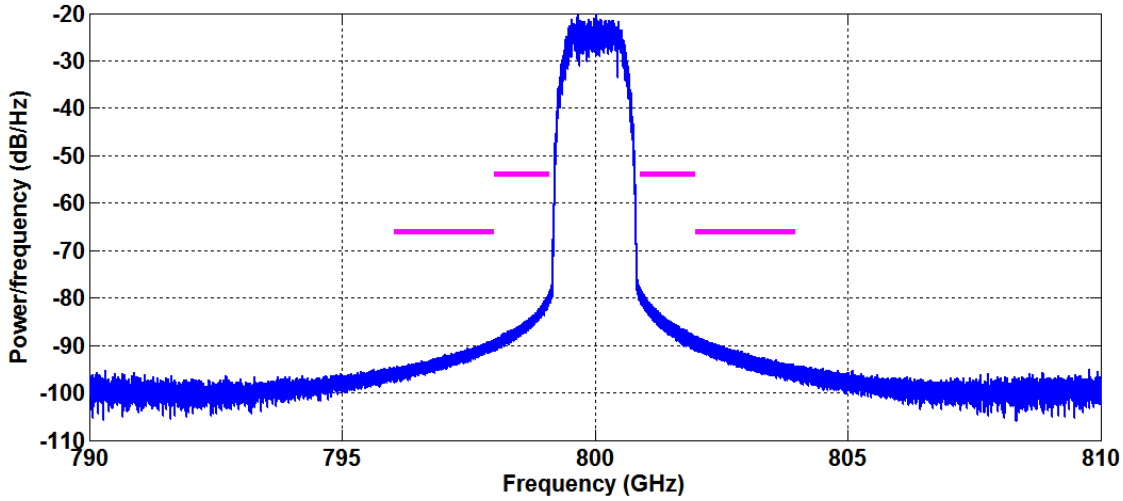

Figure 5: Zoomed view of the output spectrum in Figure 4, with lines drawn at the approximate ACPR limits shown.

The ideal signal has plenty of ACPR margin.

3.4. Amplification

The output of the modulator section is fed to a switching amplifier. Depending on the requirements of the transmitter, the power amplifier could be as simple as a large digital inverter that produces digital outputs corresponding to the delta-sigma signal. A major drawback is that classical digital inverters have little gain. This puts pressure on the design of the driver stages, as low gain amplifiers cause the driver stages to affect system efficiency more than traditional high-gain amplifier chains, where driver efficiency has little effect on total system efficiency.

This work focuses on two amplifier topologies: an inverter like structure and its differential analogue, an H-bridge. Both of these circuits are considered a voltage mode class-D amplifier (VMCD).

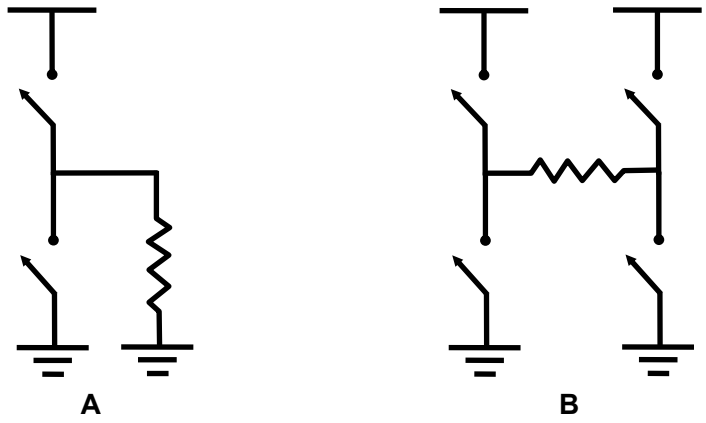

Figure 6: Class-D switching amplifiers: A) Single-ended B) Differential (H-Bridge)

Ideal two-state (one-bit) signals are a good match for switching amplifiers due to their inherent linearity. As long as these two states remain constant cycle to cycle, the system is linear. Non-ideally, states that change with time or memory effects can cause nonlinearities even in a two-state system. This nonlinear behavior of two-state amplifiers will be analyzed further in chapter 5. Two-state signals are well matched to drive both types of class-D amplifiers shown in Figure 6 A and B.

The H-bridge is typically used in two-state mode, where the pair of inverters switches differentially. The H-bridge has an interesting property as it can be also run as a three-state system with the addition of a state where both the inverters are switched into the same state. Three-state signals amplified though the use of an H-bridge structure (see Figure 6 B) also have a linearity advantage, as the two opposite output levels are derived from the same supplies using a differential drive structure. The linearity of a three-state H-bridge assumes the switching devices are well matched and the system can handle the common mode generated by the additional state.

3.5. Reconstruction Filter

Lastly, the output of the amplifier needs to be band-pass filtered to remove out-of-band quantization noise. This can be achieved by dedicated filters or a combination of duplexers already in a transmitter, additional resonators, and matching circuitry integral to the power amplifier, or by the frequency response of the antenna itself.

4. Delta-Sigma Modulator Simulations

The performances of different delta-sigma architectures were evaluated in simulation, primarily by the following criteria: spectral distribution of the test CDMA sequence and output noise, implementation complexity, and power dissipation. These evaluation criteria follow from key goals in designing handset transmitters: meeting specifications, lowering cost, and lengthening battery life.

4.1. Modulator Noise Transfer Function

One of the major problems with higher order modulator is that multiple noise transfer function (NTF) zeros all placed on the same part of the Z-plane, have diminishing benefits. Typical higher-order delta-sigma designs place NTF zeros across a band where quantization noise cannot be tolerated. The NTF zeros that do not fall on the axes of the Z-plane necessitate multiply operations and inter-stage adders in the corresponding hardware implementation. These complex implementations require many more gates, worsening the timing slack and power dissipation in the corresponding digital design. Inter-stage adders also preclude the use of many of the digital logic optimizations that will be presented later.

Techniques exist to synthesize high order delta-sigma modulators with staggered NTF zeros, where all the multiplier coefficients are powers of two [6]. Assuming the modulator is implemented in a binary number system, multiplication by powers of two can be accomplished with a shift operation, requiring little or no hardware. However, even when this technique is applied, higher order modulator implementations require intra-stage adders and a higher quantity of adders than a lower order system.

In evaluating whether this additional complexity is warranted, simulations were performed comparing a fourth-order modulator with an eight-order modulator. The eight-order modulator used the technique in [6] to stagger the NTF zeros. Both modulators were simulated with a 16-bit word length. As expected, the eighth-order modulator was less stable and had to be run at a lower in-band power ratio, and also required a larger word length to operate reliably. A comparison of spectra from the two modulators is shown in Figure 7:

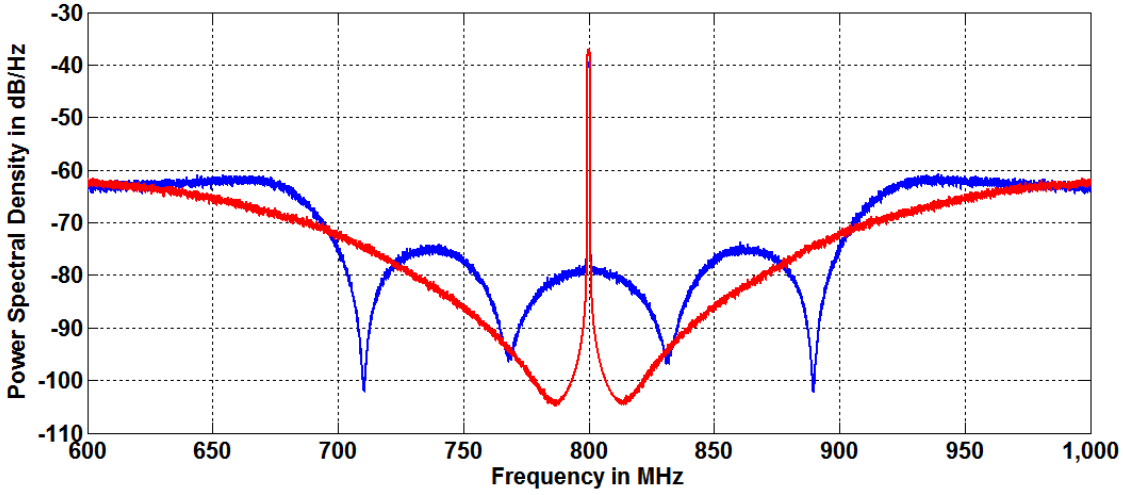

Figure 7: Simulated output spectra of an eighth order band-pass delta-sigma with staggered NTF zeros (blue) compared to a simple fourth-order modulator (red). Both modulators are running at a 3.2 GHz sampling rate, using 16-bit digital integrators.

The higher order design performs worse in the near-band (although both pass ACPR specs with margin). On the average the lower order design performs better over a wider band as well, except at the far NTF zero. The possibility of centering the quiet band caused by the NTF zero around the receive band is difficult, as moving the zero in the Z-plane causes the coefficients to change. If the coefficients are not powers of two, hardware multipliers will need to be used in place of the shift operation. Hardware multipliers running at multi-gigahertz rates, even in contemporary CMOS processes, would negate most of the power savings of the digital transmitter design. Optimizing the modulator for a quiet receive band will be the subject of the next section.

Higher order designs were not considered further in this research because of the aforementioned drawbacks. The rest of this work will focus on a fourth order band-pass design, where all of the NTF zeros fall on exactly on the Z-plane.

4.2. Optimizing a Delta-Sigma Modulator for Full Duplex Receive Band Noise

In the delta-sigma systems presented, the delta-sigma modulation rate is set at exactly four times the transmit band, putting the NTF zeros at the transmit freqeuncy. For a full duplex system, this freqeuncy plan is not feasable, as it would put high levels of quantizaion noise in the receive band, around 45 MHz higher than the transmit band, in the worst case frequency plan. The amount of filtering requred to condition this signal to avoid self jamming would negate the desired cost savings.

A better frequency plan is to set the sampling rate of the delta-sigma modulator to four times that of the receive channel, and freqeuncy shift the transmit signal down to the

desired transmit channel. This negates some of the simplification in section 3.3, but as this algorithmic complexity is not inside of a feedback loop, pipelining and other types of logical optimization can be used.

A simulation was setup targeted to a hypothetical cellular band, with handset transmit freqeuncies between 824-849 MHz, and receive channels between 869-894 MHz. The delta-sigma rate was set at four times the receive channel. The maximum power spectral density (PSD) allowed in the receive channel typically is around -140 dBm/Hz. The spectrum is given below:

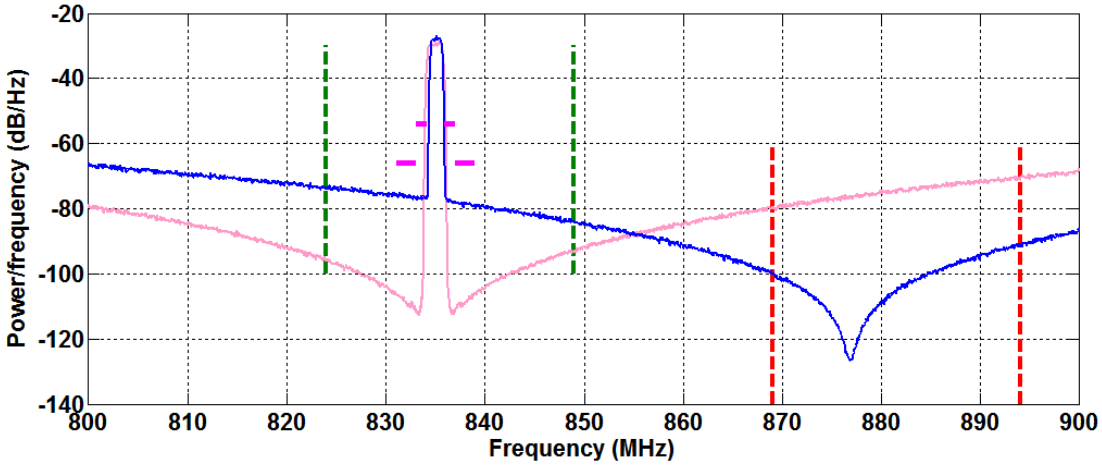

Figure 8: Simulated spectrum of a delta-sigma system with a frequency plan optimized for receive channel noise supression (dark blue). The power level is scaled for a 33 dBm transmitter. A Hann window was used to compute the PSD to preserve the NTF notch. A spectrum from a modulator with a NTF on the trasmit is shown for referance (light red) and the verticle dotted lines denote transmit (green) and receive bands (red). Approximate ACPR limits are shown in solid cyan.

In a full-duplex system this frequency plan offers around 40 dB lower trasmit to receive power leakage. The simulated system is only around 15 dB short of meeting the noise specification in a single receive channel. The ACPR is reduced, but still has signifigant margin.

This simulation paints an optimistic picture of a delta-sigma system which is close to meeting receive band noise specifications in a non-constant envelope full duplex system. However, the deep notch shown in simulaton is unlikely to survive in a realistic amplifier due to nonlinear effects. The entirety of chapter 5 is dedicated to the subject of preserving a quiet receive band though nonperidic switching amplifiers.

4.3. Modulator Block Diagram

The modulator implementation of Figure 9 was chosen.

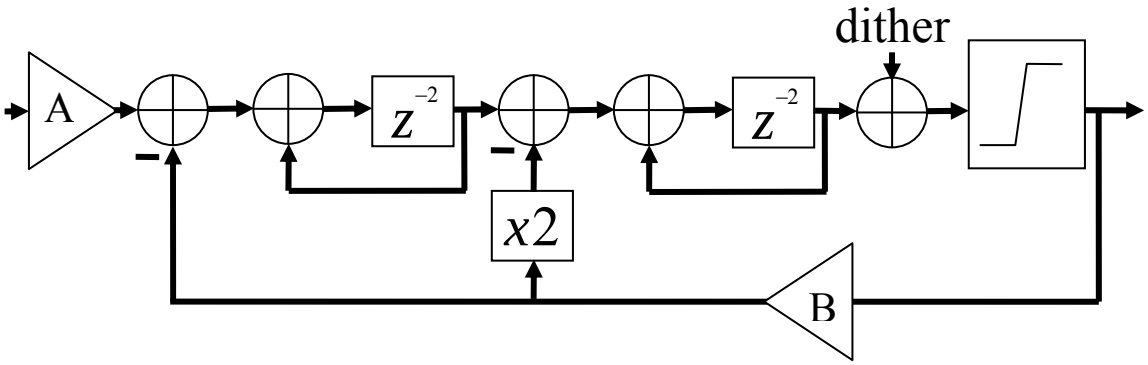

Figure 9: Delta-sigma modulator block diagram.

The block diagram shown in Figure 9 was chosen for simple, efficient implementation into digital logic. All the coefficients in the modulator are powers of two, thus allowing their implementation to be realized by a radix shift, requiring no logic. Further, delay elements in the modulator are arranged to occur immediately after major logical operations, so that the delay can be incorporated into the logical operation in the form of pipelining (in which the logical operation is split into sub-operations taking several clock cycles). Further optimization is possible because of these properties, and will be discussed later in the chapter.

The coefficients denoted by A and B (in Figure 9) set the input scaling and feedback scaling, respectively. The value of these coefficients together set the dynamic range through the delta-sigma internals. This range is important for modulators implemented in digital logic, working on fixed-point arithmetic. Low values of these numbers will increase the quantization noise added during each of the fixed-point mathematical operations that comprise the delta-sigma modulator. Excessively high values of A or B can cause adders to overflow, where the results of the add operation exceeded the maximum value that can be represented in the digital logic. This will be discussed more extensively later in the chapter.

The ratio of B to A determines the quantization level of the modulator. Higher ratios will cause more of the output power to be comprised of the desired signal, meaning a higher in-band power ratio. Lower ratios will cause more quantization noise to be generated, lowering the in-band power ratio. Excessively high ratios will have detrimental effects, similar to an analog amplifier in compression. These include: spectral impairments, such as ACPR degradation, and signal accuracy impairment, such as an increase in EVM. High ratios can also cause impairments not similar to classical amplifier compression, such as limit cycles to the point of complete modulator instability. The value and the ratio of the A and B coefficients also have nuanced effects, such as the shape of the overall noise transfer function. These will also be discussed in detail later in the chapter.

4.4. Modulator Numerical Representation

A signed integer-based representation (rather than floating point) was chosen based on the simplicity and speed of operations carried out with integers. In order to represent signed values, two's complement form is used based on easy adder implementation and widespread use.

The word length (or bit-depth) of the digital integrators is critical to circuit delay time, power dissipation, and die area. Longer word length not only requires more logic to compute, it also causes the carry signal to have to propagate through more logic. More advanced adder logic can reduce the critical path through the adder, but this advantage usually comes at the expense of die area and power dissipation.

Simulations, illustrated in Figure 10, show the output spectrum as a function of the word length of the digital integrators. This bit-depth simulation used a "no-overflow" simulation, where the integrator values are stored in variables larger than necessary and the entire value history of the variable is recorded in bin values, similar to a histogram. From the bin values, the log base two is taken of the largest absolute value. Rounding this maximum up results in the integrator word length required to represent the entire range of values seen by the integrator without an overflow.

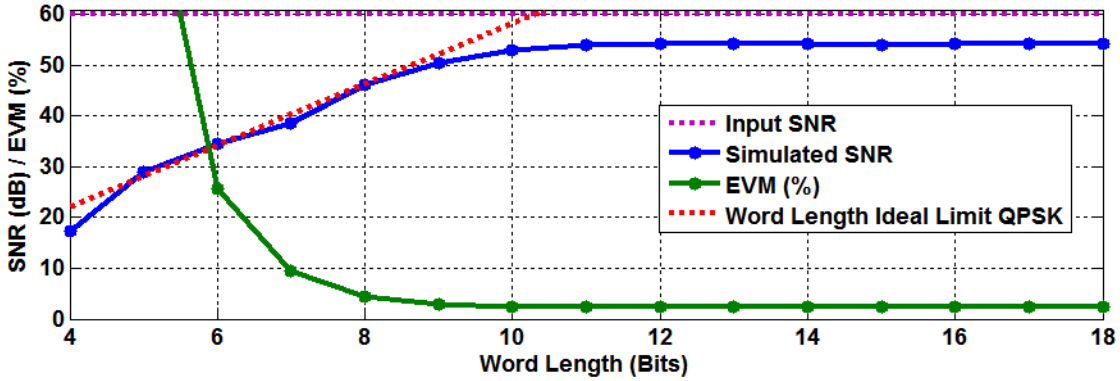

Figure 10: Simulated signal-to-noise ratio (SNR) (solid blue with circles, top) and Error Vector Magnitude (EVM) (solid green with circles, bottom) versus delta-sigma modulator word length. Also shown are the SNR of the input, and theoretical limits for quantization of the QPSK signal (red dashed, top left) and the pulse shaping filter SNR (cyan dashed, top).

The simulation suggests that word lengths in excess of 10 bits provide diminishing return as far as spectral purity and signal accuracy measures. However, the word length also affects the depths of the NTF notches which are important for frequency plans such as those introduced in section 4.2. Therefore, this work focuses on modulators with a 12-bit, two's complement numerical representation.

4.5. Dithering

Dithering purposely adds entropy into a delta-sigma modulator in order to randomize its operation and prevent spurious-tone-generating limit-cycles. Explicit dithering is essential for the operation of a delta-sigma modulator performing digital-to-analog conversion on periodic signals. This is in contrast with delta-sigma modulators serving as analog-to-digital converters where some level of noise is always present on the input signal and, due to the presence of natural noise adding entropy, explicit dithering is not always necessary. Delta-sigma modulators implemented with digital gates are

essentially finite state machines with no inherent entropy, so randomization is necessary. When given periodic inputs, or other sequences of low data entropy, limit cycles in the modulator can cause spurious tones [4].

The dithering operation is physically implemented by a linear feedback shift register (LSFR). The LSFR consists of series of registers in series with XOR gates placed at different locations, dependent on the length of the shift register. This implementation results in a finite state machine producing a one-bit pseudorandom sequence that repeats every 2^N-1 cycles (where N is the number of registers in the loop).

The outputs of the LSFR can be added to the final signal immediately before quantization (in the NTF loop), or to the incoming signal. Adding the dither in the NTF loop causes the modulator to shape the dithering noise along with the quantization noise. This allows for large dithers of up to a significant fraction of full-scale. Unfortunately adding the dither into the NTF loop worsens the timing slack in the digital domain, as another adder is cascaded in a feedback loop, which needs to complete in two clock cycles.

In the case of adding the dither to in the input signal, the adder is outside of any loop, so it can be pipelined, thus not adding to the critical path of the design. Unfortunately, the noise is added directly to the signal, with no noise shaping applied. This can be mitigated by filtering the noise with a digital filter, at the expense of the area and power dissipation used by said digital filter. The digital filter will keep the noise from falling in NTF zeros, but will, at high levels, lower the in-band power ratio and distort the shape of the NTF. To avoid these issues, dither added directly to the input signal is typically limited to a small fraction of the signal.

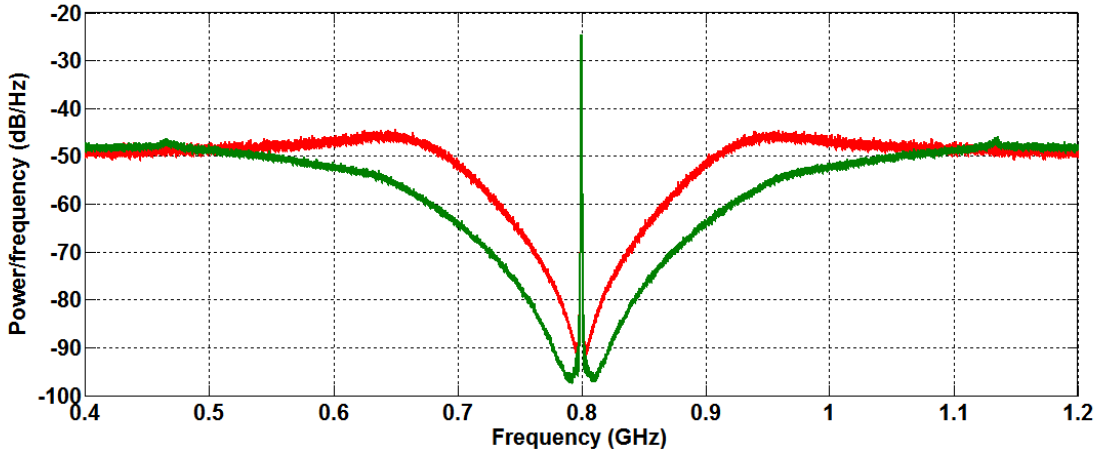

Figure 11: Simulated output of a delta-sigma modulator with no dither (green), and full-scale uniform dither (red) added in the NTF loop.

Fortunately, dithering for the applications considered here is typically not critical, since spread-spectrum signals, like CDMA, are pseudorandom by nature and have enough entropy in most cases to keep delta-sigma modulators from exhibiting excessive spurious tones. Figure 11 shows a delta-sigma system encoding a spread spectrum signal with no dither. For comparison, a system with full-scale dither is also included to exaggerate the effects of the dither. With spread-spectrum signals, dither is only needed in special cases, and will not be used by default.

4.6. Digital Integrator Overflow

A realistic delta-sigma system encoding a pseudorandom spread-spectrum signal would periodically encounter a statistically improbable peak. Improbable peaks can cause add operations to result in numbers larger than can be represented in the fixed word length of the adder (overflow). Up to this point, simulations have tracked the range of values stored in the simulated integrators, but overflows have been avoided by design.

Understanding the overflow behavior in a digital system implementing a delta-sigma modulator is important due to the significant disruption caused by the default overflow behavior of digital adders. A binary complement adder in an overflow condition applies a modulo operation to the resulting sum. This causes the result of an overflow causing add to wrap from positive set of integers to negative and vice versa. The following base-10 function describes the overflow in a two's complement adder, where % represents the modulo (remainder) operator:

$$SignedSum(A,B) = \left[\left(A + B - 2^{N-1}\right)\%2^{N}\right] - 2^{N-1} \tag{4}$$

With the overflow behavior described in (4), overflows introduce a huge error the integrator. The error is large enough that the noise shaping properties of the modulator degrade to the point of failing ACPR specifications when only 1 out of 100,000 adds results in an overflow. Figure 12, below, shows the degradation from overflow behavior a delta-sigma modulator:

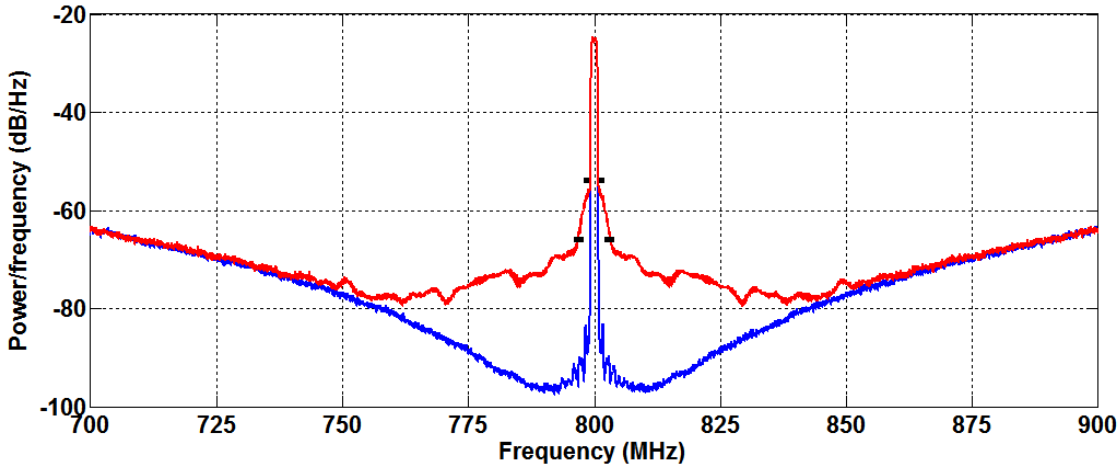

Figure 12: Simulated output spectra for a delta-sigma modulator with wrap overflow (red). A modulator without overflow is shown for reference in blue. ACPR approximate limits are shown in black.

Delta-sigma modulators with overflow are very sensitive to the scale of the input signal, and very unstable under conditions of large input swings. A modulator can transition from stable proper operation to a limit cycle with only a factor of two in input amplitude scaling.

A fix to this problem is to detect an overflow condition in the integrator and limit the integrator value to the maximum or minimum, depending on which way the overflow occurs. After the simulated integrators were changed to limit rather than overflow, proper spectra were obtained. The overall sensitivity to input scale is greatly reduced. A greater fraction of the digital integrator can be utilized, effectively increasing the word length. The increased integrator utilization can be seen in the right of Figure13:

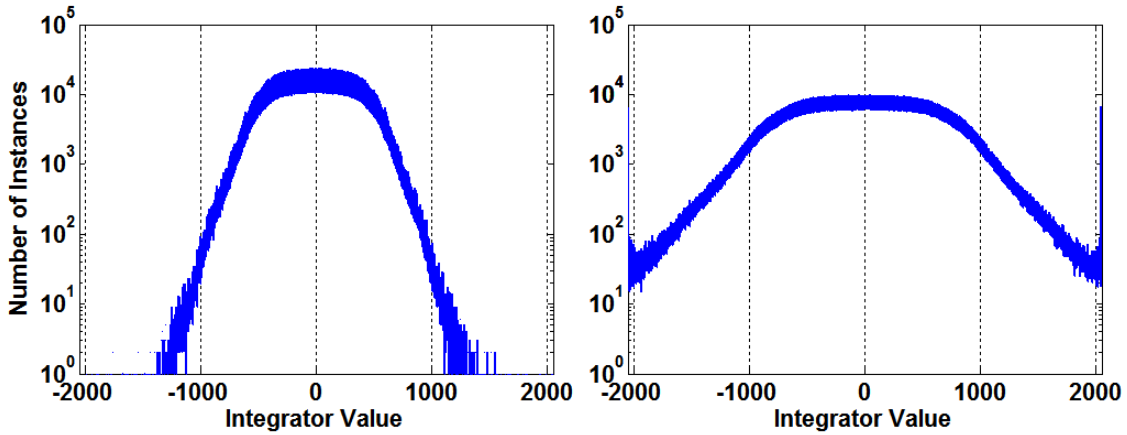

Figure 13: Histograms of simulated final stage integrator values with wrap overflow (left) and saturate overflow (right). Both systems use 12-bit integrators, and the coefficients are set for maximum SNR.

This fix increases the performance and, as a side benefit, the stability is improved. The modulator with modified overflow can stably operate with overflow conditions occurring in one out of fifty operations. As a side note, directly comparing rates of overflows between the two types of modulators is an invalid comparison. For a given input

magnitude, saturate-on-overflow systems will have more overflows because the wrapping effectively resets the stored value in the integrator to the opposite magnitude.

Saturate-on-overflow reduces the sensitivity to input signal magnitude. Input magnitudes increasing to the point of causing overflows gradually degrade the spectral performance of the modulator, rather than causing instabilities and a catastrophic breakdown of the noise-shaping properties of the modulator. Saturate-on-overflow based modulators can also be more aggressively tuned for high in-band power ratio, an advantage to be discussed later in the chapter.

Modifying the digital adders to saturate on overflow increases their complexity, but can also allow similar modulator performance using narrower word lengths. Implementing adders to saturate on overflow is a clear overall benefit, so all simulations later in the chapter will use saturation. Optimization techniques, presented later in the chapter, alleviate some of the hardware implementation penalties of saturate-on-overflow.

4.7. Number of Quantizer States

Most switching amplifier systems utilize delta-sigma modulators having two-output states, due to the simplicity of driving standard switching amplifiers with two-level signals. Also, two-level systems are free from the integral and differential nonlinearities that plague multi-level systems implemented without perfect component matching. However, as discussed earlier in section 3.4, a differential amplifier topology can be used to implement a three-level system while maintaining an inherent output level matching.

The differences between the digital implementations of the two- and three-state machines are minimal, with the triple-state machine being slightly more complex. Aside from the obvious benefit of lowering quantization noise and raising in-band power ratio, adding an additional state adds stability to the delta-sigma system. Added stability allows modulator tunings for higher in-band power. For the rest of chapter 4, both two and three-state modulator systems will be considered.

4.8. In-Band Power Ratio

As discussed earlier, one of the main figures of merit in a power delta-sigma design is in-band power ratio: the ratio between the total output power (desired power and quantization error power) and the desired power. In low power delta-sigma systems, this figure of merit is not as critical as the desired power ratio is less important than linearity, resolution, and accuracy. In a power system, accuracy and linearity can be traded for power efficiency to the extent the EVM and spectral mask specifications allow.

The ratio of desired power to total power in a delta-sigma system can be easily altered by changing the ratio of the input amplitude (A in Figure 9) to the feedback amplitude (B in Figure 9). The following simulation shows two delta-sigma systems though a range of feedback coefficients:

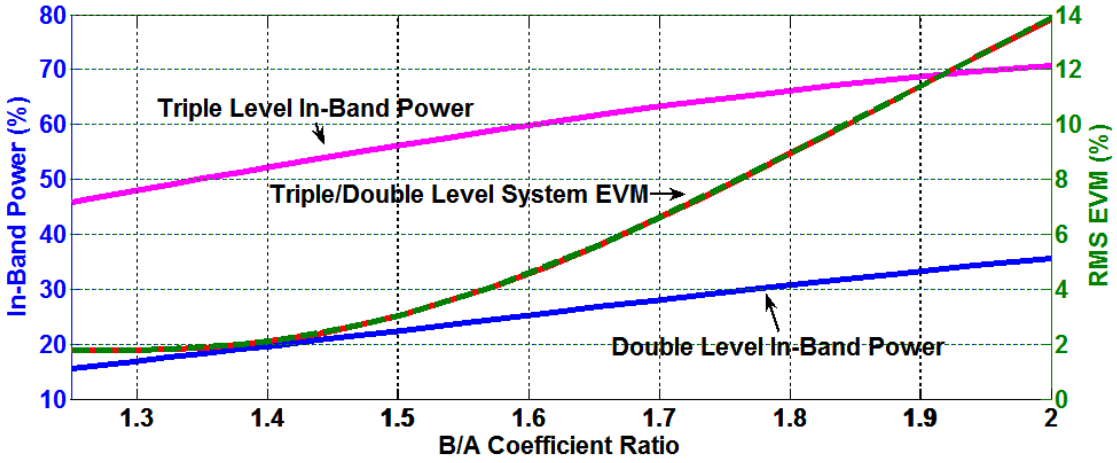

Figure 14: Simulated EVM and in-band power ratio for two and three-level based delta-sigma systems.

Figure 14 illustrates tuning for the tradeoffs between EVM, and usable power. The ACPR is not shown because as the B/A ratio is increased the spectral purity is mostly maintained, while the signal accuracy degrades very rapidly. For this reason, spectral mask tests alone are a poor evaluation in tuning the feedback ratio in delta-sigma systems.

From this point on, graphs will use the in-band power ratio as an independent variable, as opposed to the algorithmic coefficients. This detaches the data from the specifics of this delta-sigma algorithm, allowing better comparison between different encoding algorithms, not necessarily having equivalent coefficients.

4.9. Gain Control

A critical requirement for handset transmitters, (particularly CDMA) is the need to vary the average RF output power over a wide range (typically 60-70 dB) in accordance with the characteristics of the wireless channel. A user near the edge of cellular coverage must use a high RF power (~28 dBm), while a user near the base station

must use a much lower power (~-30 dBm) in order not to interfere with other users. Many of the spectral purity specifications are relative (for high output powers) to the transmit power. Lowering the transmit power without causing additional quantization noise is challenging for a delta-sigma system.

The system envisioned in this work uses a DSP controlled DC-to-DC converter to control the supply voltage to the switching amplifier for coarse transmit power control. Power control can also be achieved by purposely scaling down the in-band power ratio, but this will not lower the quantization noise floor [3]. Lowering the power by scaling the signal degrades the signal-to-noise ratio by the same scaling factor, which is unacceptable over a large dynamic range. A simulation was performed of a delta-sigma modulator undergoing algorithmic power control:

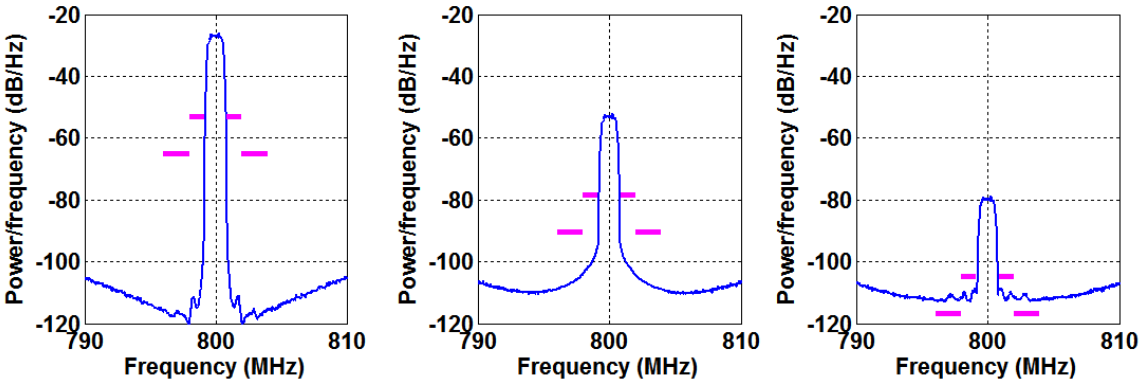

Figure 15: Output spectra CDMA waveform power scaled solely using delta-sigma coefficient changes. Shown with approximate ACPR limits.

Power control using coefficient scaling does not change the noise floor of the system, and only works to the point of the ACPR margin. The system, as ideally simulated, shows a large range of power levels that still meet ACPR. In a real system, the ACPR margin will be reduced by the nonlinearity of the transmitter components, and the majority of this margin will disappear. This type of power scaling could still be

useful to achieve a limited range of fine step-size power control. This would be particularly useful if fixed attenuators are switched in to reach the lowest average transmit power levels.

5. Delta-sigma Modulator Hardware Implementation

The limiting digital block for the delta-sigma modulator hardware implementation is the integrator within the delta-sigma modulator feedback loop. In this application, this adder has to operate around 3.2 GHz, meaning the longest operation can take no longer than 312 picoseconds. The adder must also detect overflow conditions and override the default wrapping behavior. The timing specification is difficult to meet, since standard overflow detection algorithms XOR the last two carries to determine if an overflow has occurred. The carry out signal in adders is usually the last signal to become valid, and thus any logical operations performed with it add to the critical path delay. Cascading adder stages make the delay worse, as multiple adders must operate, all with saturate-on-overflow hardware. Many techniques can been employed to implement the delta-sigma modulator function in a hardware-efficient manner, some of which will be discussed for this application.

5.1. Band-pass Resonator Parallelization

A band-pass resonator that has no inter-stage adders has no data dependence between cycles, and therefore can be broken into two interleaved low-pass integrators:

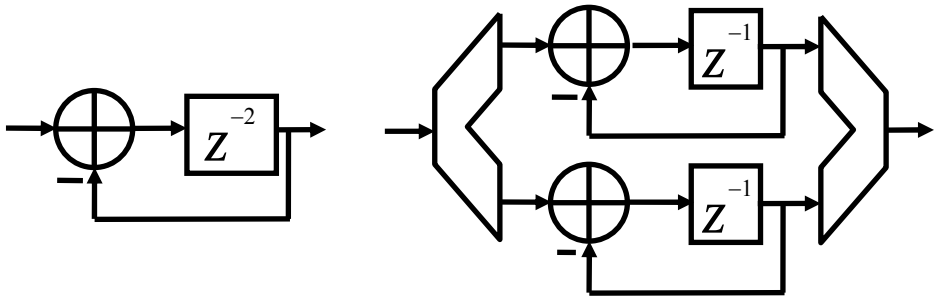

Figure 16: Band-pass double-delay resonator (left) to parallel single-delay resonator (right) transformation.

This halves the clock rate of a band-pass delta-sigma modulator, with the caveat that the adders no longer can be pipelined over the two clock cycle delays. Nonetheless, parallelization is helpful for optimization.

5.2. Two's Complement Negation Optimization

Unfortunately, negation in two's complement requires a bit-wise inversion followed by an increment. This increment operation is typically carried out by a binary adder. In the worst case condition, where a zero is negated, a carry signal has to ripple through the entire increment adder, adding as much delay to the system as the adder implementing the integrator. Lastly, in a saturate-on-overflow system, this adder needs to have overflow detection circuitry, further adding to the delay.

These problems can be solved by implementing the negation operation as a bitwise inversion, which is in effect a negation with an error of negative one, as shown in Figure 17. This offset can be cancelled out by holding the carry-in bit of a subsequent adder high.

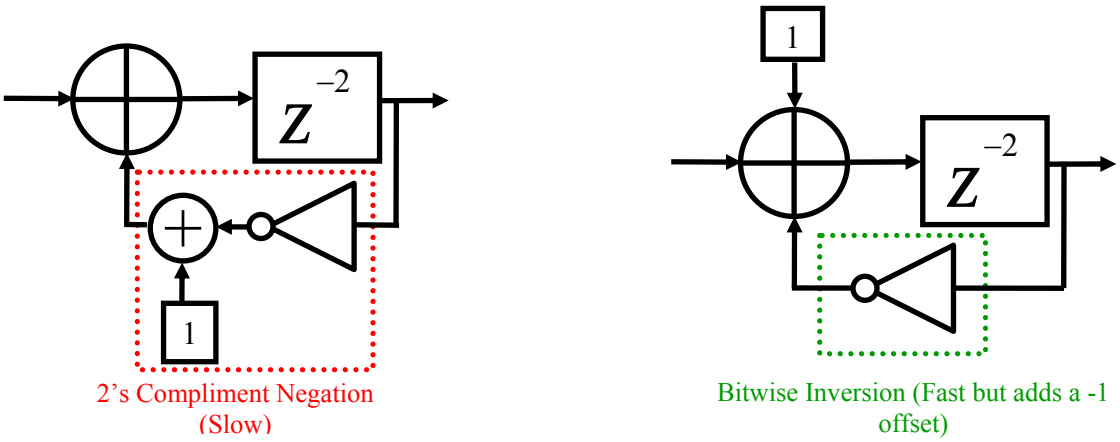

Figure 17: Two's complement negation optimization (right) shown compared with standard negation (left).

This technique allows the two's complement negation to run as fast as a bit-wise inversion operation. This is a huge advantage, as bit-wise operations are completely independent of adjacent bits, and have very low latency.

5.3. Triple-Input Adders

The last operation in the delta-sigma modulator with significant room for logical improvement is the two cascaded add operations, both with saturate on overflow. One of the adders implements an integrator, and thus has its own negated output as in input. The other adder has the delta-sigma output back for an input. The feedback signal from the quantizer is a two/three state signal and, depending on the feedback coefficient (B in Figure 9), the first adder only needs to change a certain number of the most significant bits (MSBs) of the incoming signal. A three-input adder structure can be implemented, where all three input values are added simultaneously. This has the added benefit of only requiring one overflow detection step.

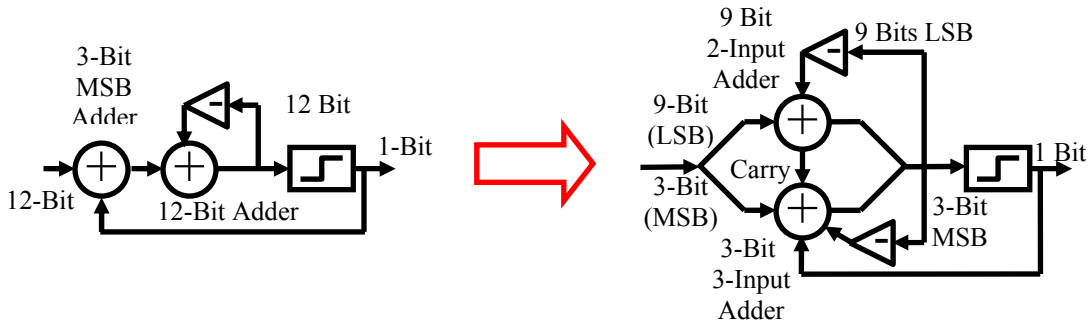

Figure 18: Block diagram for one possible method to transform a 12-bit two-input adder cascade to a single triple-input adder.

Here, two cascaded adders from a twelve-bit delta-sigma system with a feedback coefficient of a minimum one quarter of full-scale are transformed into an adder formed from a nine-bit LSB adder and a three-bit three-input MSB adder. The feedback signal only affects the three most significant bits of the signal, so the adder is split into a three-bit MSB and a nine-bit LSB sections. The logic for a three-bit three-input adder is significantly more complex than the typical two-input adder. The equations for a three-input non-cascaded binary adder are visualized by the following figure:

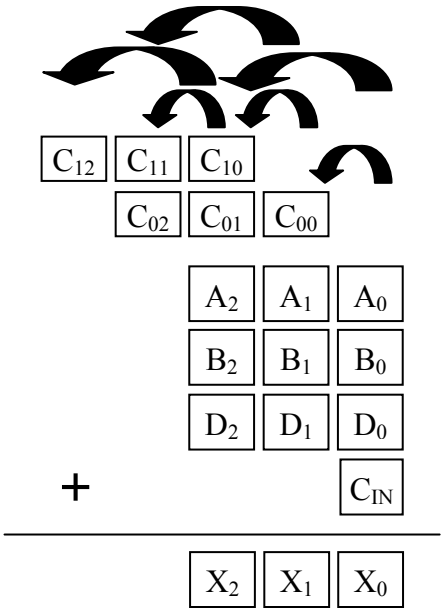

Figure 19: Graphical depiction of equations for a three-bit two-input binary adder. The top arrows trace the origins of the carry signals.

The greatest difference between a two-input and a three-input binary adder structure is the carry chain. A typical two-input adder is implemented with a carry generate/propagate/kill structure. When this is extended to a three-input case, the carry lines expand to a two output system, a carry and a carry-skip signal. In the worst carry case of a 3-input adder, the row of 4-bits can generate a carry that "skips" the next most significant bit. An illustrative example would be where A_0, B_0, C_0, and C_{IN} are all ones, we would expect an output of 4 in binary (100). The output bit, X0 would be zero, the typical carry signal, C00 would also be zero, but the carry "skip" signal would be one. The following Boolean equations (5-12) implement a three-bit three-input adder as shown in Figure 19.

$$X_0 = A_0 \text{ XOR } B_0 \text{ XOR } D_0 \text{ XOR } C_{in} \quad (5)$$

$$C_{00} = (A_0 \text{ XOR } B_0)(D_0 + C_{in}) + D_0(A_0 \text{ XOR } C_{in}) + A_0(D_0 \text{ XOR } B_0) \quad (6)$$

$$X_1 = A_0 \text{ XOR } B_0 \text{ XOR } D_0 \text{ XOR } C_{00} \quad (7)$$

$$C_{01} = (A_1 \text{ XOR } B_1)(D_1 + C_{00}) + D_1(A_1 \text{ XOR } C_{00}) + A_1(D_1 \text{ XOR } B_1) \quad 8)$$

$$C_{11} = C_{00} A_1 B_1 D_1 \quad (9)$$

$$X_2 = A_2 \text{ XOR } B_2 \text{ XOR } D_2 \text{ XOR } C_{01} \text{ XOR } C_{10} \quad (10)$$

$$C_{02} = (A_2B_2D_2 + `A_2`B_2`D_2)(C_{10} \text{ XOR } C_{01}) + C_{10}C_{01}`A_2`B_2 + A_2 (B_2 \text{ OR } D_2)`C_{10}`C_{01} + (A_2 \text{ XOR } B_2)`D_2C_{10}C_{01} + `A_2B_2D_2`C_{10} \quad (11)$$

$$\text{Positive Overflow} = C_{11} \text{ XOR } C_{O2} \text{ XOR } A_2 \text{ XOR } B_2 \text{ XOR } D_2 \text{ XOR } X_2 \text{ AND } A_2 \text{ AND } (B_2 \text{ OR } (D_2 \text{ AND } B_2) \text{ OR } (A_2 \text{ AND } D_2)) \quad (12)$$

$$\text{Negative Overflow} = C_{11} \text{ XOR } C_{O2} \text{ XOR } A_2 \text{ XOR } B_2 \text{ XOR } D_2 \text{ XOR } X_2 \text{ AND } `(A_2 \text{ AND } (B_2 \text{ OR } (D_2 \text{ AND } B_2) \text{ OR } (A_2 \text{ AND } D_2))) \quad (13)$$

To have a non-overflowing three-input adder, the adder would require two carry out signals derived from adding the three extra carry signals. Saturate-on-overflow characteristics can be achieved by adding logic to override the normal outputs when an overflow line is asserted.

5.4. FPGA Implementation

The above algorithms were written into VHDL and synthesized and implemented in a field programmable gate array (FPGA) to verify functionality and quantify any improvement over directly synthesized integrator structures. The integrator structure was further refined to implement the saturate-on-overflow characteristics.

The novel structure, dubbed a cross-select adder, has both a carry select line propagating from the least significant adder, and an overflow select line propagating down from the most significant adder. Similar to carry select adders, two sets of MSBs are pre-calculated, and the carry out of the least significant adder is used to select which set of MSBs are outputted. In this case, the carry out of the least significant adder is also used to select the overflow out of the most significant adder, which in turn overrides the LSBs of the lease significant adder. This is shown in the following block diagram:

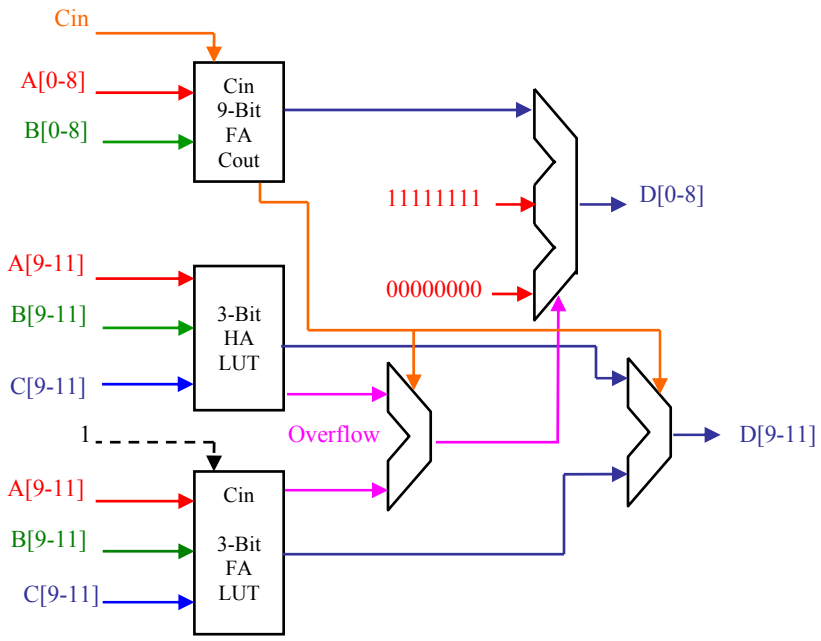

Figure 20: 12-bit three-input adder implementation block diagram.

The adder was designed in VHDL, and simulated in Xilinx ISE. Implementing the three-input adders in a look up table (LUT) was faster and smaller than using the above equations to implement the three-input adders. As a side benefit, the LUT based adders can have the saturate-on-overflow characteristics built into the table.

Table 1: Adder propagation delay comparison.

Adder Type	Logic Delay (Virtex 2P)
Synthesized Default 2-Input Adder (No Saturate on Overflow)	9.29 nS
Optimized 3-Input Adder (Saturate on Overflow)	6.1 nS

The optimized design completes an operation equivalent to a cascade of two adders, both with overflow detection. Delta-sigma modulator implemented with these adders can operate more than twice as fast as the synthesized default with the added benefit of saturate-on-overflow.

6. Hardware Measurements

Two of the two-stage VMCD amplifier chips with output resonators, first introduced in chapter 2 section 4.5, were combined to form an H-Bridge amplifier. Impedance matching from a 7 Ω load line at 800 MHz to 50 Ω was achieved using a quarter-wave transmission line combined with a coax balun. The resonators were designed to present an open circuit to the amplifiers at frequencies outside the 800 MHz target frequency.

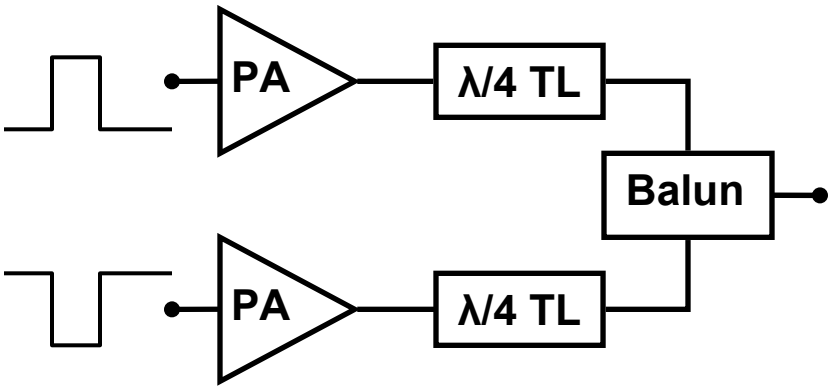

Figure 21: Block diagram of H-bridge amplifier.

Under continuous wave (CW) operation with a 2 V supply, the resulting amplifier achieved a peak drain efficiency of 62%, with a PAE of 45%, and a maximum power out of 21 dBm. The PAE here is defined as the power output over the dissipated power of both the final stage and the driver. The drain efficiency is defined as the power out over the power dissipated in the final stage only.

The amplifier is driven by an Agilent 81134A pulse pattern generator loaded with delta-sigma encoded CDMA signals. Ten sets of signals are generated, all based off of the same CDMA sequence, but encoded with varying ratios of B to A (see section 4.8). The in-band power ratio of these signals ranges from 10% to slightly over 40%. The ACPR specification is violated slightly as the in-band power is ramped to 30%. The corresponding drain efficiency is 31%. The entire measurement is presented below:

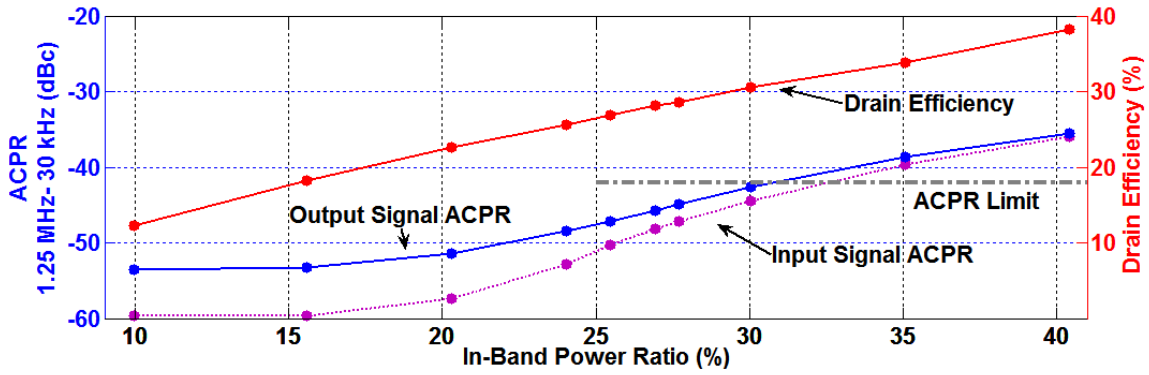

Figure 22: Drain efficiency and ACPR for the H-bridge with distributed match, at a 2 V supply, driven with a two-level CDMA delta-sigma signal.

Here, the in-band power ratio of the input sequence is an excellent predictor of amplifier performance, as losses in this amplifier are dominated by capacitive switching loss. Resistive losses in this amplifier are low due high power back-off required to meet the spectral purity requirements.

Adding a third state to this system improves the efficiency slightly but not nearly as much as the simulations predict. The following figure compares the H-bridge amplifier with both two and three state drive:

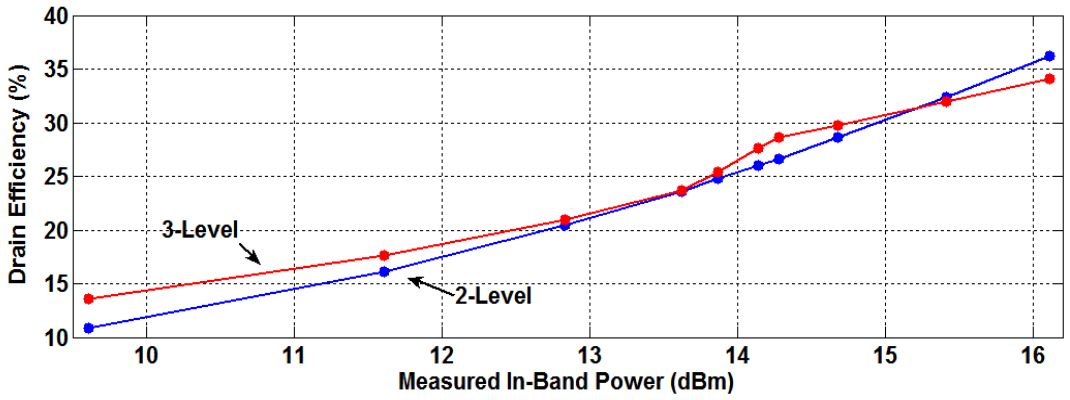

Figure 23: Drain efficiency comparison between H-bridge amplifier driven with two-level signal and three-level signal.

The marginal improvement from the three-state system results from the common mode response of the balun. The simulation did not take into account the particularities of the output balun when driven in common mode operation. When the amplifier is in the middle state, it is no longer a true differential system. This excites the common-mode response of the balun, which was not taken into account in the simulation.

Even with a two-state drive, the wide-band spectral performance of the amplifier is orders of magnitudes away from being usable in a full-duplex system. The input/output spectra of the amplifier are given below:

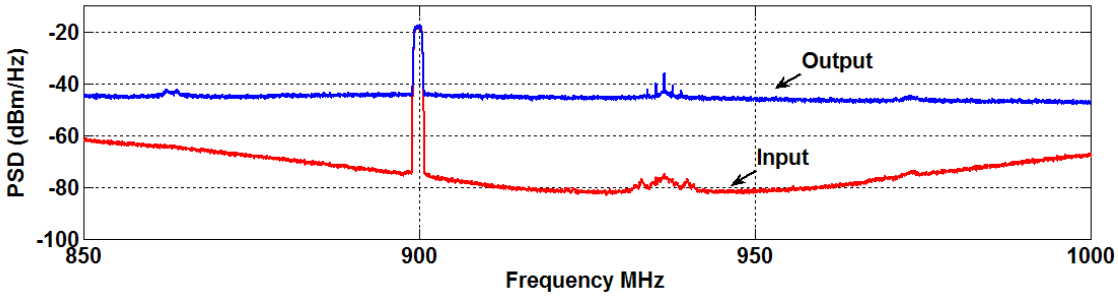

Figure 24: Wideband spectral performance of the CMOS VMCD amplifier.

The measurements of the wideband noise were verified several times. The noise from the amplifier is basically flat from the adjacent channel, and the NTF notch of the delta-sigma modulator is completely filled in by the amplifier. The reasons and solutions for this spectral degradation are the subject of the next chapter.

7. Summary and Conclusions

Digital cellular standards with a time-varying envelope, such as CDMA, are a difficult class of signals to reproduce at high power levels with a delta-sigma based digital transmitter. Even with mitigation techniques, the spectral purity of the VMCD output is several orders of magnitude from meeting the requirements of a full-duplex communication system. The dynamic range of power offered by this delta-sigma system is at least an order of magnitude short of contemporary standards and needs augmenting with other techniques.

A delta-sigma driven VMCD digital transmitter design cannot meet all of the power and spectral purity specifications demanded by modern communication standards without a level of workarounds that would negate the simplicity and power benefits a digital design brings. The rest of this work will explore other techniques to make possible a handset-class digital transmitter.

8. Acknowledgments

Some of the material presented in chapter 4 is as it appears in [9], [10], and [11]. The author of this dissertation was the primary investigator and primary author for [9] and [10] and the portions used from [11]. Some of the data used in this chapter is as it appears in [7] and [8]. This research has been partially supported by the UCSD Center for Wireless Communications, by the US Army under the MURI program, and by Cal-(IT)2.

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Chapter 5
Switching Mode Nonlinearities and Broadband Noise

1. Introduction

This chapter presents a detailed analysis of nonlinearities in switching amplifiers that cause broadband noise. A fixed time-step simulation method is introduced that captures switching amplifier nonlinearities that are computationally prohibitive with traditional simulation techniques. New measurement techniques are introduced that can quantify the level of asymmetric slew rate impairments that cause signal corruption. Lastly, the analysis will be validated with an amplifier redesign reducing broadband noise by more than an order of magnitude.

2. Frequency-Division Full-Duplex Communication

Limited bandwidth drives modern communication systems to higher spectral efficiency resulting in a migration toward full-duplex uplink/downlink signals using frequency-division duplexing (FDD), thus avoiding the overhead of guard times necessary with time-division duplexing (TDD). FDD avoids both inter and intra base station guard times, increasing network capacity [1].

As FDD systems transmit and receive RF signals simultaneously, more demanding spurious noise specifications are necessary in transmitter design to avoid self-jamming. TDD transmitters need only have spurious emissions attenuated to levels set by the regulatory agencies in the relevant country of operation. For low to medium

power TDD digital transmitters, these limits are typically quite easy to meet with little or no filtering. However, they are difficult to meet for the spurious power levels needed to avoid self-jamming in FDD systems. Consider a simplifier block diagram of the antenna in a FDD system:

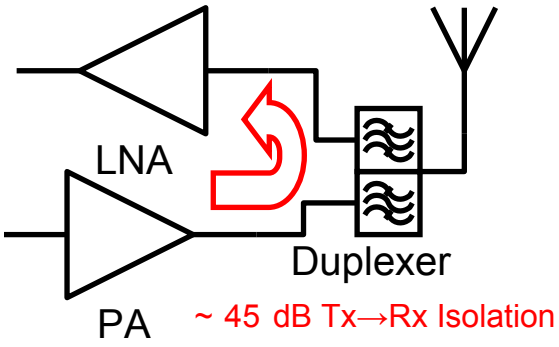

Figure 1: Full duplex communication system block diagram showing TX-to-RX self-jamming.

In order to have maximum receiver sensitivity, a communication system should avoid desensitizing its receiver with transmitter noise, which can leak through the duplexer from the transmitter. Self-jamming occurs when spurious emissions from the transmit chain, falling in the frequency band of the system's receiver, degrade the received signal. Normally the receiver and transmitter are electrically separated by a duplexer. A duplexer is typically a sophisticated set of filters to allow the downlink signal to pass from the antenna to the low noise amplifier (LNA) of the receiver, and the uplink signal from the power amplifier to the antenna. Duplexers are often made from exotic electroacoustic filter technology and typically offer from 40-50 dB of isolation from transmit to receive path in the receive frequency band. Even with this high level of

isolation, self-jamming limits in an FDD switching amplifier based transmitter are difficult to meet.

Ideally, to avoid receiver desensitization, the spurious tones leaking though the duplexer should be near the natural thermal noise of the system (approximately -174 dBm/Hz at room temperature). Accounting for the attenuation of the duplexer and overhead allowed in the standards, the maximum spurious power a transmitter can generate in the receive band, before receiver desensitization occurs, is approximately -140 dBm/Hz. Typical transmit-to-receive frequency separations can be as much as 400 MHz in the high bands (UMTS IV) and as little as 30 MHz in the low bands (UMTS XII, planned) [2].

3. Delta-sigma NTF and Full Duplex Receive Band

As discussed in chapter 4, the delta-sigma noise transfer function (NTF) zeros can be optimized to shape quantization noise out of the receive band. The center of the receive band is set to one quarter of the clock rate of a band-pass delta-sigma modulator. The desired communication signal, QPSK, is thus frequency shifted into the proper transmit channel. This frequency planning strategy allows a significant reduction in the amount of quantization noise needed to be filtered from the LNA in order to not to interfere with the receiver, as shown in Figure 2:

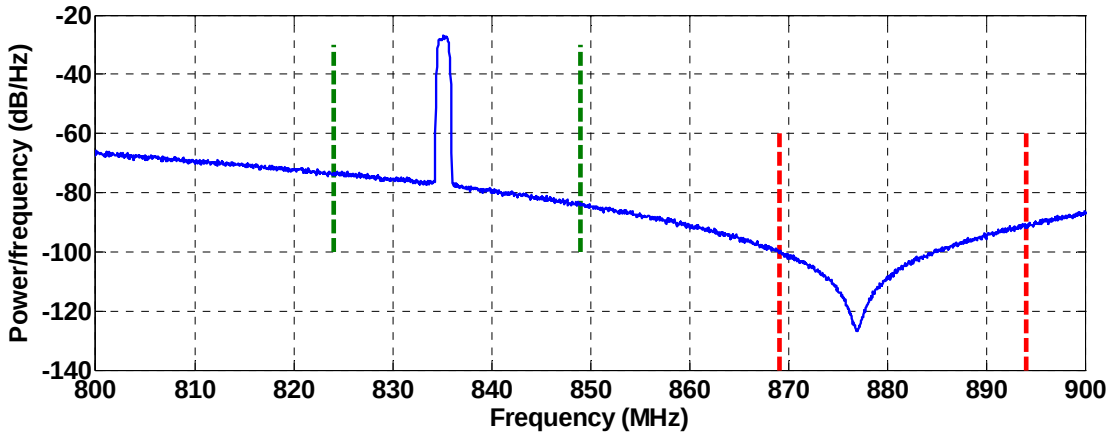

Figure 2: Simulated delta-sigma encoded CDMA spectrum with NTF zeros optimized for RX band noise performance (from chapter 4, Figure 8).

This simulated spectrum example shows a delta-sigma system targeting the 850 MHz cellular band. The delta-sigma sample rate is set to four times of the center of the downlink frequency, here 3.526 GHz. For verification a 2^{25} long pattern is generated from a simulation of the above delta-sigma modulator and loaded into the pattern memory of an Agilent 81134A. This pattern is then played back and measured with an Agilent N9020A MXA spectrum analyzer.

For verification purposes, the signal generator was first connected directly to the spectrum analyzer, resulting in the spectrum in Figure 3:

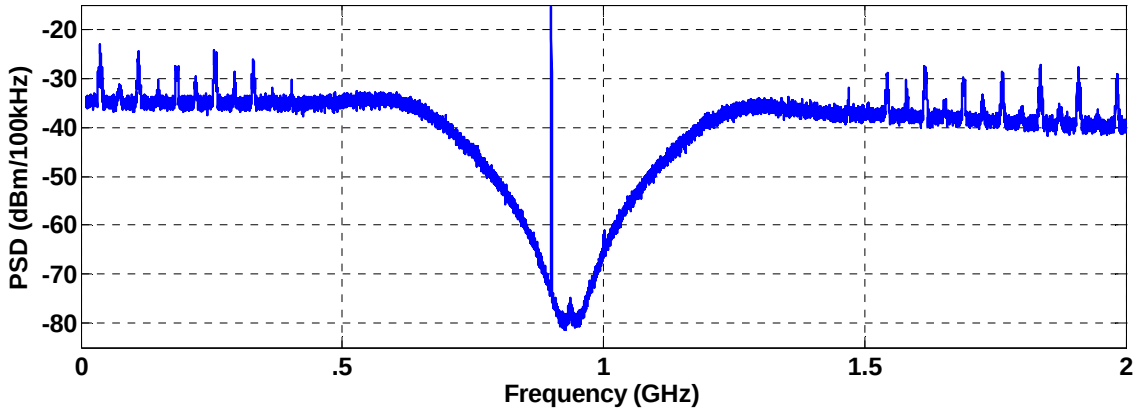

Figure 3: Measured output from the delta-sigma signal generation system (Agilent 81134A).

When this signal is subsequently used to drive a CMOS based VMCD amplifier, the signal spectrum is corrupted to the point that the noise notch in the receive band effectively disappears. Figure 4 shows the output and input of the CMOS VMCD amplifier first introduced in chapter 4, section 6, with the drive signal given in Figure 3:

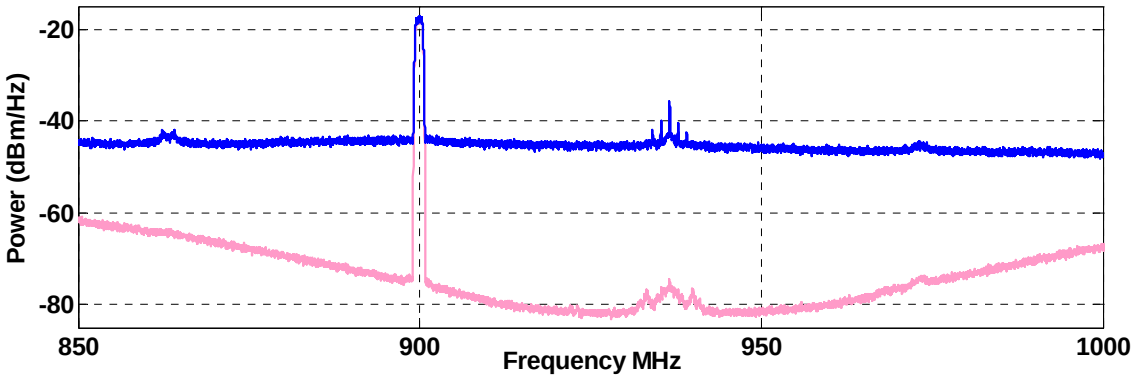

Figure 4: Measured input (light red) and output (blue) of the VMCD amplifier driven with a delta-sigma signal.

The amplifier severely corrupts the output signal. Looking at wider bandwidth, in Figure 5, the spurious emissions of the VMCD amplifier are so large that the noise shaping of the delta-sigma signal is almost lost:

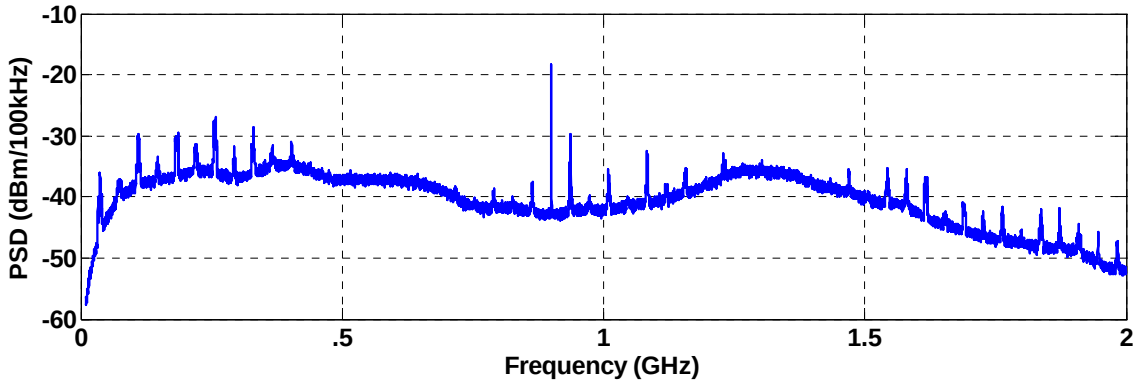

Figure 5: Measured broadband spectra of VMCD amplier output.

Unfortunately, due to the extremely wide bandwidth of the delta-sigma signal, the particular source of the spurious noise is not readily ascertainable. Many different types of nonlinearities and memory effects exhibit similar spectral corruption. Due to the broadband nature of the quantization noise, many of these undesired non-idealities manifest in the frequency domain in a convolution, folding the broadband quantization noise back into the NTF notch, effectively filling it in.

4. Quantifying Nonlinearities in VMCD Amplifiers

Quantifying the nonlinearities causing TX-to-RX band noise contamination involves identifying nonlinearities in the amplifier though the use of both laboratory tests and simulations. The tests and simulations are designed to isolate and quantify the contribution of each type of non-ideality to total nonlinearity in the amplifier system. This work will use the VMCD CMOS amplifier discussed in the last section as a reference point. This amplifier will then be improved using insight gained from the tests and simulations. Wherever possible, simulations are validated with measured data. Although, the specific techniques are rooted in this example amplifier design, the approach is extendable to other designs.

4.1. Delta-Sigma Driven VMCD Amplifier Simulations

Simulating amplifier spectra in response to delta-sigma inputs is a difficult task. Simulation methodologies used in typical amplifier designs such as linear AC analysis and S-parameters are of limited use in switching amplifier designs due to the nonlinear operating region of the switching amplifier. More advanced simulations used in periodic switching amplifier design, such as harmonic balance and envelope simulations, are useful for predicting switching amplifier efficiency, and tuning the RF waveforms, but offer little insight into the aperiodic delta-sigma spectral response. Transient simulation can effectively model the delta-sigma driven system but are too computationally intensive to result in output sequences extensive enough to provide meaningful spectra.

In this work, a fixed time-step transient simulation technique was developed. The amplifier system (in this work, the VMCD) is broken into differential equations modeling the ideal switches interacting with the passive components. These continuous-time differential equations are solved with a fixed time-step using the Bogacki-Shampine method for numerically solving differential equations. This simulation method has the advantage of being much more computationally efficient than a variable time-step transient simulation performed in a traditional circuit simulation system.

The total simulated sequence length is determined by available memory. Step size trades off spectral resolution with simulation error and stability. Longer simulation time steps result in finer spectral resolution, due to the increased amount of time captured in the simulation. On the other hand, a finer simulation time step decreases the amount of error created by the numerical differential equation solutions. Fundamentally, the time

step needs fine enough time-resolution to capture the transient response of the modeled differential systems. Failing to do so will result in unstable simulation system outputs.

In this work, most of the simulations use around fifty time slices per delta-sigma period. This works out to roughly 125,000 samples per chip in a QPSK simulation. At the time of writing, standard computers can simulate a few dozen chips, effectively capturing the spectral response of the nonlinearities to be discussed.

4.2. Asymmetrical Slew Rate Non-Idealities

Asymmetrical slew rate limitations can cause nonlinearities in delta-sigma systems. Symmetrical slew rate limitations alone do not cause nonlinearities, provided the slew rate is sufficient that the output voltage reaches the desired final value. As a starting point, though transient simulation, the slew rate limitations of this VMCD amplifier system are quantified.

The full VMCD amplifier is simulated with a transient simulation performed in Advanced Design System (ADS) using the CMOS device models provided by the manufacturer. The drive signal is the same delta-sigma pattern used in the laboratory measurements. To visualize the output of the transient simulation, an eye diagram of the output voltage is constructed by over-plotting the output signal with a time constant of three delta-sigma time periods. The eye diagram of the amplifier digital output, at the switching devices, before the resonator, is given in Figure 6:

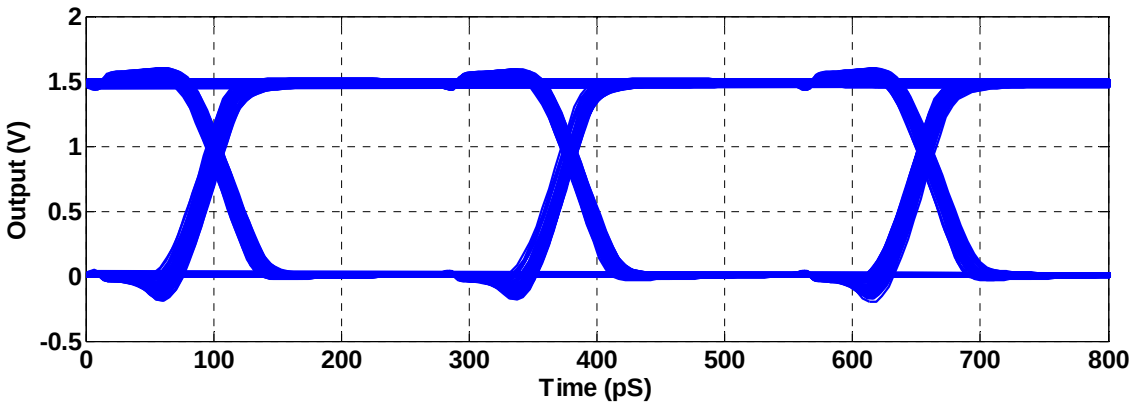

Figure 6: Simulated output transient response of the VMCD amplifier, over-plotted to form an eye diagram.

This over-plotting at a sample rate submultiple of the digital switching rate allows the different transitions to be compared visually. This can be extended to the time-derivative of the above signal to a slew-rate eye diagram given in Figure 7:

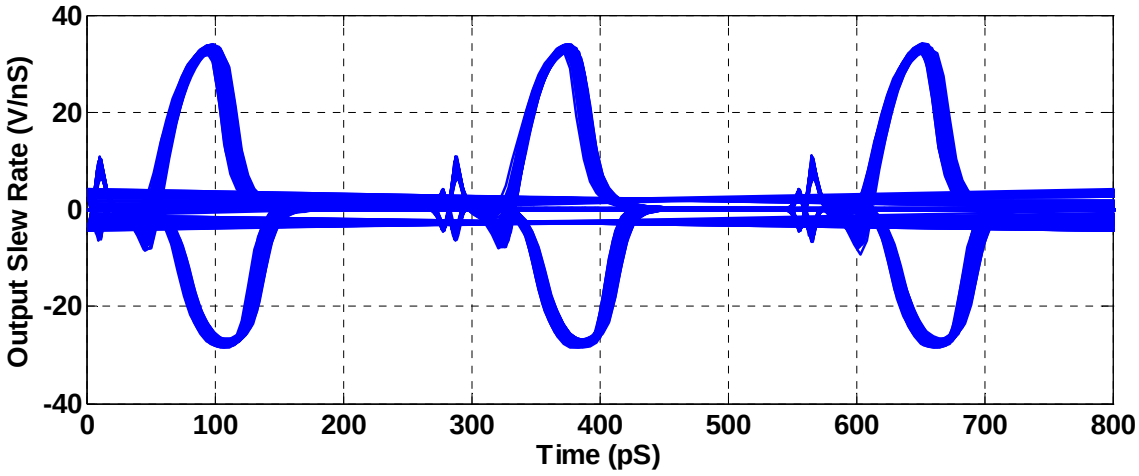

Figure 7: Slew rate eye diagram constructed by over plotting the derivatives of the voltage transitions.

This transient simulation is too computationally complex to be performed for a simulation time long enough to result in a useful spectrum, so the rise/fall times are extracted from the full transient simulation, and used later in the fixed time-step simulation environment to result in a usable spectrum.

However, it is important to first quantify that symmetrical slew rate limitations alone do not have a significant spectral effect below the Nyquist frequency. A delta-sigma signal was subjected to more than twice the symmetrical slew expected from this system, as shown in the time domain plot of Figure 8:

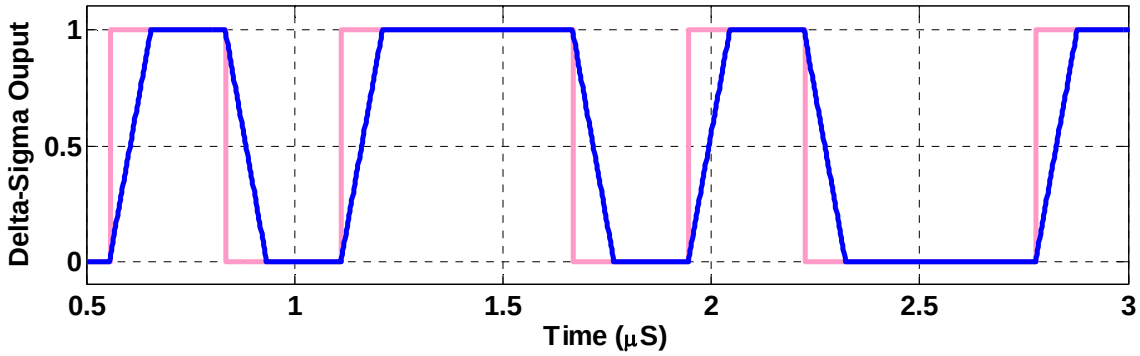

Figure 8: Example of severe symmetrical slew applied to test delta-sigma signal.

Using a much longer sequence than is shown above and subsequently running a power spectral density estimate, results in the following spectra:

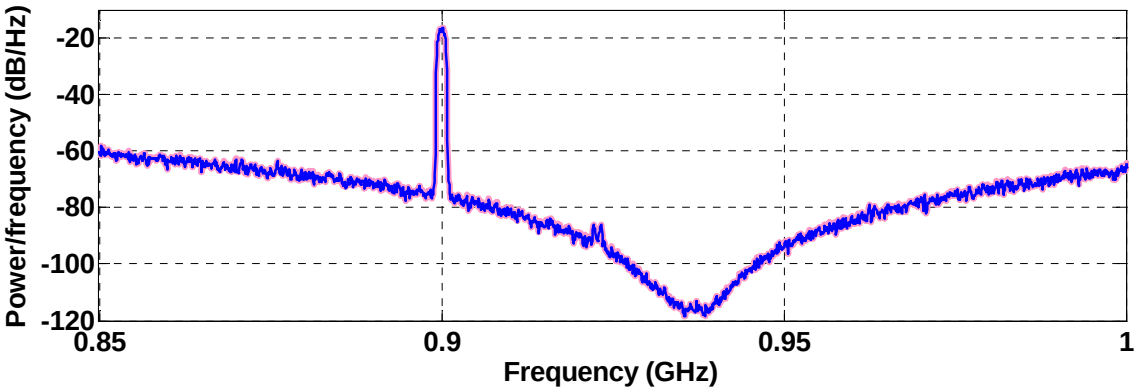

Figure 9: Simulated delta-sigma with symmetrical slew applied (blue) is compared with an ideal, no slew signal (light red) (40 GHz sampling rate, 10 V/nS rise/fall, simulated for 1 mS). The input signal plotted with a thicker pen to enhance visibility.

Running this simulation we can see no degradation in the delta-sigma signal, due to the fact that the slew rate is sufficient to reach the final value in every switching case, and the

slew rates are symmetrical. Rerunning the simulation with the non-symmetrical slew values from the transient simulation results in small, but noticeable degradation in Figure 10:

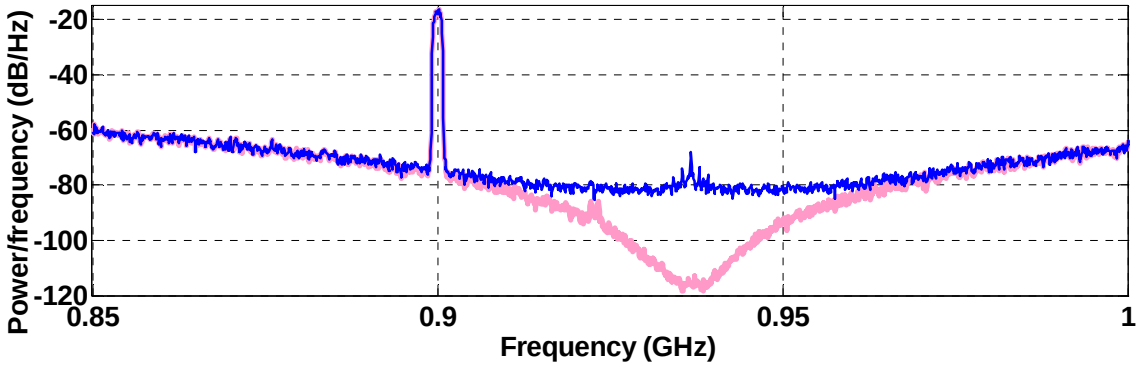

Figure 10: Simulated delta-sigma signal with the asymmetrical slew applied (blue) compared with the measured amplifier results (light red). The asymmetrical slew applied is 33 V/nS rise and 27 V/nS fall time.

The spectral degradation predicted for the non-ideal slew rates is small and on order of the degradation caused by the amplifiers in the Agilent 81134A pattern generator.

The slew rate of an amplifier connected to a frequency tuned load cannot be directly measured, as the output slew rate of the amplifier is determined by the resonances of the tuned output. Specially designed period test sequences can extract slew rate data by exciting intermodulation products proportional to the asymmetrical slew in the amplifier. Periodicity in the test sequence is necessary, because aperiodic signals can exercise other classes of nonlinearities. The sequence also needs to be two-state, to properly drive the switching amplifier.

Such a periodic test signal consists of a square wave that reverses polarity periodically. Asymmetrical slew rates will cause intermodulation products to form in-between the expected signal harmonics. These intermodulation products, or error tones,

are proportional to the asymmetrical slew rate of the amplifier. Faster rates of phase reversal will increase the amplitude of the error tones generated, but will result in a higher bandwidth test signal. The reversal rate needs to be chosen such that the error tones are in the pass-band of the output filtering and matching of the amplifiers, while having sufficient amplitude to be above the noise floor of the spectrum analyzer.

The test signal used for this VMCD amplifier is a 900 MHz square wave, reversed every 100 cycles (i.e., at 9 MHz). The test signal simulation, using the rise/fall time of the amplifier, predicted the spectrum shown in Figure 11:

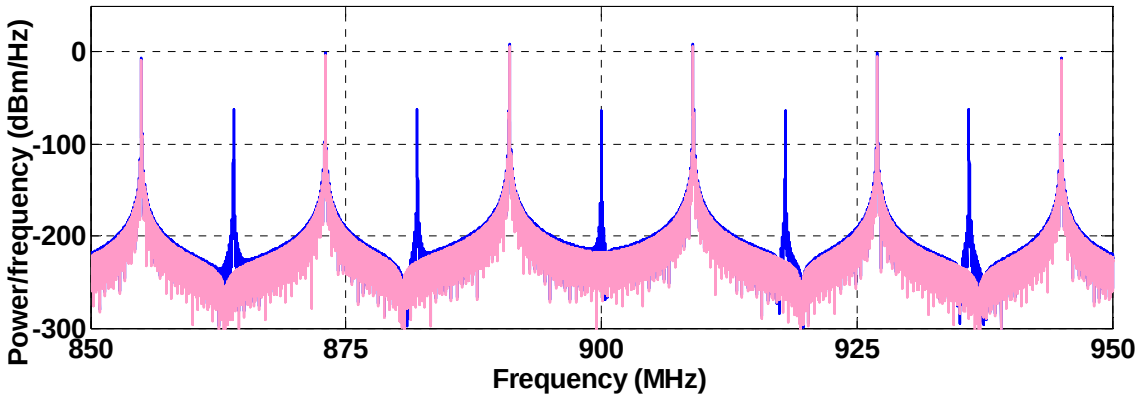

Figure 11: Simulated spectra of phase reversal signal (dark blue) with a 24V/nS rise time and 28 V/nS fall time. Shown with spectrum of ideal phase reversal signal with no slew impairment (light red). The ideal signal is drawn over the output signal to facilitate comparison.

The test pattern was then loaded into the pattern memory of the 81134A and input to the VMCD amplifier, and the following spectrum was measured:

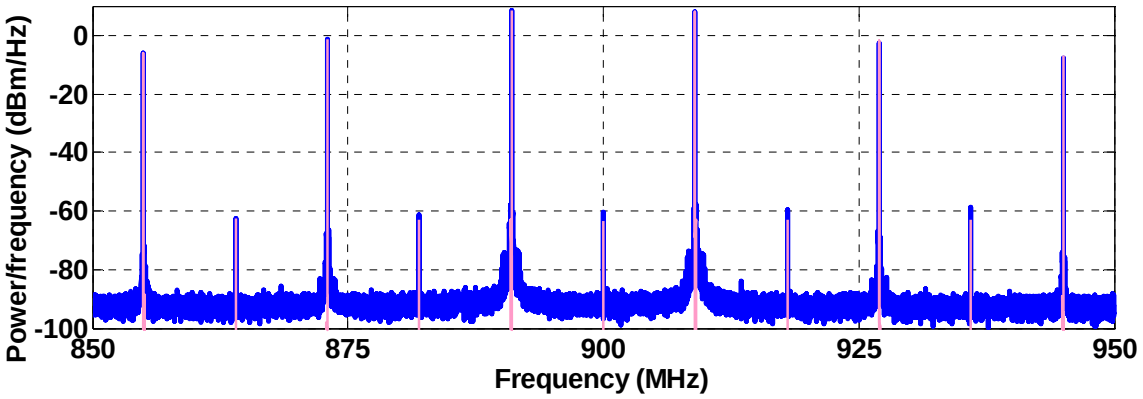

Figure 12: Measured phase reversal signal output (dark blue) shown with spectrum of slew simulation (light red). Spectrum of the measured output is shown in thicker pen to facilitate comparison.

The measurements show that the actual slew rate mismatch is very close to the values predicted by the simulator. Thus, the slew rate mismatch of this VMCD amplifier is is not responsible for the majority of the signal corruption observed.

4.3. Mismatched On-Resistances

Mismatched on-resistances of switching devices in a VMCD amplifier can cause nonlinear behavior when switching nonperidically. Consiter the following VMCD circuit diagram:

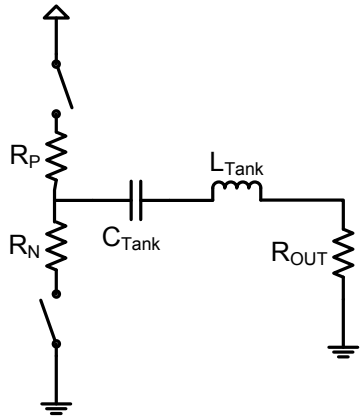

Figure 13: Simplified VMCD amplifier schematic diagram emphasizing mismatched on-resistance ($R_P \neq R_N$).

In the simplest case, the current through the series LC tank circuit closly resembles the desired QPSK comminication signal, and the CMOS devices switch according to a delta-sigma modulator. On-resistance changes with the delta-sigma switching signal, and essentialy mixes with the current though the LC circuit. In effect, the delta-sigma signal is mixed with a filtered attenuated version of itself.

The on-resistance delta was measured by using a network analyzer to examine the output of the fabricated amplifier, with a DC value used to hold the output stage in both a high and a low state:

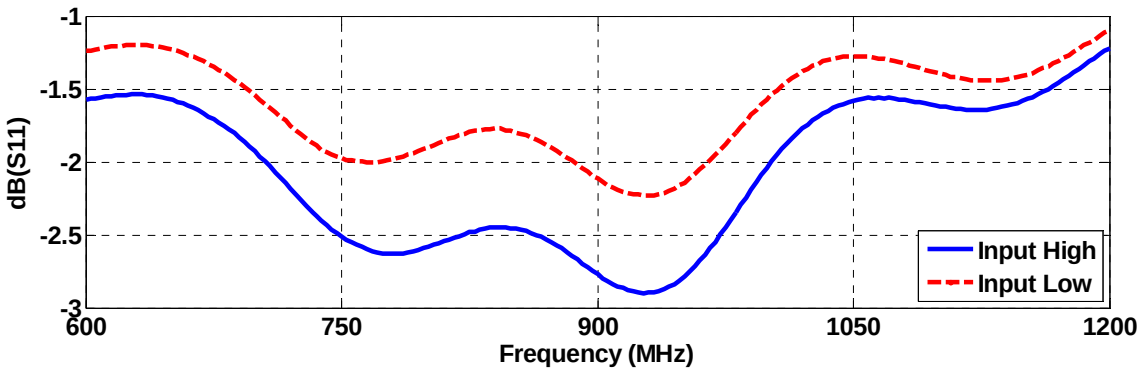

Figure 14: S-parameter measurements looking into the output of the amplifer.

This measurement shows that device matching is not perfect. Simulations show that a 0.6 dB difference in S11 corresponds to about a 7% mismatch in on-resistance through the output resonator and matching network. Using the provided models from the manafacturer, an on-resistance of 2.86 Ohms for the PMOS and 2.61 Ohms for the NMOS were calculated. These values were then simulated using a VMCD model consisting of ideal switching devices, except for the mismatched on-resitances. The matching circuitry is also included to more accuratly match the currents expected in the real VMCD amplifier.

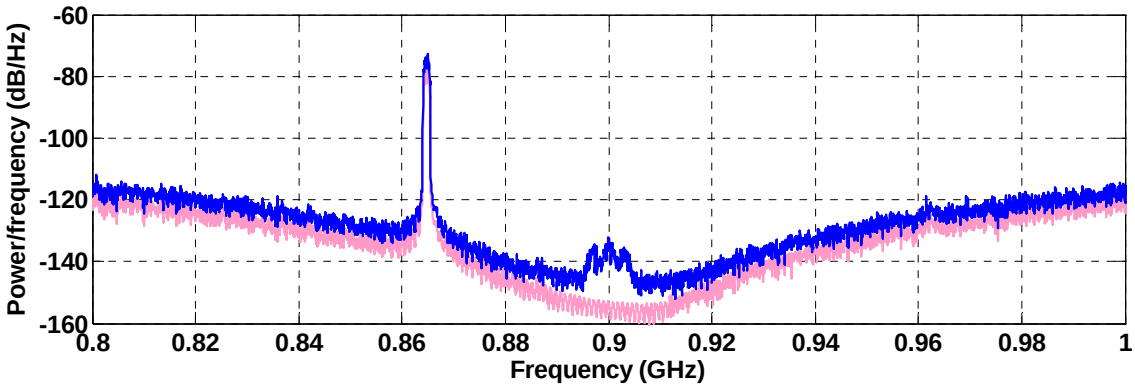

Figure 15: Simulation of VMCD amplifier with a mismatched on-resistance amplifing a delta-sigma encoded CDMA signal. Amplifier input (light red) is shown along with the output (dark blue).

Again, the amount of spectral degradation is orders of magnitude less than the total degradation from measured data, suggesting mismatch is not the root cause of the degradation.

To further validate the aobve simulations, an aperiodic test pattern was created to further reduce the broadband noise created by mismatched on-resistance while still exercising other nonlinearities. A band-pass delta-sigma signal was created consisting solely of quantization noise. This was done by running a delta-sigma modulator with no input. In order to stablize the delta-sigma system, the amount of dithering needs to be almost the entire span of the quantization step. Since the quantization-noise-only signal has little power in the resonance of the LC tank, the current through the tank will remain small. The small tank current minimizes the noise generated by the on-resistance mismatch, while still retaining many other properties of the delta-sigma sigmal. The quantization-noise-only signal was first simulated, resulting in Figure 16:

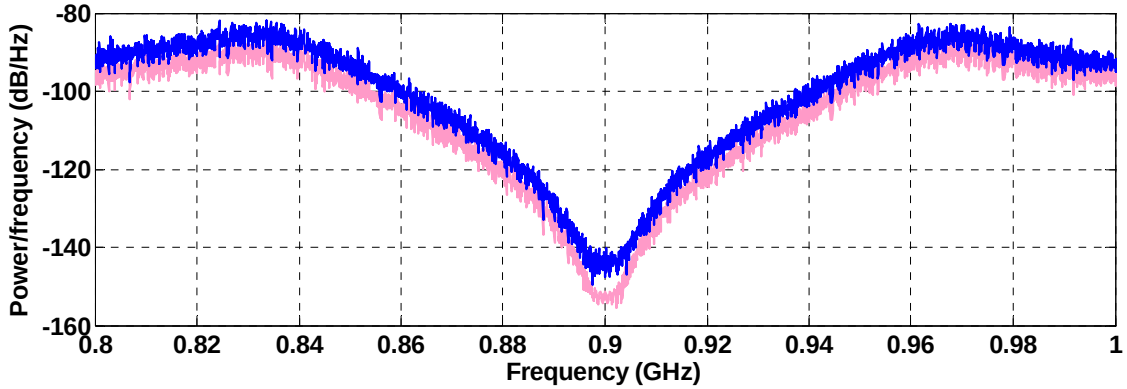

Figure 16: Simulation of VMCD amplifier with a mismatched on-resistance amplifing a delta-sigma quantiaztion-noise-only signal. Amplifier input (light red) is shown along with output (dark blue).

However, amplifiying this noise-only signal in the laboratory with the VMCD amplifier still results in a badly corrupted spectrum:

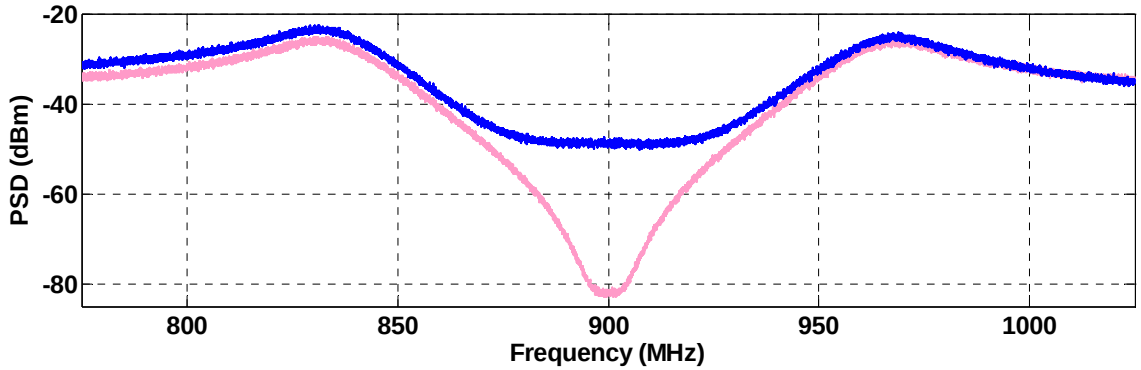

Figure 17: Measured amplifier input (light red) and output (dark blue) with a quantization noise only signal.

This result confirms the earlier simulation and S-parameter measurements, with the conclusion that the majority of nonlinearity in this amplifier is not caused by device on-resistance mismatch.

4.4. Supply Memory

All amplifiers have parasitic inductance between the supply and the actual switching devices. Typically this is mitigated by supply bypass capacitors. In linear amplifier designs, the supply ripple is further attenuated by the power supply rejection ratio (PSRR) of the amplifier. Since the active devices in a linear amplifier are not fully turned on, their inherent PSRR is quite high. The opposite is true in the case of switching amplifiers. Striving for high efficiency, switching amplifiers are designed to have as little voltage drop across the devices as possible. This causes the amplifier to have little or no inherent PSRR. When amplifying simple periodic or constant envelope signals, the supply ripple has little or no effect on the output signal. Since the switching events occur periodically, at the same period of time, even when supply variations are caused by switching currents, the amplifier encounters the same supply voltage at every switching event. Also, at a longer time average, the power demanded from the supply is constant, so the supply inductance has minimal change in voltage drop, and thus little effect on the output signal.

When used to amplify aperiodic, non-constant-envelope signals the opposite is true. The supply voltage and current will tend to vary with the instantaneous switching frequency. The variation is made worse by the combination of the output resonator and output matching typically employed. With the goal of high efficiency, the output circuitry is designed to accept in-band power from the amplifier, and reflect back out-of-band power.

4.4.1. Simulation

The following VMCD schematic will be used in the supply memory simulations:

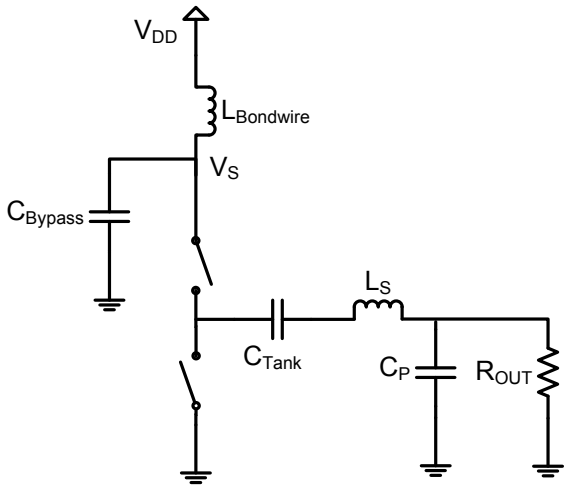

Figure 18: Simplified VMCD amplifier schematic with bondwire/supply inductance.

Using the simulator to simulate the above circuit with the corresponding values from the actual designed amplifier (C_{Bypass} = 30 pF, $L_{Bondwire}$ = 0.5 nH, C_{Tank} = 21.6 pF, LS = 5.5 nH, C_P = 7 pF, and R_{OUT} = 50 Ohms) results in the following time domain diagram:

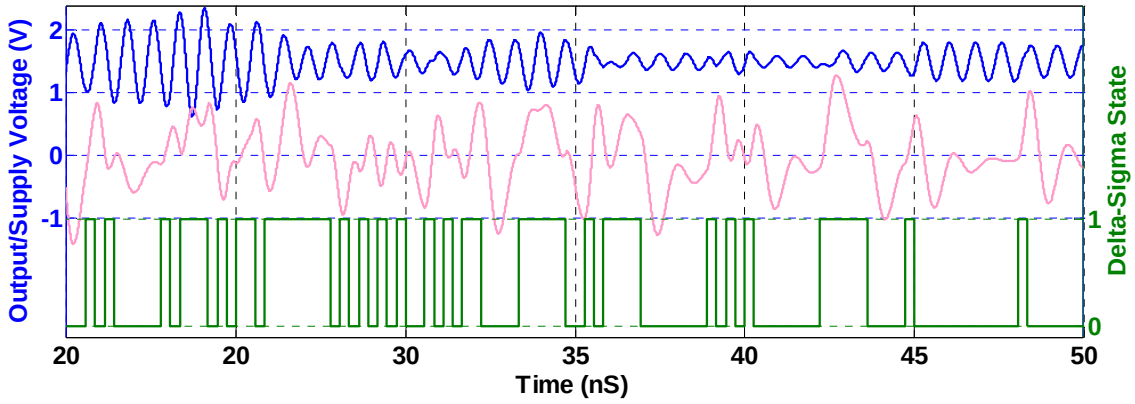

Figure 19: Time domain simulation of circuit in Figure 18. Bottom is delta-sigma drive signal (green), middle is the output voltage (light red) and top is V_S (blue).

The simulation shows a significant supply ripple. A longer sequence was generated using the simulation. Comparing the output of the simulation spectrally to the measured data from the amplifier shows an excellent match, as shown in Figure 20:

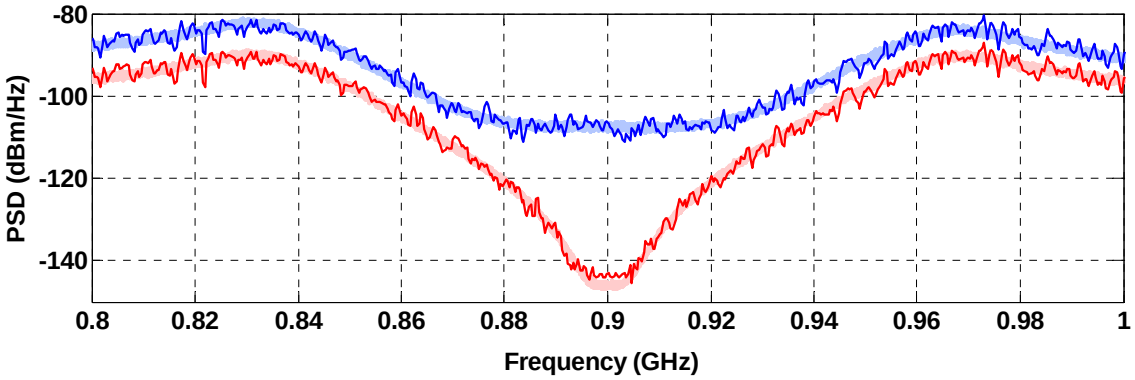

Figure 20: Spectra of both simulation (dark lines) and measurement (light lines) for the quantization-noise-only signal. Both ouput (top in blue) and input (bottom in red) is shown. The power is normalized to account for resolution bandwitdh differences, and cabling losses.

The supply capacitor resonantes with the bondwire inductor. This exacerbated by the fact that the output resonator and matching network only dissipate in-band power. During out-of-band switching events, current is delivered back to the supply, causing the LC ciruirt formed by the supply/bondwire inductance and the bypass capacitor to resonate. Another potential issue is that the bypass capacitors in this particular VMCD amplifier were designed as high-Q metal-insulator-metal (MIM) capacitors, providing little damping for such resonances.

4.4.2. Analysis

The simple circuit shown in Figure 21 is analytically modeled to give insight into nonlinearities caused by supply memory:

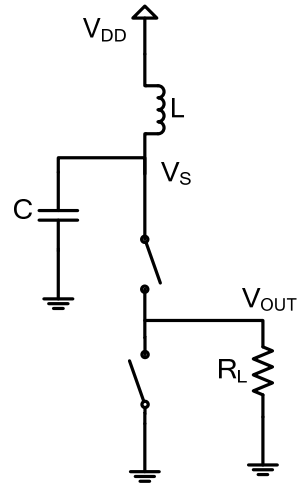

Figure 21: VMCD circuit used in hand analysis of supply memory.

The output of the amplifier is ideally the multiplcation of the delta sigma sequence (here, ones and zeros) with the voltage avalible at the switching device (V_S):

$$V_{OUT}(t) = \Delta\Sigma(t) \times V_s(t) \tag{1}$$

V_S is slightly more complex, but basically a filtered and delayed version of the delta-sigma signal itself:

$$V_s(t) = V_{DD} - L\frac{d}{dt}\left[C\frac{d}{dt}V_s(t) + \frac{\Delta\Sigma(t) \times V_s(t)}{R_L} \right] \tag{2}$$

This can be further analyzed by breaking the equation apart in to the two cases where, first, the delta-sigma signal is a zero:

$$V_s(t) = V_{DD} - L\frac{d}{dt}\left[C\frac{d}{dt}V_s(t) \right] \tag{3}$$

Secondly, where the delta-sigma signal is a one results in the following:

$$V_s(t) = V_{DD} - L\frac{d}{dt}\left[C\frac{d}{dt}V_s(t)\left(1+\frac{1}{R_L}\right)\right] \tag{4}$$

This simplification allows solving each of the separate differential equations. When the input state is at zero, the supply available to the VMCD is an undamped (for an ideal inductor) sinusoidal oscillator:

$$V_s(t) = V_{DD}\frac{1}{\sqrt{LC}}\sin\left(\frac{1}{\sqrt{LC}}t\right)u(t) \tag{5}$$

When the delta-sigma output is at one, the output (and available supply) is a damped sinusoidal oscillation.

$$V_s(t) = V_{DD}\frac{4{R_L}^2C}{L+4{R_L}^2C}e^{\frac{t}{2R_LC}}\sin\left(\sqrt{\frac{1}{LC}+\frac{1}{4{R_L}^2C^2}}t\right)u(t) \tag{6}$$

The amplifier would flip-flop between the two states defined by the above equations, and the initial conditions would be passed between the states. This is the fundamental nonlinear memory effect: a two-state system where the state values have a history dependence. Aruguably, this is an oversimplifacation of the problem, but solving the full system of nonlieanrities obscures intuitive insight into the problem.

5. VMCD Amplifier Redesign

The insight gained from the identification and analysis of the amplifier defects was used to design a second version of the VMCD chip. In order to validate the previous analyses, the only major change was a complete redesign of the power supply and power supply decoupling networks. Other important parameters were held constant; the new chip was built using the same CMOS process, and shared the same schematic diagram.

5.1. Simulations and Design

The fixed-step simulator presented earlier was used to perform parametric simulations to determine the effect of increasing the supply bypass capacator:

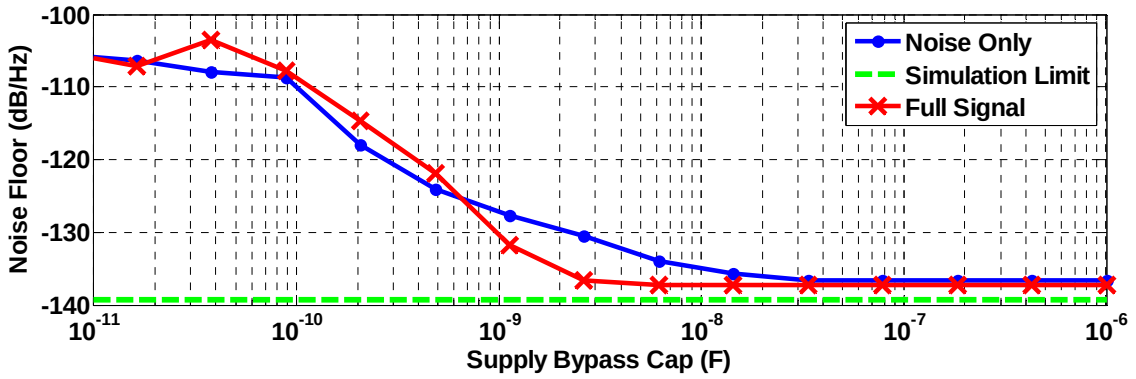

Figure 22: Simulation of noise floor vs bypass capacitor size. Shown with simulation mimumum (dotted line). Supply inductance is set at 0.5 nH and Capacator Q is set at 45.

Unfortuantly, in order to bring the noise floor of the simulated amplifier output to the level of the accuracy of this simulaiton, which is still about 30 dB above the actual RX band noise target, a supply decoupling capacitor of 5 nF was required. In a 0.18 µM CMOS process, with all layers used as capacitance (i.e., MOS capacators layered under MIM capacitors), about 12 fF/µm^2 can be achieved wihout wiring and maximum capacitor size design rule overhead. Talking into account some wiring overhead, the capacitor alone would be amost 1mm on a side. With the process area allowed for the circuit, and after fitting the active devices the wiring overhead, 1.2 nF of decoupling capacitance was fit onto the die area.

In order to further supress supply ripple, the capacitors can be designed with higher series resistance to lower the Q factor of the oscillations and thus dampen them. A

simulation was setup to quantify the effect of the decoupling capacitor Q on the system nonlinearity:

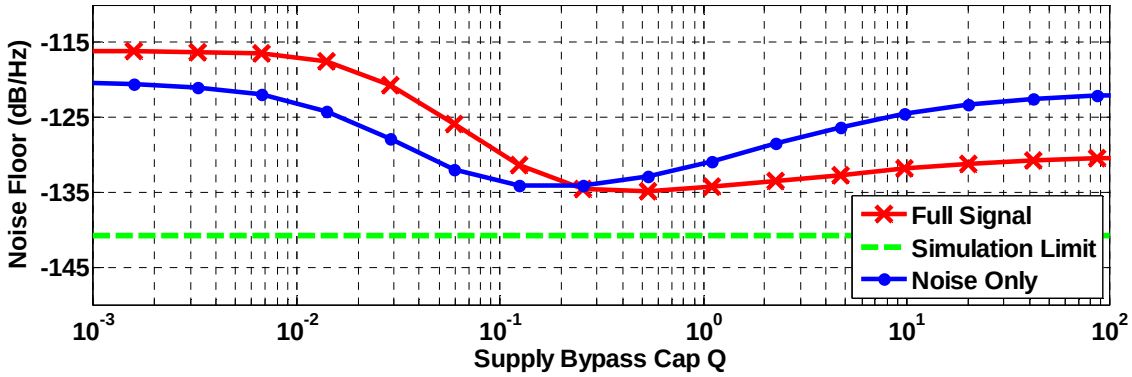

Figure 23: Simulation of a VMCD with 1.2 nF bypass capacitor with a supply inductance is set at 0.5 nH.

While reducing the capacitor Q helps, it is no substitute for larger capacitors. In this design, the MOS capacitors were connected normally due to the inherant polyslicon resistivity. The MIM capacitors were connected with a sparse via matrix to inhance series resistivity while adding minimal series inductance.

5.2. Chip-on-Board

Both the printed circuit board and pad frame design focused on lowering the parasitic inductance of the power supplies to the chip. Figure 24 shows the chip-on-board connections:

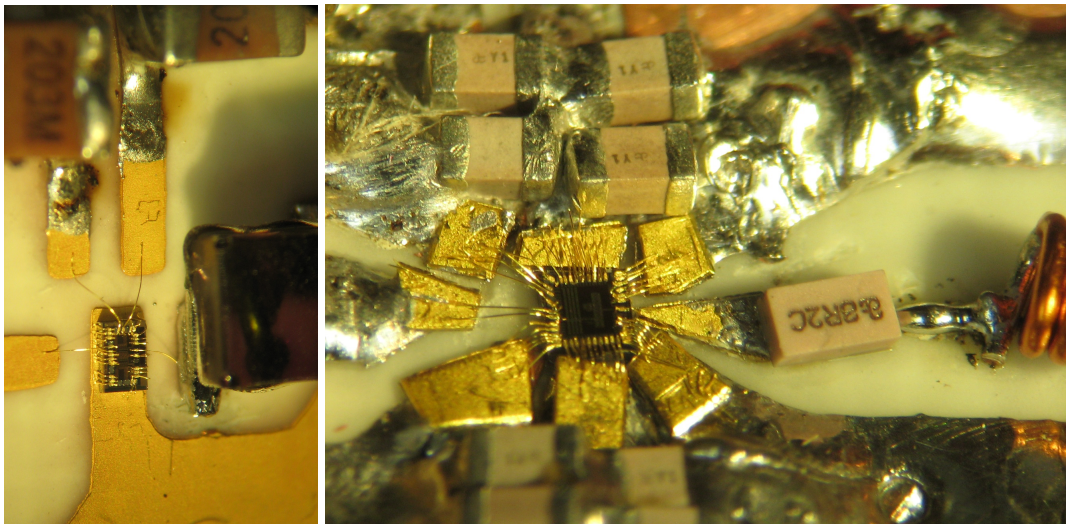

Figure 24: Microphotographs of old (left) and new (right) amplifier and respective chip-on-board components. The series capacitor is off-chip in the new design.

Ground pads are placed at all four corners of the pad frame, and two rows of supply bond pads were placed on the top and bottom of chip. The PCB was designed to minimize supply inductance and bring the decoupling capacitors as close as possible to the chip. The bond landing pads were elevated in order to minimize bond wire loop height.

5.3. Spectral Measurements

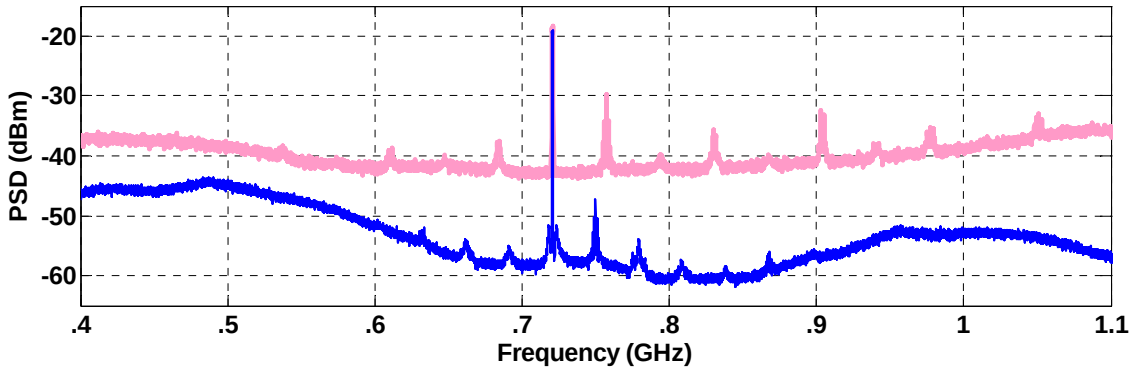

Figure 25: Measured output spectra of the new VMCD amplifier design (bottom dark blue). A frequency shifted version of the old VMCD output spectrum (top light red) is shown for dynamic range comparison.

The new VMCD amplifier design resulted in a 15 dB reduction of the broadband noise. The reduced broadband noise also raised both the efficiency and output power of the amplifier. Even with the reduced supply inductance and increased damped decoupling capacitance, the supply memory nonlinearity is still the dominate nonlinearity causing broadband noise generation.

6. Conclusion

This chapter introduced unique nonlinearities inherent to a class of amplifiers that are driven by quantization algorithms utilizing noise shaping. The nonlinearities were extensively simulated using a fixed-step transient simulator developed for this work. Novel test techniques were developed to differentiate the different types of nonlinearities in amplifiers without having access to on-chip internal signals. Power supply ripple was found to be the dominate source of noise.

Reducing the supply ripple by a combination of both reducing supply inductance and increasing decoupling capacitance achieved a significant, but not sufficient, noise

reduction and is thus not a realistic way of creating a delta-sigma VMCD that can meet the RX band noise specification. In order to create a digital transmitter for a full duplex communication system, finding an encoding algorithm where noise generated by amplifier nonlinearities is placed outside the receive band is necessary.

7. Acknowledgments

The amplifier used in this chapter's measurements was based on a design first used in [3]-[4]. The author would like to thank Jazz Semiconductor for CMOS mask space and CAD support.

8. References

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[2] 3rd Generation Partnership Project "User Equipment (UE) radio transmission and reception (FDD)." 3GPP specification: 25.101; Technical report, 2008.

[3] T.-P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "Design of H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," in *IEEE Trans. on Microwave Theory & Tech.,* vol. 55, iss. 12, pp. 2845-2855, Dec. 2007.

[4] T.-P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," in *2007 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1091-1094, June 2007.

Chapter 6

Band-pass Pulse Width Modulation Applied to Microwave Transmitters

1. Introduction

In this chapter, the applicability of pulse with modulation (PWM) as an encoding algorithm for microwave transmitters is investigated. A modification allowing PWM to reproduce communication signals with clock rates equal to that of the transmit frequency is presented. Unique time-quantization issues pertaining to simulation PWM signals with finite time-steps are addressed with a frequency domain simulation technique. A novel circuit, based on a delay locked loop (DLL) that serves as a digital-to-time converter, is introduced. The circuit generates digital transitions unaligned with a timing clock, with a high degree of accuracy. Lastly, amplifier measurements are made that demonstrate the benefits in efficiency and reduced broadband noise that RF PWM transmitter systems have over delta-sigma systems.

2. Pulse Width Modulation

PWM is one of the most commonly used encoding algorithms to drive switching amplifiers in low frequency class-S systems. PWM is simple to implement, is well suited to efficient amplification, and separates the quantization noise relatively far from the desired signal with a relatively low switching rate. PWM achieves very high in-band power ratios for a given peak-to-average ratio. All of these properties make PWM a prime candidate for a microwave transmitter.

In is most basic form, PWM creates pulses at a fixed repetition rate, with a duty cycle (or width) which varies proportionally to the desired amplitude. The pulse repetition rate is referred to as the PWM rate or PWM frequency. An example of the PWM signal and the analog signal it represents are shown in the time domain in the following figure:

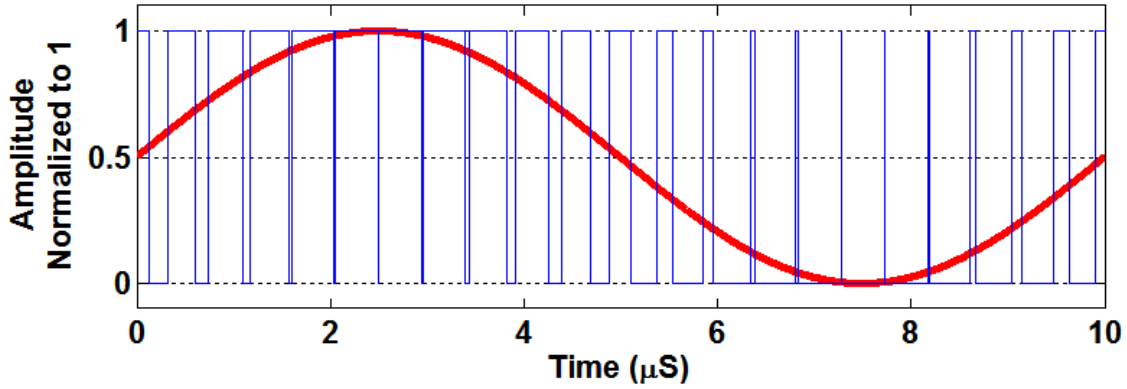

Figure 1: Example of basic PWM waveforms. A 100 kHz sine wave is encoded at a PWM frequency of 2.2 MHz. The frequency plan was chosen to maximize the visual demonstrability.

With PWM, assuming the signal to be encoded has a bandwidth much less than the PWM rate, the resulting encoded signal spectrum will be identical to the original signal from DC through the occupied signal bandwidth. The encoded signal has a quantization noise spectrum that is replica free all the way up to a harmonic at the PWM frequency. The quantization noise generated by PWM is contained in this and subsequent harmonics. These quantization noise signal replicas are produced at every harmonic of the PWM frequency, with increasing bandwidth. The increasing bandwidth causes the quantization noise harmonic to seem to smear with increasing frequency. This smearing is evident in the example spectrum to be presented in section 3.

This low-pass spectral characteristic of PWM is not desirable for generating communication signals. In order to achieve acceptable SNR characteristics, the PWM rate must be chosen to be a multiple of the carrier frequency; as a result, the required PWM rate is unrealistically high for microwave applications. Fortunately, a simple modification to the PWM algorithm makes it suitable for higher frequency, band-limited signals.

3. Band-Pass Pulse Width Modulation

Band-Pass Pulse Width Modulation (BPPWM) extends the original idea of PWM by setting the pulse repetition rate to the carrier frequency of the desired signal, making the pulse rate much lower than in the PWM case to reproduce a narrowband microwave signal. Furthermore, the phase of the pulses is varied in accordance with the phase of the desired RF signal. The duty cycle is now limited to 50%, as this achieves the maximum RF power at the fundamental frequency. The pulses are still quasi-periodic, but now the centers of the pulses vary slightly from pulse-to-pulse in accordance with the input signal phase. An example of a BPPWM signal waveform is given in Figure 2:

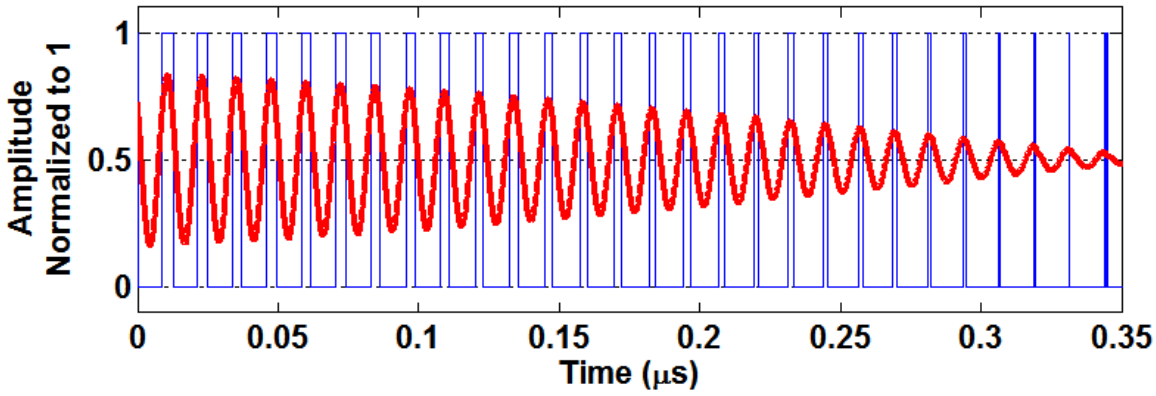

Figure 2: Example BPPWM waveforms (thin blue). The input is a QPSK signal (thick red) at a chip rate of 1.25 MHz, on an 81 MHz carrier. The unusually low carrier frequency was chosen to maximize the visual demonstrability by allowing envelope variations to be visible in the small time scale shown.

The amplitude and phase representation of the time-varying signal amplitude is evident, with the pulse widths varying in accordance to the envelope of the signal, and the pulse phases aligned to the signal, such that the centers align with the maximum of the encoded signal.

Spectrally, BPPWM is similar to PWM, except the RF signal is at the fundamental frequency of the PWM clock. The spectrum of the above signal is given below:

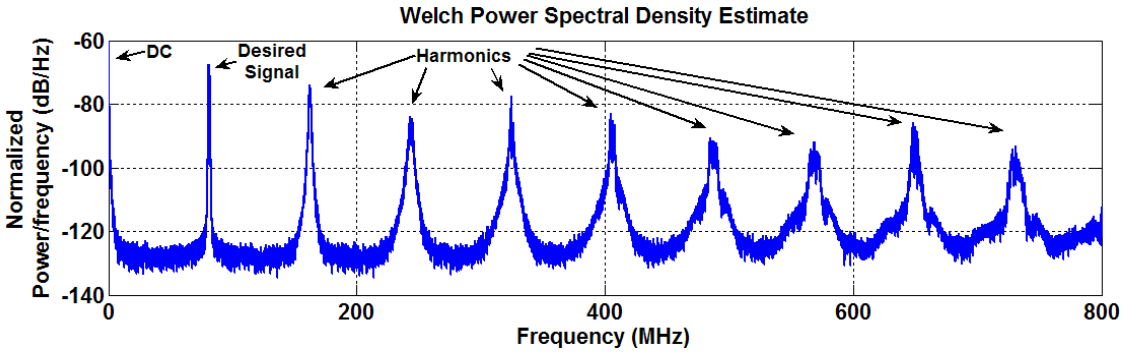

Figure 3: Spectrum of example BPPWM signal shown in the time domain in Figure 2.

Adding phase variation to PWM increases the frequency of the encoded signal from spectrally centered around DC to centered around the PWM rate. Harmonics are produced in a similar manner to PWM. The bandwidth of the higher order harmonics still increases with frequency, causing them to progressive smear as mentioned previously. A noise floor is also present, due to both sampling rate and finite sequence length limitations. Issues pertaining to this noise floor will be examined later in the chapter.

4. Generating PWM/BPPWM signals

In the analog domain, a widely practiced way of generating PWM signals exists. A triangle wave, scaled to the largest input amplitude expected, is generated and fed to the inverting input of a comparator while the desired waveform is fed to the non-inverting input. The comparator outputs a high state when the input is greater than the triangle wave, and outputs a low otherwise. Due to the shape of the triangle wave, the resulting pulse width will be proportional to the input amplitude.

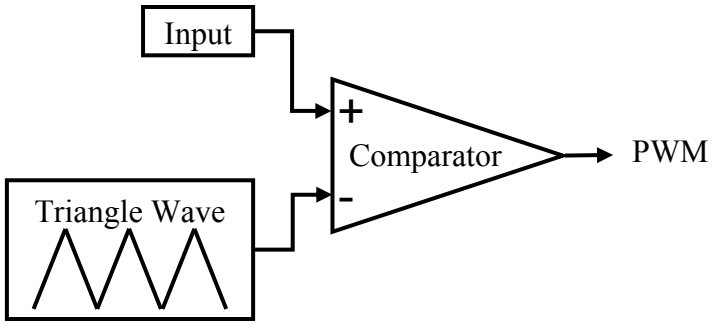

Figure 4: Block diagram of analog PWM generation technique.

This circuit serves as an asynchronous amplitude-to-time converter. A straightforward modification to extend this circuit to generate BPPWM is presented below:

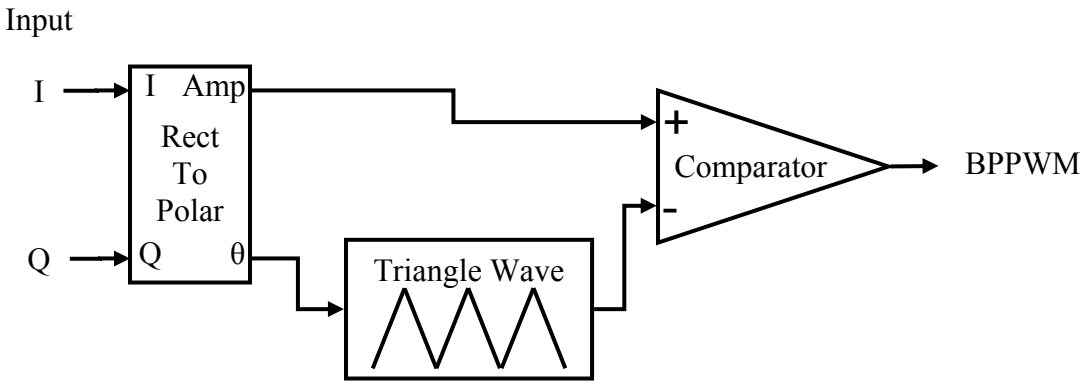

Figure 5: Block diagram of analog BPPWM generation technique.

The analog BPPWM converter is similar to the PWM case, except that there is an added phase control of the triangle pulse, and the triangle wave is scaled to two times the maximum input amplitude. The next sections will explore implementing these architectures digitally.

5. Synchronous Versus Asynchronous PWM/BPPWM

The PWM generation examples discussed up to this point have employed analog circuits to generate asynchronous PWM. Asynchronous PWM can have edges (low-to-

high and high-to-low transitions) occurring at any time. One of the important issues when implementing PWM algorithms in digital logic is that most digital logic systems are synchronous, deriving timing from a fixed clock. These synchronous systems can only produce signals with edges occurring during a clock transition. This imposes a time-quantization factor in the PWM output, effectively rounding the envelope of the desired signal. Envelope quantization adds noise to the signal, and imposes a maximum SNR that can cause signal to fall short of spectral purity specifications [1]. This is also true of simulations representing either asynchronous or synchronous PWM as a time-sampled digital signal.

Several methods of mitigating this time-quantization noise will be presented in the following sections. Since many simulation algorithms use sampled time, and the majority of signal generators have a synchronous output, time-quantization noise in lab setups and simulations is often unavoidable. To minimize the effect of this noise in laboratory measurements and in sampled simulations, algorithms are presented to shape time-quantization noise out of the frequency band of interest. A new PWM simulation technique is introduced that avoids sampling PWM, and thus avoids the quantization noise associated with the sampling. Additionally, new circuit topologies are introduced to perform accurate digital-to-time conversion, allowing PWM transitions to occur in small time-steps calibrated by a relatively slow reference clock.

6. Traditional Digital PWM Generation

Traditional synchronous digital PWM generation closely mirrors the analog topology. A very high clocked, relative to the PWM rate, digital up/down counter is used

to generate a digital equivalent of a triangle wave with a period that is a submultiple of the clock rate. The output is then fed into a digital comparator along with the desired signal. The digital logic implementing this system evaluates once per clock cycle, so transitions can only occur during an evaluation/clock cycle. This is not a problem for the mainstay applications of PWM: motor drives and low-frequency audio. In these applications, CMOS technology allows for clock speeds thousands of times faster than the highest frequency demanded by these applications. However, it is a problem for communication systems, as seen from a representative example, WCDMA. WCDMA requires a minimum five bits of effective envelope quantization to meet ACPR specifications. The clock frequency for synchronous BPPWM necessary to achieve N bits of amplitude resolution for a given transmit frequency, F_C, is:

$$F_{CLK} = F_C \cdot 2^{N+1} \tag{1}$$

Thus, even the lowest frequency commercial cellular band at 825 MHz would require a synchronous PWM generator to be clocked around 50 GHz, a very unrealistic and power hungry clock rate. Developing a circuit architecture that can achieve resolution finer than a single clock period would alleviate the need for such high clock frequencies.

7. Shaping PWM Time Quantization Noise

The very severe time-quantization requirements of synchronous PWM also affect simulations relying on sampled representations of the PWM signal. To enable simulations and laboratory experiments to generate communication signals encoded without near-band quantization noise, an algorithm was developed to spectrally shape the time-quantization noise generated by rounding pulse transitions to the nearest clock

cycle. This algorithm is very similar to delta-sigma, except that the noise shaping loop operates on time instead of amplitude.

The algorithm starts with a pair of desired characteristics for each of the PWM pulses: 1) The pulse width (w_i), a time period proportional to the amplitude of the encoded signal; and 2) a pulse center time (c_i), which corresponds to a series of linearly increasing points, perturbed by a phase signal in the band-pass case. By adding and subtracting one half of the pulse width from the pulse center time, the algorithm generates a pair of values corresponding to the desired PWM transitions, which are the times in which an asynchronous PWM system would create a low-to-high and a high-to-low transition. Typically, these desired transitions would not align exactly with the clock transitions of the synchronous system. A rounding operation (quantizer) then rounds these transitions in time to the nearest possible transition allowed by the system. The difference between the desired transition and the actual, rounded transition is computed. This time-quantization error is then integrated to create a running sum of the time-error in the system. This running sum of the time-error is then added to the next incoming signal amplitude before rounding during its corresponding clock cycle. The algorithm described above is shown in a block diagram below:

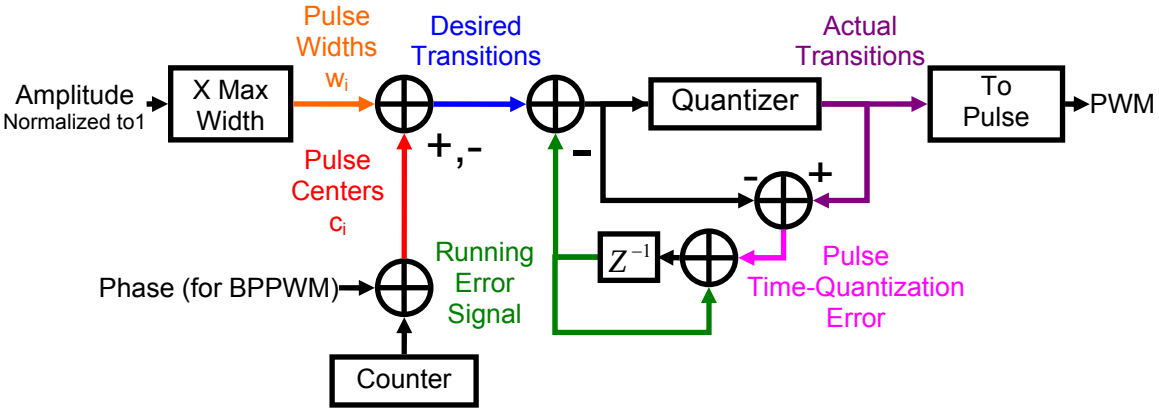

Figure 6: Block diagram of noise-shaped PWM generation algorithm.

To demonstrate the advantages of using noise-shaped time-quantization in PWM generation, a BPPWM QPSK signal was generated using both traditional and noise-shaped algorithms. The signal is similar to IS-95, having a 1.25 MHz chip rate, consisting of pseudorandom chips filtered by a raised cosine filter with a roll-off factor of 0.35. The simulation was performed for 1000 chips at sampling rate of 12.8 GHz. This sampling rate was chosen to correspond to the capabilities of an Agilent 81140A Serial Pulse Data Generator used in the laboratory to drive experimental amplifiers.

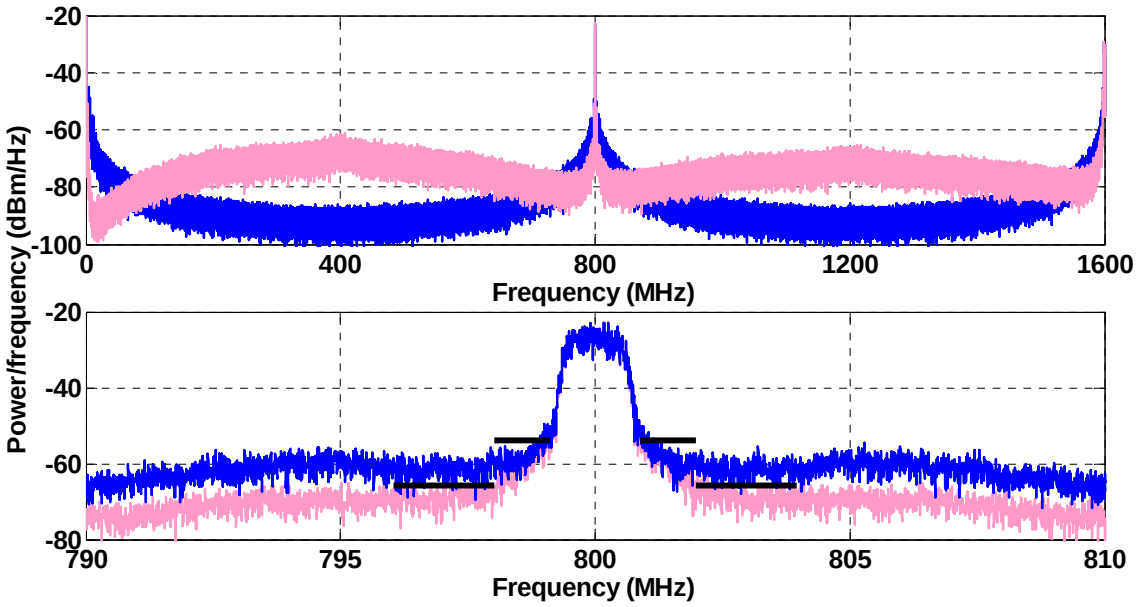

Figure 7: Simulated spectra of synchronous PWM, standard (blue) and noise-shaped (light red), for both wideband (top) and narrowband (bottom). The approximate ACPR limits on the narrowband spectra are shown with black lines. Both signals are digitally sampled at 12.8 GHz (for 8 possible pulse widths).

The wideband spectra show the noise shaping provided by the introduced algorithm. In this case, the noise shaping improves the adjacent channel interference from an unacceptable level to a level where it meets the limits set by the CDMA standard, although this comes at a cost of higher broadband noise. In situations where synchronous PWM signals must be used, the improved ACPR can be a critical advantage. As a separate approach, developing a circuit that allows PWM transitions to occur at very fine time scale could do away with the need to shape the time-quantization noise.

8. Generating Asynchronous PWM/BPPWM Digitally

The basic principle of a direct digital-to-duty-cycle conversion circuit is the technique of performing asynchronous operations on suitably delayed synchronous

signals, where the delay is digitally controlled (with values typically much less than the period of the synchronous signal.) In the example architecture of Figure 8, a PWM signal is generated by taking a clock at one half the frequency of the desired PWM signal and splitting it into two identical signals. These two signals are then delayed by different amounts by two digitally variable delay lines. The resulting signals are then passed to an exclusive-or (XOR) gate, as shown in the block diagram:

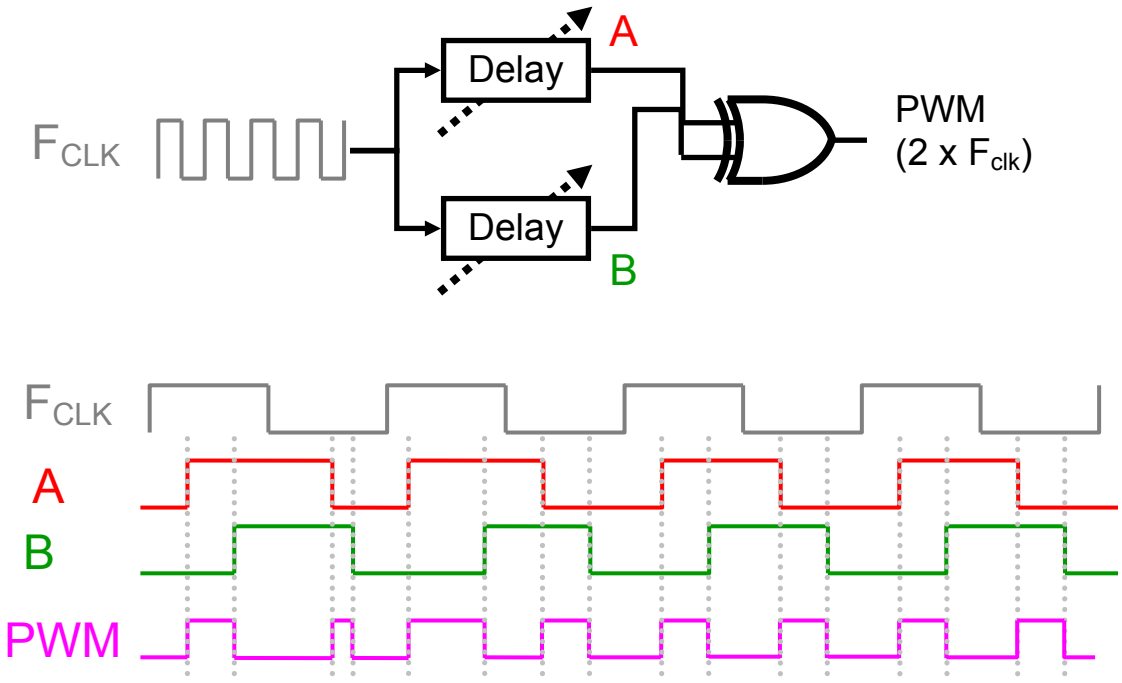

Figure 8: Digital asynchronous PWM generation example. Dotted lines added to emphasize delayed pulse edges of signals A and B.

The major disadvantage of this solution is the fact that realistic variable delay elements do not have very repeatable characteristics; i.e., the delay at a particular setting is affected by CMOS processing, supply voltage, and temperature (PVT) variations. Some of these variations could be calibrated out, but this would have to be done at every possible operating point.

A solution to this problem is to employ a well-known structure called a delay locked loop (DLL) to provide the delays:

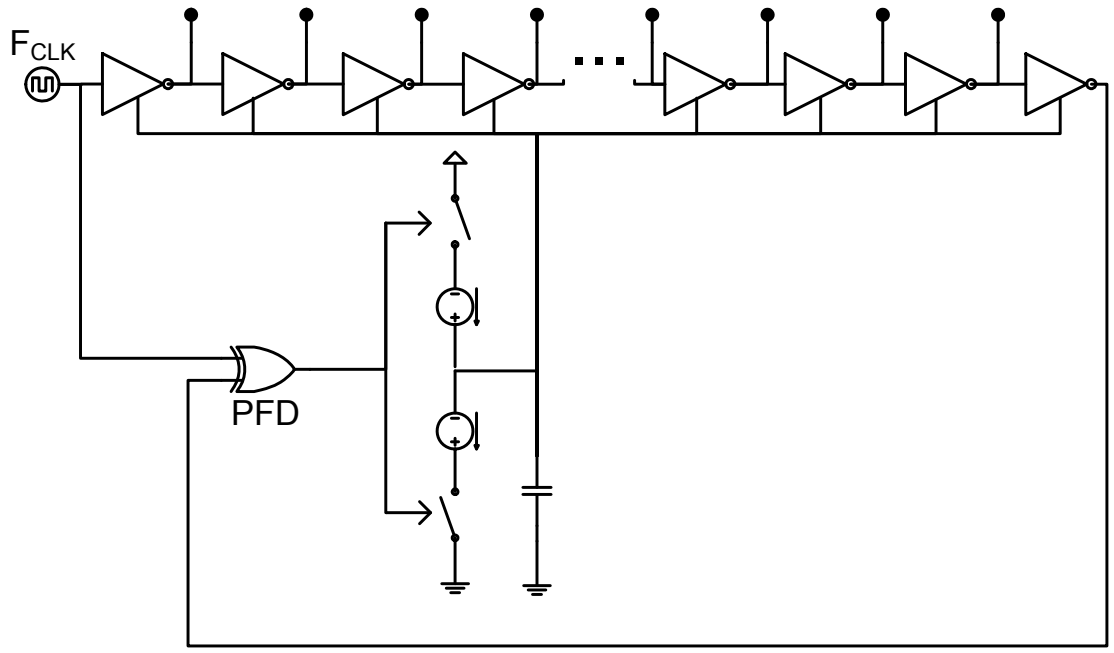

Figure 9: Block diagram of an example DLL with an inverter chain acting as a voltage-controlled delay line.

The delay locked loop is a feedback circuit topology that sets the total delay though a series of variable delay elements to exactly one clock cycle. This delay is enforced by a feedback loop comprising a phase/frequency detector and a charge pump. The phase/frequency detector compares the relative arrival of two clock transitions: one directly from the clock source, and another from the output of the variable delay element. The phase detector then sends adjustments to a charge pump, which in turn drives the adjust inputs of the delay elements. During operation, when the output clock arrives early, the charge pump starves the delay elements, thus increasing the delay. When the output clock is late, the charge pump increases the supply, thus speeding the delay

elements. This feedback regulates the delay of the inverter chain to a one clock cycle delay.

This known delay property of the DLL is leveraged to generate PWM. Assuming the individual delay elements are matched, a reasonable assumption for an integrated circuit, the delays between the individual delay elements will be an even multiple of the fixed total delay. Taps are placed between the delay elements to create a cascade of known equal delays. Digital multiplexer circuits are used to select two different delay taps from the DLL. The outputs of the multiplexers are then passed to an exclusive or (XOR) gate. Selecting different pairs of delays allows control of the pulse width emerging from the XOR gate.

A simplified block diagram is shown below:

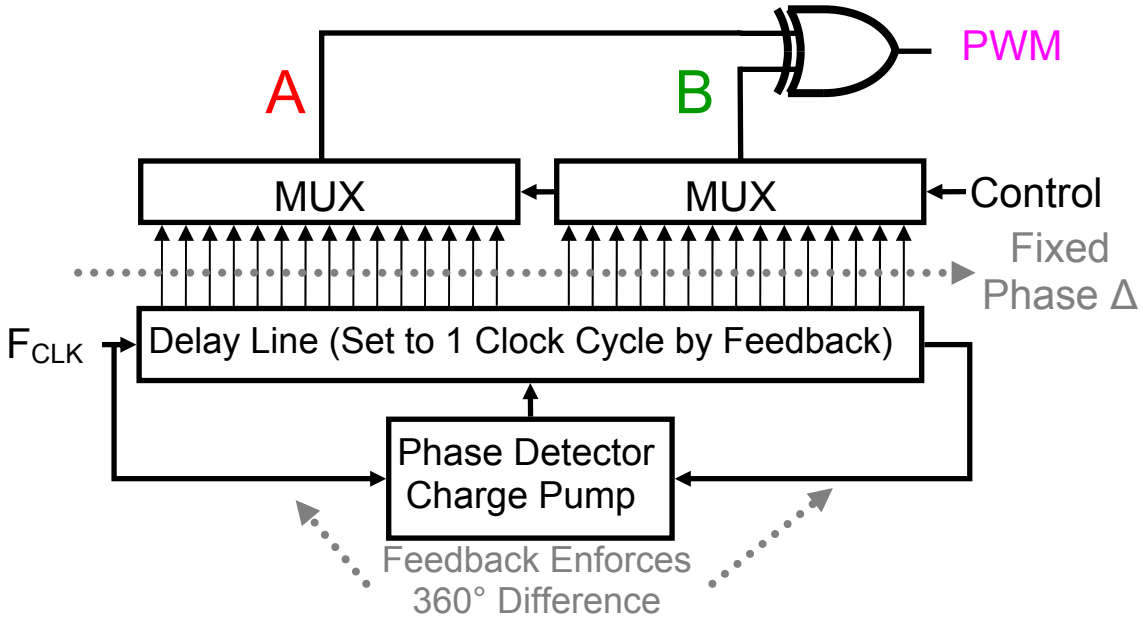

Figure 10: Block diagram of DLL-based PWM generator.

The major drawback of this architecture is that the time resolution is limited by the total number of delay elements. In turn, the number of delay elements is limited by the minimum delay possible for the target technology. Also, increasing the number of delay elements costs power. In order to increase the resolution without having to increase the number of delay elements, a technique called phase interpolation can be used to increase the resolution.

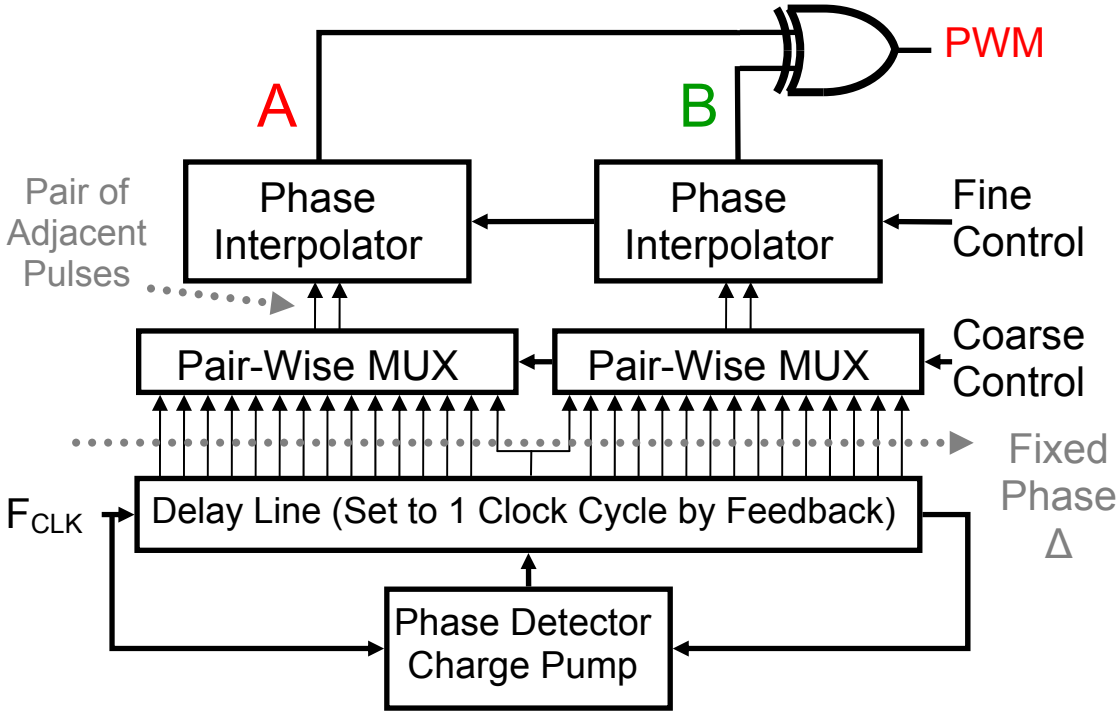

Figure 11: PWM generation with phase interpolation.

Here, two adjacent signals are selected by the pair-wise multiplexers from the delay line on each side, controlled by a coarse digital control. The adjacent signals are then interpolated to generate a third signal that has a phase that is a weighted average of the two adjacent signals. The interpolation is controlled by a fine digital control. Adding the fine control on top of the coarse control increases the maximum resolution possible to the limit imposed by the amount of jitter and the component matching in the system.

With a modification to include phase control of the pulse, these circuits can also be used to generate band-pass PWM. This can be achieved by employing another tapped DLL to phase modulate the incoming PWM clock signal. An alternative architecture

would be to expand the multiplexers across the entire range of the DLL, allowing the PWM pulses to be selected from the entire 360º phase range of the DLL.

9. Simulating Asynchronous PWM/BPPWM

Simulating the above circuit with sampled time using Matlab (or any other system using sampled time) also creates the time-quantization issue. Typically these simulations are limited by available memory, in that for reasonable runtime, the entire sampled sequence must fit in available memory. Using sampling rates fast enough to give a wide range of possible pulse widths limits the total sequence length. Developing a superior simulation method for PWM would give a better estimate of the performance of an asynchronous PWM system.

A way around the sample rate limitation was conceived and developed during this work. The key is to perform the simulation in the frequency domain. The Fourier transform of an individual pulse (the rectangle function in time) is well known: the sinc function in the frequency domain. Applying the time-shifting and time-stretching properties of the Fourier transform to account for the differing centers and widths respectively gives:

$$\sum_i pulse(c_i, w_i) \overset{Fourier}{\Leftrightarrow} \sum_i w_i e^{j\omega c_i} \mathrm{sinc}\left(j\omega w_i\right) \tag{2}$$

This equation can be used to directly translate a pulse train described by a series of centers/widths (here designated the pulse domain), directly to the frequency domain without rounding. Only sections of interest in the spectrum need to be calculated, and the spectrum can be calculated with a non-uniform sampling: i.e., the focus can be on just the near-band performance of a PWM signal. The disadvantage of this simulation technique

is that all of the operations subsequent to the PWM generation need to be performed in the frequency domain. This necessitates finding the Fourier transform relationship of the desired operation in the time-domain. Lastly, implemented directly, this frequency domain algorithm is very computationally inefficient compared to the fast Fourier transform.

As an example of the application of this technique, Figure 12 shows the spectra of a BPPWM encoded CDMA signal computed directly from pulses to the frequency domain, compared with the identical signal computed by a time-domain fast Fourier transform:

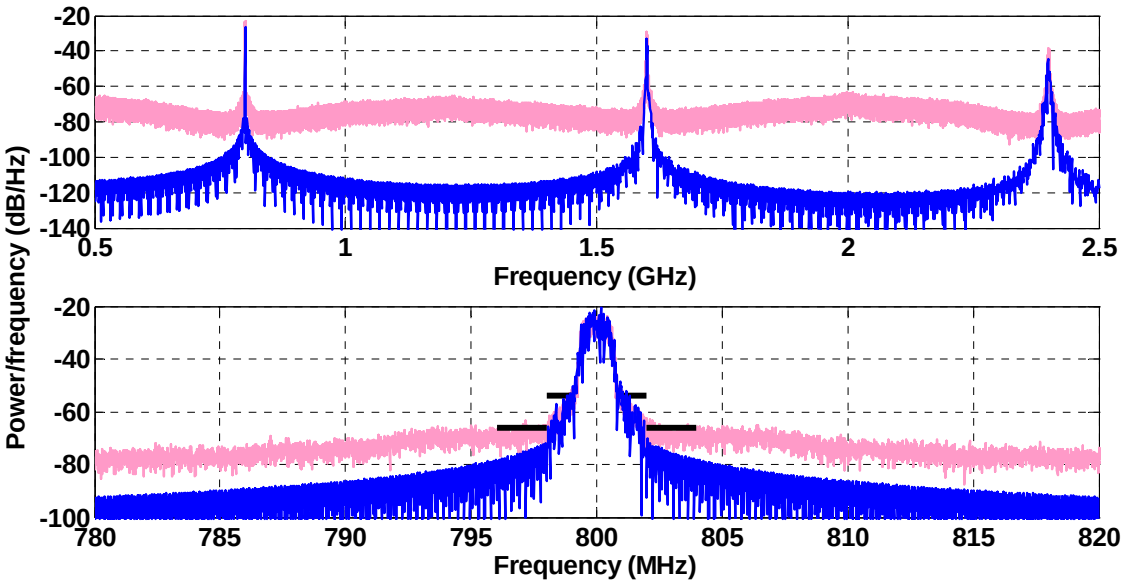

Figure 12: Computed spectra using a sampled simulation with shaped time-quantization noise, from Figure 7, (light red) and using the direct pulse to frequency domain method (blue). The discrete time Fourier transform was sampled at 12.8 GHz (8 possible pulse widths).

As expected, the noise floor is drastically reduced due to the absence of time-quantization using this technique. A noise floor still exists due to the finite sequence

length of the pulse train, but is significantly lower than the sampled simulation for a given sequence length.

10. VMCD Broadband Noise Excited by BPPWM vs. Delta-sigma

As was shown earlier, the noise transfer function (NTF) of BPPWM places all of the quantization noise into the signal harmonics. This greatly changes the behavior of a VMCD amplifier exhibiting the same nonlinearities discussed in the previous chapter.

Briefly reviewing, the supply memory nonlinearity causes the input signal to be mixed with a filtered version of itself. Due to the broadband nature of the quantization noise generated by the delta-sigma algorithm, this mixing operation causes some of the broadband noise to fall in the NTF notch, effectively raising the noise floor. This is not the case with BPPWM, as the quantization noise generated by BPPWM is not broadband in nature.

With BPPWM, the VMCD supply memory will cause spectral degradation similar to that of a classical analog amplifier. As with classical amplifiers, the noise generated will land in the frequency bands adjacent to the transmit signal. This is due to spectral characteristics of the BPPWM signal: the majority of the signal power is at the desired fundamental, and all the quantization noise is grouped tightly into the harmonics, with quiet bands in-between. The spectral equivalent of a time-domain mixing operation is a spectral convolution. Convolving a spectrum consisting of a signal with harmonics with itself adds side lobes to the desired signal (and all of the harmonics). This is virtually identical to the nonlinear distortions created by classical amplifiers.

Using the techniques developed in the previous chapter, the spectral performance of BPPWM driving a VMCD with supply memory was simulated. The setup is identical to the simulation used in chapter 5, section 3.4. Figure 13 shows the results:

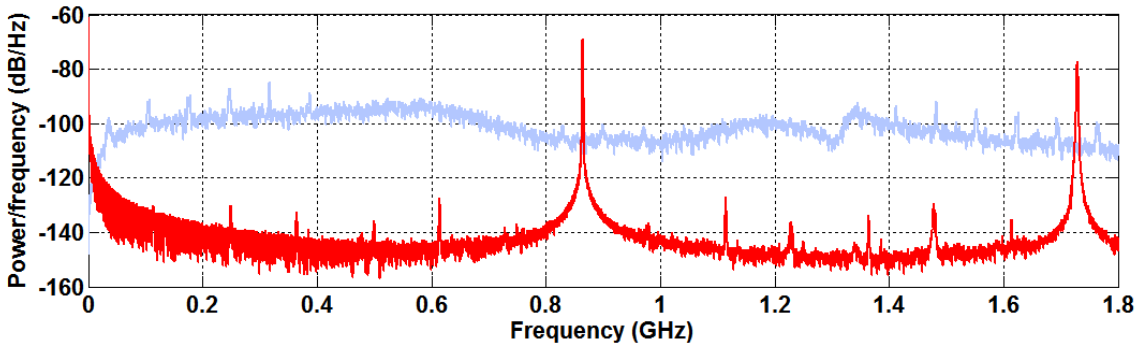

Figure 13: Simulated spectra of BPPWM signal driving the nonlinear VMCD amplifier model from chapter 5 (shown in dark red). Equivalent VMCD model driven with a band-pass delta-sigma is provided for reference (shown in light blue).

The same VMCD model is also shown driven with a delta-sigma modulator with an offset NTF optimized for a quiet receive band. As predicted by the VMCD analysis, the noise floor for BPPWM is almost at the noise floor of the simulation (-150 dB/Hz) and is significantly lower than the delta-sigma case. Unfortunately due to sampling rate and sequence length trade-offs, the amount of memory required to create a sequence length long enough to result in frequency bins small enough to accurately evaluate the near band spectral performance was not possible. Laboratory measurements in the next section will capture the near-band performance.

11. Experimental Results

In order to provide experimental verification of the performance of BPPWM with a real power amplifier, measurements were made using the improved VMCD amplifier that was first discussed in chapter 5. These BPPWM measurements are subsequently

compared to the performance of the same amplifier driven with the delta-sigma modulation used earlier in chapter 3. Similar to the previous experimental setups, a BPPWM encoded QPSK signal similar to IS-95 was generated using the time-quantization noise-shaping BPPWM algorithm outlined in section 7 of this chapter. The signal was formatted for playback on an Agilent 81140A Serial Pulse Data Generator. The signal was generated at the maximum pattern length of 2^{25} data points, at a 12.8 GHz playback sampling rate.

11.1. Time Quantization Noise in Generated Signal

Unfortunately, even when a 12.8 GHz (near the 13.5 GHz maximum capability of the 81140A) sampling rate is used, the signal envelope is quantized to 3-bits (eight distinct amplitude levels, see equation 1). Even when using the time-quantization noise shaping algorithm, the envelope quantization is too coarse for the generated signal to meet the target ACPR specifications of IS-95A. The BPPWM generated signal has an ACPR1 of -40 dBc (-42 dBc is the specification) and an ACPR2 of -53 dBc (-54 dBc is the specification).

The BPPWM generation system also generates more broadband noise in the amplifier input due to the time-quantization of the clocked BPPWM signal. The generated BPPWM amplifier drive signal has a noise floor around -55 dBc (at 100 kHz RBW, see Figure 14) compared with -65 dBc (at 100 kHz RBW, see chapter 5, Figure 3) for the generated delta-sigma drive signal.

This makes direct comparison with delta-sigma more difficult, as the delta-sigma drive signal can meet the ACPR specifications, and the BPPWM drive signal cannot. To

ensure the best comparison, a delta-sigma in-band power ratio tuning (set by the B to A coefficient ratio in the delta-sigma modulator, see chapter 4 section 4.8) was chosen to closely match the output ACPR of both systems.

11.2. Spectral Performance

The measured spectral performance of the BPPWM system is given below in Figure 14:

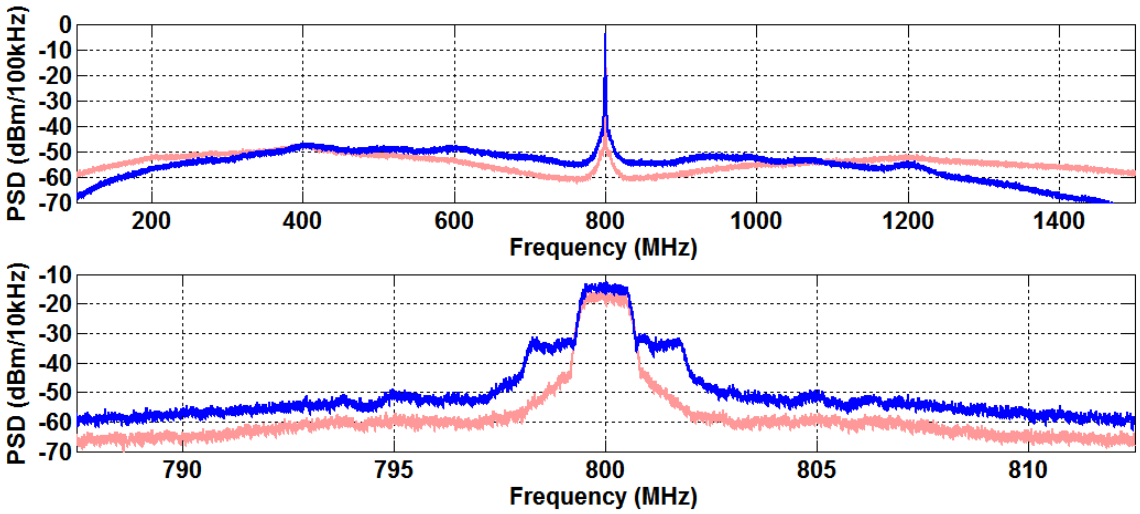

Figure 14: Spectral measurements of BPPWM. Input signal shown in light red, output signal shown in dark blue.

The laboratory spectral performance of the BPPWM driven VMCD confirms the predicted behavior when the distortions caused by the VMCD amplifier create near-band noise instead of broadband noise. This can be seen in Figure 14, in the lower zoomed spectra where the amplifier output has "shoulders."

Also, as predicted, the wideband noise performance is much superior to that of delta-sigma. Plotting the wideband spectral data from the top of Figure 14 with the wideband

spectral data from the delta-sigma system from chapter 5, Figure 24, results in the comparison shown in Figure 15:

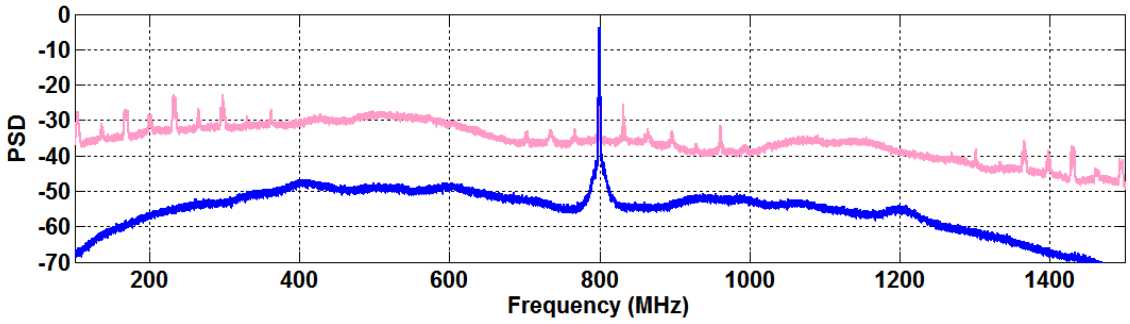

Figure 15: Output spectra of BPPWM driven VMCD (same as Figure 14 top, in dark blue) compared with output spectra for the amplifier with delta-sigma drive.

BPPWM shows a significant wideband noise improvement over delta-sigma. Unfortunately a more detailed quantification of the broadband noise in this BPPWM system is difficult to determine because of the broadband noise present on the drive signal due, discussed in section 11.1. The broadband noise on the input effectively sets a noise floor to the measurement.

11.3. Efficiency Performance

Efficiencies of the BPPWM system and the delta-sigma are tabulated. The following table gives the amplifier performance with 0.6 dB of cabling loss factored out for both systems:

Table 1: Comparison of BPPWM and delta-sigma.

	BPPWM	Delta-Sigma
Signal In-band Power Ratio	63%	40%
Final Stage Drain Efficiency	49.1%	36.8%
Dual Stage PAE	27.2%	19.5%
ACPR1	-31.3 dBc	-32.5 dBc
ACPR2	-41.8 dBc	-48 dBc

Examining the efficiency performance relative to the previous delta-sigma work, BPPWM has a clear efficiency advantage over the delta-sigma driven amplifier.

Creating a power back-off comparison is not possible due to the coarse time-quantization created by the clocked signal generation systems. Backing the BPPWM signal off causes a larger effective quantization, as the signal is restricted to progressively narrower maximum pulse widths. The signal spectral and accuracy measures rapidly degrade, unlike in the delta-sigma case, where improvement is seen. Also, the signal properties of the BPPWM signal in high levels of quantization are determined in larger part by the time-quantization algorithm. If a higher time resolution signal source is employed, the degradation expected from back-off is much less severe.

12. Conclusion

BPPWM is a promising encoding algorithm for digitally generating microwave communication signals. When generated with high accuracy, BPPWM significantly outperforms delta-sigma in both power efficiency and spectral purity. Furthermore, the spectral characteristics of BPPWM preserve the quiet spectral bands necessary for full duplex communication. This does come at a price of complexity in the signal generation, which is addressed by new circuit topologies.

In this work, three novel contributions to the state of the art in high speed PWM were developed: 1) a noise shaping algorithm that shifts time-quantization error in synchronous PWM away from the band of interest; 2) a technique that allows PWM systems to be simulated without the time-quantization noise, and 3) a circuit that

generates PWM with high time resolution using a low-speed clock. Experimental results were also shown using a VMCD amplifier.

13. Acknowledgments

The amplifier used in this chapter's measurements was based off of a design first used in [2]-[3]. The author would like to thank Jazz Semiconductor for CMOS fabrication.

14. References

[1] C. Presti, F. Carrara, G. Palmisano, A Scuderi "A High-Resolution 24-dBm Digitally-Controlled CMOS PA for Multi-Standard RF Polar Transmitters", in *IEEE Journal of Solid-State Circuits*, vol. 44, iss. 7, pp. 1883-1896, June 2009.

[2] T. Hung, J. Rode, L. Larson, P. Asbeck, "Design of H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters", in *IEEE Transactions on Microwave Theory and Techniques*, , Volume 55, Issue 12, Part 2, Dec. 2007 pp, 2845 – 2855

[3] T.-P. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "H-Bridge Class-D Power Amplifiers for Digital Pulse Modulation Transmitters," in *2007 IEEE MTT-S Int. Microwave Symp. Dig*., pp. 1091-1094, June 2007.

Chapter 7
Digital Polar Amplifier

1. Introduction

The goal of the work reported in this chapter is to implement a digitally driven polar amplifier suited to a high dynamic range communication signal, while still meeting noise specifications for full-duplex communication. This chapter presents a unique design of a polar amplifier consisting solely of switching amplifiers. Novel algorithms to drive this amplifier efficiently, while achieving accurate output, are presented. A general study of broadband noise generated by polar amplifiers is undertaken. Unique properties of broadband noise generated by common polar amplifier impairments are analyzed. A novel algorithm is presented that can suppress broadband noise in polar amplifiers in the presence of time-misalignment, a common impairment in polar transmitters.

In previous chapters, the amplifiers under investigation used binary input signals to switch between fixed voltage states. Non-constant envelope amplification was achieved by using encoding techniques: pulse-density modulation (PDM) in the case of delta-sigma/noise-spreading or pulse-width modulation (PWM). These encoding algorithms allow a non-constant envelope signal to properly drive a switching amplifier to saturation. In contrast, this chapter is concerned with an alternative technique that allows a non-constant envelope signal to be amplified with a switching amplifier by separating the drive signal into two different drive signals, representing the phase and the amplitude separately. This is referred to as a polar amplifier or, alternatively, as envelope elimination and restoration (EER).

2. Polar Amplifiers

Polar amplification splits the desired signal into two components: a phase modulated RF signal that is typically fed into the gate/base of the amplifier, and a magnitude or envelope signal, proportional only to the power level of the desired signal. The saturated power amplifier serves as a multiplier, and ideally outputs a correctly reconstructed communication signal:

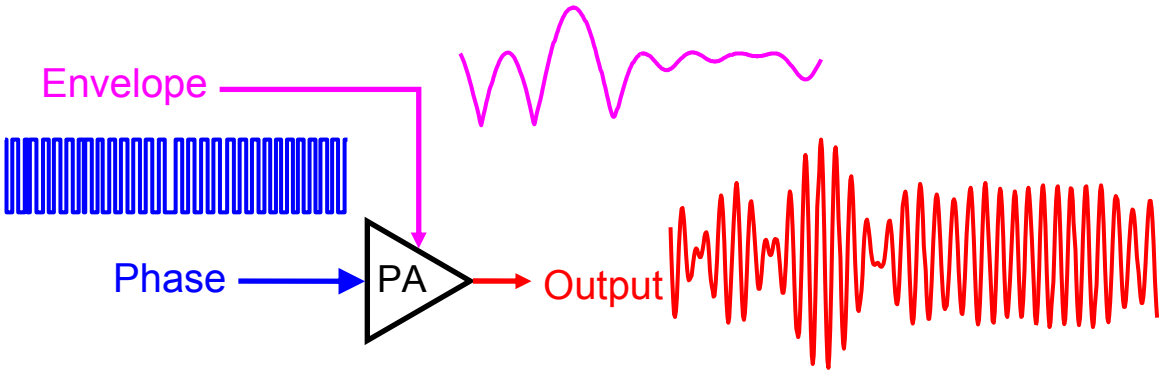

Figure 1: Block diagram of a polar amplifier, shown with example waveforms.

The operation carried out by the polar transmitter signal generator is a Cartesian-to-polar coordinate system conversion. The polar representation of communication signals has several advantages that allow efficient amplification. First, the envelope signal has a bandwidth proportional to only the modulation bandwidth of the system, and not the transmit frequency. Typically modulation bandwidths of most communication systems are orders of magnitude lower than the transmit frequency. Second, the phase signal has constant envelope. The phase signal can be amplified directly with switching amplifiers using resonant techniques, preserving efficiency even at high switching frequencies. The envelope signal is not constant envelope, but it is much lower

bandwidth and frequency, lending itself well to amplification with digital techniques previously discussed in this work.

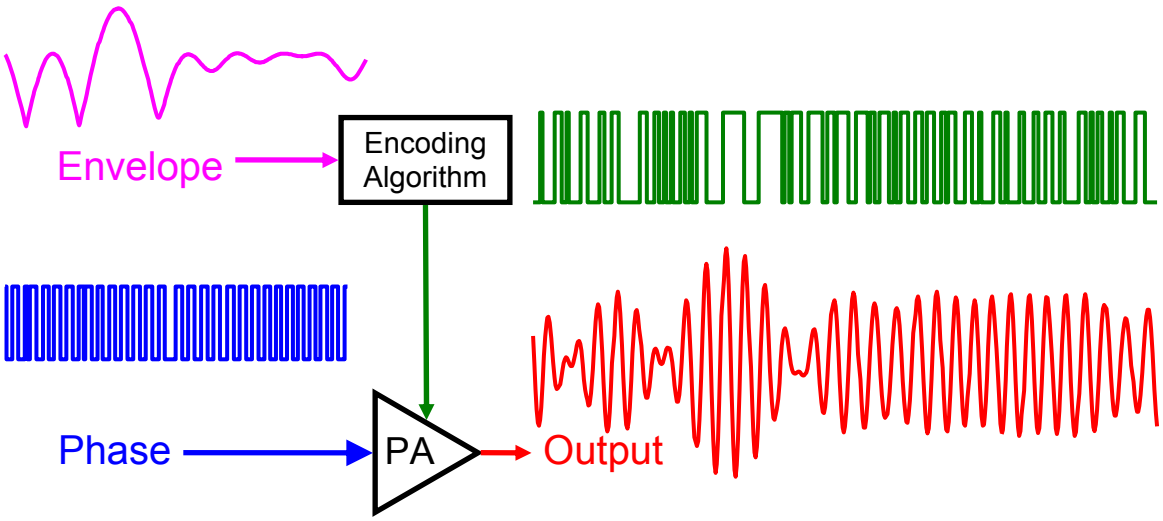

Figure 2: Block diagram of a digital polar amplifier, shown with example waveforms.

The envelope signal is typically amplified with a separate amplifier, usually referred to as an envelope amplifier. Traditional polar amplifier systems use an analog envelope amplifier. This chapter presents a novel polar amplifier system, referred to here as a digital polar amplifier, in which the envelope amplifier is driven with a binary signal, as shown in Figure 2. All of the elements in this system are switching amplifiers that are driven digitally.

The design has been extensively simulated, and many of the problems encountered and their corresponding solutions are generalized when possible to encompass all polar transmitter/amplifier systems, including traditional analog ones. Design and simulation issues include: accurate simulation; finite envelope amplifier slew rate; and finite bandwidth along with envelope/phase time alignment, both impacting broadband noise generation.

3. The VMCD/ CMCD Digital Polar Amplifier

The particular digital polar amplifier discussed in detail is the VMCD/CMCD digital polar amplifier, which comprises a voltage mode class-D (VMCD) drain amplifier driving a current mode class-D (CMCD) amplifier through an inductor, as shown in Figure 3:

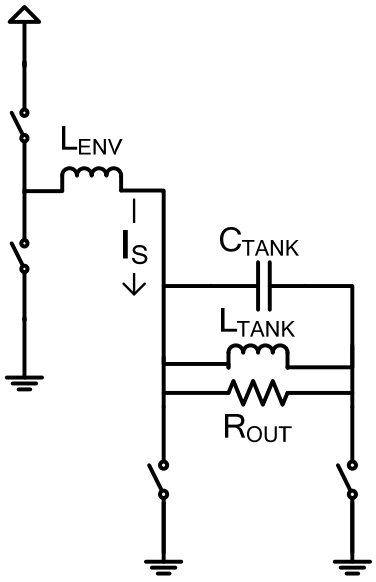

Figure 3: Schematic diagram of proposed VMCD/CMCD digital polar amplifier. For simplicity no output matching is shown.

The CMCD has an output RF amplitude proportional to the supply current (I_S) and, at the envelope rate, presents a resistive load to the envelope amplifier. The VMCD, driven through an encoding algorithm, such as delta-sigma or PWM, rapidly switches and generates an appropriate current through the envelope inductor. The switching waveform chosen to drive the VMCD envelope amplifier must take into account the inductor/resistor transfer function. The following equation is the inverse transfer function of the LR circuit formed by the envelope inductor and CMCD load:

$$V_{VMCD} = \frac{L_{ENV}}{R_{CMCD}} \frac{dV_{ENV}}{dt} + V_{ENV} \quad (1)$$

The following diagram shows the proposed digital polar amplifier with the inductor compensation and the encoding algorithm, along with example waveforms:

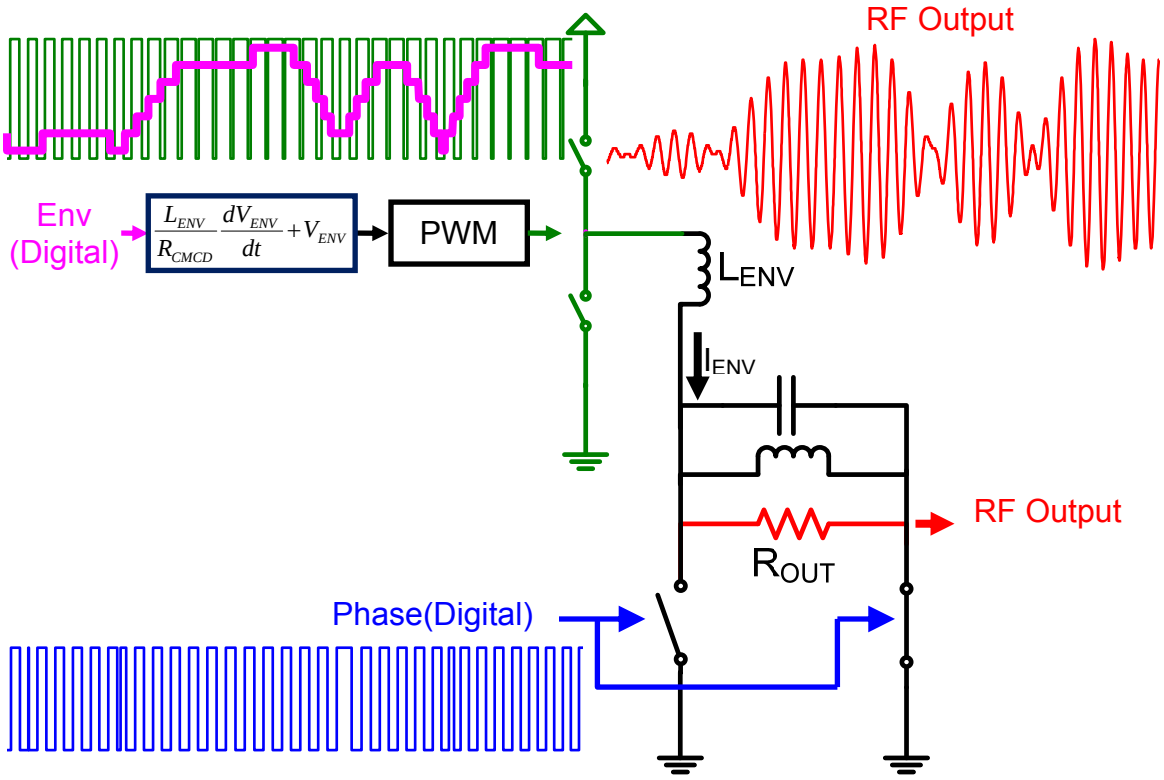

Figure 4: VMCD/CMCD system block diagram shown with example waveforms. PWM is used here for the envelope encoding. The PWM frequency is typically much lower than the RF frequency.

The advantages of this architecture include the potential for high efficiencies, even when amplifying signals with high peak-to-average ratios. The inductor has the side benefit of smoothing the switching transients generated by the VMCD envelope amplifier and partially suppressing the higher frequency quantization noise generated by the envelope encoding algorithm

4. Targeted Communication Standard

For a first pass design, wideband CMDA (WCDMA) was selected as a target standard. WCDMA was chosen due to its ubiquity and reasonable bandwidth and peak-to-average ratio (PAR). All of the WCDMA signals presented here have been initially generated with a pseudorandom series of chips modulated with offset quadrature phase shift keying (OQPSK) at 2.84 Mchips/second. These chips are then pulse shaped with a root-raised cosine filter with a roll-off factor of 0.2. The signal is then upsampled to the universal mobile telecommunications system (UMTS) frequency band I (1.95 GHz). The power is normalized to a typical handset transmit power of 33 dBm (which is coincidentally about -33 dBm/Hz because the WCDMA transmit bandwidth of 3.84 MHz corresponds to 66 dB-Hz). A typical spectrum of the generated WCDMA signal is shown in the following figure:

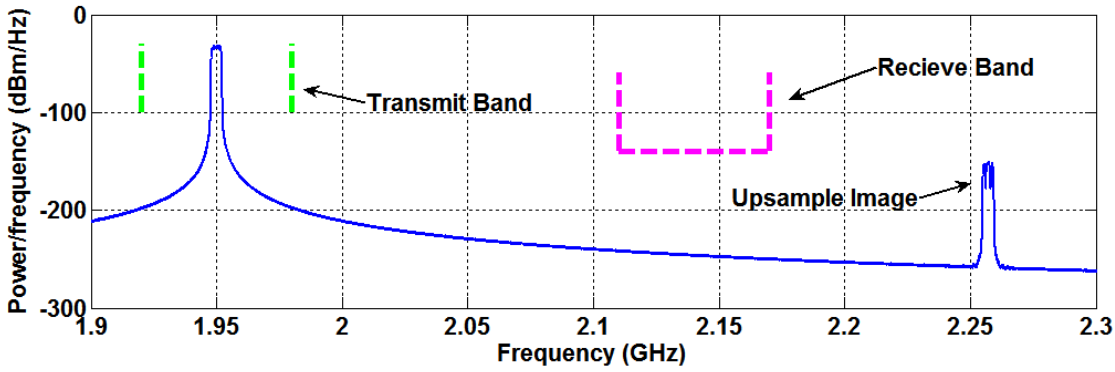

Figure 5: WCDMA simulation signal spectrum. Relevant bands and limits are shown with dotted lines

Spectra will typically be annotated with dotted lines showing the relevant spectral limits mandated by the WCDMA standard. These include limits such as adjacent channel power ratio (ACPR), also referred to as alternate channel power ratio (ACPR) for nonadjacent channels, or adjacent channel leakage ratio (ACLR). The lines shown for

ACPR are an approximation, as the actual calculation of ACPR involves extracting the power from the adjacent channel with a root-raised-cosine filter. The receive band (RX Band) and transmit band (TX Band) are also annotated, along with the self-jamming upper limit.

5. Simulation Methodology

Similar problems to that in chapter 5 were encountered when simulating this system using standard variable-step transient simulations. For this reason, the system simulation was setup in a similar manner to the VMCD receive band noise simulations performed in chapter 5: equations were setup in the Simulink environment that performed a quick, ideal fixed time-step transient simulation. As the final block diagram is fairly complex, the explanation will begin with a basic polar amplifier, and then extend to the envelope-only simulation. Limited full-rate RF simulation is used to verify the accuracy of the envelope-only simulation.

First an ideal polar amplifier simulation is setup with only the Cartesian-to-polar conversion and reconstruction:

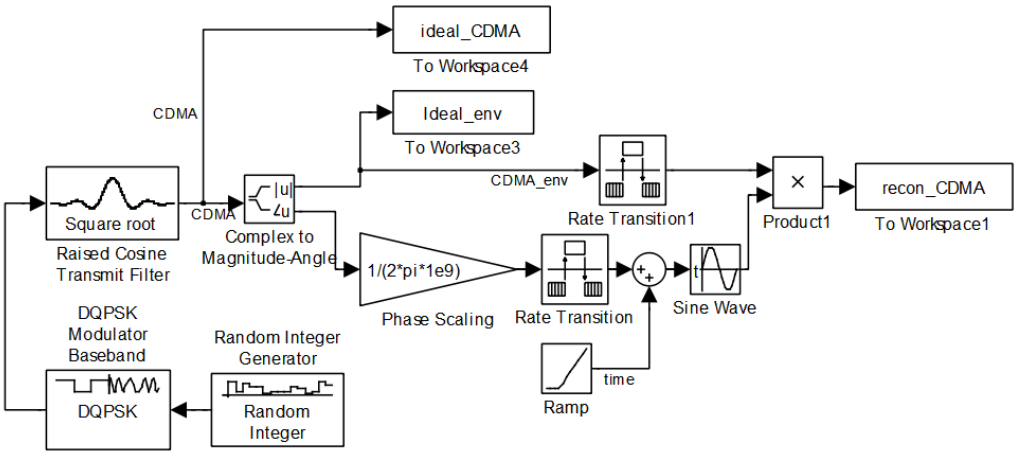

Figure 6: Block diagram of the basis of the WCDMA polar system simulation.

The block diagram starts with a random integer generator feeding the baseband modulator. This signal is subsequently filtered with a raised cosine pulse shaping filter. The signal is then converted from a complex representation to a polar, magnitude/angle representation. This signal is subsequently reconstructed by using the phase signal to modulate a carrier, and multiplying this with the envelope signal. The multiplier is the ideal model of an RF amplifier in saturation.

The next step is to add the envelope modulator and envelope inductor to the system. The block diagram of the simulation, shown in Figure 7, starts with the block diagram in Figure 6 and adds the inverse transfer function (a derivative) of the envelope inductor to the incoming envelope signal. The envelope is then encoded with standard PWM by a comparator fed with a triangle wave. The PWM envelope signal is then fed into an inductor, modeled by a numerical integration of the simulated voltage across the inductor terminals. The output signal of the CMCD amplifier is subsequently reconstructed by multiplying the inductor current with the phase encoded carrier.

Realistic component values are chosen to shown they result in proper system operation. Values include an envelope inductor of 200 nH and a CMCD load impedance of 2 Ω.

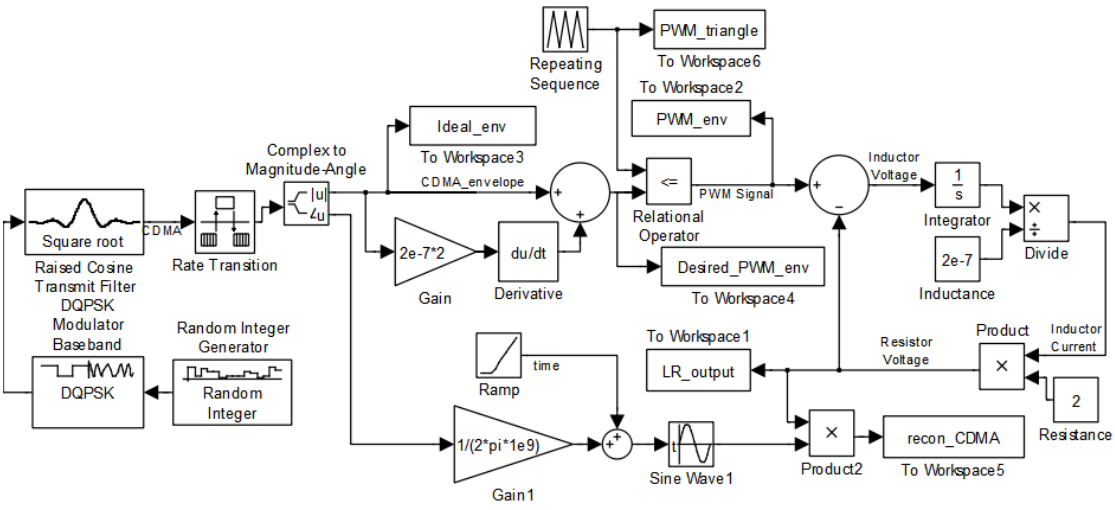

Figure 7: Block diagram of the PWM-based digital polar amplifier envelope simulation.

The maximum time step, in which this simulation will converge, is related to the time constants of processes being modeled. For computationally efficient simulation it desirable to perform all of the simuatons at the largest time-step possible. Due to run time and memory limitation, simulations with time steps small enough to capture resonances at the RF carrier frequency result in output sequences too short for spectra accurate enough to evaluate ACPR type metrics. This issue is addressed by modeling the RF amplifier as a resistive load when seen at the lower envelope frequencies. A simulation is used to verify the assumption that the CMCD RF amplifier is accuratly modeled as resistive load when seen though the envelope inductor at the lower envelope frequecies. Figure 8 shows the current and voltage relations assumed in the CMCD amplifier.

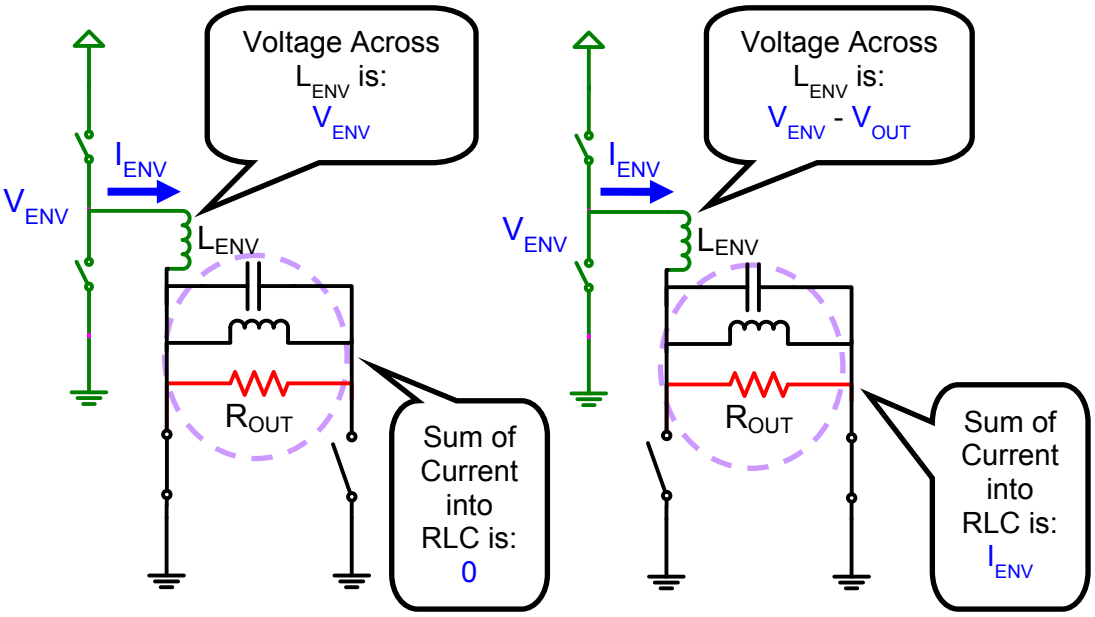

Figure 8: The two states of the CMCD states, and the corresponding voltage and current relationships between the envelope inductor and the RF RLC resonator.

The simulation starts by assuming ideal switches, so the circuit is broken into two phase states, corresponding to the switching states of the CMCD amplifier. The current state of the CMDC is set by the modulated phase signal from the polar signal represenetation. The supply input current is modeled identically as in the envelope simulation in Figure 7. Translating these relationships into a block diagram results in Figure 9, below:

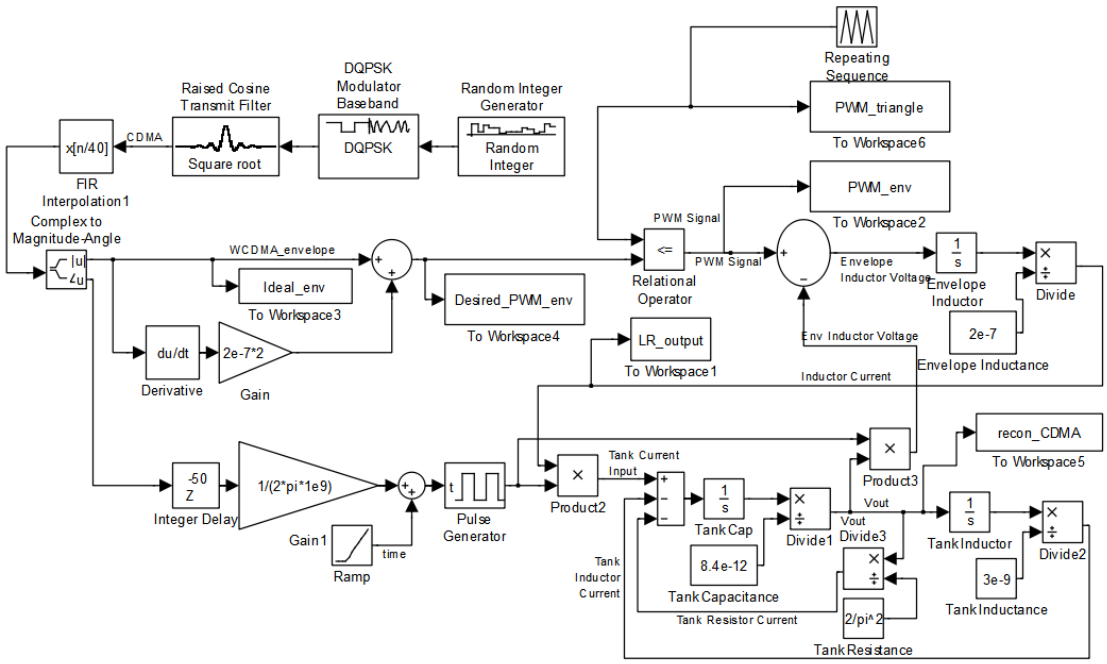

Figure 9: Entire block diagram of full digital polar amplifier simulation.

The block diagram of Figure 9 encompasses all of Figure 7 plus the additions of the relationships in Figure 8. Again, realistic values were chosen for the RF inductor and capacitor values of 3 nH and 8.4 pF for an initial simulation. For explanation, a stripped version of the above block diagram is presented below in Figure 10, with the signal generation sections removed:

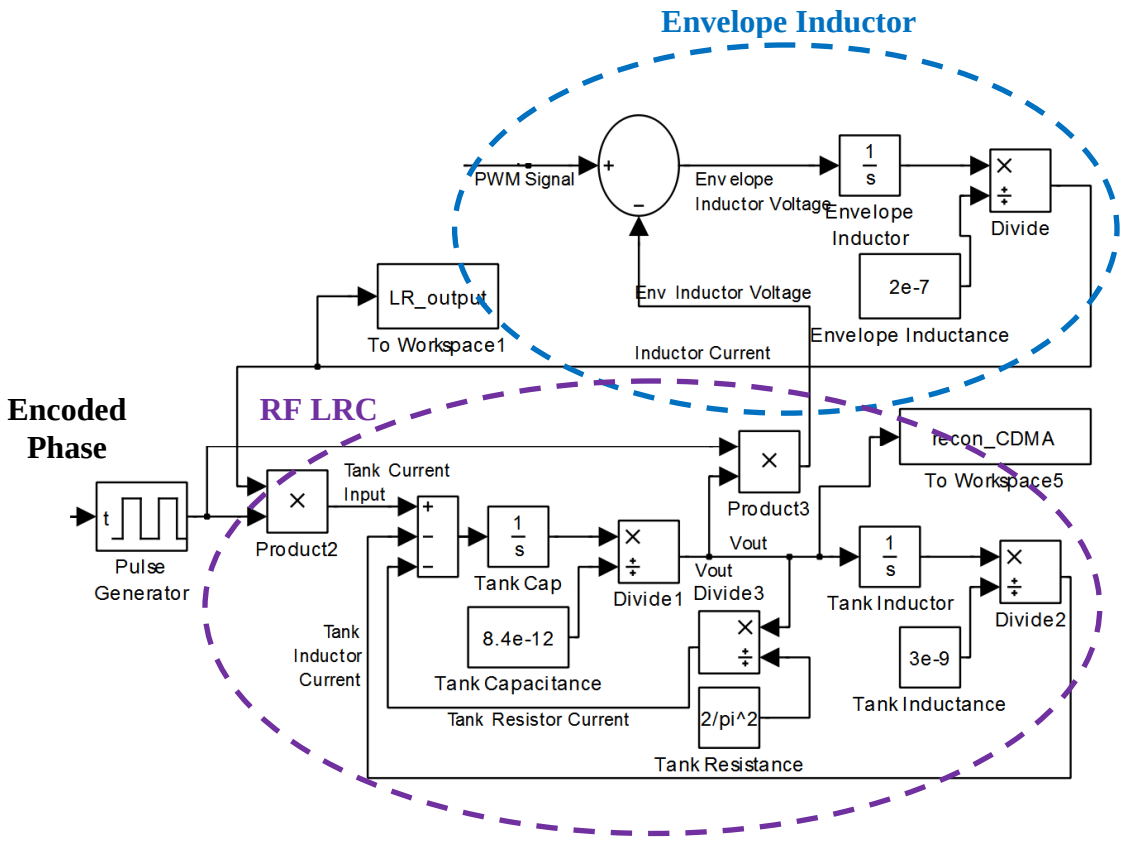

Figure 10: Simplified and annotated version of Figure 9.

The parallel RLC circuit is modeled by a set of numerical integration steps fed by a calculated current from the envelope inductor model. The envelope current is multipled by the incoming phase pulse. The full RF simulation matches both the ideal envelope, and the envelope based simulation in the time, as shown in Figure 11.

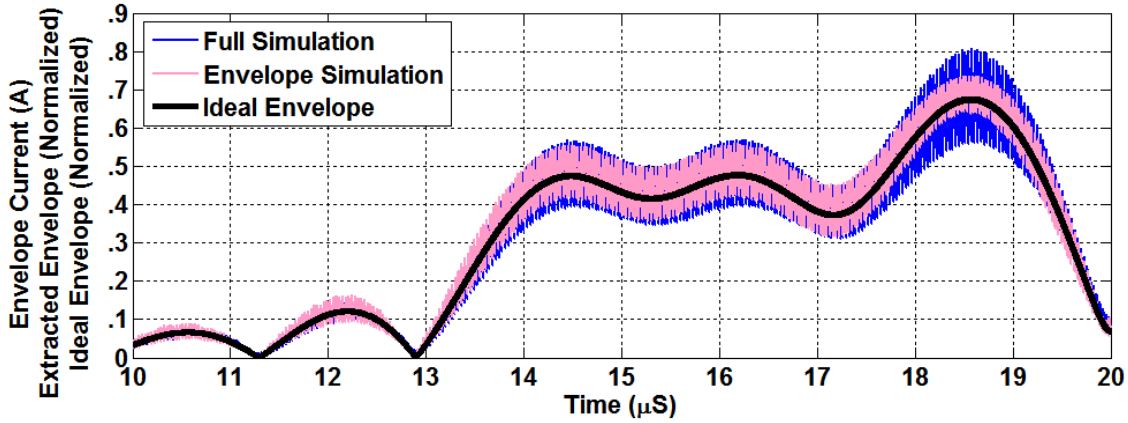

Figure 11: Time domain over-plot of the input envelope (red), the inductor current from the full RF simulation (blue) and the envelope simulation (green).

As the full RF simulation models devices with small time constants, it is very unstable at low oversampling rates compared with the envelope-only simulation. The full simulation required a factor of 40 more sampling steps to converge than the envelope simulation. This made spectral comparisons difficult, as generating sequences long enough to obtain detailed spectra was computationally prohibitive. All subsequent simulations in this section treat the CMCD as a resistive load at the envelope rate of the system.

6. Encoding Algorithm Selection

Low-pass delta-sigma modulation and pulse-width modulation were both simulated with the envelope simulation method discussed previously. The same initial values were used as above, a 2 Ω CMCD equivalent resistance with a 200 nH envelope inductor connected to a VMCD, with voltage supplies set such that 33 dBm of average RF power could be achieved. (Supply voltage requirements will be discussed more extensively later in the chapter.) In the initial simulations, both envelope encoding algorithms showed good spectral performance across the transmit band, but for a given

clock rate, PWM vastly outperformed delta-sigma in the receive band. The PWM system showed some ACPR artifacts due to time quantization. In Figure 12 the spectra are compared with ideal spectra to give a reference as to the noise floor of the simulation:

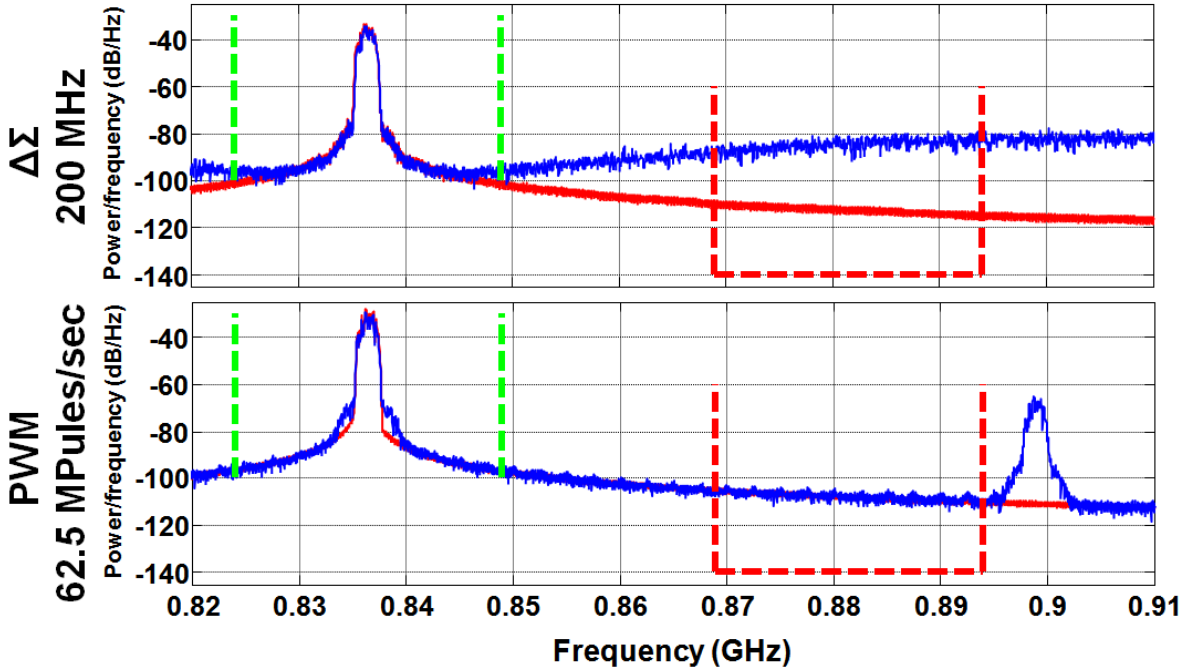

Figure 12: Simulated spectral compairson of ΔΣ and PWM in the VMCD/CMCD digital amplifier system. Blue lines are the simulated spectra; red lines denote the ideal signals. Dotted vertical lines denote transmit and receive bands, with horizontal line at self-jamming limit.

The superior broadband noise performance of PWM is due to the previously discussed fact that the quantization noise in PWM is grouped into signal harmonics, as opposed to delta-sigma, where the noise is shaped into a broad band that overlaps the RX band for reasonable delta-sigma clock rates. For good RX band performance in a delta-sigma based digital polar amplifier, prohibitively fast clock rates are necessary. For this reason PWM was selected as the envelope quantization algorithm for the digital polar amplifier design.

7. Inductor Sizing

An envelope simulation was setup to explore the effect of the envelope inductor size on the system's spectral perfomance. The impedance of the CMCD RF amplifier was held constant at 2 Ω. As the maximum voltage needed for the envelope amplifier is a function of the inductor size, the voltage supply rails in the simulation were set so that the envelope amplier would be able to produce the necessary voltage to track the signal envelope accuratly with the inductor current.

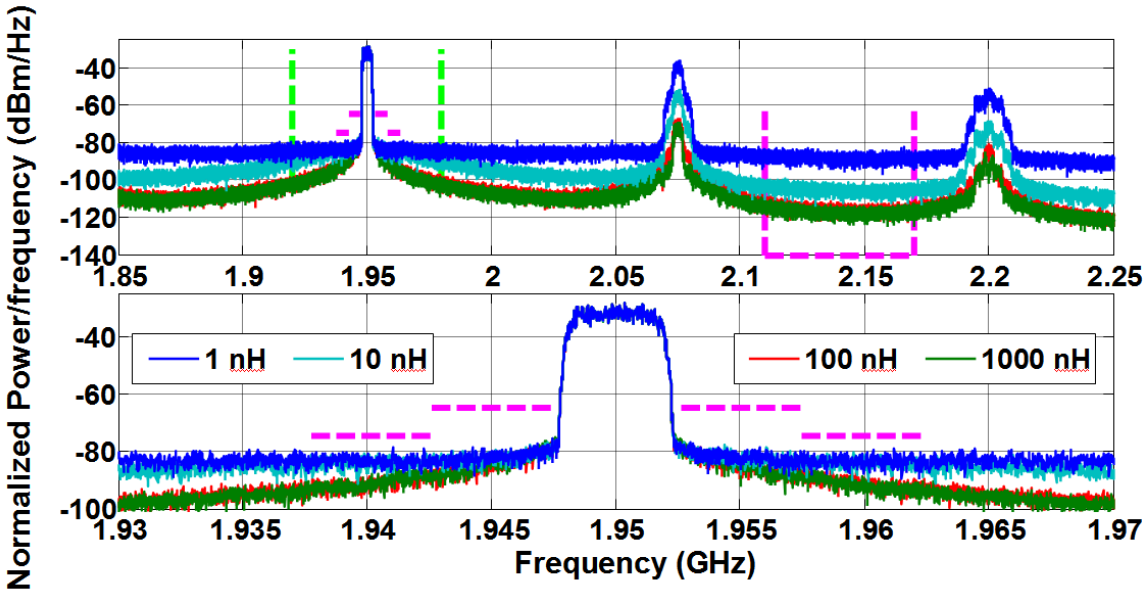

Figure 13: Simulated spectra of the polar system with different envelope inductor sizes. Dotted vertical lines denote transmit and receive bands, with horizontal lines at self-jamming limit in the receive band, and the approximate ACPR limits in the transmit band.

Free from constraints on power supply rails, larger envelope inductors suppress PWM harmonics and improve the noise floor in general, all the way down to the simulation limit. This comes at an expense of the voltage demanded from the envelope amplifier. Larger inductors demand larger voltages to force current changes. Figure 14 shows the minimum supply voltages necessary to accurately track a WCDMA envelope:

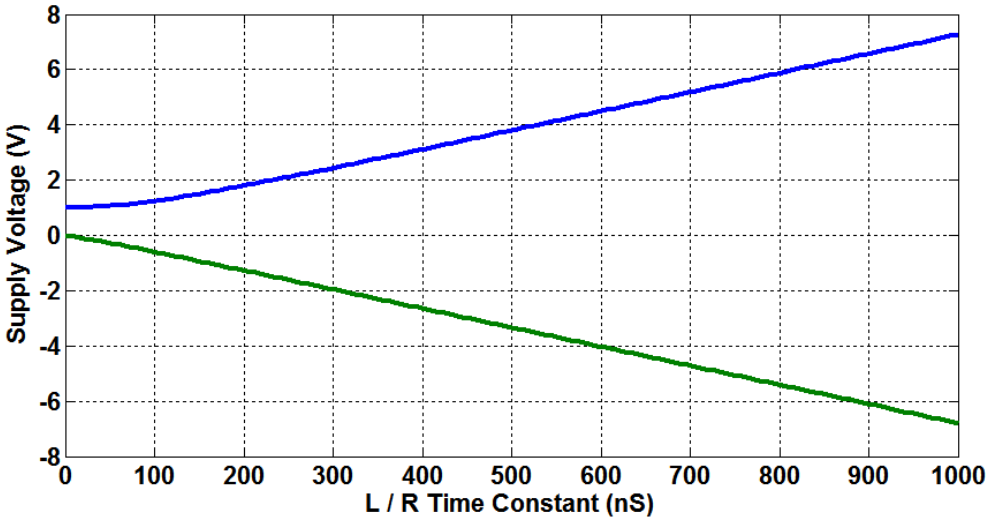

Figure 14: Simulated supply voltages necessary to meet WCDMA envelope slew rates thought different time constants formed by the LR circuit.

The positive supply rail is reasonable all the way out to inductor sizes of several hundred nH. This is not true of the negative supply rail, since the requirement for having a negative supply rail in a handset design negates many of the efficiency gains expected from the VMCD/CMCD design. Ideally, the amplifier system should be made to work without a negative supply. In the next sections, the impairments of this system running without a negative supply will be explored, and modifications to the basic system that allow the amplifier to track the signal envelope to zero, even with residual envelope inductor current.

8. Envelope Inductor Current Slew Rate

The inductor imposes a physical limit on how fast the envelope current can slew. Figure 15 illustrates the equivalent circuit of the envelope path of the digital polar amplifier:

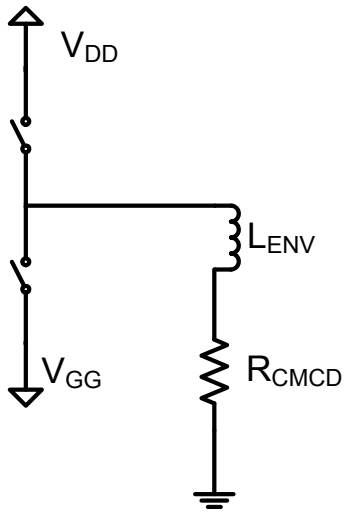

Figure 15: Equivalent envelope circuit of the digital polar amplifier.

There are two maximum current slew rates associated with the pull-up and pull-down devices:

$$\frac{dI_L}{dt} = \frac{1}{L}\left[V_{DD} - I_{ENV} \times R_{OUT}\right] \tag{2}$$

$$\frac{dI_L}{dt} = \frac{1}{L}\left[V_{GG} - I_{ENV} \times R_{OUT}\right] \tag{3}$$

From these equations, the maximum current slew rate of the system is found to be dependent on the current already flowing though the inductor. When most of the supply voltage is being dropped across the resistor, there is little residual voltage to force a current change in the inductor. This would occur at high envelope inductor currents for the pull-up, and at low envelope inductor currents for the pull-down.

8.1. WCDMA Envelope Slew Rate and Zero-Crossings

To establish proper design parameters, it is important quantify the slew rate of WCDMA envelope signals. Taking a numerical derivative of the envelope, and plotting

instantaneous slew rate versus envelope magnitude (or envelope current in this case) results in the following trajectories given in Figure 16.

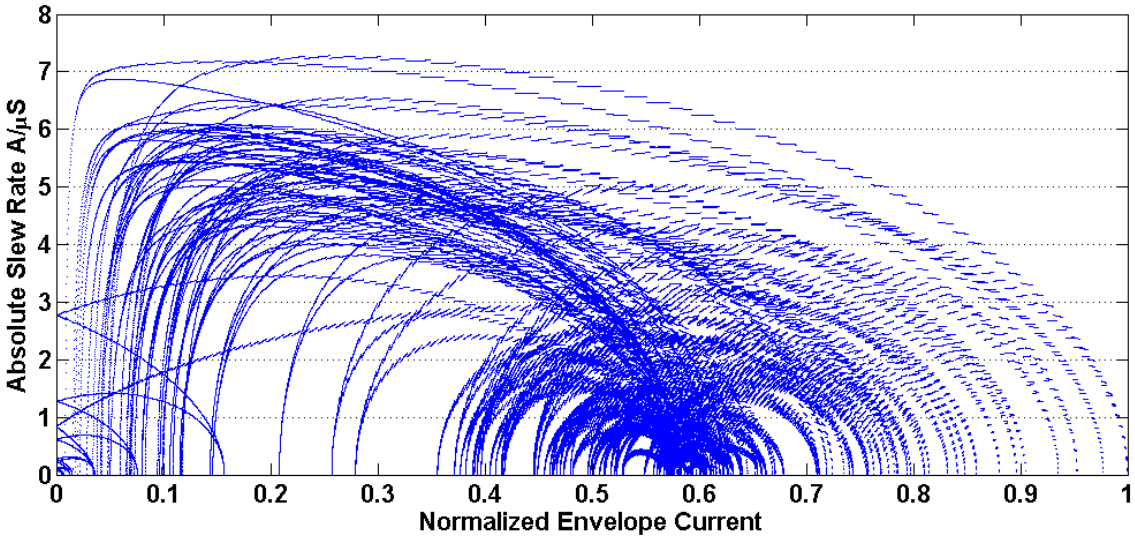

Figure 16: Absolute value of envelope current slew rate versus normalized envelope magnitude for a WCDMA driven VMCD/CMCD system.

From this plot, the events with the largest slew rates all occur near the origin of the I/Q plane. Looking at a time domain plot of these high slew rate events, they are all associated with close approaches to the origin, or zero-crossings in the I/Q plane. These zero crossings are caused by diagonal transitions where the I and Q signals move together, i.e. 00 to 11 or 01 to 10 in either direction, that cause the signal trajectory of the complex envelope to cross near the origin. Slicing a time segment containing a zero crossing out of a simulated WCDMA signal allows a typical zero crossing to be examined in detail in Figure 17.

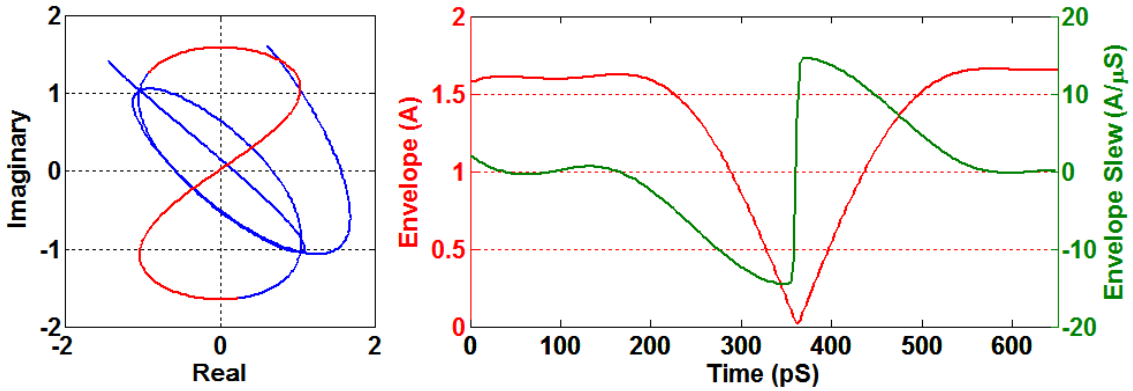

Figure 17: I/Q diagram of a zero-crossing (left) and envelope magnitude and envelope slew rate (right). The I/Q diagram shows a larger section of the WCDMA signal trajectory, while the right plot expands the zero-crossing (highlighted in red) of the I/Q trajectory.

The magnitude of the slew rate (and correspondingly the severity of the zero-crossings) is determined by the bits leading up to and out of the diagonal transition. The I/Q trajectory is brought closer to the origin by long runs of repeated bits before and after the diagonal transition. The worst case zero-crossing will occur from a run of repeated data long enough to completely settle the pulse shaping filter, followed by a diagonal transition, ending with another similar length run of repeated data. Zero-crossings in polar amplifiers will also cause other problems in this amplifier, which will be examined later in the chapter.

8.2. Polar Envelope Slew Rate Expansion

In baseband, the pulse shaping filter limits the bandwidth of the individual signals, and thus the time derivative of the individual I/Q signals is also limited. When these band-limited signals are converted into the polar domain, the bandwidth and slew rate limited properties of the signals are not completely preserved. A quantitative

analysis begins with the complex modulus function that converts a complex signal into its envelope:

$$E(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{4}$$

Taking the total differential of the Cartesian to polar function results in the following multivariable differential:

$$\frac{dE(t)}{dt} = \frac{I(t) \cdot \frac{dI(t)}{dt} + Q(t) \cdot \frac{dQ(t)}{dt}}{\sqrt{I(t)^2 + Q(t)^2}} \tag{5}$$

or:

$$\frac{dE(t)}{dt} = \frac{I(t) \cdot \frac{dI(t)}{dt} + Q(t) \cdot \frac{dQ(t)}{dt}}{E(t)} \tag{6}$$

The slew rate remains finite even at zero crossings since, as the envelope reaches zero, both I and Q signals also reach zero. A crude estimate of the slew rate of the envelope during a zero crossing can be made using the assumptions that both of the baseband signals are relatively narrow band and sinusoidal. Setting both I and Q to a sine wave gives equation (7):

$$\frac{dE(t)}{dt} = \frac{2 \cdot \omega \cdot \sin(\omega t) \cdot \cos(\omega t)}{\sqrt{2 \cdot \sin(\omega t)^2}} \tag{7}$$

Simplifying (7) gives (8):

$$\frac{dE(t)}{dt} = \sqrt{2} \cdot \omega \cdot \cos(\omega t) \tag{8}$$

This simple example results in a factor of approximately 1.5x in slew rate expansion.

Slew rate expansion also causes a bandwidth expansion in the envelope signals. Generalizing the bandwidth expansion mathematically is not very useful, as the

bandwidth expansion encountered in a real system will depend on the implementation details of the particular system.

9. Envelope Current Slew Rate Limitations for the VMCD/CMDC Polar Amplifier

The polar trajectory of the envelope near zero crossings creates an asymmetrical slew limitation in this system. When the I/Q trajectory approaches a zero-crossing, the pull-down device is primarily active, and when the trajectory moves beyond the zero-crossing, the pull-up device is primarily active. By definition, the zero-crossing occurs at very low envelope magnitudes. At the origin, rapidly increasing the envelope inductor current requires only a reasonable voltage from the envelope amplifier, as the corresponding voltage drop across the resistive CMCD load is low, allowing all of the supply voltage to be dropped across the envelope inductor, causing a rapid rise in current. The opposite is true for a pull-down device connected to ground. The grounded pull-down device will cause the inductor current to exponentially approach zero. The exponential approach can not match the rapid slewing of the WCDMA envelope. The coming sections will analyze the expected effects of the envelope inductor current failing to track the envelope signal, and offer a solution.

9.1. WCDMA Peak-to-Minimum Ratio

Prior to detailed investigations about the effects of not accurately following the envelope zero crossings, a more general study was performed. A simulation was performed where an ideal WCDMA signal was brought into the polar domain, and the envelope minima were hard clipped to different levels. Three envelope signals were

generated, where the envelope was not allowed to travel below 20%, 16%, or 10% of full scale to explore the expected spectral degradation. This operation of "detroughing" is roughly analogous to the de-cresting operation often applied to reduce peak-to-average ratio in communication signals.

Clipping off the minima of a WCDMA signal is not expected to significantly degrade the signal accuracy, as all QPSK symbols are on the unit circle. Figure 18 shows the noise generated by clipping the envelope minima, and thus diverting the signal trajectory around the origin in the I/Q plane:

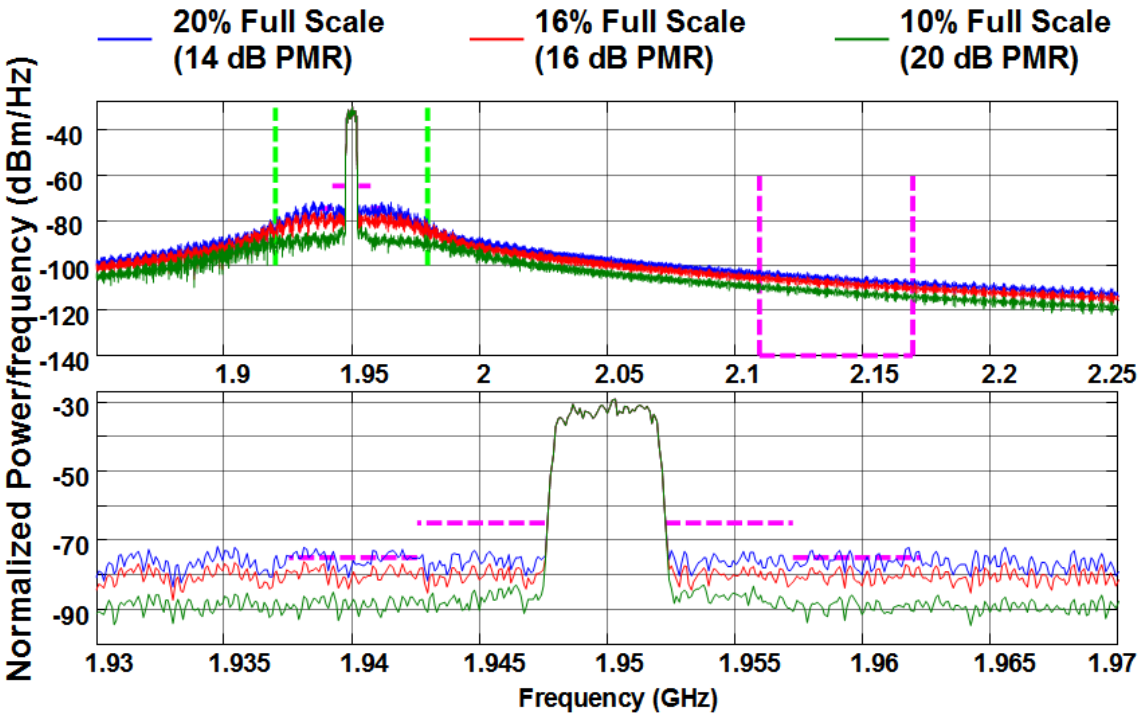

Figure 18: Broadband (top), and narrowband (bottom) spectra from a minima clipped WCDMA signal. Dotted vertical lines denote transmit and receive bands, with horizontal lines at self-jamming limit in the receive band, and the approximate ACPR limits in the transmit band.

Hard clipping the minima generates both broadband and near-band noise. ACPR specifications are violated around 20% of full scale. Broadband noise generated by the

VMCD/CMCD system should be lessened by the envelope inductor, but the hard-clipping case is an illustrative example for general polar amplifier designs, as most amplifiers become very nonlinear at high gate/base input power levels combined with low drain/collector input power levels.

9.2. Envelope Error Memory

In this system, failure of the envelope inductor current to accurately track the signal envelope not only causes an instantaneous error, but if not properly compensated, also causes a signal error to persist beyond the point of rapid slewing. The error persists because the initial conditions of the derivative function, which pre-computes the necessary voltage to induce a corresponding current in the envelope, are not met. The result is a decaying error. A WCDMA envelope, and corresponding envelope inductor current, is simulated below for a represented scenario which highlights this error:

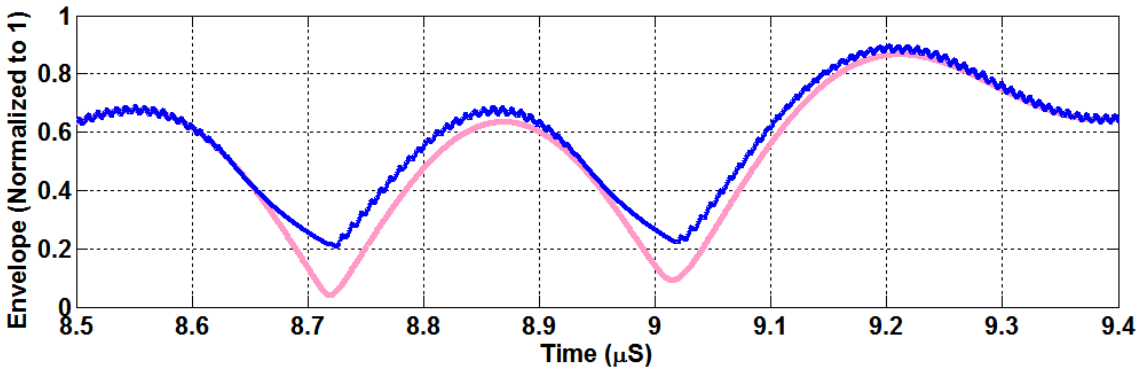

Figure 19: Envelope inductor current (dark blue) showing persistent error. The ideal envelope (light red) is shown for comparison. The simulated LR time constant is 100 nS. Note that the WCDMA chip rate is 260 nS.

Referring to the equivalent circuit diagram, any voltage error introduced by slew rate limitations in the envelope path to the LR circuit will cause an error to persist beyond

the high slew rate. The error will then decay at the LR time constant of the envelope path.

A simulation was setup to investigate the effects of finite envelope current slew. The following spectra show the spectral degradation from both the slew errors, and the decaying envelope error:

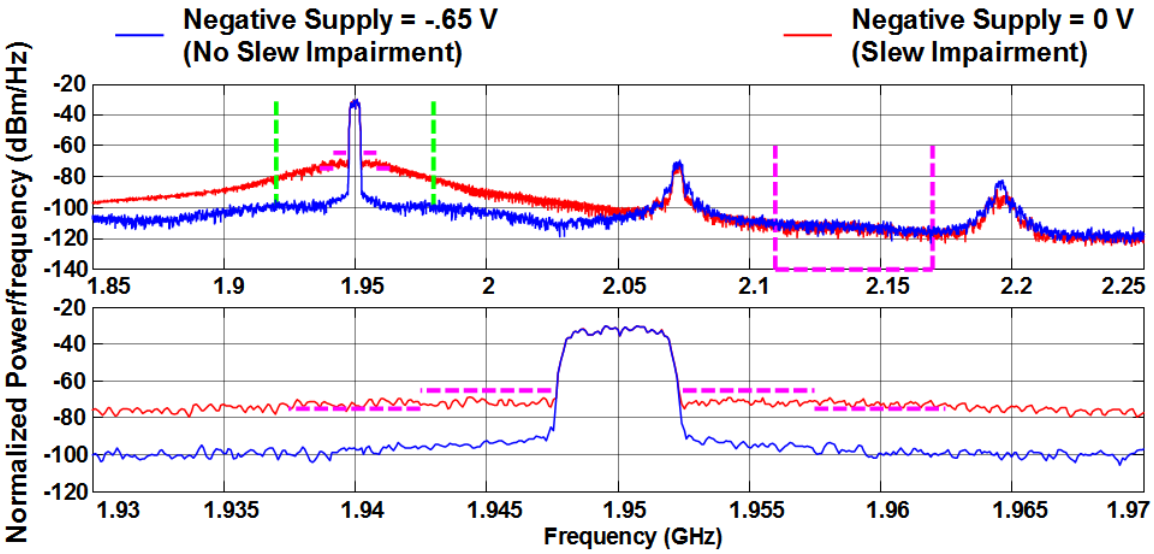

Figure 20: Simulated spectra of a VMCD/CMCD amplifier system with a 100 nH envelope inductor, 1 Ω CMCD resistance, and a 1.3 V pull-up supply voltage. The simulation is done with a pull-down voltage of 0 (red) and -0.65 V (blue).

Slew rate issues from a low pull-down voltage cause substantial near band spectral noise to be generated, falling off with the decay of the LR time constant.

9.3. PWM Modulators and Sampled Time

The PWM simulation architecture presented in chapter 5 for RF signals was also adopted for the envelope portion of the CDMD/VMCD digital polar amplifier simulation. Many of the same issues with sampling PWM in time that were encountered in chapter 5, with sampled time and PWM signals, were again encountered and similar solutions were

used. Additionally, a time constant was added to the error feedback to enable the algorithm accumulated error to decay at the same rate as the LR circuit. The block diagram is presented below:

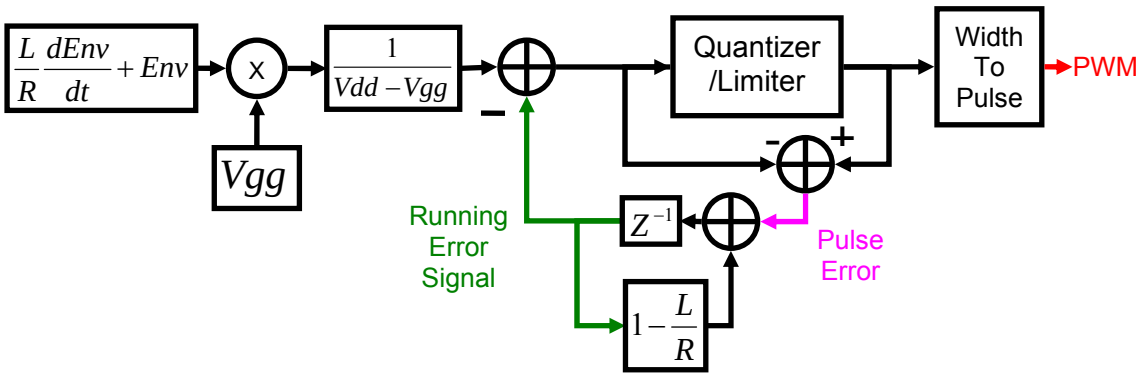

Figure 21: Block diagram of digital time-quantization based PWM.

Another featured added to PWM generator is the ability to impose maximum and minimum pulse widths sent to the envelope amplifier. These limits are imposed inside of the quantizer along with the time-quantization. Figure 22 gives sample waveforms from the system described in the block diagram of Figure 21:

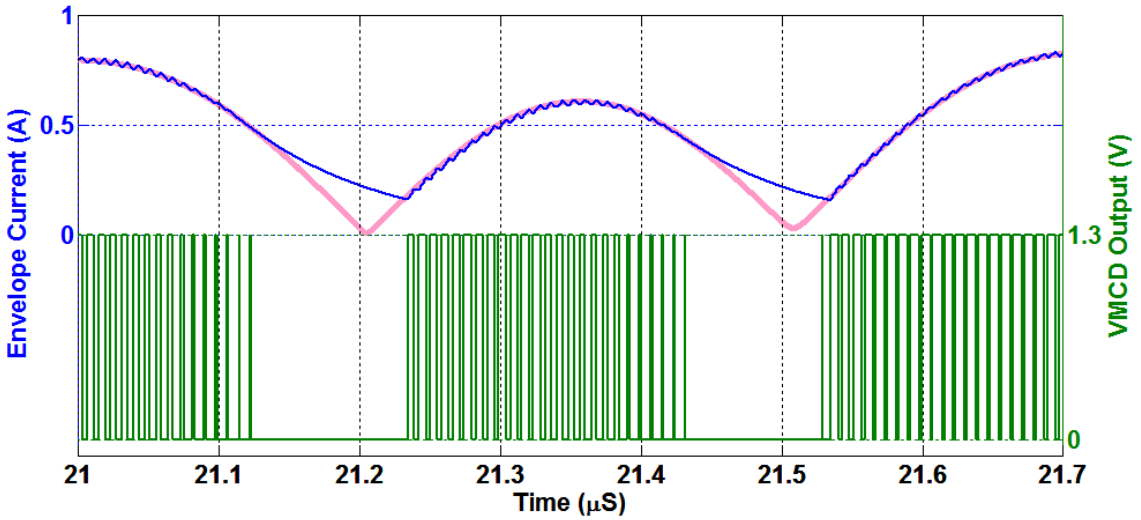

Figure 22: Sample simulated waveforms from the time-quantized PWM system. Envelope inductor current is shown on top (dark blue) along with the ideal envelope (light red). The PWM switching waveform is show at the bottom (dark green).

The modulator generates PWM waveforms that cause the envelope inductor current to track the envelope waveform as closely as possible, given limited supply voltages. When slew rate errors occur, the modulator accumulates the error with the proper decay, and then continues switching when accurate tracking of the envelope waveform is again possible.

The same simulation performed for Figure 20 was rerun with the improved time quantization algorithm given in Figure 21. Even after elimination of the persistent envelope error, spectral degradation, from the inability of the inductor current to track the fall rate of the ideal envelope signal, is prohibitive to meeting WCDMA standards. The next sections examine methods to minimize this degradation.

9.4. Pulse Density Modulation in the Phase Path

In a traditional polar amplifier, the phase signal is always constant envelope. Envelope tracking (ET) transmitters are similar to polar transmitters, in that ET transmitters use the same envelope signal as a polar system, but use the full signal on the gate/base of the amplifier instead of a constant envelope phase waveform. ET has been shown to be less sensitive to errors in the envelope signal [1].

Using a signal with a varying envelope on the gate/base line of the CMCD amplifier is not an option, as it would require an analog signal path, and the CMCD amplifier would not be running in full saturation. Using a quantization algorithm, such as delta-sigma on the phase line, is a possibility, but as the phase signal is multiplied in the time-domain with the envelope signal, the quantization noise generated by the delta-sigma modulator will be convolved with the envelope signal, along with the quantization noise from the envelope modulator. Using any sort of delta-sigma like noise shaping algorithm will result in broadband noise arising from the shaped quantization noise on the phase path convolved with the harmonic noise generated by PWM on the envelope path. The net result would be broadband noise across the entire band, including the receive band.

Using band-pass PWM directly on the phase path involves changing the width of the already high clock rate phase signals. The high-band carrier frequencies for WCDMA are typically around 2 GHz. To achieve the time resolution control necessary to meet specifications, a PWM resolution of tens of picoseconds is required. Even when using the techniques presented in chapter 5, time resolutions are expected to be poorer than what is required here.

The proposed solution is to adopt a hybrid amplifier, where the system takes on properties of an ET system when needed; that is during the high slew rate envelope signal zero crossings. The output signal will then track all the way down to zero envelope, despite the residual inductor current, by selectively dropping phase pulses sent to the CMCD in their entirety. Dropped pulses will introduce more quantization noise into the system, but fortunately only at points where the system already is at low envelope amplitudes, reducing the power of said quantization noise.

The pulse dropping is done in pulse groups, with the groups varying in proportionality with the inductor current error, where the phase pulse groups are selected at the same frequency as the envelope PWM pulse rate. This frequency plan causes the phase pulse dropping quantization noise to follow the same spectral harmonic pattern as the envelope quantization noise, staying out of the receive band. Unlike the envelope case, any noise added into the phase path is directly passed to the output, as the phase path does not contain an equivalent to the inductor found in the envelope path.

The block diagram of the proposed system, with the addition of the PDM on the phase system, is shown below:

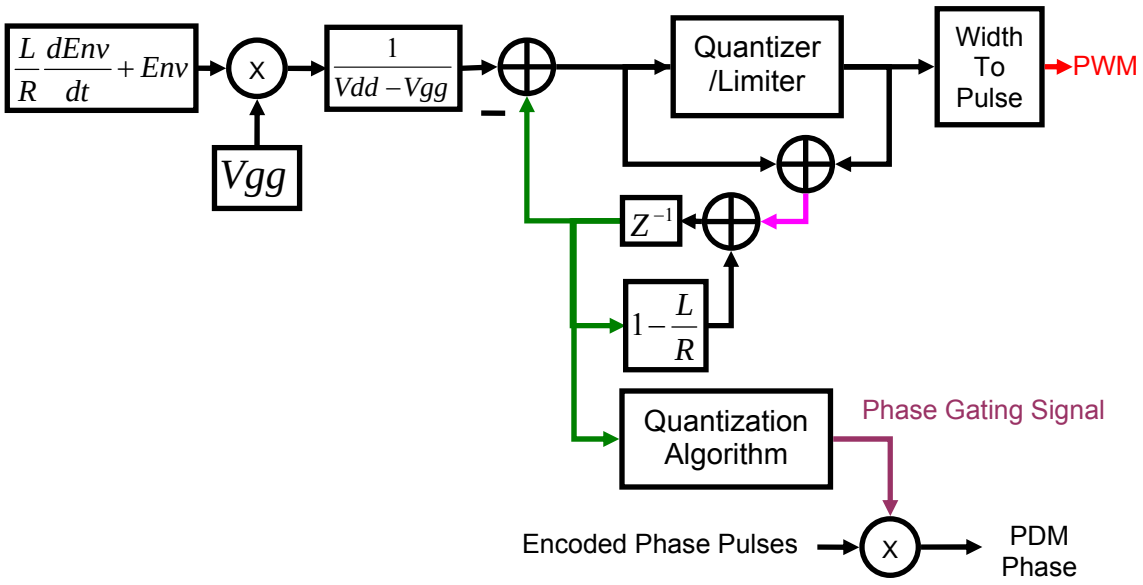

Figure 23: Block diagram of VMCD/CMCD drive algorithm with hybrid EER/ET.

Pulse dropping is achieved by a gating signal that is subsequently multiplied with the phase signal. This gating signal is generated by using a PWM-like algorithm to quantize the error signal. Recall that the error signal is the difference between the voltage required to achieve ideal envelope current on the inductor, and the actual current. Simulated waveforms from the hybrid EER/ET are presented below:

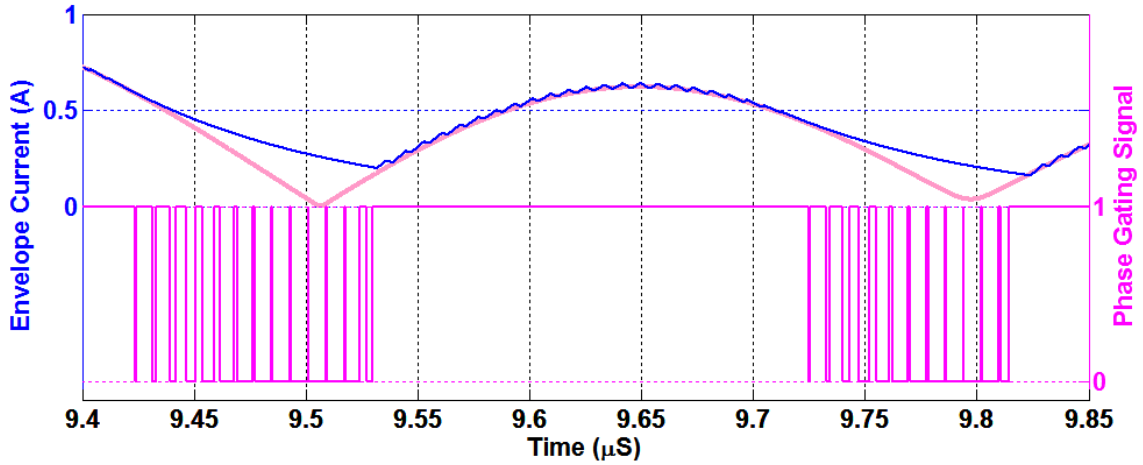

Figure 24: Simulated waveforms from hybrid ET/EER driving algorithm. The top shows an ideal envelope (light red) and the envelope inductor current (blue). The bottom shows the phase gating signal (cyan).

The phase gating signal is constantly held high when the inductor current is accurately tracking the envelope signal. When the envelope inductor current fails to track the envelope, phase pulses are dropped in such a manner that the fraction of pulses dropped multiplied by the envelope inductor current equals the ideal phase signal magnitude. This allows the time-average of the transmitted signal envelop to match that of the ideal envelope.

Figure 25 shows the simulated spectrum of the hybrid ET/EER amplifier with noise reduction in the near-band:

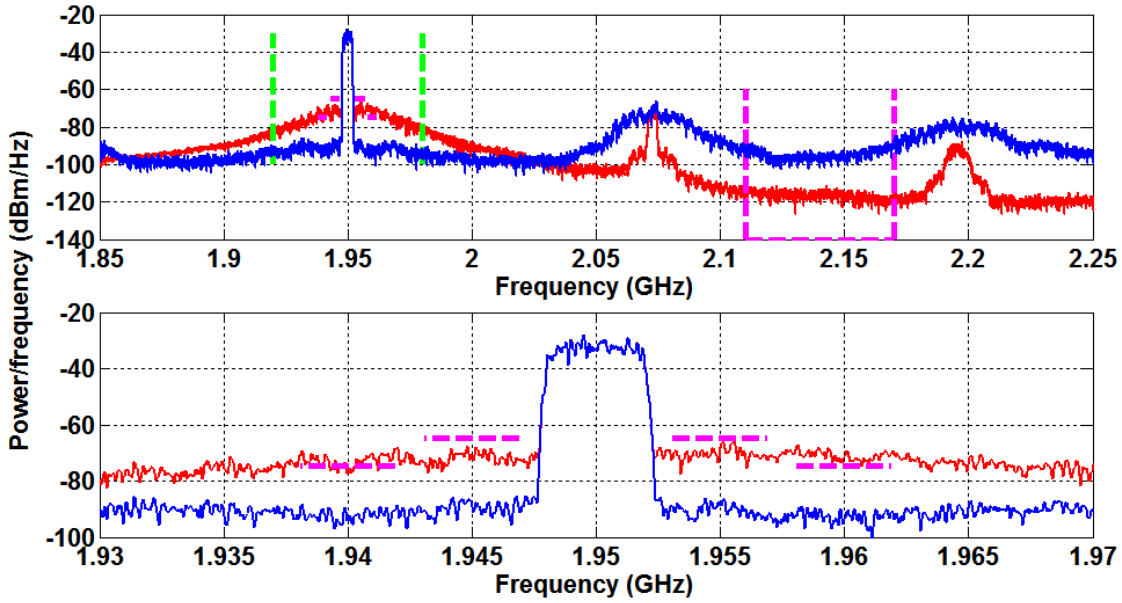

Figure 25: Spectra of VMCD/CMCD hybrid ET/EER system (blue). Spectra of an uncorrected system (red) are shown for comparison.

The increased broadband noise is due to the simulation noise floor rising significantly, which in turn results from both phase and envelope path suffering from finite time quantization noise. Prior simulations only had noise added on the envelope path. Simulations using the direct-to-frequency domain technique presented in chapter 6 are computationally intensive, but should be possible with subsequent generations of computers.

10. Polar System Broadband Noise Generation

As polar amplifier designs move into the realm of full-duplex communication systems, broadband noise performance of polar amplifier systems becomes a significant design challenge. This section examines simulation of some fundamental parts of polar amplifier systems that cause generation of undesired broadband noise

10.1. Finite Bandwidth Signals

Most modern baseband signals are generated digitally. The finite bandwidth of the DAC and reconstruction filter chain can dramatically affect the broadband noise generated by a polar transmitter. Ideally, the Cartesian-to-polar conversion causes a bandwidth expansion in both the envelope and phase signals, which is later negated when these signals are multiplied together in the polar. Considering the following signal spectra:

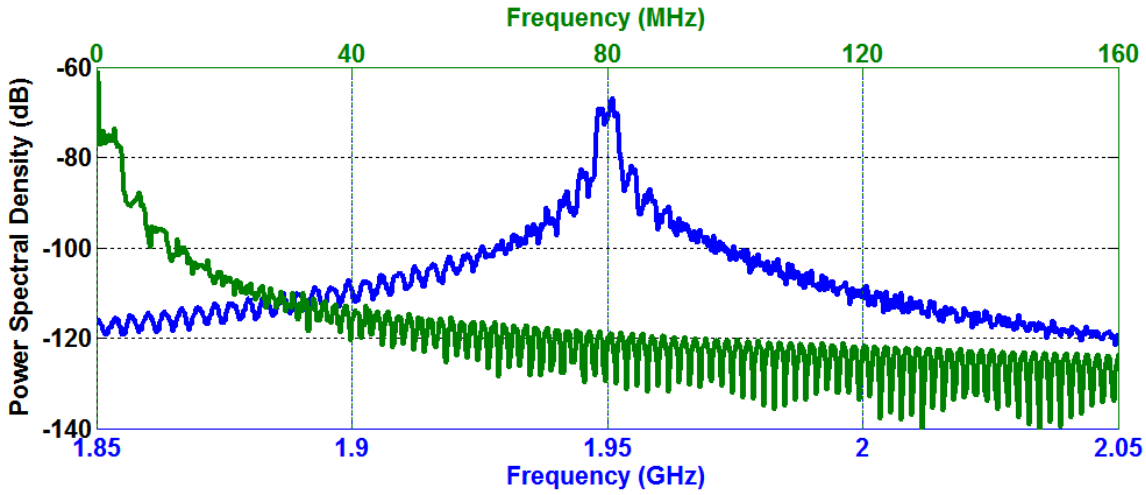

Figure 26: Polar representation of WCDMA signal. Envelope with a peak at DC (green) is shown with a sine encoded phase signal with a peak at 1.95 GHz (blue).

The phase and envelope signal spectra show the bandwidth expansion of the Cartesian-to-polar conversion. Ideally, when these signals are multiplied back together in time domain, the skirts disappear. This occurs because the added frequency components are phased such that the multiplication causes them to fold back into the desired signal. If the envelope and phase signals are band limited, this property no longer necessarily applies.

Filtering an individual signal changes the amplitude and phase relationship of the Cartesian-to-polar bandwidth expansion products, such that they no longer fold spectrally back in-band. This filtering can dramatically alter the broadband noise properties of the signal, without noticeably affecting the spectra of the in-band signal. Due to the large dynamic range between the power spectral density required at typical receive band offsets and transmit power level, the additional power lost in-band is very small.

A simulation was setup to demonstrate the broadband noise characteristics of polar transmitter systems. The source signal is the WCDMA signal that has been used in previous parts of this chapter. The envelope was passed though a quantizer, then a zero-order hold, and finally a low-pass filter. This sequence of operations was chosen to closely mimic a DAC. The signal was then multiplied by the unchanged sine wave encoded by the phase signal, at the simulation sampling rate of 6.3 GHz. The simulation block diagram is as follows:

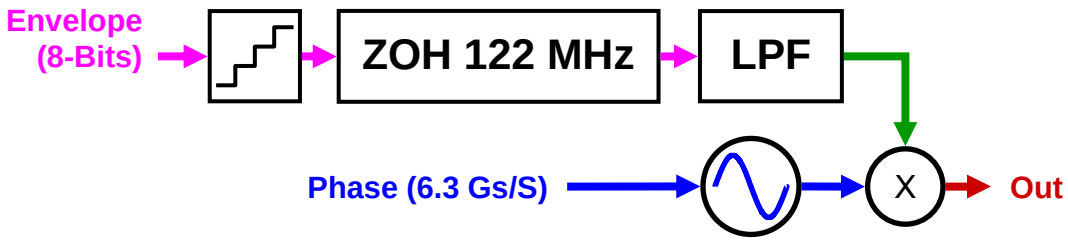

Figure 27: Simulation block diagram.

This simulation was run for two different low-pass filter bandwidths, and, for reference, no filter. Importantly, to isolate this simulation from the effects of the phase shift caused by most realizable filters, a non-causal, phase-shift-free forward-backward filtering operation was used. The filtering operation chosen was a low-pass Hamming-window

based linear-phase FIR filter twice: once with time increasing, and again, with time decreasing (backwards time). This results in the frequency transfer function being squared in magnitude, and the phase distortion of the two filtering operations cancelling each other out [2]. The resulting spectra from the above simulations are given below:

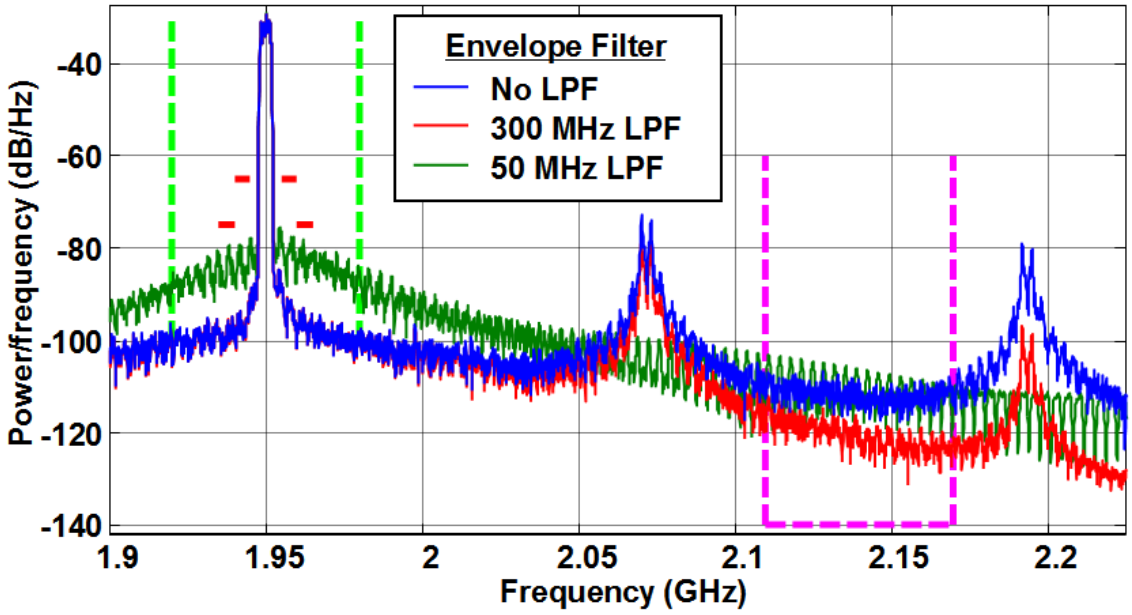

Figure 28: Simulated WCDMA spectra for a polar system with an unfiltered phase signal, and modeled DAC with different reconstruction filters.

The broadband noise of this test system improves with some filtering, and then degrades with heavy filtering. The in-band spectral performance is degraded by the heavy filtering, and is unaffected by the lack of filtering. The wide bandwidth skirts of the unfiltered phase signal are no longer cancelled out by the wide bandwidth skirts envelope signal. The solution to the phase skirts creating wide-band noise is to filter the phase signal to match the bandwidth of the envelope path. This can be achieved by either low-pass filtering the zero frequency centered phase signal, or band-pass filtering the RF encoded phase signal.

A simulation was performed, similar to the last block diagram, with the addition of a low-pass filter in the phase path prior to RF modulation:

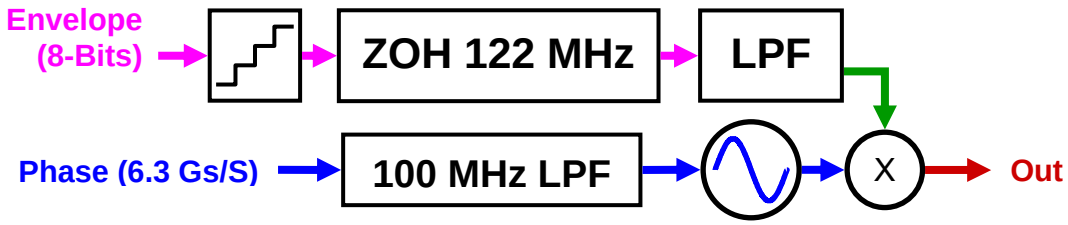

Figure 29: Block diagram of simulation with added phase filter.

Again, forwards-backwards filtering was used to remove any phase delay effects on the simulation. The following spectra show the phase filter improvement:

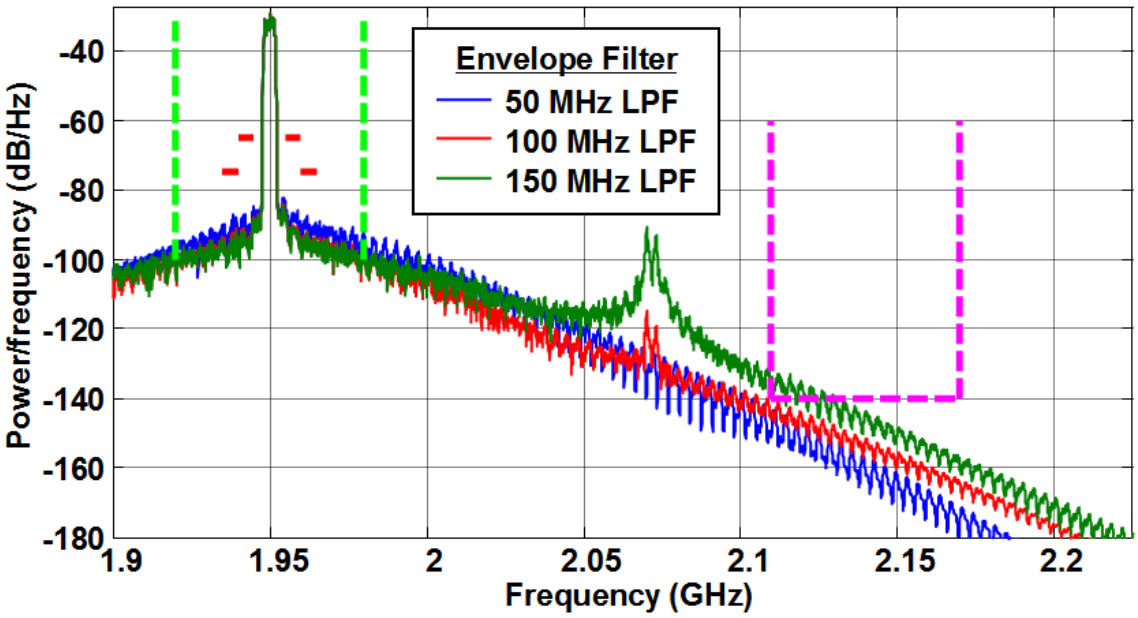

Figure 30: Simulated WCDMA spectra with filtering on both phase and envelope paths.

The broadband noise in the polar system is significantly reduced by matching the bandwidth between the two paths of the system.

10.2. Time Alignment

Another source of broadband noise generation in polar transmitters is phase/envelope time misalignment. Previous studies have linked polar time misalignment with ACPR degradation [3]. A simulation was setup to characterize the broadband noise in time misaligned polar transmitter systems. The block diagram is as follows:

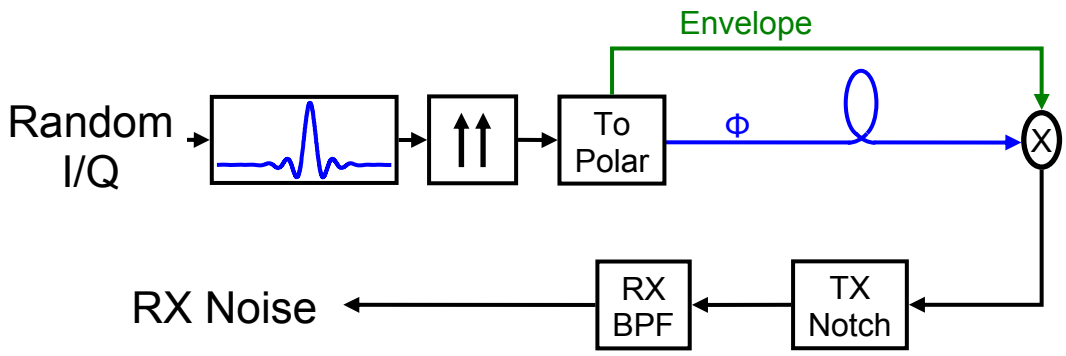

Figure 31: Block diagram of time misalignment simulation.

The simulation starts by generating a WCDMA-like baseband signal by running random chips though a pair of root raised cosine filters at an oversampling rate of 128, resulting in a 492 MHz baseband sampling rate. The signal is then upsampled by another factor of 16 for a sampling rate of 7.9 GHz and then filtered with a low pass filter. The I and Q signals undergo a rectangular to polar conversion. The phase signal is then delayed relative to the envelope signal to represent the time misalignment of the system. The resulting signal is then reconstructed by a phase modulated signal at the UMTS band I uplink frequency of 1930 MHz. The signal was subsequently scaled to have 33 dBm of in-band power for proper absolute power spectral density results.

The delay was chosen such that the signal met ACPR specifications, but had significant noise in the RX band. The delay for this simulation was 5 nS. The polar reconstruction of the misaligned signal has the following spectrum:

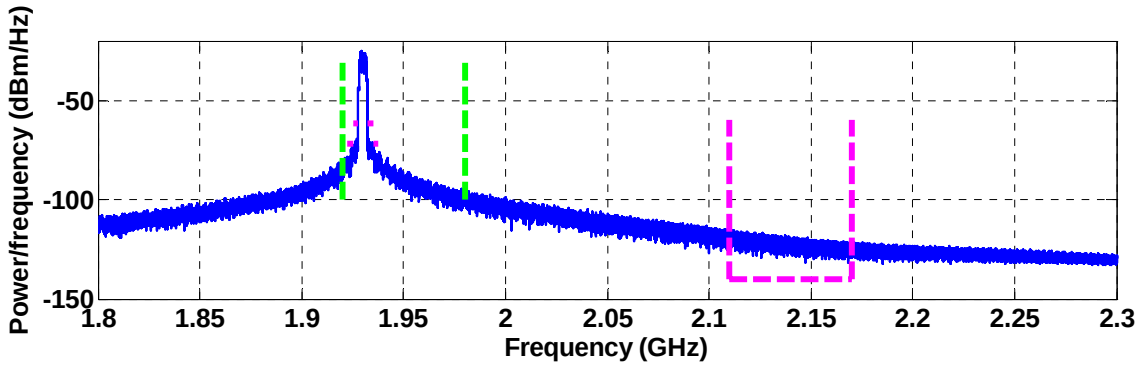

Figure 32: Spectra of the time-misaligned signal.

The distorted signal was then run through the notch filter and subsequently the band-pass filter. Both filters are Chebyshev type II filters. Chebyshev type II design was chosen for its efficiency and passband flatness. Again, the forwards-backwards method was used to eliminate phase distortion, so the filter phase response is eliminated from consideration. The transfer functions of the filters are as follows:

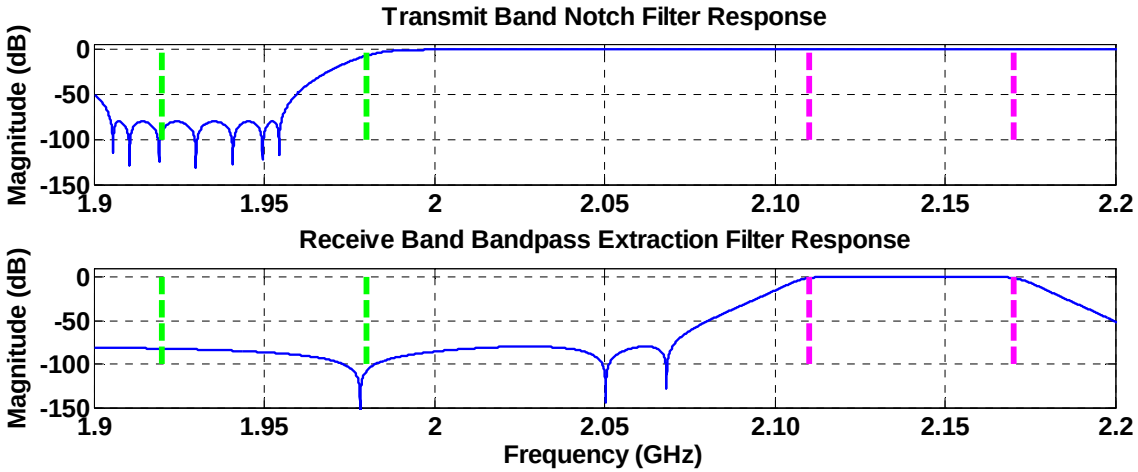

Figure 33: Frequency response of digital extraction filters: notch (top) and band-pass (bottom).

For verification the spectrum was examined post filtering:

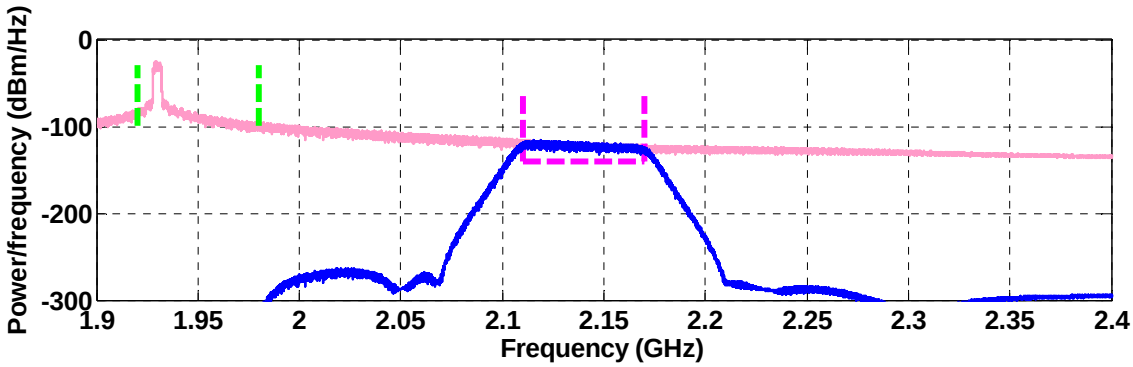

Figure 34: Spectrum of RX band extraction (blue), shown with unfiltered distorted signal (light red).

Insight comes from looking at the time domain output of the filter bank versus the envelope of the WCDMA signal, plotted below:

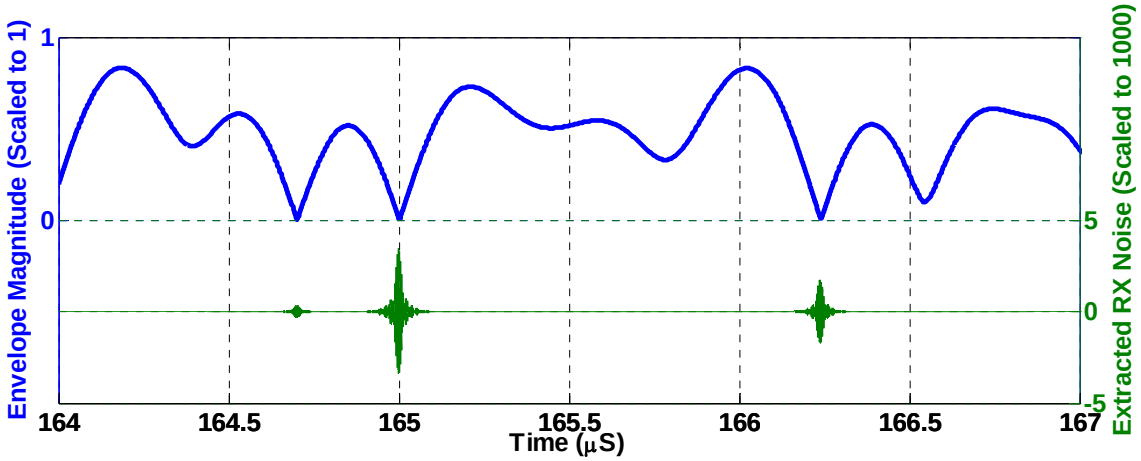

Figure 35: Time domain of WCDMA envelope (blue, scaled to maximum of 1) and time domain of extracted RX band noise (green, scaled 1000x larger in magnitude).

The wide-band noise generated by the time-misalignment is not continuous, but rather comes in distinct bursts. Not surprisingly, these bursts are highly correlated with the zero-crossings that have been previously shown to cause bandwidth and slew rate expansion. All of the noise bursts occur during times that the envelope trajectory makes

a transition near the origin in the I/Q complex plane. Zooming in on the worst noise event in the above plot, noise peak are seen to occur simultaneously with the minimum in the envelope signal:

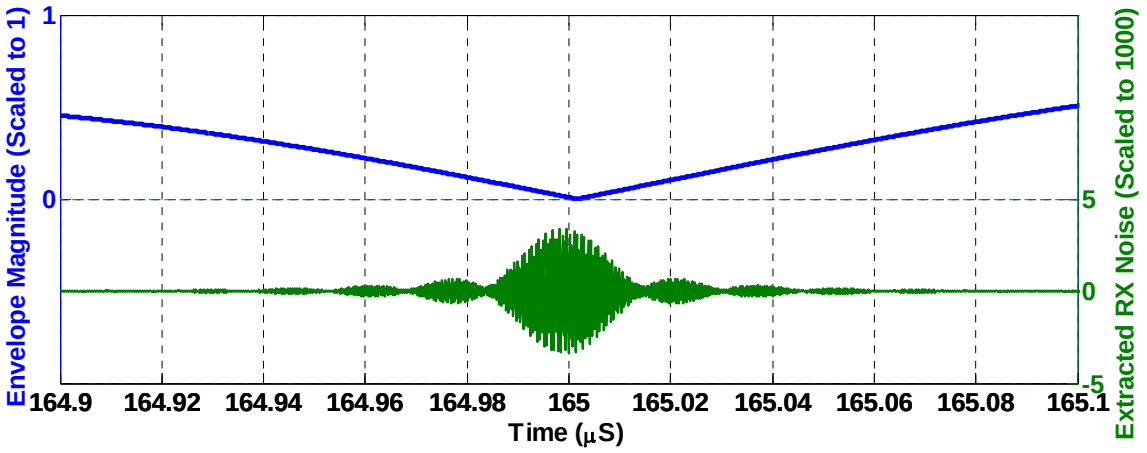

Figure 36: Zoom of worst noise burst in the sequence used in Figure 35.

The non-causal behavior of the noise pulse is expected, and is a result of the forwards-backwards filtering. The non-causality centers the noise pulse on the generating event, as opposed to realizable systems, where the noise pulse would occur after the filter's group delay. The delay-free filtering makes identifying the source event much simpler.

Software was developed to automatically parse though the simulation data, and log the amplitudes of the noise events, and the envelope trough minima that cause these noise events. The simulation was then run for 2000 chips of a WCDMA signal, and the relevant parameters were extracted from the zero-crossings. The first pass data was less than insightful, as shown in the scatter plot of Figure 37:

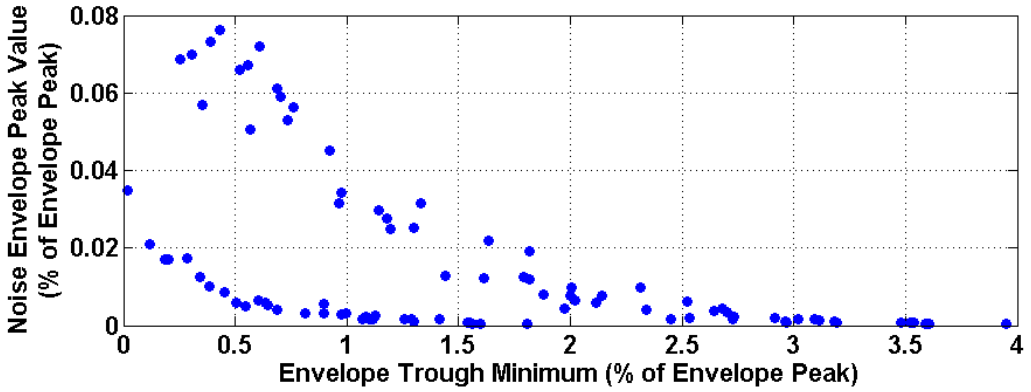

Figure 37: Scatter plot of noise magnitudes vs. envelope minima.

The amplitudes of the noise bursts generated appear to be strongly correlated to the minimum of envelope reached during the zero-crossing, but the simulated scatter plot shows that there is not a simple relationship. The nature of the relationship is explored analytically in the following section.

10.2.1. Time Misalignment Error Derivation

Starting with the complex definition of a signal, s(t), from the polar representation: envelope represented by E(t), and phase represented by θ(t).

$$s(t) = E(t) \cdot e^{j\theta(t)} \tag{10}$$

We define a time misaligned signal ŝ(t) by advancing the phase signal by a factor of Δt:

$$\hat{s}(t) = E(t) \cdot e^{j\theta(t+\Delta t)} \tag{11}$$

We then define the error signal r(t) as the complex vector difference between the two signals:

$$r(t) = s(t) - \hat{s}(t) \tag{12}$$

Substituting the above two equations into the error term, and factoring out the envelope term gives the error as a subtraction of two complex exponentials:

$$r(t) = E(t) \cdot \left[e^{j\theta(t)} - e^{j\theta(t+\Delta t)} \right] \tag{13}$$

Expanding the misaligned phase term using a lowest order Taylor expansion of the phase results in:

$$r(t) = E(t) \cdot \left[e^{j\theta(t)} - e^{j\left[\theta(t)+\theta'(t)\cdot\Delta t\right]} \right] \tag{14}$$

Finally substituting the original definition of the polar signal back in, gives the simplified error signal:

$$r(t) = \Delta t \cdot \theta'(t) \cdot j \cdot s(t) \tag{15}$$

In reality, what is desired is the Fourier transform of the above equation during a zero crossing event. Setting the signal to the following gives a simple case of a polar zero crossing.

$$\cos(\omega t) + j \cdot m \tag{16}$$

Here, the example signal takes a trajectory that comes within m of the origin. Taking the derivative of the phase of this zero crossing example gives:

$$\theta'(t) = -\frac{\omega \cdot m \cdot \sin(\omega t)}{m^2 + \cos(\omega t)^2} \tag{17}$$

Here we can see that the phase slope is not well-defined during a zero-crossing (m=0). In actual systems, the slope will depend more on the bandwidth and sampling rate of the particular implementation. We will just rely on the numerical derivative of the phase to estimate the magnitude of the noise created in the RX band. Using the phase slope results in the following plot:

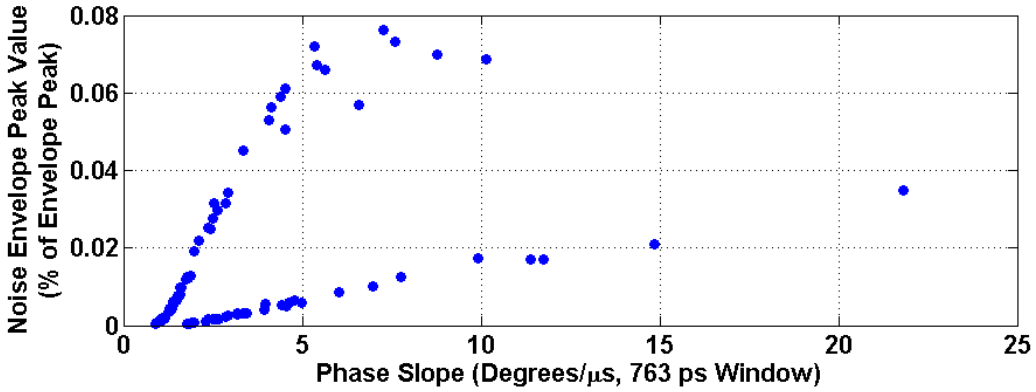

Figure 38: Simulated RX band noise versus zero-crossing absolute value of phase signal slope.

From the dual slopes evident in the plot it is clear that another factor is missing. The next section will examine the differences between the two linear dependencies of the RX noise amplitude.

10.2.2. Time Misalignment Error Trajectory

Plotting the time domain of two similar zero-crossings that have virtually identical slopes, but generate significantly different noise amplitudes, i.e. one pulse from the top curve, and one pulse from the bottom curve results in the following two constellations:

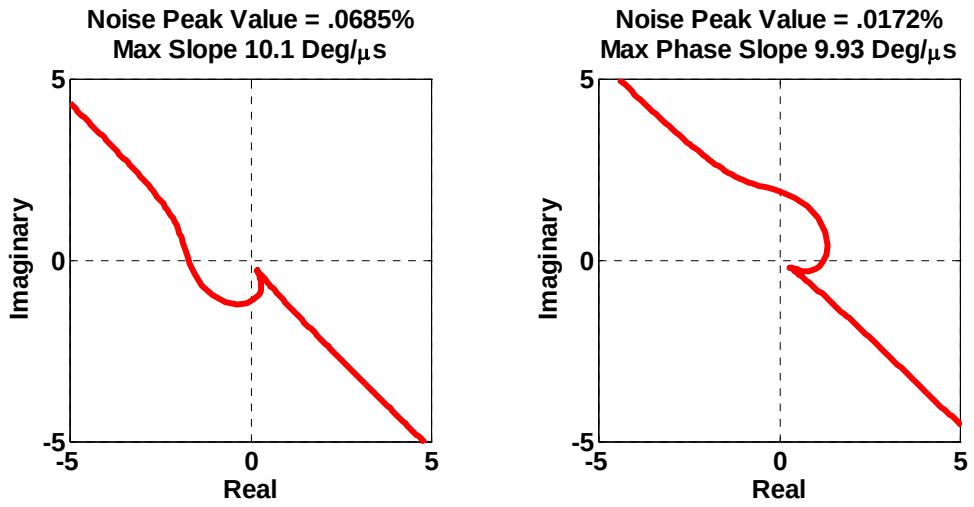

Figure 39: Two zero-crossing trajectories: left is selected from the higher linear dependency and right is selected from the lower linear dependency.

After examining many of these zero crossing trajectories, the only important difference is the difference of the trajectory. The left plot has a clockwise rotation around the origin, and the right plot has a counterclockwise rotation around the origin. A clockwise rotation causes more of the error energy to end up in frequencies higher than the transmit frequency, and the inverse is true for a counterclockwise rotation. Separating out the directionality results in the following plot:

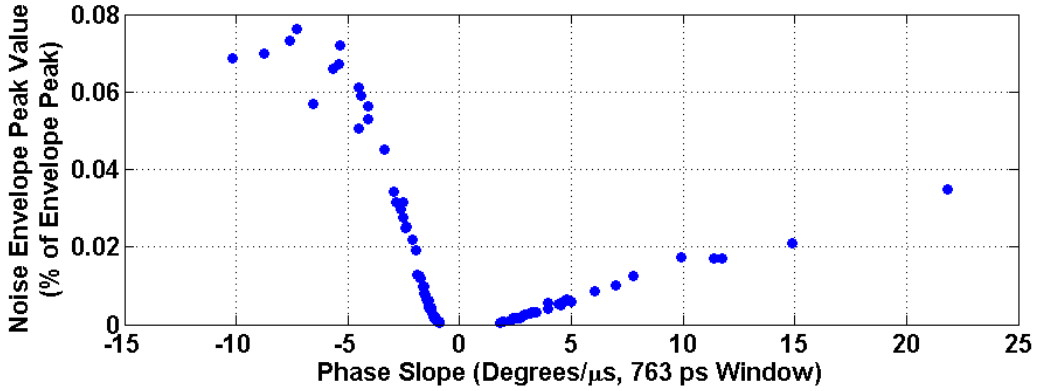

Figure 40: Simulated RX band noise versus zero-crossing phase signal slope.

A linear relationship for the smaller noise bursts exists between the slope of the phase and the amplitude of the noise generated. The slopes are different for positive and negative phase transitions, due to the positive frequency offset of the receive band. This would be inverted in the case of a RX band located lower in frequency, as in most base-station frequency allocations. This linearity breaks down during the highest noise events, due to sampling rate non-idealities present in the simulation.

10.2.3. Envelope Pre-distortion for Broadband Noise Suppression

This section explores the possibility of suppressing broadband noise generation in polar systems without having to accurately align the phase and envelope path. In the previous sections, we have seen that broadband noise in polar amplifier systems, caused by time-misalignment, occurs when the phase signal undergoes rapid slewing when then envelope signal is at a non-zero value. As has been shown in the ideal polar signal, during a zero crossing, the envelope remains at zero for a very short period of time, and the phase undergoes an almost instantaneous change. Ideally, this rapid phase change is multiplied by the zero-envelope, and no noise is generated. However, time misalignment causes the rapid slewing phase to be multiplied by a non-zero value.

Small deviations in time-alignment can be made noise-free by expanding the amount of time the envelope signal spends at zero. A tradeoff is additional noise due to the trajectory differing from the path set by the pulse shaping filter. The most simplistic of these systems would threshold the envelope signal, such that any envelope value below the threshold would be set to zero. This thresholded envelope signal is then run though a low-pass filter to remove noise caused by the switching transient. A simulation of this

system was setup. A zoom of the envelope signal, during a zero-crossing event shows the original signal, and the new predistorted signal:

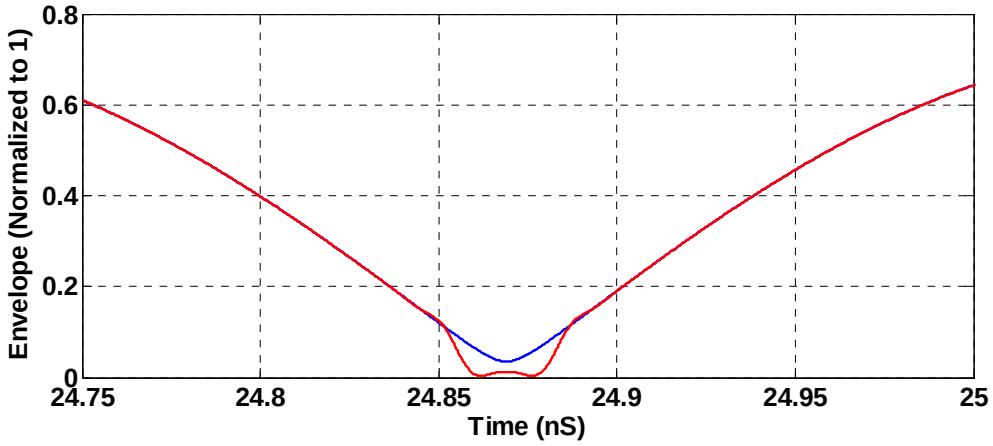

Figure 41: A subset of the time domain of the predistorted envelope signal (red) is compared with the original signal (blue) during a zero-crossing event.

The signals are equal for all times besides zero-crossings. This technique effectively moves the signal noise power closer into the transmit signal. This can be desirable because most communication standards allow for much higher leakage power in the transmit band than for the receive band.

Applying this predistortion technique to the example polar system, ideal in every aspect except for a 5 nS time misalignment, results in the following spectra:

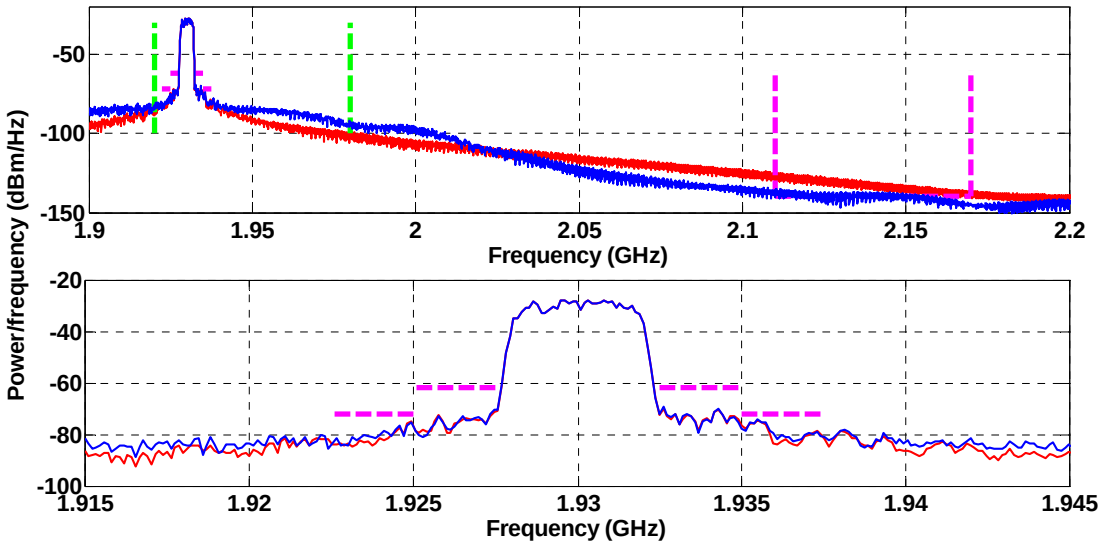

Figure 42: Spectra of misaligned polar system with predistortion (blue) and without predistortion (red).

The predistortion technique lowered the RX band noise by 10 dB at the expense of a 10 dB higher noise floor in the near-TX band. This is a highly desirable tradeoff as typical regulatory in-TX-band spurious emission limits (-73 dBm/Hz here) are easier to meet with polar systems. In this example, the predistortion technique allows the simulated spectrum to become spectrally compliant.

11. Conclusion

A unique, hybrid polar amplifier system was presented, analyzed, and simulated. Many of the presented ideas and analyses of issues relating to polar amplifier systems are broadly applicable to the entire class of polar transmitters. Unique properties of broadband noise generated by polar amplifiers were explored. A novel predistortion technique was presented that can shift noise out of the RX band.

12. Acknowledgments

The author would like to acknowledge the helpful discussions about this topic with many different individuals, most notably Dr. Calogero Presti and Paul Draxler.

13. References

[1] F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P.M. Asbeck,L. Larson, "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications" in Microwave Theory and Techniques, IEEE Transactions on, vol. 52, iss. 12, pp. 4086-4099, December 2006.

[2] Oppenheim, A.V., and R.W. Schafer, *Discrete-Time Signal Processing,* Prentice-Hall, 1989, pp.284–285.

[3] C. Presti, F. Carrara, G. Palmisano, A Scuderi "A High-Resolution 24-dBm Digitally-Controlled CMOS PA for Multi-Standard RF Polar Transmitters", in *IEEE Journal of Solid-State Circuits*, vol. 44, iss. 7, pp. 1883-1896, June 2009.

Chapter 8

Fractional-N Direct Frequency Synthesis

1. Introduction

Modern communication systems, even those using multiplexing techniques other than frequency division multiplexing, typically rely on frequency channelization to increase network capacity. Many of the digital transmitter systems presented in previous chapters require an agile frequency source to transmit on a range of channels, across an assigned frequency band. Traditional communications systems use manually tuned local oscillators that directly generate the necessary frequency to transmit on a given channel. Unfortunately, these traditional variable frequency references are not accurate enough for digital communication standards, since newer communication standards demand the use of an accurate, coherent frequency source. Quartz crystals can provide the necessary accuracy and stability, but are fixed in their output frequency. In order for a transmitter to operate across these channels, a frequency synthesizer must be employed to generate a range of frequencies from a fixed reference frequency.

2. Frequency Synthesis

Traditional frequency synthesis techniques include phased locked loops (PLL) and direct digital synthesizers (DDS), whose design is challenged by steadily increasing application requirements including high frequency output, large tuning range, small settling time, easy integration with digital systems, and simple implementation.

One of the issues with many current frequency synthesis techniques is the use of tuned analog circuitry or complicated high-resolution, high-speed digital-to-analog converters (DACs). These analog circuits can be difficult and inefficient to implement in many of today's digital IC processes, resulting in poor economics. Current efforts are underway to implement highly integrable frequency synthesizers [1].

The DDS method proposed here consists entirely of digital circuitry, making integration into existing systems-on-chips much easier. The present system is an open-loop based system, offering nearly instantaneous settling, not possible with closed-loop frequency synthesis systems. Fast settling time allows a designer to modulate the output signal by simply varying the input to the frequency synthesizer at the modulation rate. Modern wireless systems have steadily increasing data rates, demanding wider bandwidth modulation systems, which the proposed synthesis system can address.

The architecture discussed in this work, with its flexibility and integrability, has potential applications in software defined radio systems. The system's speed, combined with large scale digital integration, makes possible the generation of complex waveforms for phased array radar and instrumentation applications.

3. Fractional-N Direct Frequency Synthesis

The system proposed here to generate arbitrary frequencies comprises a reference frequency (f_{ref}) driving a programmable divide-by-N counter, where the modulus, b[n], is supplied by a quantization system as shown in Figure 1. In the simplest implementation, the output of the divide-by-N counter clocks in the next number in the b[n] sequence. Clocking the quantization system with the output of the frequency synthesizer alleviates

the need for the phase accumulator and the phase-to-sinusoid lookup table. As a result of this clocking scheme, the synthesizer will change frequencies only at the zero crossings.

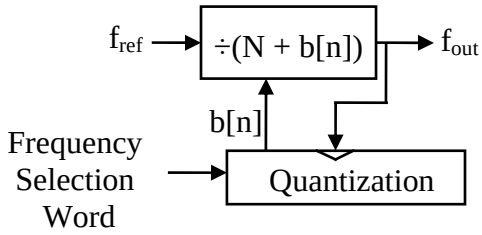

Figure 1: Fractional-N Direct Frequency Synthesizer

The system is similar to the existing feedback circuitry found in standard, closed-loop fractional-N PLL. Unlike previous work, this system is used outside of a feedback loop and more divider states are employed than in a typical closed-loop fractional-N PLL application.

Due to this DDS system's lack of phase noise suppression, the output of the multi-modulus divider should be retimed with the reference clock to ensure low output jitter (not shown in Figure 1).

During operation, the frequency selection word, inputted to the quantization system, determines the output frequency (f_{out}). The tuning step of the system is only limited by the quantization system, and can be arbitrarily increased at the cost of complexity.

Inasmuch as the output only affects the clocking of the quantization system, the DDS system can be considered to be open-loop. Due the faster of settling time in open-loop systems, the output can be modulated rapidly with any constant envelope technique by rapidly varying the frequency selection word. Such systems eliminate the need for

mixers, and allow the DDS to become a de facto transmitter, which can couple directly to a power amplifier and antenna for systems with constant envelope signals.

The programmable multi-modulus divider instantaneously generates outputs that are only integer submultiples of the reference frequency. Frequencies that are non-integer submultiples of the reference frequency are generated by employing a quantization scheme. Typically the quantizer hops between the different integer submultiples in such a way that the outputs average to the desired frequency. Creating arbitrary values by hopping between integer values creates unwanted power, or quantization noise, as a side effect. This quantization noise needs to be shaped in the frequency domain to remove it from the vicinity of the desired tone and spread it evenly throughout the band to keep the in-band noise and spurs low.

Unfortunately, the amount of quantization noise generated by this system is a dynamic, signal-dependent value, since the spacing between the quantized frequency values changes as a function of N and b[n]. For example, when N is 6, there is a much larger frequency difference between outputs when b[n] transitions from -2 to -3 than when it transitions from 1 to 0. For this reason, the quantization noise increases, as a fraction of the total power, as the synthesis system is tuned to higher frequencies. This effect is only pronounced when operating at high f_{outmax}- f_{outmin} to f_{ref} ratios.

When the system is tuning to frequencies greater than one-half of the Nyquist frequency, it is possible for outputs from the quantizer system to be greater than or equal to the N value of the divider. In this case, two choices can be made: 1) the out-of-range outputs can be limited, or 2) they can simply swallow previous pulses, e.g., when N=6 and b[n] = -7, one previous pulse would need to be swallowed. A sum of zero would just

be dropped from the sequence. Limiting the values keeps clocking simple, but limits the upper range of the system. Allowing the out-of-range quantizer outputs to swallow adjacent pulses makes it possible for the output range to tune almost up to the Nyquist rate of the system. Unfortunately, this complicates the clocking scheme because at higher rates, when many out-of-range outputs occur in a row, the quantization system needs to run at a different data-rate than the output of the multi-modulus divider.

These clocking issues can be solved by placing a buffer between the quantizer and the divider. The quantization system still must run at a higher frequency, but is no longer directly clocked by the output. A timing feedback method is necessary to keep the buffer from emptying or overflowing. For a given tuning range, this is a tradeoff between reference clock speed and system complexity.

In this work, two different quantization systems are demonstrated, delta-sigma and segmented quantization, along with the aforementioned simple non-swallowing fractional division system. The performance of each system is simulated, and the segmented quantization system is also tested in a hardware demonstration for verification of the simulated results.

4. Delta-Sigma Based Fractional-N Direct Frequency Synthesis

In this system, a low-pass delta-sigma modulator selects the value of b[n] using the frequency selection word as the input. Many different variants of delta-sigma modulators exist; here a multi-stage noise-shaping (MASH) architecture is chosen because of its enhanced stability and lower sensitivity to idle tones with constant inputs [2]-[3]. The delta-sigma signal diagram is shown below in Figure 2:

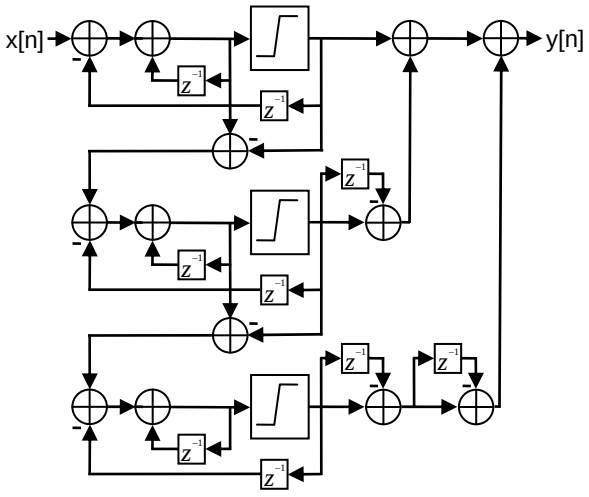

Figure 2: MASH delta-sigma architecture

In a simulation, the reference frequency (f_{ref}) was set at 6GHz. The MASH delta-sigma modulator was setup with three quantizers, and a word-length of sixteen bits. The eight possible output combinations of this MASH system were set to b[n] values of {-4, -3, -2, -1, 0, 1, 2, 3}. The N value was chosen as 7. The LSB of the first integrator has a one-bit dither signal injected to suppress tones.

The maximum and minimum frequency outputs of this delta-sigma based system are limited by the stable operating range of the MASH modulator. The system operates stably from 330 MHz to 425 MHz, as shown below in Figure 3. The noise floor shape changes slightly over the band, but is no worse than -85 dBm/Hz. In-band spurious tones are observed at -50 dBc, as well as near-band spurs at -45 dBc.

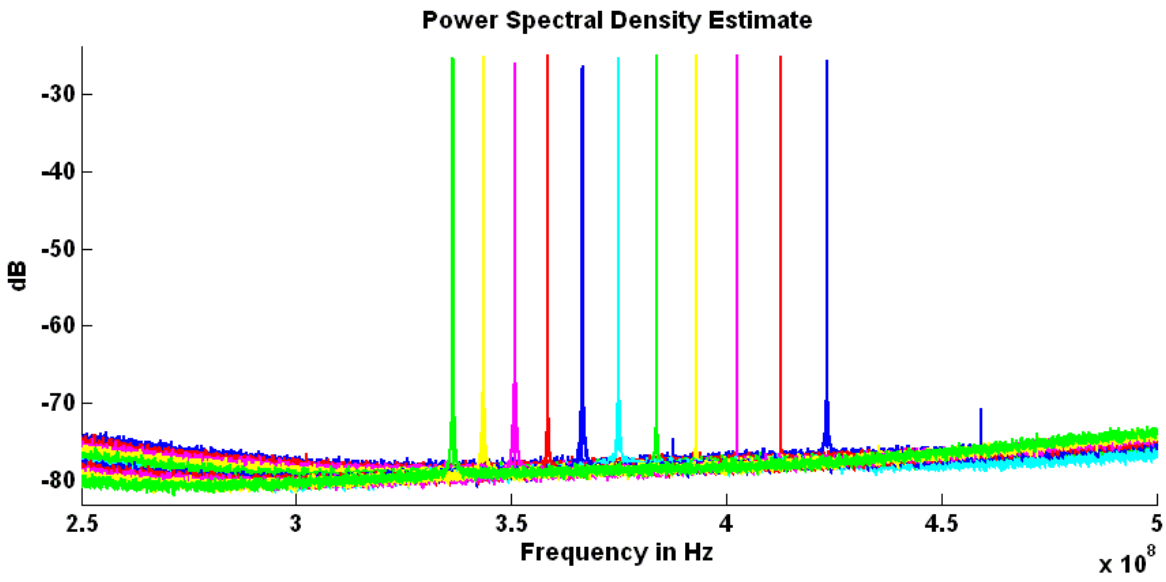

Figure 3: MASH based frequency synthesizer maximum and minimum simulated outputs (32.3 kHz bin width).

The system tuning range here is limited by the stability of the delta-sigma modulator, and spurs encroaching on the band-of-interest. Increasing the stability range is difficult, as stabilizing techniques tend to radically alter the noise shaping properties over the tuning range of the system. A quantization system that is stable over all inputs would allow for a much higher performance system.

5. Successive Requantization

Successive requantization is a technique first introduced in [4] as a digital common-mode rejection technique for an analog-to-digital converter. It has been further extended as an improvement for more traditional fractional-N PLLs in [5].

In successive requantization, the quantization operation is broken into steps, where each step reduces the number of states by a factor of two, as shown in Figure 4. Individual quantizers are added to form a cascade of quantizers until the desired level of overall quantization is reached.

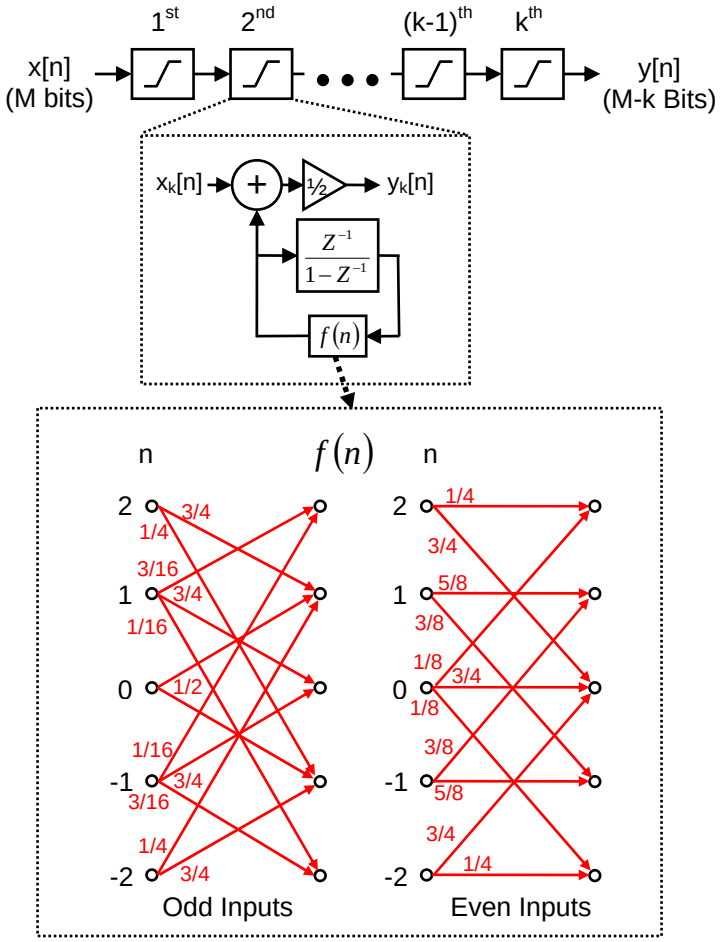

Figure 4: First order noise shaping successive requantization diagram. The state diagram of f(n) is detailed graphically on the bottom. The fractions denote the relative probability of the transition.

The individual quantizers work by adding a sequence of numbers to the input, f(n), in a way that always results in an even number (after which the least significant bit, a zero, can be discarded). The noise shaping in the frequency domain is achieved by bounding the cumulative sum of f(n).

The spreading of the quantization noise is achieved by using probabilistic state transitions in f(n). To avoid spurious tones, the expected value of the magnitude of the state transitions needs to be independent of the input and the modulator state. This also

ensures the quantization noise is independent of the modulator's input history. Lastly, the expected value of the magnitude of the state transitions needs to be balanced, not only in the linear domain, but also for any nonlinearity in the system. Failing to compensate for nonlinearities will result in spurious tones being generated from the quantization noise passing through a nonlinear system.

In this example synthesis system, a five state system is presented, bounded by ±2. This results in a maximum output given by:

$$\left|Y_{\max}\right| \le \left[\frac{X_{\max}}{2^k} + \sum_{r=-1}^{k} \frac{1}{2^r} \right] \tag{1}$$

Advantages of this system include constant quantization noise, spur free operation (assuming a good source of random numbers is used), and stable operation over the entire input range of the system.

6. Successive Requantization Based Fractional-N Direct Frequency Synthesizer

In the next example system, the successive requantization system described above is demonstrated within the frequency synthesizer. The system was simulated with a reference frequency of 6 GHz, as shown in Figure 5. This particular addition sequence yields a frequency output of:

$$f_{out} = \frac{f_{clk}}{2\left[\frac{x_{in}}{2^k} + N \right]} \tag{2}$$

In this case, the tuning range is limited by the third harmonic encroaching on the band of interest on the low end, and the divider's smallest allowable value of b[n] on the

high end (since this system cannot tolerate values of N + b[n] less than two). In this particular case, limiting the tuning range from 380 MHz to 960 MHz gives a simulated noise floor of -85 dBc/Hz and spurious performance of better than -60 dBc. For this frequency plan, all observed spurious tones occur out-of-band. A simulation that differentiates quantization noise from spurs occurring below -60 dBc across the entire band is very computationally intensive.

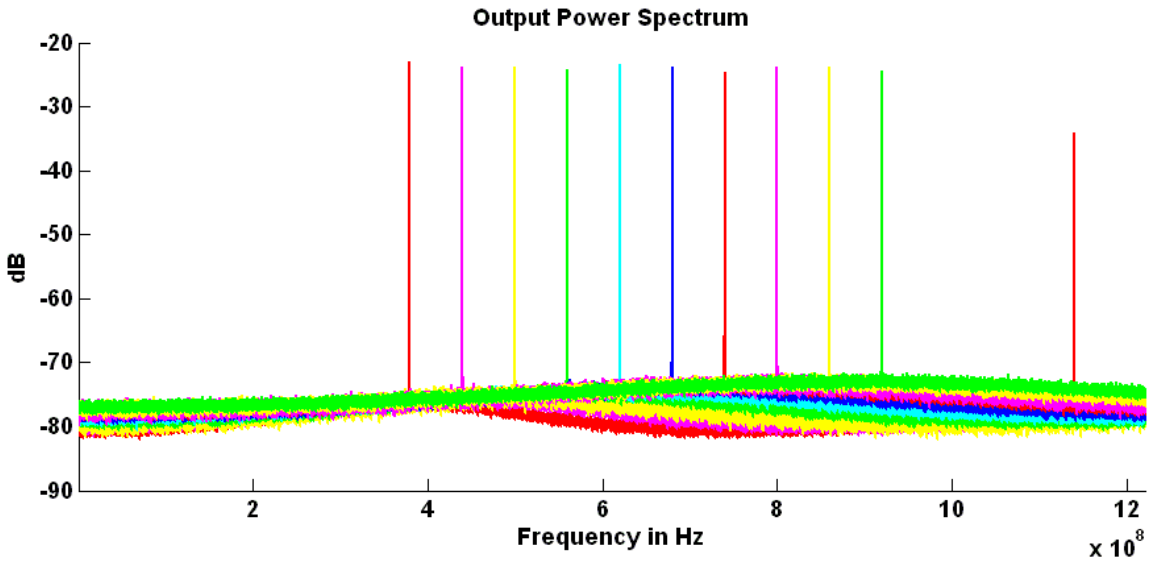

Figure 5: Successive requantization based frequency synthesizer simulated outputs (28.6 kHz bin width).

7. Measurements

The system simulated in Section 6 was tested in a hardware demonstration in order to verify performance. Signals generated in MATLAB were loaded into the 2^{23} bit pattern memory of an Agilent 71612C bit error rate tester (BERT). The signals were then played back at 6 Gbit/sec to verify that the signals can be generated, and ascertain the real world performance.

The measured results degraded slightly compared to the simulation as shown in Figure 6. The worst case noise floor was -80 dBc/Hz. There were no spurs distinguishable from the noise floor. Due to the open-loop nature of the system, jitter on the frequency reference of the system is not attenuated in magnitude by this frequency synthesis technique.

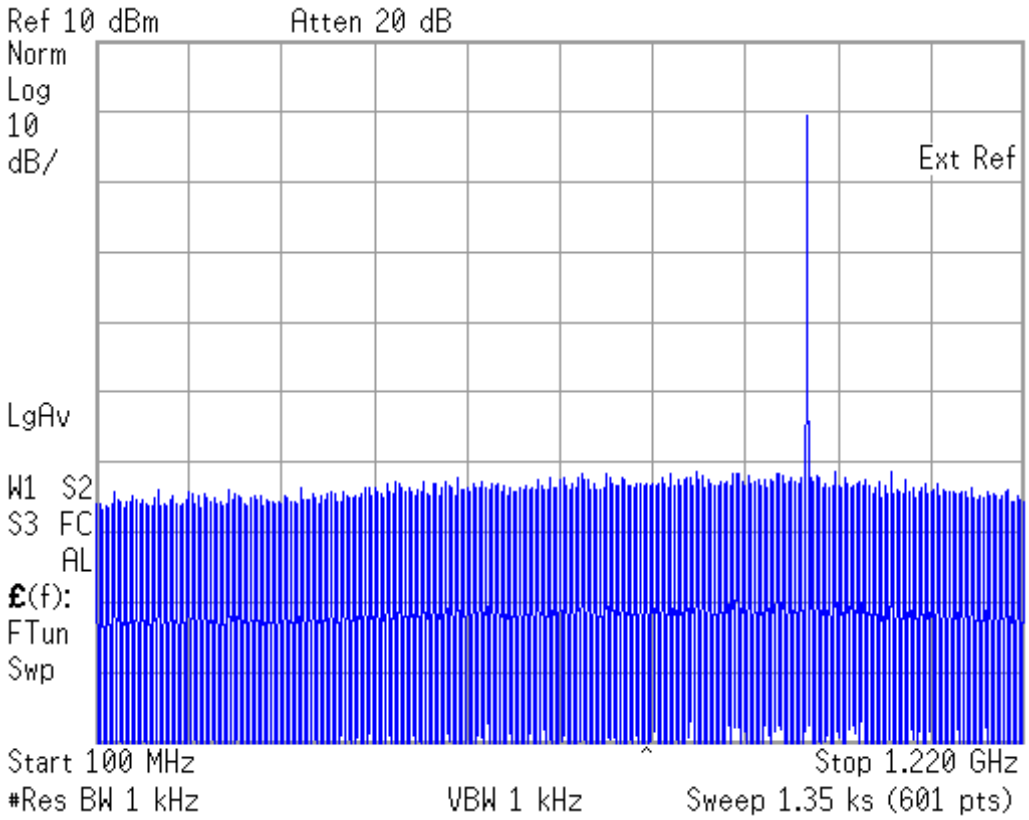

Figure 6: Measured segmented quantization based frequency synthesizer output at f_{out} = 960 MHz

8. Conclusion

A novel frequency synthesis technique with a large tuning range and open loop tuning response has been proposed. The frequency synthesis system is well suited for wide bandwidth systems using constant-envelope modulations (or, with additional amplitude modulation methods, for arbitrary modulation formats). In these cases,

employing this architecture can simplify the design of the transmitter, and ease integration with other digital systems, since this frequency synthesis system can be implemented entirely in digital logic. This system also eases the task of frequency band migration, since the same design can operate at different reference frequencies without any change.

9. Acknowledgments

Some of the material presented in chapter 7 was previously published in [6]. The author of this dissertation was the primary investigator and primary author for this publication. The author would like to thank Andre Metzger for help with measurements, photographs, and floppy disks. The author is also grateful to the UCSD Center for Wireless Communications, the UC Discovery Grant program and the MARRS MURI program of the US Army Research Office for funding.

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Chapter 9
Conclusion

1. Dissertation Summary

The dissertation begins with an outline of the unique challenges and metrics unique to digital transmitter designs. A novel metric is introduced to compare efficiencies from switching amplifiers driven by different encoding algorithms. A design of an all-digital transmitter, targeting the IEEE 802.15.4 wireless communication standard, is presented that achieves 10.8 dBm of output power at 42% PA drain efficiency, with a bits-to-RF system efficiency of 22%. The design is capable of integration into digital CMOS processes, and requires few off-chip components. The designed uses a novel encoding algorithm that requires few digital resources, lowering digital logic power consumption.

Optimizations of delta-sigma modulators, designed to drive switching PAs, are presented along with digital logic structures to implement these modulators. Techniques to optimize the NTF of delta-sigma systems to achieve low interference are presented. The delta-sigma system achieves 30% in-band power, corresponding with a VMCD amplifier achieving 31% drain efficiency amplifying a QPSK signal similar to IS-95, while meeting ACPR specifications.

Nonlinearities in VMCD switching amplifiers, causing broadband noise generation, are analyzed and simulated. Novel test signals are introduced that enable characterization of asymmetrical slew rate nonlinearities in switching amplifiers, even with narrowband resonant output matching. Fixed time-step simulation techniques are

introduced that capture nonlinearities associated with aperiodic switching events that are not modeled correctly by many simulation algorithms. The analysis of the nonlinearities is validated with a VMCD amplifier redesign that reduces broadband noise by 15 dB.

A variation on PWM is developed that has significant advantages over delta-sigma when driving switching RF power amplifiers. Problems associated with PWM switching events occurring unaligned to clock transitions are analyzed in relation to both simulation and signal generation. A pulse-to-spectrum frequency domain simulation technique is introduced that overcomes some of the noise floor issues that occur when using a sampled time simulation of PWM systems. A novel circuit based on a DLL is developed that generates PWM with a high degree of time accuracy without using a frequency reference higher than the RF carrier. Amplifier measurements show that this PWM driven amplifier achieves a drain efficiency of 49% with compliant ACPR, compared with a delta-sigma driven system that achieves a maximum drain efficiency of 37% with ACPR compliance. Simulations show that BPPWM does not cause supply memory nonlinearities to generate broadband noise.

A new digital driven polar amplifier topology is introduced along with new drive algorithms. A hybrid ET/EER digital drive algorithm is developed that helps the polar amplifier accurately reproduce signals with a high peak-to-minimum ratio. General studies on polar transmitter time misalignment affecting broadband noise generation are performed. Simulations highlight interesting time-domain properties of the broadband noise generated. A pre-distortion technique that reduces the power of the broadband noise generated is introduced and simulated.

A novel all-digital frequency synthesis algorithm is introduced. The corresponding all-digital circuit can increase the level of integration in transmitter systems since it can be implemented entirely in digital logic.

2. Conclusion and Future Work

The current state of the art in digital transmitter designs is ready to meet the specifications of WPAN-class wireless standards. The cost and integration benefits of digital transmitter designs fit well with the goals of WPAN technology: ubiquitous small inexpensive energy efficiency transmitters. Digital transmitter design technology can bring analog WPAN designs, now implemented in prior generations of higher voltage CMOS, to the extreme levels of integration possible with sub 100 nanometer class CMOS.

Full duplex communication standards have broadband spurious noise specifications impossible to meet with the current state of digital transmitters with reasonable filters. This work has developed switching transmitters with a quieter RX band, achieved by both reducing nonlinearities causing self-mixing, and creating encoding algorithms with noise transfer functions that can tolerate self-mixing. Delta-sigma modulation is not a future direction as it creates broadband quantization noise very intolerant of amplifier nonlinearities. Instead, addressing broadband noise in the encoding aspects of a digital transmitter design as well as amplification could lead to less stringent filtering requirements.

Band-pass pulse width modulation is an attractive drive signal for digital transmitters. BPPWM signals have efficiency and noise benefits that for many designs

can offset the added complexity of high time-resolution. Implementing the proposed circuits to generate BPPWM drive signals is an important next step.

Digital polar amplifiers have promise to amplify large dynamic range communication signals with high efficiency. A solid groundwork for the signal generation of these systems was laid. Test amplifiers are currently being fabricated, and testing an actual amplifier under these drive signals is an immanent next step.

The polar amplifier noise analysis performed, and the resulting noise-reducing pre-distortion technique, are valid for all polar transmitters. The pre-distortion technique can help transition polar designs to full duplex standards with higher peak-to-minimum power ratios. The process of setting up the extensive amount of lab equipment to perform the pre-distortion on a polar amplifier is currently underway.

Obstacles still exist for specification compliant handset-class digital transmitters. Ideally, work on these obstacles can be motivated by the benefits shown by WPAN-class digital transmitter designs.