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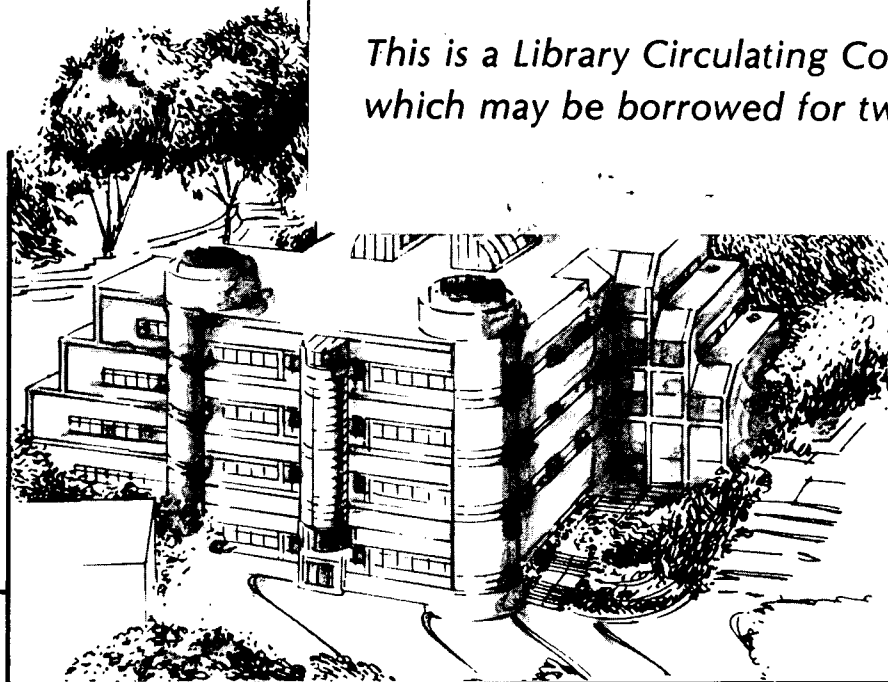
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**Suppression of Defect Propagation in Heteroepitaxial
Structures by Strained Layer Superlattices**

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SUPPRESSION OF DEFECT PROPAGATION IN HETEROEPITAXIAL STRUCTURES BY STRAINED LAYER SUPERLATTICES

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Abstract

Defects present in GaAs on Si(211) heteroepitaxial layers grown by MBE have been analyzed in detail by TEM. Efficient reduction of dislocation propagation by strained layer superlattices was found. The mechanisms of defect reduction were suggested based on Burgers vector analysis. It was shown that additional threading dislocations can glide into the epilayer during cooling process and that misfit dislocations at the interface can be forced to dissociate on a 111 plane inclined to the interface leaving one partial dislocation at the interface and forming extended stacking faults.

1. INTRODUCTION

The heteroepitaxy of GaAs thin films on Si substrates (GaAs on Si) has attracted considerable interest in recent years [1-4], mainly for two reasons: (1) the possibility of fabricating existing GaAs-based devices on large, low cost Si substrates, and (2) the exciting potential of monolithic integration of GaAs-based electronic and optoelectronic devices with Si integrated circuits. However, the density of structural defects such as dislocations, stacking faults, and microtwins in GaAs on Si heteroepitaxy is still too high for many applications. These defects are formed because of the different lattice constants and thermal expansion coefficients in the substrate and epilayers. As a result of these mismatches, defects in the epilayer are formed initially during the growth process or during postgrowth cooling by propagation into the epilayer. Even for GaAs grown on Si(001), where a large fraction of dislocations formed at the interface have Burgers vector's in the interfacial plane [5], dislocation densities in the range of 10^6 to 10^7 cm⁻² are usually found. This is over three orders of magnitude greater than the dislocation density for GaAs films grown directly on GaAs substrates. Another difficulty arising in the growth of a polar on a nonpolar crystal is the presence of antiphase disorder and the formation of a very large intrinsic electric charge, which can act as a sheet of very high doping. One solution to these problems may be the use of (211)Si substrates to grow GaAs [4]. However, many misfit dislocations in the GaAs grown on (211)Si have Burgers vectors inclined to the interface [6,7], making them susceptible to dissociations and gliding into the GaAs layer. In order to obtain device-quality epitaxial GaAs material, a reliable method for suppressing defect propagation in the epilayer is necessary. One promising method is to use strained layer superlattices (SLSL's).

In this paper, we compare, by transmission-electron microscopy (TEM), the effectiveness of SLSL's (InGaAs/GaAs) in controlling dislocation propagation into the GaAs epilayer grown on Si(2 $\bar{1}1$) substrates. The influence of furnace annealing and rapid thermal annealing (RTA) was investigated as well.

2. EXPERIMENTAL

GaAs crystal growth on a Si(2 $\bar{1}1$) substrate was conducted in a molecular-beam epitaxy (MBE) system (Varian-360). A two step cleaning procedure was applied for the Si wafers. The first step involved a procedure described by Ishizaka [8] where four major steps were involved: degreasing, acidic oxidation, alkaline oxidation, and boiling in HCl:H₂O:H₂O₂ (3:1:1) for 5-7 min followed by DI water rinse. After this, the Si wafers were mounted on a molybdenum block with In, and the Si wafer was dried with filtered nitrogen. The second step involved Ga reduction in the MBE chamber. The Si sample temperature was raised to 800°C, and a beam of Ga was simultaneously impinged on the sample surface. This "Ga-reduction" procedure lasted for ~10 min. Then the Ga furnace shutter was closed, but the sample temperature was still kept at 800°C for one more minute to eliminate the excess Ga on the surface. After this procedure the surface was considered oxide free, and the specific layers were grown.

Four different kinds of structures were investigated: (a) sample "23", with 50 layers of GaAs/InGaAs (5 nm thick each) grown directly on the Si surface followed by an 0.5- μ m-thick GaAs epilayer, (b) sample "60", with a 50-nm-thick GaAs buffer layer followed by 10 layers of GaAs/InGaAs (5 nm thick each) and a 1- μ m-thick GaAs epilayer, (c) sample "72", with three sets of SLSL's, and (d) sample "62", with only one InGaAs layer (30 nm thick), followed by 1 μ m of GaAs. Detailed informations about these structures were described previously [6]. Those structures were grown to investigate the influence of the presence of a GaAs buffer layer and the thickness of the SLSL sequence on defect density. The influence of annealing (furnace and RTA) was investigated for sample 60 and compared with similar annealing for GaAs grown on (001)Si.

All structures shown were investigated by using a JEOL JEM 200CX electron microscope with a point-to-point resolution of a 2.4 Å and by the Atomic Resolution Microscope (ARM) at Berkeley with its 1.7 Å point-to-point resolution. All samples were investigated in cross sections prepared along Si[111] and Si[011] parallel to the electron beam.

3. RESULTS

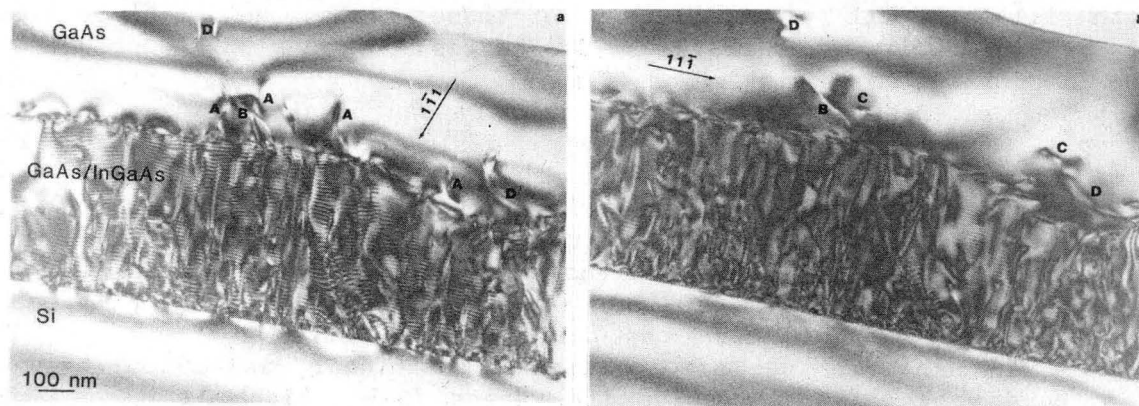
Before discussion the experimental results of the dislocation study, it is useful to consider the possible geometries of misfit and threading dislocations in the GaAs/Si heterostructures. Complete dislocations have a translation vector of the crystal lattice as Burgers vector (b). In the diamond structure the shortest translation vector is of the type $\frac{a}{2} \langle 011 \rangle$. The dislocations found in GaAs/Si heteroepitaxial layers can be distinguished with respect to their Burgers vectors in the following way:
 GaAs/Si(001): Type I -- $\frac{a}{2} [\bar{1}10]$ and $\frac{a}{2} [110]$; type II -- $\frac{a}{2} [011]$, $\frac{a}{2} [\bar{1}01]$, $\frac{a}{2} [0\bar{1}1]$, and $\frac{a}{2} [101]$; GaAs/Si (2 $\bar{1}1$): type I -- $\frac{a}{2} [011]$; type II -- $\frac{a}{2} [110]$ and $\frac{a}{2} [\bar{1}01]$; type III -- $\frac{a}{2} [101]$ and $\frac{a}{2} [0\bar{1}1]$; type IV -- $\frac{a}{2} [\bar{1}10]$. With this classification type I dislocations have Burgers vectors

in the hetero-interface. Type II dislocations have Burgers vectors inclined to the heterointerface. For GaAs/Si (001) these dislocations can glide on $\{111\}$ planes, which are inclined 55° to the heterointerface. Type II dislocation in GaAs/Si ($2\bar{1}1$) can glide on the $(1\bar{1}1)$ plane, which is inclined only 19.5° to the interface. Type III dislocations in GaAs/Si ($2\bar{1}1$) can glide on the $(11\bar{1})$ plane, which is perpendicular to the $(2\bar{1}1)$ interface plane. Type III as well as type IV dislocations can glide on (111) or $(\bar{1}11)$, both of which are 61.9° from $(2\bar{1}1)$.

3.1. As grown epilayers

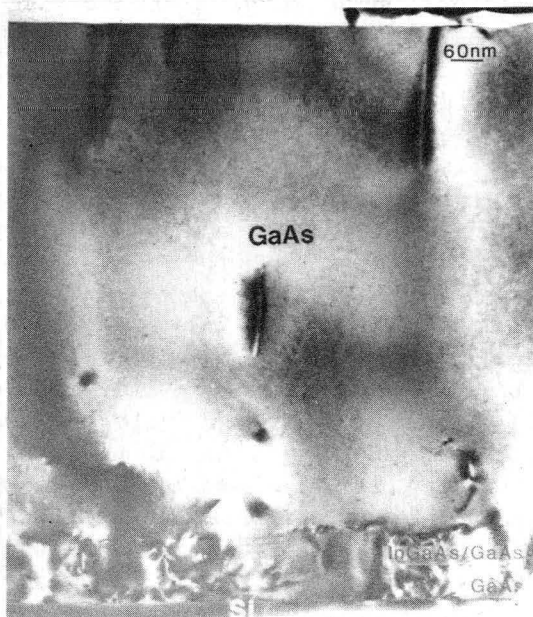
A cross-section TEM study (Fig. 1) of sample "23" shows that the use of SLSL's can reduce the dislocation density by about two orders of magnitude. A very important feature of the blocking of dislocation propagation in these samples is that it occurs almost entirely at the uppermost interface between the strained layers and the final GaAs layer. Therefore, the reduction of dislocation density is only weakly dependent on the thickness of whole set of strained-layer superlattices. Many stacking faults occur through out SLSL's (visible as straight lines in Fig. 1). These stacking faults are formed primarily on $(11\bar{1})$ planes perpendicular to the interface. Many dislocations interact with each other in the epilayer. Imaging with two-beam approximation and using $g \cdot b = 0$ (invisibility conditions) for particular dislocations allowed one to determine Burgers vector of the threading dislocations. Dislocations A in Fig. 1 vertical to the interface are type III. Dislocations C parallel to the interface are type II. Dislocations B and D are always visible for all low-index diffraction vectors in the (011) plane. In this sample areas with very low dislocation densities have been found. However, on the average the dislocation density in the area directly above the SLSL's was in the 10^8 cm^{-2} range. Close to the surface the dislocation density was around $5 \times 10^7 \text{ cm}^{-2}$.

This study shows that the suppression of defect propagation depends only weakly on the combined thickness of all the SLSL's. Samples "60" are prepared with only 10 layers of SLSL's grown on the 5-nm-thick buffer layer. These samples, with a buffer layer grown at 505°C , turned out to have large dislocation-free areas in the GaAs, and the average dislocation



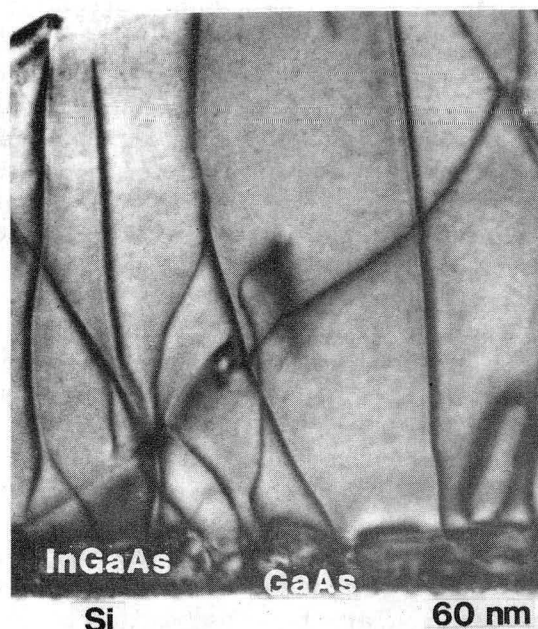
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FIGURE 1. TEM cross-section micrograph of sample "23". Note that the large number of stacking faults on the $(11\bar{1})$ plane was suppressed by the SLSL's of InGaAs/GaAs and a low defect density was observed in the GaAs epi-layers; a and b show that disappearance of particular dislocations for different diffraction conditions (e.g., $g = [11\bar{1}]$ and $[\bar{1}11]$).



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FIGURE 2. TEM micrograph of sample "60". Note the SLSL grown on the GaAs buffer layer. Many areas with low dislocation densities were found.



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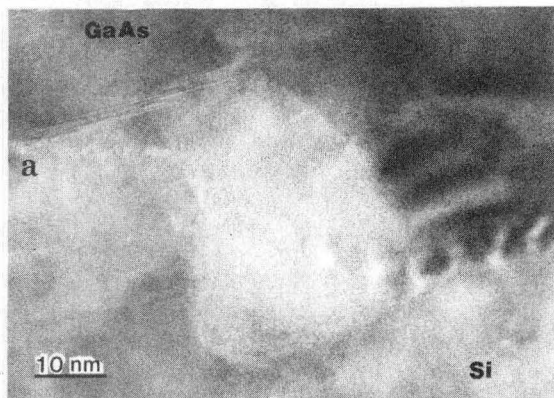
FIGURE 4. Dislocation bending by only one 30-nm-thick layer of InGaAs (sample "62").

density was in the range of 10^7 cm^{-2} at 150 nm from the Si interface (Fig. 2). Similar kinds of threading dislocations were observed in the GaAs epilayer above the SLSL's: arc dislocations (type IV) resulting from the interaction between these dislocations in the SLSL's, dislocations inclined to the interface with SLSL's of (type II), and dislocations that were always visible for all three $\langle 220 \rangle$ directions in the (111) plane. Stacking faults and microtwins were formed in the buffer layer on both (11 $\bar{1}$) and ($1\bar{1}1$) planes. Study of these samples shows that formation of stacking faults and microtwins is often associated with the presence of some impurities on the interface (Fig. 3).

It was interesting to observe that only one strained layer of InGaAs (sample 62) was enough to bend many dislocations, but many of these dislocations still propagated into the GaAs. Bending of dislocations again occurred on the upper interface with GaAs (Fig. 4).

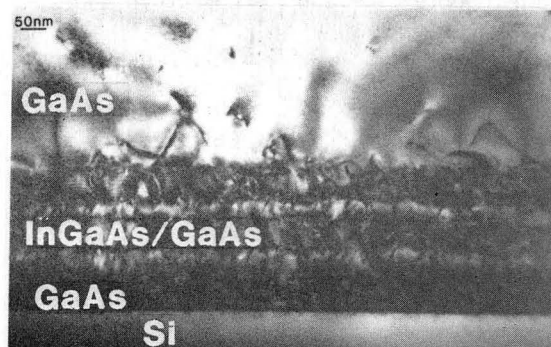
Because of the observation that the upper interface of SLSL's is most efficient in bending of dislocations, three sets of SLSL's were grown on the Si separated by 50 nm of the GaAs buffer layer (sample "72"). Each set was expected to reduce the dislocation density on the upper GaAs layer. Indeed, each set of SLSL caused additional dislocation bending, and there were many dislocation free areas (3-5 μm long) (Fig. 5). But there were also areas where additional dislocations were formed at the lower interface between the buffer layer and the SLSL. Therefore, in some areas the dislocation density was slightly higher; however, an average dislocation density in this sample was in the $\sim 2 \times 10^7 \text{ cm}^{-2}$ range.

In all samples investigated, the interface with Si was contaminated less by impurities than described in earlier reports of samples grown on Si(001) [9]. These results show that cleaning by "Ga reduction" is



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FIGURE 3. Impurities present on the Si surface cause additional defects in the form of protrusions. Such areas are an additional source for the formation of stacking faults.



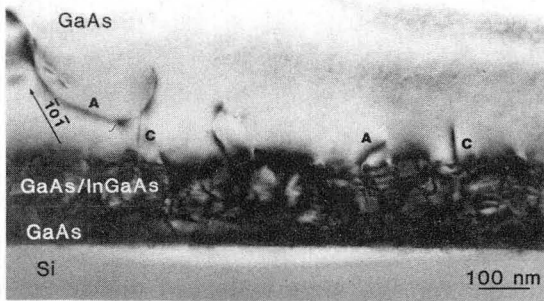
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FIGURE 5. TEM micrograph of sample "72". Note bending of dislocations by three sets of SLSL's.

clearly an improvement over earlier procedures [8]. However, wherever Si surface contamination was present, origination of stacking faults and microtwins was observed. Burgers circuits for the perfect misfit dislocations observed on (011) projections show that the Burgers vector lies in the slightly inclined (111) plane. For the interfaces viewed in [111] projection, two types of Burgers vectors were observed: lying on the (211) interface plane and lying on the (110) plane.

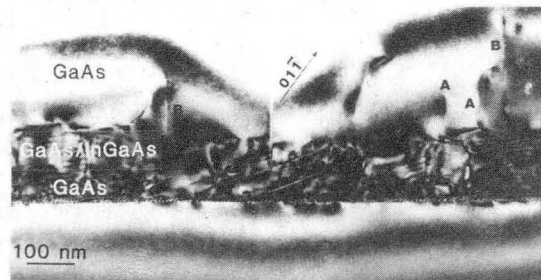
3.2. Annealed epilayers

Furnace annealing of the samples "60" at 800°C for 10 min change the defect rearrangement very slightly, (Fig. 6). The dislocation density remains in the same range as for "as-grown samples." Arc and vertical dislocations (type IV) (A and C in Fig. 6, respectively), and bowed dislocations (type II) were observed in the GaAs above the uppermost interface with SLSL. As in "as-grown samples," there were many dislocations for which invisibility conditions were not found (for low index planes). Some improvement of GaAs quality was observed (Fig. 7) when the samples 60 were annealed by RTA for 10 seconds in a commercial Heatpulse furnace by the capless close-proximity method. However, as in all previously investigated samples, cracking of the GaAs epilayers was observed in these samples. The main change in RTA-annealed samples was the disappearance of the stacking faults on the (111) planes perpendicular to the (211) interface. The stacking faults on the (111) planes inclined to the interface were still present (Fig. 7). The TEM study of GaAs grown on 4°-off (001)Si annealed under the same conditions did not reveal stacking faults formed at the interface [10]. Type II and IV threading dislocations were observed after RTA. As in all previously observed cases, there were dislocations for which invisibility conditions were not found.



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FIGURE 6. TEM micrograph of sample "60" after furnace annealing.



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FIGURE 7. Sample "60" after RTA. Note the stacking faults on the (111) plane and cracking of the GaAs.

4. DISCUSSION

The formation of threading dislocations and stacking faults in GaAs/Si heteroepitaxial growth can be caused by defect formation during growth and/or during cooling after the growth. During growth, the formation of misfit dislocations and their subsequent glide to the hetero-interface can result in threading dislocations in the epitaxial layer, as suggested by Mathews [11]. In GaAs/Si ($2\bar{1}1$), these dislocations are type I or II. At the end of the growth process, the epitaxial layer has very little residual strain if the misfit dislocation density at the heterointerface corresponds to the lattice mismatch of GaAs ($a = 5.675 \text{ \AA}$ at 600°C) and Si ($a = 5.439 \text{ \AA}$ at 600°C). However, the difference in thermal expansion coefficient ($\alpha_{\text{GaAs}} = 6.8 \cdot 10^{-6}/^\circ\text{C}$, $\alpha_{\text{Si}} = 2.6 \cdot 10^{-6}/^\circ\text{C}$) will produce a new strain during cooling from the growth temperature. In GaAs/Si, this strain is of the opposite sign to the lattice mismatch strain, and photoluminescence measurements of GaAs/Si structures indeed confirm the presence of tensile strain after growth [12]. The tensile strain observed experimentally is considerably lower than the expected value of $2.4 \cdot 10^{-3}$, indicating strain relief by plastic flow. Cooling from 600°C to 400°C is sufficient to generate a biaxial tensile stress far above the experimentally determined critical resolved shear stress of 15 MPa at 400°C [13], which can result in the glide of additional threading dislocations of various types into the epilayer. In addition, misfit dislocations at the interface can be forced to glide back into the epilayer or to dissociate on a $\{111\}$ plane inclined to the interface, leaving one partial dislocation at the interface and forming an extended stacking fault. The formation of extended stacking faults by glide processes was first found in plastically deformed semiconductors cooled under high stress [14,15].

Type I misfit dislocations with an edge component cannot move into the epilayer by glide, as their glide plane is the interface plane. Only screw dislocations at the interface with a type I Burgers vector can either glide as complete dislocations or dissociated into two partial dislocations, leaving a vertical stacking fault in GaAs/Si ($2\bar{1}1$), as frequently observed (Fig. 1). A second source for vertical stacking faults can be dissociated type III dislocations. Type II dislocations have a glide plane inclined to the interface, allowing for each dislocation gliding as a complete dislocation or dissociated into two partial dislocations, forming a stacking fault. In GaAs (001), type II dislocations can dissociate in this way, e.g., a dislocation along $[\bar{1}10]$ with a Burgers vector $\frac{a}{2} [011] \rightarrow \frac{a}{6} [1\bar{2}\bar{1}] + \frac{a}{6} [112]$, leaving a partial dislocation

with $\underline{b} = \frac{a}{6} [1\bar{2}1]$ at the heterointerface, which still relieves all of the misfit strain of the total dislocation. In GaAs/Si ($2\bar{1}1$), the dissociation reaction is for type II dislocations along $[011]$, with $\underline{b} = \frac{a}{2} [110] \rightarrow \frac{a}{6} [21\bar{1}] + \frac{a}{6} [121]$, in which case the partial dislocation with $\underline{b} = \frac{a}{6} [121]$ still relieves all the misfit compared to the complete dislocation.

Thermal annealing at temperatures above the original growth temperature reverses the sign of the stress due to the difference in thermal expansion coefficient, providing a driving force in the opposite direction as compared to the original cooling process. This stress may force the reversal of the glide processes discussed above, including the removal of stacking faults by recombination of the partial dislocations. The removal of stacking faults in GaAs/Si (001) and ($2\bar{1}1$) and the disappearance of type III dislocations in GaAs/Si ($2\bar{1}1$) seem indeed to be the most clearly observed annealing effects. It is not surprising that furnace annealing is less efficient in the reduction of threading defects, compared to rapid thermal annealing. The subsequent slow cooling period after furnace annealing might reverse the beneficial effects of the high-temperature treatment, whereas the rapid quenching after RTA more likely preserves those effects.

Bending of dislocations at a strained interface provides an opportunity for dislocations to react with each other, which can result in annihilation of the threading parts or in the formation of immobile stair-rod dislocations. Thus, the total density of threading dislocations can be reduced substantially by SLSL's.

Early studies clearly showed bending of the threading dislocations at each interface of a SLSL [11]. Our work clearly shows that in superlattices consisting of periods of 10 nm or less, the dislocation bending effect and reduction of dislocation densities by several orders of magnitude is confined to the first and last interface of the SLSL (see Figs. 1-2, 4-7). This result can be easily explained by the fact that the dislocation strain field is a far-ranging $1/r$ field. If the thickness of the individual strained layer is too small, the total energy of a dislocation moving through a SLSL is only slightly modulated, depending on its position within the SLSL (in an area of positive or negative strain). Only a dislocation entering or leaving a SLSL or a dislocation moving through a SLSL consisting of thick layers experiences a strong change in total energy in each layer and thus a force bending it into the interface. However, if the individual layers of the SLSL exceed the critical thickness for strained structures, new misfit dislocations will be formed. Therefore, a careful optimization of the growth parameters of SLSL's is necessary.

5. CONCLUSION

This study shows that the density of threading defects in lattice mismatched heteroepitaxy can be substantially influenced by post-growth annealing treatments and by the insertion of strained layer superlattices. A detailed analysis of the character of the observed dislocations and stacking faults has allowed us to suggest mechanisms for the observed density reduction. It is obvious that the current growth technology is not optimum. We have shown that it is possible to grow low-defect density lattice mismatched structures with a controlled network of misfit dislocations at the heterointerface by removing the misfit

strain. A method for reliably eliminating threading dislocations has not been found yet. Our studies show occasional $\sim 1\text{-}\mu\text{m}^2$ -wide areas of GaAs/Si structures free of all threading defects. It can be expected that careful optimization of the design of strained layer superlattices and of annealing sequences during and after growth will help to reach the final goal of device-quality GaAs/Si and other mismatched structures.

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