Steep On/Off Transistors for Future Low Power Electronics

By

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Abstract

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In the last couple decades, the phenomenal growth of mobile electronics is fueling the demand for multi-functional, high performance and ultra-low power integrated circuits. Reduction in Vdd to achieve orders of magnitude reduction of energy consumption is crucial if the promise of many more decades of growth of electronics usage is to be realized. For MOSFETs, Vdd reduction can only be achieved at the expense of speed loss and/or off-state leakage increase because the subthreshold slope is fundamentally limited to 60mV/decade. New transistors with sub-60mV/dec swing allowing Vdd scaling to 0.3V and below are therefore highly desirable.

In this research, two approaches to achieve transistors with sub-60mV/dec swing are explored. Feedback FET (FBFET) uses positive feedback to induce an abrupt change in current with a small change in the gate voltage. Experimental results show FBFET can achieve less than 2mV/dec swing, with Ion/Ioff ratio larger than six-orders-of-magnitude. Simulation is used to illustrate the operating principle, and to evaluate the potential of FBFET. Another approach is to integrate negative capacitance element onto the gate stack of MOSFETs. The negative capacitance does not change the transport physics, but rather seeks to "amplify" the gate voltage electrostatically to achieve less than 60mV/dec swing. Design considerations and optimizations of Negative Capacitance FET (NCFET) are explored using simulations. Simulation shows the possibility of achieving hysteresis free, sub-30mV/dec operation of NCFET based on an UTBSOI design. The experimental NCFET result of epitaxial ferroelectric thin film on SOI substrate is presented.

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Chapter 1: Introduction

1.1 Introduction

Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) has been the workhorse for the semiconductor industry in the last two decades. For each new technology nodes, technology boosters such as stress memorization technology (SMT) [1.1], high-k metal gate (HKMG) [1.2], Ultra-thin-body (UTB) [1.3] and FinFET structures [1.4] have enabled the scaling of transistors density, performance, and/or power consumption.
With the increasing importance of mobile devices, scaling of power consumption is arguably the most important factor. However, power consumption, which is proportional to the square of supply voltage (V_{DD}), is the least scaled factor among the three (density/performance/power consumption) in recent technology nodes.

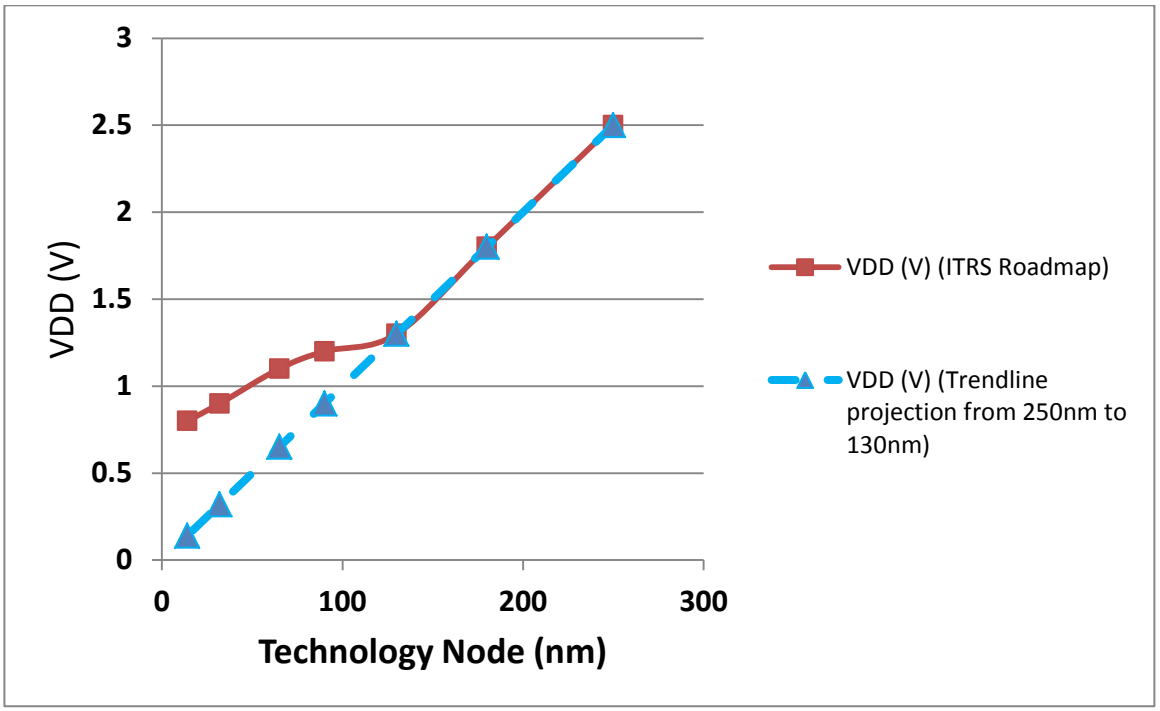

Figure 1.1: Historical trend of V_{DD} scaling VS technology node. [1.5]

Had V_{DD} scaling been following the trend from 250nm to 130nm, 14nm node would have been operating at 0.14 V_{DD} instead of ~0.8 V_{DD}. Since dynamic power consumption is proportional to the square of V_{DD}, circuits are consuming 32X [(0.8/0.14)^2] more power than it should have if the V_{DD} scaling had been following physical dimension scaling trend.

In the next section, we will look at why V_{DD} scaling has been stalled.

1.2 V_{DD} scaling limitation

The classical constant field scaling theory suggests that when dimensions of transistors are scaled by a factor of 1/α, the V_{DD} can also be scaled by 1/α such that the electric field remains constant [1.6]. However, when V_{DD} is close to 1V and below, the threshold voltage (V_T) becomes a significant portion of the V_{DD}, and V_T does not scale linearly with transistor dimensions. This is the main reason why V_{DD} scaling has been slowing down in the last few technology generations.

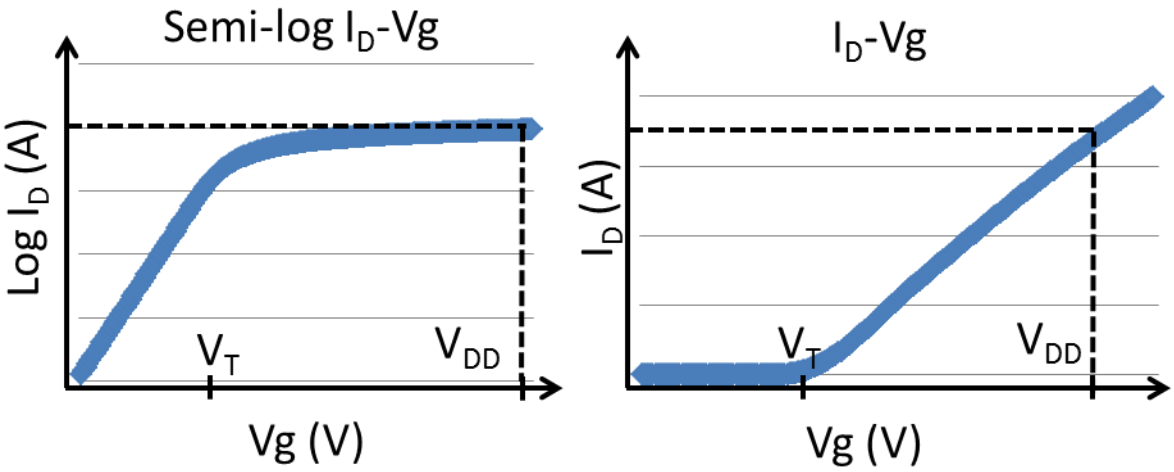

Figure 1.2: Log Id-Vg and Id-Vg of MOSFET.

1.3 Threshold Voltage of MOSFET

Before deep diving into addressing the threshold voltage problem, let's understand what is V_T and why V_T does not scale well in MOSFETs.

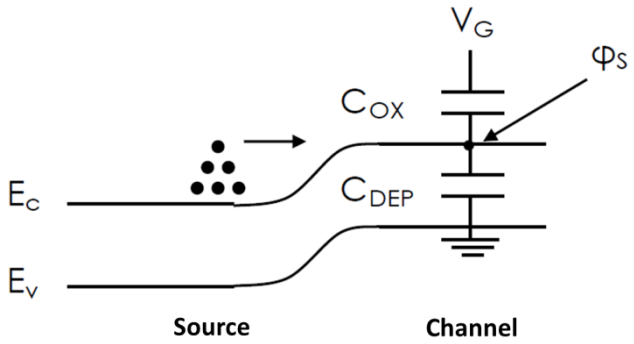

Fig 1.3: Energy Band Diagram from source to channel.

For MOSFETs, the carriers in the source are thermally injected over the channel barrier (gate modulated) and collected by the drain. And the distribution of source carrier (n_s) as a function of

energy (E) can be described by Boltzmann distribution, where k is the Boltzmann constant and T is the temperature.

$$n_s(E) \propto e^{-qE/kT} \quad (1.1)$$

To find the total drain current (I_D), we can integrate the n_s above the channel potential (φs), and I_D before reaching V_T can be given by:

$$Id(\varphi s) \propto e^{q\varphi s/kT} \text{ or } I_D(V_G) \propto e^{qVg/\eta kT} \quad (1.2)$$

Where η is the body factor, derived from the capacitive divider between the gate capacitance (C_{OX}) and the depletion capacitance (C_{DEP}):

$$\eta = 1 + C_{DEP}/C_{OX} \quad (1.3)$$

The change in current in the subthreshold region w.r.t. V_G is called the subthreshold swing (SS), which is given by

$$SS(mV/decade) = \eta * 60\ mV*T/300K \quad (1.4)$$

For MOSFETs, even with and ideal factor of η =1, the best SS it can achieve is 60mV/decade at room temperature, meaning for an I_{ON}/I_{OFF} ratio of 6 orders, the V_T must be at least 300mV. **It is the fundamental limit for MOSFET technology and it has to be addressed in order to enable future ultra-low power applications [1.7].**

1.4 References:

[1.1] Auth, Chris, et al. "45nm high-k+ metal gate strain-enhanced transistors." *VLSI Technology, 2008 Symposium on*. IEEE, 2008.

[1.2] Packan, Paul, et al. "High performance Hi-K+ metal gate strain enhanced transistors on (110) silicon." *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*. IEEE, 2008.

[1.3] Choi, Yang-Kyu, et al. "Ultra-thin body SOI MOSFET for deep-sub-tenth micron era." *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*. IEEE, 1999.

[1.4] Huang, Xuejue, et al. "Sub 50-nm FinFET: PMOS." *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*. IEEE, 1999.

[1.5] ITRS Roadmap Executive Summary [online] Available:

http://www.itrs.net/Links/2007ITRS/ExecSum2007.pdf

[1.6] Dennard, Robert H., et al. "Design of ion-implanted MOSFET's with very small physical dimensions." *Solid-State Circuits, IEEE Journal of* 9.5 (1974): 256-268.

[1.7] Hu, Chenming. "3D FinFET and other sub-22nm transistors." *Physical and Failure Analysis of Integrated Circuits (IPFA), 2012 19th IEEE International Symposium on the*. IEEE, 2012.

Chapter 2: Feedback FET (FBFET)

2.1 Introduction

As discussed in the last chapter, one of the fundamental limits of MOSFET is its inability to turn on faster than 60mV/decade, which is the bottleneck in the scaling of V_{DD} for future ultra-low power applications.

One way to circumvent this problem is to use positive feedback mechanism. Positive feedback is a well-known phenomenon and has been used widely in different engineering disciplines. One of the common applications of positive feedback in electronic circuits is operational amplifiers for signal amplifications. With positive feedback, a small perturbation of the input can induce a large change in the output signal. Therefore, if a "MOSFET" has a build-in positive feedback amplifier, a small change in V_G can induce a large change in the drive current, and therefore, less than 60mV/decade SS can be achieved.

2.2 Positive Feedback and hysteresis

Before we go to the actual device, let's first look at a simple feedback loop.

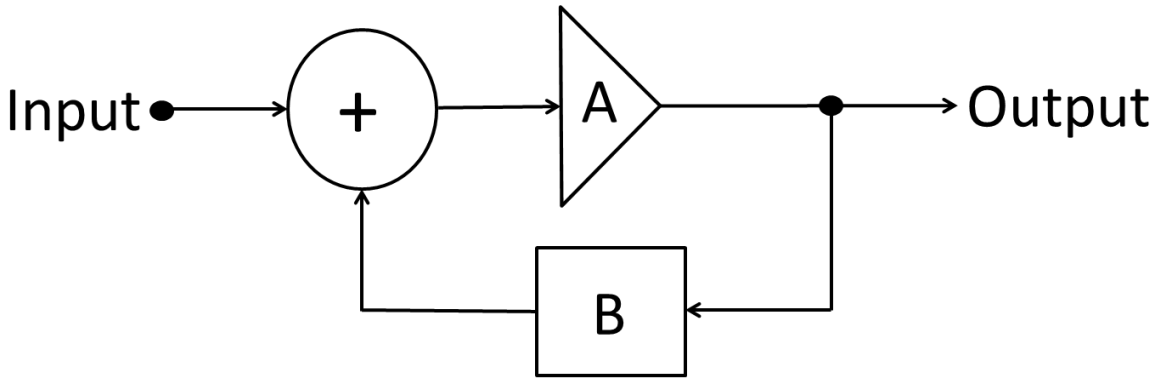

Figure 2.1: A simple feedback loop. A is the open-loop gain, B is the feedback factor, and the product of A and B is the loop gain.

The close-loop gain (G) of the system can be written as

$$\text{Output/Input} = G = A/(1-AB) \qquad (2.1)$$

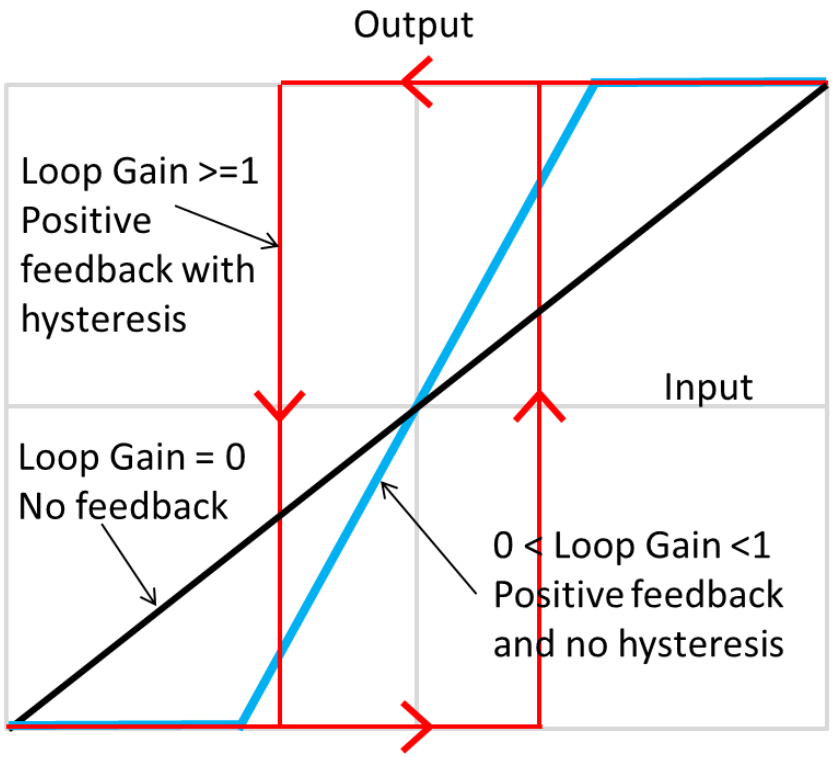

Figure 2.2: Illustration of the transfer characteristics in three cases: (a) No feedback: black line, (b) positive feedback without hysteresis: blue line, and (c) positive feedback with hysteresis: red line.

Where B is zero, i.e. when there is no feedback or the feedback loop is open, the output equals the input times the open-loop gain A. When loop gain is larger than 0 and smaller than 1, the input will be amplified, and the close-loop gain G will be greater than A. When the loop gain is equal to or greater than 1, G becomes infinite, and the system will be become unstable and hysteresis will be observed. We will revisit this important concept again when designing a hysteresis-free NCFET in chapter 3.

In the next session, we will discuss the device structure and how we can incorporate a positive feedback system into a single device.

2.3 Device structure and working principle

The structure of a FBFET is very similar to a MOSFET, except that the source and drain are doped with opposite dopants, and the silicon underneath the nitride spacers are undoped. Figure 1 shows the typical structure of a FBFET fabricated on SOI wafer using FinFET technology.

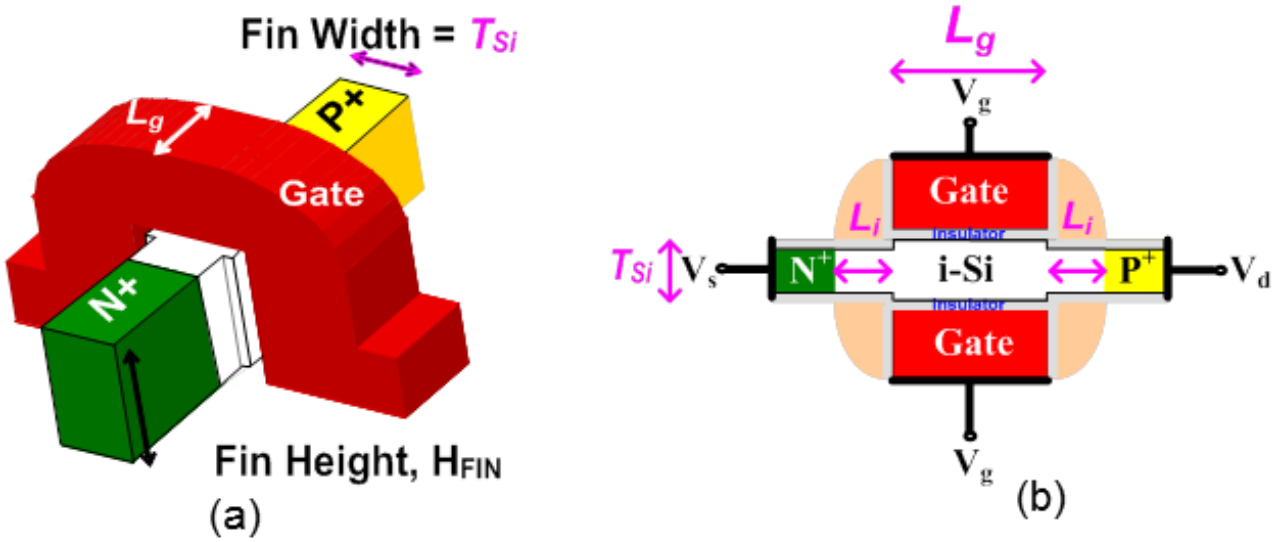

Figure 2.3: Schematic illustrations of the FB-FET structure. (a) Isometric view (gate-sidewall spacers not shown, for clarity), and (b) 2-D cross-sectional view.

After fabrication, the device needs to be conditioned/programmed first [4]. With the appropriate programming conditions, electrons are trapped in the nitride spacer under the N+ source and holes are trapped in the nitride spacer near the P+ drain. These trapped charges create electron and hole barriers which is essential for the feedback mechanism.

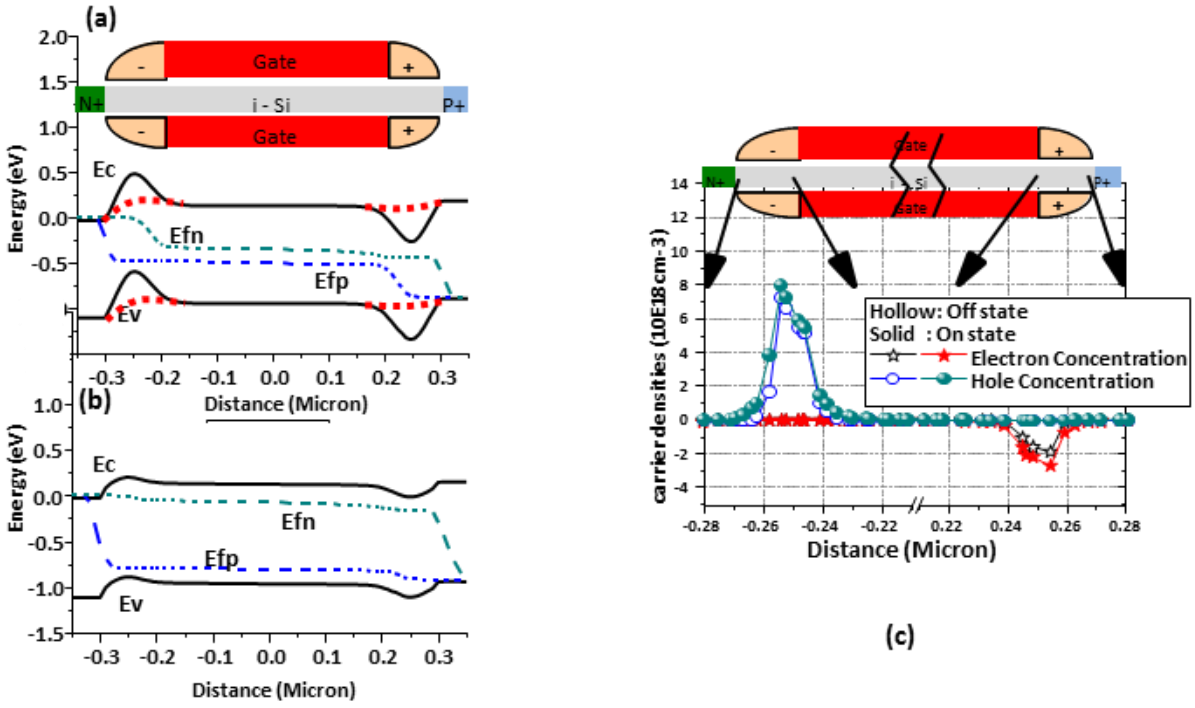

Figure 2.4: Simulated energy band diagrams in (a) before conditioning (dash red line) and the off state (solid line) (b) on state. (c) Carrier densities along the center of the fin. Vds=0.8V.

Figure 2.4(a) shows the band diagrams before and after conditioning. Before conditioning (the dash red line), there is no barriers (besides the build-in potential barrier of the PN junction) for electron and holes to the stop the current flow. The device behaves like a PIN gated diode. Once the device is conditioned, the negative charges in the spacer near the N+ source will induce a potential barrier preventing the injection of electrons into the channel. Likewise, the positive charges near the P+ terminal create potential barrier to block holes from injecting to the channel. Therefore, the current will be very low even a forward bias is applied across the Source and Drain terminals and this it the OFF state.

Figure 2.4(b) illustates the ON state of the device. In this state, there are a lot of electrons and holes injecting from both the N+ and P+ terminals into the channel because the barrier for holes/electrons are very small. At the same time, the electron (hole) barrier are filled with holes (electrons), so both barrier heights are much reduced compared with the OFF state. Figure 2.4(c) shows the carrier densities are much higheer in both the ON states under the spacer region.

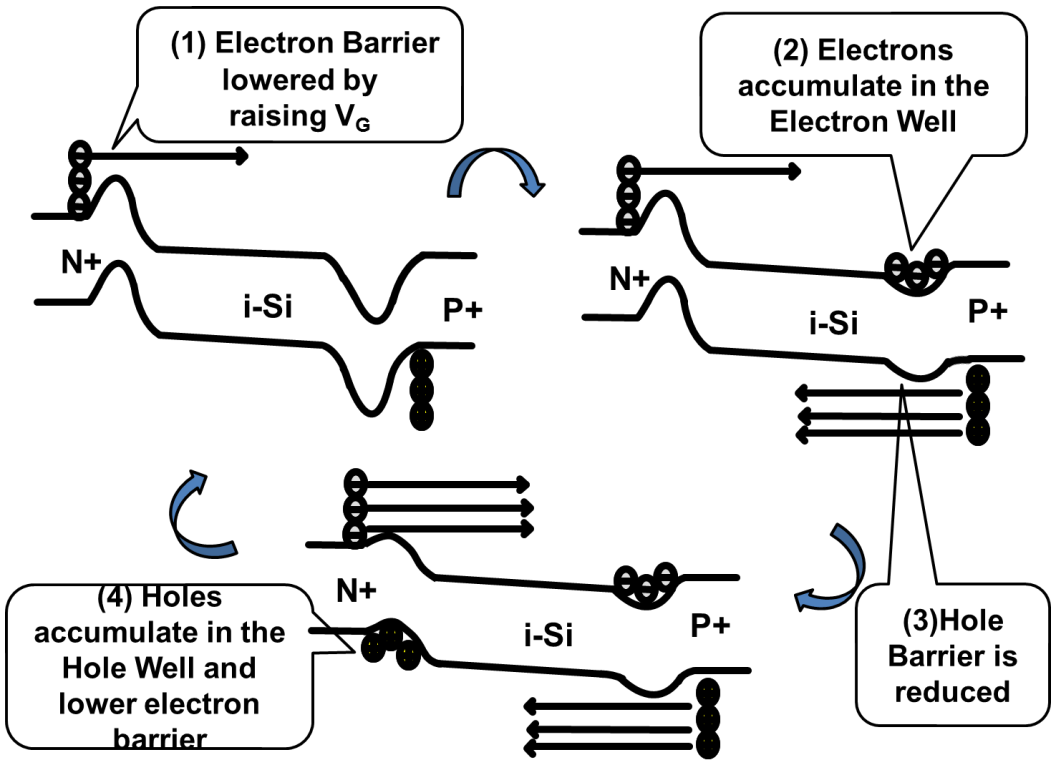

Figure 2.5: Illustration of the feedback mechanism.

Figure 2.5 illustrate the feedback mechanism triggers the device from the OFF to ON state. In the OFF state, both barriers for electrons and holes are large, so very small can current flow. A small change of the gate voltage can lower the electron barrier, and causes a small increase in electron current flowing into the channel from the N+ source. Then these electrons will accumulate at the potential well near the P+ region. The accumulation of electrons will reduce the hole barrier and hole current starts to flow into the channel. Likewise, these holes will accumulate at the potential well near the N+ region, and further reduce the electron barrier. And these cycles keep going so the device will turn on abruptly with a small change in V_G.

2.4 Device Fabrication and Characteristics

FBFETs were fabricated on lightly doped p-type SOI wafers using a "spacer FinFET" process flow [6]. After thermal oxidation to thin the SOI layer down to 50 nm thickness and to form an oxide hard-mask layer, spacer lithography was used to define narrow Si fins (with width TSi ~45nm), and optical lithography was used to define the S/D contact regions (Fig. 2.5a). After the SOI film was patterned by dry etching (Fig. 2.5b), a sacrificial oxidation (~3 nm SiO2) was performed to remove fin-sidewall etch damage, and then thermal oxidation was used to grow the gate oxide (3 nm SiO2). In-situ doped n-type poly- Si gate and low-temperature-deposited oxide (LTO) gate-hard-mask layers, each ~150 nm thick, were then deposited and patterned using optical lithography and dry etching (Fig. 2.5c). Fig. 6 shows a scanning electron micrograph of a FB-FET after this step. After gate sidewall oxidation (which narrowed TSi in the source/drain regions) and gate-sidewall nitride spacer formation (Fig. 2.5d), masked ion implantation was performed to separately dope the S/D regions p-type and n-type (Figs. 5e and 5f): 5E15 As+/cm2 at 80keV, 7o tilt (RP~57nm); 5E15 B+/cm2 at 15keV, 0o tilt (RP~59nm). Lastly, thermal

annealing (20s @ 900oC in N2, followed by 30m @ 400oC in forming gas) was performed to activate the implanted dopants and to improve Si/SiO2 interface properties.

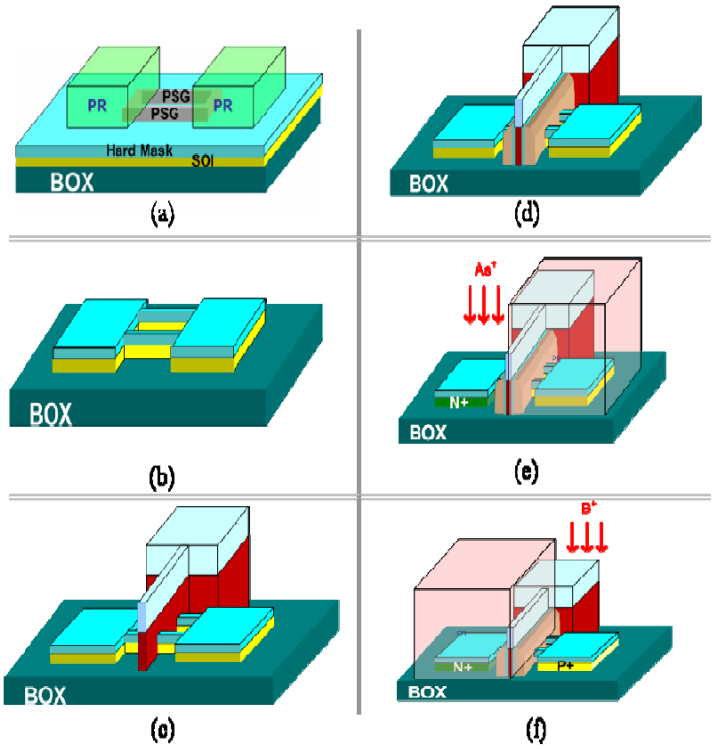

Figure 2.6: Fabrication process flow of FBFET.

The measured I_D-V_G characteristic is shown in Figure 2.7. The n-type FBFET transistor behavior appears only after properly conditioning the spacer charges. The SS is 1.67mV/decade with an I_{ON}/I_{OFF} ratio larger than 10E6.

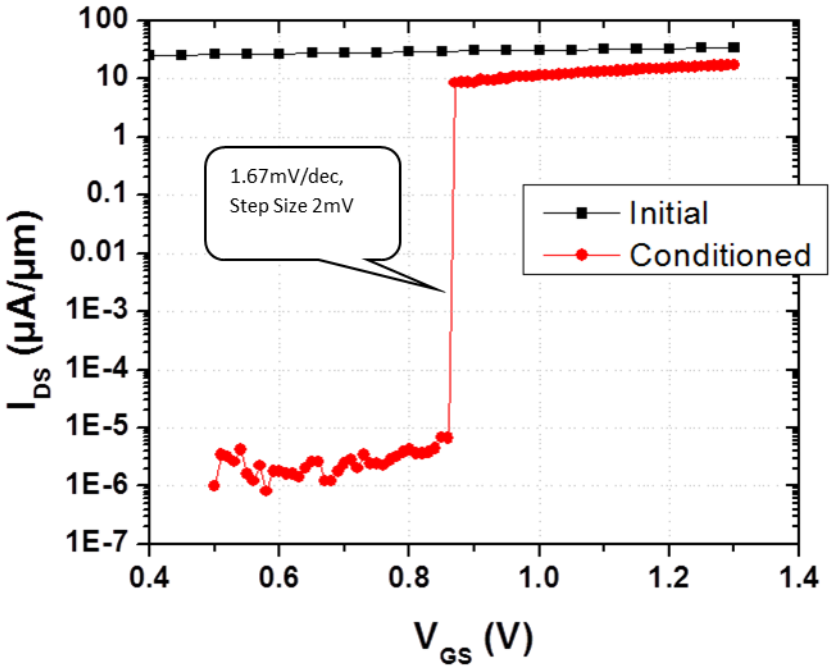

Fig. 2.7: FBFET transistor behavior appears only after properly conditioning the spacer charges.

Because this device uses both carriers to conduct current, it can be operated either as a PFET or an NFET depending on the terminal connections. If operated as a NFET (PFET), the P+ will be the drain (source), and N+ the source (drain). Supply voltage will be applied to the drain (source), with source (drain) grounded. Figure 3 shows the ID-VG curves of a FBFET operating in both NFET and PFET mode.

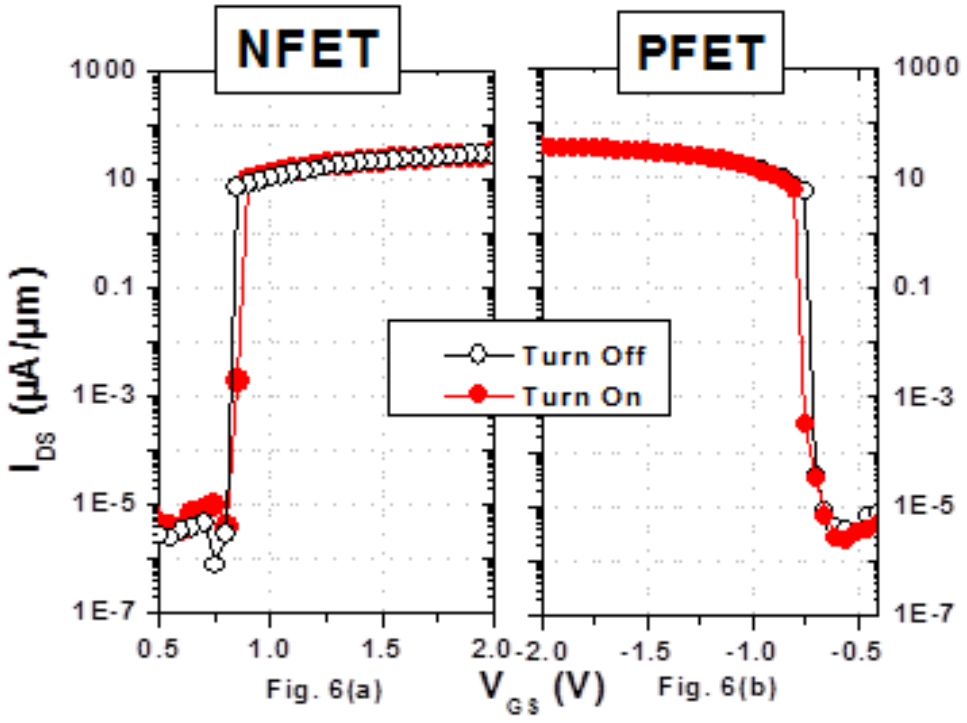

Fig. 2.8: (a) N-type FBFET. Vn=0V, Vp=1.1V. (b) P-type FBFET. Vp=0V, Vn=-1.1V

2.5 Quantitative Model

With the qualitative model in mind, we can try to analyze the feedback mechanism analytically by studying the gain of the device as illustrated in figure 2.9.

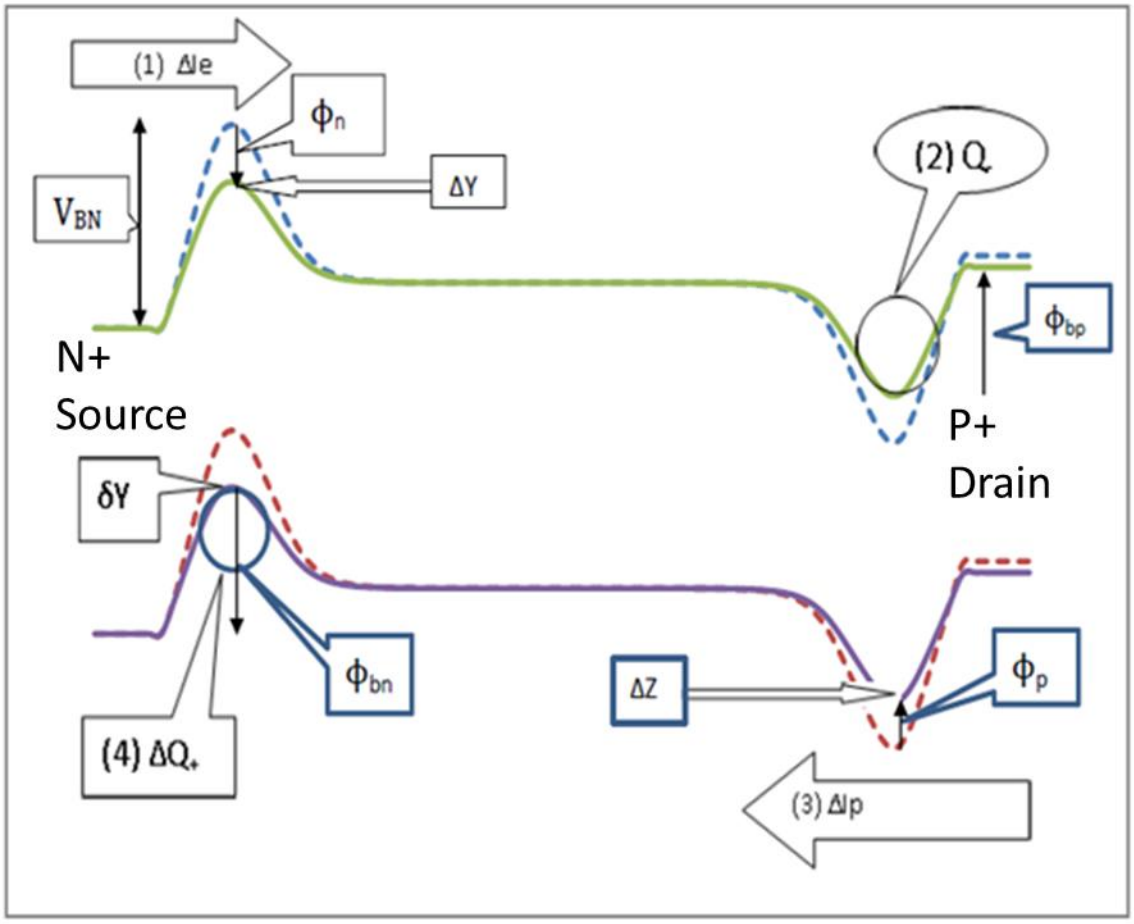

Fig. 2.9: Four steps in the feedback loop. Dash line – Low V_{DD}. Solid line – High V_{DD}.

Let V_{BN} (the potential barrier for electron injection) be the initial potential barrier between the N+ source and the N spacer region (after conditioning with trapped electrons) at zero gate bias and zero drain bias at equilibrium.

Let ϕn (ϕp) be the additional reduction of the electron (hole) injection barrier at a positive gate bias (V_{G0}) and drain bias (V_{D0}) at equilibrium. The electron injection barrier height can be written as (V_{BN} – ϕn).

Let the initial electron current at V_G=V_{G0} and V_D= V_{D0} be $I_{eo} * (e^{\left(\frac{\phi n}{kT}\right)} - 1)$, and at the same bias, the initial hole current injected through the hole barrier (at the drain side) will be defined as $I_{po} * (e^{\left(\frac{\phi p}{kT}\right)} - 1)$. Where, Ieo and Ipo define as the electron and hold current when ϕn and ϕp are zero.

Now, assuming there is a smaller perturbation ΔY to the electron injection barrier due to a small changes of the gate voltage or drain voltage.

1) First, the change in ΔY will induce more electrons injected into the channel. The change in electron current (ΔI_e) is given by:

$$\Delta I_e = I_{eo} * (e^{\left(\frac{\phi n}{kT}\right)} - 1) * (e^{\left(\frac{\Delta Y}{kT}\right)} - 1) \quad (2.2)$$

Using Taylor expansion on $e^{\left(\frac{\Delta Y}{kT}\right)}$ and only include the first two terms, we have:

$$\Delta I_e = I_{eo} * \left(e^{\left(\frac{\phi n}{kT}\right)} - 1\right) * \frac{\Delta Y}{kT} \quad (2.3)$$

2) Assume there is no recombination in the channel, so the injected electrons will accumulate in the E_C potential well near the drain. Some carrier will be stored locally in the well, while some will have sufficient kinetic energy to surmount the potential well barrier and injected into the drain and get recombined.

$$\Delta I_e = \Delta Q_- / \tau_- + \Delta I_e * A e^{\left(\frac{-\phi bp}{kT}\right)} \quad (2.4)$$

where, ΔQ_- is the charge stored in the potential well, τ- is the electron carrier lifetime, ϕbp is the barrier potential seen by electrons in the potential well, and A is a parameter.

Therefore, the electrons stored in the E_C potential well is given by:

$$\Delta Q_- = \Delta I_e * \tau_- * (1 - A e^{\left(\frac{-\phi bp}{kT}\right)}) \quad (2.5)$$

3) The stored electrons will lower the V_{BP} (ϕp increases) and induce more holes injected into the channel. The change in the hole barrier (ΔZ) and change in hole current (ΔI_P) are given by:

$$\Delta Z = \frac{\Delta Q_-}{Cp} \quad (2.6)$$

$$\Delta I_p = I_{po} * (e^{\left(\frac{\phi p}{kT}\right)} - 1) * (e^{\left(\frac{\Delta Z}{kT}\right)} - 1) \quad (2.7)$$

where, C_P is the capacitance under the P+ spacer. Again, using Taylor expansion on $e^{\left(\frac{\Delta Z}{kT}\right)}$ and only include the first two terms:

$$\Delta I_p = I_{po} * (e^{\left(\frac{\phi p}{kT}\right)} - 1) * \frac{\Delta Z}{kT} \quad (2.8)$$

4) Similar to 2) and 3), the holes current (assume no recombination in the channel) will flow to the source side and be stored in the valance band (E_V) potential well near the N+ source, and the V_{BN} will be reduced by δY:

$$\Delta Q_+ = \Delta I_p * \tau_+ * (1 - B e^{\left(\frac{-\phi bn}{kT}\right)}) \quad (2.9)$$

$$\delta Y = \frac{\Delta Q_+}{Cn} \quad (2.10)$$

where, τ+ is the hold carrier lifetime, Cn is the capacitance under the N+ spacer, ΔQ_+ is the change in holes in the N+ spacer, ϕbn is the barrier seen by holes in the hole well, and B is another parameter.

Therefore, the gain equation can be written as:

$$Gain = \frac{\delta Y}{\Delta Y} = \frac{\tau_- \tau_+ {I_{eo}}^* {I_{po}}^*}{CnCp(kT)^2} \tag{2.11}$$

where:

$${I_{eo}}^* = I_{eo} * (e^{\left(\frac{\phi n}{kT}\right)} - 1) * (1 - Ae^{\left(\frac{-\phi bp}{kT}\right)}) \tag{2.12}$$

$${I_{po}}^* = I_{po} * (e^{\left(\frac{\phi p}{kT}\right)} - 1) * (1 - Be^{\left(\frac{-\phi bn}{kT}\right)}) \tag{2.13}$$

When the gain is equal to or great than 1, the positive feedback will trigger the abrupt turn on of FBFET.

2.6 FBFET Simulations

Medici is used to perform device simulations. However, simulation of FBFET I_D-V_G characteristics is plagued with non-convergence problems, probably because the device is bistable in the low-V_G region. Fortunately, much can still be learned from the I_D-V_D simulations.

Simulation (Fig. 2.10) confirms that without the spacer charges, the Id-Vd characteristic is that expected of a PIN diode with 60mV/decade swing until high-level injection and ohmic effects set in. With appropriate spacer charges, the Id-Vd characteristics also exhibit steep transitions. As Vds (Vp) increases, Ev in the P+ region is lowered but the Ev minimum under the spacer remains unchanged and a larger hole current flows into the channel. This initiates the positive feedback just as a higher Vg does by allowing more electron current to flow as described previously. Note that the turn-on and turn-off transitions occur at different Vds values. The Id-Vd steep transitions and hysteresis are verified by experiment in Fig. 2.11.

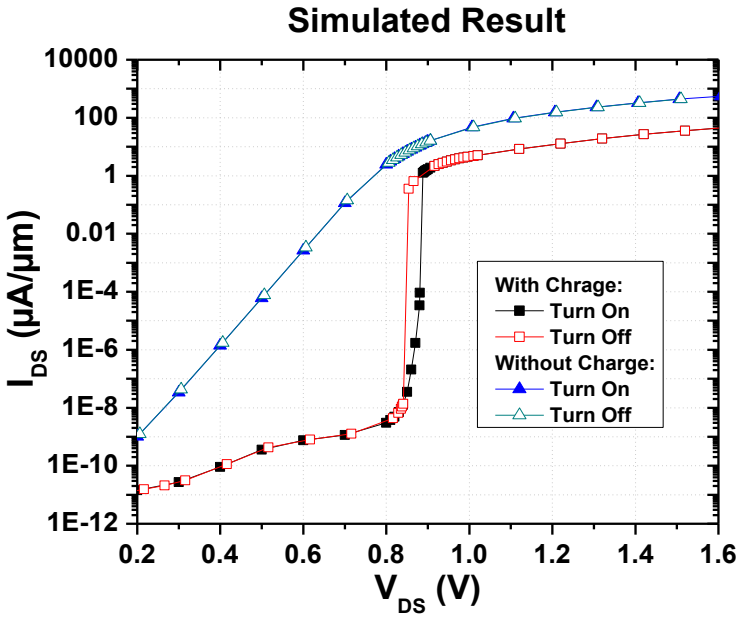

Figure 2.10: Without spacer charge, Id-Vd is that of a PIN diode. After conditioning, steep transition appears. Lg=0.4mm. Vg=0.4V.

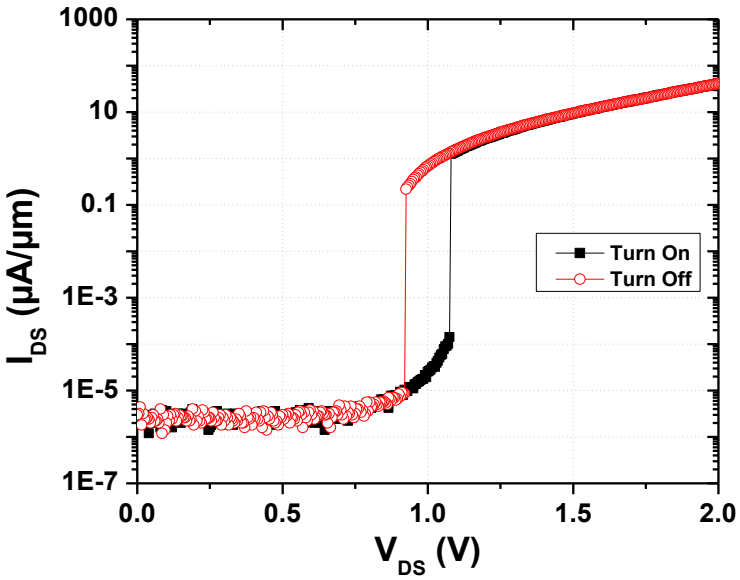

Figure 2.11: Experimental verification of the steep Id-Vd transition. Lg=0.37mm. Vg=-0.5V.

2.7 Programming Characteristic

Fig. 2.12 shows the simulated effects of decreasing the hole charge stored in the P+ side spacer. As a result, a lower Vds (Vp) is needed to inject the same hole current over the hole barrier and the curve in Fig. 2.12 shifts to the left. The ratio of 2E12q C/cm2 (reduction of spacer charge) to 0.1V (reduction in the transition Vds in Fig. 2.12) agrees well with the areal capacitance of the 3nm gate oxide of the FBFET. When the stored carrier density is reduced to 1E12q C/cm2, there is no longer a sufficient P+ side barrier and the simulated Id-Vd curve shows the 60mV/decade characteristic of a simple PIN diode.

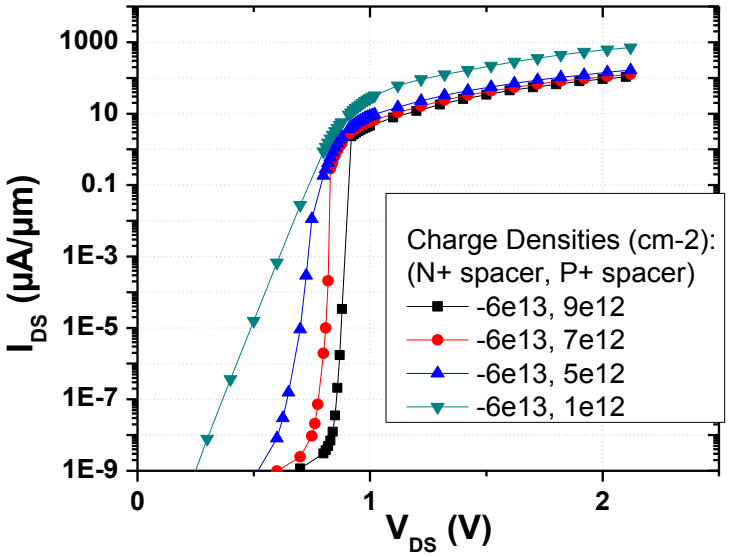

Fig. 2.12 Simulated effects of reducing the P+ side spacer charge. Vn= Vs=0V, Vg=0.4V. Lg=0.4mm.

Fig. 2.13 indicates it takes 2E13 cm-2 change in the N+ side spacer electron density to effect the same 0.1V shift in Vds – ten times lower sensitivity as compared with the P+ side spacer charge. Initiating steep switching by raising Vp is very similar to initiating steep switching by reducing Vg for a FBFET operating as a p-type device, because both involve reducing the hole barrier.

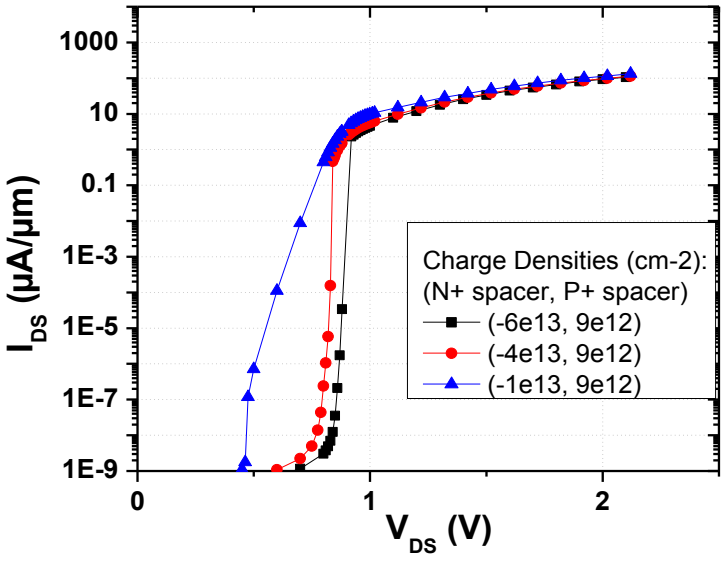

Fig. 2.13 Simulated effects of reducing the N+ side spacer charge. Vn= Vs=0V, Vg=0.4V.

As expected, Fig. 2.14 shows experimentally that positively charging the P+ side spacer, thus increasing the hole barrier height, can effectively shift the threshold voltage to more negative values.

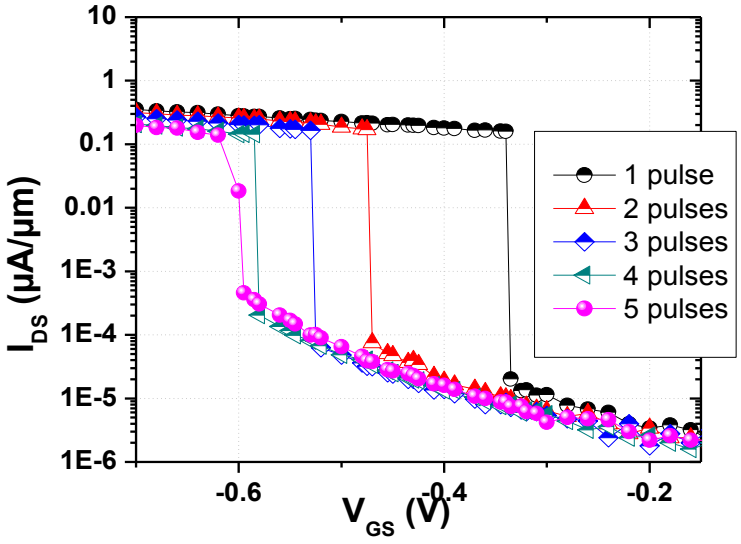

Fig. 2.14 Measured changes in P-FBFET Vt due to P+ side spacer charge increase. Programmed with 10us pulses at Vp=0V,Vn=-8V, Vg=-9V. Lg=0.37mm. Vds=0.9V.

By symmetry, one would expect that reducing the electron charge stored in the N+ side spacer would reduce the electron barrier and reduce the N-FBFET threshold voltage. This is verified experimentally in Fig. 2.15.

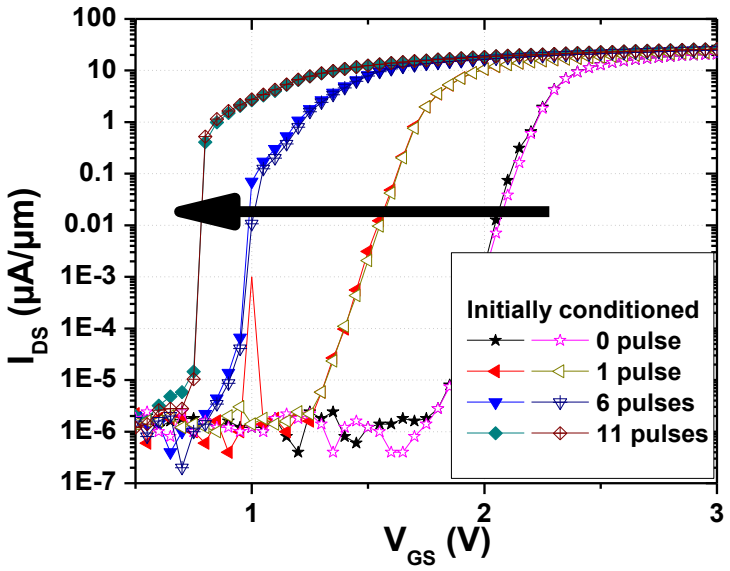

Fig. 2.15. Measured changes in N-FBFET Vt due to N+ side spacer charge reduction. Solid symbols: low Vg to high Vg. Open symbols: high Vg to low Vg. Programmed at Vn=0V, Vp=-3V, Vg=-9V. Lg=0.35mm. Vds=0.9V.

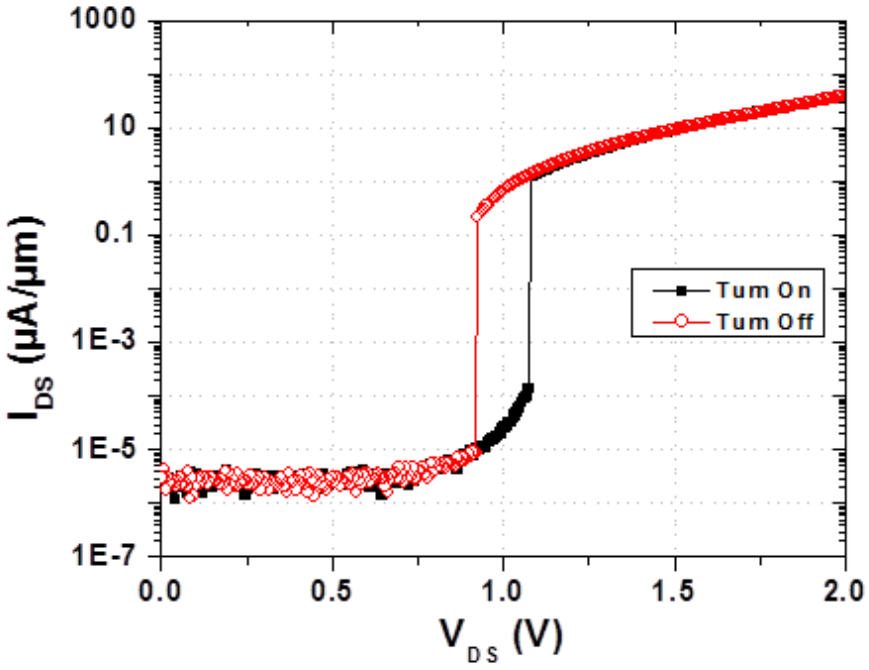

Fig.2.16 Measured I_D-V_D curve. The turn-on and turn-off V_Ds are different.

2.8 Alternate structure using ion implantation

The carrier barriers, V_{BN} and V_{BP} are crucial in creating the abrupt switching behaviors, but it is not a simple procedure to condition the device before it can be functioning. Moreover, charges stored in the nitride spacer may leak out overtime. An alternate approach is to use ion implantation to create the barriers. Fig. 2.17 shows the device structure. Instead of using nitride spacers to trap charges to create barriers for electrons and holes, dopants can also be used to create the barriers. The intrinsic regions underneath the spacers can be doped with n-type near the P+ spacer and p-type near the N+ spacer.

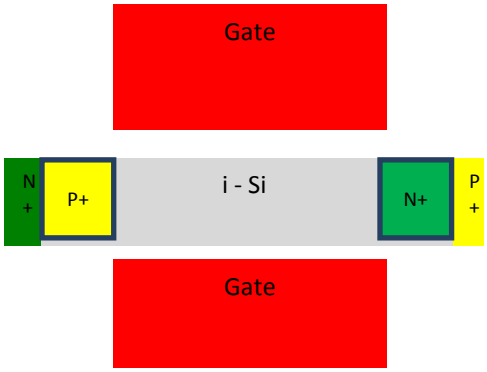

Figure 2.17. Schematic of FBFET structure using ion implantation.

Fig. 2.18 shows the band diagram using ion implantation to create the barriers. We can see the band diagram shows similar characteristics as in Fig. 3. There is still a large V_{BN} and V_{BP} blocking carriers entering the channel in the off-state, and the barriers are reduced in the on-state.

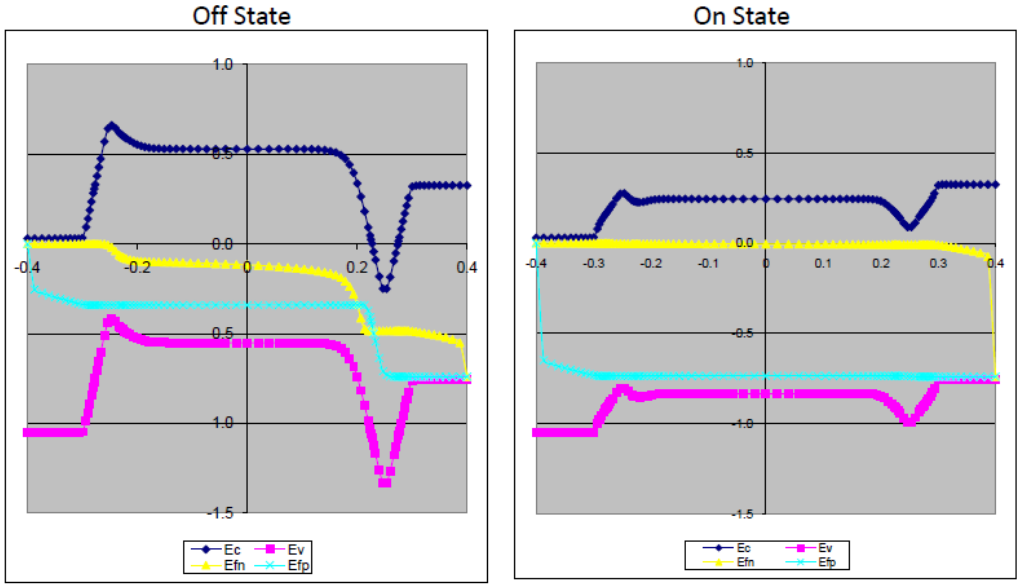

Figure 2.18. Simulated band diagram of FBFET using dopants to create carrier barriers.

Fig. 2.19 is the simulated I_D-V_G curve for this structure. The I_{ON} is low because the V_D is only 0.8V due to convergence problem.

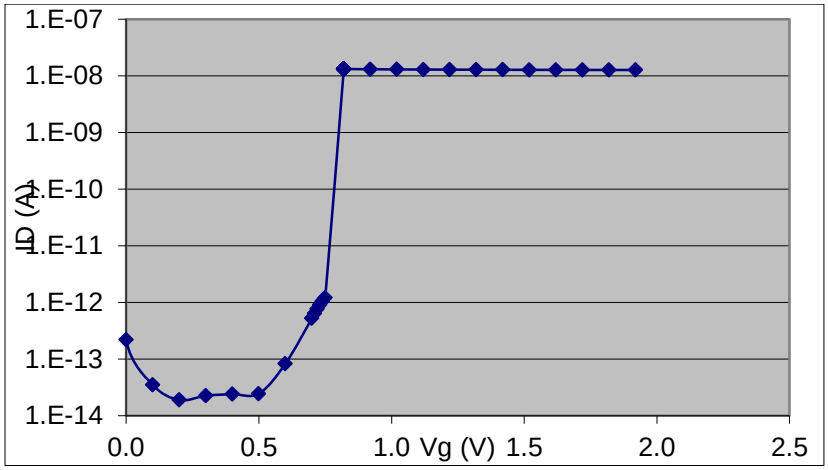

Fig 2.19. Simulated ID-VG of FBFET using ion implantation.

2.9 FBFET considerations

Although FBFET has demonstrated excellent SS, there are some aspects of FBFET should be considered.

Speed. The turn on speed should be proportional to the transit time of carriers, and the turn time will depends on how fast the carriers are recombined in the potential wells. Compare with ~ps turn-on turn-off time of MOSFETs, FBFET may have some disadvantage in this regard.

Density. Since there is extra area required for the potential wells, the total area for a FBFET will likely be larger than a MOSFET for the same feature size. Moreover, the scaling capability of the potential wells with feature size is still unknown. It might be a limiting factor for this technology.

V_{DD} scaling. Since there is a built-in potential between the source and the drain, this sets the limit of the minimum operating V_{DD}. Lower bandgap material may help lower the required V_{DD}.

2.10 Conclusion

The FBFET has shown excellent subthreshold swing of 1.67mV/dec with high ION/IOFF ratio (~10E6). It can also be operated at relatively low supply voltage (<1V). The analytical model for the FBFET feedback mechanism has been presented, and the theory of the feedback mechanism agrees well with both experimental and simulated results.

However, for this device to have practical use for logic, the required power supply must be able to scale down. Future research of fabricating FBFET using a low bandgap material might be an option. Other properties such as the transient response and the sensitivity to noise should also be investigated further.

Besides the non-volatile memory and logic applications, FBFET might also be used for sensor applications due to its abrupt SS.

2.11 References

[2.1] Hu, C., et al., "Green Transistor - A VDD Scaling Path for Future Low Power ICs," International Symposium on VLSI Technology, Systems and Applications, pp.14-15, April, 2008.

[2.2] Gopalakrishnan, K., et al, "Impact ionization MOS (I-MOS)-Part I: device and circuit simulations," Electron Devices, IEEE Transactions on , vol.52, no.1, pp. 69-76, Jan. 2005

[2.3] Padilla, A., et al, "Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages," Electron Devices Meeting, 2008. IEDM 2008. IEEE International , vol., no., pp.1-4, 15-17 Dec. 2008

[2.4] Yeung, CW., et al." Programming Characteristics of the Steep Turn-on/off Feedback FET (FBFET)", VLSI, Tech. Dig. (2009)

Chapter 3 Negative Capacitance FET (NCFET)

3.1 Introduction

In the last couple decades, the phenomenal growth of mobile electronics is fueling the demand for multi-functional, high performance and ultra-low power integrated circuits. As transistor scaling continues, reduction in V_{DD} is crucial for future ultra-low power electronics. For MOSFETs, as mentioned in Chapter 1, scaling V_{DD} means the threshold voltage needs to scale down accordingly at the expense of off-state leakage because the subthreshold slope is fundamentally limited to 60mV/decade. Transistor technologies with sub-60mV/dec swing allowing V_{DD} scaling to 0.5V and below without compromising leakage are therefore highly desirable.

In 2008, Salahuddin proposed using ferroelectric, which theoretically has a negative capacitance transition between the two polarization states [3.1], to integrate to the gate stack of MOSFETs, and the negative capacitance can be exploited to reducing the SS of MOSFETs to 60mV/decade and below.

The promise of replacing the gate dielectric with ferroelectric (or any other negative capacitance elements in general) for ultra-low power applications is quite appealing for the following reasons:

1. Negative capacitance could act as an external amplifier to MOSFETs as it will "amplify" the gate voltage and therefore achieving SS of less than 60mV/decade.
2. NCFET does not change the transport physics of the MOSFETs; therefore, it can benefit from all the ongoing and future materials research aimed at improving the channel transport of MOSFET.
3. NCFET can be seen as simply replacing or inserting new dielectric(s) material into the gate stack of MOSFET. The process simplicity and the potential CMOS compatibility make it an attractive technology booster to MOSFET in the future.

The focus of this study will be to treat the ferroelectric (or if other negative capacitance elements exist) as a negative capacitance "blackbox", assuming the capacitance-voltage relation follows Landau's equation, and from a device prospective, to design, optimize, and simulate NCFET to evaluate the feasibility, potential, and limits of creating sub-60mV/decade swing and hysteresis free transistors.

The second part will be focusing on fabricating a NCFET prototype with epitaxial single-crystal ferroelectric integrated on Si channel MOSFETs.

3.2 Negative Capacitance

Before diving into negative capacitance transistors, let's look at negative capacitor.

One type of materials that might have the capability of having negative capacitance is ferroelectrics (FE) [3.1]. The free energy (F_P) of ferroelectric can be described by Landau's Theory:

$$F_P = 1/2aP\text{^}2 + 1/4bP\text{^}4 + 1/6cP\text{^}6 - EP \quad (3.1)$$

Where P is the polarization, E is the electric field, and a, b, and c are coefficients.

Since the derivative of the F_P w.r.t. P should be zero when the system is at equilibrium where the energy is minimized:

$$dF_P/dP = 0 \quad (3.2)$$

Therefore, electric field E can be written as:

$$E = aP + bP\text{^}3 + cP\text{^}5 \quad (3.3)$$

For a parallel plate capacitor:

$$V = E*t \quad (3.4)$$

Where V is the voltage and t is the thickness of the capacitor, and assuming charge (Q) equals polarization (P), we have a voltage-charge relation:

$$V = aQ/t + bQ\text{^}3/t + cQ\text{^}5/t \quad (3.5)$$

Fig. 3.1(a) shows the P-E relation, and can be converted into Q-V relation as shown in (b). The slope in (b) is the capacitance (C=Q/V). As we can see, according to Landau's equation, there is positive capacitance region and the possibility of a negative capacitance region. Because the negative capacitance by itself is unstable, it is very difficult to directly measure negative capacitance experimentally.

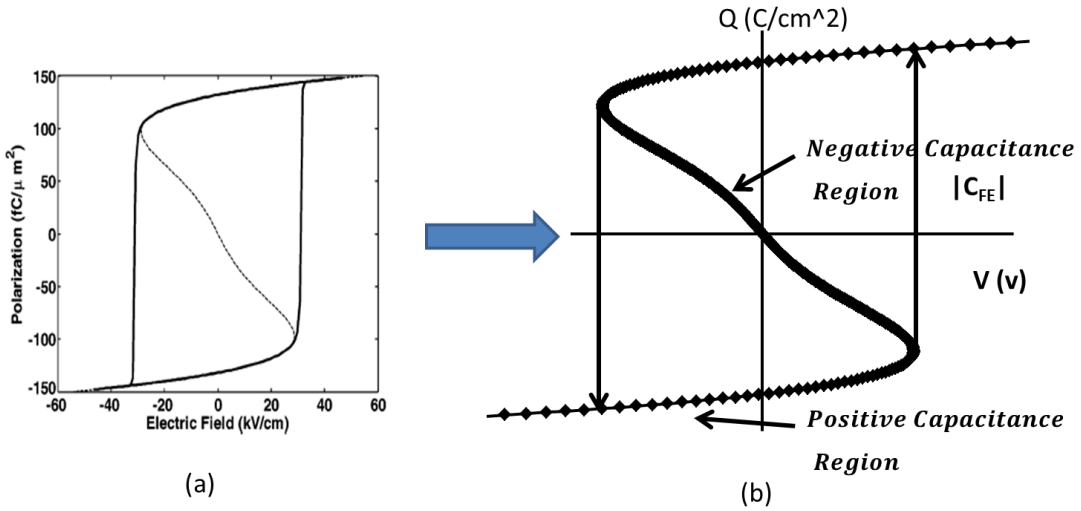

Fig. 3.1. (a) Polarization vs electric field for a typical ferroelectric material. [3.1] (b) Transformation of polarization vs electric field into charge vs voltage.

Negative capacitance by itself is unstable as mentioned above; however, when it is connected in series with another positive capacitor, the equivalent total capacitance (Ceq) could be larger than the positive capacitor, and Khan has measured negative capacitance using this argument [3.2]. The equivalent capacitance of two capacitors in series is given by:

$$Ceq = C1*C2/(C1+C2)$$

C1	C2	Ceq	Remark
10	10	5	Ceq smaller than C1 or C2
10	9	4.736842	
10	8	4.444444	
10	7	4.117647	
10	6	3.75	
10	5	3.333333	
10	4	2.857143	
10	3	2.307692	
10	2	1.666667	
10	1	0.909091	
10	0	0	
10	-1	-1.11111	Ceq is negative, unstable
10	-2	-2.5	
10	-3	-4.28571	
10	-4	-6.66667	
10	-5	-10	
10	-6	-15	
10	-7	-23.3333	
10	-8	-40	
10	-9	-90	
10	-10	#DIV/0!	Ceq is undefined
10	-11	110	Ceq is larger than C1
10	-12	60	
10	-13	43.33333	
10	-14	35	
10	-15	30	
10	-16	26.66667	
10	-17	24.28571	
10	-18	22.5	
10	-19	21.11111	
10	-20	20	

Table 3.1. Equivalent capacitance of two capacitors connected in series.

Table 3.1 tabulates the equivalent capacitance when C2 varies from positive to negative. Note that when C2 is negative, and the absolute value of C2 is larger than C1, the equivalent capacitance will always be larger than or equal to C1. This simple result has profound impact on the design of negative capacitance FET, and will be discussed in next section.

In the following section, we will explain how to use negative capacitance to design a stable MOSFET (no hysteresis) with sub-60mV/dec swing.

3.3 Negative Capacitance FET (NCFET)

Now, using the Landau's Theory as the basis, we can look at the structure of a NCFET.

Figure 3.3 shows the schematic of a n-type NCFET.

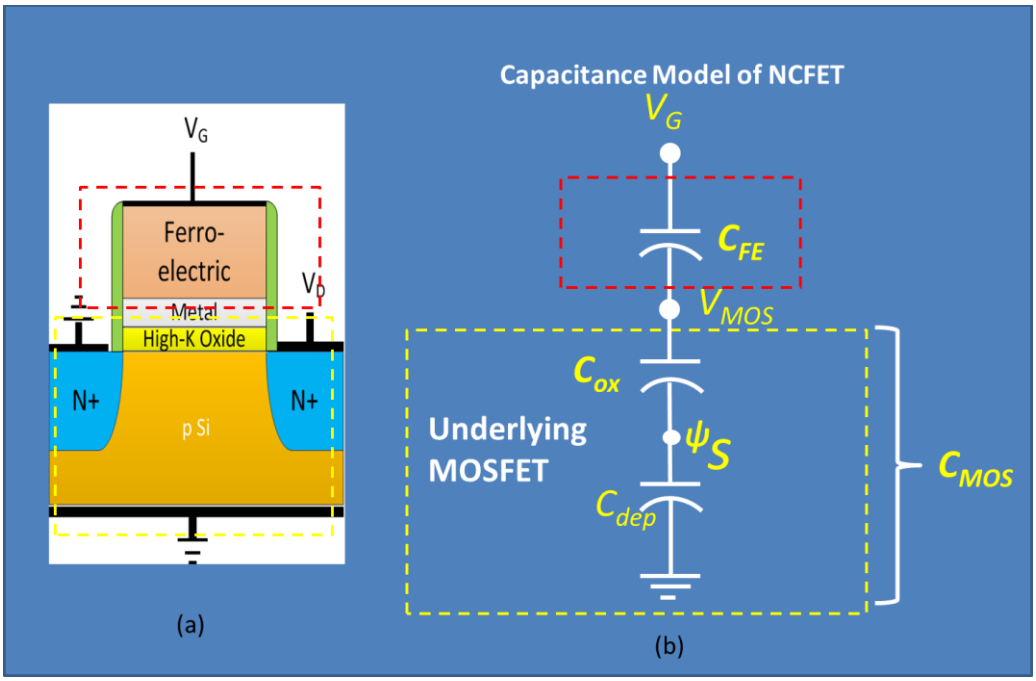

Figure 3.3: (a) Schematic of a NCFET. (b) Capacitance Model of NCFET

The structure of the N-type NCFET is shown in Fig. 3.3(a). N-type Si MOSFET with high K gate oxide is referred to as the intrinsic MOSFET. FE oxide is assumed to be deposited on a metallic template grown on the oxide [3.3]. The intermediate metallic layer between the FE and the high-K gate oxide is chosen following the experimental device [3.4]. This layer averages out the non-uniform potential profile along the source-drain direction as well as any charge nonuniformity coming from domain formation in the FE. Thus as long as the MOSFET is concerned, the FE looks like a monodomain dipole. This structure therefore can be used to understand, design, and simulate NCFET based on a 1-D landau model.

We use a simplified capacitance model (Fig. 3.3(b)) to illustrate the voltage amplification concept. The capacitance of NCFET can be represented by a series combination of ferroelectric capacitor (C_{FE}) and underlying MOSFET capacitor (C_{MOS}). The voltage relationship between V_G and V_{MOS} can be written as:

$$V_{MOS} = V_G \frac{C_{FE}}{C_{FE}+C_{MOS}} \tag{3.6}$$

If C_{FE} is a positive capacitor, V_{MOS} will always be smaller or equal to V_G, as the voltage drop from V_G to ground is divided between the two capacitors C_{FE} and C_{MOS}.

When C_{FE} is negative, equation 3.6 becomes:

$$V_{MOS} = V_G \frac{-|C_{FE}|}{-|C_{FE}|+C_{MOS}} \tag{3.7}$$

Therefore, the voltage amplification (Av) can be rewritten as:

$$Av = \frac{\partial V_{MOS}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}|-C_{MOS}} \tag{3.8}$$

From now on, the notation of C_{FE} in the text always implicitly refers to the magnitude of the negative capacitance state unless explicitly specified. Equation 3.8 shows that Av could be greater than 1 when C_{MOS} is larger than zero, meaning a small change of V_G will induce a larger change in V_{MOS}; therefore, the swing of NCFET can be smaller than 60mV/dec.

To achieve a large Av, the value of C_{FE} and C_{MOS} should be close. However, in order to avoid hysteresis, the Av cannot be infinite (mentioned in Chapter 2); therefore, C_{MOS} cannot be equal or exceed C_{FE} (from V_G= 0 to V_{DD}) or Av will become infinite. This is the key in designing a stable (no hysteresis) NCFET.

The subthreshold swing of a NCFET can be obtained by dividing the swing of the underlying MOSFET by the factor Av:

$$\text{NCFET SS} = \text{MOSFET SS} * \frac{1}{Av} = 60\text{mV/dec} * \left(1 + \frac{C_{dep}}{C_{ox}}\right) * \frac{1}{Av} \tag{3.9}$$

By substituting Av from Eq. 3.8into 3.9, and then expanding C_{MOS} into the series combination of Cox and Cdep, we get Eq. 3.10.

$$\text{NCFET SS} = 60\text{mV/dec} * \left(1 + \frac{C_{dep}}{C_{ox}} - \frac{C_{dep}}{|C_{FE}|}\right) \tag{3.10}$$

It is intuitive to think that Cdep/Cox increases the SS, so there is a "+" sign in front of the $\frac{C_{dep}}{C_{ox}}$ term; meanwhile, Cdep/C_{FE} reduces the SS (because of negative capacitance), so there is a "– " sign in front of the $\frac{C_{dep}}{|C_{FE}|}$ term. **It is also very important to note that for SS less than 60mV/decade, C_{FE} must be smaller than C_{OX} such that $\frac{C_{dep}}{C_{ox}} - \frac{C_{dep}}{|C_{FE}|}$ is less than zero**. This is the necessary condition for using negative capacitance to create sub-60mV/dec SS transistors. For conventional MOSFET design, reducing the swing can be achieved by increasing the gate capacitance and reducing C_{dep}. For NCFET, reducing C_{dep} alone cannot reduce the swing to below 60mV/dec. NCFET with close to zero Cdep can only achieve the MOSFET limit of 60mV/dec. Interestingly, a finite C_{dep} is needed for NCFET to achieve sub-60mV/dec swing.

And as mentioned above, C_{FE} must be larger than C_{MOS} to avoid hysteresis. It means SS cannot be negative, and it is the equivalent of satisfying the following condition:

$$\frac{C_{dep}}{C_{ox}} - \frac{C_{dep}}{|C_{FE}|} > -1 \tag{3.11}$$

Designing a NCFET with $C_{OX} > C_{FE}$ (for sub-60mV/dec) and $C_{FE} > C_{MOS}$ (for no hysteresis) while maintaining C_{FE} close to C_{MOS} (for large Av) within the range of V_G (e.g. 0 to V_{DD} for NMOS) requires special device considerations and will be discuss in section 3.4.

Criteria	Condition
No Hysteresis	$C_{MOS} < \|C_{FE}\|$
Sub-60mV/dec swing	$C_{OX} > \|C_{FE}\|$
Large Av (small SS)	$C_{MOS} \sim \|C_{FE}\|$

Table 3.2. Summary of the conditions for NCFET

3.4 Subthreshold Swing Optimization

As mentioned in section 3.3, designing a NCFET with sub-60mV/dec swing, hysteresis free, and sufficiently large Av (small swing) requires special considerations. In this section, we will look at how to design a hysteresis free sub-60mV/dec swing NCFET by optimizing the intrinsic MOSFET.

Large Av in the subthreshold region

As discussed above, to achieve a large Av, the value of C_{MOS} and $|C_{FE}|$ should be close. However, the change of C_{MOS} in the subthreshold region can vary from several times up to orders of magnitude, while the change in C_{FE} is very small compared with the change in C_{MOS}.

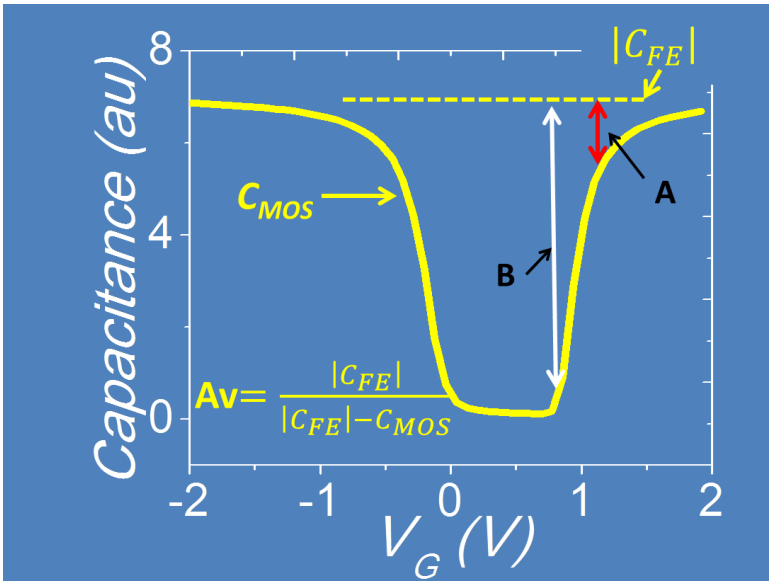

Figure 3.4. Capacitance of $|C_{MOS}|$ and $|C_{FE}|$.

Fig. 3.4 illustrates the no hysteresis scenario ($C_{FE} > C_{MOS}$). At A, the Av is large because the difference between C_{FE} and C_{MOS} is small. However, at B (the onset of subthreshold region), the Av is very small because the difference between C_{FE} and C_{MOS} is large.

One can reduce the swing by reducing the C_{FE} (e.g. by increasing the thickness of the FE) as illustrated in fig 3.5. However, once C_{FE} is smaller than C_{MOS}, the additional reduction in swing will be accompanied by hysteresis using conventional MOSFET design. Fig. 3.5 illustrates the trade-off between reducing swing and hysteresis. In this particular simulation, four structures are simulated with different ferroelectric thickness (t_{FE}) on identical intrinsic MOSFET structure. The SS reduces with increasing t_{FE} (smaller $|C_{FE}|$). Hysteresis is observed for t_{FE} equal 210nm and 260nm.

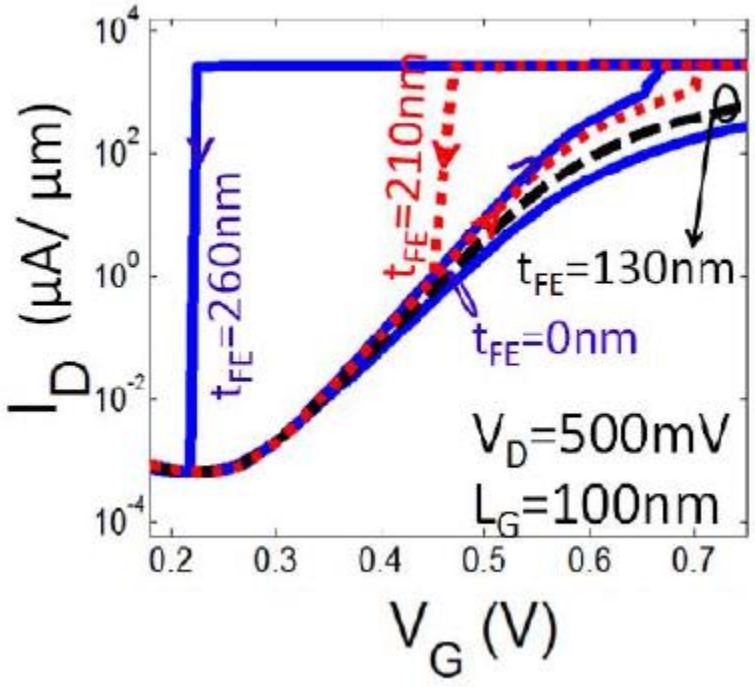

Figure 3.5. Simulated I_D-V_G of NCFET with different ferroelectric thickness (t_{FE}).

Therefore, it is not straight forward to achieve very small SS and hysteresis free NCFET using conventional MOSFET design. One way to address this issue is to engineer the C_{MOS} so that the variation of C_{MOS} is small in the subthreshold region. In the following two sections, we will describe two ways to achieve such design.

3.4.1 Super-Steep Retrograde Well Design.

Super-steep retrograde well (SSRW) design is used in bulk MOSFET to control short channel effects. A heavy and abrupt well doping in the channel helps reducing the sub-surface leakage. By optimizing the channel doping profile, a larger ratio of effective current (Ieff) to off-state current (Ioff) can be achieved.

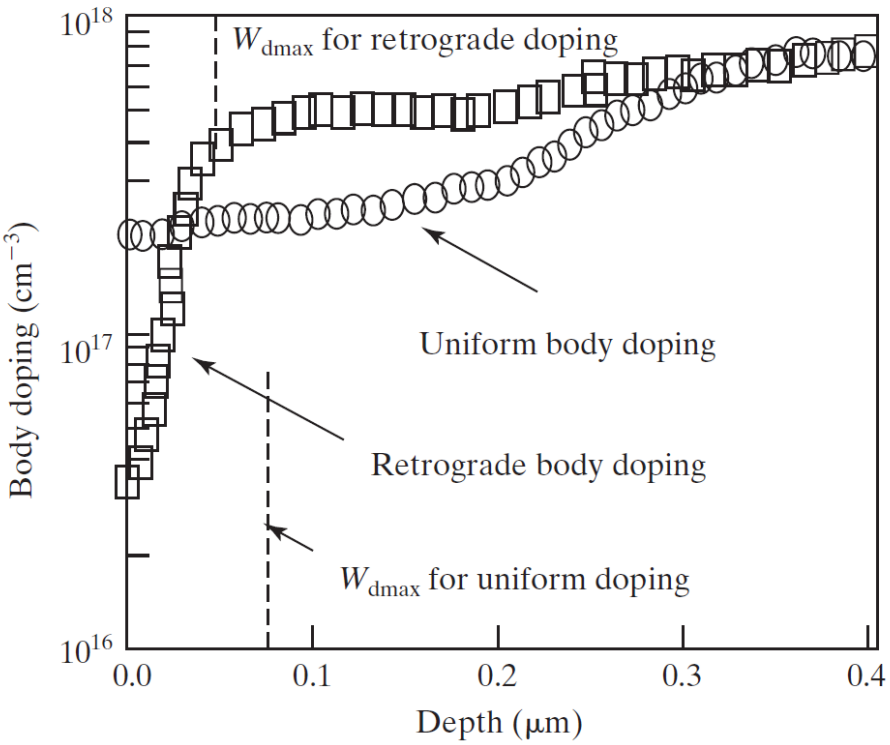

Figure 3.6. Comparison of a steep retrograde doping profile and a uniform doping profile. [3.5]

With abrupt retrograde well doping, the depletion width (Wdep) will be pinned at the undoped channel/retrograde well interface. The minimum value of depletion capacitance will be determined by the thickness of the lightly doped channel region (design parameter) instead of the maximum depletion width (Wdmax).

The advantages of this design for NCFET are:

(1) We can engineer the minimum of C_{MOS} by controlling the thickness of the undoped channel (Tsi).
(2) The change in C_{MOS} in the subthreshold region will be less sensitive to Vg because the Wdmax is pinned by Tsi.

In the following section, we will discuss how to exploit SSRW design to create a low subthreshold swing NCFET.

Structure and simulation method

The structure of the device is shown in Fig. 3.7(a). The bottom layer is heavily doped p-type (NWELL), which serves to terminate the depletion region in the channel and to cut off the sub-surface leakage path. The channel is a thin undoped silicon layer on heavily doped silicon or, in general, a thin semiconductor on conductor (TSOC), which is the key to this design. Similar to FinFET, the thin layer design also allows scaling to extreme short channels [3.6, 3.7] and reduces the effects of random dopant fluctuation and mobility degradation. This layer could be formed by epitaxial deposition as demonstrated in [3.10]. For simplicity, zero source/drain contact resistance is assumed. A ferroelectric (FE) film is deposited over a metal/high-k dielectric stack. The function of the electrically floating metallic layer and the use of 1-D Landau model for the FE are explained in [3.8].

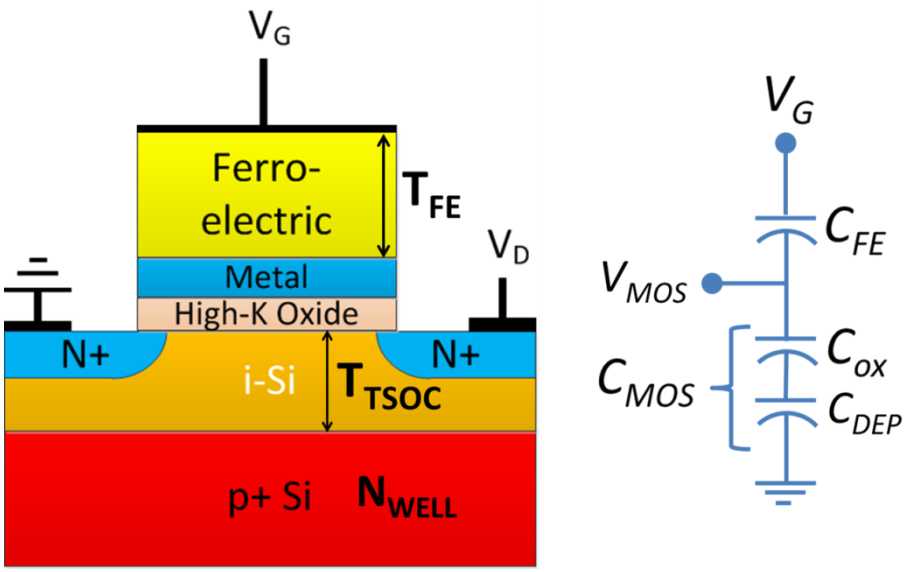

Figure 3.7 (a) Schematic cross-section views of a NCFET. (b) Simplified capacitance representation of a NCFET.

The design concept

We use a simple capacitance model (Fig. 3.7(b)) to illustrate the design concept, and then present detailed 2-D simulation results.

One may consider NCFET as a MOSFET with an added voltage amplifier. Because of the negative capacitance voltage amplifying effect (Av) ($Av=\Delta V_{MOS}/\Delta V_G$), subthreshold swing is reduce by a factor of Av. In the subthreshold regime, Av can be derived from a simple capacitive divider as shown in Fig. 3.7(b):

$$\mathbf{\Delta V_{MOS} = \Delta V_G * C_{FE} / (C_{FE} + C_{MOS})} \quad (3.12)$$

In order to obtain a large Av, the magnitude of C_{FE} and C_{MOS} needs to be relatively close. However, C_{MOS} is not a constant but varies with V_G (think the MOS CV curve), therefore Av is not a constant. If and when $|C_{MOS}|>= |C_{FE}|$, e.g. in strong inversion, the "swing" is infinite and I_D jumps to another branch of the hysteretic I_D-V_G curve [3.10].

For non-hysteretic operation, $|C_{FE}|$ needs to be larger than C_{MOS} throughout the V_G range. With uniformly doped substrate, the depletion capacitance (C_{DEP}) and therefore C_{MOS} could be much lower than C_{OX}. So from equation (1), Av cannot be significantly larger than 1 over a large V_G range. The proposed TSOC structure pins the depletion width at T_{TSOC}, making C_{DEP} large and insensitive to gate bias. Therefore, (1) a small SS can be achieved and (2) the SS remains small in the entire subthreshold regime.

Simulation results and discussions

We use a simple capacitance model (Fig. 3.7(b)) to illustrate the design concept, and then present detailed 2-D simulation results.

2D simulation includes all the usual effects in MOSFETs such as parasitic capacitances between the metallic floating gate and source drain, etc. For simplicity, strain induced mobility enhancement is not included. Fig. 3.8 shows I_D-V_G of non-hysteretic NCFETs at V_{DD} of 0.3 to 0.5V. The average SS is 27.2mV/dec for $0.5V_{DD}$, and 28.3mV/dec for $0.3V_{DD}$, calculated from ID of 1 pA/μm to 1 μA/μm.

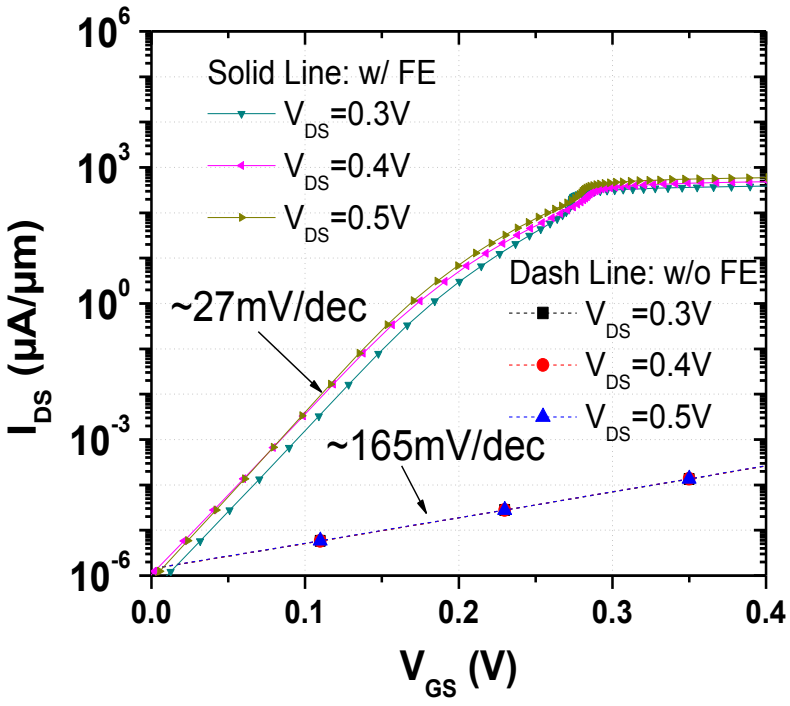

Figure 3.8. 2-D Simulated non-hysteretic NCFET I_D-V_G transfer characteristic.

Fig. 3.9 illustrates the effect of C_{FE} to the design of a stable non-hysteretic NCFET. The T_{FE} required is dictated by FE material characteristics. It is around 50nm using the FE reported in [3.11]. The optimal C_{FE} is defined as the minimal C_{FE} required for non-hysteretic operation.

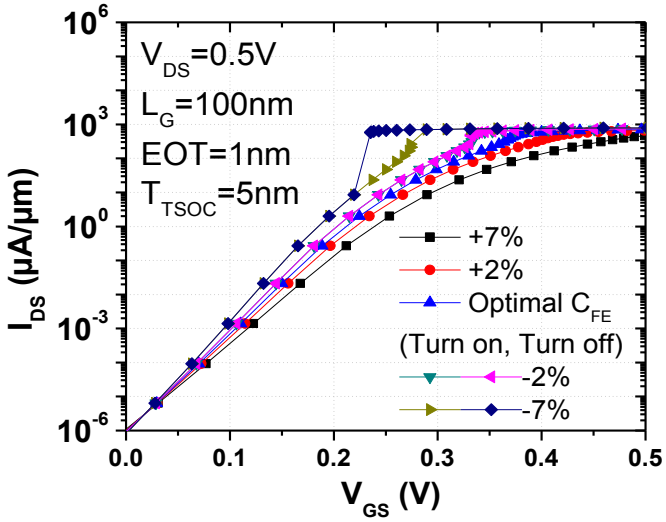

Figure 3.9. Simulated ID-VG for different C_{FE} values.

Fig. 3.10 shows that average SS changes almost linearly when C_{FE} is larger than the optimal value. It also indicates that thicker EOT reduces SS even with C_{FE} optimized for C_{OX}. Since T_{TSOC} and therefore C_{DEP} is not scaled with C_{OX} in this case, C_{MOS} stays in a narrower range from subthreshold to inversion for thicker EOT, resulting in a larger Av (Eq. 1) and therefore smaller SS.

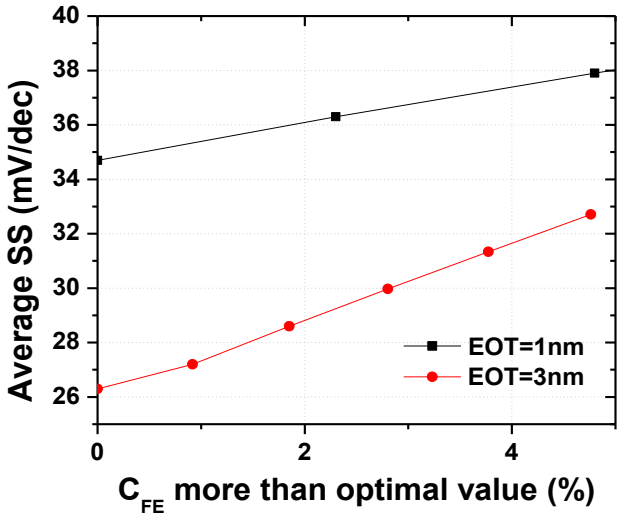

Figure 3.10. Effects of C_{FE} larger than the optimal value

Fig. 3.11 demonstrates that the SS is lowered with increasing NWELL doping concentration. Higher doping concentration is more effective in pinning the depletion region at T_{TSOC}, ensuring that C_{DEP} and therefore C_{MOS} in eq. 1 stays in a narrower range.

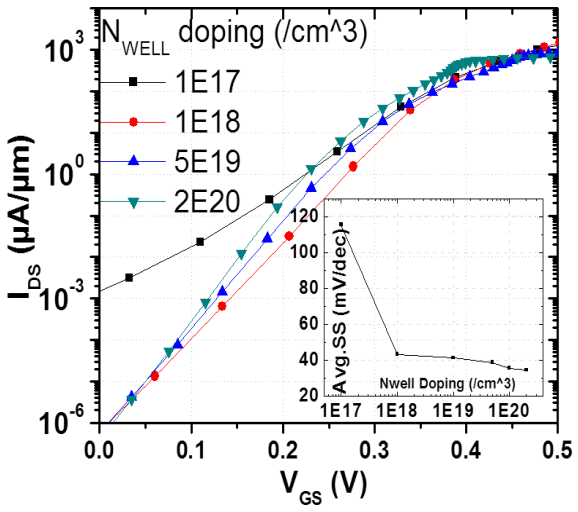

Figure 3.11. Fig. 6 Effects of N_{WELL} doping concentration.

Fig. 3.12 shows that, in order to maintain a certain average SS, T_{TSOC} should be reduced with EOT. For any fixed EOT, SS decreases with thinner T_{TSOC}, which increases C_{DEP}, making C_{MOS} relatively constant and Av very large from subthreshold to inversion, resulting in a smaller SS. Note that when T_{TSOC} is below 10nm, the reduction of SS accelerates. In this case, C_{DEP} could be larger than C_{OX}.

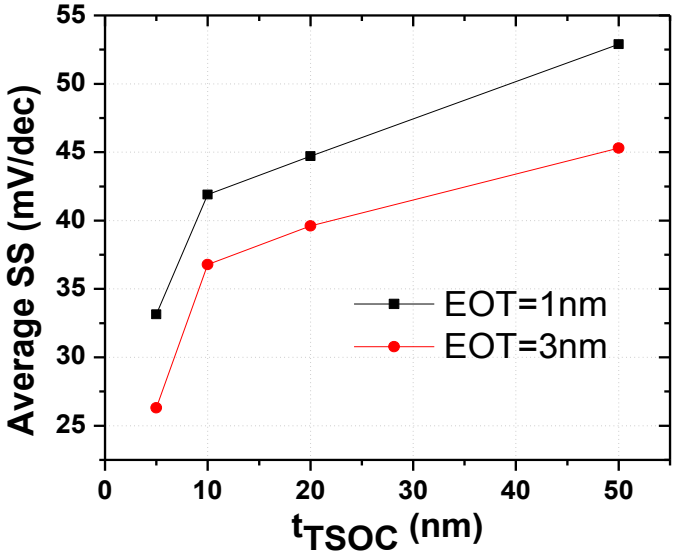

Fig. 3.12. Effects of t_{TSOC} and EOT on SS.

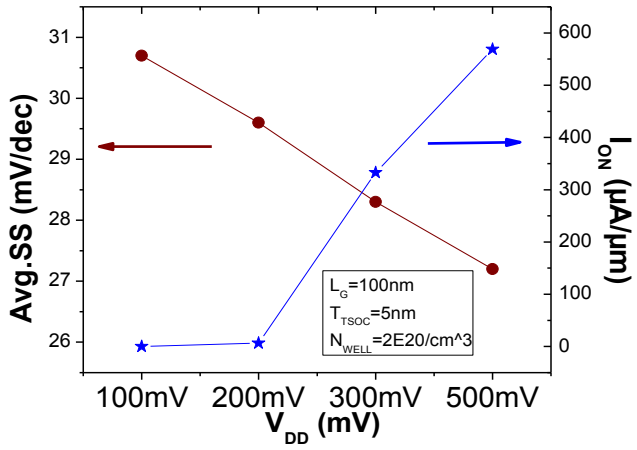

Fig. 3.13 summarizes the I_{ON} and average SS at different V_{DD}.

A non-hysteretic NCFET structure based on SSRW design with simulated SS of 28.3mV/dec over six orders of magnitude, with I_{OFF}=10pA/um, I_{ON}=0.3mA/um at V_{DD}=0.3V at L_G=100nm and without strain mobility enhancement. Performance can be further improved with shorter L_G or mobility enhancement. The thin T_{TSOC} layer design is responsible for the greatly improved performance.

3.4.2 Quantum Well (QW) Design

A new transistor concept is proposed that synergistically combines two important trends of future transistors: ultra-thin body to suppress the short-channel effects and sub-60mV/decade operation to drastically reduce power consumption. Negative-Capacitance-FET(NCFET) is a sub-60mV transistor candidate that works best when the transistor body is ultra-thin as shown here using TCAD simulation and 1nm Si body as example. Without considering mobility enhancement by strain or reduction by quantum confinement, this non-hysteretic NCFET can achieve I_{ON} of 250 μA/μm at 0.3V V_{DD}, I_{OFF}=10pA/μm, and 21mV/decade swing from 10pA to 10uA per micron.

Background

FinFET is an example of the ultra-thin body trend of future transistors [3.12]. In 2001, 3nm Si body was used to demonstrate excellent suppression of short-channel effects[3.13]. Recently, ~0.7nm monolayer-FETs have shown good mobility, perfect subthreshold swing (~60mV/dec), good ION/IOFF ratio, and are predicted to have excellent immunity to short-channel effects[3.14 ,3.15]. However, in all these transistors, 60mV/dec is still the bottleneck in scaling down the voltage and power consumption.

One solution to overcome this limit is to utilize negative capacitance (NC)[3.16, 3.17]. One may consider NCFET as a MOSFET with an external gate voltage amplifier. NCFET does not alter the carrier transport physics and therefore can benefit from all the ongoing and future materials research aimed at improving the MOSFET channel transport. Instead, NCFET seeks to 'amplify' the gate voltage electrostatically to achieve sub-60mV/dec subthreshold swing (SS). However, the price to pay for larger amplification is usually a hysteretic I_D-V_G, which is undesirable for circuit design and reduces the low V_{DD} benefit. Non-hysteretic operation has been purposed for bulk Si technology [3.18].

Device Structure Concept

The structure of the device is shown in Fig. 1(a). The key to this design is the bottom thin high-k buried oxide (BOX) over a metal (or degenerately doped Si) back gate or ground plane. For best performance, equivalent oxide thickness (EOT) of this layer (T_{BOX}) should be equal to or thinner than the EOT of the gate oxide (TOX). A thin BOX, besides providing a better body bias control, also serves to increase the ratio of C_{MOS} in Fig 1c[7] to the negative capacitance C_{FE} in the subthreshold regime. To achieve a non-hysteretic NCFET, the maximum C_{MOS} in Fig 2 should be less than the negative C_{FE} in Fig 1c so that V_G Amplification (Av) in Eq. (1) does not become infinite[3.19]. To achieve large Av (C_{MOS} close to C_{FE}) throughout the V_G operation range including the subthreshold region, we want C_{MIN} in Fig. 2 to be not much smaller than C_{MAX}.

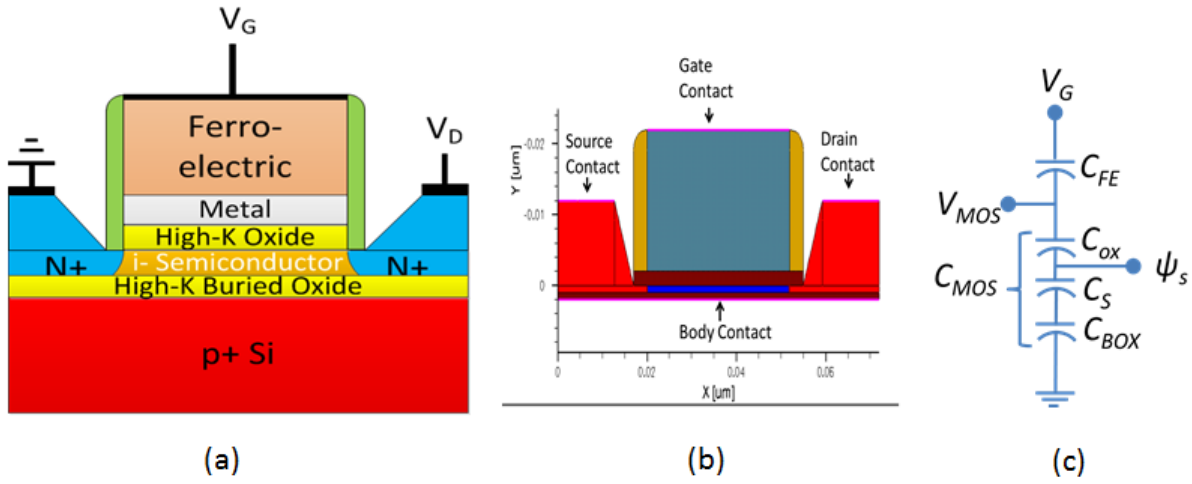

Figure 3.14. (a) Schematic (b) Simulation structure (c) Capacitance Model

Simulation Methodology

The channel is thin Si body with thickness T_S. In this simulation, we use default silicon transport parameters. A metal "floating gate" and high-k dielectric with raised source/drain is used. Sentaurus TCAD tool is used for 2D device simulation including the quantum confinement

effects and all the usual effects in MOSFETs such as parasitic capacitances between the metallic floating gate and source drain, etc. The source/drain contacts are placed on the raised region as shown in Fig. 1b. For simplicity, strain induced mobility enhancement is not included. The V_G Amplification due to the ferroelectric (FE) film is simulated with a 1-D Landau model as explained in [3.8]. This simulation methodology is adequate for estimating the V_G Amplification of V_{DD} reduction achievable regardless of the transport properties of the thin quantum-well body.

Simulation Results and Discussions

By using an ultra-thin body combined with a very thin back gate dielectric, C_{MOS} can be made insensitive to changing gate bias between 0 and V_{DD} (Fig. 2). This design provides a large Av throughout the V_G operating range while keeping the device hysteresis free.

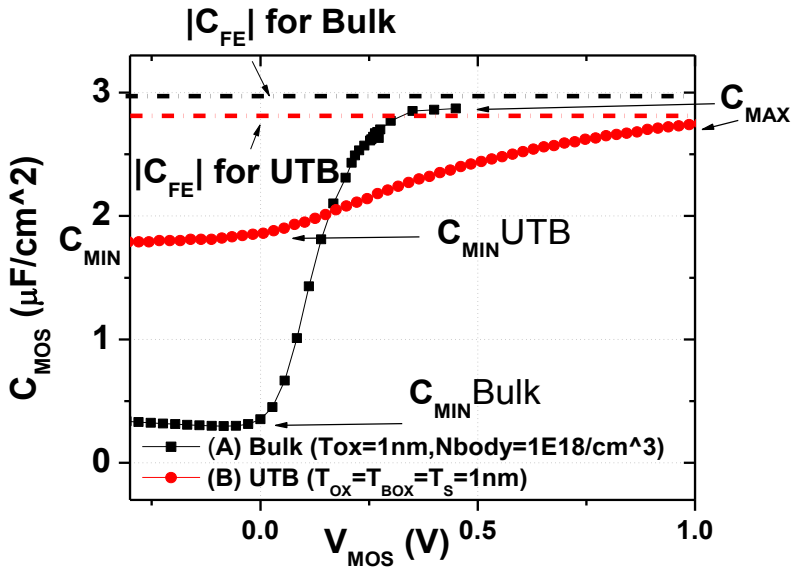

Figure 3.15. Simulated Capacitance-voltage curve of bulk and ultra-thin body capacitors.

One thing to note is that by reducing T_{BOX}, the SS of the intrinsic MOSFET will be degraded (due to large C_{BOX}), but the overall NCFET SS can still be less than 60mV/dec (Fig. 3.16). Further analysis on energy consumption will be discussed in next session.

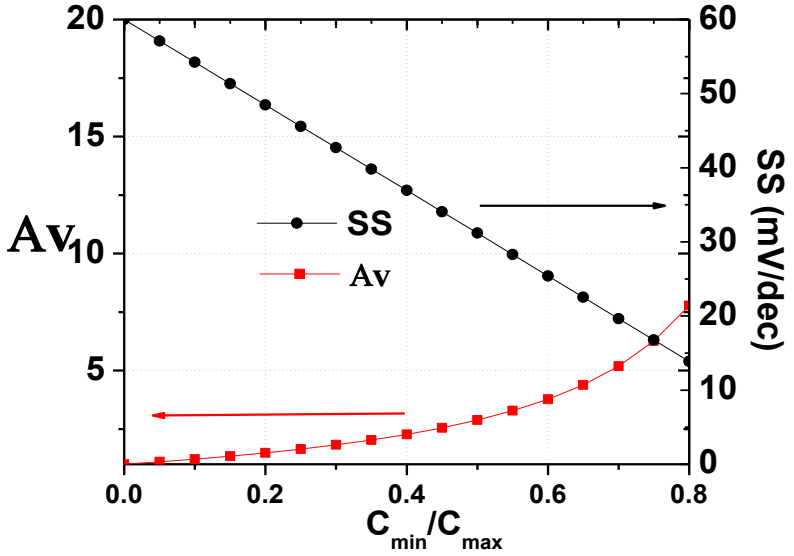

Figure 3.16. Plot of VG Amplification (Av), and NCFET SS for a given C_{MIN}/C_{MAX}.

Fig. 3.17 shows the I_D-V_G of non-hysteretic NCFETs at V_{DS} of 0.05V and 0.5V with average SS of ~ 20mV/dec while it is 235mV/decade for the intrinsic MOSFET. The swing and Av, are shown in Fig. 3.18.

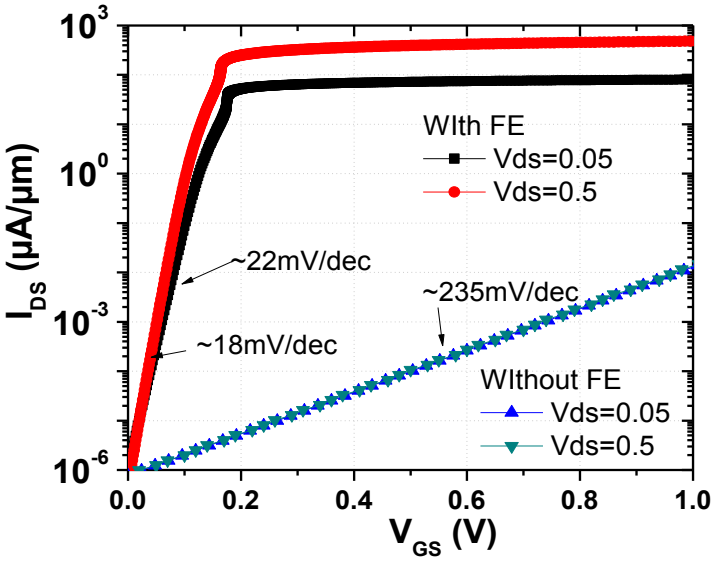

Figure 3.17. Simulated non-hysteretic NCFET (with FE) and intrinsic MOSFET (without FE) ID-VG transfer characteristic.

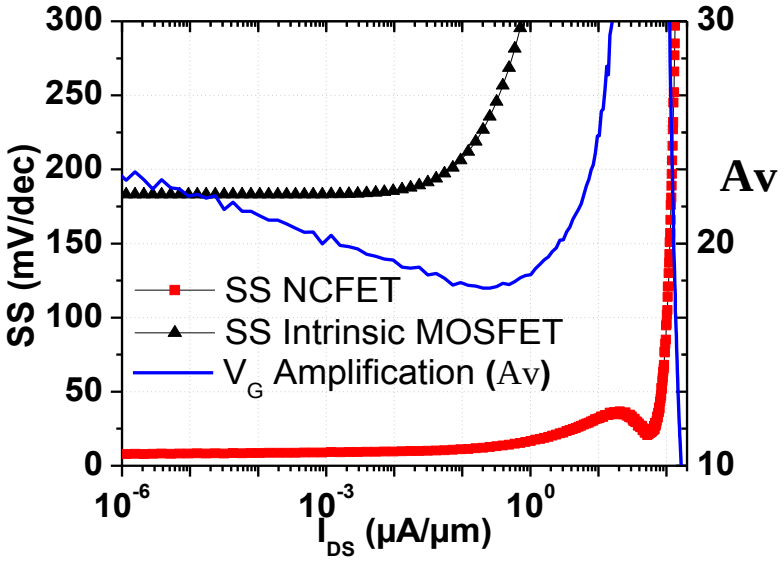

Figure 3.18. Subthreshold Swing and Av VS IDS.

Fig. 3.19 shows the relationship between Av VS V_G. Note that the Av increases after V_G reaches threshold voltage (V_T) because C_{MOS} approaches C_{FE}, and then peaks at ~0.165V, at which C_{FE} starts increasing and then begins transitioning into the positive capacitance state. Even after the convention definition (constant current) of V_T, high Av allows the I_D to increase exponentially rather than linearly. Before the Av peaks at around 0.165V, C_{MOS} is increasing due to the intrinsic MOSFET enters inversion regime. The Av increases as the difference between $|C_{FE}|$ and C_{MOS} reduces. If C_{MOS} can reach or exceed $|C_{FE}|$, Av will go to infinity and the FE will abruptly switch to the positive capacitance state and creating hysteresis. However, since by design, we controlled $|C_{FE}|$ by choosing the correct FE thickness such that C_{MOS} can never reach $|C_{FE}|$, the FE will then transition into the positive capacitance state governed by Landau's equation. During this transition, $|C_{FE}|$ increases, and this means that the difference between $|C_{FE}|$ and C_{MOS} widens again, so Av falls off. Then the FE will finish the transition and enters the positive capacitance state.

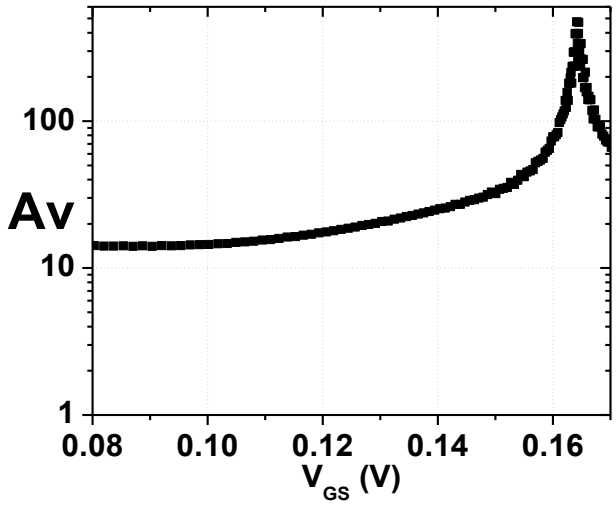

Figure 3.19. Av vs V_G. Av is extracted from the NCFET ID-VG (VDS=0.5V)

Fig. 3.20 shows the effects of changing the thickness of the fully depleted thin quantum-well body. It shows that SS degrades when Ts increases. It is due to lowered Av caused by reducing C_{MOS}, which consists of Cox, Cs due to fully depleted Ts, and C_{BOX} in series. Meanwhile, the I_{ON} increases because of the reduced transverse electric field mitigates mobility degradation due to surface scattering. The TCAD tool's mobility model may not be sophisticated enough to simulate the transport of future quantum-well bodies when the body thickness is less than few nanometers, and therefore the simulated I_{ON} should be taken as qualitative estimates.

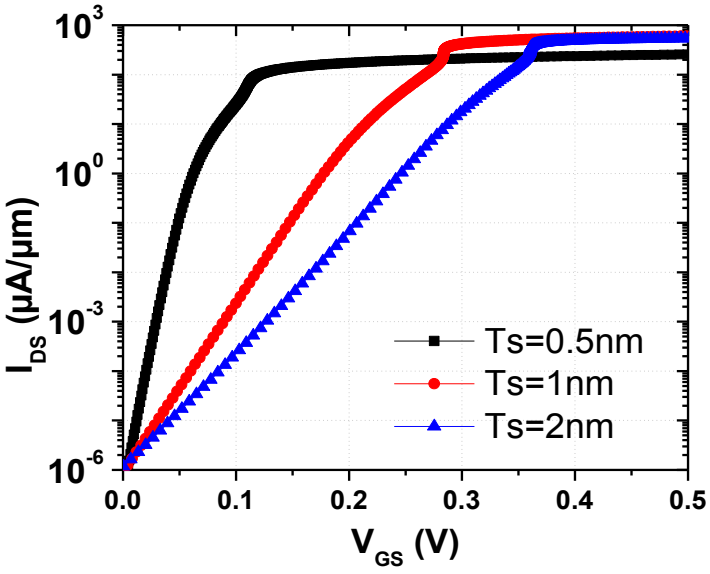

Figure 3.20. Non-hysteretic NCFET ID-VG for different body thickness.

As expected, Fig. 3.21 shows the similar effect of varying T_{BOX}. Similar to the effect of changing Ts, the SS also degrades with increasing T_{BOX}.

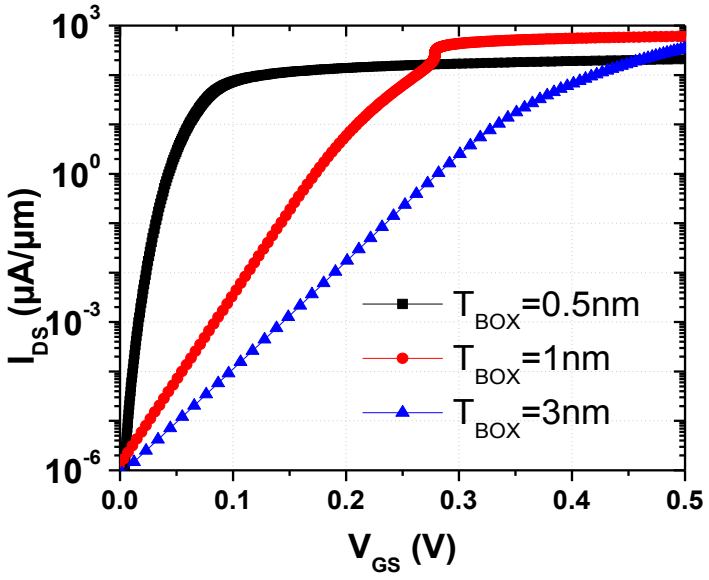

Figure 3.21. Non-hysteretic NCFET ID-VG for different BOX thickness.

Depending on the choice of the quantum-well body material, the dielectric constant of the material will impact the performance of the device. Fig. 3.22 shows that a larger dielectric constant body will improves SS and Av.

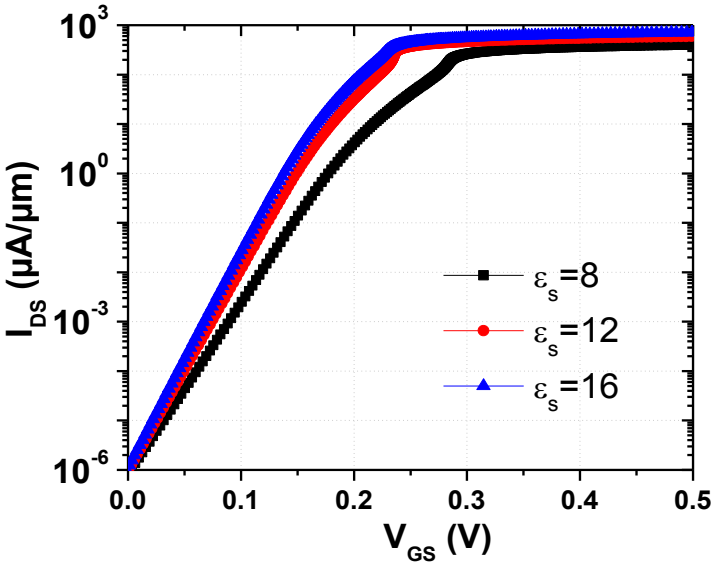

Figure 3.22 Non-hysteretic NCFET ID-VG for different dielectric constant body material.

Fig. 3.23 summarizes the I_{ON} and average SS at different V_{DD}.

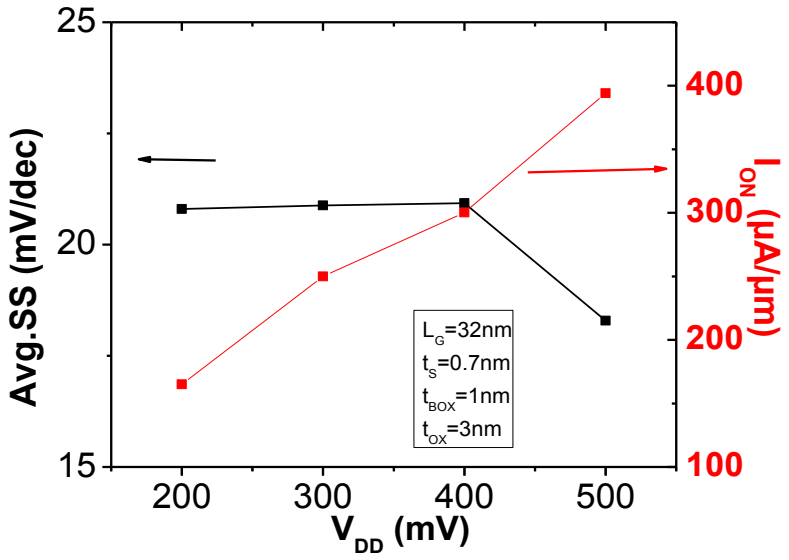

Figure 3.23. Summary of non-hysteretic NCFET ION and average SS for various VDD. Average SS is calculated from IDS of 10pA/μm to 10μA/μm.

Conclusion

A non-hysteretic NCFET structure using thin quantum well body combines two future trends synergistically. Ultra-thin body is needed to suppress short-channel effects and sub-60mV/decade operation is needed to reduce power consumption drastically. NCFET happens to need ultra-thin body as thin as 0.5nm to achieve 0.3V operation. We used simulation results of thin Si body NCFET to illustrate the possibility of achieving 10pA/μm I_{OFF}, 200uA/um Ion with 0.3V supply voltage. Layered semiconductors would be ideal for this future technology.

3.5 Energy Consumption

In the last two sections, we discussed the optimization of the intrinsic MOSFET for creating sub-60mV swing NCEFTs. Both SSRW and QW approaches are explored to engineer the Cdep (and therefore the C_{MOS}) for enhancing the Av and lowering the swing. However, there are trade-offs associated with driving an intrinsic MOSFET with larger Cdep. In this section, we will discuss some of the trade-offs.

In this section, we will treat the NCFET as a black box, intrinsic delay (t) and power-delay product (PDP) as the two performance metrics of the NCFET. The swing is also presented for

the insight it provides. (Notes for Chun: Chun, the third interesting metrics is dVt/dVd and dVt/dL, ie. effect of NCFET on scaling. I believe NCFET can be scales to shorter ultimate Lg than MOSFET because the Vg amplification effectively increase the gate or Vg control of the channel while the drain control of the channel is unchanged.)

Intrinsic device delay: tau = (Qon – Qoff)/Ion

Power-delay product: PDP = (Qon-Qoff)*Vdd

The MOFETs SS and NCFET SS are given by:

$$\text{MOSFET SS} = 60\text{mV/dec} * \left(1 + \frac{C_{dep}}{C_{ox}}\right) \tag{3.13}$$

$$Av = \frac{\partial V_{MOS}}{\partial V_G} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \tag{3.14}$$

$$\text{NCFET SS} = \text{MOSFET SS} * \frac{1}{Av} = 60\text{mV/dec} * \left(1 + \frac{C_{dep}}{C_{ox}} - \frac{C_{dep}}{|C_{FE}|}\right) \tag{3.15}$$

Fig. 3.24 plots the MOSFET SS and NCFET SS as a function of Cdep. As Cdep increases, the intrinsic MOSFET SS also increases, but since the increase in Av can compensated for the degraded SS in the intrinsic MOSFET, the overall NCFET SS can still be lowered as Cdep increases assuming these conditions hold:

1. $|C_{FE}| < C_{OX}$
2. $|C_{FE}| > C_{DEP}$

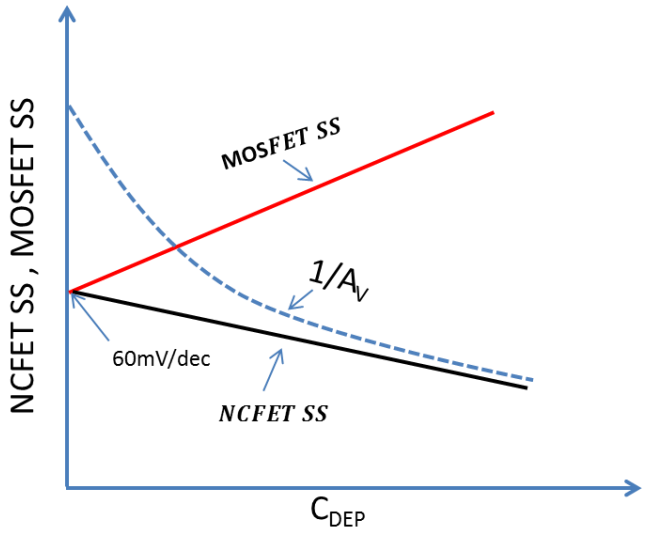

Figure 3.24. Swing vs Depletion Capacitance.

Increases amplification reduces V_{DD}, so the switching energy (ΔQV_{DD}) reduces. However, in an UTB structure, one way to engineer a larger amplification is to use a thinner Tsi. It is known that when Tsi gets down to 3nm and below, the mobilities degrades rapidly due to higher vertical field and larger surface scattering. To achieve the same drive current, more charges are needed to compensate for the mobilities drop.

Qualitatively, as illustrated in fig. 3.25, the swing can be reduced by adding an optimized t_{FE} to a MOSFET. In addition, by increasing the Av (changing the intrinsic MOSFET with SSRW or QW design), NCFET can achieve a lower swing state and consumes less energy because the V_{DD} is reduced while ΔQ remains the same for the same drive current (assuming mobilities remains the same). As we continue reducing the SS of the NCFET by using even thinner Tsi, secondary effects such as mobilities degradation or current crowding at the S/D junction increase the ΔQ for the same drive current, resulting in a net increase of switching energy.

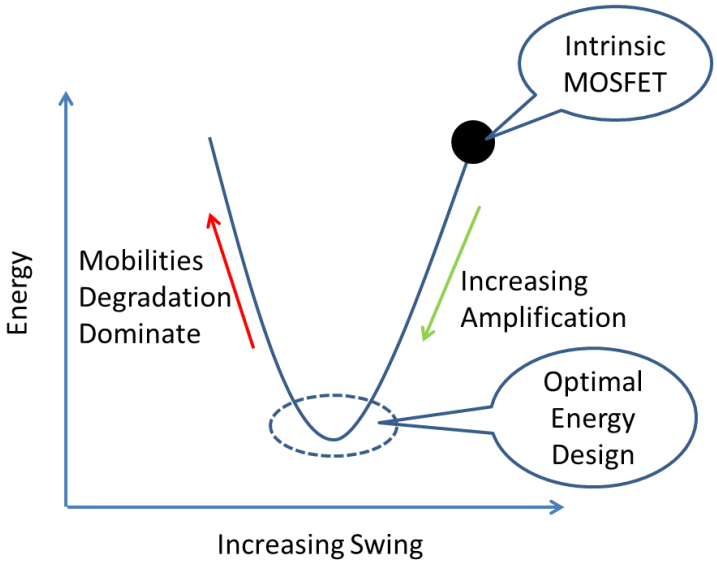

Figure 3.25. Energy vs swing.

We can approximate the delay by ΔQ/Ion. Adding an optimized t_{FE} to the intrinsic MOSFET should have the same delay as long as the intrinsic FE switching time is smaller than the inverse of the operation frequency. Adding FE does not change the charge required for the same I_{ON}, therefore, the delay should be the same. As we scale the C_{DEP} (by SSRW or QW design) to achieve a better swing, the charge required should remain the same for the same I_{ON} until the swing becomes very small (very large Cdep due to very thin Tsi) and mobilities start degrading. At this point, more charge is need for the same I_{ON}, so the delay will increase.

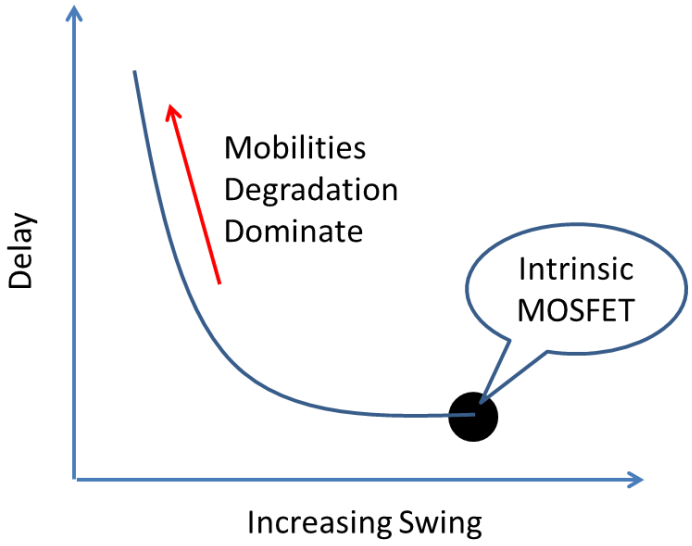

Figure 3.26. Delay vs Swing for NCFET.

Therefore, combining fig. 3.25 and 3.26, NCFET should be able to achieve a better energy-delay frontier.

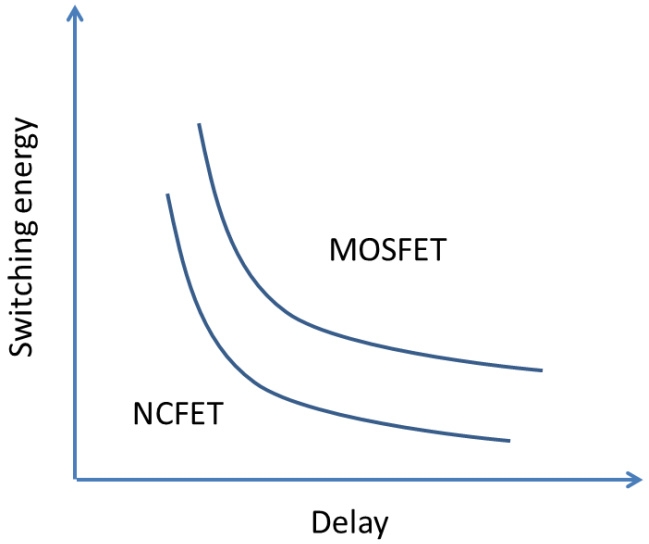

Figure 3.27. Switching energy vs delay for MOSFET and NCFET

Fig. 3.28 shows the simulated switching energy for a particular NCFET design and the ITRS projected switching energy for 2016 ETSOI and 2024 FinFET.

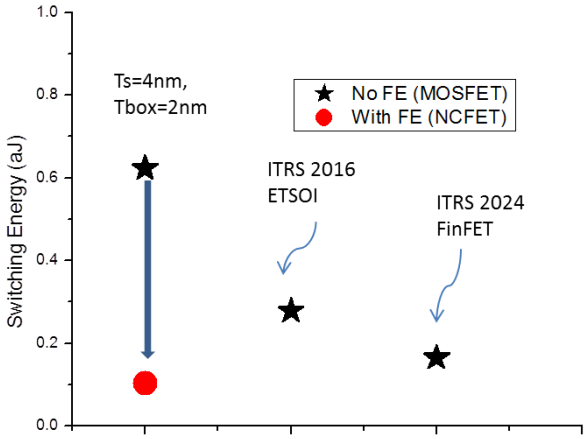

Figure 2.28. Simulated switching energy and ITRS roadmap for ETSOI and FinFET.

2.6 References

[3.1] S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” Nano Lett., vol. 8, no. 2, pp. 405–410, 2008.

[3.2] Khan, Asif Islam, et al. "Experimental evidence of ferroelectric negative capacitance in nanoscale heterostructures." Applied Physics Letters 99.11 (2011): 113501.

[3.3] McKee, R. A., F. J. Walker, and M. F. Chisholm. "Crystalline oxides on silicon: the first five monolayers." Physical Review Letters 81.14 (1998): 3014.

[3.4] Rusu, Alexandru, et al. "Metal-ferroelectric-meta-oxide-semiconductor field effect transistor with sub-60mV/decade subthreshold swing and internal voltage amplification." Electron Devices Meeting (IEDM), 2010 IEEE International. IEEE, 2010.

[3.5] C. Hu, Modern Semiconductor Devices, p.272, Pearson Pub. (2010)

[3.6] C. Hu et al., Intern'l Symp. on VLSI Tech., Systems and Applications, VLSI-TSA, p. 14-15, 2008.

[3.7] Chun Wing Yeung, Padilla, A., Tsu-Jae King Liu, Chenming Hu, "Programming characteristics of the steep turn-on/off feedback FET (FBFET)," VLSI Technology, 2009 Symposium on , vol., no., pp.176-177, 16-18 June 2009.

[3.8] Khan, A.I., Yeung, C.W., Chenming Hu, Salahuddin, S., "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," Electron Devices Meeting (IEDM), 2011 IEEE International , vol., no., pp.11.3.1-11.3.4, 5-7 Dec. 2011.

[3.9] C. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu, "A Comparative study of advanced MOSFET concepts", IEEE Trans. Electron Devices, vol. 43, pp.1742 1996.

[3.10] Fujita, K., Torii, Y., Hori, M., Oh, J., Shifren, L., Ranade, P., Nakagawa, M., Okabe, K., Miyake, T., Ohkoshi, K., Kuramae, M., Mori, T., Tsuruta, T., Thompson, S., Ema, T., , "Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications," Electron Devices Meeting (IEDM), 2011 IEEE International , vol., no., pp.32.3.1-32.3.4, 5-7 Dec. 2011.

[3.11] Boscke, T.S., Muller, J., Brauhaus, D., Schroder, U., Bottger, U., "Ferroelectricity in hafnium oxide: CMOS compatible ferroelectric field effect transistors," Electron Devices Meeting (IEDM), 2011 IEEE International , vol., no., pp.24.5.1-24.5.4, 5-7 Dec. 2011

[3.12] Chenming Hu, "Thin-body FinFET as scalable low voltage transistor," VLSI Technology, Systems, and Applications (VLSI-TSA), 2012 International Symposium on , vol., no., pp.1,4, 23-25 April 2012

[3.13] Choi, Yang-Kyu, et al. "Nanoscale ultrathin body PMOSFETs with raised selective germanium source/drain." Electron Device Letters, IEEE 22.9 (2001): 447-448.

[3.14] Yoon, Youngki, Kartik Ganapathi, and Sayeef Salahuddin. "How good can monolayer MoS2 transistors be?." Nano letters 11.9 (2011): 3768-3773.

[3.15] Fang, Hui, et al. "High-performance single layered WSe2 p-FETs with chemically doped contacts." Nano letters 12.7 (2012): 3788-3792.

[3.16] Salahuddin, Sayeef, and Supriyo Datta. "Use of negative capacitance to provide voltage amplification for low power nanoscale devices." Nano letters 8.2 (2008): 405-410.

[3.17] Khan, Asif I., et al. "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation." Electron Devices Meeting (IEDM), 2011 IEEE International. IEEE, 2011.

[3.18] Yeung, Chun Wing, et al. "Non-Hysteretic Negative Capacitance FET with Sub-30mV/dec Swing over 106X Current Range and ION of 0.3 mA/μm without Strain Enhancement at 0.3 V VDD." Simulation of Semiconductor Processes and Devices (SISPAD), 2012 International Conference on. 2012.

Chapter 4: Fabrication of pNCFET

Fabrication of NCFET is not a simple task because there must be several requirements satisfied simultaneously in order to "see" the sub-60 swing benefit:

1. Introducing single-crystal ferroelectric in the gate stack

    a. Single-crystal, defect free ferroelectric

        Integrating single-crystal ferroelectric on Si MOSFET is one of the most critical challenges in the integration scheme. First, single-crystal, defect free ferroelectric (assuming no leakage) should theoretically exhibit a sharp intrinsic switching between the two polarization states. Any extrinsic switching caused by defects or grain boundary will lead to less uniform switching [4.1] and could reduce or negate the negative capacitance benefit.

    b. Choice of buffer layer

        Buffer layer between the Si and Ferroelectric is an important subject in the integration scheme.

        i. Lattice mismatch: Since there is lattice mismatch between Si and most ferroelectrics, buffer layer is needed to ensure single crystal ferroelectric can be grown with low defectivity. [4.2]
        ii. Band offset: Ideally, the buffer layer should have good band offset for both electron and holes for N and P FET. [4.3]
        iii. Dielectric constant: high-k dielectric is preferable in the buffer layer for scaling and leakage issue similar to the reason why high-k dielectric is used in the MOSFETs in the last few technology nodes.
        iv. Diffusion barrier: a good buffer layer will also act as a good diffusion barrier preventing the inter-diffusion of elements between the ferroelectric and Si.
        v. Good interface quality between the buffer /Si and buffer/Ferroelectrics: Good interface is also one of the most important criteria in the buffer selection for NCFET. Without good interface, any SS benefit from negative capacitance might be affected by the interface.

    c. Ferroelectric deposition thickness control: As seen in the simulation section, a process that gives precise thickness control (lead to $|C_{FE}|$ control) is very critical in designing NCFET.

d. Thermal budget compatibility: Source/Drain activation in Silicon requires ~ $1000^{O}C$ for dopant activation. The high thermal may impact the ferroelectric gate stack which is grown at a lower temperature.
e. Defect annealing (ambient gas): Forming gas annealing is common processes used in fabrication to improve the quality of the semiconductor/dielectric interface after device fabrication. However, forming gas is a reducing agent which will have adverse effect on the ferroelectric. Meanwhile oxygen annealing will improve the quality of ferroelectric but affect the semiconductor/dielectric interface.

4.1 Fabrication Proposal:

After evaluating all the requirements and options we have, we decide to choose a gate last non-self aligned process using $SrTiO_3$ (STO) as the buffer for p-type devices [4.4], and $Pb(Zr_XTi_{1-X})O_3$ (PZT) as the ferroelectric, and integrating on SOI substrate for NCFET fabrication.

In our process, the S/D doping and activation is done before the deposition of the gate stack. Therefore, the process is not self aligned. The rationale of using this process is because the integrity of the gate stack is of the highest importance in this project, so all the high thermal budget steps must be done before the gate stack is formed to minimize the damage. Also, the S/D doping is intentionally chosen to be lower than 1E20/cm^3 to reduce the damage to the Si surface for better epitaxial growth of STO and PZT.

Starting substrate is 6" SOI wafer from Soitec. After the SOI is thinned down to the desirable thickness by cycles of dry thermal oxidation and diluted hydrofluoric acid (DHF) etching, mesa (active area) is defined by patterning followed by dry etching (an alternate process, "mesa last" which turns out to give lowest leakage is to perform mesa isolation last after ferroelectric deposition). Next, a sacrificial thermal oxide of ~3nm is grown to remove the defects caused by the dry etching step. After the sacrificial thermal oxide is removed by DHF, the wafer is immediately loaded (<15 minute queue time) into a furnace to ensure a good quality gate thermal oxide is grown. The wafer is then patterned, followed by source/drain ion implantation, and rapid thermal annealing (RTA) was used to activate the dopants.

[After the photoresist is removed, a control MOSFET is made by depositing the metal gate electrode by lift-off process. (For wafers without mesa definition, the control will need the following steps: mesa definition, sacrificial oxide and removal, thermal oxide, and metal gate deposition) The physical metal gate length is longer than the S/D implant distance to ensure sufficient S/D overlap with a non-self aligned scheme.]

The wafer is then cut into 3" wafer by American Precision Dicing. Then blanket STO buffer is deposited on the patterned wafer by molecular beam epitaxy (MBE). In-situ removal of native oxide is done in the same MBE chamber prior to the STO deposition. And then the wafer is further cut into 10mmx10mm dies, and another blanket layer of epitaxial PLD PZT ferroelectric

is deposited (mesa isolation followed by spacer deposition is need if it was not done at the beginning). Then the gate metal is deposited by ebeam deposition and the source/drain contact is etched by a combination of dry and wet etch processes.

This project includes designing and simulating the structures, creating new mask sets, fabricating SOI MOSFETs, collaborating with colleagues for PZT and STO deposition, and device characterization.

Fig 4.1. shows the project timeline of NCFET fabrication in the third trial, and fig 4.2 shows the simplified process flow of the fabrication mesa last step. Fig 4.3 shows the layout of a die.

ID	Task Name	Start	Finish	Duration
1	Mask Making	3/25/2013	4/3/2013	8d
2	SOI Thinning	3/26/2013	3/28/2013	3d
3	Alignment Mark Definition	4/4/2013	4/8/2013	3d
4	S/D Litho	4/9/2013	4/15/2013	5d
5	S/D Ion Implantatiom	4/16/2013	4/24/2013	7d
6	S/D Activation	4/29/2013	4/29/2013	1d
7	Active Definition	4/29/2013	4/30/2013	2d
8	Gate Oxidation	4/30/2013	5/1/2013	2d
9	Gate Electrode Deposition	5/2/2013	5/3/2013	2d
10	Control MOSFET Finished	5/6/2013	5/6/2013	0d
11	Characterization	5/6/2013	5/31/2013	20d
12	STO Deposition	4/25/2013	5/8/2013	10d
13	FE Deposition	5/14/2013	5/22/2013	7d
14	Ion Milling	5/23/2013	5/29/2013	5d
15	Oxygen Annealing	5/29/2013	6/4/2013	5d
16	Spacer Deposition	6/5/2013	6/13/2013	7d
17	Gate Electrode Deposition	6/14/2013	6/17/2013	2d
18	S/D Contact	6/18/2013	6/20/2013	3d
19	Characterization	6/21/2013	7/4/2013	10d

Figure 4.1. Project timeline of the third trial of the NCFET fabrication.

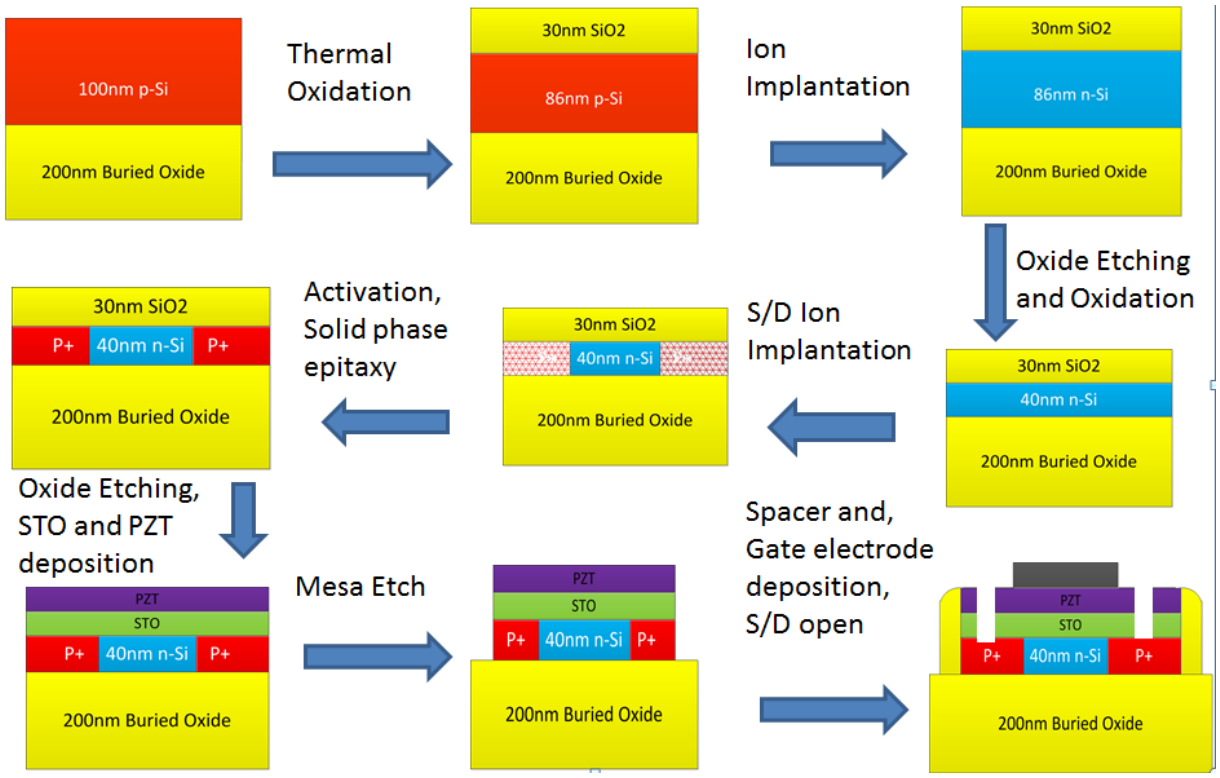

Figure 4.2. Process flow of NCFET fabrication.

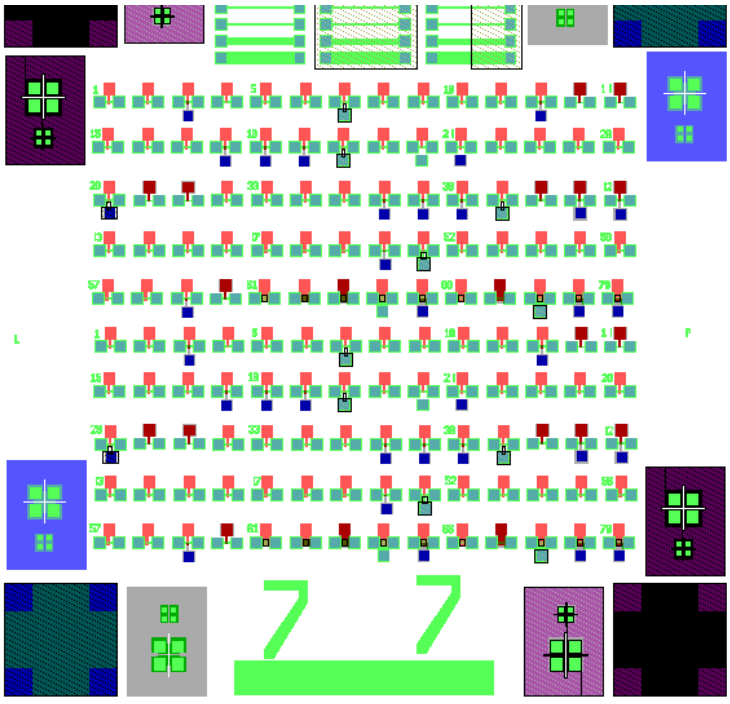

Figure 4.4. Layout of a die.

4.2 Blanket STO and PZT Deposition and Characterization

[The material in this section is provided by Asif Khan and Claudy Serro]

SrTiO3 is typically used as a template to integrate epitaxial single crystal perovskite oxide thin films on silicon.[4.4] An ~8 nm STO was grown on Si (100) substrate using molecular beam epitaxy by R. Droopad group. [4.5] A general outline of the STO growth process is as follows. .A Sr-assisted catalyst thermal desorption procedure was used to remove the native SiO2 on the surface prior to the epitaxial growth.[4.6] At the end of this oxide removal procedure, reflection high-energy electron diffraction (RHEED) exhibits bright and clear 2 x 2 patterns from the Si (100) substrate, indicating that the surface oxide was completely desorbed and the surface was clear of any native amorphous SiO2.[4.7] Source materials are contained in conventional effusion cells and oxygen introduced into the growth environment through a leak valve controlled RF plasma source. The epitaxial oxide growth on silicon is achieved using a co-deposition process in which both the alkaline earth metal (Sr) and the transition element (Ti) shutters are opened in a controlled oxygen environment. [4.5] Fig. 4.5 shows the AFM topography of STO/Si structure. The RSM roughness of the films is ~1.63 A.

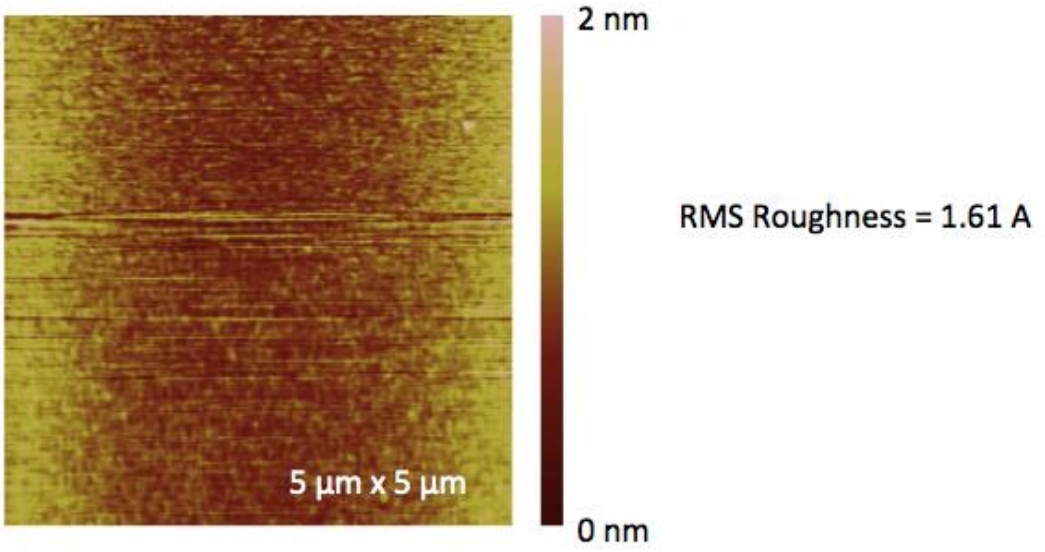

Fig. 4.5. AFM topography of STO/Si structure.

Once the STO layer is grown, the PZT layer is ex-situ deposition using the pulsed laser deposition (PLD) technique. The PZT layer was grown at 720 ^{0}C. During the growth, the oxygen partial pressure was kept at 100 mTorr, and afterwards, the heterostructures were slowly cooled down at a rate of - 5 _C/min to the room temperature at 1 atm partial pressure of oxygen. Laser

pulses with 100 mJ energy and ~4 mm^2 spot size were used to ablate the targets. Fig. 4.6 shows the AFM topographys of PZT(60nm)STO(8nm)/Si structure. The RSM roughness of the films is ~2 A.

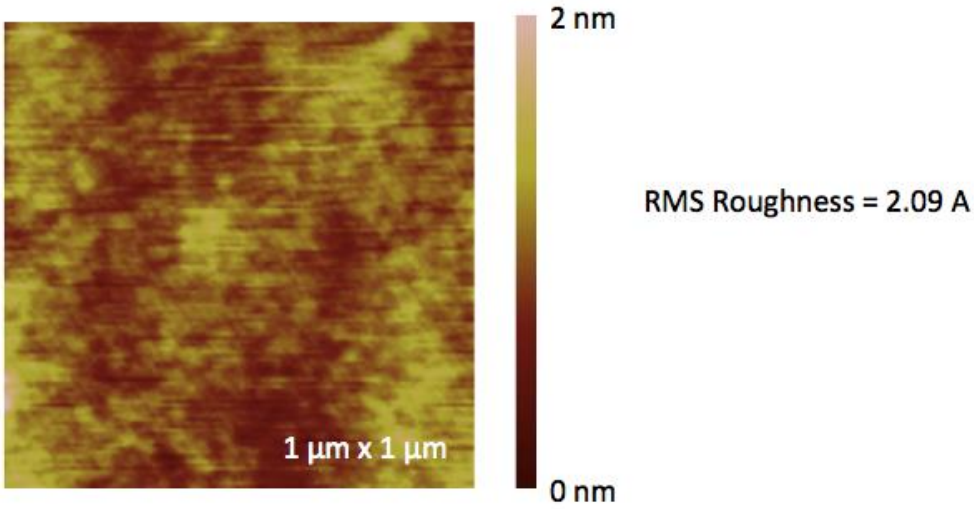

Figure 4.6. AFM topographys of PZT(60nm)STO(8nm)/Si structure

Fig. 4.7 shows the piezo-response force microscopy image of a 1 □m x 1□ □m region on the surface of the sample. A 500 nm x 500 nm region at the center is polled at -8 V. Clear change of phase is observed pointing to the fact that the ferroelectric polarization can be switching by applying a voltage via a scanning probe.

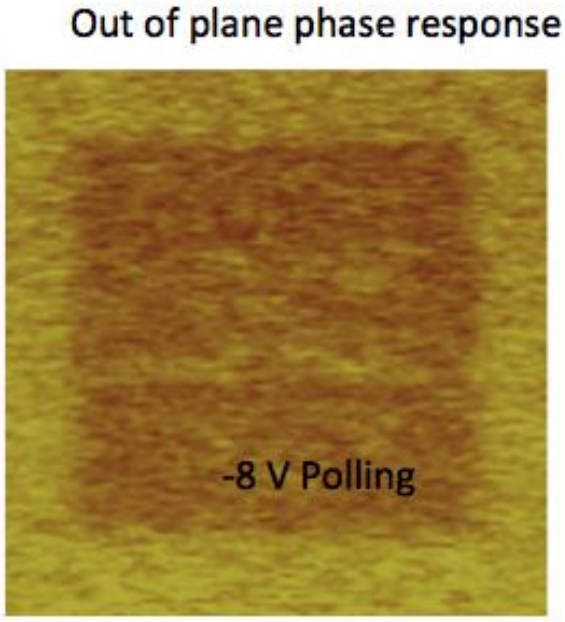

Figure 4.7 Piezo-response force microscopy image of a 1 □m x 1□□m region on the surface of the sample.

Fig. 4.8 shows the piezo-phase response of the sample as function of the applied voltage. Clear change of the phase by 180^0 at ±1 V further confirms the switchable ferroelectricity in the sample.

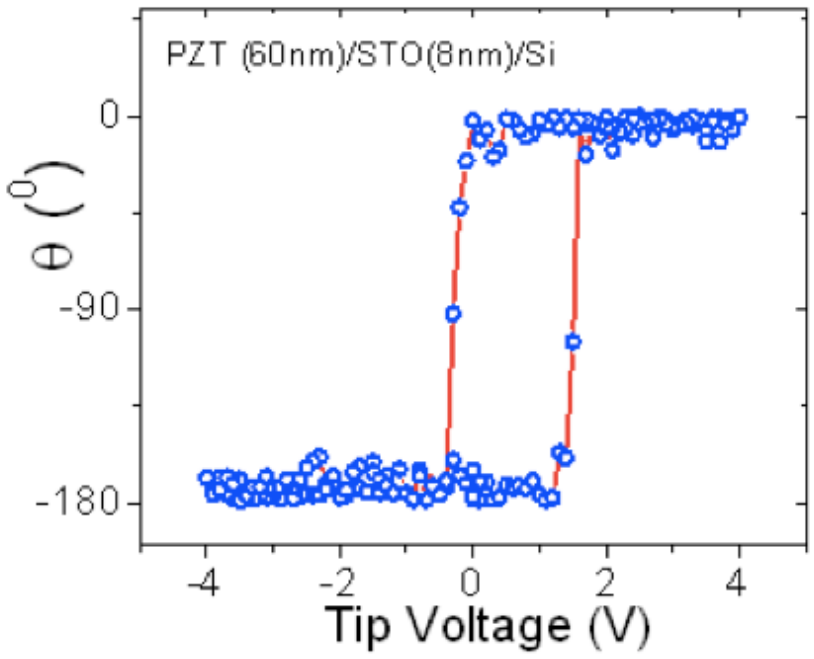

Fig 4.8 Piezo-phase response of the sample as function of the applied voltage.

Fig. 4.9 shows the X-ray diffraction spectrum of the PZT (60 nm)/STO (8 nm)/Si(100) sample. Clear (002) reflections from the PZT and STO layers are observed. The PZT c-axis parameters is calculated to 4.084 A from the spectrum. Fig. 6 shows the rocking curve measurements around the PZT and STO (002) peaks. The full-width-at-half-maximum for PZT and STO are both found to be ~0.4^0.

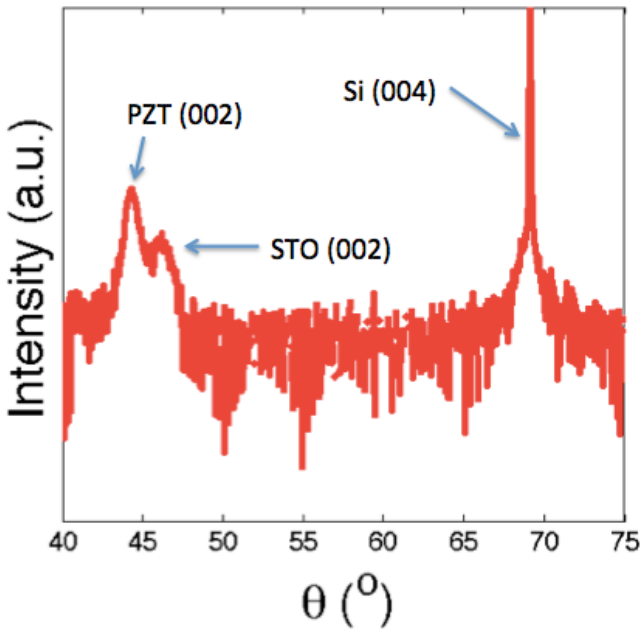

Figure 4.9. X-ray diffraction θ–2θ spectrum of the PZT (60 nm)/STO (8 nm)/Si(100) sample.

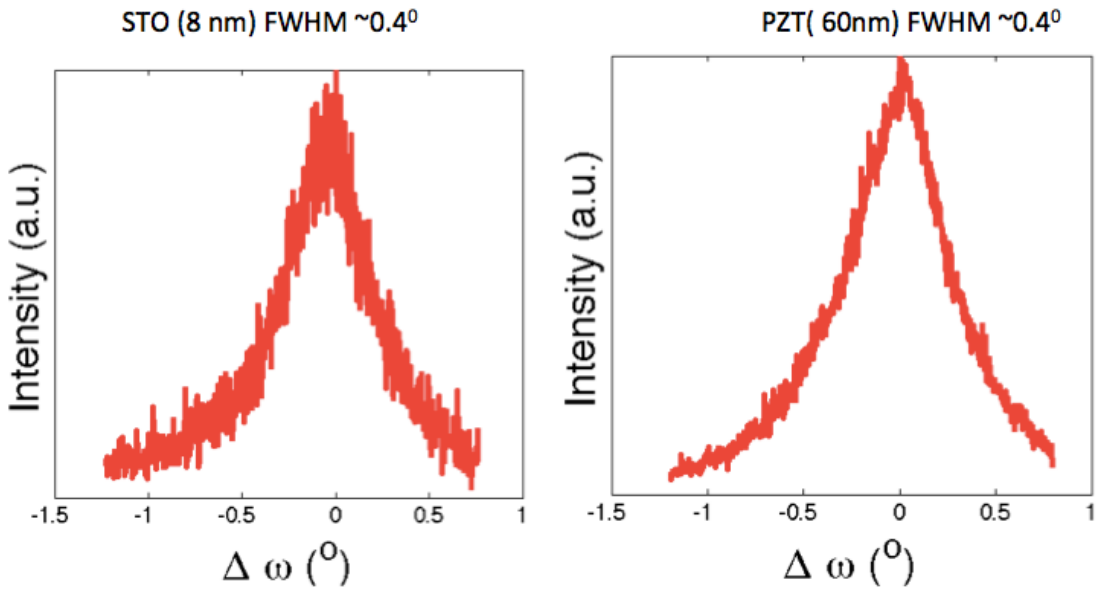

Figure 4.10. Rocking curve measurements around the PZT and STO (002) peaks.

Fig. 4.11 shows the reciprocal space map around the PZT (103), STO (103) and Si (115) reflections.

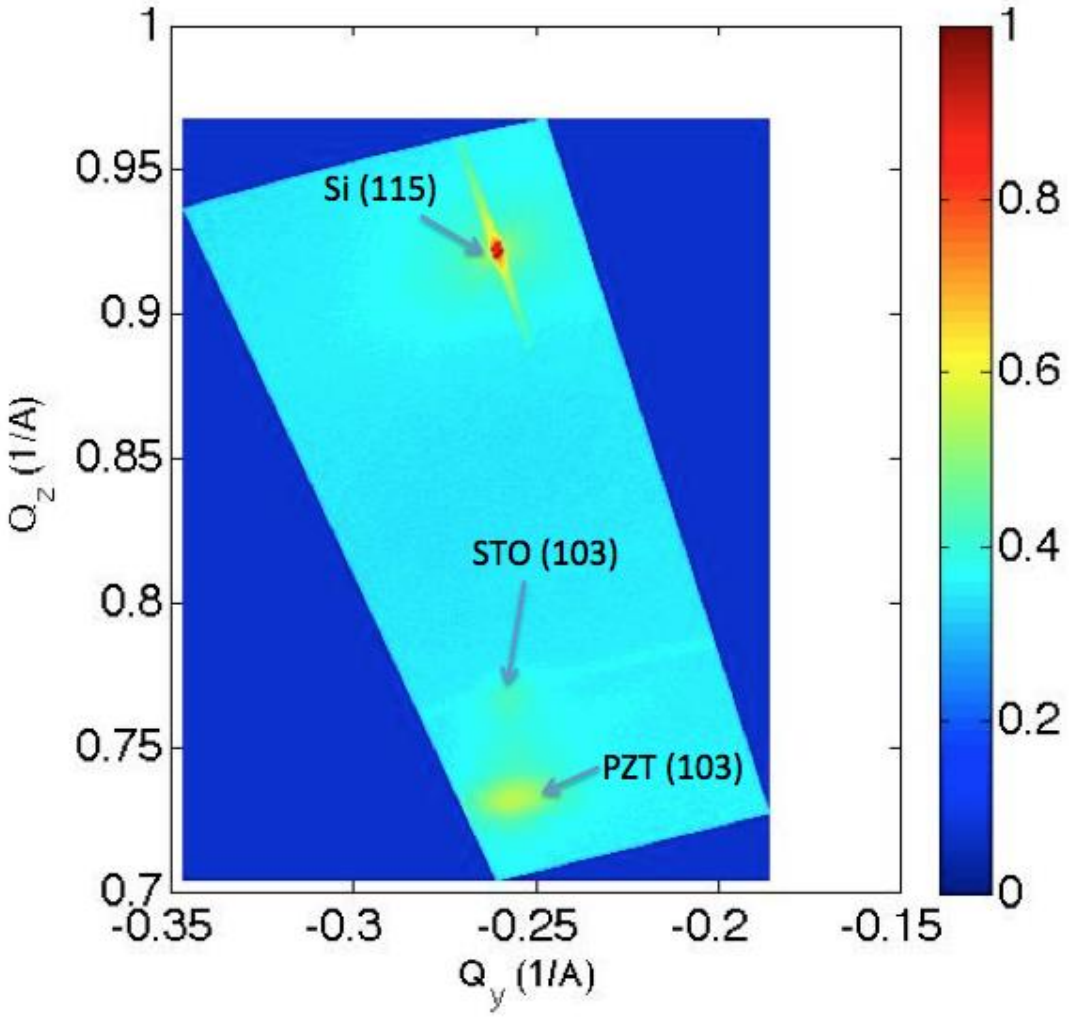

Figure 4.11. The reciprocal space map around the PZT (103), STO (103) and Si (115) reflections

4.3. Lift-off Patterning for Spacer Deposition

After blanket STO and PZT films are deposited, Au electrode is deposited as the gate electrode. However, since the deposition of both STO and PZT are not conformal, the sidewall of the channel region is not covered by the dielectric or ferroelectric. It will create a gate to channel direct leakage path when the gate metal is deposited as shown in fig 4.12 (b).

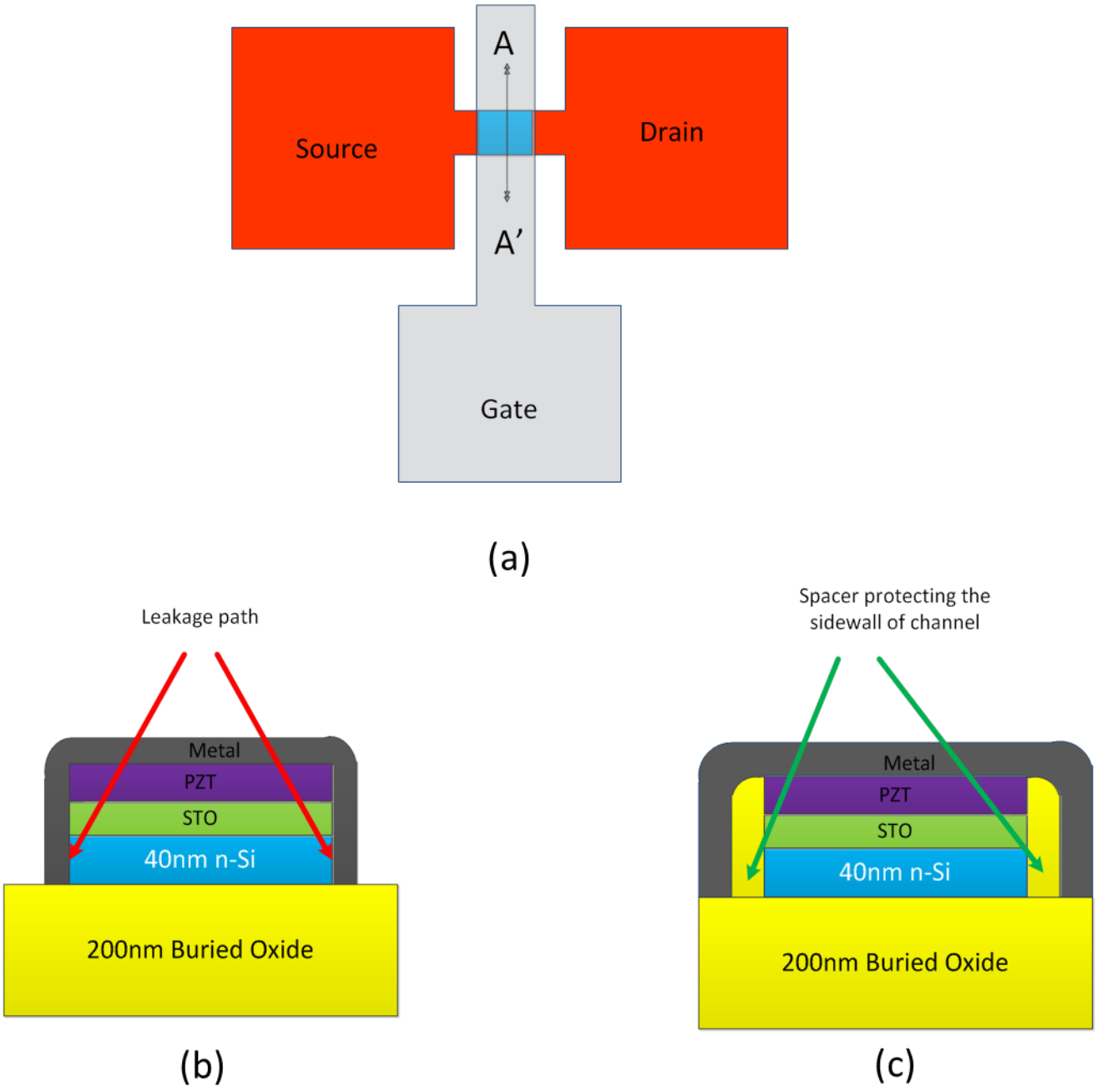

Figure 4.12. (a) Top-down of the device. A-A' indicates the cross-section of (b) and (c). (b) Possible leakage path from gate to channel. (c) Spacer protecting sidewall of the channel.

Conventional spacer process can be used to protect the sidewall as shown in 4.12(c); however, the process requires a conformal deposition of dielectric film followed by an anisotropic etch. The anisotropic etch will damage the top PZT surface and impact the device.

An alternative spacer formation method is used to solve this problem as shown in fig 4.13 (process provided by Dr. Long You). After STO and PZT is deposition, photoresist is used as the mask to etch the mesa area. Ionmilling is used to define the mesa region (device area). The photoresist is intentionally not removed, and a conformal MgO dielectric film (~75nm) is deposited by spluttering. Then the sample is soaked in an acetone bath for 24 hours. (fig). The top potion of the MgO is lifted off along with the photoresist, leaving behind the MgO on the sidewall as spacer. The resultant structure is MgO spacer covering the sidewall of the mesa without any etching steps that might potentially damage the top PZT surface.

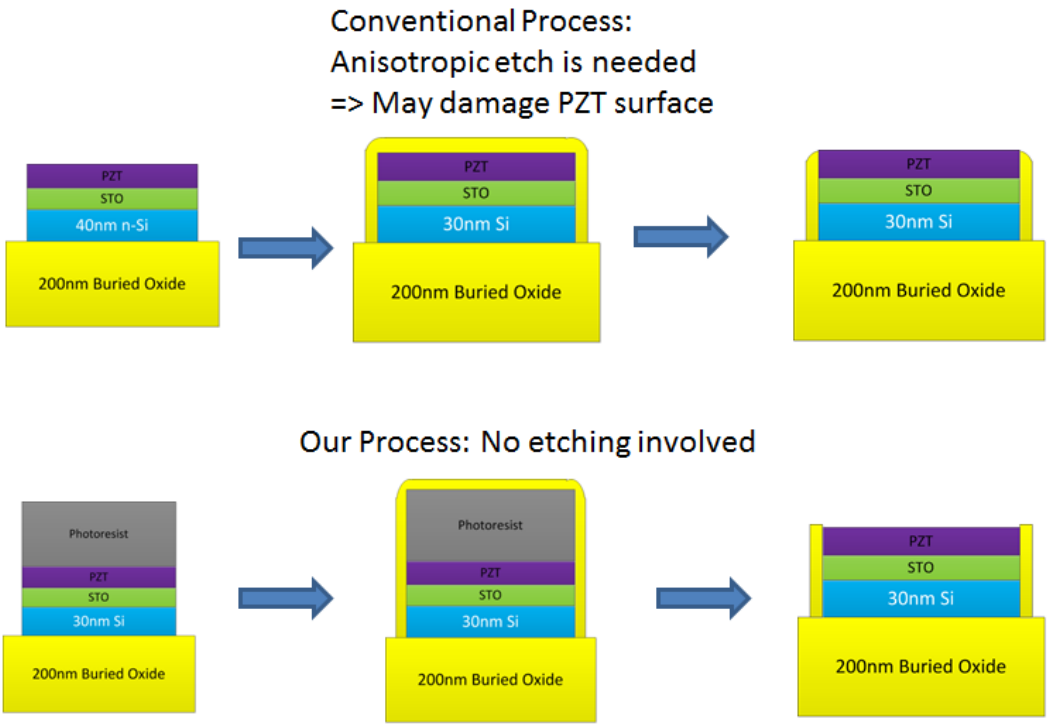

Figure 4.13. Conventional spacer process vs non etch spacer process.

4.4 Selective etching of PZT and STO for S/D contact

After gate electrode is deposited using lift-off process, the last step is to open the S/D contact area.

The most common method used for etching PZT and STO is by ionmilling, a physical bombardment of ions to remove the top material. However, this process is not selective and may cause damages to the Si surface. This method can be used for contact opening when the Tsi

thickness is larger than 80nm. In these thinner body thickness samples, where the Tsi is ~40nm or less, a highly selective etching process is needed.

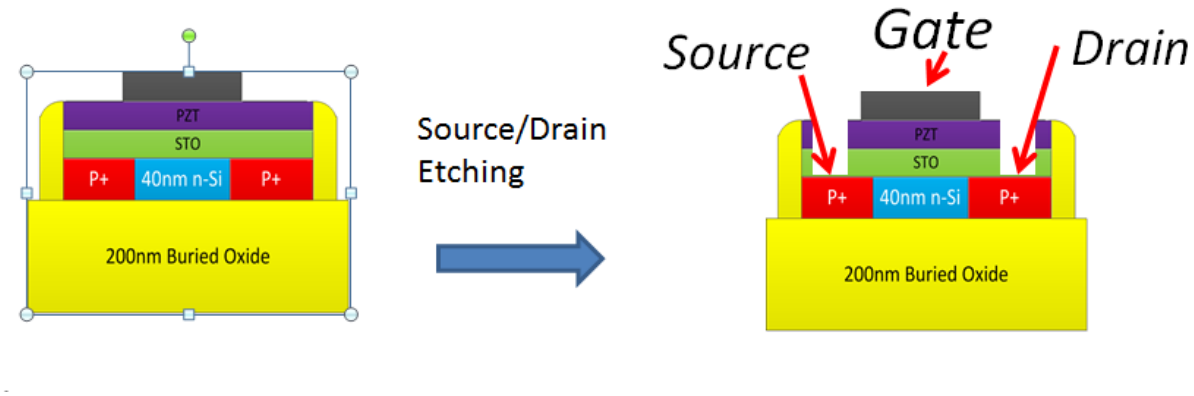

Figure 4.14. Source/Drain contact opening.

In our experiment, a combination of nonselective dry etch and selective wet etch processes is used for opening the S/D contact. The idea is to use a non-selective dry process to etch the top layer PZT and part of the STO, and then use a selective wet etch to clear the STO and leaving a pristine Si S/D surface for contact.

The first dry etch rely on the real time secondary-ion mass spectrometry (SIMS) feedback capability of the ionmilling equipment. The Strontium signal is used as the indicator of when the STO is being etched. After Strontium signal peaks, the etching is stopped manually. Fig. 4.15 shows the SIMS profile of a sample used for calibration. Each ionmilling duration is ~5min followed by a 3 minute break to allow the sample to cool down to prevent photoresist from reflowing.

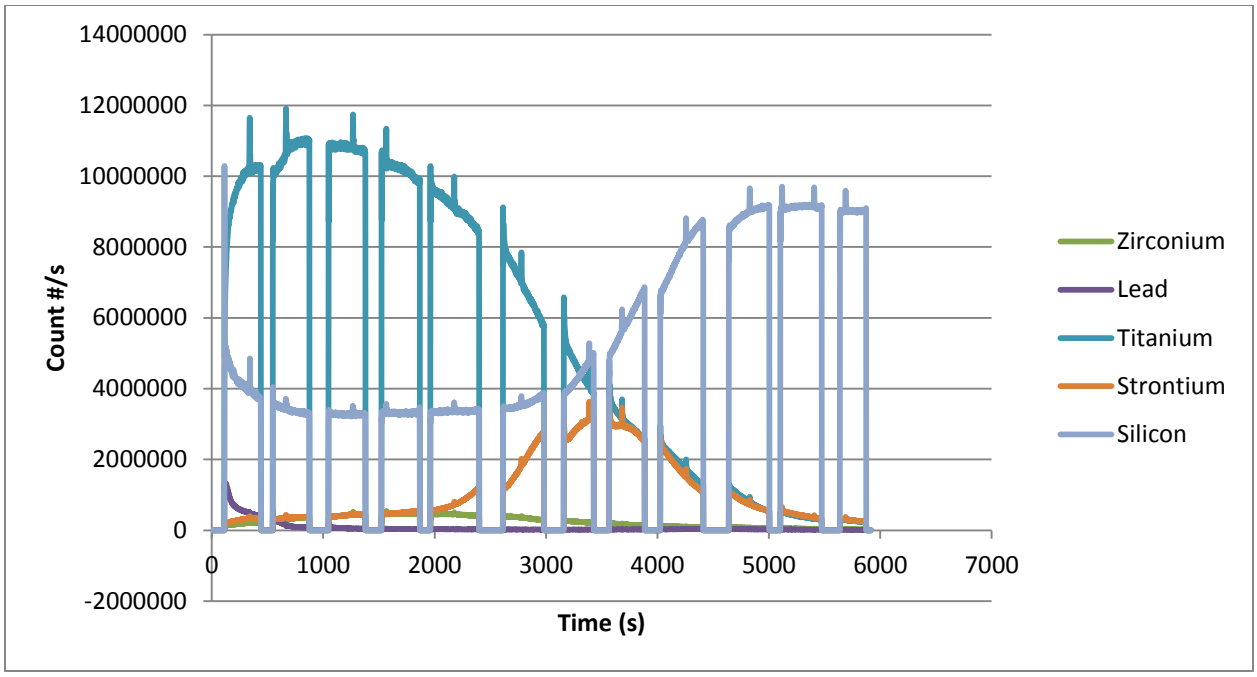

Figure 4.15. SIMS profile.

After the sample finished ionmilling, it was rinsed in DI water for 2 minutes (intentionally leaving the photoresist).

Without removing the photoresist, the same photoresist is used as the mask for the 8 minutes BHF (4.3pH) wet etch to remove the remaining STO on the Si surface. 10 minute DI water rinse is followed to clean the sample. The pH of 4.3 is crucial [4.8] as too high pH will result in flake-like residue remaining (fig 4.15(a)). Too low of pH will erode the photoresist and exposed the Au electrode or etched into the gate dielectric. Fig 4.15(b) picture shows a clean surface of Si after PZT and STO is removed.

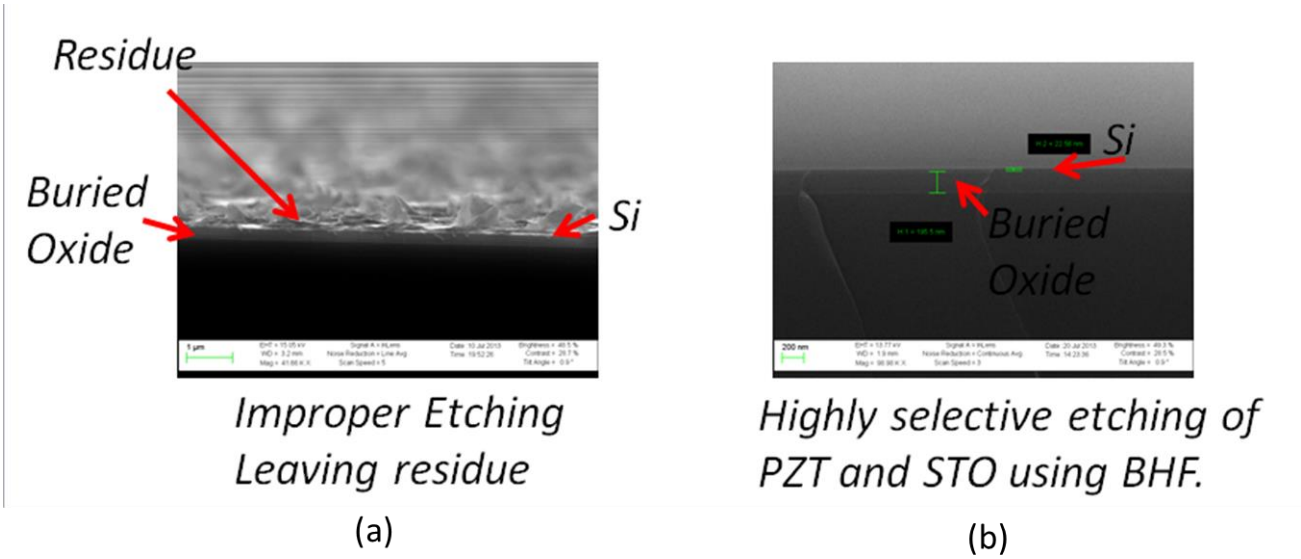

Figure 4.15. (a) Improper etching of STO leaving residue on surface. (b) Clean Si surface after wet etching.

After the sample finished etching, it was put into an Acetone bath for at least 24 hours, and then a 2 minute isopropyl alcohol (IPA) rinse, finished with a 10 minute DI water clean to complete the clean. The long ionmilling etch will hardened the photoresist, so a longer acetone bath is necessary to remove the photoresist residue completely.

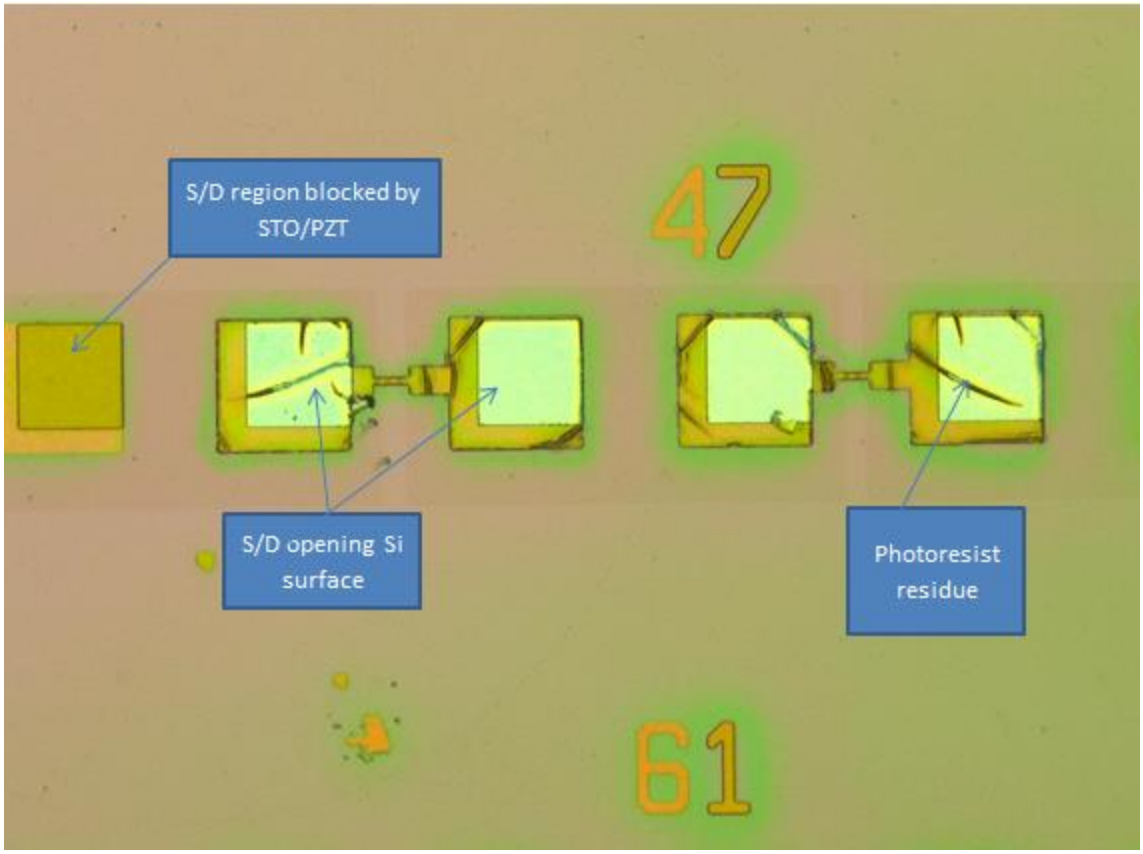

Figure 4.16. Sample after S/D opening (no gate electrode in this sample).

4.5 Device characterization.

The final p-type NCFET is fabricated, and the schematic is shown in fig. 4.17.

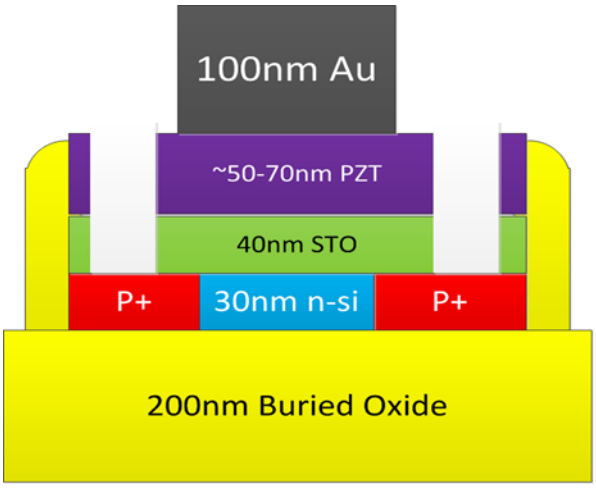

Figure 4.17. Schematic of fabricated pNCFET structure.

The finished device is characterized using Agilent B1500A. The Ion/Ioff ratio is ~1000x with SS of ~100mV/dec at room temperature without any annealing. An attempt had been made to measure transfer curves at different temperature, but the measurement did not yield result probably due to the ~100nm Au gate contact pad was too fragile and was slightly damaged during the first room temperature measurement, and then further eroded by the harder probe tips during the variable temperature measurements.

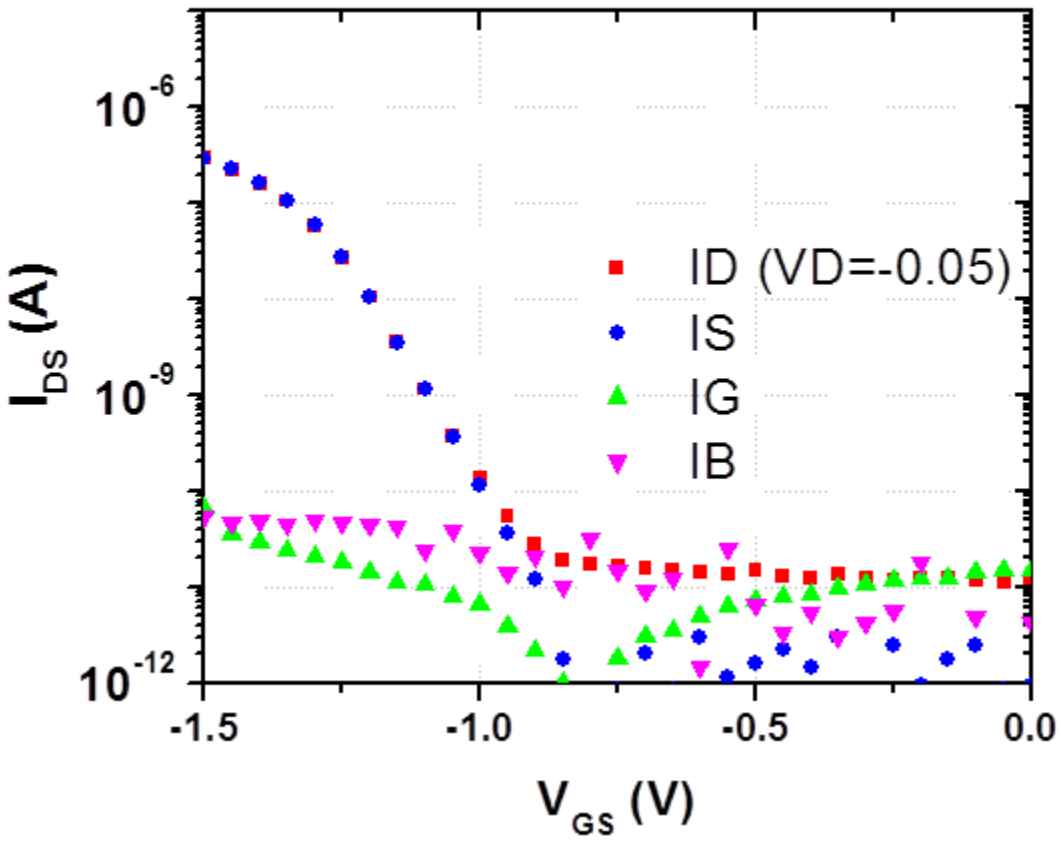

Figure 4.18. I_D-V_G of pNCFET.

Fig. 4.19 shows the pNCFET and control pMOSFET transfer curves. For the control MOSFET, forming gas anneals help improving the swing, reducing gate leakage, and possibly removing fixed charges (as indicated by the Vt shift). The subthreshold swing has improved from 120mV/decade to ~65mV/decade.

For pNCFET, the swing is ~100mV/decade as fabricated with very low gate leakage (several devices yielded). Unfortunately, after attempting different temperature IV measurements, the thin gate contact pad (~100nm Au) was damaged and was not able to measure or conduct further annealing experiment.

Therefore, there is insufficient evidence to evaluate whether there is negative capacitance effect or not. This experiment, however, has demonstrated a fabrication flow to integrate epitaxial STO and PZT on silicon channel with reasonable swing and low leakage.

Future experiment design should include deposition of different thickness of ferroelectric and compare the swing as a function of ferroelectric thickness at different temperatures.

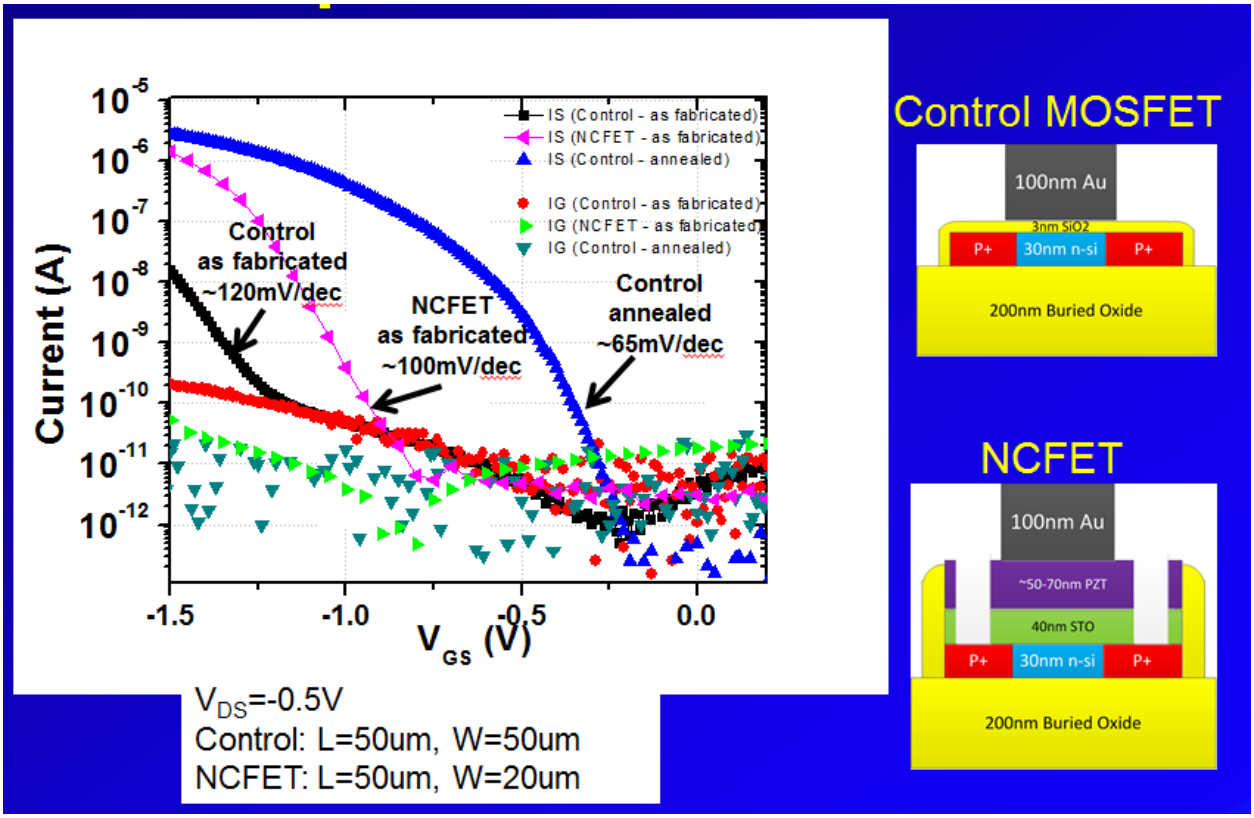

Figure 4.19. Transfer characteristics of pNCFET and control MOSFET.

4.6 NCFET Process Flow

Step	Process Name	Process Specification	Equipment
0.01	Wafers	6 inch prime SOI wafers and test wafers	Soitec
0.02	Labelling	number the wafers	
0.03	Si(SOI) Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv
0.04	Preclean	piranha, 120C, 10min / 25:1 HF 1min	sink6
1.00	**SOI Thinning**		
1.01	Preclean	piranha, 120C, 10min / 25:1 HF 1min	sink6
1.02	Dry Oxidation	Recipe: 2DRYOXA, 950C, O2 4000sccm, oxidation 330min, post anneal 20min	tystar2
1.03	Oxide Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
1.04	Oxide Removal	10:1 HF, 4min, 1100A target removal oxide thickness	sink6
1.05	Oxide Thickness Measurement	Recipe: 7. Thin Oxide on Silicon	nanoduv
1.06	Si(SOI) Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv
1.07	Dry Oxidation	Recipe: 2DRYOXA, 900C, O2 4000sccm, oxidation 150min, post anneal 20min	tystar2
1.08	Oxide Thickness Measurement	Recipe: 1. Oxide on Silicon, record in A	nanoduv
1.09	Oxide Removal	10:1 HF, 4min, 350A target removal oxide thickness	sink6
1.10	Oxide Thickness Measurement	Recipe: 7. Thin Oxide on Silicon	nanoduv
1.11	Si(SOI) Thickness Measurement	Recipe: 4. Polysilicon on Oxide, record in A	nanoduv
		Target SOI thickness 400A	
2.00	**Alignment Mark(PM) Definition**		
2.01	Preclean	piranha, 120C, 10min / 25:1 HF 1min	sink6
2.02	Alignment Mark Lithography	HMDS, 60s	sink1
		i-Line photoresist	Headway 1/2
		PR Coating: Program 1, target 1.2um thick	
	Prebake	110 degree, 60 seconds	Hot Plate
		60s cool down	Chill plate
		Exposure Time 20s (depending on intensity condition)	KS Aligner
2.03	Post development clean	DI water 5min	Beaker
2.04	Inspection	Microscope - inspection	uvscope
	Hard Bake	100 degree, 15 minutes	Hot Plate
2.05	Inspection	Microscope - inspection	uvscope
2.06	Alignment Mark(PM) Etch	Recipe: 5003_POLY_OB_ME_OE	lam5
		OB: 13mT, TCP RF 200W, bias RF 40W, CF4 100sccm, 5sec	
		ME: 12mT, TCP RF 300W, bias RF 150W, Cl2 50sccm, HBR 150sccm, 15sec	

		OE: 80mT, TCP RF 200W, bias RF 150W, HBR 100sccm, O2 1sccm, He/Ar 100 sccm, 0sec	
2.07	PR Ashing	Recipe: std - 3.75T, 400W, 200C, MFC1 40% O2, 2min 30sec	matrix
2.08	Post Cleaning	piranha, 120C, 10min	sink8
	Alignment Mark Inspection	Check PM mark step height: Target 1200A	Asiq
3.00	**Gate Oxide Deposition**		
3.01	Preclean	piranha, 120C, 10min / 25:1 HF 10sec	sink6
3.02	Sacrificial Oxidation (Dry)	Recipe: 2DRYOXA - dry O2, 850C, 1min, post N2 anneal 950C 20min	tystar2
3.03	Oxide Thickness Measurement	record in A	sopra
3.04	Oxide Removal	25:1 HF, 20sec	sink6
3.05	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	sink6
3.06	Gate Oxidation	Recipe: 1GATEOXA - dry O2, 850C, 1min, post N2 anneal 950C 20min	tystar1
3.07	Oxide Thickness Measurement	record in A	sopra
3.08	Post Cleaning	Piranha, 120C, 10min	sink8
4.00	**S/D Lithography**		
4.01	Preclean	ACE 5 min & IPA rinse 5 min	sink1
		110 degree, 60 seconds	Hot Plate
4.02	S/D Lithography	HMDS, 60s	sink1
		i-Line photoresist	Headway 1/2
		PR Coating: Program 1, target 1.2um thick	
		110 degree, 60 seconds	Hot Plate
		60s cool down	Chill plate
		Exposure Time 20s (depending on intensity condition)	KS Aligner
4.03	Post development clean	DI water 5min	Beaker
4.04	Inspection	Microscope - inspection	uvscope
	Hard Bake	100 degree, 15 minutes	Hot Plate
4.05	P+ S/D Implant	B(11)+, 1E15, 10keV, 7o tilt	Vendor
4.06	PR Ashing	Recipe: std - 3.75T, 400W, 200C, MFC1 40% O2, 2min 30sec	matrix
4.07	Post Cleaning	Piranha, 120C, 10min	sink8
5.00	**S/D Activation**		
5.01	Preclean	Piranha, 120C, 10min	sink6
5.02	Drain Activation Anneal	RTA, Recipe: - 1000C, 10sec, N2 45sccm	heatpulse4
5.03	Post clean	Piranha, 120C, 10min, DI water Rinse 4 cycles	sink6
6.00	**Cut into 3" wafer**		
6.01	Cut into 3" wafer	6" wafer cut into 3" with flat	vendor
6.02	PR Ashing	Recipe: std - 3.75T, 400W, 200C, MFC1 40% O2, 2min 30sec	matrix
6.03	Post Cleaning	Piranha, 120C, 10min	sink8
7.00	STO Deposition		

7.01	Preclean	piranha, 120C, 10min / 25:1 HF 20sec	sink8
7.02	STO deposition	MBE depsoition	Texas State Uni
7.03	Surface Roughness Measurement	AFM RMS measurement	AFM
8.00	Dicing		
8.01	Dicing	3" wfr is cut into 10x10mm dies	Diamond tip cutter
9.00	PZT Deposition		
9.01	Preclean	ACE 5 min & IPA rinse 5 min	sink
9.02	PZT deposition	PLD deposition	PLD
10.00	**Active Area Definition**		
10.01	Preclean	ACE 5 min & IPA rinse 5 min	sink1
		110 degree, 60 seconds	Hot Plate
10.02	Active Area Lithography	HMDS, 60s	sink1
		i-Line photoresist	Headway 1/2
		PR Coating: Program 1, target 1.2um thick	
		110 degree, 60 seconds	Hot Plate
		60s cool down	Chill plate
		Exposure Time 20s (depending on intensity condition)	KS Aligner
10.03	Post development clean	DI water 5min	sink
10.04	Inspection	Microscope - inspection	uvscope
	Hard Bake	100 degree, 15 minutes	Hot Plate
10.05	Active S/D Etch	Standard Recipe: 30 minutes	Ionmill
		Argon Flow: 7.1E-5, Magnet: 0.28A	
		High Voltage: 28V, Cathode: 20A, Voltage, 10V	
		Arc: Current 1.05A, Voltage 40V	
10.07	Post Cleaning	DI water 2minutes	sink8
10.08	Active S/D Height Measurement	Alpha Step - measure active height (on dummy sample)	asiq
11.00	Spacer Formation		
11.01	MgO deposition	70nm MgO deposition	Sputtering
11.02	Lift-off patterning	80 degree ACE 24 hours. 30 seconds ultrasonic.	sink
11.03	Post Clean	RT ACE 5 min & IPA rinse 5 min	sink
12.00	S/D Contact		
12.01	Preclean	ACE 5 min & IPA rinse 5 min	sink1
		110 degree, 60 seconds	Hot Plate
12.02	Contact Lithography	HMDS, 60s	sink1
		i-Line photoresist	Headway 1/2
		PR Coating: Program 1, target 1.2um thick	
12.03	Prebake	110 degree, 60 seconds	Hot Plate
		60s cool down	Chill plate

		Exposure Time 20s (depending on intensity condition)	KS Aligner
12.04	Post development clean	DI water 5min	sink
12.05	Inspection	Microscope - inspection	uvscope
12.06	Hard Bake	100 degree, 15 minutes	Hot Plate
12.07	S/D Dry Etch	Standard Recipe: 30 minutes	Ionmill
		Argon Flow: 7.1E-5, Magnet: 0.28A	
		High Voltage: 28V, Cathode: 20A, Voltage, 10V	
		Arc: Current 1.05A, Voltage 40V	
12.08	Post Clean	DI water 2 minutes	sink
12.09	Wet etch	49%DHF/DI water 1:1	sink18
		Add BHF (10:1) into DHF until pH 4.3 is reached	(Telfon beaker)
		Sample etch in ultrasonicated BHF for 8 minutes	
12.10	Resist Strip	80 degree ACE 24 hours. 30 s ultrasonic.	
12.11	Post Clean	IPA 2minutes, DI water 10 minutes	sink18
13.00	Gate electrode Deposition	(can be done before 12.00)	
13.01	Preclean	ACE 5 min & IPA rinse 5 min	sink1
		110 degree, 60 seconds	Hot Plate
13.02	Spin Coat	AZ 5214E negative resist	Headway 1/2
		500/5 and 4000/45 rpm/sec	
13.03	Reverse Expose	4s depends on light source @ CP mode	
13.04	Bake	120 degree, 45 seconds	
13.05	Flood Expose	20s depends on light source @ CP mode	
13.06	Develop	AZ 726 developer: 35s and DI water 30s	
13.07	Hard Bake	100 degree, 15 minutes	Hot Plate
13.08	eBeam evaporation	pressure: 3E-6T, 1200A Au deposition	Ultek
13.09	Lift-off resist	ACE 24 hours (no ultrasonic)	sink
13.10	Rinse	IPA rinse 5min and DI water 5min	sink
14.00	**Post Metal Annealing**	(the NCFET sample skipped this step)	
14.01	Activation Anneal / Sintering	Recipe: H2SINT4A.018, 400C, forming gas(10% H2, 90% N2, 3000sccm), 30min	tystar18

4.7 References

[4.1] Vizdrik, G., et al. "Kinetics of ferroelectric switching in ultrathin films." Physical Review B 68.9 (2003): 094113.

[4.2] Wang, Y., et al. "Epitaxial ferroelectric Pb (Zr, Ti) O 3 thin films on Si using SrTiO 3 template layers." Applied physics letters 80.1 (2002): 97-99.

[4.3] Chambers, S. A., et al. "Band offset and structure of SrTiO 3/Si (001) heterojunctions." Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films 19.3 (2001): 934-939.

[4.4] R. A. McKee , F. J. Walker and M. F. Chisholm, Phys. Rev. Lett. 81, 3014-3017 (1998).

[4.5] Droopad, Ravi, et al. "Development of integrated heterostructures on silicon by MBE." Journal of crystal growth 251.1 (2003): 638-644.

[4.6] B. K. Moon and H. Ishiwara, Jpn. J. Appl. Phys., Part 2 33, L472 _1994_.

[4.7] Gu, X., et al. "Commercial molecular beam epitaxy production of high quality SrTiO 3 on large diameter Si substrates." Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 27.3 (2009): 1195-1199.

[4.8] Eidelloth, W., et al. "Wet etch process for patterning insulators suitable for epitaxial high Tc superconducting thin film multilevel electronic circuits." Applied physics letters 59.10 (1991): 1257-1259.

Chapter 5: Conclusions

5.1 Summary of Work

This work has focused on researching new steep turn On/Off transistors for future low power electronics.

In chapter 2, The FBFET has shown excellent subthreshold swing of 1.67mV/dec with high I_{ON}/I_{OFF} ratio (~10E6). It can also be operated at relatively low supply voltage (<1V). The analytical model for the FBFET feedback mechanism has been presented, and the theory of the feedback mechanism agrees well with both experimental and simulated results.

In chapter 3, new transistor concept is proposed that synergistically combines two important trends of future transistors: ultra-thin body to suppress the short-channel effects and sub-60mV/decade operation to drastically reduce power consumption. NCFET happens to need ultra-thin body as thin as 0.5nm to achieve 0.3V operation. Simulation results of thin Si body NCFET was used to illustrate the possibility of achieving sub-30mV/dec, 10pA/μm I_{OFF}, 200uA/um Ion at 0.3V supply voltage without any hysteresis.

In chapter 4, fabrication scheme was proposed and demonstrated to integrate single crystal ferroelectric as the negative capacitance element on Si channel to fabricate p-type NCFET. Working transistor was fabricated with subthrehold swing of ~100mV/decade.

5.2 Future Directions

FBFET has demonstrated achieving excellent steep turn On/Off behavior at supply voltage of ~1volt; however, for this device to have practical use for low power logic, the required power supply must be able to scale down. Future research of fabricating FBFET using lower bandgap materials might be an option. Besides non-volatile memory and logic applications, FBFET might also be used in sensing applications due to its abrupt switching behavior.

NCFET has shown promise in achieving sub-60mV/decade swing and could be a technology booster to enable ultra-low power MOSFETs in the "Post-Silicon Era". Material research in engineering negative capacitance material suitable for NCFET should be one of the research focus. In addition, an integration scheme with good gate stack/semiconductor interfacial quality is also important for successful demonstration of sub-60mV/decade NCFET.