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Freestanding High-Power GaN Multi-Fin Camel Diode Varactors for Wideband Telecom Tunable Filters

A dissertation submitted in partial satisfaction of

the requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Nanoscale Devices and Systems)

by

Po Chun Chen

Committee in charge:

Shadi A. Dayeh, Chair
Peter M. Asbeck
Andrew C. Kummel
Vladimir Odnoblyudov
Gabriel M. Rebeiz

2024

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University of California San Diego

2024

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ABSTRACT OF THE DISSERTATION

Freestanding High-Power GaN Multi-Fin Camel Diode Varactors for Wideband Telecom Tunable Filters

by

Po Chun Chen

Doctor of Philosophy in Electrical Engineering (Nanoscale Devices and Systems)

University of California San Diego, 2024

Shadi A. Dayeh, Chair

This dissertation accentuates the significance of high-power gallium nitride (GaN) camel diode varactors for RF transmitter applications. Modern RF transmitters favor compact adaptive circuits for cost and power efficiency. Adaptive circuits include tunable filters, tunable matching networks, and antenna tuners, facilitating adjustments in resonate frequency or impedance. Crucially, these components need to exhibit robust power handling capability when operating below 6 GHz. Vertical Schottky diodes stand out as tuning elements in these high-power adaptive

circuits due to their compactness, high power handling, and superior quality factor, with GaN holds promise for achieving the highest quality factor figure of merit (QFOM) owing to its outstanding breakdown electric field and favorable electron mobility.

Popularly pursued GaN Schottky diode varactors suffer from leakage currents at high reverse voltage biases at their junctions and because of inherent threading dislocations in thin GaN layers on foreign substrates. We devised a novel device architecture to address these limitations. We employ an interdigitated anti-series multi-Fin camel diode structure composed of a thin p^+-GaN top layer situated between the Schottky metal and an n-type GaN drift layer. The p-GaN layer raises the barrier height to suppress reverse leakage current to maintain a high Q factor at higher reverse biases than Schottky diodes. Additionally, we utilize GaN on Qromis Substrate Technology (QST) wafers that permit the growth of thick GaN layers with lower dislocation densities and lower leakage currents than GaN-on-Si and that are comparable to GaN-on-GaN.

In this dissertation, we first propose a universal design flow for power varactors. Secondly, we experimentally validate the proposed methods for suppressing leakage current. Subsequently, a significant portion of this dissertation is dedicated to device optimizations encompassing epi-structure and device aspects. Detailed iterations of experiments and subsequent improvements are documented. The finalized fabrication flow and the DC, RF S-parameters of these diodes are reported, signifying their potential to outperform other power varactor technologies. Lastly, we demonstrate prototype bandpass filters using these diodes, underscoring the feasibility of real-world applications with further refinement and development efforts.

CHAPTER 1: Motivation and Challenges of GaN High-Power Varactors

1.1 Background: Unmet Need of Adaptive Circuits at RF Transmitter

The demand for faster data rate in mobile devices and novel applications has fueled higher frequency bandwidths for 5G.[1] This trend of bandwidth is associated with increased power transmission for wireless communication, paving the way for greater capacity, as per Shannon's formula.[2] Greater output power at RF transmitter also benefits the coverage area of base stations. However, expanding frequency bandwidth means a more complex RF front-end architecture, resulting in a larger and costlier RF transceiver.[3,4] For example, 6-9 antennas are typically needed in a 5G device, compared to 2-6 antennas in a 4G device.[5-9] Similarly, the number of acoustic filters in a 5G smartphone doubles compared to a 4G smartphone. Therefore, active and passive circuit miniaturization remains crucial for RF front-end modules for both mobile devices and base stations. Mobile systems as 4G LTE, 5G NR, and more advanced radio access technologies utilize multiple distinct bands that must be supported with minimal interference, along with Bluetooth, Wi-Fi connectivity, and GPS. Deploying adaptive circuits not only eases the circuit design difficulties but also keeps RF transceivers miniature. Take duplexers, which select distinct signal frequency ranges for transmission and reception, as an example. Conventional duplexers contain RF switches and acoustic filters. To operate under more frequency bands, more RF switches and acoustic filters are needed. Incorporating adaptive components, or tunable components, with electrical or mechanical passband frequency tuning mechanism enables continuous frequency tuning, multiple bands operation in a compact form. In addition to tunable filters, adaptive circuits like antenna tuners are essential components in modern RF transmitter.[10,11] Figure 1.1 shows path loss and schematic of front-end module architecture in RF transmitter tailored for 5G devices.[7] Besides size and cost challenges, RF pass loss from power amplifiers (PAs) to antennas is a notable

concern for 5G. Tunable matching networks placed after PAs for dynamic load modulation have been proposed, offering broad-band matching and efficiency improvement.[12-14] An example of load impedance modulation for a varactor based tunable matching network can be found in Figure 1.2.[13] Similarly, antenna tuners extend tuning across wide frequency and boost efficiency without the need of extraneous impedance matching components. Figure 1.3 displays how magnitude of reflection coefficient varies under different bias for a varactor loaded slot antenna.[10] These three adaptive circuit components underscore the vital role of tuning elements in modern RF transmitters.

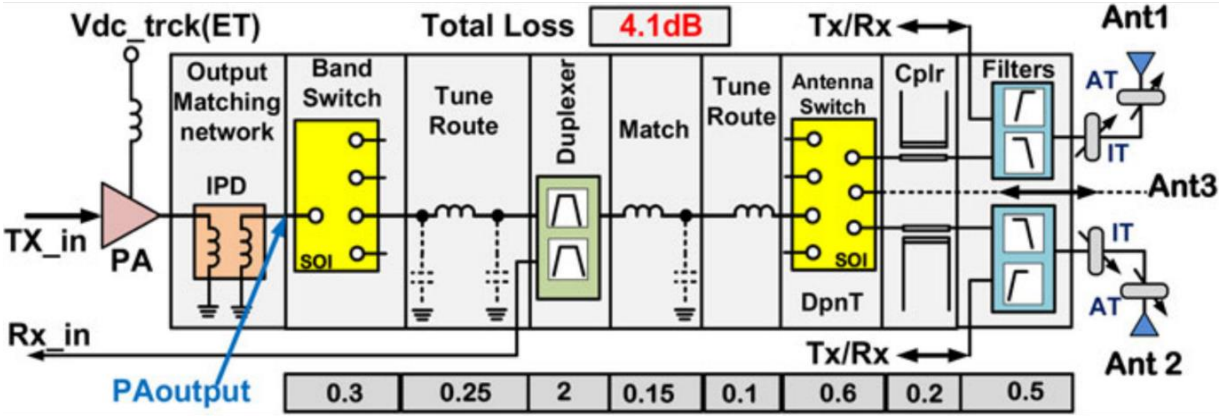


Figure 1.1 5G transmitter architecture and RF path loss from PAs to antenna.

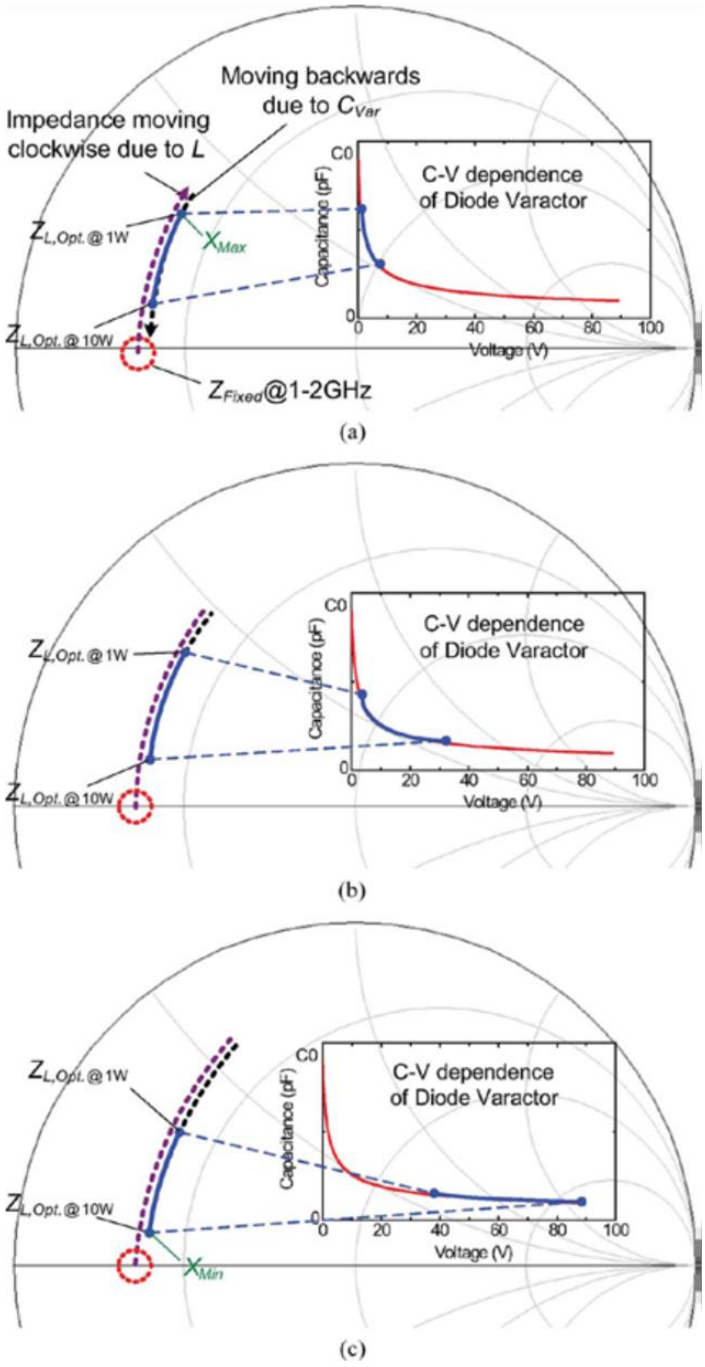


Figure 1.2 Broadband dynamic load modulation matching scheme using varactor based tunable matching network. (a) At 1 GHz. (b) At 1.5 GHz. (c) At 2 GHz.

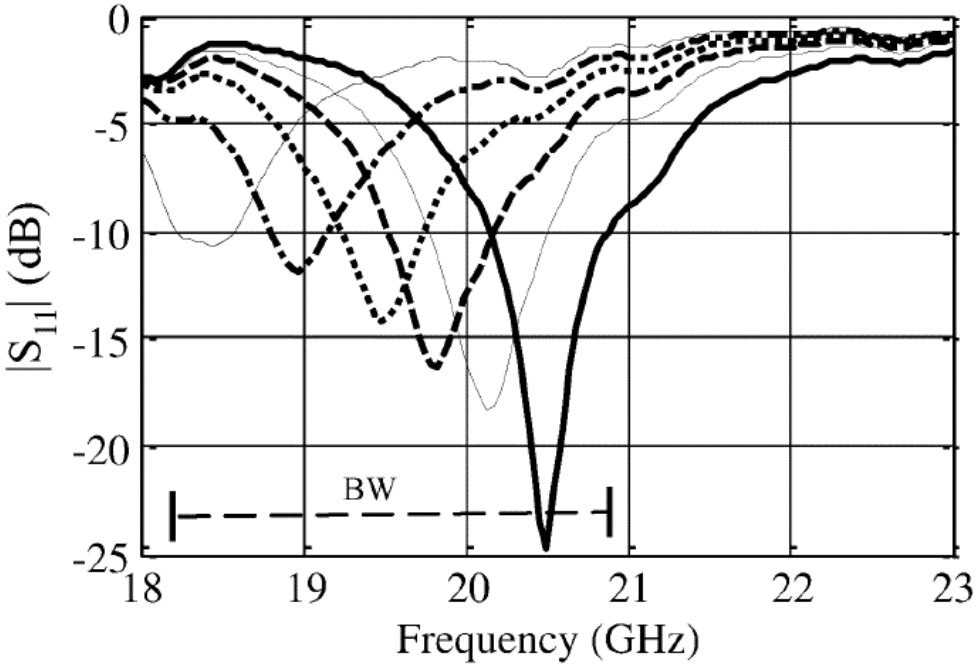


Figure 1.3 Measured magnitude of reflection coefficient for the varactor diode loaded slot antenna versus frequency for 6 values of diode voltages 4 V, 6 V, 8 V, 10 V, 12 V and 16 V.

As demands of power amplifiers with higher power density and power efficiency continues to grow in RF frequency and mm-wave frequency, power handling capability for adaptive duplexers and antenna tuners is essential to keep pace. Tunable elements at transmitters are also required to handle large power in handsets and base stations. Due to the tradeoff between output power and operating frequency of power amplifiers, the power handling capability a tunable element requires at sub-6 GHz is larger than at 30 GHz (Figure 1.4).[15-17] It's imperative to choose frequency bands of interest while developing tunable element technology. In this work, we develop high-power tunable elements targeting operating frequency less than 6 GHz. These elements are designed to hold average power exceeding 40 dBm, equivalent to a peak-to-peak voltage of 70 V in a 50 Ω system. While various tunable elements have been proposed, the required criteria of high

quality factor (Q), high linearity, high tuning ratio, and high power handling capability for a variety of civilian and military applications are not concurrently satisfied by a single device architecture in available technologies to date.

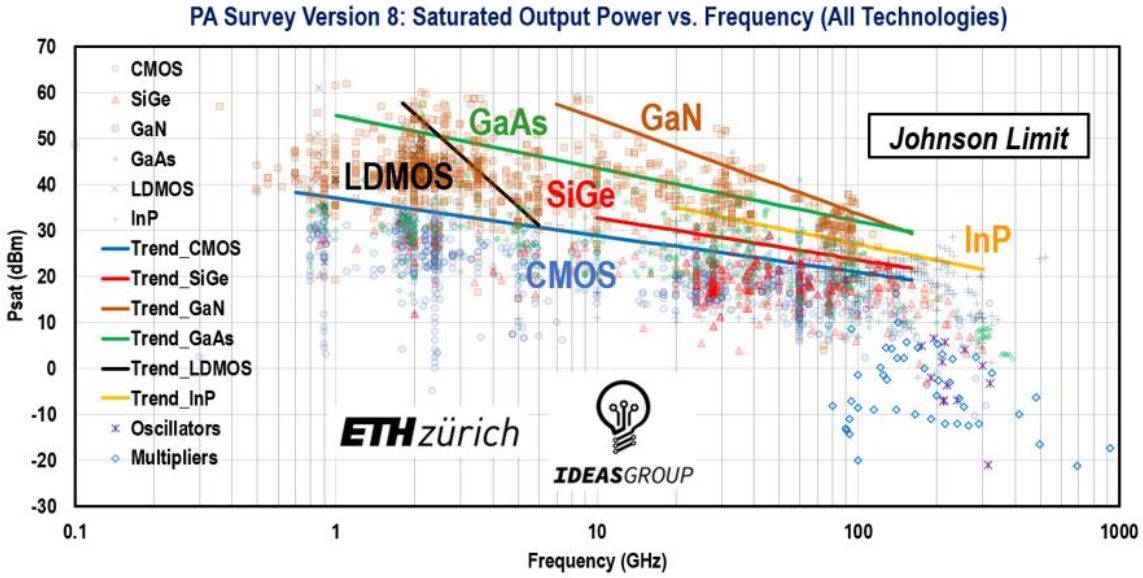


Figure 1.4 Saturated output power vs. frequency for reported PAs.

1.2 Tunable Elements for Adaptive Circuits

Tunable element technologies include mechanically tuned dielectric resonator filters,[18,19] tunable superconducting filters,[20] p-i-n diode switches,[21,22] barium strontium titanate (BST) capacitors,[23-25] and varactor diodes.[26] The tradeoffs for these tunable elements constrain their applications. For instance, mechanically tuned cavity filters are bulky, and cryogenic coolers are mandatory for the usage of superconducting filters. These factors restrict tuned cavity filters and superconducting filters for miniaturization and integration. Compared with p-i-n diode-based tunable filters that have discrete tuning, varactor diodes-based filters offer continuous tuning with better tuning resolution, more compact form factor, and lower power consumption. CMOS

varactors have limited power handling prospects and CMOS passive elements also suffer from low quality factor. Although MEMS varactors nowadays suffer less from reliability problems, they can be affected by intermodulation distortion because the modulation envelope of an RF signal can affect the position of the membrane.[27] MEMS varactors are also characterized with a small tuning range and a small capacitance density. BST-based tunable elements achieve high capacitance density, good tuning range at low voltages in the range of 1–25 V and are utilized in IC products. These ICs demonstrate good third-order intercept point (IP3) with input signals of 25 dBm but allow a 33-dBm maximum input power.[28] Among the tunable element technologies, vertical Schottky diodes based varactors are specifically tailored for high-power applications.

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1.3 Vertical Diodes Varactors: GaN Outperform Other Semiconductor Materials

Vertical Schottky diodes consist of anode metal, n^- drift layers, n^+ layer, and cathode metal. Figure 1.5 demonstrates the cross-sectional schematic of a vertical Schottky diode.[29] By applying varying reverse bias at the anode, the depletion width of n^- drift layer undergoes changes. This depletion width modulation results in variable junction capacitance. The depleted n^- drift layer can be likened to a parallel plate capacitor, while the non-depleted n^- layer, n^+ layer, and metal contact contribute to the series resistance. Lu et al. conducted a comprehensive comparison of semiconductor materials, including Si, GaAs, InP, and GaN, for high-power varactors application within vertical Schottky diode configuration. Such comparisons involve assessing the required varactor tuning ratio and power handling capability. To simultaneously meet such criteria, the quality factor (Q) varies across different semiconductor materials. Q for a varactor is calculated as follows:

$$Q = \frac{1}{2\pi f R C} \qquad (1-1)$$

Table 1.1 shows the upper bound Q_{min} for each semiconductor material where Q_{min} is the quality factor when reverse bias is 0 V.[30] Under 0 V bias, Q is smallest due to largest capacitance and largest series resistance. Thanks to its good mobility and unmatched critical electric field, GaN can reach the highest quality factor figure of merit (QFOM) compared to other semiconductor materials for the given vertical Schottky diode geometry. Detailed derivation of the QFOM comparison can be found in works done by Lu et al.

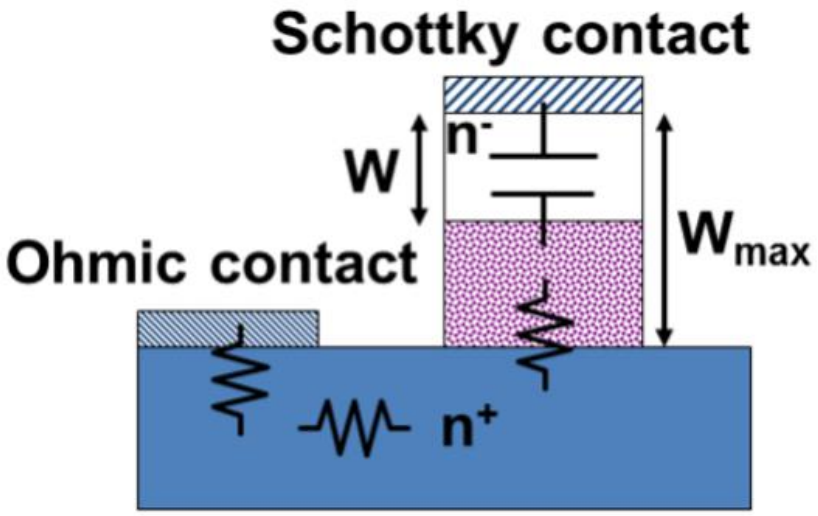


Figure 1.5 Vertical varactor diode schematic.

Table 1.1 Comparison of property and varactor FOM for various semiconductor materials. Given f = 1 GHz, C_{max}/C_{min} = 3, Vmax = 100 V, GaN varactors offer highest Q_{min}.

	Si	GaAs	InP	GaN
μ (cm^2/Vsec)	1200	4000	3500	500
E_{bk} (MV/cm)	0.25	0.35	0.40	2.5
μE_{bk}^2 (10^{12} V/sec)	75	490	560	3125
Q_{min}	30	195	223	1240

Earlier work on GaN Schottky diodes with InGaN tunneling barriers impressively achieved a breakdown voltage exceeding 120 V, a Q exceeding 100 at 1 GHz with a tuning range of 3.8:1.[29-32] When GaN Schottky diode varactors were employed in an anti-series configuration, the linearity of the varactor was improved, such that an OIP3 of 71 dBm was obtained.[33,34] However, the devices face fundamental limitations due to the growth of GaN material sapphire substrates. Consequently, the reverse leakage current density exceeded 20 mA/cm^2 at −50 V. Furthermore, contrary to expectations, an increased reverse DC bias failed to boost Q as expected and the extracted series resistance rose with bias. These phenomena imply opportunities for optimization in vertical GaN Schottky varactors, spanning from epitaxial growth to device design.

Research on high-power varactors has seen limited progress since 2012. In 2019, Song et al. reignited the conversation with a study based on physical calculations on GaN varactors.[35] Figure 1.6 provides four designs in their work, including vertical Schottky diode with bottom cathode contact, vertical Schottky diode with lateral cathode design, fin design, and multichannel design. While the latter two designs show great Q performance, the first two designs are more feasible for practical applications. The fin and multichannel design latter two designs depend on side Schottky contact and higher lithography resolution, posing challenges in perfect Schottky contact at metal and plasma-etched sidewall interface. In their work, the Q vs. tunning ratio is primarily focused yet power handling capabilities are not delved. Nonetheless, this work extensively compares simulated varactors and different Schottky diode varactors reported in various studies in terms of Q and tunning ratio, bringing valuable insights into the field of varactors.

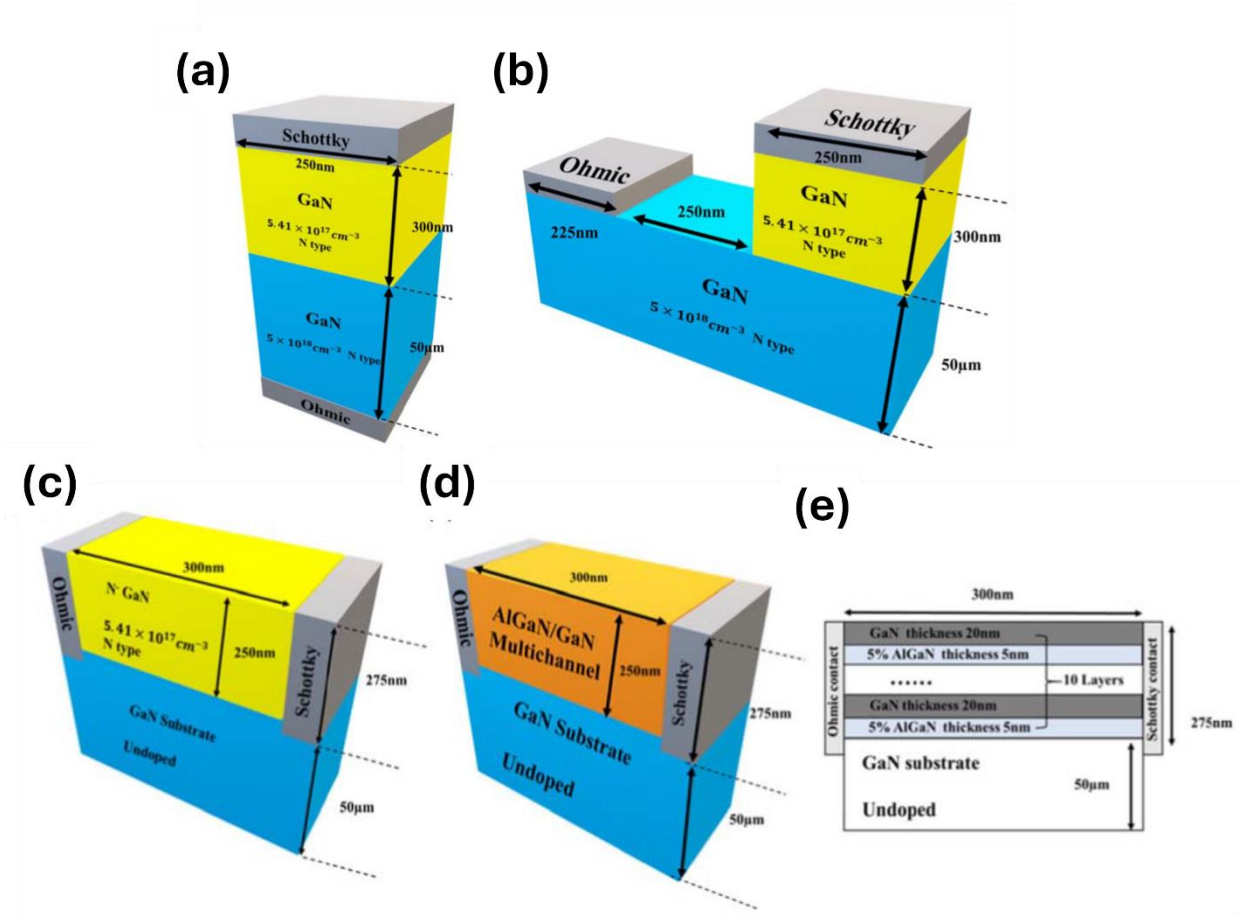


Figure 1.6 (a) Schematic structure of vertical design, (b) schematic structure of lateral design, (c) schematic structure of fin design, and (d) schematic structure of multichannel design. (e) 10-layer multichannel structure.

1.4 Thesis Outline

This dissertation endeavors to delineate the maximum performance of vertical GaN Schottky diodes across operating frequency below 6 GHz. The primary objective is to experimentally showcase state-of-art power varactors and their integration into a homemade tunable filter. This dissertation covers novel epitaxy designs, fabrication process, electrical characterization, and analysis of the varactor devices and tunable filters.

In chapter 2, we calculate and discuss the relationship between doping concentration, diode area, and operating frequency, demonstrating the expected breakdown voltage (V_{bk}), Q_{min}, small signal tuning ratio (SSTR). Furthermore, we discuss the strategies, camel diode and GaN growth on QST substrate, utilized to attain diodes with minimal reverse leakage currents. Fabrication process in details of circular diodes is covered, so is the forward bias I-V, reverse bias I-V, reverse bias C-V for our first-generation epitaxial structures.

Chapter 3 illustrates preliminary s-parameter and harmonic balance simulation according to the empirical results from circular diodes. These simulations reveal promising results, showing high quality factors and excellent linearity. Additionally, we elaborate the fabrication steps of anti-series multi-Fin diodes, unveiling the device structure. Concerns and challenges such as center parasitic capacitance and viable solutions are also discussed. We then show the reverse bias I-V, reverse bias C-V, one-port s-parameter characteristics for multi-Fin diodes for our first-generation epitaxy structures.

A new epitaxial structure is introduced in chapter 4. Doping depth profile for first-generation and second-generation epitaxial structures has been studied by secondary ion mass spectrometry (SIMS). We conduct circular and multi-Fin diode configurations on the new epi structure, head-to-head comparing the two structures. Thorough investigation of forward bias I-V, reverse bias I-V, reverse bias C-V, and one-port s-parameter characteristics has also been conducted in this chapter.

Lastly, we present a summary of this dissertation with a focus on homemade tunable filters in chapter 5. A tunable filter consisting of our varactors and coupled line resonator is first designed by ADS circuit simulation with its built-in microstrip model. Subsequently, PCB design is executed and validated by electromagnetic (EM) simulations. At the time of writing of this

dissertation, promising filter results have been obtained. Ongoing efforts are being made to further optimize the tunable filter performance.

Chapter 1, in part, is a reprint of the materials as it appears in *IEEE Transactions on Electron Devices* 2023. P. C. Chen, P. M. Asbeck, and S. A. Dayeh. The dissertation author is the first author of this paper.

CHAPTER 2: GaN Varactor Optimization: Camel Diodes on QST substrates

2.1 Varactor Design: Doping Concentration vs. Area vs. Operating Frequency

The optimal specification of a varactor varies significantly based on its application. It depends on the specific component it integrates with, operating frequency, Q factor, and power handling requirements. For instance, when a varactor is utilized as a tuner, the reactance

$$X = \frac{1}{2\pi f C} \qquad (2-1)$$

should roughly span from 20-25 Ω to 100-150 Ω. Reactance is a function of operating frequency and capacitance. The junction capacitance in a n-type Schottky diode follows

$$W_{dep} = \sqrt{\frac{2\varepsilon_s \varepsilon_0 (V_{bi} - V_a)}{qN_d}} \qquad (2-2)$$

Therefore, operating frequency, Schottky contact area, Schottky metal to use, and doping concentration all must be carefully evaluated. At the beginning of this chapter, we present detailed sketches that illustrates how variation of doping concentration, Schottky contact area, and operating frequency influence device characteristics. We calculate depletion width, breakdown voltage, Q_{min}, small signal tuning ratio (SSTR), and reactance based on different n-type doping concentration (1×10^{17} to 7×10^{17} cm^{-3}) also under different frequencies. In the case of n^--GaN Schottky contact, built-in voltage remains relatively unchanged with n^--GaN doping concentration of interest. The stability is attributed to the fact that the difference of φ_n for each doping concentration is negligible according to

$$\varphi_n = \frac{kT}{q} ln \frac{N_c}{N_d} \qquad (2-3)$$

where N_c is 2.6×10^{18} cm^{-3}. φ_n is the potential difference of conduction band and the Fermi level, and V_{bi} can be written as

$$V_{bi} = \Phi_m - \chi - \varphi_n \quad (2-4)$$

Both Schottky metal work function, Φ_m, and electron affinity of GaN, χ, are constants. Since φ_n is almost unchanged, V_{bi} also remains constant. For our calculation, we set the V_{bi} to be 3.4 V, aligned with the bandgap energy (E_g) of GaN, which is 3.4 eV. This assumption is based on the camel diode configuration explored in this dissertation. More details of camel diodes are provided in subsequent sections. Additionally, we assess GaN mobility across different doping concentrations in Figure 2.1.[36-41] To be conservative, these mobility values are derived by experimental reported data, rather than relying on the Albrecht model.[42] Mobility values are 475 cm^2/V-s, 400 cm^2/V-s, 320 cm^2/V-s, 290 cm^2/V-s, 250 cm^2/V-s for N_d of 1×10^{17} cm^{-3}, 2×10^{17} cm^{-3}, 3×10^{17} cm^{-3}, 5×10^{17} cm^{-3}, $7 \times 10^{17}$$cm^{-3}$, respectively in this dissertation.

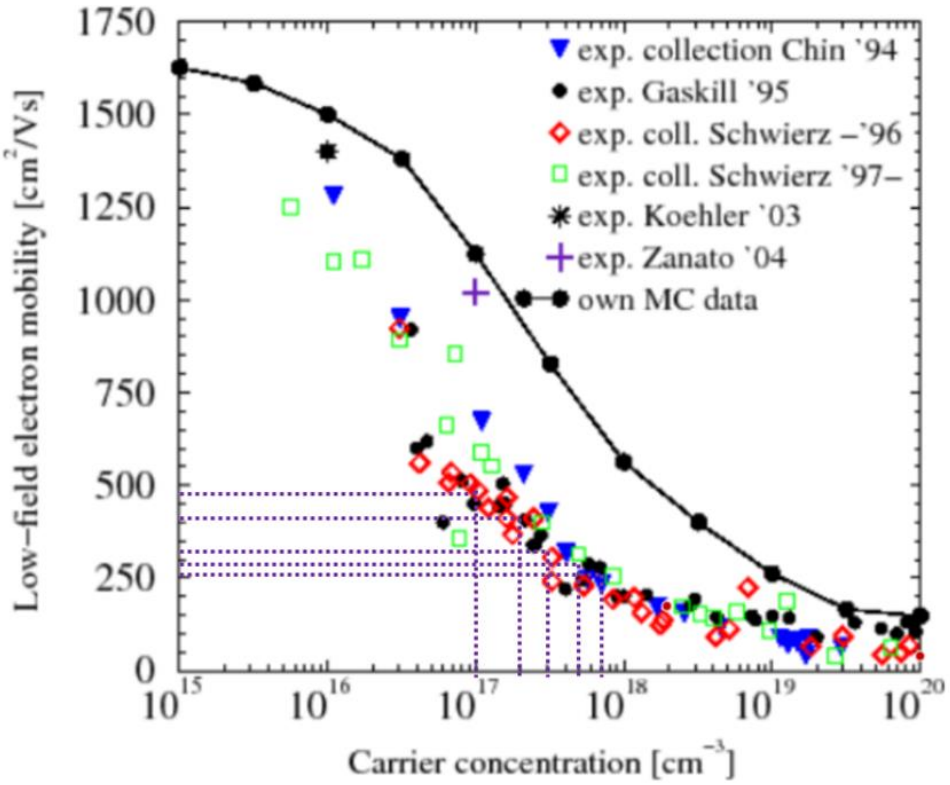


Figure 2.1 N^--GaN mobility selection to target varactor performance. 1×10^{17} cm^{-3}, 2×10^{17} cm^{-3}, 3×10^{17} cm^{-3}, 5×10^{17} cm^{-3}, 7×10^{17} cm^{-3} are selected for carrier concentration.

Table 2.1 presents estimated varactor performance. The optimal maximum depletion width, $W_{max,opt}$, is determined by the critical electric field (E_{bk}) of GaN set to be 3 MV/cm, following

$$W_{max,opt} = \frac{\varepsilon_s \varepsilon_0 E_{bk}}{qN_d} \qquad (2-5)$$

For any n^--GaN layer thicker than $W_{max,opt}$, breakdown occurs before fully depletion of the drift layer. Remaining non-depleted n^--GaN under maximum reverse bias acts as extraneous series resistance and jeopardizes Q factor. Hence, n^--GaN layer thickness is not supposed to exceed $W_{max,opt}$. The breakdown voltage (V_{bk}) is determined by

$$V_{max} = \frac{E_{bk} W_{max,opt}}{2} \qquad (2-6)$$

SSTR is the ratio of depletion width under zero bias and maximum reverse bias. Figure 2.2 (a) presents the C-V_{rev} relationship for diodes with area of 1.26×10^{-5} cm^2. Figure 2.2 (b) displays Q-V_{rev} plot, comparing quality factors at operating frequency of 1 GHz, 3 GHz, and 5 GHz.

Table 2.1 Target characteristics of ideal vertical GaN power varactor with different n−-GaN doping concentration. 1×10^{17} cm^{-3}, 2×10^{17} cm^{-3}, 3×10^{17} cm^{-3}, 5×10^{17} cm^{-3}, 7×10^{17} cm^{-3} are selected for carrier concentration.

N_d (cm^{-3})	1E17	2E17	3E17	5E17	7E17
μ (cm^2/Vs)	475	400	320	290	250
$W_{max,opt}$ (nm)	1660	830	553	331	237
V_{bk} (V)	245	121	80	46	32
Q_{min} (0V, 5GHz)	22.6	56.9	87.6	185.4	282.5
Q_{min} (0V, 20GHz)	5.7	14.2	21.9	46.3	70.6
SSTR	8.6	6.0	4.9	3.8	3.2

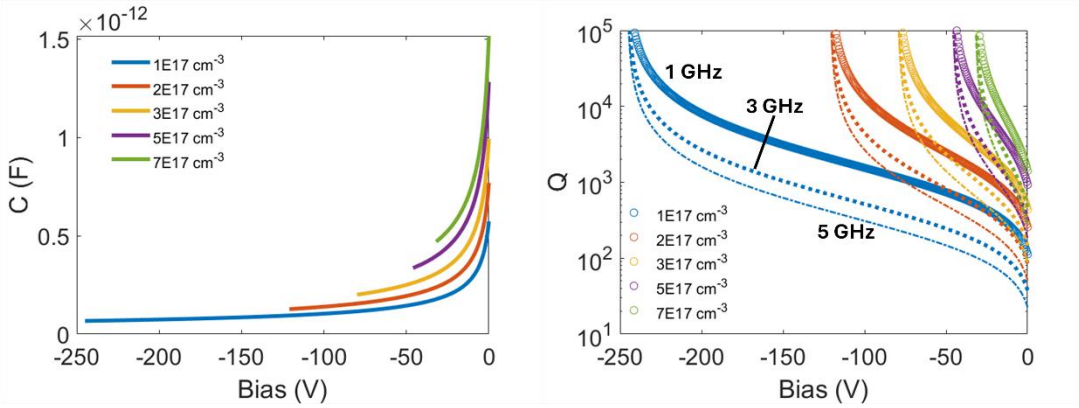


Figure 2.2 (a) Estimated C vs. V_{rev} for different n^--GaN doping concentration and (b) Estimated Q vs. V_{rev} for different n^--GaN doping concentration and under different operating frequency.

Varactor characteristics outlined in Table 2.1 and shown in Figure 2.2 are contact area and operating frequency independent, nonetheless, reactance depends on both the contact area and the operating frequency. We explore the X vs. Area vs. operating frequency across n^--GaN doping levels in Table 2.2 – 2.6. This analysis procedure is useful for varactor devices design. For instance, in the design of a high-power tuner operating at 3 GHz, a diode with 1×10^{17} cm^{-3} n- doping and area exceeding 5.03×10^{-5} will be the optimal choice.

Table 2.2 Reactance vs. area with n^--GaN of 1×10^{17} cm^{-3}.

Area (cm^{-2})	1.26E-5	2.51E-5	3.77E-5	5.03E-5	6.29E-5
$\|X\|_{max}$ (Ohm), 1 GHz	2372	1186	790.6667	593	474.4
$\|X\|_{min}$ (Ohm), 1 GHz	277.5	138.75	92.5	69.375	55.5
$\|X\|_{max}$ (Ohm), 3 GHz	790.6	395.3	263.5333	197.65	158.12
$\|X\|_{min}$ (Ohm), 3 GHz	92.5	46.25	30.83333	23.125	18.5
$\|X\|_{max}$ (Ohm), 5 GHz	474	237	158	118.5	94.8
$\|X\|_{min}$ (Ohm), 5 GHz	55.5	27.75	18.5	13.875	11.1

Table 2.3 Reactance vs. area with n^--GaN of 2×10^{17} cm^{-3}.

Area (cm^{-2})	1.26E-5	2.51E-5	3.77E-5	5.03E-5	6.29E-5
$\|X\|_{max}$ (Ohm), 1 GHz	1187	593.5	395.67	296.75	237.4
$\|X\|_{min}$ (Ohm), 1 GHz	196	98	65.3	49	39.2
$\|X\|_{max}$ (Ohm), 3 GHz	395.6	197.8	131.87	98.9	79.12
$\|X\|_{min}$ (Ohm), 3 GHz	65.4	32.7	21.8	16.35	13.08
$\|X\|_{max}$ (Ohm), 5 GHz	237.4	118.69	79.137	59.35	47.48
$\|X\|_{min}$ (Ohm), 5 GHz	39.24	19.62	13.08	9.81	7.85

Table 2.4 Reactance vs. area with n^--GaN of 3×10^{17} cm^{-3}.

Area (cm^{-2})	1.26E-5	2.51E-5	3.77E-5	5.03E-5	6.29E-5
$\|X\|_{max}$ (Ohm), 1 GHz	793.45	396.73	264.48	198.36	158.7
$\|X\|_{min}$ (Ohm), 1 GHz	160.2	80.1	53.4	40	32
$\|X\|_{max}$ (Ohm), 3 GHz	264.5	132.24	88.16	66.12	52.90
$\|X\|_{min}$ (Ohm), 3 GHz	53.4	26.7	17.8	13.35	10.68
$\|X\|_{max}$ (Ohm), 5 GHz	158.7	79.3	52.9	39.67	31.74
$\|X\|_{min}$ (Ohm), 5 GHz	32.04	16.02	10.68	8.01	6.41

Table 2.6 Reactance vs. area with n^--GaN of 5×10^{17} cm^{-3}.

Area (cm^{-2})	1.26E-5	2.51E-5	3.77E-5	5.03E-5	6.29E-5
$\|X\|_{max}$ (Ohm), 1 GHz	473	236.5	157.67	118.25	94.6
$\|X\|_{min}$ (Ohm), 1 GHz	124.1	62.05	41.37	31	24.82
$\|X\|_{max}$ (Ohm), 3 GHz	157.7	78.83	52.56	39.42	31.53
$\|X\|_{min}$ (Ohm), 3 GHz	41.37	20.68	13.79	10.34	8.27
$\|X\|_{max}$ (Ohm), 5 GHz	94.6	47.3	31.53	23.65	18.92
$\|X\|_{min}$ (Ohm), 5 GHz	24.82	12.41	8.27	6.205	4.96

Table 2.5 Reactance vs. area with n^--GaN of 7×10^{17} cm^{-3}.

Area (cm^{-2})	1.26E-5	2.51E-5	3.77E-5	5.03E-5	6.29E-5
$\|X\|_{max}$ (Ohm), 1 GHz	338.4	169.2	112.8	84.6	67.68
$\|X\|_{min}$ (Ohm), 1 GHz	104.9	52.44	34.96	26.22	20.98
$\|X\|_{max}$ (Ohm), 3 GHz	112.8	56.4	37.6	28.2	22.56
$\|X\|_{min}$ (Ohm), 3 GHz	34.96	17.48	11.65	8.74	6.99
$\|X\|_{max}$ (Ohm), 5 GHz	67.68	33.84	22.56	16.92	13.54
$\|X\|_{min}$ (Ohm), 5 GHz	20.98	10.49	6.99	5.24	4.2

2.2 Camel Diodes on QST substrate

We applied two strategies simultaneously to improve leakage current density and breakdown voltage in vertical GaN varactors by leveraging low-defect density GaN by thick

epitaxy on engineered substrates, Qromis Substrate Technology (QST),[43-45] and by implementing the abovementioned camel diode device architecture. The leakage current density in vertical GaN devices is proportional to the dislocation density, which decreases as the GaN layers become thicker, as well as to the density of defects and impurities in the GaN layers.[46] Thick layers are also crucial for current spreading improvement and heating effects mitigation. The thermal expansion coefficient of QST substrates matches with GaN, allowing very thick GaN growth without cracking while cooling down from the MOCVD growth. In contrast, the inherent limitation of growing GaN on Si to just few micrometers greatly compromises the quality of GaN by high density of dislocation and Ga/Si interdiffusion, which have been a bottleneck of GaN on Si technology.[47-50] Our group has shown in a previous report that Schottky diodes with regrown GaN/QST templates could reach a low dislocation density (Figure 2.3) and a comparable leakage current density to similar sized and manufactured diodes on regrown GaN on freestanding GaN substrates (Figure 2.4).[51] The camel diode device architecture constitutes a fully depleted p^+-GaN layer atop n^--GaN, which offers an anode barrier height up to 3.4 V, higher than the conventional n^--GaN-based Schottky diode, which is characterized with a barrier height of 0.7 V with the well-developed Ni contacts. A greater barrier height and a wider tunneling width at the surface of the camel diode can provide low leakage currents. A p-n diode structure with a thicker p^+-GaN layer can in principle reduce the leakage currents but suffers from losses due to both the poor ohmic contact between the metal and the p^+-GaN interface and the non-depleted p^+-GaN layer.[52,53] If a conventional p-n diode is utilized in this work, the total series resistance may increase by several times even with a p^+-GaN contact resistivity of 1×10^{-4} Ωcm^{-2}, which is considered as a good resistivity for a p^+-GaN Ohmic contact.[54] In this dissertation, we follow the principle shown in Table 2.1 for W_{max} and N_d selection. We also introduce epitaxy on engineered substrate and a thin

p^+-GaN which is expected to raise the barrier height and suppress reverse leakage current more effectively compared to heterostructure such as InGaN on GaN. The experimental development including process optimization, circular diode DC validation, and multi-Fin diode DC/RF validation is discussed in the following sections.

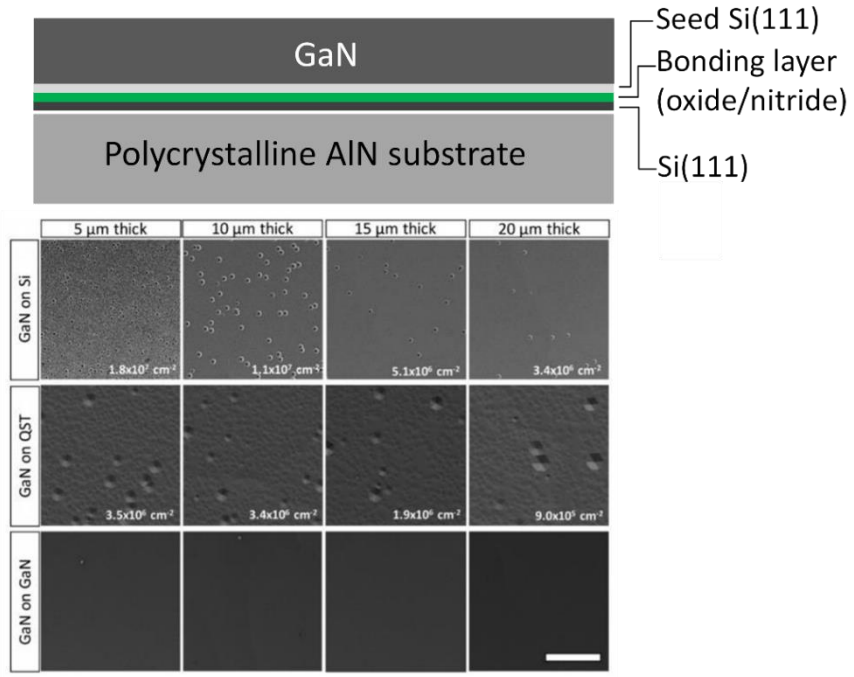


Figure 2.3 Cross-sectional structure of GaN/QST substrate and SEM images of GaN surface after defect selective wet etching.

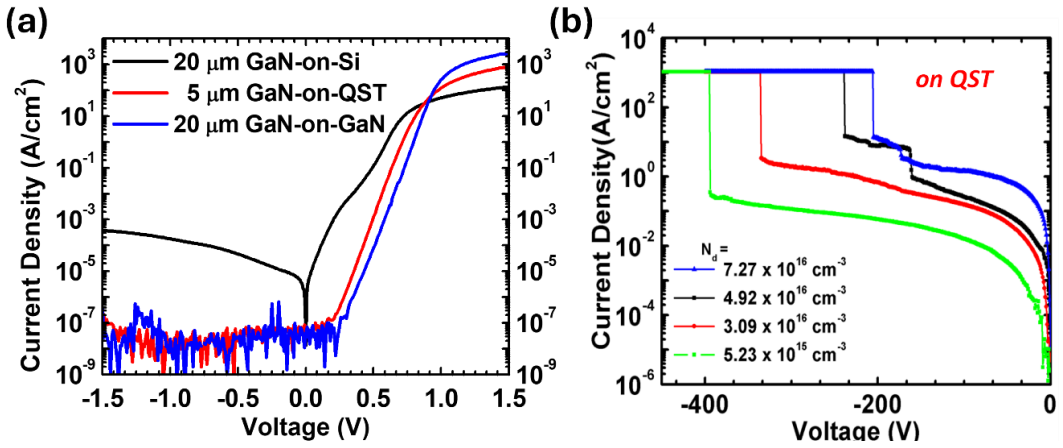


Figure 2.4 (a) I-V characteristics of best Schottky diodes on GaN/Si, GaN/QST, and GaN/GaN and (b) breakdown characteristics of GaN-on-QST Schottky diodes on 20 µm thick drift layers with different carrier concentrations.

2.3 Static Characteristics for Circular Diodes

The designed material structure consisted of a top 23-nm p+ GaN (Mg doped, $N_a = 2 \times 10^{19}$ cm^{-3}) and 1-μm n^--GaN (Si doped, $N_d = 2 \times 10^{17}$ cm^{-3}) on top of 5-μm n^+-GaN (Si doped, $N_d = 2 \times 10^{18}$ cm^{-3}) grown by metal organic chemical vapor deposition (MOCVD) on 6″ GaN-on-QST substrate template that consisted of 5-μm n^--GaN on nucleation, bonding, and isolation layers on a polycrystalline AlN substrate. The 6″ wafer surface was protected with photoresist, which after dicing was dissolved in remover PG (N-methyl-2-pyrrolidone-based solvent) in a 4-h immersion at 80 ˚C. A 200-nm-thick Ni Schottky metal was patterned, evaporated, and lifted off to form circular anode pads. A 700-nm-thick SiO2 layer was then deposited by plasma-enhanced chemical vapor deposition (PECVD), patterned, and etched with CHF_3/Ar reactive ion etching (RIE). After photoresist stripping, the circular SiO_2 layer on top of Ni served as an etching mask for GaN mesa etching. A 1.2-μm-deep GaN mesa etching was performed with BCl_3/Cl_2 RIE, which additionally partially etched the SiO_2 mask layer. The remainder of the SiO_2 mask layer was then dissolved by immersion into a 6:1 buffered oxide etchant (BOE). A Ti/Al/Ni/Au (20/120/40/50 nm) stack was evaporated and lifted off to form ring shape ohmic contacts with n^+-GaN without annealing. A cross-sectional schematic of the circular diodes is shown in Fig. 2.5(a). Fig. 2.5(b) illustrates that the built-in potential and the depletion width for camel diodes are expected to be higher than those of Schottky diodes and therefore reduce the reverse bias leakage current.

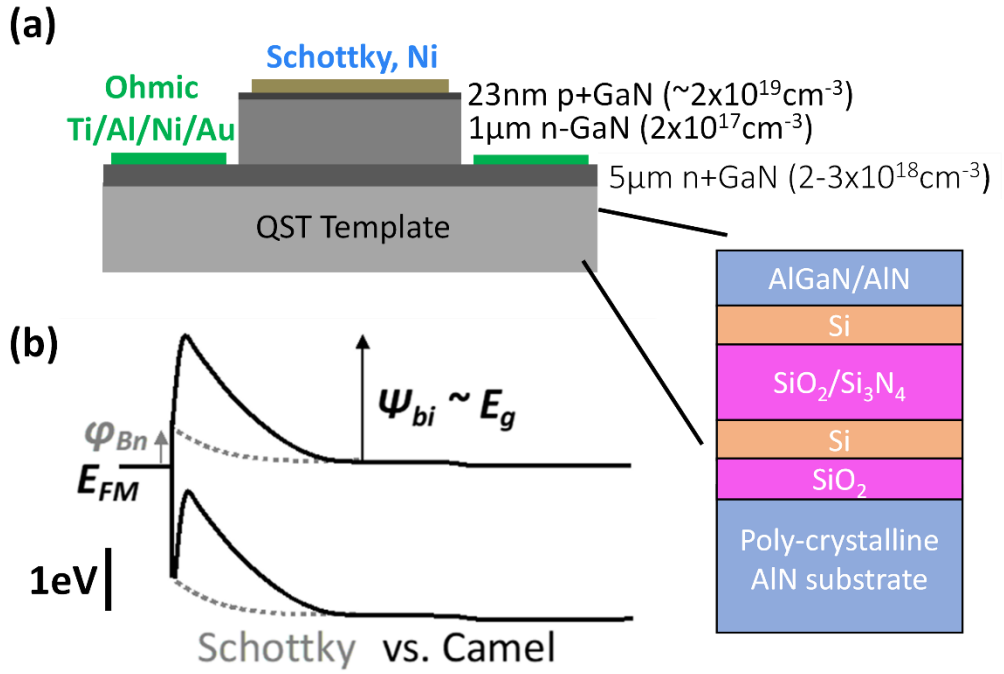


Figure 2.5 (a) Cross-sectional structure of circular diodes and (b) Schematic of a typical band-edge diagram for Schottky and camel diodes.

The reverse leakage current plays a crucial role in varactor performance. Paths of the diode leakage can be categorized into bulk (including junction) and sidewall (surface) leakages. We fabricated circular diodes with different diameters to investigate whether bulk or surface leakage currents were dominant (Figure 2.6).[55] A leakage current density that is dependent on the area of the diode, i.e., exhibits parabolic dependence on the radius of the diode contact, indicates that volumetric or bulk leakage is dominant. A leakage current density that is linearly proportional to the radius of the diode contact indicates that surface leakage current is dominant. In Figure 2.7, we compare the leakage and breakdown characteristics of circular diodes on GaN/QST substrate (1-µm n^-- GaN, $N_{eff} = 1.5 \times 10^{17}$ cm^{-3}) and that of a Schottky diode on freestanding GaN substrate (1-µm n^--GaN, $N_{eff} = 3 \times 10^{17}$ cm^{-3}). N_{eff} represents effective carrier concentration. The reverse breakdown characteristics of 24 camel diodes and five Schottky diodes were measured with a

Keithley 2410 source meter. Camel diodes, with higher built-in potential than Schottky diodes, were characterized with significantly lower leakage currents and significantly higher breakdown voltages than Schottky diodes. For the camel diodes, the leakage current density did not significantly change with the radius of the diode contact (Figure 2.8), indicating a dominant bulk leakage current and that the optimized RIE etching process does not lead to appreciable surface current leakage. The forward I –V and reverse C-V characteristics were measured with a B1500 parameter analyzer. The turn-on voltages were around 0.5 V for Schottky diodes and around 4.5 V for diodes with p^+-GaN surface layers (Figure 2.9), which further supports their superior leakage and breakdown behavior. The ohmic contact to the n^+-GaN diode body was not annealed to avoid possible degradation of the Schottky contact. As a result, this contact may contribute to a series resistance, which in turn leads to a higher turn-on voltage than the GaN bandgap of 3.4 V. Not fully depleted p+ layer and Ni/p^+-GaN layer contact can be another possible explanation for unexpected high this high turn-on voltage. This, however, does not compromise the practical varactor operation under anti-series configuration which will be covered in subsequent sections. Under such configuration, ohmic contact to the n^+-GaN is used to apply a reverse DC bias to the diodes and must be connected to a high value bias resistor to block any RF leakage. Therefore, low resistance ohmic contact is not needed. The C-V characteristics of the varactors with p^+ surface layers were measured as a function of reverse bias (Figure 2.10a). The ten devices that were measured exhibited uniform characteristics in the voltage range of 0 to −40 V, with a C_0 V/C_{-40} V of approximately 3.5. Figure. 2.10b shows a plot of $1/C^2$ as a function of reverse bias. The n^--GaN drift layer effective carrier concentration of $1.5 \times 10^{17} \pm 7 \times 10^{15}$ cm^{-3} was extracted from the slope of $1/C^2$–V curve according to

$$N_{eff} = \frac{2}{q\varepsilon_0\varepsilon_s}\left[-\frac{1}{d(1/C^2)/dV}\right] \qquad (2-7)$$

where ε_0 is the permittivity of free space, ε_s of 10 is the dielectric constant of GaN, and C is the capacitance that arises from depletion in the n^--GaN.[56] Overall, the circular diodes exhibited robust static I –V and C-V characteristics, and these measured reverse bias characteristics (0 V to -40 V) can be written as

$$I_{leak} = 7.4 \times 10^{-9} A V_{rev}{}^{3.905} \qquad (2-8)$$

$$C = \frac{1.8 \times 10^{-7} A}{(V_{rev} + 3.4)^{0.5}} \qquad (2-9)$$

These mathematical expressions based on empirical results is electrical characteristics are helpful to understand RF characteristics practical varactors.

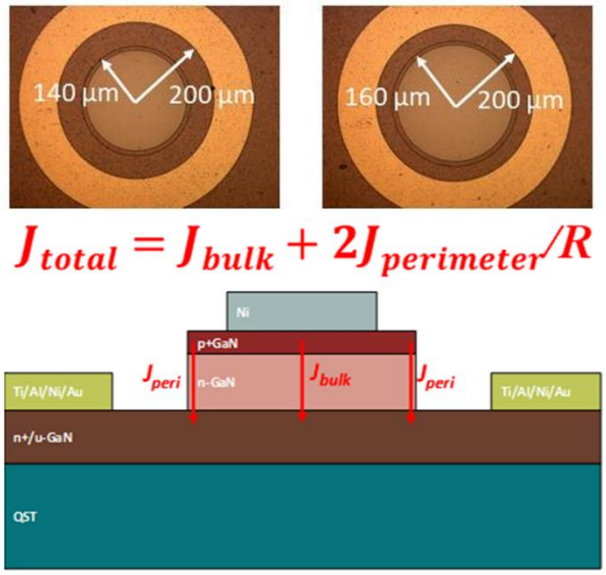


Figure 2.6 Images of circular diodes and schematic of the leakage current paths for bulk leakage and sidewall leakage.

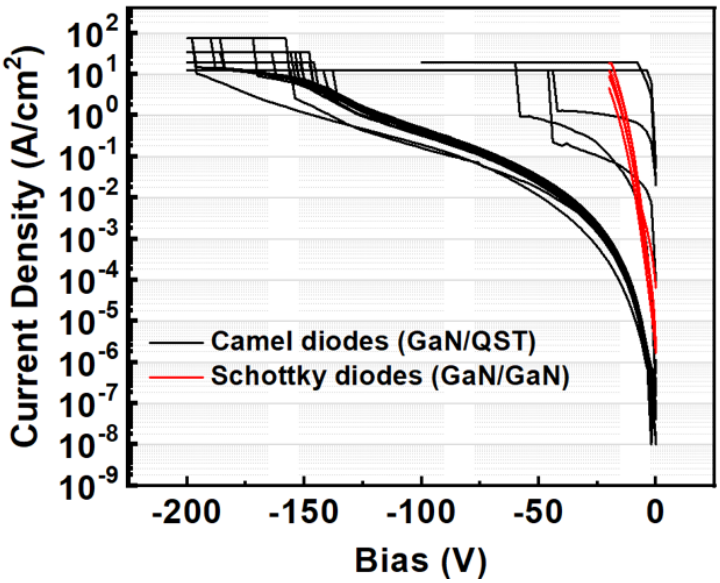


Figure 2.7 Comparison of J_{leak}-V_{rev} of GaN/QST camel diodes and GaN/GaN Schottky diodes.

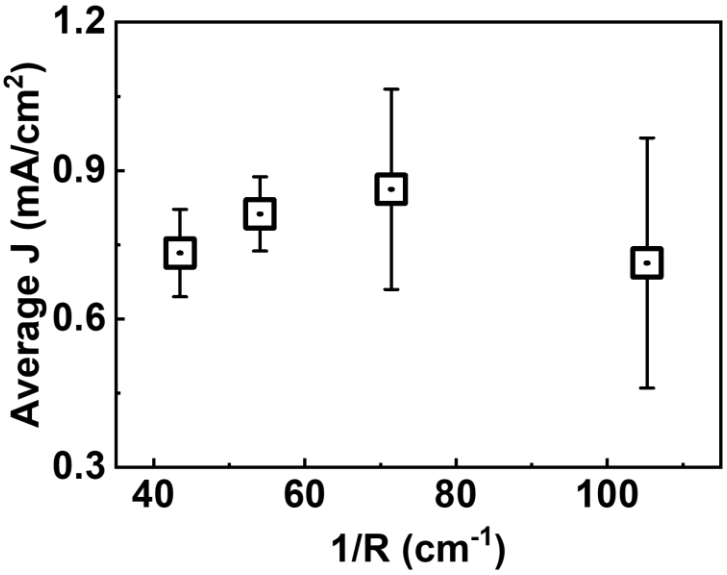


Figure 2.8 Average current density dependence with anode radii of 95 μm, 140 μm, 185 μm, 230 μm at -20 V. The error bars represent standard deviation.

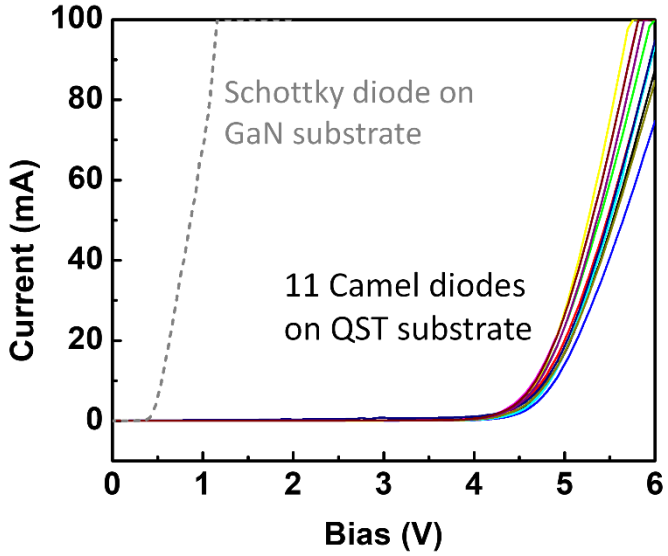


Figure 2.9 I-V turn-on characteristics of a Schottky diode and 11 camel diodes.

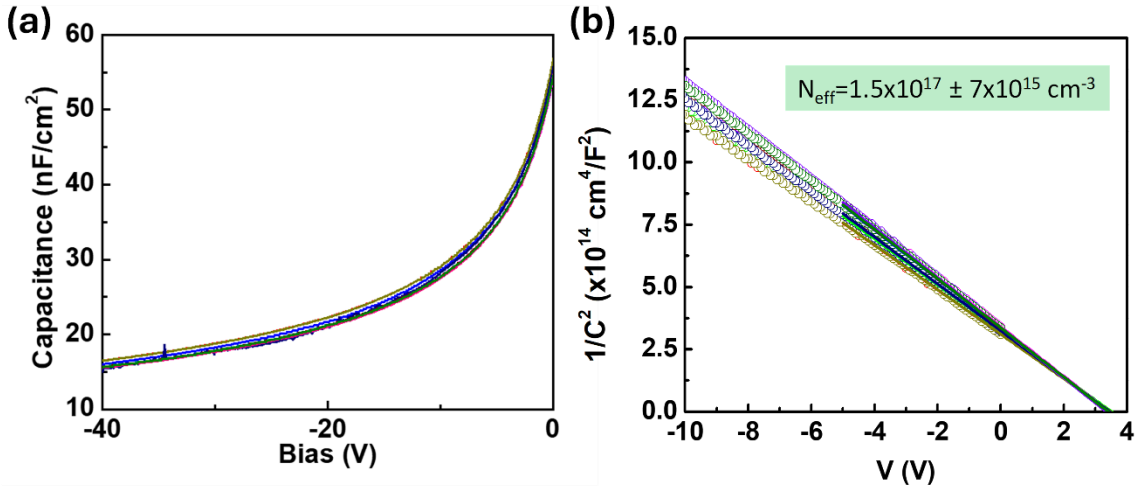


Figure 2.10 (a) Measured C-V_{rev} characteristics of diodes normalized with contact diode area and (b) Plot of $1/C_2$ versus V_{rev} and the extracted N_{eff} of diodes normalized with diode contact area.

2.4 Process Optimizations for Circular Diodes

The fabrication method described in section 2.3 yielded the best device performance and process yield. There were 3 preliminary versions of circular diode fabrication before finalizing our

standard approach. Figure 2.11 outlines the process flow of our initial three attempts. Both process 1 and process 2 begin with solvent clean and SiO_2 hard mask followed by GaN RIE. In process 1, we defined Ohmic contact atop n^+-GaN, annealing at 600 ºC under N_2 ambient for 5 minutes after GaN etching. The SiO_2 hard mask was then removed using BOE, and Ni Schottky contact was then formed. In contrast, for process 2, SiO_2 was removed before defining the Ohmic contact and conducting the Ohmic annealing. Differing from process 1 and 2, where Schottky metal was deposited after n^--GaN etching and Ohmic metal formation, Ni Schottky metal was deposited on p^+-GaN immediately after the first solvent clean step. We performed IV measurements for more than 20 devices in each sample. The yield for low-leakage devices from high to low is process 3, process 2, then process 1. Despite the comparable leakage current for the low-leakage devices across these three processes, Ni first process generally exhibits higher V_{bk} as demonstrated in Figure 2.12. Thus, we chose Schottky first process as our standard device fabrication protocol. We later found that the process mentioned in section 2.3, Ni lift off first associated with SiO_2 hard mask for GaN etch, outperforms process 3. Ni lift off plus SiO_2 hard mask also became the standard process throughout this dissertation.

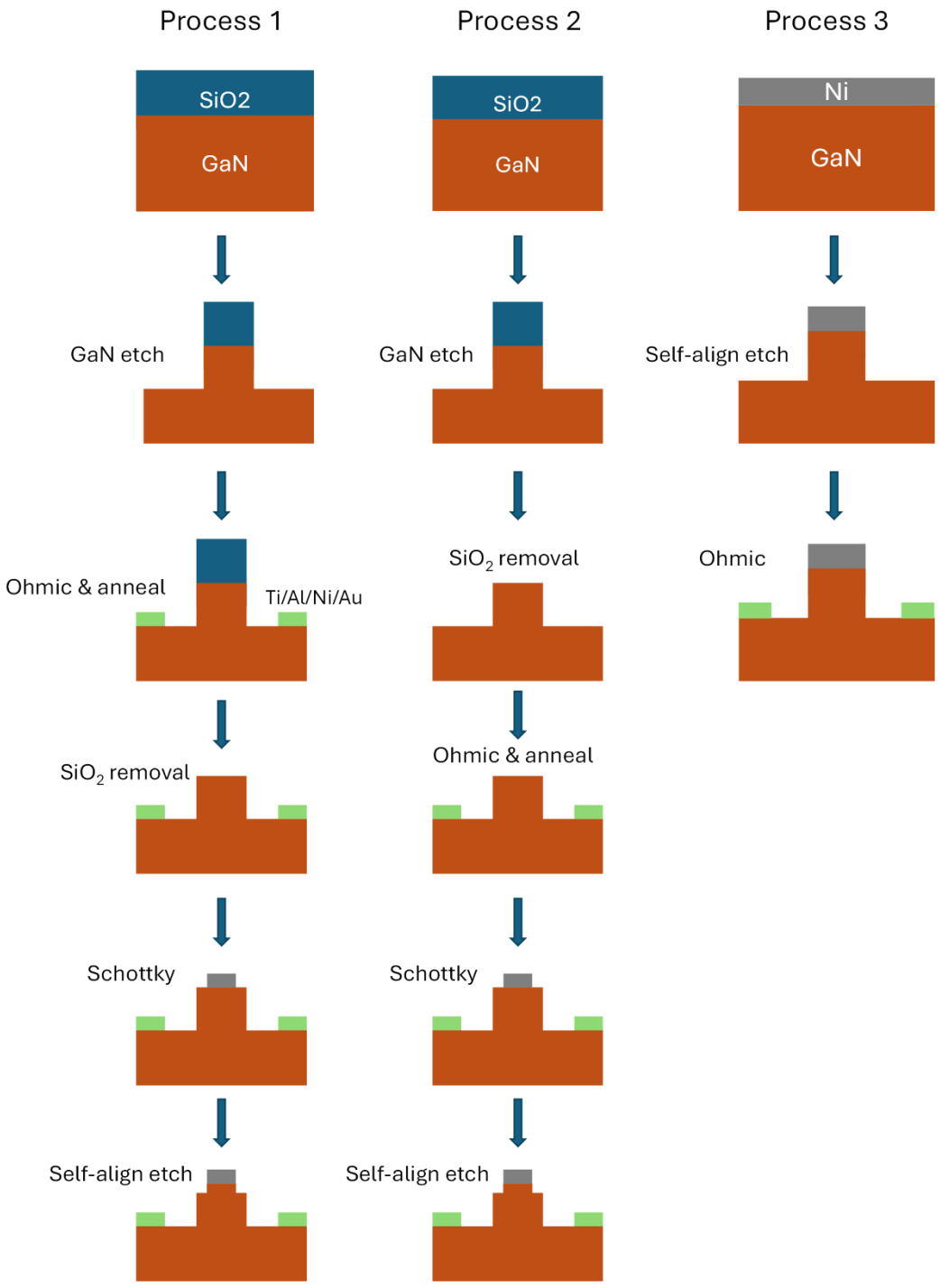


Figure 2.11 Initial process optimization with three circular diode process procedures.

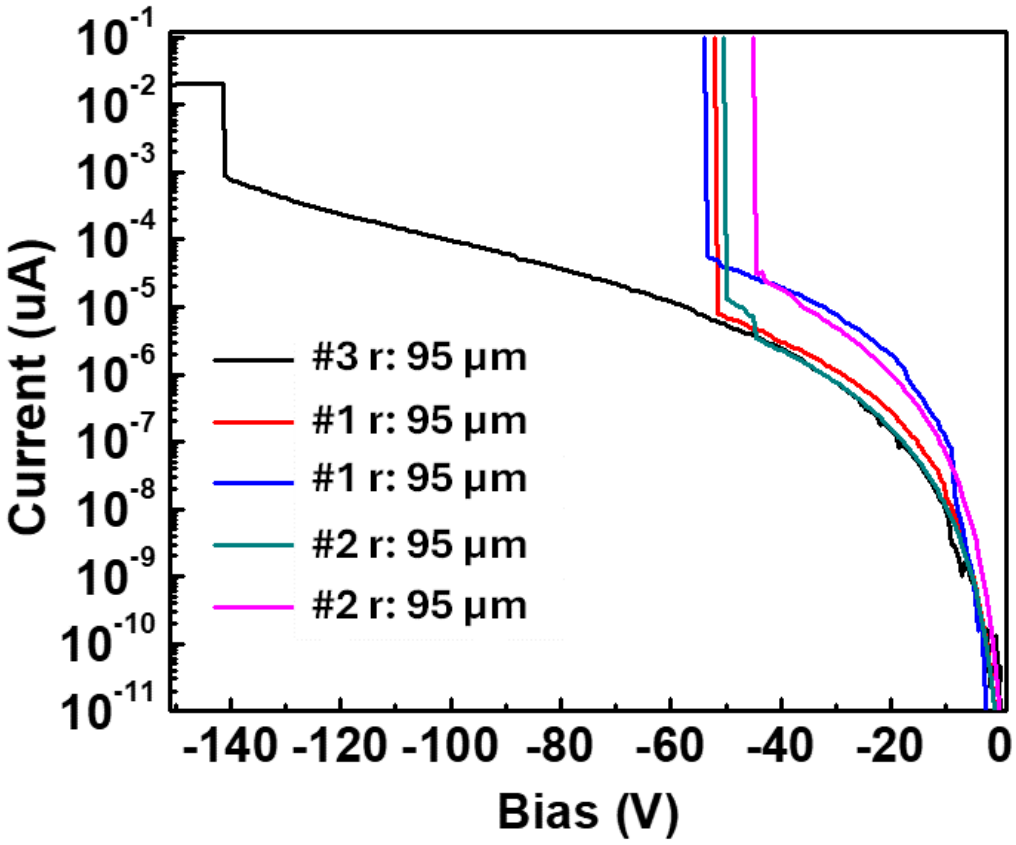


Figure 2.12 Reverse leakage current comparison between different process flow. r represents the radius of Schottky contact.

2.5 Conclusions

This chapter unfolds with a comprehensive design blueprint for GaN based varactor, presenting a practical approach that allows engineers to navigate GaN varactors design landscape from epitaxial layer to device area dimension aspect for various performance metrics. Since the efficacy of GaN based Schottky diode varactors are hampered by reverse leakage current, two strategies to suppress reverse leakage current applied in this dissertation are then proposed. One is to apply engineered substrates, QST, allowing comparable GaN quality to freestanding GaN but at a significantly reduced cost. The second strategy involves a thin p^+-GaN atop n^--GaN foundation that improves reverse leakage current while preserving the Q factor. The optimized varactor

fabrication process flow is then presented followed by standard I-V and C-V evaluation of circular diodes. The reason why we choose Schottky first process steps is then explained with process evolution. The optimized circular diode results suggest that these varactors can be operated under high reverse bias, and it is worth moving forward to next set of experiments, RF evaluation for the anti-series diodes with multi-Fin configuration, a more practical varactor structure.

Chapter 2, in part, is a reprint of the materials as it appears in *IEEE Transactions on Electron Devices* 2023. P. C. Chen, P. M. Asbeck, and S. A. Dayeh. The dissertation author is the first author of this paper.

Chapter 2, in part, is currently being prepared for submission for publication. P. C. Chen, P. M. Asbeck, and S. A. Dayeh. The dissertation author is the first author of this paper.

CHAPTER 3: Multi-Fin Varactors: Fabrication Process and Characterizations

3.1 Preliminary Simulation for Ideal Multi-Fin Varactors

The anti-series configuration sustains high varactor linearity, and the multi-Fin structure reduces the series resistance path between the diodes and therefore maintains high Q values. Before the experimentation of anti-series diode with multi-Fin structure, we assessed RF characteristics of our varactors in anti-series diode configuration by ADS s-parameter and harmonic balance simulations. Empirical I-V and C-V characteristics displayed as equation 2-8 and equation 2-9 were included in the simulations. In Figure 3.1a, we present the schematic of the anti-series varactor as proposed by Lu et al. Our devices share a close structure with theirs, primarily differing in the control resistance. We used an on-chip metal resistor instead of a snake shape GaN resistor to mitigate parasitic effects. Figure 3.1b is the ADS circuit schematic showing the implementation of empirical equations. The varactor capacitance (C_s) is modeled using the empirical C-V, while the reverse leakage resistance (R_{leak}) in parallel with the capacitor is modeled using the empirical I-V data. Additionally, we determine the resistance (R_s) of the non-depleted n^--GaN, which is placed in series with C_s. This calculation is based on the designated W_{max} of 1 μm, mobility of n^--GaN (μ) of 500 cm^2/Vs, and N_d of 1.5×10^{17} cm^{-3}. Following the setup, s-parameter and harmonic balance simulations were carried out. Figure 3.2a displays the Q factors and operating frequency relationship under various reverse bias. Figure 3.2b, on the other hand, illustrates IIP3 versus reverse bias with fundamental tones of 1.995 GHz and 2.005 GHz. These simulation outcomes are promising, offering confidence as we proceed with experimentation.

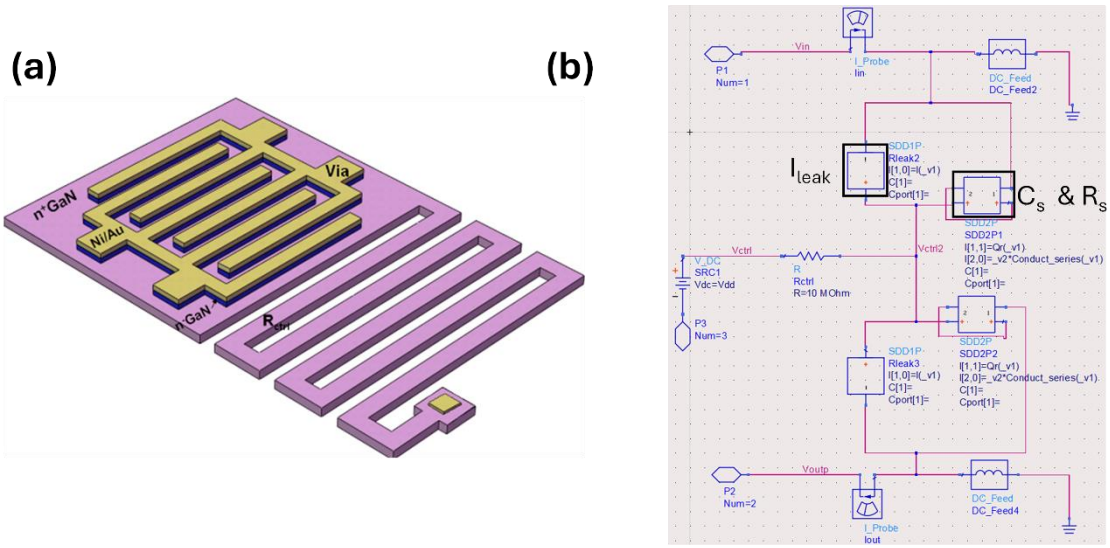


Figure 3.1 (a) Anti-series schematic for linearity improvement and (b) ADS circuit schematic of the varactor model.

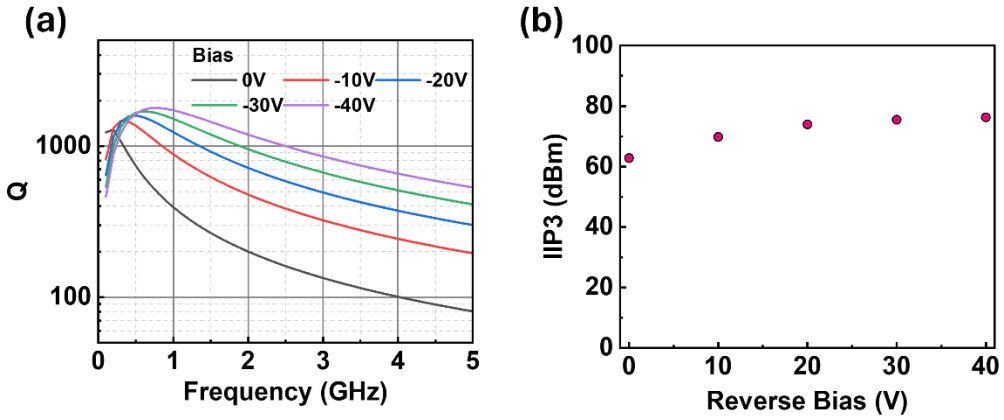


Figure 3.2 (a) Calculated Q vs. operating frequency based on the empirical C-V_{rev} and I-V_{rev} and (b) expected IIP3 vs. reverse bias with C_{max} = 0.7 pF, R_{ctrl} = 1MΩ, f_1 = 1.995 GHz, f_2 = 2.005 GHz, and μ_{n-} = 500 cm^2/Vs.

3.2 Structure and Fabrication Process of Multi-Fin Varactors

Figure 3.3 shows the fabrication process flow of the GaN multi-Fin anti-series varactor diodes. The first steps in the fabrication process are identical to the circular diode fabrication process steps up to the GaN etching step. The only significant differences for the multi-Fin

varactors were the thickness and composition of the Fin contact metal lines, which were significantly thicker and made of Ni/Au/Ti/Au (40/100/100/1200 nm), as shown in Figure 3.3a. The thicker metal lines atop the Fins reduce the current spreading resistance from the Ni Schottky contact to the p^+-GaN top layer of the epitaxial structure of the varactor diode. The samples were then immersed in 40 ˚C, 25% tetramethylammonium hydroxide (TMAH) for 10 min to smoothen the plasma damaged sidewalls that were specifically aligned parallel to the m-plane that we found to be smoother than those aligned to a-plane with the same process. Immediately after rinse and dry, the sample was coated with SiN_x/SiO_2 (120/4500 nm) by PECVD and was patterned to define varactor isolation by deep GaN RIE etching of 12 μm with a BCl_3/Cl_2 plasma to eliminate parasitic effects from conductive GaN. An RIE plasma etch with CHF_3/Ar gas followed by a BOE oxide etch was performed to remove the remaining dielectric layers atop n^+-GaN. An ohmic contact metal stack on n^+-GaN consisted of Ti/Al/Ni/Au (20/120/40/50 nm) was evaporated and lifted off (Figure 3.3b). After mesa isolation and to implement ground-source-ground (GSG) pads for RF characterization, a polymer fill-in step was performed. We used HD-4104 photodefinable polyimide (PI) to encapsulate the entire device and expose only the Schottky and ohmic metal contacts on the multi-Fin varactors (Figure 3.3c). Ti/Au (100/1200 nm) GSG pads and Ti (40 nm) resistors were defined followed by the deposition of Al_2O_3 (25 nm) passivation layer with atomic layer deposition (ALD). The sample was then patterned with photoresist and underwent a XeF_2 anisotropic silicon etching to remove the silicon nucleation layer in between GaN and AlN substrate. The final structure prior to being released from the QST substrate is illustrated in Figure 3.3d.

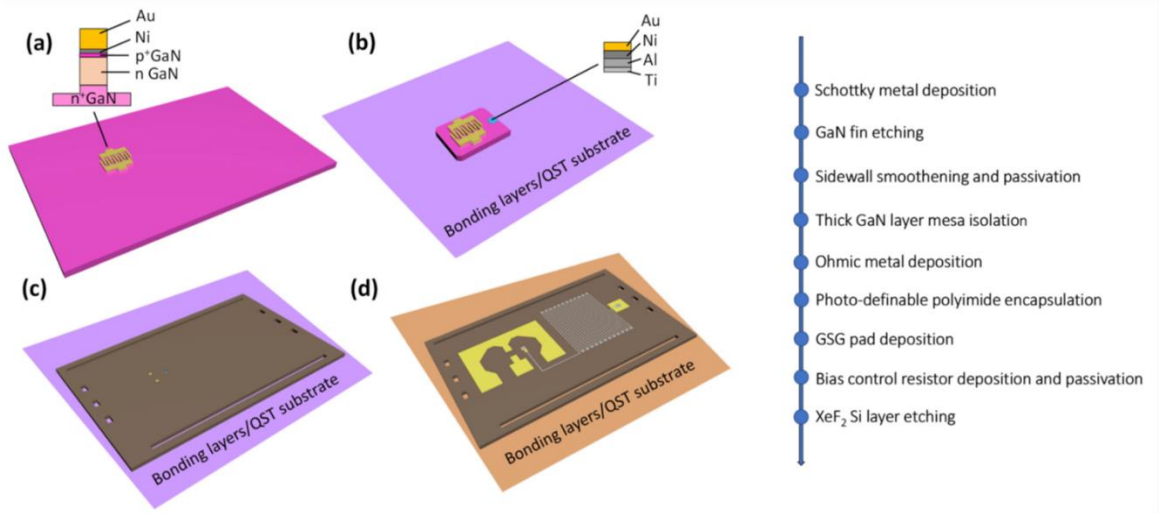


Figure 3.3 Fabrication process flow of the anti-series multi-Fin varactor diodes with interdigitated structure. (a) Definition of Schottky metal Ni/Au and etch GaN Fin with RIE. (b) Smoothening and passivation of GaN sidewalls by TMAH treatment and SiN_x deposition. Deep etching of GaN with RIE for varactor isolation and deposition of Ti/Al/Ni/Au Ohmic contacts atop n^+-GaN. (c) Patterning and curing of photo-definable PI and the formation of vias for metallization to connect to the Schottky/ohmic contacts. (d) Definition of GSG metallization with Ti/Au layers and of snake-shaped Ti resistor followed by ALD Al_2O_3 passivation. XeF_2 isotropic Si etch to remove the underlying Si layer below the diodes.

Figure 3.4a shows a cross-sectional image of our very first device without the XeF_2 release process. Between GaN and poly-AlN, there are AlGaN/AlN buffer layers for GaN growth on a thin silicon layer as well as additional bonding layers that include SiO_2, SiN_x, and silicon. The effect of XeF_2 is delineated in Figure 3.4b, where the XeF_2 gas flows through via holes in the PI layer and laterally etches the silicon layer present at the surface of the poly-AlN substrate. Once this silicon layer is fully etched, the GaN varactors embedded in polyimide levitate from the surface of the substrate. This freestanding structure does not naturally separate from the substrate and remains hinged in the non-XeF_2 etched regions. The top view optical image after XeF_2 etching process is shown in Figure 3.4c, where the contrast allows one to discern levitated and hinged parts of the structures on the substrate.

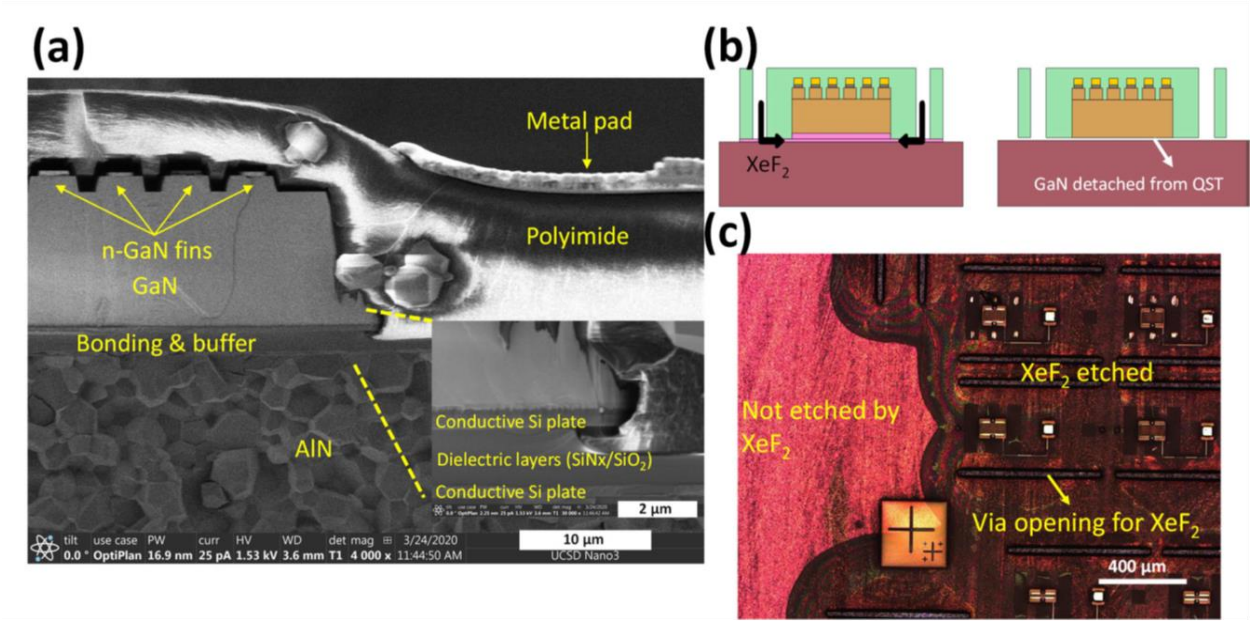


Figure 3.4 Cross-sectional SEM of initial multi-Fin diodes showing PI encapsulation as well as the intermediate layers between GaN and the polycrystalline AlN substrate. (b) Illustration of the varactor release method with XeF_2 flow through the PI vias and lateral etching of the silicon conductive plates. (c) Top view image of a sample exposed to the XeF_2 process.

The conductive silicon sheet under the varactors can lead to additional stray capacitance that compromises their RF behavior. The XeF_2 etching process is necessary to reduce the impact of this center parasitic capacitance, which is supported by both experimental results and by computational analysis. In a two-port S-parameter measurement, the S_{11} curve should lie inside the 50-Ω circle of the Smith chart, as expected for an ideal resistor placed in series with a capacitor because the total resistance is supposed to be higher than 50 Ω. However, a device not processed with the silicon removal by XeF_2 exhibits a signature of high capacitance to ground; S11 does not stay within 50-Ω circle throughout the 100-MHz– 26.5-GHz frequency range. On the contrary, after the XeF2 process, S_{11} lies within the 50-Ω circle, as shown in Figure 3.5a. To further support this analysis, a one port test structure that has the signal pad (input port) connecting to n^+-GaN and ground pad atop PI without connecting to n^+-GaN was fabricated (Figure 3.5b). The capacitance

extracted from S_{11} before and after XeF_2 etching process is plotted in Figure 3.5c. The reduction of capacitance indicates that the center capacitance below varactors can be obviated by eliminating the conductive silicon sheet. A qualitative analysis of the effect of this extra silicon sheet was investigated with ADS Momentum electromagnetic simulation. The simulation results shown in Figure 3.5d indicated that capacitance calculated with buried conductive layer is much higher than that without a conductive layer underneath, in agreement with those experimental results of Figure 3.5c.

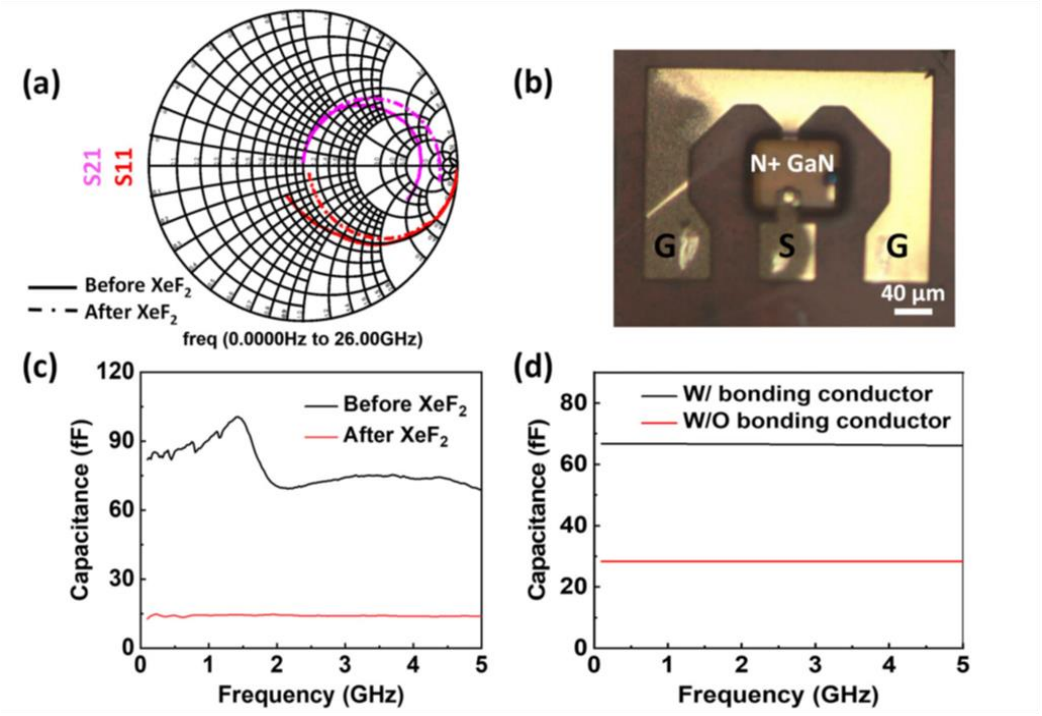


Figure 3.5 (a) Comparison of two-port S_{11} and S_{21} for a device before and after XeF_2. (b) Test structure with n-type ohmic contact at signal pad and open at ground side. (c) One port S_{11} measurement showing that there is lower capacitance after the XeF_2 process. (d) Capacitance extracted by EM S_{11} simulation for the cases of with and without a buried conductor representing the silicon plate on AlN.

The final devices that were released from the QST substrate are shown in Figure 3.6. Figure 3.6a displays a cross-sectional SEM view of the final structure, including Schottky metal, n^-- GaN, n^+-GaN. Both the Schottky metal thickness and the GaN etch depth exceeded 1 µm. The

thick Schottky metal aims to retain low series resistance caused by the metal itself, and at least 1-μm deep GaN trenches confine the signal path in the anti-series configuration to be n^--GaN/n^+-GaN from one Fin capacitor the n^+-GaN/n^--GaN of the second anti-series capacitor. One can also notice from Figure 3.6a that GaN sidewalls are passivated by SiN_x/SiO_2 dielectric layers. SiN_x is too thin to be discerned in the image. The device levitation after XeF_2 etching can be seen in the zoom-out cross-sectional view of Figure 3.6b, where the black contrast at the bottom of the image indicates the absence of any underlying layer. Anti-series (Figure 3.6c) diodes prepared for one-port S-parameter measurements to characterize R_s, C_s, and quality factor and two-port devices for two-tone linearity measurements are shown in Figure 3.6d and 3.6e, respectively.

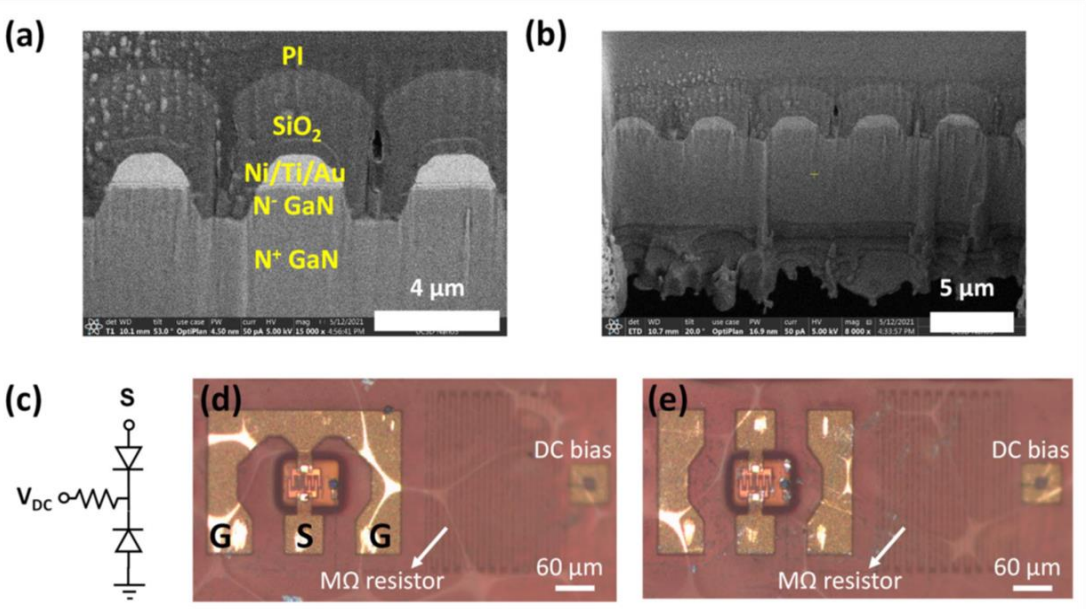


Figure 3.6 (a) Close view of Fins illustrating the structure of the diodes. (b) Another wider field of view SEM showing the device levitation after XeF_2 etch step. (c) Schematic of diodes anti-series connected. (d) One-port devices with GSG pads and a Ti resistor. (e) Two-port devices with GSG pads and a Ti resistor.

3.3 Static Characteristics of Multi-Fin Varactors

The multi-Fin diodes with different fin lengths (20 and 40 μm) and different numbers of fins (5 and 10) exhibited uniform C-V characteristics for 22 devices measured in the voltage range

of 0 to −40 V, as shown in Figure 3.7a. The reverse leakage current density and breakdown characteristics of nonleaky circular and multi-Fin diodes are plotted in Figure 3.7b. In general, we found that the yield of 12 out of 22 multi-Fin diodes was lower than the yield of 19 out of 24 circular diodes. However, for devices that were not leaky, the current density in both configurations was comparable. Additionally, those nonleaky multi-Fin diodes exhibited lower breakdown voltage than the circular diodes attributed to the enlarged electric field at sharp edges in the higher surface area of the multi-Fin structures than that of circular structures. The highest breakdown voltage for the multi-Fin diodes was −146 V, which was lower than −196 V of the circular diodes. This lower breakdown voltage for multi-Fin diodes does not preclude excellent varactor RF performance as will be discussed next.

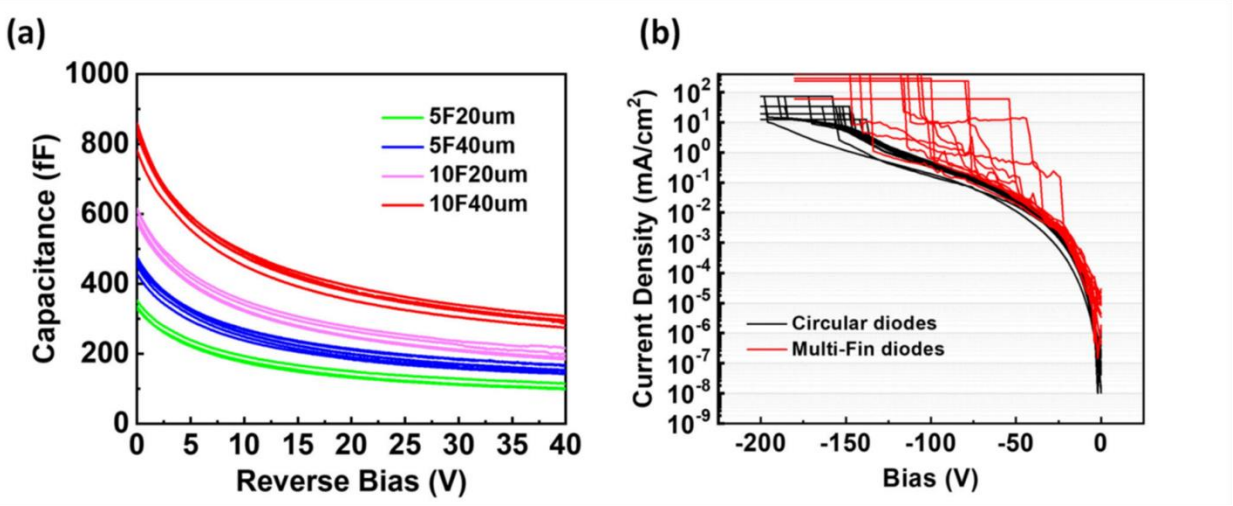


Figure 3.7 (a) CV curves of 22 multi-Fin diodes. Number of Fins and Fin length in four structures are 5 Fins/20 μm, 5 Fins/40 μm, 10 Fins/20 μm, 10 Fins/40 μm. (b) Comparison of reverse bias dependence of leakage current density for between 19 circular diodes and 12 multi-Fin diodes with relative low leakage current.

3.4 One-Port S-Parameter Measurements

The one-port devices for S-parameter measurements with two structures of anti-series multi-Fin diodes of 5 Fins/20 μm and 5 Fins/40 μm were measured and are presented in Figure

3.8. These devices have 3 μm Fin width and 2 μm spacing. The S_{11} measured with an Agilent N5242A network analyzer from 100 MHz to 26.5 GHz under different reverse bias conditions provided by an Agilent E3631A DC power supply is plotted in Smith charts in Figure 3.8a and 3.8b. The modulation of the depletion width in the diodes with reverse DC bias can be confirmed with the bias-dependent traces in the Smith chart figures. The blue curves represent S_{11} under zero bias with a larger capacitance indicating smaller depletion width. The red curves represent a −25 V bias and smaller capacitance corresponding to larger depletion width. The series capacitance expressed as

$$C_s = -\frac{1}{2\pi f Im(Z_{in})} \qquad (3-1)$$

and the series resistance expressed as

$$R_s = Re(Z_{in}) \qquad (3-2)$$

can be extracted from the input impedance that is computed from the S-parameter measurement according to

$$Z_{in} = Z_o \frac{(1+S11)}{(1-S11)} \qquad (3-3)$$

where f is the frequency and Z_o = 50 Ω. Figure 3.9a illustrates the extracted C_s of different devices under 0 and −25-V bias. The capacitance curves were characterized by a convex shape due to the higher contribution of the parasitic inductance to input impedance at high frequencies above 10 GHz. The imaginary part of input impedance can be expressed as

$$Im(Z_{in}) = -\frac{1}{2\pi f C} + 2\pi f L \qquad (3-4)$$

where C and L symbolize the quantities associated with each measurement. From the measurement analysis, we determine an extracted capacitance, C_s, and estimated series inductance, L_s. In order to understand the relationship between C_s, L_s, and Z_{in}, we introduce the estimated capacitance, C_{est},

which represents the ideal capacitance of the diode, C_{est}, assumed to be frequency independent. Moreover, to obviate nonideal effects at the low-frequency regime and the inductance contributions at high-frequency regime, we determined C_{est} values by averaging extracted C_s values in the frequency range of 4–6 GHz and calculated L_s according to

$$L_s = \frac{1}{2\pi f}\left(\frac{1}{2\pi f C_{est}} + Im(Z_{in})\right) \qquad (3-5)$$

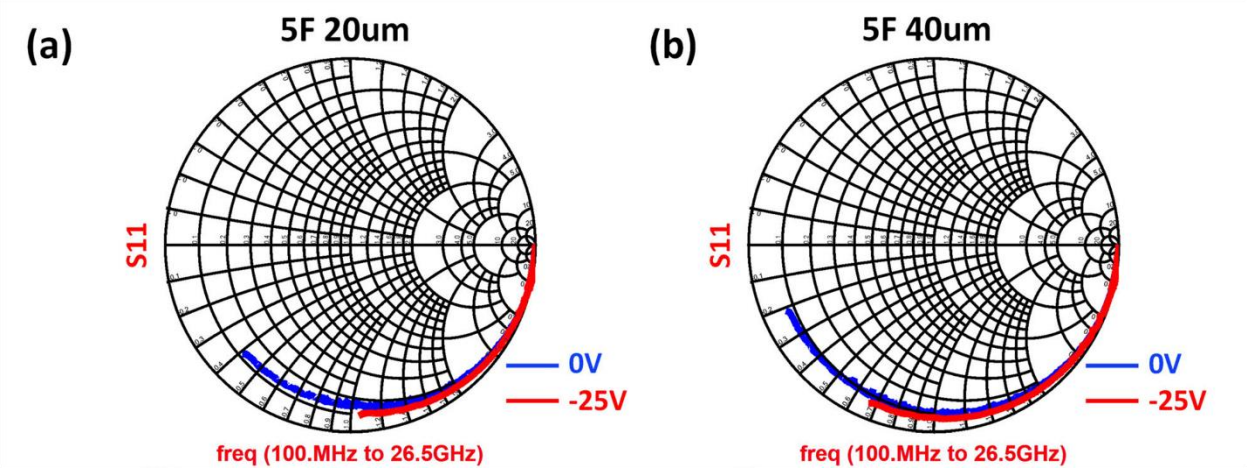


Figure 3.8 (a) 5 Fins/20 μm S_{11} plot in Smith chart for 0- and -25-V bias conditions and (b) 5 Fins/40 μm S_{11} plot in Smith chart for 0- and -25-V bias conditions.

Here, the inductance estimation was expected to be most accurate when the frequency was 26.5 GHz, the highest frequency in our measurements. C_{est} values for 5 Fins/20 μm at 0 and −25 V and for 5 Fins/40 μm at 0 and −25 V were 175, 90, 233, and 124 fF, respectively. Ls calculated at 26.5 GHz for 5 Fins/20 μm at 0 and −25 V and for 5 Fins/40 μm at 0 and −25 V are 80, 80, 89, and 89 pH, respectively. L_s does not scale much with varactor finger length since the metal trace connected to one diode and ground (Figure 3.6d) also contributes to series inductance importantly. Figure 3.9b shows the extracted Rs calculated by $R_s = Re(Z_{in})$, where the frequency-dependent resistance is more prominent at the lower frequencies. With these calculations, we can now

compute the quality factors, which are critical figures of merit of varactors and are calculated according to

$$Q = \frac{Im(Z_{in})}{Re(Z_{in})} \qquad (3-6)$$

as plotted in Figure 3.10a. For both measured devices, the calculated Q values as a function of frequency at −25-V bias voltage are higher than those calculated for a 0-V bias. For a given bias, the Q curves of both devices closely overlap indicating that doubling the Fin length from 20 to 40 μm does not contribute to an increase in the series resistance that compromises Q. The measured Q values at 2 GHz for 5 Fins/20 μm at 0 and −25 V and for 5 Fins/40 μm at 0 and −25 V were 27, 34, 24, and 32, respectively. At 10 GHz, they were 11, 20, 11, and 20, respectively. The plot of Q versus frequency in Figure 3.9a does not exhibit an ideal inverse relationship with the frequency below 5 GHz mainly due to the frequency dependent R_s in our extractions. There are a few possible causes to this nonideality including, but not limited to, parasitic components not understood in these diodes, inaccurate calibration, or phase/magnitude inaccuracy of the Agilent N5242A network analyzer. Another possible parasitic component is the formation of a Ni/non fully depleted p-GaN junction, which could produce large series contact resistance coupled with capacitive components. As-measured multi-Fin diodes exhibited an overall higher series resistance and a lower quality factor than expected at low frequency. To better predict these values and exclude the low frequency nonidealities, we used C_{est} discussed before and R_{est} (R_s extracted at 26.5 GHz) to extrapolate Q for the entire frequency range. The extrapolated quality factor

$$Q_{extrapolated} = -\frac{1}{2\pi f C_{est} R_{est}} \qquad (3-7)$$

is plotted in Figure 3.10b as a function of frequency. This reveals significantly higher Q values in the sub-5-GHz low-frequency regime than those complicated by the measurement nonidealities

and illustrates the potential of our multi-Fin diodes for high-performance varactors. The $Q_{extrapolated}$ values at 2 GHz for 5 Fins/20 μm at 0 and −25 V and for 5 Fins/40 μm at 0 and −25 V were 73, 163, 84, and 181, respectively. At 10 GHz, they are 14, 32, 16, and 36, respectively. Aside from anomaly in the behavior of the series resistance at low frequency, the extracted series resistance at high frequency appears to be the main limitation in this set of varactor diodes. Specifically, in the optimal operating regime with a varactor impedance of 50 Ω, the operating frequency is approximately 3 GHz for a 1-pF varactor capacitance. At this frequency, the extrapolated Q is 56 at zero bias, which is not optimal for various applications.

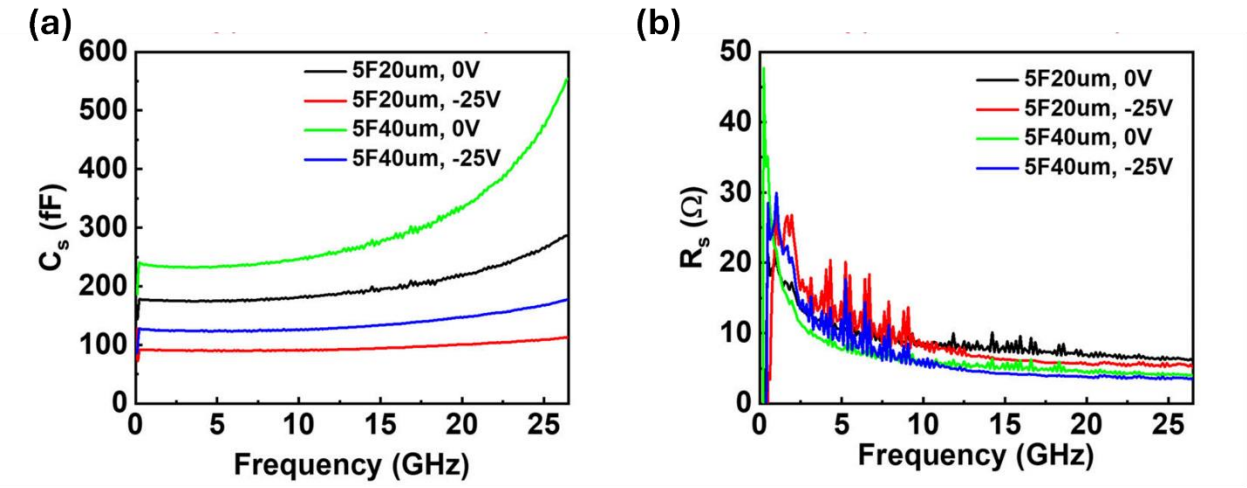


Figure 3.9 (a) Capacitance values for different devices and bias conditions calculated using $Im(Z_{in})$. (b) Series resistance values of different devices and bias conditions extracted from $Re(Z_{in})$.

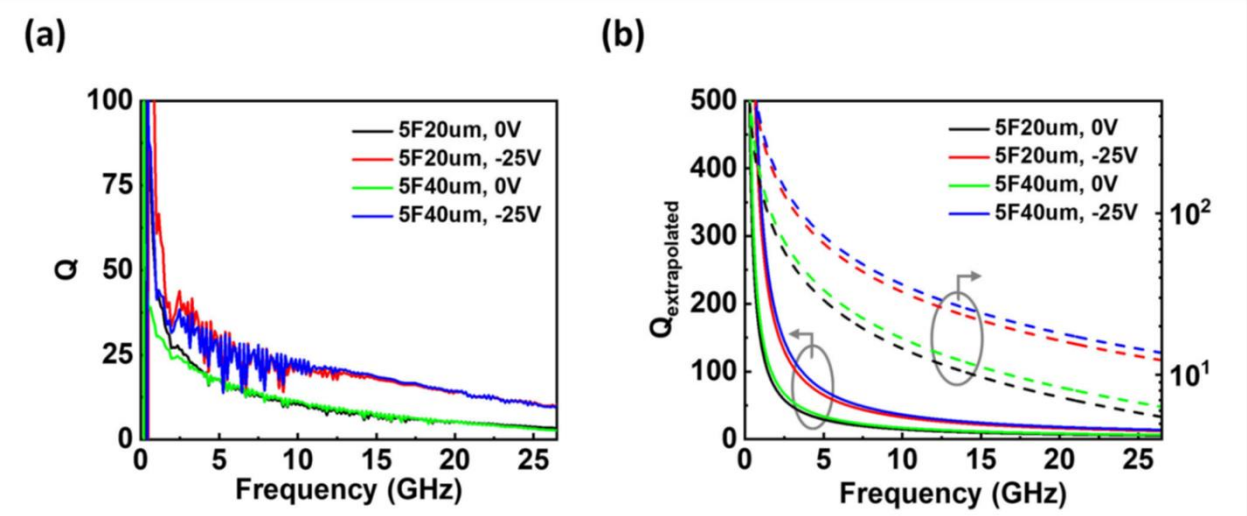


Figure 3.10 (a) Q versus frequency plot calculated using the measured $Im(Z_{in})/Re(Z_{in})$. (b) $Q_{extrapolated}$ versus frequency plot by estimating the capacitance and the series resistance and by excluding the series inductance and nonideal effects causing frequency dependent R_s.

To explore the possible origins of the series resistance and deduce possible mitigation strategies, we used ADS Momentum EM simulation. The Schottky metal resistance (R_M), the non-depleted n^--GaN resistance (R_{n-}), and the n^+-GaN resistance (R_{n+}) contributions were calculated for two cases for the n^--GaN mobility of 1) 300 and 2) 500 cm^2/V-s. Based on measurements for test device structures, we used an empirical conductivity of 1.4×10^7 S/m for the Schottky metal and an empirical resistivity of 8100 S/m for the n^+-GaN in the simulation setup. Table 3.1 shows the ratio of the three resistance components, R_M, R_{n-}, and R_{n+} to the total series resistance, R_{tot}, where both R_{n-} and R_{n+} appear to dominate R_{tot}. Therefore, to further improve Q, both the mobility of the n^--GaN layer and the conductivity of the n^+-GaN need to increase in the epitaxial structures that form the varactor diodes.

Table 3.1 Series resistance contribution from R_M, R_{n-}, and R_{n+} to R_{tot}.

	R_M/R_{tot} (%)	R_{n-}/R_{tot} (%)	R_{n+}/R_{tot} (%)
$\mu_{n\text{-}GaN}$ 500 cm^2/V-s	2.4	52.4	45.2
$\mu_{n\text{-}GaN}$ 300 cm^2/V-s	1.9	62.8	35.3

3.5 Two-Tone Linearity Measurements

Figure 3.11 illustrates the setup used for the two-tone linearity measurement setup designed specifically for determining the output third order intercept point (OIP3) measurements. In this setup, two fundamental tones, namely, 1.995 GHz and 2.005 GHz, were directed toward power amplifiers which offered high input power, enabling the detection of third order intermodulation product (IM3) by the spectrum analyzer. A power combiner was connected to the spectrum analyzer, with our anti-series varactor shunted to ground. The nonlinearity of the varactor was assessed by measuring the reflective power from the varactor to the spectrum analyzer. To understand the limitations of our setup, we conducted two-tone measurements without a T-connector, a bias tee and a varactor. This configuration shorted the power combiner to the spectrum analyzer. The IM3 versus output power of fundamental tone is depicted in Figure 3.12. The findings indicated the necessity of power amplifiers and isolators. In our case, two isolators were placed after each power amplifier and before a power combiner to ensure unidirectional transmission. Using only one isolator for each power amplifier resulted in higher IM3 in the spectrum analyzer. Lines difference from the same setup (blue lines: isolators and power amplifier) was due to different input power. This is because under a fixed dynamic range of the spectrum analyzer, measurable OIP3 is larger. That is, it's preferable to conduct two-tone measurement with higher but clean input power for the fundamental tones. In the figure, the highest OIP3 is noted to be 56 dBm. Any devices that have higher OIP3 cannot be confirmed by this setup. We tried to increase input power using different power amplifiers, but either the power amplifiers saturated too early or excessively large signal were distorted by spectrum analyzer. Later, two-tone signals, 1.93 GHz and 1.97 GHz were directed to the system with the incorporation of an attenuator and a notch filter to minimize fundamental-tone power reaching the spectrum analyzer as shown in

Figure 3.13 and 3.14. The purpose was to attenuate f_1 and f_2, so the measurement is not conducted at the dynamic range limit of the spectrum analyzer. Since the highest OIP3 observed when probing on OPEN pads (Figure 3.13) matched the measured OIP3 when probing on the devices (Figure 3.14; multi-Fin configuration; 0 V), we estimated that the minimum OIP3 (0 V) of our multi-Fin varactors exceed 54 dBm with 1.93 GHz and 1.97 GHz. Power amplifiers with higher and more linear output power will be necessary for more accurate IP3 determinations.

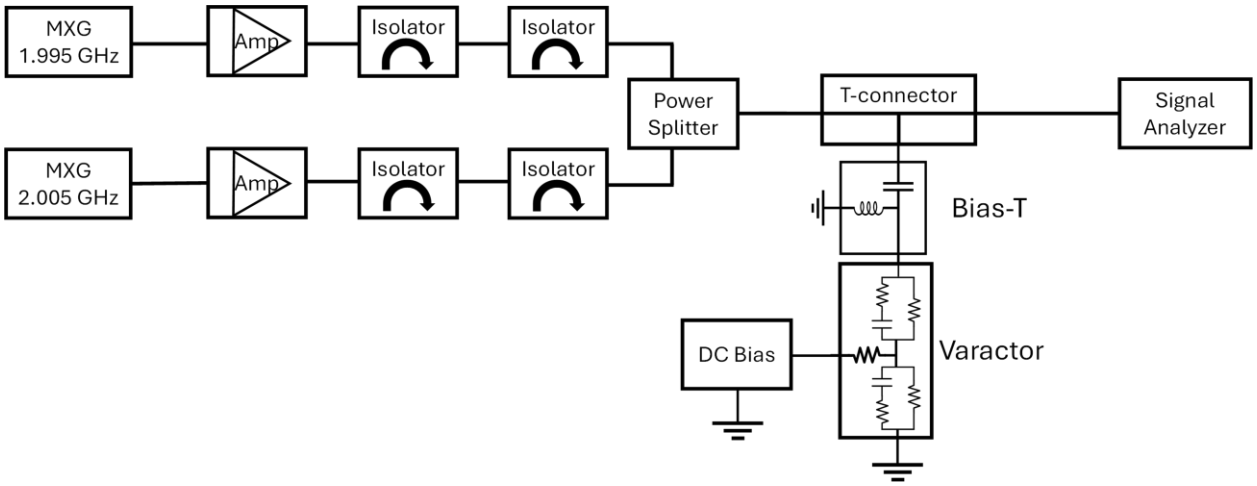


Figure 3.11 Block diagram for the proposed two-tone test of reflective power from the varactor.

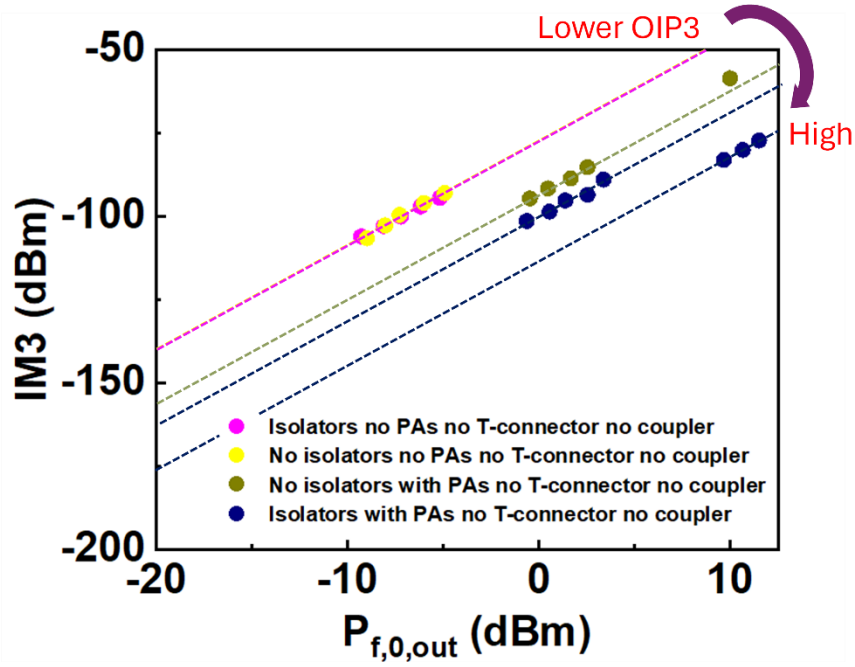


Figure 3.12 Comparison for different two-tone test setup when the T-connector side is left open.

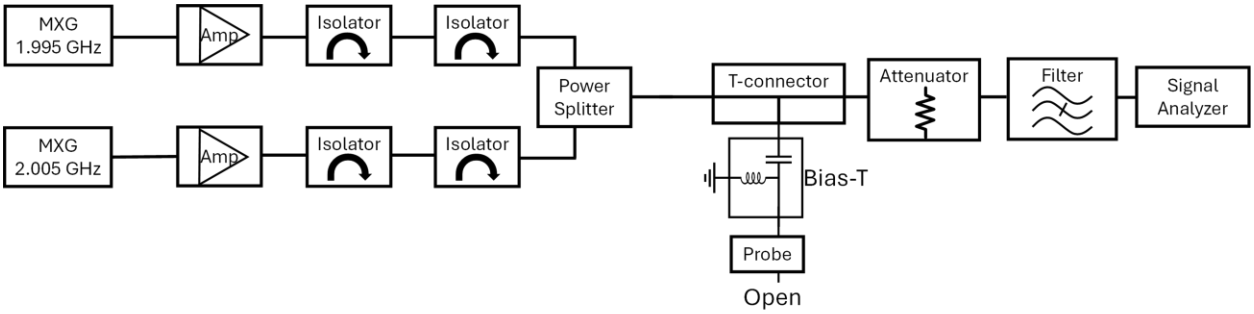


Figure 3.13 Block diagram when the T-connector is connected to a bias-T with RF probes to open.

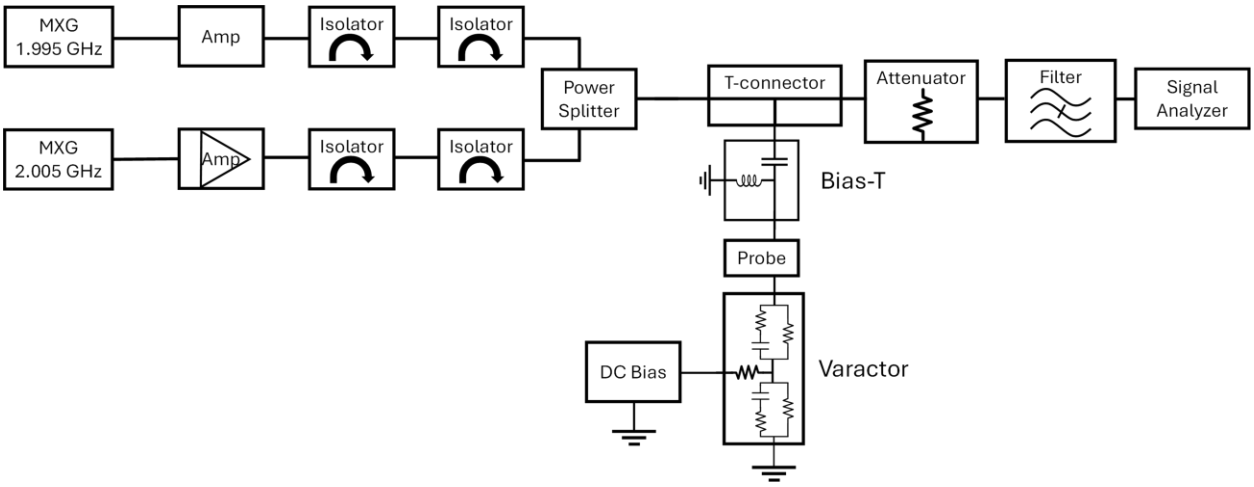


Figure 3.14 Block diagram when the T-connector is connected to a bias-T with RF probes to open.

3.6 Microwave Power Varactors Projected Benchmark

To better understand the potential of GaN-based camel diodes for power varactor applications, we compare this work with other varactor technologies using different figures of merit and criteria. For a power varactor, it is crucial to provide a wide tuning range with a high input power. When the input power is high, we need to operate the varactors with a negative bias voltage to avoid driving the varactor diode to the forward bias regime with the ac swing. This results in a maximum operating capacitance (C_{max}) that is smaller than the highest achievable capacitance at 0 V. Additionally, we need to operate the varactor at a minimum operating capacitance (C_{min}) that is higher than the minimum achievable capacitance, so that the signal voltage amplitude added to the reverse bias does not lead to reverse voltage breakdown. A schematic of C_{max} and C_{min} definitions can be found in Figure 3.15. Using these definitions, we computed a small signal tuning ratio of 5 in the bias range of 0 to −100 V, and the highest DC voltage we were able to apply in our CV characterization setup with small signal voltage amplitude of 100 mV. We note that a small signal tuning ratio of 6.4 is expected in the bias range of 0 to

−138 V, where punch through occurs for the 1-μm drift layer. Figure. 3.16 exhibits effective tuning ranges as a function of superimposed signal voltage amplitudes for different power varactor technologies. Our diodes demonstrate a high tuning range throughout the whole voltage amplitude span. Table 3.2 summarizes key metrics that evaluate the performances of power varactors. The varactor figure of merit (VFOM) accounts for tuning range, for Q, and for power handling at the desired signal frequency of operation and is determined as follows:

$$VFOM = (TR - 1) f V_{max} Q_{min} \quad (3-8)$$

where TR is the tuning ratio, f is the frequency of operation, V_{max} is the punchthrough voltage, and Q_{min} is the quality factor without applied reverse voltage bias. Our varactors exhibited high tuning ratio with a wide range of voltage amplitudes, higher punchthrough voltages, and highest breakdown voltages with superior quality factors, which result in better VFOM than the existing SiC,[57,58] GaAs,[59] and GaN[30] microwave power varactors, as shown in Table 3.2. The GaN camel diode varactors offer concurrent high cutoff frequency and high tuning range compared to other high-power varactors technologies. This is illustrated in Figure 3.17, which plots the cutoff frequency as a function of small signal tuning range for a variety of varactor technologies including the projected valued for our GaN camel diode like varactors.[31,35,58-66] In conclusion, GaN-based camel diode varactors are promising to facilitate more RF adaptive circuit applications, where high-power signals are transmitted.

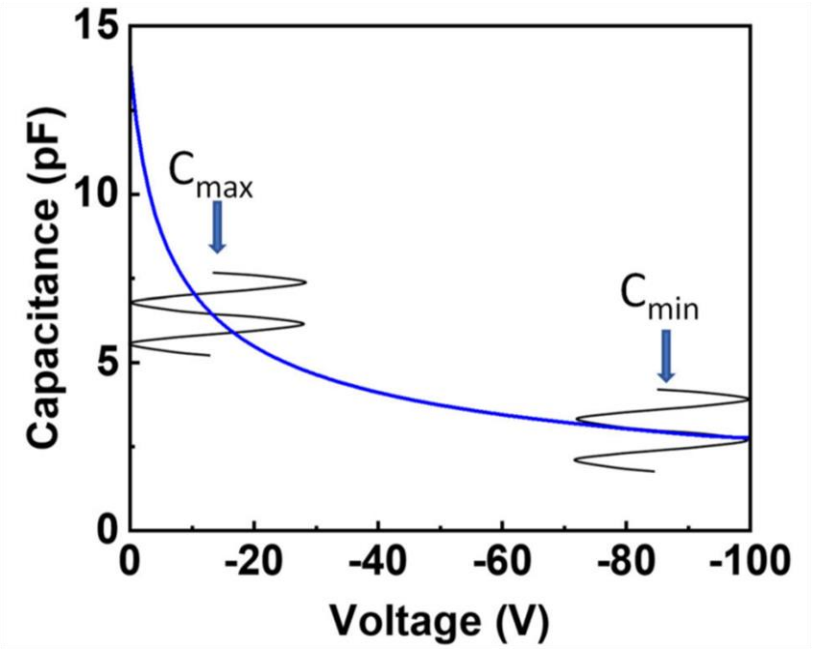


Figure 3.16 Schematic illustrating the method for determining C_{max} and C_{min} on C-V_{rev} with reverse bias ranging from 0 to 100 V. Measured under circular diode configuration.

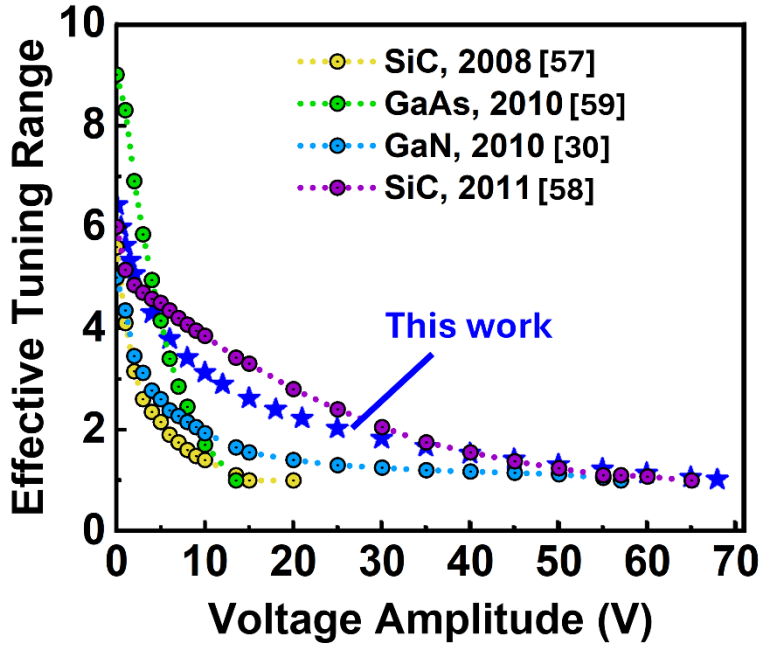


Figure 3.15 Comparison of power varactor technologies for capacitance tuning range versus superimposed signal voltage amplitude.

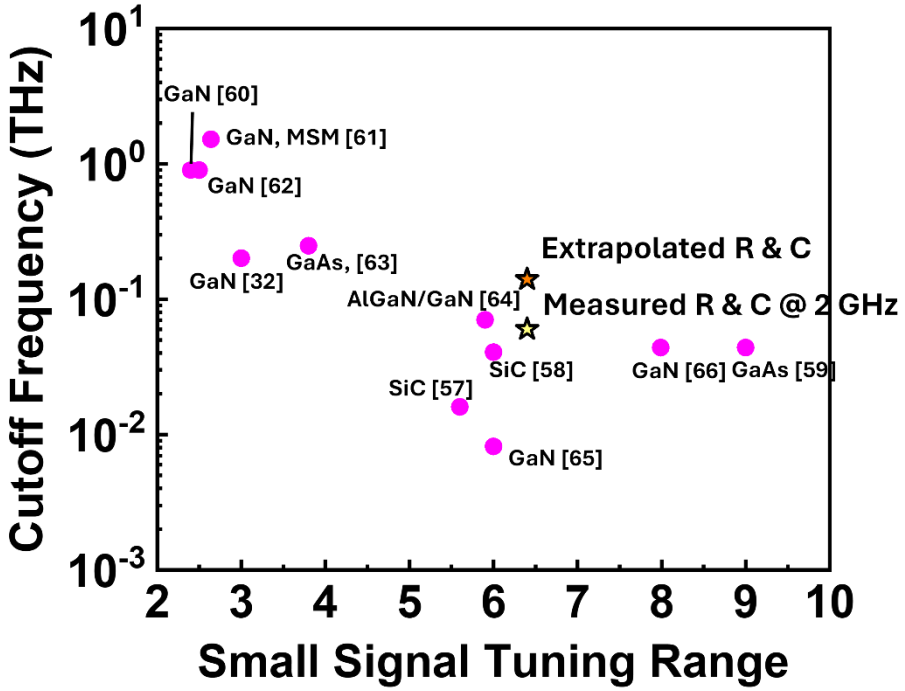


Figure 3.17 Comparison of different varactor technologies for their cutoff frequency versus small signal tuning range.

Table 3.2 Comparison of key FOMs for microwave power varactors.

Technology	SS Tuning	Punch-Through	Breakdown (V)	Q_{min}	Q_{max}	VFOM
SiC [57, @ 2GHz]	5.6/1	15	40	8	45	1100
GaAs [59, @ 2GHz]	9:1	15	28	22	150	5280
GaN [30, @ 1GHz]	5:1	N.A.	120	N.A.	>35	<16800
SiC [58, @ 2GHz]	6:1	60	>150	20	160	12000
1st generation [@ 2GHz]	6.4:1	138 (expected)	Circular: 196 Multi-Fin : 146	>30 (measured) >70 (extrapolated)	N.A. >420	44700

3.7 Key device design and process optimization

The finalized device structure is detailed in sections 3.2 to 3.4. This section will explore the evolution of process steps and device structure. In our initial batches of multi-Fin varactors, we encountered nonideal S-parameters from two-port measurements. The s-parameter results implied the existence of center parasitic capacitance. We conjected that this center parasitic capacitance was due to imperfect n+ GaN isolation etching at the time then optimized the isolation

etching process. After improving GaN isolation, we still observed similar S-parameter characteristics, indicating continued presence of center parasitic capacitance as shown in Figure 3.18. To pinpoint the source of the parasitic capacitance, we attempted to replicate the measurement results as closely as possible using ADS circuit simulation. In the simulation, instead of aligning simulated s-parameters with measured results on a smith chart, we tried to fit the extracted quality factors, and the quality factor is calculated by:

$$S11^{*} = S11 - \frac{S12 \times S21}{1 + s22} \qquad (3.9)$$

$$Z_{in} = 50 \times \frac{(1 + S11^{*})}{(1 - S11^{*})} \qquad (3.10)$$

$$Q = -\frac{imag(Z_{in})}{Real(Z_{in})} \qquad (3.11)$$

Figure 3.19a shows the simulation configuration of a device with 5 fingers and finger length of 23μm. The black frames are the serial resistance and capacitance components which should correspond to real varactor diodes. The serial capacitance put into the simulation under different bias was determined by the C-V characteristics. To keep the similar Q while increasing the bias, we had to keep serial resistance the same. Figure 3.19b and 3.19c show the extracted Q from measurement and simulation, respectively. We also simulate the design of with 12 fingers and finger length of 46μm. The simulation setup and extracted quality factors are shown in Figure 3.20. The major changes in this configuration are the serial R and C, and the values of center capacitance and the serial resistance. By normalizing the center R & C (R=800 Ω, C=1000 fF in Figure 3.19a) with area, we obtained R=349 Ω and C=2300 fF for the larger design as shown in Figure 3.20a. The extracted Q based on simulation fit those extracted by measurement. Based on these studies, we conjected two main issues with our early design. The first is the center parasitic resistance and capacitance coming from the backside of the diodes, and the second issue is the overall high series

resistance. Before applying XeF_2 process for center parasitic removal, we tried another approach, the bonding dielectric layer wet etching as displayed in Figure 3.21. By using this method, we could separate the conductive silicon plates. The devices were encapsulated in polyimide film and released from the substrate then transferred to water, followed by RIE etching from the back for silicon layer removal and sample fixation on a glass slide. Figure 3.22a and 3.22b are a photo of a released sample and a microscope image for a released sample. This wet etching approach was later replaced by XeF_2 etching process due to process complexity and inferior yield.

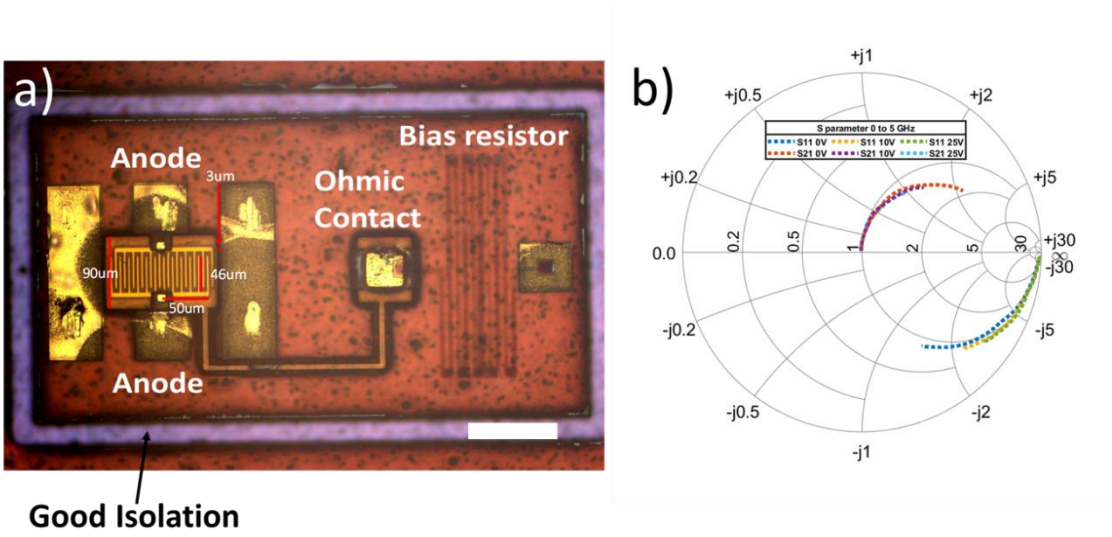


Figure 3.18 An early batch of multi-Fin diode varactor with good isolation. (a) Optical image of a varactor with 12 Fins and 46 μm length. (b) S-parameter measurement results from 0 to 5 GHz under reverse bias of 0V, 10V, and 25V.

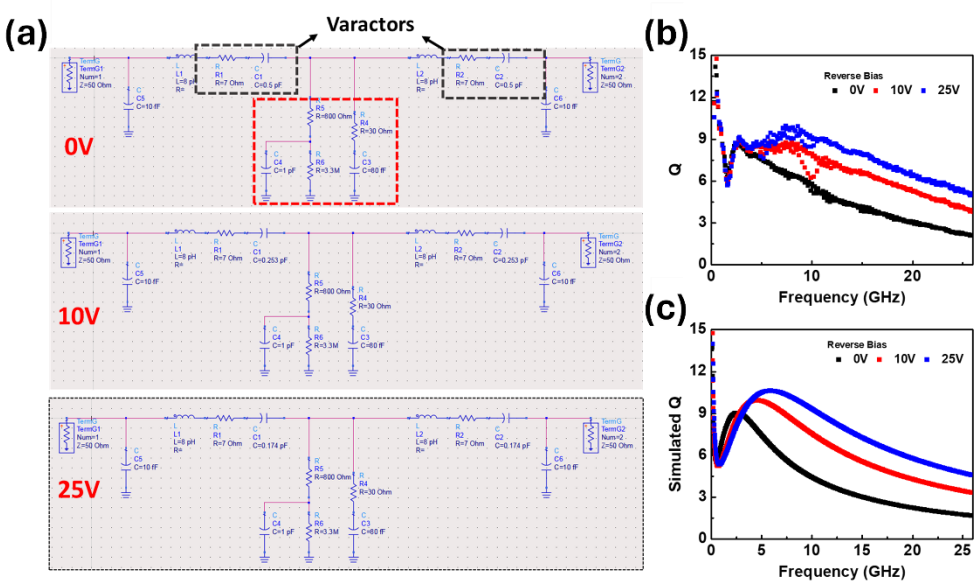


Figure 3.19 Simulation of a 5 finger, finger length of 23μm device. (a) Circuit setup under reverse bias of 0V, 10V, and 25V. (b) Extracted Q based on s-parameter measurement results from 0 to 26 GHz under reverse bias of 0V, 10V, and 25V. (c) Extracted Q based on ADS simulation from 0 to 26 GHz under reverse bias of 0V, 10V, and 25V.

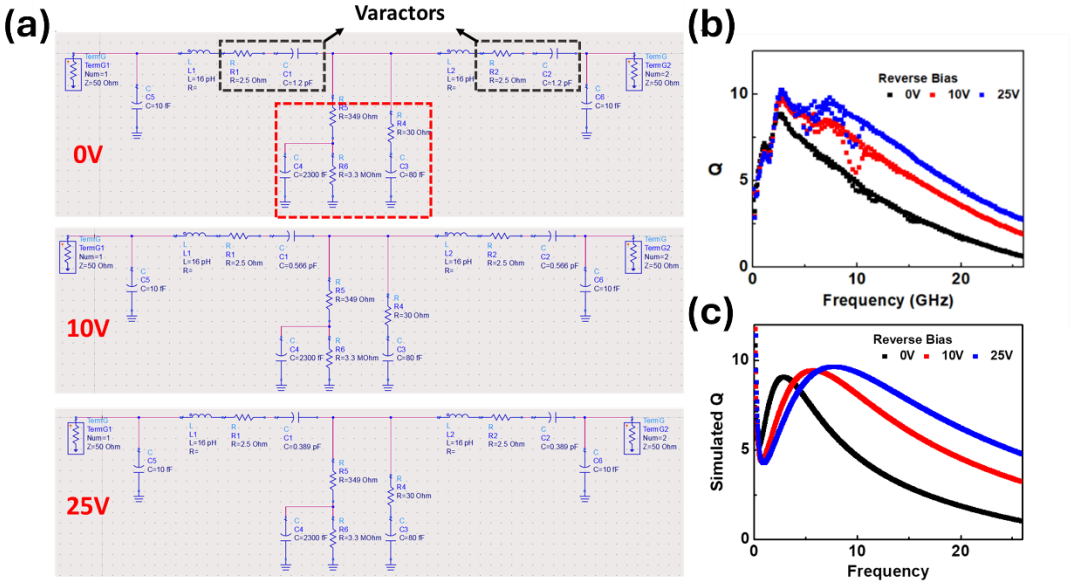


Figure 3.20 Simulation of a 12 finger, finger length of 46μm device. a) Circuit setup under reverse bias of 0V, 10V, and 25V. b) Extracted Q based on s-parameter measurement results from 0 to 26 GHz under reverse bias of 0V, 10V, and 25V. (c) Extracted Q based on ADS simulation from 0 to 26 GHz under reverse bias of 0V, 10V, and 25V.

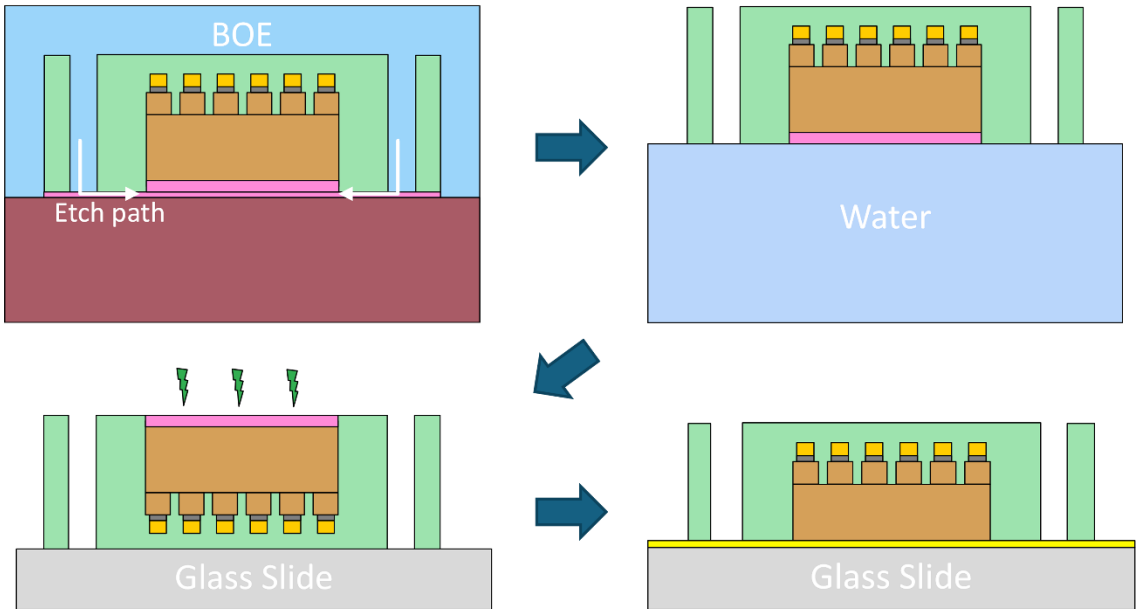


Figure 3.21 Process flow of BOE method used to release devices.

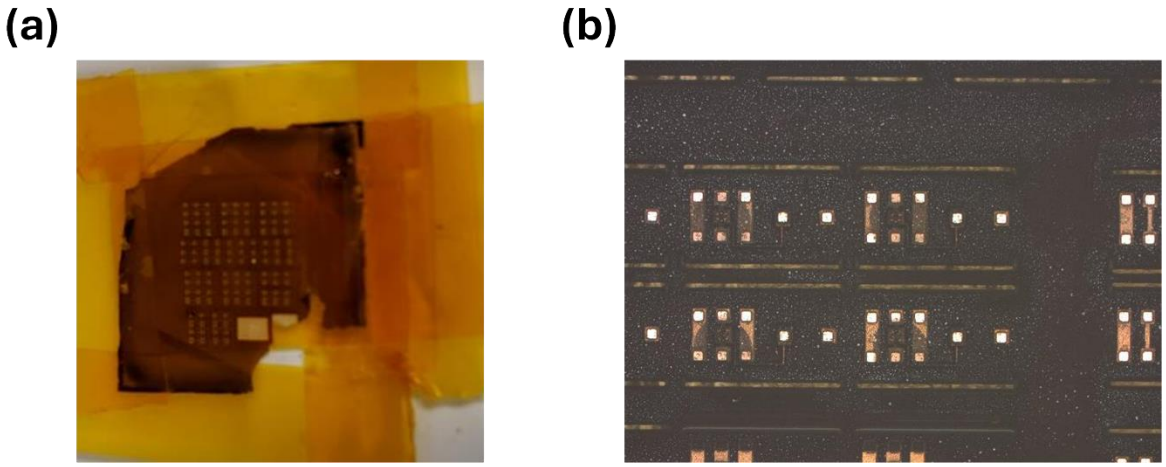


Figure 3.22 (a) Photo of a BOE released sample. (b) Optical microscope image of a BOE released sample.

In our early multi-Fin varactor design, we referred to our circular diode process since the process was optimized. Instead of Ni fully covering the fins (Figure 3.6a), p^+-GaN layer with Ni contact only occurred at the center of a Fin (Figure 3.4a). Apart from the RC effect from the backside of devices, we attribute the high series resistance to RC leakage throughout the diode

itself. Three potential physical causes, non-depleted p^+-GaN at Fin edges, traps at etched Fin sidewalls, and traps in p^+-GaN layers, are illustrated in Figure 3.23. We addressed these concerns with TMAH treatment followed by SiN_x passivation and realign GaN etching without exposed p^+-GaN as shown in Figure 3.24. Device characteristics were improved significantly after these modifications.

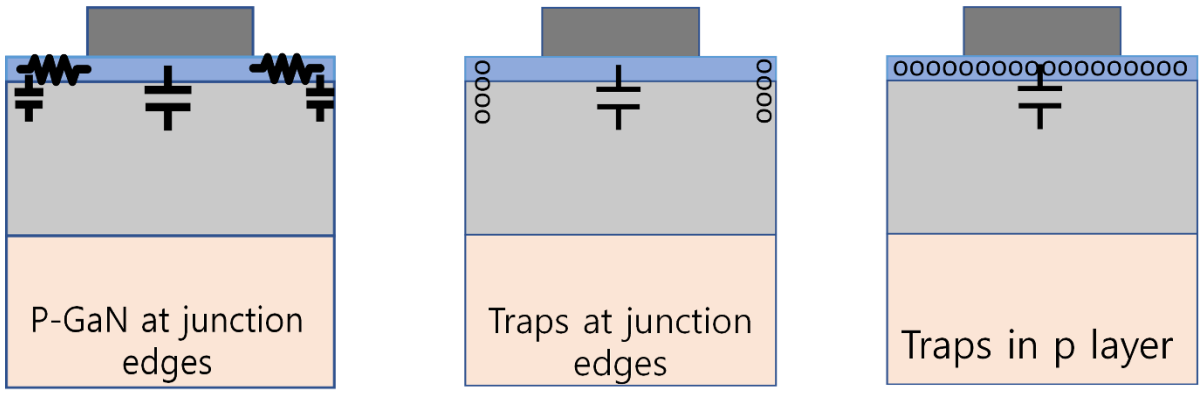


Figure 3.24 Possible causes for the RC leak through the devices.

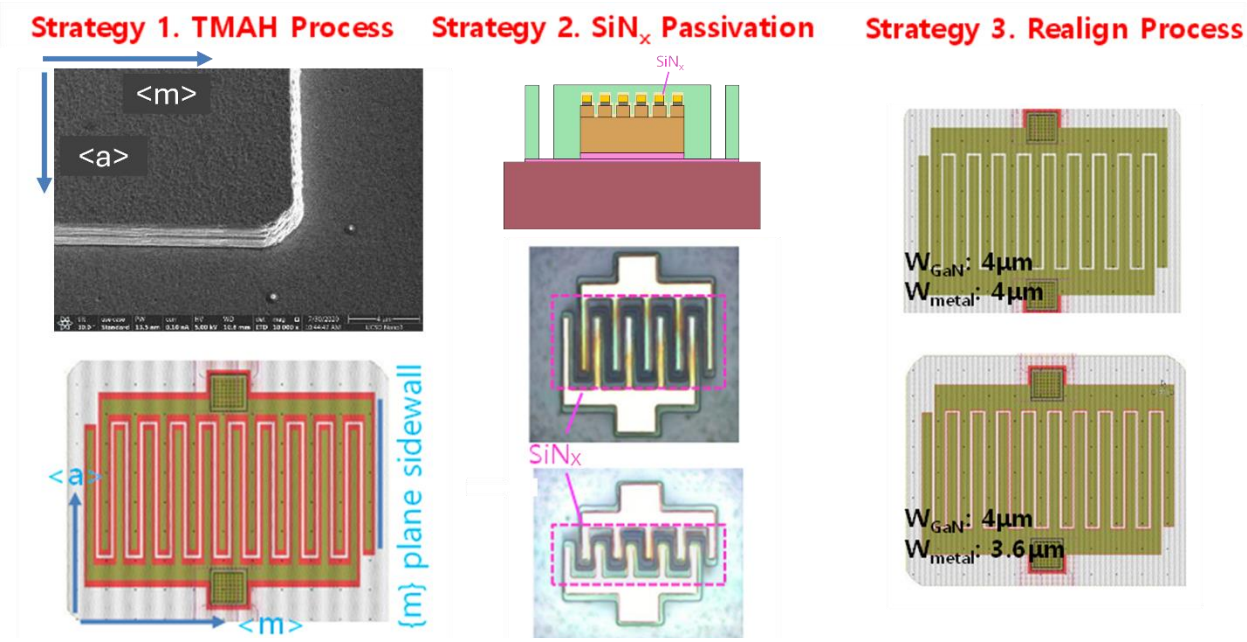


Figure 3.23 Strategies applied in our final process.

3.8 Conclusions

In summary, we demonstrated ideal RF characteristics based on empirical results derived from circular diodes by ADS circuit simulation. We fabricated multi-Fin diodes in anti-series configuration and optimized device fabrication process flow and structure was optimized to mitigate parasitic effects. Static electrical characterizations were also carried out. Also multi-Fin diodes generally exhibited a lower breakdown voltage and lower yield than circular diodes, the least leaky multi-Fin diode demonstrated decent power handling capabilities. These multi-Fin devices could achieve Q_{min} greater than 30 at 2 GHz as determined by one-port S-parameter measurements. Our two-tone linearity measurement suggested that the OIP3 at 0 V under anti-series configuration exceeded 54 dBm. More accurate linearity measurements will require higher input power with decent linearity. P^+-GaN layer in our wafer may be too thick to be fully depleted, resulting in nonideality such as series resistance varying with operating frequency. Despite some discrepancies arising from the wafer itself and measurement artifacts, these devices represent the proof of concept, showing significant potential of GaN camel diodes, which outperform other technologies for power varactor applications.

Chapter 3, in part, is a reprint of the materials as it appears in *IEEE Transactions on Electron Devices* 2023. P. C. Chen, P. M. Asbeck, and S. A. Dayeh. The dissertation author is the first author of this paper.

CHAPTER 4: Multi-Fin Varactors: 2nd Epi-Layer

4.1 Epitaxial Layers Comparison: 1st vs. 2nd

Our inference about p^+-GaN layer thicker than expected was confirmed by secondary ion mass spectrometry (SIMS). Figure 4.1a reveals the magnesium concentration in the wafer processed for our circular and multi-Fin diodes discussed in Chapter 2 and 3. While more intricate material and electrical characterizations are necessary to precisely ascertain the thickness of the p^+-GaN layer, a rough estimation can be made. Assuming a 5% to 10% Mg activation rate, p^+-GaN layer thickness of the wafer is around 40 nm, elucidating high series resistance at low frequencies. Additionally, a sample wherein the top 100 nm GaN was etched away was fabricated for SIMS measurements. Figure 4.1b portrays the depth profile of silicon concentration. The measured n^--GaN Si concentration concurs the effective carrier concentration, 1.5×10^{17} cm^{-3}, as extracted in Chapter 2. Based on these findings, the layer stack of our first-generation wafer is approximately 40 nm p^+-GaN/1070 nm n^--GaN/5566 nm n^+-GaN. The electrical and material analysis reveals two critical shortcomings of the 1st generation wafer. Firstly, thicker p^+-GaN than anticipated, and secondly, conductive silicon layers sandwiched between GaN and the poly-AlN substrate. Subsequently, we designed new GaN/QST epi-layers with thinner p^+-GaN, higher n^+-GaN doping concentration, and semi-insulating silicon layers. However, the silicon concentration (6×10^{17} cm^{-3}) within the n^--GaN drift layer in the revised wafer was four times higher than designed (1.5×10^{17} cm^{-3}). We concluded that doping concentration control required more optimization with semi-insulating silicon on QST wafers, so returned to the GaN/QST under conductive silicon plates configuration. SIMS measurements were also carried out for the second-generation wafer with conductive silicon plates. Figure 4.2a showcases the depth profile of Mg concentration, indicating thinner p^+-GaN than 1st generation. Moreover, a 100 nm etched sample

via SIMS implies thinner drift layer in the received 2nd generation wafer, as illustrated in Figure 4.2b. The structure of our second-generation wafer can be outlined as approximately 25 nm p^+-GaN/675 nm n^--GaN/5535 nm n^+-GaN.

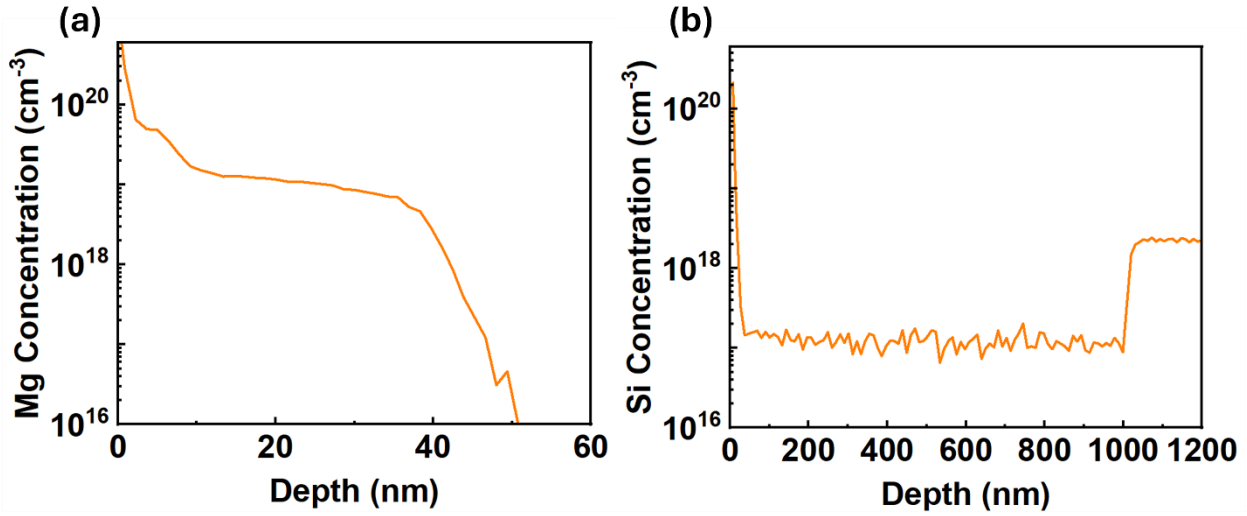


Figure 4.1 1st generation doping profiles. (a) Mg concentration vs. depth. (b) Si concentration vs. depth for a 100 nm etched sample.

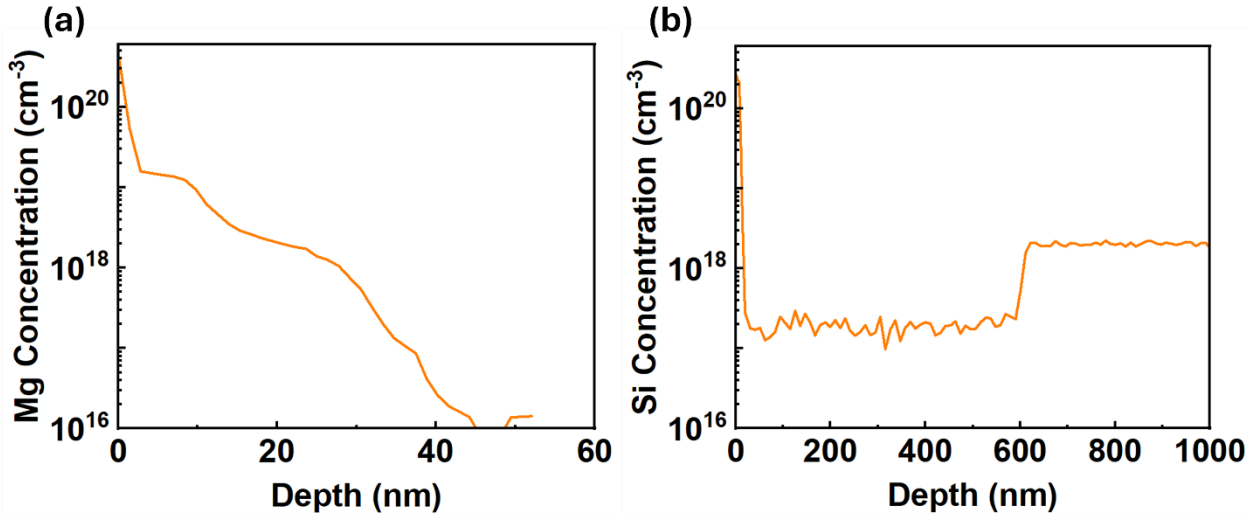


Figure 4.2 2nd generation doping profiles. (a) Mg concentration vs. depth. (b) Si concentration vs. depth for a 100 nm etched sample.

4.2 Static Characteristics Comparison

Like Chapter 2, we fabricated circular diodes on diced coupons from the 2nd generation wafer. These samples exhibited generally higher reverse leakage current than the 1st generation. Some leaky devices demonstrated leakage currents three orders of magnitude higher than those of the 1st generation, while the less leaky ones are also a few times leakier than the 1st generation. Figure 4.3a exhibits current density versus reverse bias for the less leaky devices spanning from 0 V to -40 V. Reverse current density at -10 V for most devices ranged from 10^{-4} to 10^{-3} A/cm^2. Only two devices showed leakage current density lower than 10^{-4} A/cm^2 at -10 V. Conversely, most devices from 1st generation showed leakage current density lower than 10^{-4} A/cm^2 (Figure 2.7). Figure 4.3b presents the average current density versus reciprocal of anode radius, suggesting that larger devices possess more leakage paths than their smaller counterparts, with the path unrelated to fabrication process. Though the expected lower barrier height from thinner p^+-GaN aligns with higher leakage current, the lower yield and the tendency for larger devices to perform leaky nature may also suggest that the 2nd generation wafer inherently contains more defects.

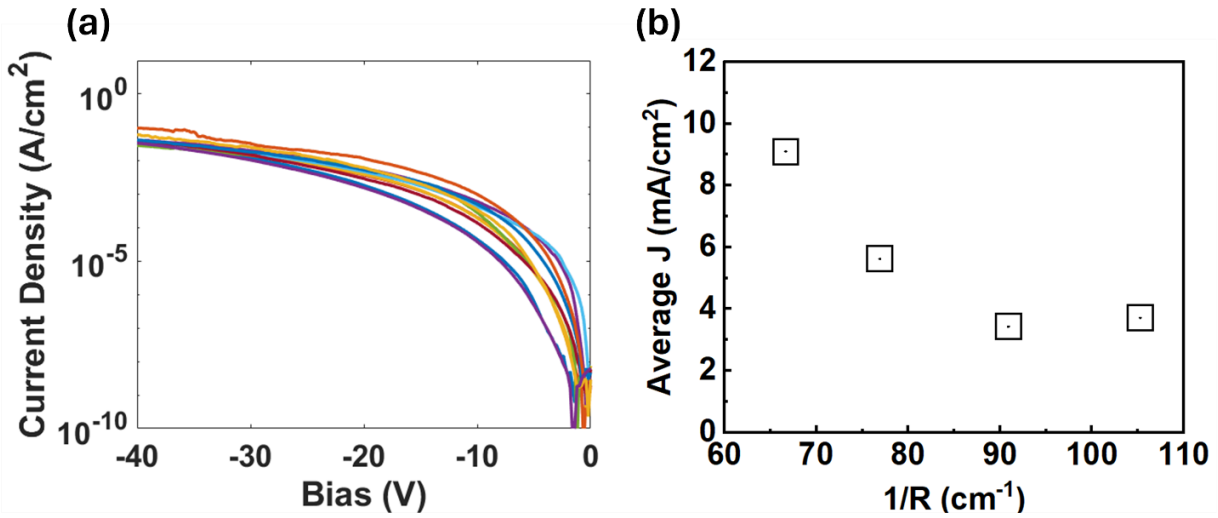


Figure 4.3 (a) J_{leak}-V_{rev} of circular diodes fabricated with 2nd generation wafer. (b) Average current density dependence with anode radii of 95 μm, 110 μm, 130 μm, 150 μm.

A forward bias characteristics comparison between a Schottky diode, 1st generation, and 2nd generation are displayed in Figure 4.4. Devices manufactured from the new wafer have lower turn-on voltage than the 1st generation, exhibiting characteristics akin to camel diode configuration where the turn-on voltage is typically smaller than 3.4 V. Despite low yield, capacitance modulation could still be attained for good devices. C-V_{rev} characteristics for different sizes (95 μm, 110 μm, 130 μm, 150 μm for anode radii) are shown in Figure 4.5a. For devices with 95 μm radius, C_{0V} are around 15 pF and 18.8 pF for 1st and 2nd generations, respectively, corresponding with depletion width around 167 nm and 133 nm. From $1/C^2$-V_{rev} (Figure 4.5b), we extracted carrier concentration for n^--GaN and built-in voltage (V_{bi}). The average Si concentration in the drift layer was found to be 1.78×10^{17} cm^{-3}, consistent with SIMS results. On the other hand, the average V_{bi} is 2.91 V. Both forward bias I-V and reverse bias C-V implies a higher likelihood of full depletion of p^+-GaN for 2nd generation than 1st generation wafers.

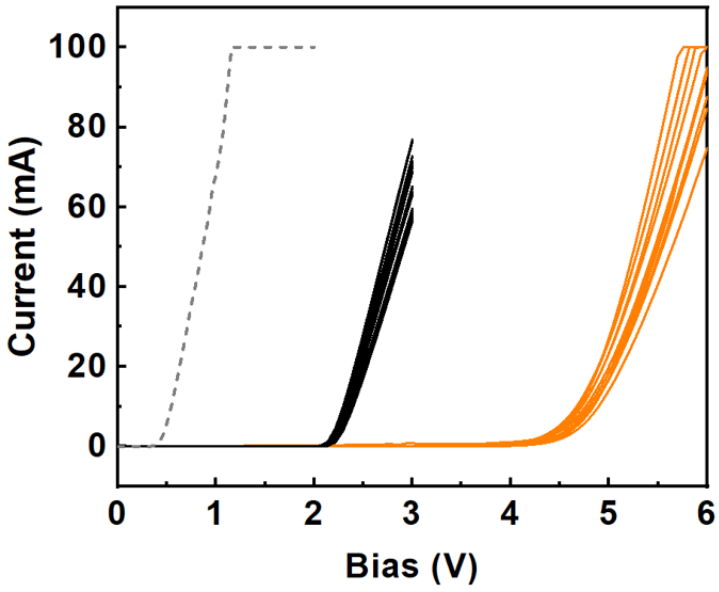


Figure 4.4 I-V turn-on characteristics of a Schottky diode and 1st epi (orange) and in 2nd epi (black).

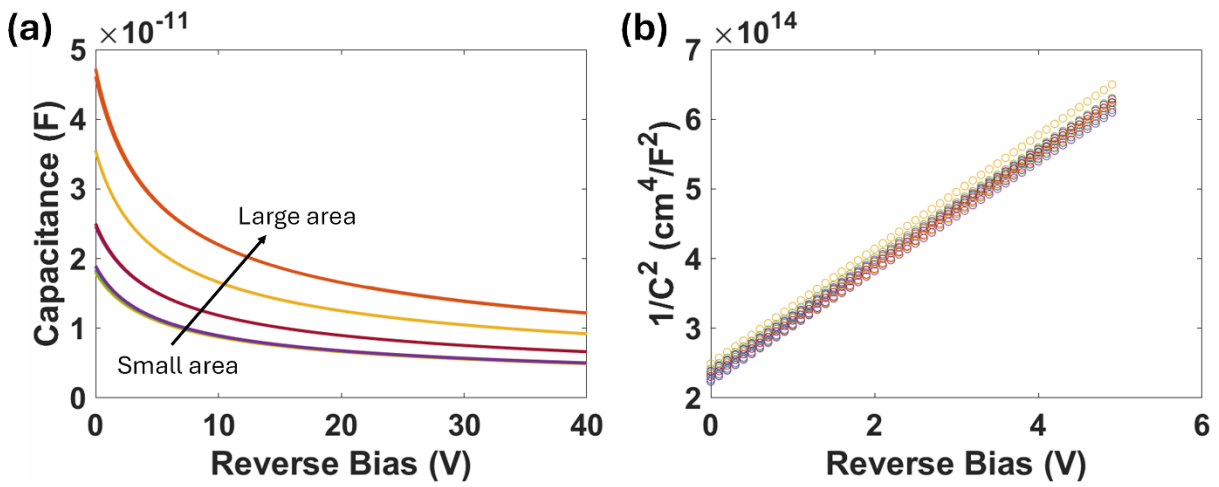


Figure 4.5 (a) Measured C-V_{rev} characteristics of diodes and (b) Plot of $1/C^2$ versus V_{rev} and the extracted N_{eff} of diodes from normalized with diode contact area.

Though it's preferrable that 2nd generation diodes possess thinner p^+-GaN layer compared to the 1st generation, the reduced drift layer compromises both power handling capability and tuning ratio. According to the methodology outlined in section 2.1 for ideal Schottky diodes, a drift layer with Si concentration of 1.78×10^{17} cm^{-3} ideally should be 931 nm thick to maximize the handling capability and tuning range. 675 nm n^--GaN can potentially result in higher Q, yet the punch through voltage is compromised from 136 V to 70 V compared to the optimal scenario when using the same approach. On top of that, the tuning ratio also drops from 6.4 to 4.7. We conducted measurements on these diodes from 0 V to -70 V. In Figure 4.6, C_{0V} is 18.36 pF, and $C_{-63.5V}$ is 4.19 pF. The tuning ratio of 4.38 roughly aligns with the value obtained from the simple one-dimensional calculation. Between -63.5 V to -70 V, where carriers are fully depleted, capacitance barely changed. However, in this bias range, since electric field across the drift layer increased drastically after punch through, leakage current surged, leading to false capacitance readings around -70 V, as depicted in the figure.

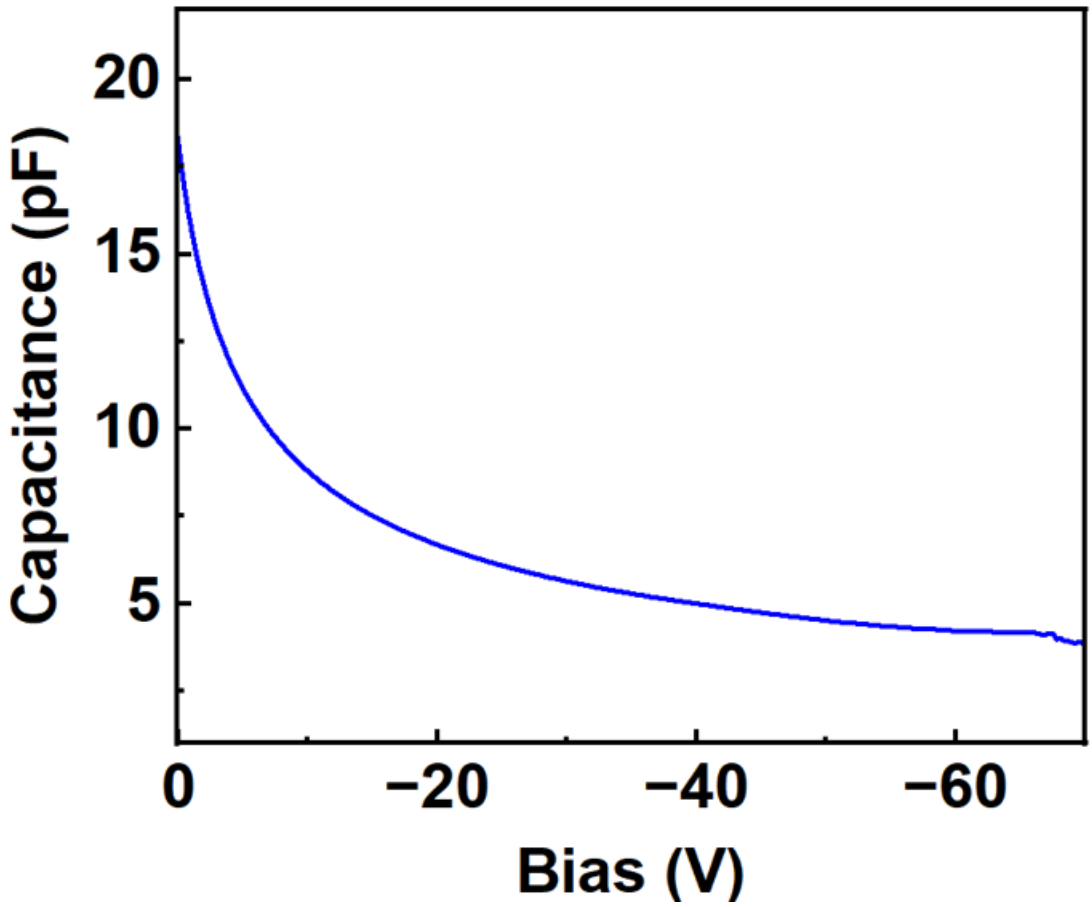


Figure 4.6 C-V_{rev} with reverse bias ranging from 0 to 70 V. Measured under circular diode configuration.

4.3 One-Port S-Parameter Measurements for Multi-Fin Diodes

Ideally, multi-Fin varactor diodes from the 2nd generation wafer should adhere to the same process steps detailed in section 3.2, with the GaN Fin etching depth targeted at 700 nm. The primary reason behind is the thinner drift layer in the 2nd generation. To circumvent excessive series resistance stemming from n^+-GaN, it's imperative to terminate fin etch once the n^+-GaN layer is reached. However, the 2nd generation multi-Fin diodes discussed in Chapter 4 and Chapter 5 underwent a 1200 nm Fin etching step, just like 1st generation. These devices were fabricated

before we ascertain the reduced drift layer thickness. As of the writing of this dissertation, we have fabricated a few batches of multi-Fin devices with 700 nm Fin etch. However, the propensity of leakage has led to a poor yield in 2nd generation, particularly for the multi-Fin configuration. Functional devices with shallow etching depth have yet to be achieved. Further effort will be dedicated to obtaining reasonable one-port S-parameter data and thorough analysis from devices with 700 nm Fin etching.

We performed one-port S-parameter measurements and parameter extractions with the same approaches mentioned in section 3.4. The one-port S-parameter measurements with anti-series multi-Fin diodes of 5 Fins/20 μm was conducted and the Smith Chart plot of S_{11} is presented in Figure 4.7 (might change). The devices also feature a 3 μm Fin width and 2 μm spacing. The depletion width modulation in the diodes with reverse bias can be confirmed through the traces in the Smith chart. The blue curve represents S_{11} under zero bias with a larger capacitance, corresponding to a smaller depletion width. Conversely, the red curve represents a −25 V bias and smaller capacitance corresponding to larger depletion width. The series capacitance, series resistance, and input impedance are calculated according to equation 3-1 to 3-3. Figure 4.8a displays the extracted C_s of under 0 and −25 V bias, showing similar convex shape as Figure 3.9a due to parasitic series inductance. We estimated inductance to be 109 and 95 pH for 0 V and -25 V using equation 3-5 with C_{est} of 160 fF at 0 V and C_{est} of 91.5 fF at -25 V (average of extracted C_s values at 4–6 GHz), respectively. Figure 4.8b shows the R_s extraction, where frequency dependent resistance still presents. Quality factors were calculated using equation 3-6, and Q versus frequency can be found in Figure 4.9a. The measured Q values at 2 GHz for 5 Fins/20 μm at 0 and −25 V were 39.6 and around 68, respectively. The Q of 103 at 2 GHz from the plot coincides with a spike that might be caused by measurement artifact. At 10 GHz, they were 12.3

and 15.7, respectively. Compared to 1st generation, 1200 nm Fin etched multi-Fin diodes in 2nd generation exhibit higher quality factors at low frequency. However, the quality factors of 2nd generation devices are comparable to 1st generation at high frequency. Since the yield is suboptimal at this stage of dissertation preparation, additional devices will need to be fabricated with 700 nm Fin etch for a fairer comparison before drawing any conclusion. $Q_{extrapolated}$ using C_{est} and R_{est} for the entire frequency range is plotted in Figure 4.9b to compare the ideal characteristics with our 1st generation devices. Calculation details are outlined in section 3.4. In the 2nd generation multi-Fin diodes, $Q_{extrapolated}$ values at 2 GHz for 5 Fins/20 μm at 0 and −25 V are 77 and 182. At 10 GHz, they are 15, 36, respectively. $Q_{extrapolated}$ values for 2nd generation devices with 1200 nm are like the 1st generation under various operating frequency. Validation of devices figure of merit deploying a 700 nm etch is poised to imminent evaluation as soon as the devices are ready.

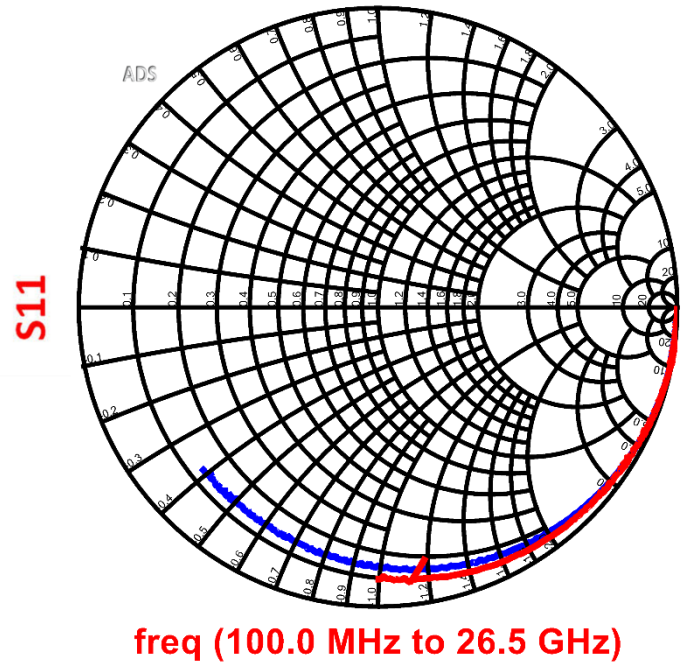


Figure 4.7 (a) 5 Fins/20 μm S_{11} plot in Smith chart for 0- and -25-V bias conditions.

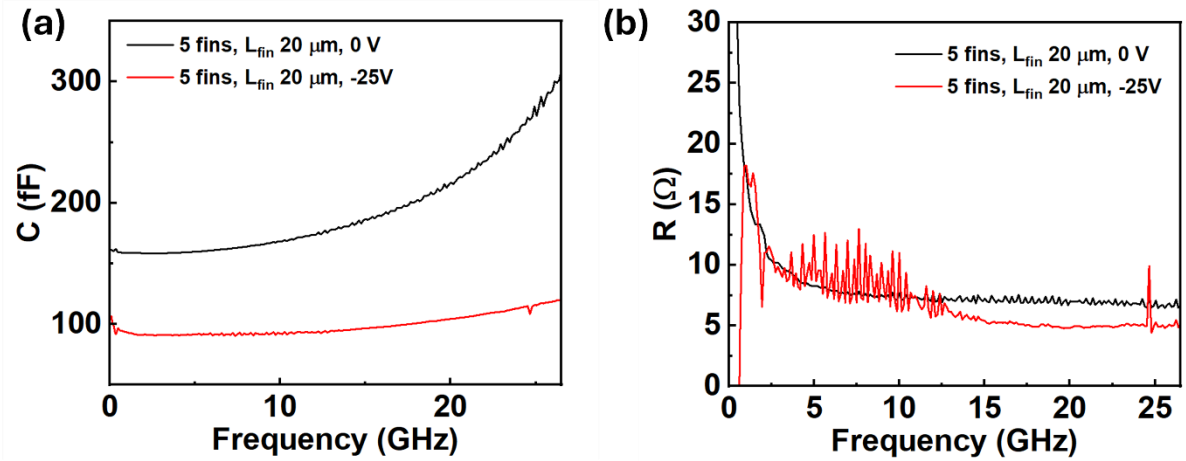


Figure 4.8 (a) Capacitance values for different bias conditions calculated using $Im(Z_{in})$. (b) Series resistance values of different bias conditions extracted from $Re(Z_{in})$.

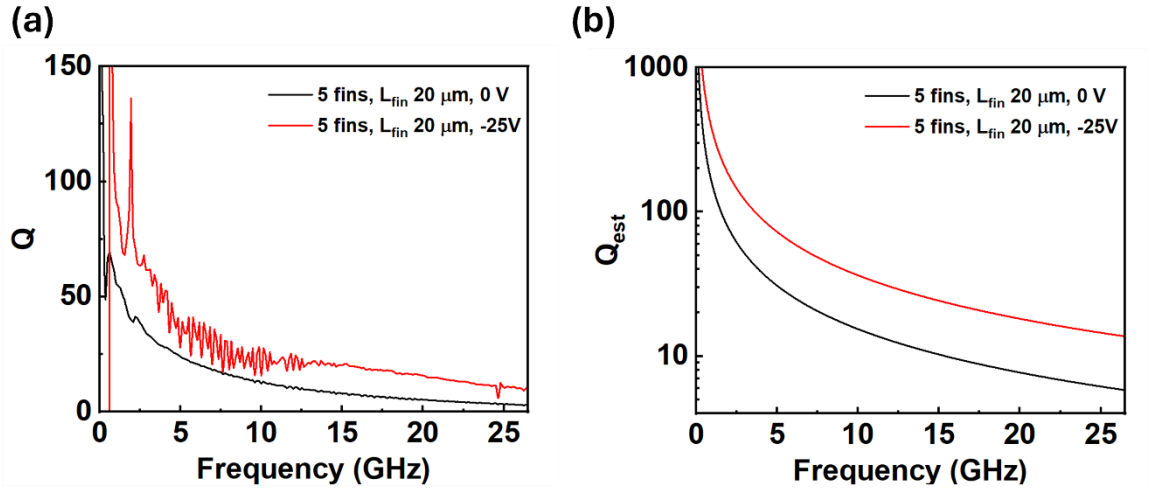


Figure 4.9 (a) Q versus frequency plot calculated using the measured $Im(Z_{in})/Re(Z_{in})$. (b) $Q_{extrapolated}$ versus frequency plot by estimating the capacitance and the series resistance and by excluding the series inductance and nonideal effects causing frequency dependent R_s.

4.4 Microwave Power Varators Projected Benchmark Revisit

Like section 3.6, we compare figure of merits of the 2nd generation devices alongside other high-power varactor technologies including the 1st generation. As discussed in section 4.2, tuning ratio of 2nd generation devices is 4.38. We report the effective tuning range versus signal voltage

amplitude for these devices in Figure 4.10, where the maximum allowed reverse bias is 63.8 V. Table 4.1 revisits key metrics to evaluate the performances of power varactors incorporating the new devices. Notably, 1st generation devices still outperform all discussed technologies, while 2nd generation devices with 1200 nm Fin etch still exhibits comparable VFOM compared to the reported SiC varactors. However, due to their low tuning ratio, 2nd generation diodes did not outshine SiC and GaN technologies despite the high cutoff frequency. This comparison is illustrated in Figure 4.11, which plots the cutoff frequency as a function of small signal tuning range.

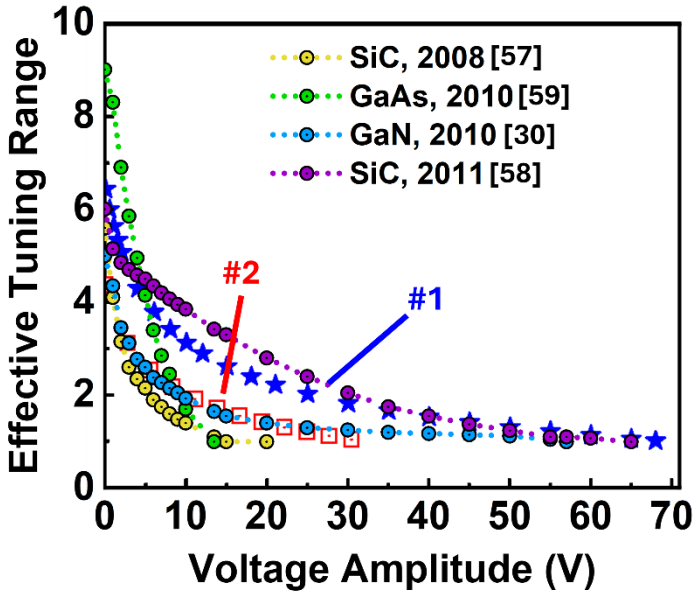


Figure 4.10 Comparison of power varactor technologies for capacitance tuning range versus superimposed signal voltage amplitude. Camel diode data in this work is calculated under circular diode and anti-series configuration under signal peak.

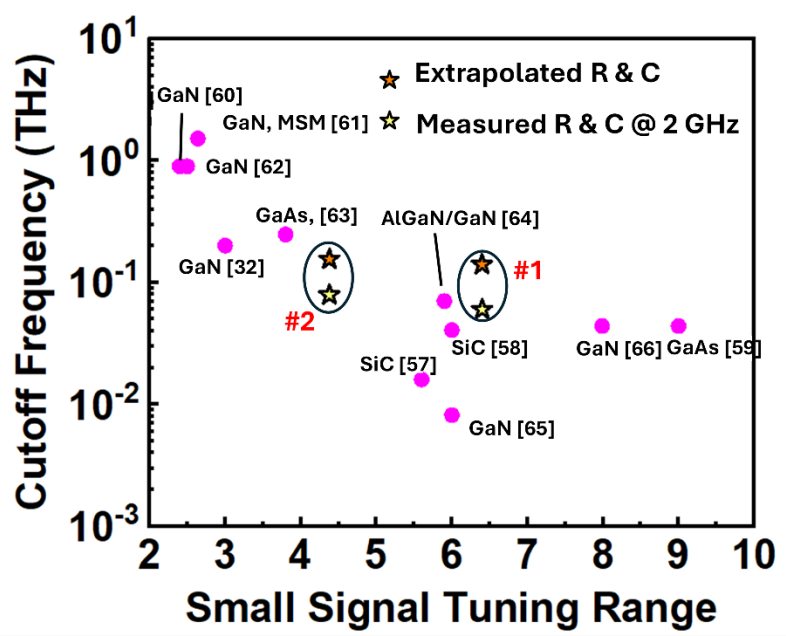


Figure 4.11 Comparison of different varactor technologies for their cutoff frequency versus small signal tuning range.

Table 4.1 Comparison of key FOMs for microwave power varactors.

Technology	SS Tuning	Punch-Through	Breakdown (V)	Q_{min}	Q_{max}	VFOM
SiC [57, @ 2GHz]	5.6/1	15	40	8	45	1100
GaAs [59, @ 2GHz]	9:1	15	28	22	150	5280
GaN [30, @ 1GHz]	5:1	N.A.	120	N.A.	>35	<16800
SiC [58, @ 2GHz]	6:1	60	>150	20	160	12000
1st generation [@ 2GHz]	6.4:1	138 (expected)	Circular: 196 Multi-Fin : 146	>30 (measured) >70 (extrapolated)	N.A. >420	44700
2nd generation [@ 2GHz]	4.38:1	63.5	Circular: >70 Multi-Fin : NA	>39 (measured) >70 (extrapolated)	N.A. >420	17084

4.5 Conclusions

In this chapter, we verify the epitaxy stack of the wafer deployed in the varactor fabrication, as detailed in Chapter 2 and Chapter 3. We discovered that the p^+-GaN in these wafers is twice as thick as intended in the design, which well explains the observed anomaly in R_s values. A wafer with thinner p^+-GaN and thinner n^--GaN drift layer confirmed by SIMS depth profile was prepared subsequently. Static characterizations performed on circular diodes fabricated using the new wafer indicate that this 2nd generation wafer is aligned more closely with a camel diode than the 1st

generation wafer. Despite the higher reverse leakage current and low yield for the 2nd generation wafer, we were able to conduct high-voltage CV measurements to determine the tuning ratio. Additionally, one-port S-parameter measurement on multi-Fin diodes with a 1200 nm Fin etch revealed a Q_{min} greater than 39 at 2 GHz, consistent with thinner p^+-GaN and thinner n^--GaN in the 2nd generation wafer. We compared the performances of devices fabricated from the 2nd generation wafer with those of other power varactor technologies and devices from 1st generation wafer. Looking forward, we plan to further enhance the performance of devices from the 2nd generation wafer by conducting 700 nm Fin etch.

Throughout this dissertation, multiple DC and RF considerations were considered to ensure the functionality of these varactors. For instance, we introduced a thin p^+-GaN as the top epi-layer and GaN/QST to minimize reverse leakage current. For RF consideration, we employed thick Schottky metal to reduce series resistance, extended bias resistors on the planarized polyimide, and eliminated bottom silicon, and so on, to mitigate parasitic effects. However, to achieve optimal performance for this technology in practical applications, further design factors optimization is essential. For instance, since the multi-Fin diodes in this work exhibit lower yield and V_{bk} than circular diodes, anti-series disk arrays without compromising Q too much would be preferrable. With proper design, disk array configuration can also provide better tuning range. Additionally, considering the dielectric between the Fins, it would be advantageous to develop devices with only air between the Fins to maximize the tuning ratio, given its lower dielectric constant. We utilized ADS momentum EM simulation to study these effects. In our design featuring five 20 μm Fins with 1 μm thick Schottky metal, a dielectric between Fins with dielectric constant of 3.3 yields a tuning ratio of 3.57 while the one with dielectric constant of 1 achieves 4.57. It's noteworthy that lots of design factors can be interdependent and do not constitute universal rules. Thorough

calculations and careful evaluation of design trade-offs are crucial. Material properties such as mobilities of n^--GaN and n^+-GaN, undoubtably follow the principle of "the higher, the better", given certain doping level, as mobilities directly influence series resistance. Moreover, as the decrease in mobility occurs at a slower rate than the increase in Si doping concentration in n^+-GaN, augmenting the doping concentration in n^+-GaN is desirable to reduce series resistance.

Chapter 4, in full, is currently being prepared for submission for publication. P. C. Chen, P. M. Asbeck, and S. A. Dayeh. The dissertation author is the first author of this paper.

CHAPTER 5: Tunable Bandpass Filter based on GaN Multi-Fin Varactors

5.1 Tunable Filter Design by Circuit Simulation with ADS Built-in Microstrip

A tunable band pass filter consisting of two coupling capacitors, two GaN varactors, and a coupled-line resonator is proposed in this chapter.[59,60] We first deployed ADS circuit simulation to fine-tune the capacitance target for the coupling capacitors, the geometry of the parallel couple lines, and the dimensions and material for the PCB board. The varactor model employed in the simulation is based on the empirical calculation from section 2.3, the same as the model used for preliminary RF simulation in section 3.1. The circuit incorporated two anti-series varactors, each with fourteen 40 μm Fins (approximately 700 fF) shunted to ground, and included two 2 Ω resistors in series with the varactors to replicate practical scenario. We fixed the varactors and resistors then tweaked couple capacitors, couple lines, and substrate properties to minimize insertion loss and achieve the narrowest bandwidth at various bias point. The optimal capacitance (C_{cou}) for coupling capacitors was found to be 0.2 pF. The dimensions for the parallel couple lines were set at a width of 200 μm, a length of 1376 μm, and a spacing of 4098 μm. Furthermore, the substrate dielectric constant, substrate thickness, and metal line thickness were determined at 3.717, 508 μm, and 66.04 μm, respectively. Figure 5.1 displays the circuit simulation setup with the parameters utilized in our real-world filter demonstration. Figure 5.2 presents the S_{11} and S_{21} with varactors under bias ranging from -1 V to -31 V. In this ideal scenario, we expected to obtain largest insertion loss with varactors under at -1 V not greater than 4 dB and center frequency tuning greater than 1 GHz.

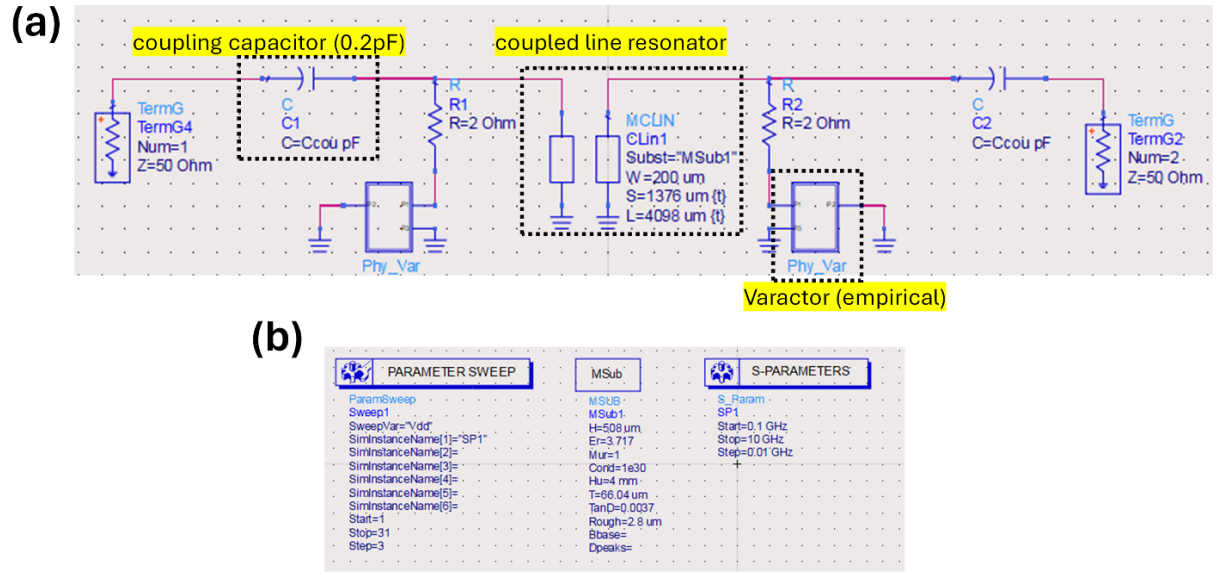


Figure 5.1 (a) Circuit simulation schematic for a coupled line resonator and varactor based tunable filter. (b) Reverse bias sweep, frequency sweep, and substrate setup.

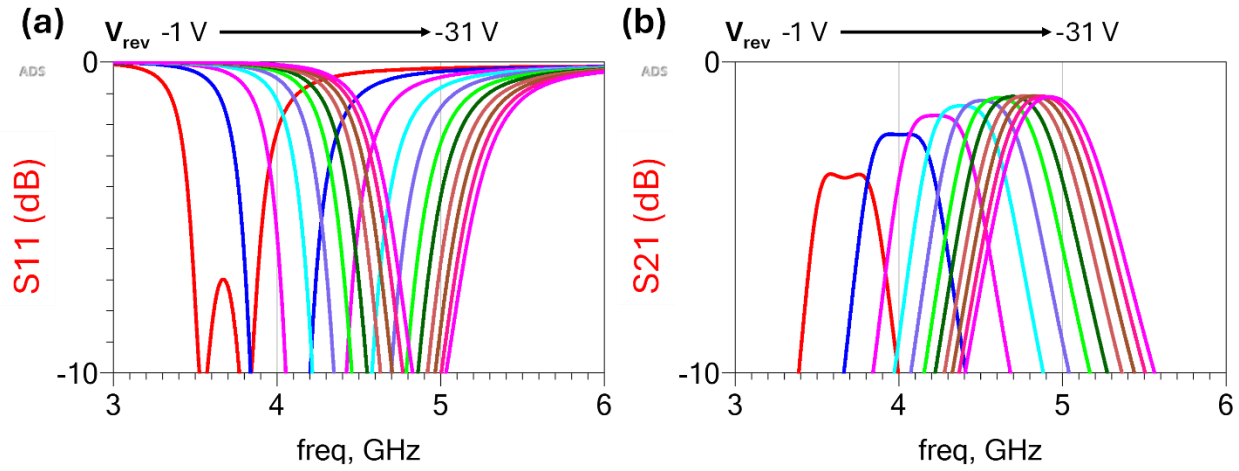


Figure 5.2 (a) Simulated S_{11} under reverse bias ranging from -1 V to -31 V. (b) Simulated S_{21} under reverse bias ranging from -1 V to -31 V.

5.2 PCB Board and EM Simulation

PCB design was conducted after the circuit simulation. Figure 5.3 is the PCB board schematic. The full design from left to center and from right to center was a SMA connector, a 50 Ω microstrip transmission line, and a coupling capacitor. The anodes of the varactors were

connected to one side to coupling capacitors and couple lines and to the ground. DC bias pads connected to varactor cathodes and would be applied with positive bias. In addition to circuit simulation, we performed EM simulation using ADS momentum after the PCB design to further check the difference between the EM simulation and the circuit simulation. Whichever has behavior closer to the measured results would be used to analyze the filter and varactor performance. The details for the EM simulation are presented in Figure 5.4a. Our EM simulation setup utilized the identical layout and the material properties of the PCB board with C_{cou} and varactor capacitance ($C_{varactor}$) of 0.2 pF. To simplify the process, coupling capacitors and ideal varactors were replaced by parallel plate capacitors for the EM simulation. These parallel plates were confirmed to exhibit 0.2 pF. On the other hand, circuit simulation like Figure 5.1a with C_{cou} and $C_{varactor}$ of 0.2 pF was performed. The resistor on each side was set to be 0.5 Ω. Figure 5.4b and 5.4c demonstrate magnitude of S_{21}, showing lower pss band frequency obtained from the EM simulation. Though there is little disagreement between different simulation methods, they both show that the design of this prototype filter is reasonable. The final PCB utilized 20 mil thick Rogers RO4350B substrate, coated with 2U" ENIG atop 2oz. copper on both sides.

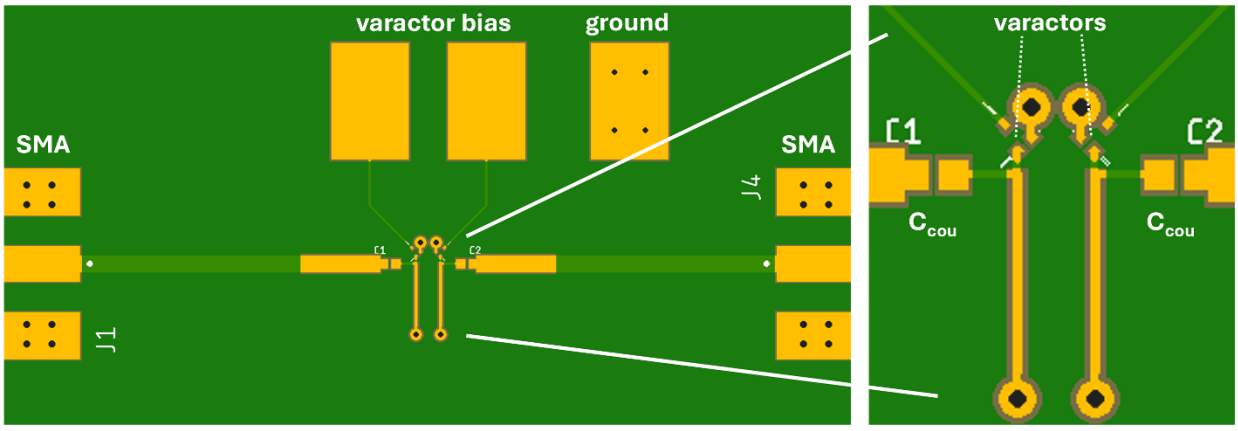


Figure 5.3 PCB board design schematics.

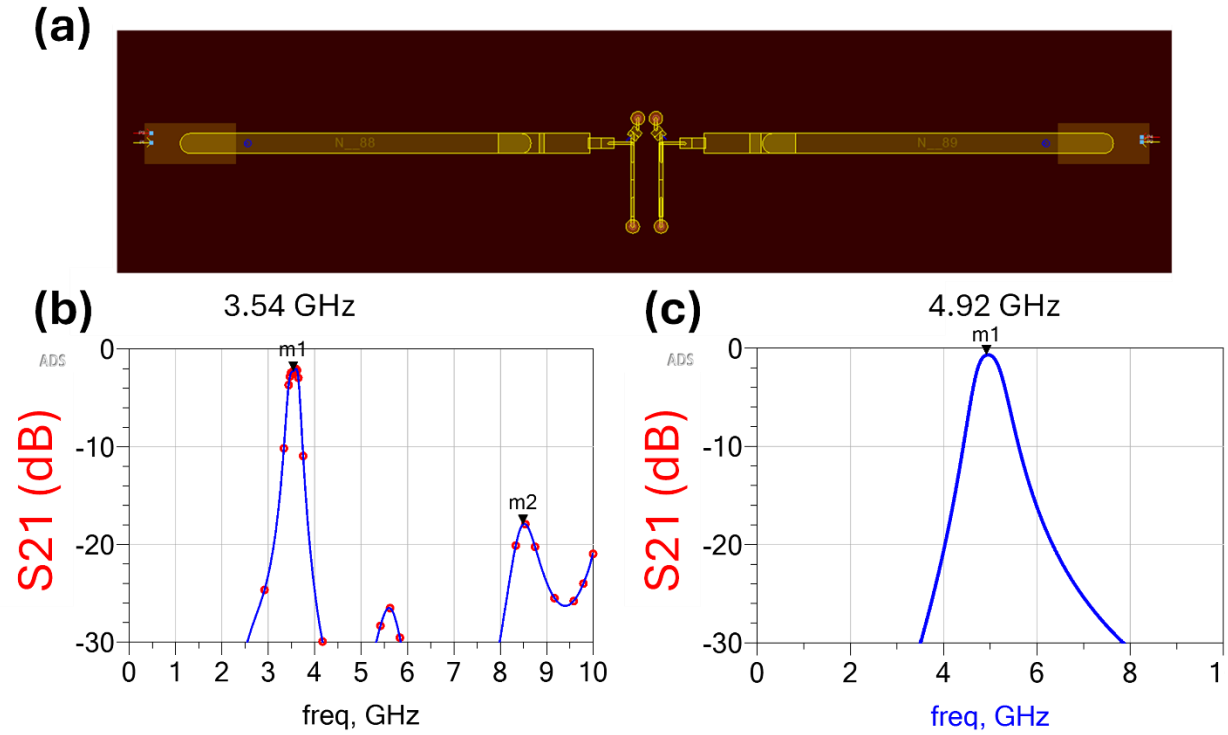


Figure 5.4 (a) EM simulation layout for a tunable filter with the designed board. Coupled capacitors and varactors are replaced with parallel plate capacitors for simplification. (b) EM simulation result when $C_{varactor}$ is 0.2 pF. (c) Circuit simulation result with ADS built-in microstrip component when $C_{varactor}$ is 0.2 pF.

5.3 Characteristics of Tunable Filter Based on GaN Multi-Fin Varactors

Figure 5.5a shows a diced GaN varactor prepared for flip-chip bonding. Figure 5.5b displays the zoom-in view of varactors once bonded onto the PCB, and Figure 5.5c offers a zoom-out perspective of the entire filter and the test structures. The flip-chip bonding by silver epoxy and solder paste were calibrated, and the series resistance caused at each bonding contact is lower than 0.2 Ω. Additionally, the THRU structure showed very low insertion loss from 2 GHz to 5 GHz, confirming good SMA connections. Figure 5.6 presents S-parameter results for the assembled filter incorporating our 1st generation GaN varactors. The insertion losses surpassed 8dB, while the 3dB bandwidth expanded beyond our simulation predictions across different reverse bias. The

Q of varactors under zero bias was about 50 if fitting the insertion loss with EM simulation. However, 3dB bandwidth is wider in the measurement. However, circuit simulation fitting indicated a Q-factor of approximately 17. Further research is required to improve the filter performance, primarily dependent on varactors' performance. One significant challenge was the initial low yield of our bonding process. Consequently, very few working 1st varactor samples remained. The varactor devices shown in Figure 5.6 were produced before the bonding process was finalized and optimized. We also developed tunable filters using 2nd generation varactors, which were assembled with a more reliable bonding method. Figure 5.7 shows S-parameter results of the assembled filter based on our 2st generation GaN varactors, showing higher insertion loss and broader 3dB bandwidth compared to the earlier filter version. The primary limitation for 2nd generation varactor based filters remains varactor yield. It's challenging to achieve varactors with high Q and low leakage concurrently from the new wafer. Future efforts will focus on producing a larger quantity of filters for more comprehensive analysis.

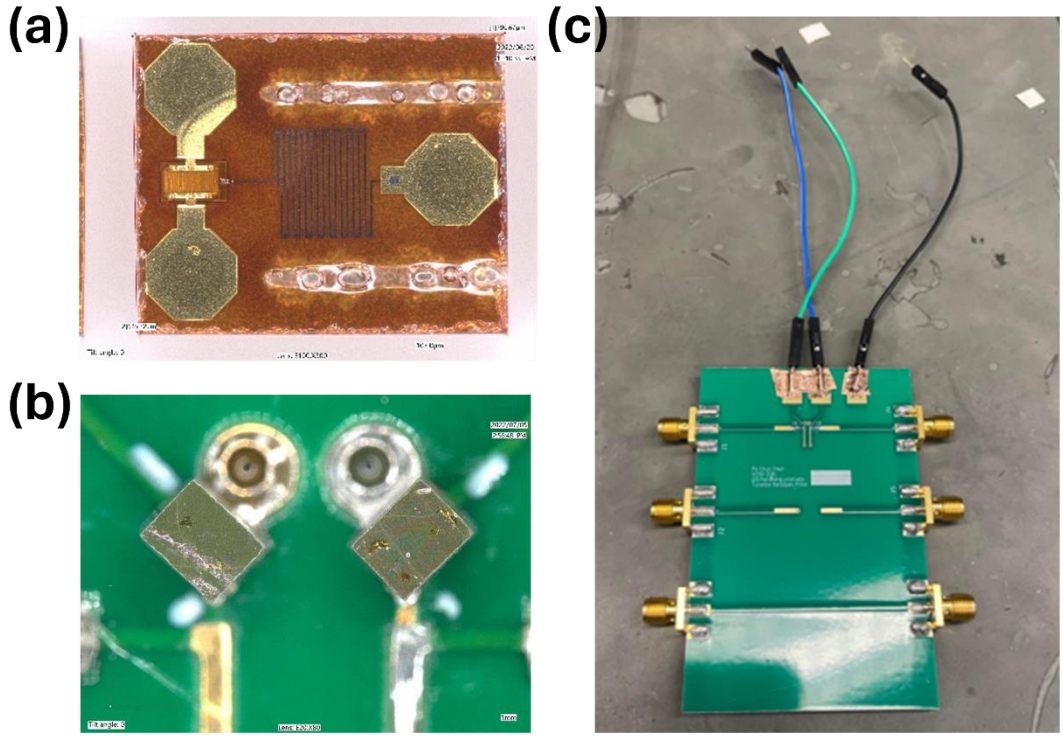


Figure 5.5 (a) A diced varactor die ready for bonding. (b) Flip-chip bonded varactors on a tunable filter board. (c) Zoom-out view for a tunable filter with open, short, and through test structures.

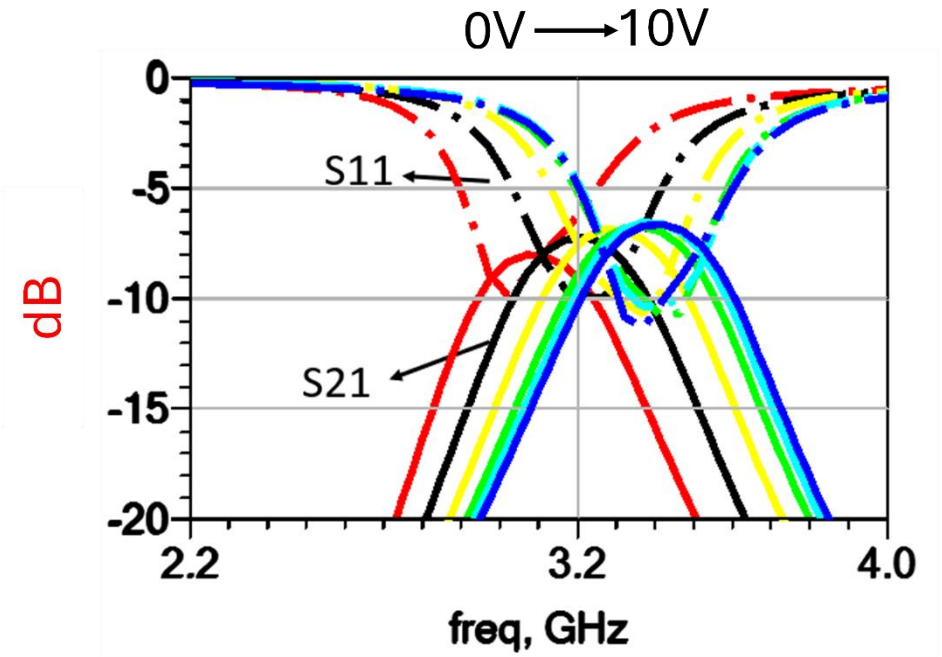


Figure 5.6 S_{11} and S_{21} characteristics of a 1st generation varactors bonded tunable filter.

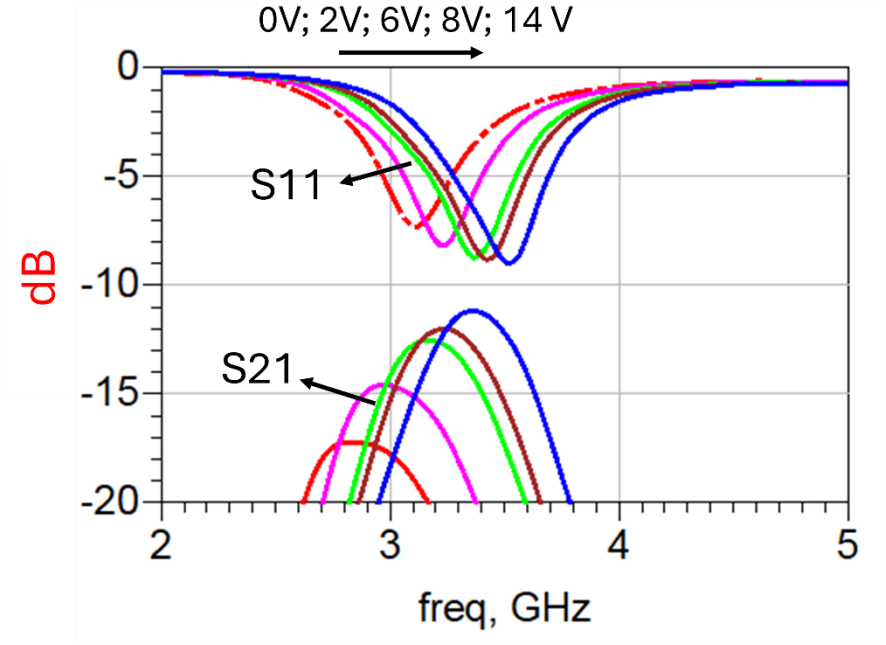


Figure 5.7 S_{11} and S_{21} characteristics of a 2nd generation varactors bonded tunable filter.

5.4 Conclusions

In summary, we devised a tunable bandpass filter integrating a coupled line resonator and GaN varactors. Through meticulous circuit simulation, we fine-tuned coupling capacitors, coupled line resonator, and microstrip parameters to achieve optimal filter performance. Following validation via EM simulation, PCB boards were designed and procured. Both 1st generation and 2nd generation varactors were employed in assembling tunable filters. S-parameter measurements revealed higher insertion loss and broader 3dB bandwidth than initially projected from simulations. For the filter made of 1st generation devices, the main challenge was the bonding yield. It cost a few devices after several iterations until we optimized the bonding process. Conversely, for the filter made of 2nd generation devices, varactor yield was the main challenge. Future improvement

of yield and varactor quality factors by shallow etch for 2nd generation devices may further enhance the filter performance.

Chapter 5, in full, is currently being prepared for submission for publication. P. C. Chen, P. M. Asbeck, and S. A. Dayeh. The dissertation author is the first author of this paper.

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