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ABSTRACT

Some recent multichannel scintillation-counter experiments are so complex that the use of test routines and fault monitoring becomes essential. In a recent experiment, it was desired to initially align the system, provide continuous calibration during the experiment, and rapidly locate the cause of threshold drift or catastrophic failure. A test and monitoring system was devised in which synthesized pulses are injected into several points of the system, and the operation is automatically compared with the desired response. If the system performance does not agree within prescribed limits, an alarm sounds.

Through a program that varies the amplitude of the test signal, one can check coincidence-circuit threshold and feed-through characteristics. By programming delay between input pulses, the resolving time can be measured.

Several novel monitoring devices have been developed which allow one to assess the display of a large volume of information at a glance. One unit for reading time delays involves the use of a cathode-ray-tube raster display; another unit for reading binary information employs a transistor-driven incandescent lamp panel.

Further aspects of this system are discussed by S. C. Baker, F. A. Kirsten, D. A. Mack, and C. Wiegand in "An Electronic Data-Acquisition System for Use with a Complex Nuclear Physics Experiment, " UCRL-9271, December 1960; by S. C. Baker in "A Transistor Coincidence-Discriminator Circuit for 10^{-8} -Second Pulses, " UCRL-9272, November 1960; by A. Bjerke, Q. A. Kerns, and T. Nunamaker in "A Solid-State Chronotron for Digitizing Time Delays, " UCRL-9270, December 1960; by F. Evans and F. A. Kirsten in "An 1800-Bit Buffer Store and Readout System, " UCRL-9274, December 1960; and by Q. A. Kerns, and G. C. Cox in "A Nanosecond Triggered Light Source Using Field Emission, " UCRL-9269, October 1960.

TEST ROUTINES AND MONITORING FOR A LARGE COUNTER EXPERIMENT^{*}

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I. INTRODUCTION

With recent expansion in the complexity of nuclear counter experiments, it has become desirable to automate not only the acquisition of the experimental data but also the methods of checking the counting system for proper performance. In a recent pion-scattering experiment, a number of error-checking techniques were employed to (a) facilitate initial alignment of the equipment during setup, (b) maintain a check on the threshold amplitude levels of the discriminator units during running, and (c) detect faulty operation in the over-all system.¹ A block diagram showing how the error-checking units apply to the system is shown in Fig. 1.

Some error-detection schemes are directly applicable to the signals generated by a nuclear event. In general, however, it is more desirable to inject light or electrical test pulses at an appropriate point in the system to simulate the variables normally encountered in operation. An example of the former method, in which the signal does its own checking, is the use of the redundancy parity-bit check in the paper-tape punching unit in this experiment as well as in many computers. In the latter type of test routine, simulated signals are programmed both in amplitude and time of occurrence to verify the limits of reliable operation.

This paper describes checking methods that were employed in a recent experiment along with plans for a more complete checking program in a future run.

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II. ERROR DETECTION

Before considering the particular devices used, it would be well to discuss our requirements for an error-detecting system. The following design criteria were incorporated into this experiment whenever practical:

a. The test program must simulate as nearly as possible the actual response to a desired nuclear event in a background of undesired events. Test signals should have the same range in rise time, duration, and amplitude as those expected from the nuclear interaction. One can simulate the response to random events by testing at repetition rates higher and lower than the maximum encountered in actual operation and with signal amplitudes greater and less than those produced by a correct event.

b. The system response to one desired event out of a background of as many as 100,000 or more unwanted events per acceleration period should be evaluated.

c. The test routine must detract as little as possible from the normal running of the experiment. How often tests are made must be a compromise between shortened running time and the loss from possible catastrophic failures occurring between infrequent test periods.

d. Error-detection circuits must be of the highest reliability to insure proper test-routine results.

e. Error detection should localize the trouble to a particular area. Then operation can be restored usually by simply exchanging a functional unit with a spare. If operation is still not restored, a technician must then resort to point-by-point circuit tracing.

f. It is helpful if the test routine is capable of marginal checking to detect incipient failures. It is also desirable to differentiate between the response of a circuit that is out of adjustment (e.g., a drift in voltage-threshold level) and one that is completely inoperative.

g. The test routine must be as straightforward as possible, and the results easily and rapidly interpreted. Time is often of the essence for restoring the experiment to normal operation.

h. Error-correcting circuits should be considered where feasible.

III. COINCIDENCE - DISCRIMINATOR TEST ROUTINE

A. General Discussion

An automatic testing and checkout unit for the coincidence portion of the data-acquisition system was designed to utilize a ramp pulser as a test-signal source. The purpose of this test is (a) to check the amplitude threshold of each of the 168 discriminator units, (b) to test for cross-talk between coincidence-discriminator units, (c) to check the operation of the core store and associated circuits, and (d) verify the operation of the tape-punch driving circuits. This test routine was applied to the system by interrupting normal operation after 128 Bevatron acceleration periods and using the interval of two Bevatron beam times for testing. Simulated phototube pulses from the ramp generator were applied to the even-numbered coincidence-discriminator circuits during the first of these two Bevatron beam times, and to the odd-numbered circuits during the second. A group of about 30 simulated phototube pulses was generated during each ramp; they ranged in amplitude from 80% to 110% of the previously determined threshold level of each discriminator. The discriminators were required to maintain signal thresholds within $\pm 10\%$; thus any discriminator which triggered during the 80 to 90% portion of the ramp had drifted outside the specified range. If any of them produced an output during the 80 to 90% interval, the ramp was terminated at the 90% level, the number of the misbehaving coincidence-discriminator was indicated on a light panel, and an alarm sounded. If no outputs were detected by the 90% level, the ramp was

continued up to the 110% level where it terminated. By this time, all even- (or odd-) numbered channels should have triggered. The test "event" was then stored, and the process repeated nine more times, filling the core store. The results were then punched out onto paper tape as is done for normal events. During the punching process, a part of the test-routine circuitry sampled the voltages across the tape-punch magnets. The purpose of this was to verify that the proper channels were being punched. A missing signal in one channel indicated a failure in some part of the system. Accordingly, an alarm sounded. The presence of cross-talk between channels was also detected during the punching by noting whether any even-numbered channels triggered when only odd-numbered ones should be present and vice versa.

B. Ramp Pulser

The ramp pulser generated bursts of simulated phototube pulses having a rise-time of about 3 nsec and a decay time of about 10 nsec. During each burst of about 30 msec duration, the amplitude of the pulses varied linearly with time from 80 to 110% of a nominal amplitude.

A mercury-relay capsule was chosen as a pulse-generating element capable of producing signals of accurately controlled amplitude and of sufficiently high energy to be split into groups of 84 signals. With such a pulse generator, the ramp envelope is generated simply by applying a similarly shaped charging-voltage waveform to a small capacitor. The capacitor is periodically discharged by the vibrating relay contacts into a 25-ohm-impedance shaping network. The pulses from the shaping network simulate normal phototube pulse response. They are then split into two 50-ohm outputs which feed two pulse distributors. The pulse distributors further split the pulse 12 ways as shown in Fig. 2, for distribution to groups of 5 coincidence discriminators each.

The method of generating the ramp is shown in Fig. 3 and some of the waveforms in Fig. 4. When a gate is applied, the charging voltage is allowed to rise to the 80% level. The bootstrap charging circuit causes the voltage to change linearly. When the 110% level is reached, a blocking oscillator triggers and produces a signal that turns off the gate.

C. Display Panel

The display panel has a two-fold use. It provides an easy method for the observation of experimental data during the running of the experiment and facilitates error checking during test periods. The panel consists of an array of incandescent lights arranged in the same spatial pattern as the scintillation counters in the experiment; there is one light for each coincidence-discriminator unit. While the data-acquisition system is capable of storing ten different events per Bevatron beam burst, the eye has difficulty in remembering more than one event in an interval of a few seconds; thus it was decided to display only the first event in any beam burst. This is accomplished by a gated flip-flop driving each light circuit.

A light-gate generator normally holds all of the flip-flop gates so that they cannot receive a pulse. Just before the accelerator beam, this gate is opened so that each flip-flop may receive a pulse from its respective coincidence-discriminator circuit. When the first event is detected by the system, the light-gate generator is turned off for the duration of the Bevatron beam period. In this manner, only the first event pattern in each beam burst is stored on the light panel. The display flip-flops are reset at the beginning of the next Bevatron acceleration cycle. The light bulbs (General Electric No. 344) glow brightly at 12 v and draw about 20 ma. They glow very dimly at 5v and draw about 9 ma. An emitter-follower stage which couples the flip-flop to the light bulb was designed so that when the flip-flop is on, the

the light bulbs draw 20 ma, and when the flip-flop is off, the light bulbs draw 9 ma. Thus both the binary 0 and 1 state can be distinguished from an open circuit or a defective bulb.

The lights are essential in determining the threshold of the coincidence-discriminator circuit and in checking the operation of the whole system. The system is constructed so that it is easy to program a known test pattern into each coincidence-discriminator circuit through a test-pulse input. By comparing the light-display panel with the punched-tape record, one can determine if a system malfunction occurred in circuits of the coincidence discriminators or after them. That is, if the display panel indicated the correct pattern but the punched tape did not, the trouble was in the core-memory or read-out circuits.

IV. CHRONOTRON TEST CIRCUITS

A. General Discussion

The test-pulse generator and cathode-ray-tube (CRT) display was designed to check the operation of the chronotron under simulated operating conditions.² Simulated phototube pulses are sent to the chronotron, where their time delay is measured. The measured time delay is read back to the CRT raster, where the display patterns for all four chronotrons may be observed simultaneously and compared. A block diagram of the test circuits is shown in Fig. 5. Knowing the correct patterns, an observer can quickly discern whether or not a chronotron is operating properly. If it is not, the changes in the raster pattern quickly help localize the trouble.

The display tube uses the horizontal and vertical sweep circuits of a standard television set. The display is a binary-coded signal shown in the form of a bar graph. The vertical oscillator runs at the 60-cycle line frequency, while the horizontal oscillator free runs at about 15.75 kc. A pulse-pair generator and reset-pulse generator are slaved to the horizontal oscillator. The pulse-pair generator sends two simulated phototube pulses to the chronotron at the start of the horizontal sweep. At the end of the horizontal sweep, the reset-pulse generator sends a reset pulse to the chronotron. By programing the interval between the two pulses of the pair, one is able to check all possible delay combinations of each chronotron and present these on one raster.

The test routine is gated on whenever the data-acquisition system is not in operation. For this experiment, the test routine was off for a few tenths of a second out of each 6 sec, so there was a nearly continuous display.

The pulse-pair generator uses 2N501 transistors operated in the avalanche mode to generate two simulated phototube pulses. The time delay

between the two pulses is controlled by firing one unit (avalanche No. 1) at a fixed time with respect to the horizontal sweep, and firing the other (avalanche No. 2) with a ramp generated at the beginning of the horizontal sweep plus some fraction of the vertical sweep voltage. The fraction of the vertical sweep voltage depends upon the time interval that it is desired to test and display. Thus the relative timing between these two pulses is varied as a function of the vertical sweep with time increasing from top to bottom of the CRT display.

At the end of the horizontal sweep, the reset generator sends a reset pulse to the chronotrons, thereby resetting them for the next pair of test pulses.

B. Chronotron Test Cycle

At the beginning of the horizontal sweep, the pulse-pair generator sends two simulated phototube pulses to all four chronotrons, along with a search command signal that starts the chronotrons. The chronotron measures the time delay between the two test pulses and reads out into a parallel-to-serial converter; its operation is described below. The readout of the parallel-to-serial converter is actuated by the readout pulse generated about 5 μ sec after the beginning of the horizontal sweep. This readout pulse reads all the chronotron outputs into a type-HH-2000 delay line. The chronotron signals thus arrive at the CRT video amplifier in serial fashion, where they are amplified to brighten the video display. The proper test display is shown in Fig. 6, where all four chronotrons are being checked together and are displaying all possible time-delay combinations simultaneously. In actual operation not involving a test routine, a chronotron obviously measures only one interval per nuclear event. The display is in binary form; 1, 2, and 4 being read from left to right from each of the four

chronotrons. At the top of the display, all chronotrons are reading out from time interval one, while at the bottom of the display, all chronotrons are reading from interval seven. Time is calibrated in vertical steps and marked on the screen so that any timing error shows immediately as a vertical shift in a portion of the pattern. The display not only tells when there is an error, but also tells its magnitude and location in a particular time interval. It is possible to observe any 60-cycle effects in the chronotron by changing the phase of the 60-cycle vertical sweep. If there are line-frequency effects present, these will produce a shift in the display as the phase of the vertical sweep is changed. This is useful for checking against 60-cycle effects in the chronotrons.

Figure 7 shows the display of Fig. 6, with the vertical time scale expanded. A 1-nsec delay has been introduced intentionally into the second (β) channel in order to give a time calibration for the picture. The jitter of the display is within 0.1 nsec, as can be seen from the photo. This is seen more easily by observing the display in operation for a few minutes. This jitter is the sum of the jitter in the pulse-pair generator and in the chronotron.

If desired, events can be read directly from the chronotron on a 21-in. oscilloscope by using the parallel-to-serial converter. In this case, the CRT is swept in the vertical direction by a 0.1-sec ramp that is triggered whenever the Bevatron is pulsed. The horizontal sweep of the CRT is triggered for each chronotron event, and the video signal is controlled by the parallel-to-serial converter. The resulting display is a series of dots along each horizontal sweep in accordance with the binary readout of each of the four chronotrons.

By means of switches in the parallel-to-serial converter, the decimal output of any one chronotron can be displayed along with its binary output. This feature is useful for pin-pointing any malfunction; by inspection of the decimal display, one can tell which chronotron channels are operating properly and which ones are not. For example, if the decimal display is correct and the binary display is not, the trouble must be in the binary storage rather than in the chronotron itself. The flexibility of this type of monitoring has made it possible to keep the chronotron operating properly with very little down time, since trouble normally can be spotted and corrected before it becomes serious.

C. Parallel-to-Serial Converter

The binary outputs of the four chronotrons appear as dc levels at the inputs to the parallel-to-serial converter, as shown in Fig. 8. When the amplifier gates of the converter are pulsed by a read signal, a 1- μ sec pulse is sent down the HH-2000 delay line only if there is a chronotron input. Because each chronotron is tapped into the delay line at a different point, its output is a serial representation of the chronotron inputs.

The read-gate amplifiers are 2N501 transistors with their collectors tied to the center conductor of the HH-2000 line through a diode. The diodes are necessary to prevent pulses on the line from forward biasing the 2N501 transistor and thus shorting out the line. Collector voltage for all transistors is supplied from the center conductor of the delay line. When the amplifier is pulsed, the transistor saturates, which shorts the line for about 1 μ sec, and thus puts a positive pulse on the line equal to the collector voltage of the transistor. To compensate for the pulse-height attenuation of the delay line, a higher collector voltage is used at the far end of the delay line than at the output end of the line by establishing a dc voltage gradient along the line

with a dc current through the line. Without compensation, the pulse-height variation was about 3:1; with compensation, the variation was reduced to about 3:4. This first-order compensation was sufficient to produce a well-standardized video output after going through a simple shaping circuit.

D. Switching

To increase the flexibility of the converter, all inputs are brought in through patch panels and switches. This makes it possible to arrange the display in any desired manner. The most useful displays used were (a) all four chronotron binary outputs, and (b) the display of the decimal outputs of a single chronotron along with its binary display. The binary display of all four outputs provides a check on the whole chronotron system, while the display of the decimal plus binary outputs affords a check on the internal operation of each chronotron.

E. Pulse-Pair Generator

The pulse-pair generator is a conventional avalanche pulse generator using 2N501 transistors. Each avalanche unit is driven by a blocking oscillator which is in turn driven by a ramp generated at the beginning of each horizontal sweep. In order to time the variable pulse, a portion of the 60-cycle vertical sweep is added to its ramp. This varies the timing between the two avalanche pulses as a function of the vertical-sweep position.

The output of the avalanche transistors is taken from the collector through a 10- μ f capacitor to a 50-ohm output cable and has an amplitude of about 5 v. When using 2N501 transistors in the avalanche mode, we have found that reliable operation is possible only for light loads.

V. CONCLUSIONS

The methods described here, while quite elementary, have given us confidence in the system and, when faults did occur, allowed rapid location and correction. Several improvements are planned for use in the fault location system of a future scattering experiment. It is desirable to have the initial error-checking procedure include the entire chain of counting equipment from detector to output-data unit; that is, test signals injected at the detectors should produce a known set of output signals.

Programmed light pulses illuminating scintillation or Čerenkov detectors should generate the correct coincidence-system response. This information would then be placed in the buffer-store unit and recorded on magnetic tape. Should the magnetic tape record not correspond to the expected output response, then the experimental equipment would be divided into several logical blocks to localize the circuit malfunction. These divisions include the scintillation detectors and gate-forming circuits, the coincidence and chronotron circuits, the core storage, and the magnetic tape transport. Work is under way to provide a more complete error-checking system.

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1. S. C. Baker, F. A. Kirsten, D. A. Mack, and C. Wiegand, Lawrence Radiation Laboratory Report UCRL-9271, December 1960.
2. A. Bjerke, Q. Kerns, and T. A. Nunamaker, Lawrence Radiation Laboratory Report UCRL-9270, December 1960.

MU-22291

Fig. 1. Block diagram of data-acquisition system emphasizing error-checking circuits.

MU-22290

Fig. 2. Schematic diagram of test pulse distributor. All cables are miniature 50-ohm coaxial. Each group of four cables makes four turns around a toroid.

MU-22289

Fig. 3. Simplified schematic diagram of ramp pulser. The wave forms for A and B are shown in Fig. 4. The mercury delay capsule vibrates at 400 cps.

MU - 22288

Fig. 4. Wave forms of the ramp generator.

MU-21210

Fig. 5. Block diagram of chronotron test routine.

ZN-2629

Fig. 6. Display of binary-coded test signals of all four chronotrons. Left to right are Chronotrons α , β , γ , and δ . Time increases from top to bottom.

ZN-2630

Fig. 7. Expanded display of chronotron binary-coded test signals showing 1-nsec delay in channel β .

MU-21211

Fig. 8. Block diagram of chronotron parallel-to-serial converter.

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