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Characterizing defects and transport in Si nanowire devices using Kelvin probe force microscopy

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Abstract
Si nanowires (NWs) integrated in a field effect transistor device structure are characterized using scanning electron (SEM), atomic force, and scanning Kelvin probe force (KPFM) microscopy. Reactive ion etching (RIE) and vapor–liquid–solid (VLS) growth were used to fabricate NWs between predefined electrodes. Characterization of Si NWs identified defects and/or impurities that affect the surface electronic structure. RIE NWs have defects that both SEM and KPFM analysis associate with a surface contaminant as well as defects that have a voltage dependent response indicating impurity states in the energy bandgap. In the case of VLS NWs, even after aqua regia, Au impurity levels are found to induce impurity states in the bandgap. KPFM data, when normalized to the oxide-capacitance response, also identify a subset of VLS NWs with poor electrical contact due to nanogaps and short circuits when NWs cross that is not observed in AFM images or in current–voltage measurements when NWs are connected in parallel across electrodes. The experiments and analysis presented outline a systematic method for characterizing a broad array of nanoscale systems under device operation conditions.

Online supplementary data available from stacks.iop.org/Nano/23/405706/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon nanowires have played a key role in the development of nanoelectronic devices [1] and are a promising platform for further development of integrated functional nanosystems that, for instance, can probe local cellular behavior [2, 3]. Several prototype Si nanowire (NW) devices have been demonstrated, including: field effect transistors (FETs) [4–7], chemical and biological sensors [1, 8–11], thermoelectrics [12], and p–n junction devices and solar cells [13, 14]. Single-crystal Si NWs with controlled atomic structure have been grown using microelectronic compatible techniques [8, 9, 15, 16] allowing integration of nanoelectronic devices with microelectronic platforms for signal amplification and high throughput data analysis. For the majority of the above applications, the local surface electronic structure is a critical parameter in determining reproducible device performance. Fabrication processing methods have been shown to affect surface electronic structure and device performance. For example, the diffusion of Au into NWs is reported to introduce defect states into the energy bandgap that are observed locally on the surface [17], and the type of etching process has been demonstrated to affect mobility in Si NWs [9]. While Si NWs configured as FET device structures have frequently been characterized using current transport measurements [4, 6, 9, 10], this characterization method studies the collective electronic properties of the NW(s) in the conductive region and does not explore localized electronic

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properties that can be used to understand how defects affect reproducibility and reliability in nanoscale devices.

In this study we examine how the surface electronic structure in the vicinity of defects and impurities is affected under conditions of current flow across Si NWs using scanning Kelvin probe force microscopy (KPFM). KPFM since first introduced [18] has demonstrated great utility to characterize surface electronic phenomena on nanometer and even atomic length scales when performed in ultrahigh vacuum [19]. For example, KPFM has been used to characterize tandem solar cells [20], laser diodes [21], light emitting diodes [22], and chemical-sensitive FETs [23]. Local surface charge densities due to step edges [24, 25], surface defects [26], dipoles [27], dopant profiles [28], and trapped charge at interfaces [29] are measurable with KPFM. Dopant variations along Si NWs [30] and acceptor states [17] have also been measured with nanometer scale resolution using KPFM. This is complimentary to studies using Raman spectroscopy to measure global dopant behavior in NWs [31, 32] and scanning photocurrent microscopy studies measuring diffusion length with 100 nm resolution [33]. Very few papers have studied local electronic structure during conditions of current flow [34], but here we show that the combination of KPFM and current transport measurements can provide information regarding local electronic properties of Si NW devices under device operating conditions. KPFM can distinguish between impurity states in the energy bandgap and surface impurities since the former will exhibit a bias-dependent surface potential response and the latter will not. For example, methods to characterize local current flow as a function of position are particularly useful for systems such as branched NW structures [35].

AFM and KPFM data were acquired in a two-pass technique—topography followed by surface potential measurements in order to correlate electronic structure and morphology. The surface potential was measured on NW surfaces with and without a source–drain bias in order to investigate the surface electronic structure under device operation conditions. FET-integrated Si NWs in this study are fabricated by the ubiquitous methods of reactive ion etching (RIE) [8, 11] and vapor–liquid–solid (VLS) growth [7, 36] yet with the modification that the electrodes are predefined and NWs are crystallographically integrated with the electrodes. Impurities, surface states, open and short circuits could be identified in the devices using KPFM and were confirmed using SEM. RIE fabricated Si NWs exhibited local potential drops corresponding to defects that were either sensitive or insensitive to the applied bias. The former were associated with an impurity state in the energy bandgap and the latter type were consistent with surface contaminants introduced during the fabrication process. VLS-grown Si NWs also exhibited defects that were sensitive to applied bias and were attributed to residual Au incorporated in NWs despite an aqua regia etch. Fundamental studies of how localized charged defects affect surface potential and current transport along Si NWs in FET architectures are critical to gain insight into fabrication of robust devices with reproducible performance on this, or any, material platform. The methods and results illustrate how scanning KPFM links fabrication with local electrical properties and surface electronic structure in order to optimize fabrication methods on many promising NW based devices.

2. Results and discussion

2.1. Reactive ion etched Si NWs

The first Si NW fabrication method studies used e-beam (and optical) lithography to pattern NWs (and source and drain electrodes) on silicon-on-insulator (SOI) substrates [8, 11]. A schematic and optical microscopy images of the NW device is shown in figure 1(a). Si NWs are between the source (S) and drain (D) in the upper right image of figure 1(a), labeled on two connections for reference. These Si NW devices consist of a single NW between source and drain electrodes, all originally part of the same Si device layer on the SOI substrate. The Si NWs and source/drain were doped to a boron concentration of 10^{19} cm^{-3} and 10^{20} cm^{-3}, respectively and have a thermally grown oxide of approximately 3 nm in thickness on the surface. Al was deposited on the source and drain after removing the oxide from these regions and the sample was annealed to make ohmic contact between Al and Si as well as to passivate interface states between Si NWs and the thermal oxide. An AFM topography image of a Si NW device that was fabricated in this manner is shown in figure 1(b). The Si NW has a length of 20 μm, width of 200 nm, and height of 115 nm, and the height variation between NW and both source and drain electrodes is less than 5 nm. Figure 1(c) is a KPFM image of the Si NW at a source–drain bias (V_{SD}) of +1 V that was acquired using the two-pass technique.

KPFM measures the contact potential difference (CPD), defined as the difference between the work function of the sample surface and the tip work function for conductive surfaces. In the case of non-conductive surfaces and samples in ambient conditions, KPFM will also measure the surface charge between the tip and the underlying conductive substrate [37]. In figure 1(c), the surface potential is observed to decrease along the NW between the source and the drain electrodes. Dark regions corresponding to regions of locally low surface potential are observed on the NW surface in figure 1(c) and are highlighted with white arrows. In our experimental setup, a decrease in surface potential corresponds to an increase in the work function of the sample in the case of a conductive sample. In order to more clearly observe surface potential variations as a function of position along the NW, line profiles of the surface potential data were acquired along the NW at different source–drain biases, $V_{SD} = 0.25$ V (red dashed line), 0.50 V (green short-dashed line), 0.75 V (blue dotted line), and +1 V (cyan short-dashed line), and are shown in figure 1(d) from the lowest curve to the highest curve, respectively. The substrate is grounded, corresponding to a gate bias of zero.

CPD line profiles have been normalized by subtraction of data acquired at $V_{SD} = 0$ V (figure 1(d)) and data along the oxide surface between electrodes in the absence of a NW

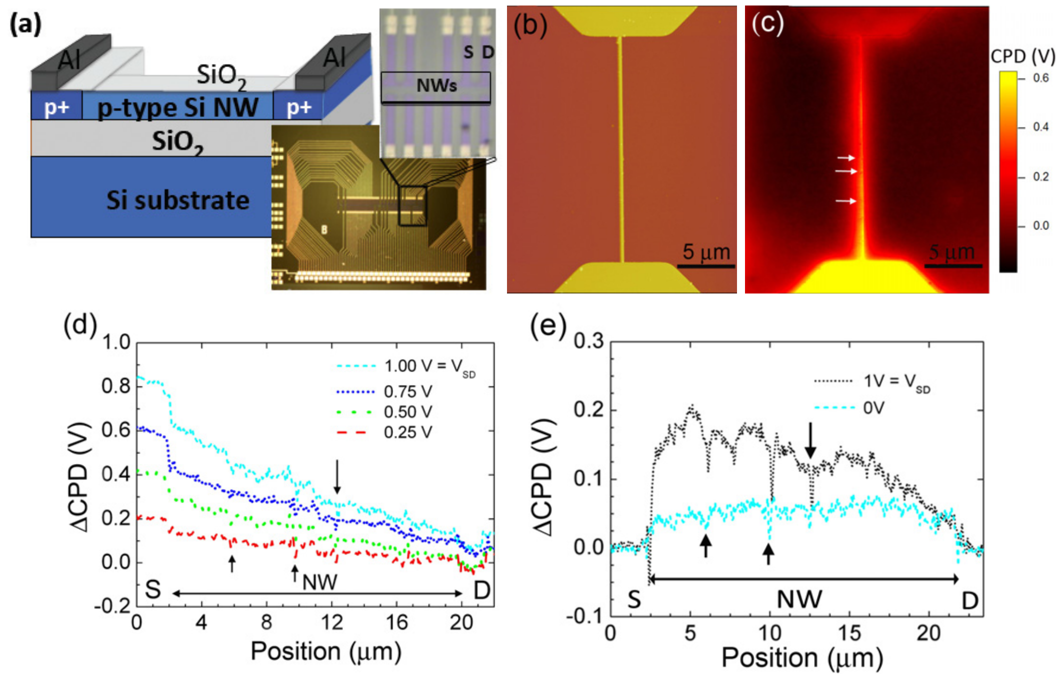

Figure 1. (a) Schematic and optical images of Si NW devices fabricated using RIE with a single Si NW between source and drain. (b) AFM and (c) KPFM images of RIE fabricated Si NW at $V_{SD} = +1$ V. (d) Surface potential line profiles along the NW and electrodes acquired at $V_{SD} = 0.25$ (red dashed curve), $V_{SD} = 0.50$ V (green dotted curve), $V_{SD} = 0.75$ V (blue short-dotted curve), and $V_{SD} = +1$ V (cyan short-dashed curve). 'S' and 'D' signify the location of the source and drain electrodes, respectively. (e) Oxide-normalized surface potential data acquired at $V_{SD} = 0$ V (cyan dashed curve) and $V_{SD} = +1$ V (black dotted curve).

(figure 1(e)), referred to as oxide normalized, to examine surface potential response of NWs due to applied bias. The raw CPD data are shown in supporting information 1 (available at stacks.iop.org/Nano/23/405706/mmedia) where the normalization process is further described. In figure 1(d), local decreases in surface potential are observed at zero applied bias and under a source–drain bias (illustrated with upward pointing arrows). In another region, a surface potential decrease is only observed with an applied bias (illustrated by the downward pointing arrow). The different behavior with applied bias indicates two different behaviors (or defect types) for local decreases in surface potential. In figure 1(e), the local decrease in surface potential becomes more apparent with applied bias across the source and drain, $V_{SD} = 1$ (black dotted line) in the oxide-normalized data; the local decreases in surface potential at $V_{SD} = 0$ V (cyan dashed line) is not easily distinguishable from measurement noise in this case. Note that although the surface potential decreases in figure 1(d) are small, they are observable in several independent measurements at the same location on the NW and so are not suggestive of measurement noise.

We measured five different Si nanowire devices fabricated in the same manner and found that the most prevalent defect was a decrease in surface potential that is observed at both $V_{SD} = 0$ V and under applied bias; some NWs exhibited more of these defects than others. Higher resolution AFM and KPFM measurements were performed on a Si NW exhibiting such a defect; a 1 μm × 1 μm KPFM image acquired at $V_{SD} = +1$ V is shown in figure 2(a). The vertical black line indicates the region where line profiles were acquired. KPFM images of the whole NW can be seen in supporting information 2 (available at stacks.iop.org/Nano/23/405706/mmedia). The vertical black line in figure 2(a) indicates the line over which the height and CPD line profiles were acquired. In figure 2(a), the arrow points to a region with a local decrease in surface potential on the Si NW near the drain electrode of magnitude 30 mV, as shown in the line profile of figure 2(c) (cyan triangles). A topographical protrusion is also observed at this same location and has a measured height of 7 nm as labeled in the topographic line profile of figure 2(b). While the tip–sample distance does influence the measured CPD due to non-local, cantilever–sample capacitive coupling [38–40], we can investigate the weight of this effect by measuring CPD variations associated with features on the neighboring oxide surface. The CPD variation for a topographic feature with a measured height of 10 nm on the oxide surface near the source is 4 mV with $V_{SD} = 0.75$ V and is not distinguishable from experimental noise. Thus it is not the change in the cantilever–sample distance that leads to the decrease in the measured CPD on the Si NW surface. The polarity of the source and drain were reversed ($V_{SD} = -1$ V) to examine if there is a bias-dependent response from the defect; the corresponding KPFM image of the whole NW is shown in supporting information 2b (available at stacks.iop.org/Nano/23/405706/mmedia). The surface potential line profile under $V_{SD} = -1$ V is shown in figure 2(c) (open black circles). The measured surface potential again decreases at this feature, this time by 40 mV instead of 30 mV when $V_{SD} = 1$ V. Since the noise in the measurements is at least 10 mV, the bias-independent surface potential decrease for the

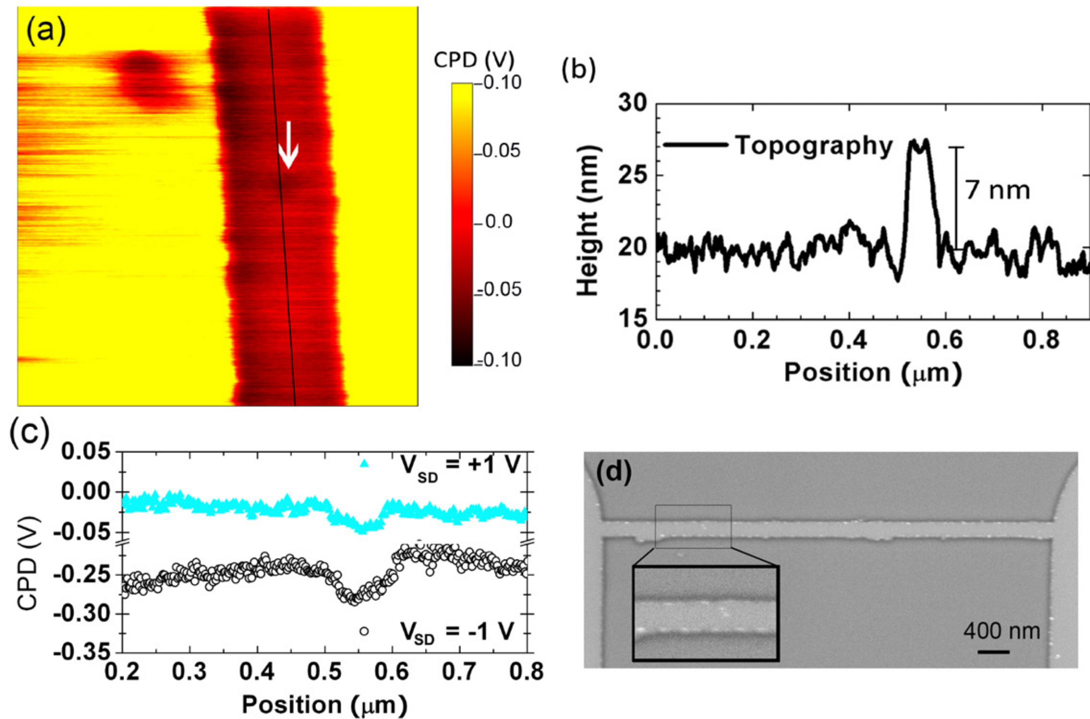

Figure 2. (a) 1 μm × 1 μm KPFM image of a Si NW fabricated by RIE. (b) Topography and (c) surface potential line profiles at $V_{SD} = +1$ V (cyan closed triangles) and $V_{SD} = -1$ V (black open circles) along the NW (highlighted with the vertical black line in (a)). (d) SEM image of the same NW acquired with an accelerating voltage of 3 kV and detector bias of 1 kV; the inset is a higher resolution region correlated with the scan region of (a).

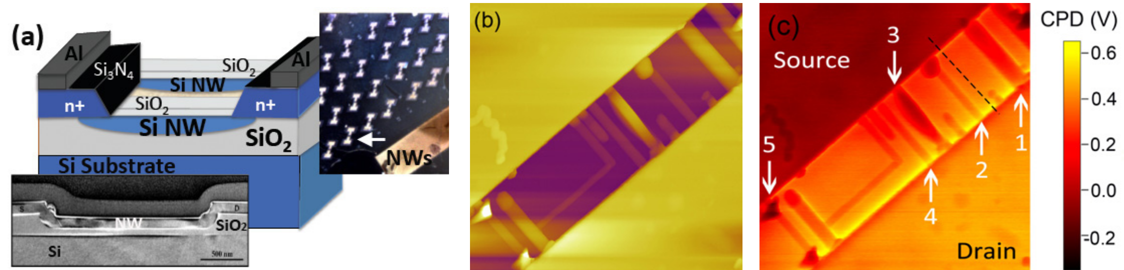

Figure 3. (a) Schematic, optical, and TEM images of a Si NW device fabricated via VLS growth across predefined electrodes illustrating multiple Si NWs between source and drain. 5 μm × 5 μm (b) AFM and (c) KPFM images acquired with $V_{SD} = +1$ V.

topographic feature is characteristic of a material with a higher work function.

An SEM image of the same Si NW in figure 2 was acquired using an energy selective backscattered filter and is shown in figure 2(d). The accelerating voltage was 3 kV, and the bias in the column was 1 kV in order to enhance elemental contrast where brighter features correspond to an element with heavier mass. Bright features are observed in the SEM image on the sides of the NW, and a few bright features are observed near the center of the NW at the location that correlates to the position of the topographic feature. Both the brighter features observed in SEM data and the higher work function observed in KPFM data are consistent with a surface contaminant. These likely result during the device fabrication process, for example, incomplete removal of material during processing steps, particularly since the feature is found along the perimeter of the NW, the source, and drain in the SEM image of figure 2(d).

2.2. VLS Si nanowires

The second Si NW fabrication method uses a combined top-down/bottom-up approach, which is detailed as referenced here [7, 36]. Optical lithography was used to define Si source and drain electrodes on a 100 nm thick, (001)-oriented, Si surface on an underlying buried oxide (BOX) layer on an SOI substrate. The source and drain were doped by ion implantation to a phosphorus concentration of 10^{19} cm^{-3} and Al was deposited to form the contacts to the source and drain. KOH was used to etch Si source and drain leaving {111} sidewalls. Colloidal Au nanoparticles with diameters of 40 and 100 nm were deposited on Si sidewalls. Au nanoparticles alloyed with Si sidewalls catalyzed VLS growth and governed the diameter of Si NWs. After NW growth, samples were soaked in aqua regia, which has been reported to remove Au nanoparticles. A thermal oxide was grown on Si NW surfaces and NWs were not intentionally doped. A schematic

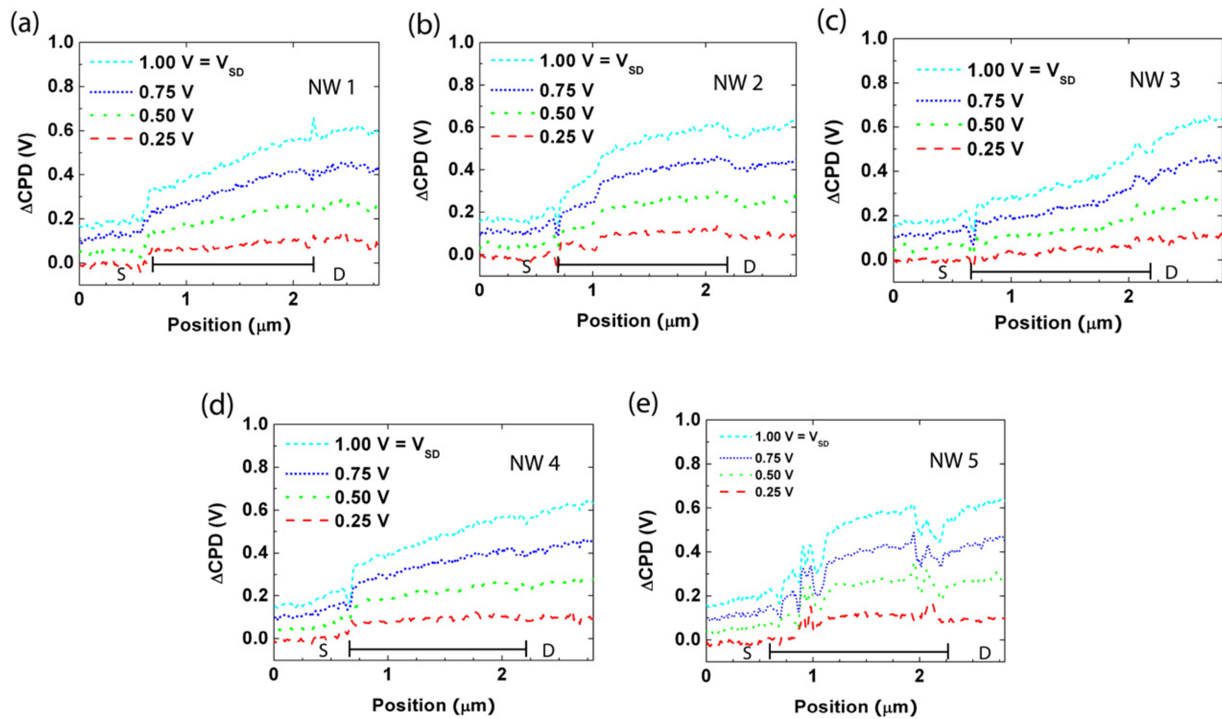

Figure 4. Surface potential line profiles from KPFM images acquired with $V_{SD} = 0.25$ (red dashed curve), $V_{SD} = 0.50$ V (green dotted curve), $V_{SD} = 0.75$ V (blue short-dotted curve), and $V_{SD} = +1$ V (cyan short-dashed curve) for NW1–NW5, (a)–(e), respectively. 'S' and 'D' signify the location of the source and drain electrodes, respectively.

of the device geometry is shown in figure 3(a) along with an optical image of the device regions and transmission electron microscopy (TEM) cross-sectional image of a NW fabricated in this manner.

A 5 μm × 5 μm AFM image and the corresponding 5 μm × 5 μm KPFM image acquired at $V_{SD} = +1$ V (figures 3(b) and (c), respectively) show several Si NWs between the source and the drain. Although VLS Si NWs have not been intentionally doped, positive surface charge density in SiO_2 on the order of 10^{12} cm^{-2}, leads to accumulation of electrons in the NW [41], making them effectively n-type. Unlike in figure 1(c) where the source and drain were p-type, in figure 3(c), the surface potential on the source is lower than the drain since the source and drain are n-type. Examination of the KPFM image of figure 3(c) illustrates that the measured surface potential is observed to vary across the NWs, and the variation is different from NW to NW.

In order to systematically examine the surface potential variations across NWs, line profiles are plotted from KPFM data that were acquired with V_{SD} ranging from 0.25 V to +1 V in 0.25 V increments and normalized as in figure 1(d). These normalized line profiles are shown in figure 4 for the NWs labeled NW1–NW5. The raw CPD data are shown in supporting information 3 (available at stacks.iop.org/Nano/23/405706/mmedia). These line profiles of NWs 1–5 demonstrate significant variations in their surface potential. The surface potentials of NW1, NW3, and NW4 exhibit ohmic behavior and exhibit only small discontinuities at the NW–source and NW–drain interfaces. Some possible contributions to the discontinuity in surface potential at these NW–source and NW–drain interfaces are differing doping density [30], occupied interface states [42], and the height variation between NW (and oxide trench) and source/drain electrodes [38, 39]. A topography line profile across NW4 in figure 4(b) is shown in supporting information 4 (available at stacks.iop.org/Nano/23/405706/mmedia); the NW is approximately 225 nm lower than the source/drain. Although the data acquisition is performed in constant height mode, maintaining constant height while scanning features with abrupt height variations is limited by the system feedback and cantilever geometry [38]. Overall, height discontinuities, contact resistance, and localized charge at interfaces can contribute to the discontinuity in surface potential at the interfaces.

The ohmic behavior of NW1, NW3, and NW4 is consistent with behavior observed in similar devices fabricated with the same protocol and source/drain doping density, in which appreciable drain current was measured across NWs with zero applied gate bias (the gate bias is also zero in data shown here) [7, 36]. Thus, the near linear surface potential response with applied V_{SD} observed for NW1, NW3, and NW4 is reasonable. Non-ohmic behavior, however, was observed in NW2 and NW5 in figures 4(b) and (e), respectively.

The non-linear surface potential response of NW2 and NW5, observed in the line profiles of figure 4, was examined more closely with a higher resolution 1 μm × 1 μm KPFM measurement, which was performed on a NW with similar non-linear characteristics. These measurements are shown in figure 5. KPFM images of the boundary between a NW,

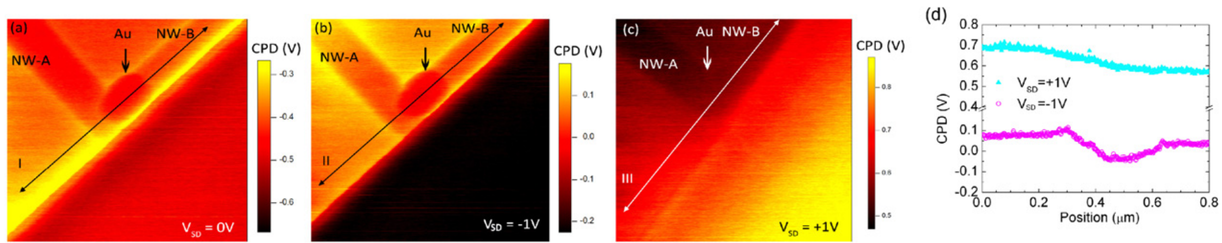

Figure 5. 1 μm × 1 μm KPFM images of VLS Si NW and electrode at (a) $V_{SD} = 0$ V, (b) $V_{SD} = -1$ V, and (c) $V_{SD} = +1$ V. (d) Surface potential line profiles acquired across lines in (b) and (c) with $V_{SD} = -1$ V (fuchsia open circles) and $V_{SD} = +1$ V (solid cyan triangles), respectively.

labeled NW-A, and source were acquired at $V_{SD} = 0$ V (figure 5(a)), $V_{SD} = -1$ V (figure 5(b)), and $V_{SD} = +1$ V (figure 5(c)). These images reveal a second NW (labeled NW-B) that has grown perpendicular to NW-A. There have been reports suggesting that a VLS-grown NW kinks thereby changing growth directions when the gold catalyst migrates from the tip to the side of the NW [43]; this was likely the case in this instance and is described in [36]. Line profiles (figure 5(d)) at $V = 1$ V (cyan closed triangles) and -1 V (fuchsia open circles) were taken along NW-B; the line is shown in figures 5(a)–(c) and the intersection point of NW-A and NW-B occurs near the center of this line.

The surface potential response at the junction of NW-A and NW-B appears to be bias dependent since there is a 130 mV CPD decrease when $V_{SD} = -1$ V but there is not one when $V_{SD} = 1$ V. The junction between NW-A and NW-B appears to be associated with an acceptor type defect since these defects are either neutral or negatively charged. This result is in agreement with a previous study that identified acceptor states in Si NWs that were attributed to Au induced states in the energy bandgap resulting from Au catalyzed VLS growth [17]. Although the Si NWs have been treated with aqua regia, residual Au may be incorporated into the NW during growth or diffusion from the surface inward during annealing, thereby not removed during etching [44]. Thus, these localized depressions in surface potential at the junctions of the Si NW-A and NW-B are attributed to states induced in the NW from diffusion of Au from the catalysts into the NW and we also attribute the decreases in surface potential at the NW–source/drain interfaces observed in figures 4(b) and (e) to have a contribution from Au impurity states.

In order to de-couple the surface potential response of the NWs as a function of V_{SD} from that of the capacitance of the thermal oxide, oxide-normalized data are plotted [45]. The oxide trench also exhibits a bias-dependent CPD response; a capacitive response of the underlying oxide layer due to applied V_{SD}, see supporting information 3 (available at stacks.iop.org/Nano/23/405706/mmedia). The oxide-normalized surface potential line profiles of NWs 1–5 are shown in figures 6(a)–(e), respectively. The oxide-normalized surface potential line profiles of NWs 1, 3, and 4, shown in figures 6(a), (c), and (d), respectively, exhibit a systematic decrease in surface potential with increasing V_{SD}. Thus injection of electrons in the NW results in a surface potential decrease; the opposite is observed in the p-type RIE fabricated wires shown in figure 1(e). This is reasonable since the carriers have opposite charge and carrier accumulation will lead to the opposite surface potential response. Considering that the magnitude of the surface potential is related to charge flow, the normalized surface potential variation in response to V_{SD} indicates that the resistance of NW3 $<$ NW1 $\leq$ NW4. NW2 and NW5 demonstrate only minimal changes in their surface potential for $V_{SD} > 0$ V in comparison to the oxide trench, as observed in figures 5(b) and (e), respectively, with the exception at the NW–source interfaces that has been attributed to residual Au and Au defect states in Si. This minimal bias-dependent change in the oxide-normalized surface potential profiles of NW2 and NW5 suggests that these NWs are not well connected to both source and/or drain.

Further analysis was performed to investigate the variation in the oxide-normalized surface potential line profiles. SEM images of two different VLS Si NWs on different device regions are shown in figures 7(a) and (b). The SEM images clearly show that the NW in figure 7(a) is connected to both electrodes whereas the NW in figure 7(b) makes physical contact with only one electrode. The differences in physical connections of the two NWs of figures 7(a) and (b) suggest the two NWs should display markedly different surface potential response with an applied bias. Figures 7(c) and (d) show the normalized surface potential line profiles (normalized with respect to $V_{SD} = 0$ V) for the connected NW and disconnected NW, respectively. The line profiles do not exhibit significant differences that make it clear which NW is disconnected. Both NWs have a change in slope in the normalized surface potential that is highlighted by the vertical downward arrow in both figures 7(c) and (d); yet the origin of this change in slope is not clear in the surface potential data.

The oxide-normalized surface potential line profiles for the connected NW, figure 7(e), show a clear decrease in surface potential for the data acquired at $V_{SD} = +1$ V (cyan closed triangles) when compared to that acquired at $V_{SD} = 0$ (black open circles). The oxide-normalized surface potential line profiles for the disconnected NW, shown in figure 7(f), when acquired with $V_{SD} = +1$ V (cyan closed triangles) and $V_{SD} = 0$ V (black open circles) are both zero on average. Thus, the surface potential of this disconnected NW does not differ significantly from the oxide trench under applied

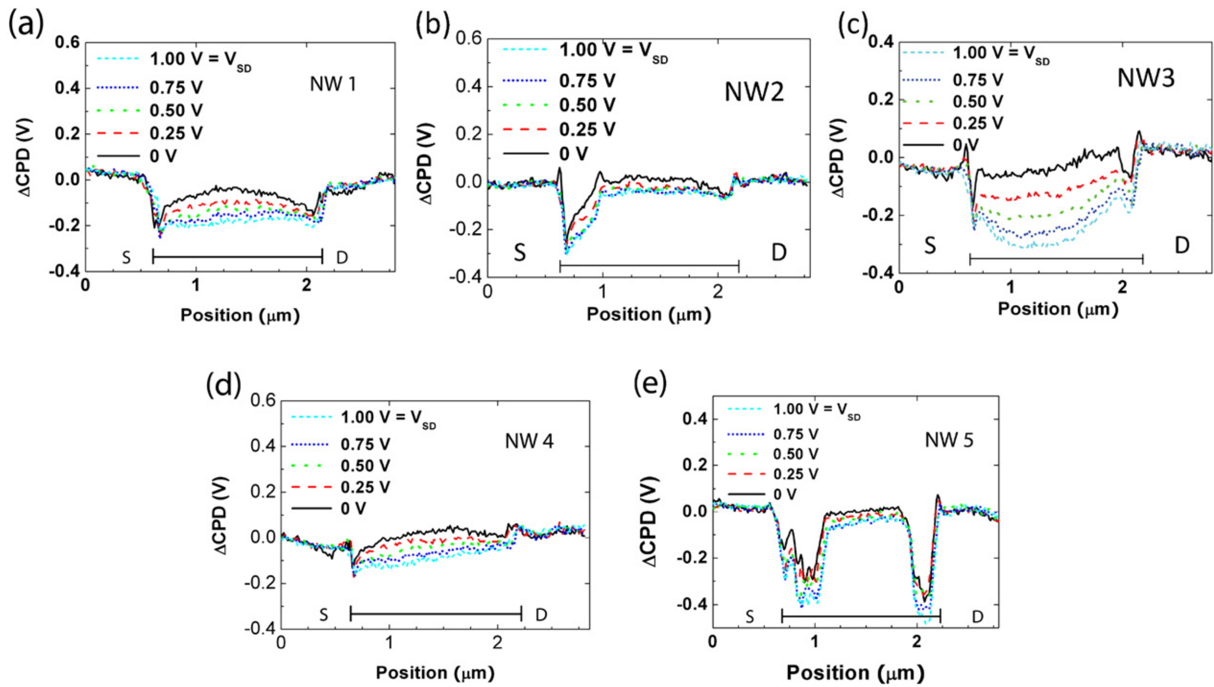

Figure 6. Oxide-normalized surface potential line profiles from $V_{SD} = 0$ V (black solid line), $V_{SD} = 0.25$ (red dashed curve), $V_{SD} = 0.50$ V (green dotted curve), $V_{SD} = 0.75$ V (blue short-dotted curve), and $V_{SD} = +1$ V (cyan short-dashed curve) of (a) NW1, (b) NW2, (c) NW3, (d) NW4, and (e) NW5 as labeled in figure 3(c).

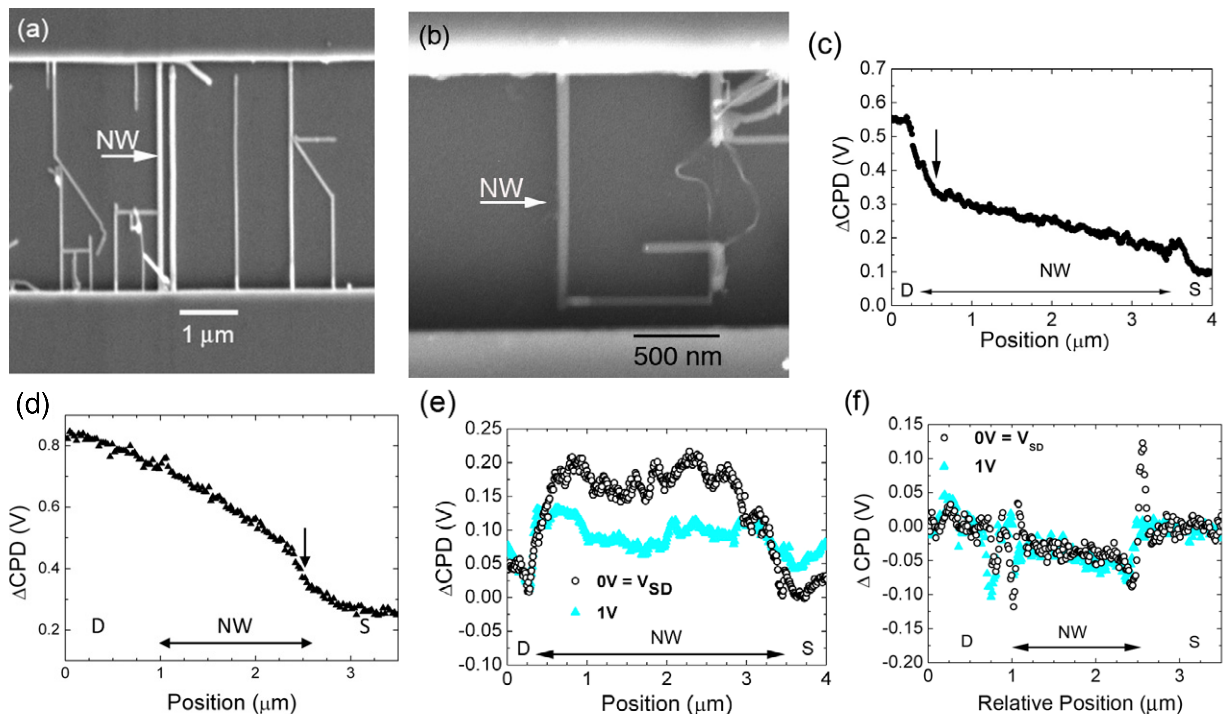

Figure 7. (a), (b) SEM images of VLS fabricated NWs. (c), (d) Surface potential line profiles that were acquired across the NWs at $V_{SD} = +1$ V for the NWs highlighted with a horizontal arrow in (a) and (b), respectively. The downward arrows highlight regions with a change in slope. Oxide-normalized surface potential line profiles acquired at $V_{SD} = 0$ V (black open circles) and $V_{SD} = +1$ V (cyan closed triangles) across (e) the NW shown in (a) and (f) the NW shown in (b).

bias and changes in KPFM data of the disconnected NW are attributable to the oxide capacitive response to V_{SD} and are not related to current flow in the NW. The open circuit can only be identified in the oxide-normalized surface potential response. The gap between the NW and source is only resolvable in SEM images (figure 7(b)) and not resolvable in the AFM

topography or KPFM surface potential data (that has not been normalized) due to the height of the sidewalls. By correcting for contributions from the oxide capacitance, NWs with poor electrical connections have significantly different surface potential response to an applied bias than NWs connected to both electrodes and this type of normalization can be used to identify open circuits. From the oxide-normalized data shown in figure 7(e), we also notice that the surface potential drops to zero at the position where the NW crosses another NW (diagonal NW at the bottom center of the SEM image of figure 7(a)). The oxide-normalized surface potential indicates the presence of a short at this point. Thus, evaluation of the NW surface potential response as a function of applied V_{SD} provides information on local electrical contacts.

3. Conclusion

In this study, Si NWs were fabricated using RIE and VLS growth and these devices were characterized with AFM, KPFM, and SEM to examine how fabrication affects morphology, surface electronic structure, and current transport. KPFM measures surface potential with nanoscale lateral resolution and was used to probe local electronic properties as a function of source–drain bias alongside AFM for correlation with the fabrication method. Impurities, although originating from different processes, on both types of NWs led to variation of the surface potential locally around the impurity. RIE fabricated NWs exhibit two types of defects. Those associated with a small bias-independent surface potential decrease were related to impurities on the surface that are primarily found near the edges of features in SEM images. These surface impurities are characteristic of the fabrication process since they were not observed on VLS NWs. Other impurities exhibited a local decrease in surface potential that was bias dependent and these were attributed to defects that induce acceptor states in the energy bandgap since they are negatively charged or neutral. VLS fabricated Si NWs also exhibited defects with a surface potential response in KPFM data consistent with acceptor states; the defect states in this case were attributed to Au diffusion in NWs during VLS growth. While the lateral resolution of the AFM tip was not sufficient to verify the physical connection between NWs and electrodes or in some cases image regions where NWs cross, oxide-normalized KPFM data were able to identify open circuits and short circuits, respectively, that were confirmed in SEM images as well as giving an indication of the relative resistances of the NWs. In summary, KPFM data when used in conjunction with traditional current–voltage measurements can identify open circuits, short circuits, and differentiate between impurity-induced states in the energy bandgap versus impurities on the surface. The normalization method presented will be applicable to a variety of device structures that include insulators as surface passivating layers, ionic devices based on oxide materials, or in electronic devices fabricated on SOI substrates.

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