A Fully Integrated RF-Powered Energy-Replenishing Current-Controlled Stimulator

Sohmyung Ha, *Member, IEEE*, Chul Kim, *Member, IEEE*, Jiwoong Park, *Student Member, IEEE*, Gert Cauwenberghs, *Fellow, IEEE*, and Patrick P. Mercier, *Senior Member, IEEE*

***Abstract*—This paper presents a fully-integrated current-controlled stimulator that is powered directly from on-chip coil antenna and achieves adiabatic energy-replenishing operation without any bulky external components. Adiabatic supply voltages, which can reach a differential range of up to 7.2 V, are directly generated from an on-chip 190-MHz resonant LC tank via a self-cascading/folding rectifier network, bypassing the losses that would otherwise be introduced by the 0.8 V system supply-generating rectifier and regulator. The stimulator occupies 0.22 mm^2 in a 180 nm silicon-on-insulator process and produces differential currents up to 145 μA. Using a charge replenishing scheme, the stimulator redirects the charges accumulated across the electrodes to the system power supplies for 63.1% of stimulation energy recycling. To benchmark the efficiency of stimulation, a figure of merit termed the stimulator efficiency factor (SEF) is introduced. The adiabatic power rails and energy replenishment scheme enabled our stimulator to achieve an SEF of 6.0.**

***Index Terms*—Adiabatic stimulation, brain initiative, electrocorticography, neuromodulation, neural stimulation, neural technology.**

I. Introduction

IMPLANTED electrical neural stimulators (neuromodulators) are devices that inject electrical current into neural tissue via at least two electrodes to either alter the firing conditions of the underlying neurons, or directly induce action potentials. Such devices have been successfully deployed in a wide assortment of applications ranging from stimulation of cortical or deep brain regions to treat neurological disorders like Parkinson's Disease, dystonia and epilepsy [1]–[5], stimulation of sensory cells to restore sensations like hearing or vision in patients who are profoundly deaf or blind [6]–[9], stimulation of the spinal cord to treat chronic pain [10], [11], and beyond [12]. Next-generation neural stimulators are beginning to increase the spatial resolution of stimulation via higher electrode density designs that will enable more precise therapy across a wide range of applications [13]–[16], while also exploring new directions such as vagus nerve stimulation for targeted pharmaceutical replacement (i.e., electroceuticals) [17].

In all cases, implanted neural stimulators have two important constraints that must be met for long-term use in humans: 1) devices must be sufficiently small to fit within natural human anatomy without significantly damaging or displacing surrounding tissue; and 2) devices must dissipate low power such that local temperature increases do not exceed safety limits [18]. In addition, most practical devices prefer fully wireless operation to minimize the risk of infection otherwise posed by transcutaneous electrical conduit, thereby necessitating either embedded battery power, transcutaneous wireless power transmission (WPT), or both [19]–[26]. Since the overall area or volume of implanted neural stimulators are often dictated by the size of energy storage or power-receiving elements (i.e., the battery or WPT coil), whose size in turn are primarily dominated by the average power consumption of the implant itself, minimizing the power dissipation of the implant can be an impactful way to minimize implant size, tissue heating, or potentially both at the same time. In many prior-art neural stimulators, power dissipation is dominated by the energy consumed per stimulation event [27]–[32], and thus improving the energy efficiency of stimulation can yield significant device-level power reductions. Unfortunately, it is conventionally difficult for neural stimulators to be both small and energy efficient at the same time. Conventional constant-current stimulators can be implemented in a small area using integrated circuit technology, yet dissipate substantial power across the current source itself when powered by a DC supply voltage. Recently developed millimeter-sized stimulation systems [25], [33], [34] were implemented with off-the-shelf discrete components so that their power efficiencies were compromised with simplicity in implementation. On the contrary, adiabatic stimulators, which slowly ramp the supply voltage up and down to minimize the voltage drop across the current source and recycle charge from electrode and tissue capacitance as described in Section II-C, can be more energy efficient, yet typically require large off-chip passives to synthesize the adiabatic voltage waveforms [28], [35].

In addition to size and efficiency challenges, it is conventionally difficult to generate the large compliance voltages necessary to support constant-current stimulation across large

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S. Ha was with the University of California San Diego, La Jolla, CA 92093-0021 USA. He is now with New York University Abu Dhabi, Abu Dhabi 129188, UAE, and also with the New York University, Brooklyn, NY 10012 USA (e-mail: sohmyung@nyu.edu).

C. Kim, J. Park, G. Cauwenberghs, and P. P. Mercier are with the University of California San Diego, La Jolla, CA 92093-0021 USA (e-mail: kimchul1484@gmail.com; jip049@ucsd.edu; gert@ucsd.edu; pmercier@ucsd.edu).

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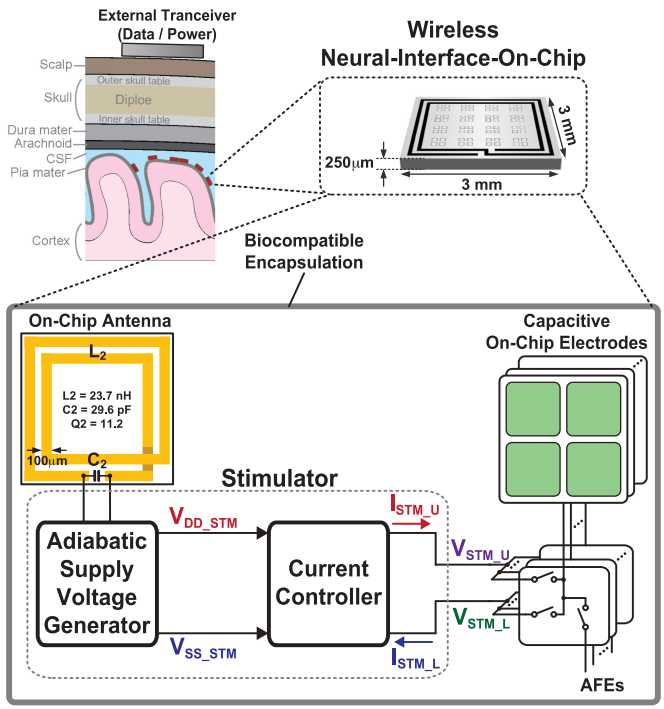


Fig. 1. Overall block diagram of the stimulator that is integrated in a encapsulated neural interfacing acquisition chip (ENIAC).

ranges of electrode and tissue impedances. This is typically accomplished in wirelessly-powered systems via a two-step rectification/boosting (and/or regulation) process that introduces cascaded losses and further degrades efficiency. As next-generation neural stimulation devices continue to shrink in size [25], [33], [34], [36], in some cases via full on-chip integration of all necessary neuroinstrumentation functionality [37], [38], inclusion of energy-efficient adiabatic stimulation functionality is necessary in a small, fully-integrated form factor.

This paper presents an adiabatic current-controlled stimulator architecture, depicted in Fig. 1, that achieves efficient, single-step waveform synthesis, and is fully-integrated on-chip with no external components necessary. Here, adiabatic waveforms are synthesized directly from an on-chip resonant coil by cascading and folding auxiliary rectification stages according to stimulation voltage needs. A prototype of the design is fabricated in a 0.18 μm silicon-on-insulator (SOI) CMOS process, and measurement results reveal the architecture achieves a large output voltage compliance at high efficiency, all in a single fully-integrated chip. This paper has been extended with additional materials and more comprehensive explanation on stimulation methods and circuits compared to the previously published conference proceeding [37]. While [38] reviews current ECoG interface technology and gives an overview of the whole system and [39] presents its wireless power transmission and regulating rectifier circuits, this paper presents circuit-level detail in the implementation of the stimulator with more extensive characterization and analysis of performance.

The paper is organized as follows. In Section II, we describe and compare representative stimulation methods highlighting how adiabatic stimulation using dynamic power rails improves energy efficiency. Section III then presents design details of the proposed adiabatic stimulator, while Section IV presents measurement results. To evaluate the effectiveness of stimulation and benchmark against prior-art, this paper reviews the theory behind adiabatic stimulation and proposes an energy-efficiency figure of merit in Section V. Finally, Section VI concludes the paper.

II. Electrical Stimulation Methodologies

Generation of action potentials in underlying neurons through electrical stimulation is typically achieved by passing a sufficient amount of charge to the membranes of neurons. The energy efficiency of neural stimulation strongly depends on the voltage and current waveform of the generated stimulus waveforms, and the characteristics of the employed electrodes [40]–[43]. Historically, neural stimulation has been accomplished using either constant-voltage or constant-current waveforms due to their relatively simple implementations and demonstrated clinical effectiveness [44]. However, such approaches can suffer from unpredictable charge delivery and/or significant inefficiencies. This section describes the advantages and disadvantages of conventional and emerging stimulation methodologies.

A. Constant-Voltage Stimulation

Clinical stimulation devices, for example, those used in deep brain stimulation, traditionally utilized constant-voltage (voltage-controlled) stimulation due to its simplicity in implementation [45], [46]. In constant voltage stimulation, power supplies or DC voltage sources such as V_{DD} and V_{SS} are directly connected to the electrode as shown in Fig. 2(a). The only required components on the stimulator side are just voltage sources at desired voltage levels.

The resulting stimulation current is determined by the stimulation voltage divided by the impedance summations of the electrode, electrolyte, and tissue. As a result, the amount of current delivered to the neuron depends on the impedances based on Ohm's law ($I = V/Z$). Since the impedance of tissue and electrode-tissue interfaces can vary across patients and also with time, the current varies accordingly and its variation is difficult to estimate [47]–[49].

Furthermore, due to the capacitive component of the electrode impedance, the current has an exponentially decaying waveform as shown in Fig. 2(b). Thus, the total delivered charge to the tissue during a stimulation pulse is quite difficult to estimate, and the total charge is difficult to be balanced, which may lead to generation of toxic byproducts and electrode degradation over time.

B. Constant-Current Stimulation

For better controllability of the amount of charge delivered during stimulation, most recent neural stimulators utilize constant-current (current-controlled) stimulation. By doing so, a constant-current stimulator can provide a set amount of charge to the tissue and evoke desired response regardless of the electrode and tissue impedances, which are unknown and can vary

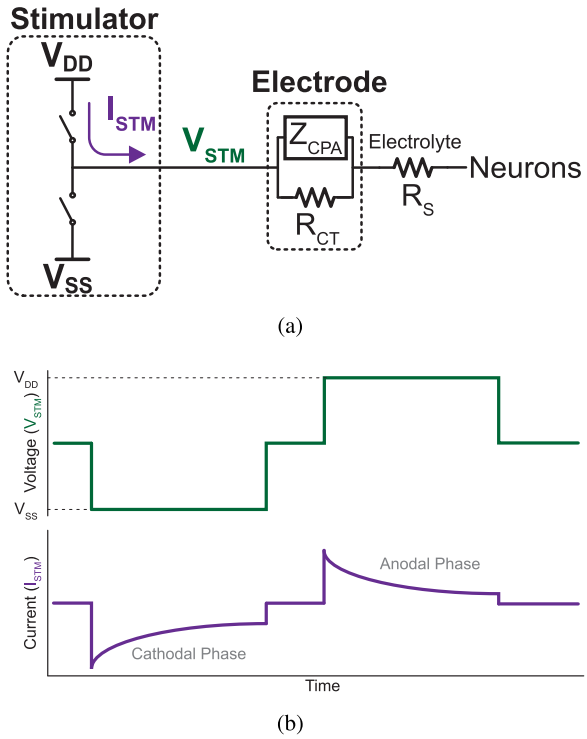


Fig. 2. (a) Simplified configuration and (b) voltage and current waveforms of constant voltage stimulation.

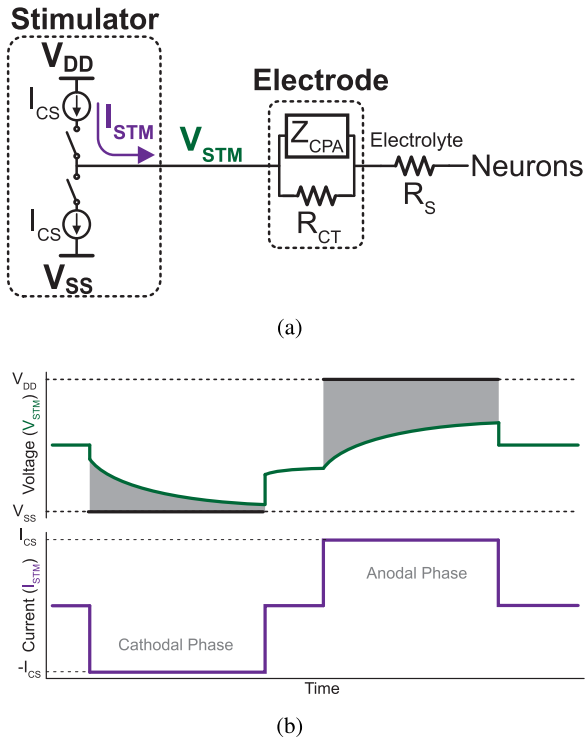


Fig. 3. (a) Simplified configuration and (b) voltage and current waveforms of constant current stimulation.

over time [44]–[46]. As illustrated in Fig. 3, a constant current delivered to an electrode results in a ramping electrode voltage. If a high impedance is encountered either in the electrode or within tissue, high voltage compliance (i.e., a large DC supply) is required for the current source.

In such constant current stimulators, the voltage drop across the current source (i.e., between the DC supply and the ramping electrode voltage), represented by the gray shaded region in Fig. 3(b), is energy that is not delivered to tissue, but that is instead dissipated as heat across the current source. As a larger compliance voltage is needed to tolerate a wider range of impedances, the energy wasted across the current source gets much larger. Thus, while constant-current stimulators are generally preferred over constant-voltage stimulators due to increased robustness, they tend to be quite energy inefficient.

C. Constant-Current Adiabatic Stimulation

To improve the efficiency of constant-current stimulation, it is important to recognize that it is not strictly necessary to operate the stimulating current sources from a fixed supply voltage. An impactful way to reduce unnecessary losses is to operate the current sources from variable supply voltages that closely track the output voltage in order to minimize the voltage drop across the current source. Fig. 4 illustrates a nearly-ideal temporal supply voltage for such an adiabatic stimulation arrangement.

Unlike in the case of conventional constant-current stimulation (Fig. 3), which draws current during the cathodal phase from a fixed supply rail, V_{SS}, while the electrode voltage, V_{STM}, decreases, here, a variable supply rail, $V_{SS\_Adiabatic}$, is generated

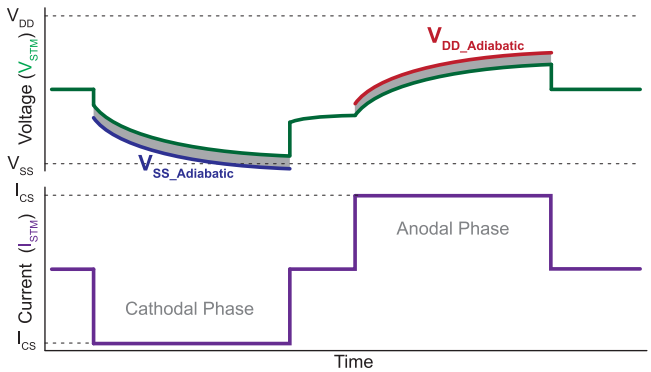


Fig. 4. Voltage and current waveforms of adiabatic stimulation.

such that it dynamically follows the trajectory of the electrode voltage with a small gap, sized to be just large enough to make sure the current source remains in saturation. After the cathodal phase, an anodal phase follows where a constant current is injected from another dynamic supply rail, $V_{DD\_Adiabatic}$. In doing so, $V_{DD\_Adiabatic}$ increases as the electrode voltage increases. By minimizing the voltage gap between the supply voltages and the electrode voltage, energy loss across the current sources can be minimized.

Despite its higher energy efficiency, the adiabatic stimulation method has not been widely deployed in practice, largely due to the complexity and/or size and energy overhead of the circuits needed to create the adiabatic voltage rails. For example, [28] sequentially switch electrodes between a bank of off-chip capacitors, each biased at increasingly large voltage steps, in order to synthesize a step-wise approximation to a slow voltage ramp.

In contrast, [35] synthesized adiabatic ramp waveforms though a forward-buck/reverse-boost DC-DC converter utilizing an off-chip inductor. As such, despite achieving excellent energy savings, most prior art relied on bulky external components such as capacitors [28] or inductors [35], or alternatively cascade several power converters, each with substantial loss mechanisms, in order to synthesize the required waveforms [50]. The stimulator in [51] relied on comparison at the RF frequency so that it is limited to applications with low frequency (<10 MHz) RF input.

The following section will present details of the proposed fully integrated stimulator, which synthesizes adiabatic supply rails directly from an on-chip LC tank resonating at 190 MHz, and furthermore recycles the charge stored on the electrode capacitance and delivers it back to V_{DD} in order to further increase energy savings.

III. Design Details of the Stimulator

A. Overall Architecture

The proposed stimulator is integrated into a single-chip neural interfacing system termed ENIAC: an encapsulated neural interfacing and acquisition chip [37], [38]. ENIAC includes an on-chip antenna for wireless power and data telemetry, 16 electrodes on the top metal, and all circuitry required for wireless neural recording and stimulation. An illustration ENIAC, along with a stimulator top-level block diagram, is shown in Fig. 1.

The stimulator consists of two major blocks: an adiabatic supply voltage generator, and a constant-current controller. The adiabatic supply voltage generator generates two adiabatic supply voltages, V_{DD_STM} and V_{SS_STM}, directly from the on-chip LC resonant tank. From the two adiabatic supplies, the current controller supplies constant differential currents, I_{STM_U} and I_{STM_L}. The currents flow to the on-chip electrodes through switch multiplexers, which connect the electrode either to the stimulator or to the analog front-end (AFE) used for neural recording. The electrodes, formed by the top-metal layer of the CMOS chip, should be coated with a high-k dielectric material to construct a capacitive electrode, which also enables eliminating any net DC charge transfer. In addition, a capacitive electrode does not have a parallel resistive components, which models a faradaic current. Thus, there is minimal I^2R-based energy dissipation in electrodes while the energy is stored across the electrode by CV^2 instead. The total amount of charge that can be delivered per stimulation phase in capacitive electrodes is proportional to the electrode capacitance and the total voltage rail that the stimulator can generate [38]. While conventional stimulators use high voltage supplies and current sources in a high voltage process, which may lead to poor power and area efficiencies, the proposed stimulator enables both high area- and power-efficiency at high compliance voltage with the strategies described in the following sub-sections.

B. Stimulation Principle

The operational principle of adiabatic stimulation with ENIAC is described in Fig. 5. The stimulation process is composed of two phases: 1) energy provision and 2) energy replenishment. During the first phase, the adiabatic supply voltage generator produces the adiabatic supply voltages, and the differential constant currents flow to differential electrodes as shown on the top side of Fig. 5. Since the electrodes are capacitive in ENIAC, the voltages at the electrode V_{STM_U} and V_{STM_L} increase and decrease linearly as the constant stimulation currents flow through them. During this phase, energy is provided by the stimulator to the tissue through the electrodes. However, a significant amount of the provided energy is accumulated across the capacitive electrodes.

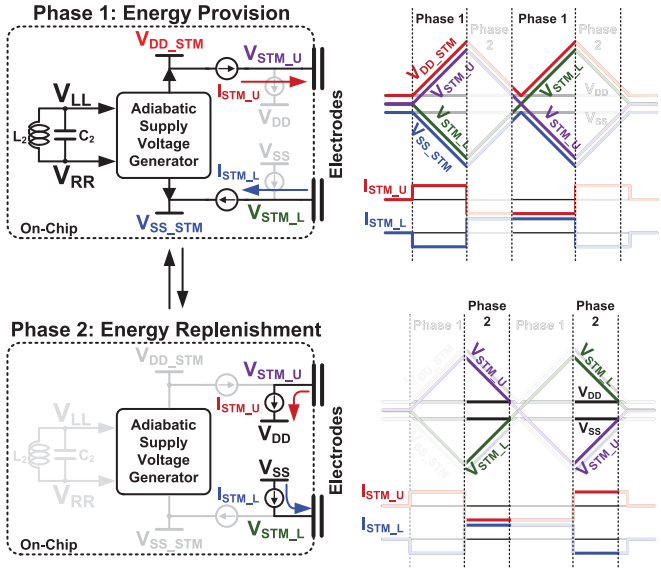


Fig. 5. Conceptual illustration of the adiabatic stimulation [38].

To simplify discussion, a single-ended equivalent model for the proposed adiabatic capacitive stimulation approach, valid over the first phase of stimulation, is illustrated in Fig. 6(a). Here, a constant stimulation current, I_{STM}, is provided to the tissue, modeled as resistor R_{TIS}, through the electrode capacitor, C_{EL}. Because I_{STM} is constant over the stimulation time, T_{STM}, the electrode voltage, V_{STM}, increases linearly as shown in Fig. 6(b). To not waste energy, the adiabatic supply voltage, V_{DD_STM}, ramps up following V_{STM} with a voltage gap ΔV, which is effectively applied across the current source.

The energy provided by the current source and the energy dissipated and/or stored by the elements can be found by computing the areas denoted in Fig. 6(b) because the current is constant over the period of interest. The total energy provided by the current source over time T_{STM} can be calculated as:

$$E_{CS} = \frac{1}{2}\{(\Delta V + V_{TIS}) + (V_H + \Delta V + V_{TIS})\} \times I_{STM} \times T_{STM} \quad (1)$$

where $V_{TIS} = I_{STM} \cdot R_{TIS}$. Since $I_{STM} \cdot T_{STM} = C_{EL} \cdot V_H$, the above equation can be rewritten as:

$$E_{CS} = V_{TIS} I_{STM} T_{STM} + \Delta V I_{STM} T_{STM} + \frac{1}{2} C_{EL} {V_H}^2. \quad (2)$$

Here the first term is the energy transferred to the tissue as highlighted with the blue shadow in Fig. 6(b). The second term

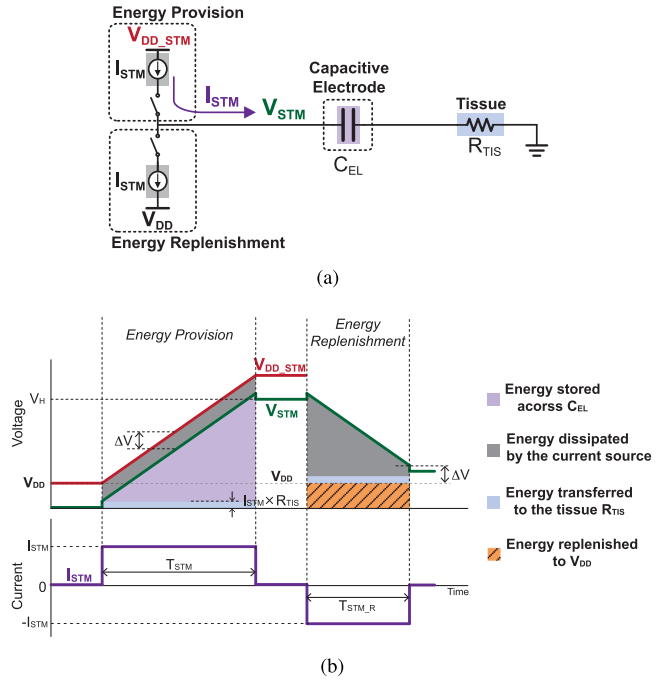


Fig. 6. Energy usages for adiabatic stimulation. The purple shaded region indicates the energy stored across the capacitive electrode, the gray the dissipated energy at the current source, and the blue the energy delivered to the tissue.

and the gray shaded area in Fig. 6(b) represent the energy dissipated across the current source. The last term is the energy stored across the capacitive electrode corresponding to area of the purple shadow with a triangular shape in Fig. 6(b).

As shown, a significantly large part of the provided energy by the stimulation is actually accumulated across the electrode. The energy transferred to the tissue (the first term) is typically much smaller compared to the other two terms. When ΔV is minimized in adiabatic stimulation, almost all provided energy is stored across the capacitor at the end of this stimulation period. For example, assume a realistic case when $I_{STM} = 50\ \mu$A, $R_{TIS} = 1$ kΩ, $\Delta V = 0.5$ V, $T_{STM} = 1$ ms, $C_{EL} = 10$ nF, and $V_H = 5$ V. In this case, the stored energy in the capacitive electrode is 125 nJ, the dissipated energy at the current source 25 nJ, and the transferred energy to the tissue 2.5 nJ, while the total energy provided by the stimulator is 152.5 nJ. In this example, 82% of the provided energy is stored across the electrode.

Interestingly, after the first phase of stimulation, conventional stimulators (and, for that matter, conventional digital CMOS logic, which operates on a similar principal) draw the charge down to a negative supply voltage or ground. In doing so, all of the energy stored in the capacitor is discarded to the lowest potential of the stimulator system, and therefore wasted.

To further improve efficiency above the gain introduced by the ramping adiabatic rails, the presented stimulator replenishes the energy nominally stored within the electrode capacitance, and delivers this energy back to the supply rails. The waveforms for energy replenishment as shown in Phase 2 of Fig. 5. Here, the stored electrode charge accumulated during the first phase of stimulation is delivered to the power supplies of the system instead of being directly dumped (and thus wasted) to V_{SS}. Here the capacitive electrode accumulated with the positive voltage, V_{STM_U}, delivers charge to V_{DD}, while the other electrode takes charges from V_{SS}. By doing so, the replenished energy can be reused by other circuits in the system. Since the replenished energy comes back to the system power supplies (V_{DD} and V_{SS}), this contributes to system-level power efficiency.

The various components of energy transfer occurring during replenishment is illustrated in Fig. 6. During the energy replenishment phase, charge accumulated in the electrode flows back to the main system supply, V_{DD}. The time period when V_{STM} is larger than $V_{DD} + \Delta V$, denoted by T_{stm_r}, which enables current flow from the electrode to V_{DD}, can be calculated as follows:

$$T_{STM\_R} = \frac{V_H + V_{TIS} - V_{DD} - \Delta V}{V_H} \cdot T_{STM}. \quad (3)$$

The replenished energy E_R is:

$$E_R = V_{DD} I_{STM} T_{STM\_R}. \quad (4)$$

For the example used above, the energy that can be replenished using the scheme is 35.1 nJ, which is 28.4% of the total energy stored in the electrode, assuming $V_{DD} = 1$ V.

C. Current Controller

Redirecting currents between voltage supplies and electrodes is carried out by the current controller shown in Fig. 7. During the energy provision phase shown in Fig. 7(a), current source $I_{STIM}[4:0]$ is multiplied to I_{STM_L} through a current mirror formed by $MN1$ and $MN2$. I_{STM_L} flows from the electrode to the ramping-down supply voltage V_{SS_STM}. At the same time, an identical current flows from V_{DD_STM} to the other electrode through $MP1$. The gate of $MP1$ is controlled by an amplifier, which makes sure V_{STM_CM} the common mode voltage of the electrodes to be equal to a reference voltage that is 0.4 V ($\frac{1}{2}V_{DD}$).

During the second phase for energy replenishment, the same current mirror ($MN1$ and $MN2$) used for the previous phase is re-utilized, but now with different power supplies as shown in Fig. 7(b). The source of $MN1$ is switched to the electrode voltage V_{STM_L}, while the the source and the drain of $MN2$ are swapped in this phase. The lower terminal of $MN2$ serves as the drain during this phase connecting to V_{SS}, while the upper terminal is connected to V_{STM_L} as the source. Here, the source terminals of both $MN1$ and $MN2$ are connected to the common voltage, V_{STM_L}, working as a current mirror. In this manner, current I_{STM_L} flows from V_{SS} to the electrode. Note that $MN2$ has a floating bulk, facilitated by the employed SOI technology.

At the same time during the second phase, an identical current is generated, in this case flowing from the electrode (V_{STM_U}) to V_{DD}. In order to make sure a faster transition and lower peak current during the transition, another pMOSFET $MP2$ and another amplifier are used. Similar to the previous phase, the amplifier maintains the common mode by controlling the current I_{STM_U} to be identical to I_{STM_L}.

A resistor and capacitor are inserted across $MP1$ and $MP2$ for better stability at every phase transition between the energy provision and replenishment. They stabilize the feedback loop formed by the amplifier, $MP1$ and the capacitor between the

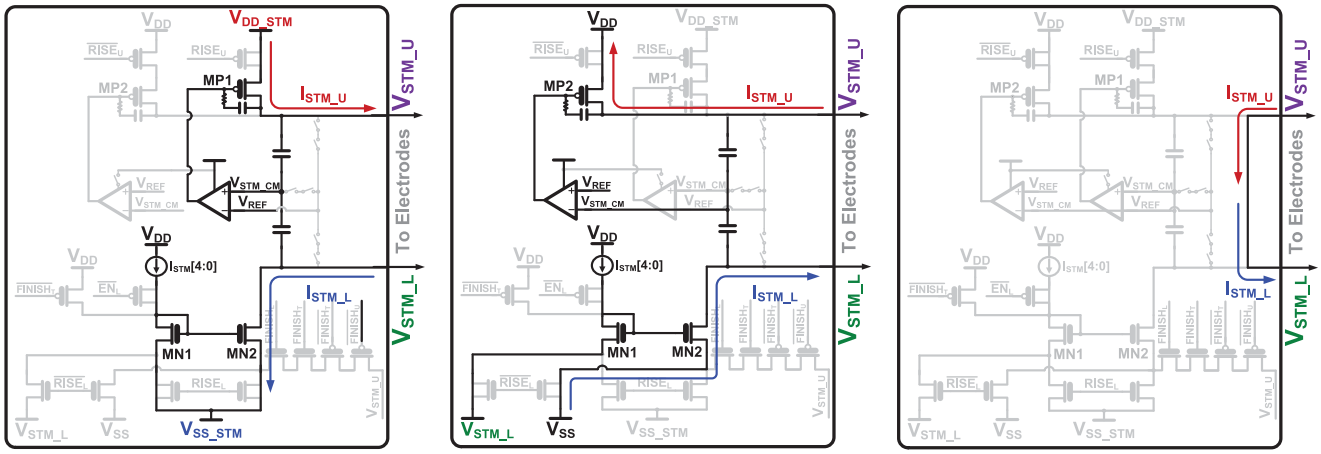


Fig. 7. Circuit diagrams of the current controller for (a) the energy provision phase, (b) energy replenishment phase, and (c) final phase.

drain of $MP1$ and the input of the amplifier. The parameter values for the resistor and capacitor are 27.6 kΩ and 1 pF, respectively.

In summary, the accumulated charge at the electrodes are redirected to the system power supplies (V_{DD} and V_{SS}) during the second phase when the electrode voltage are above and below these supplies, respectively. The analog control circuits maintains the stimulation currents to be constant and identical each other while the common-mode voltage remains constant during stimulation.

The first and second phases can be alternated as many times as necessary. In tri-phasic stimulation as depicted in Fig. 5, another first phase follows the second phase. At the end any residual charge on the electrodes is then canceled out by shorting as shown in Fig. 7(c).

Due to varying adiabatic supply voltages, digital control signals such as $RISE$, EN, and $FINISH$, shown in Fig. 7, must vary their reference potentials when describing logic 0 and 1 states to be correctly understood and to prevent leakage and gate breakdown. There are three classes of digital signals that must be generated: signals with subscripts T, U, or L. They must be valid within the landscape of possible voltage rails as depicted in Fig. 8(a). Signals with subscript T are in the typical voltage range between V_{DD} and V_{SS}, as shown in Fig. 8(b), and do not require special consideration. As shown in Fig. 8(c), the logic 1 level for signals with subscript U must be adapted to be the higher level between V_{DD_STM} and $2V_{DD}$, which is around 1.6 V in the proposed prototype. The logic 0 level is $2V_{SS}$, which is about −0.8 V, when V_{STM_U} is below 1.2 V, and is switched to V_{SS} when V_{STM_U} increases over 1.2 V. Similarly, the logic levels for signals with subscript L are generated as shown in Fig. 8(d).

D. Adiabatic Supply Voltage Generator

The adiabatic supply voltage generator is shown in Fig. 9, and is powered by the on-chip LC tank resonating at 190 MHz. The generator produces stimulation power supplies, V_{DD_STM} and

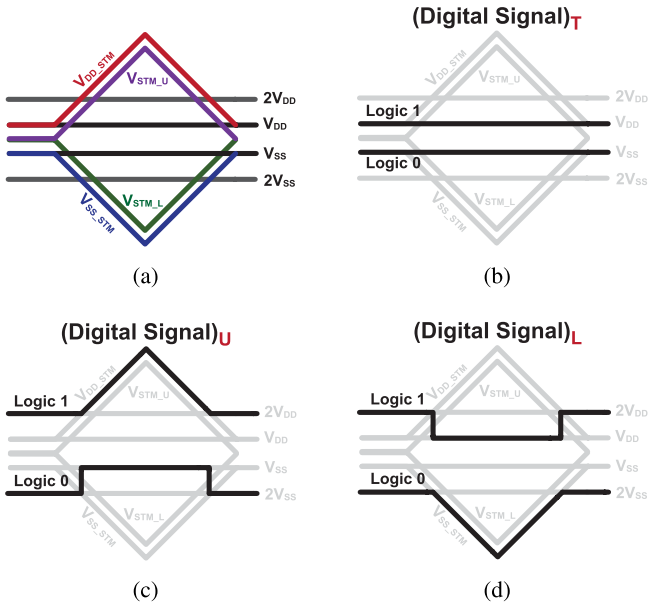


Fig. 8. (a) Power supply voltages during stimulation. Voltage levels of digital control signals with subscript of (b) T, (c) U and (d) L in Fig. 7.

V_{SS_STM}, according to the activity occurring with stimulation electrodes V_{STM_U} and V_{STM_L}. Ramping adiabatic supplies, V_{DD_STM} and V_{SS_STM}, are generated by a reconfigurable stack of modified differential Dickson charge pumps starting from from V_{DD} and V_{SS}, respectively. The circuits to generate V_{DD_STM} and V_{SS_STM} are symmetric.

The unit cell for the V_{DD_STM} part is shown in Fig. 10(a). It includes a pair of cross-coupled nMOSFETs $MN1$ and $MN2$ and a pair of diode-connected pMOSFETs $MP1$ and $MP2$, forming a rectifier. The electrode voltage V_{STM_U} controls a pair of nMOSFETs $MN3$ and $MN4$ on the inner bottom side and two pMOSFETs $MP3$ and $MP4$ on the outer sides.

Three different operation phases can be distinguished for the unit cell according to V_{STM_U} as shown in Fig. 10(b–d). When V_{STM_U} is lower than the internal V_{DD}s by more than

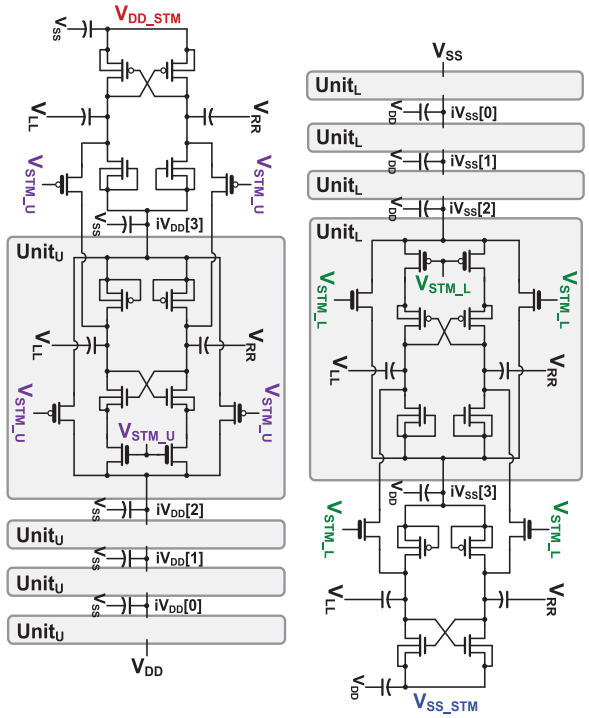


Fig. 9. Adiabatic supply generator.

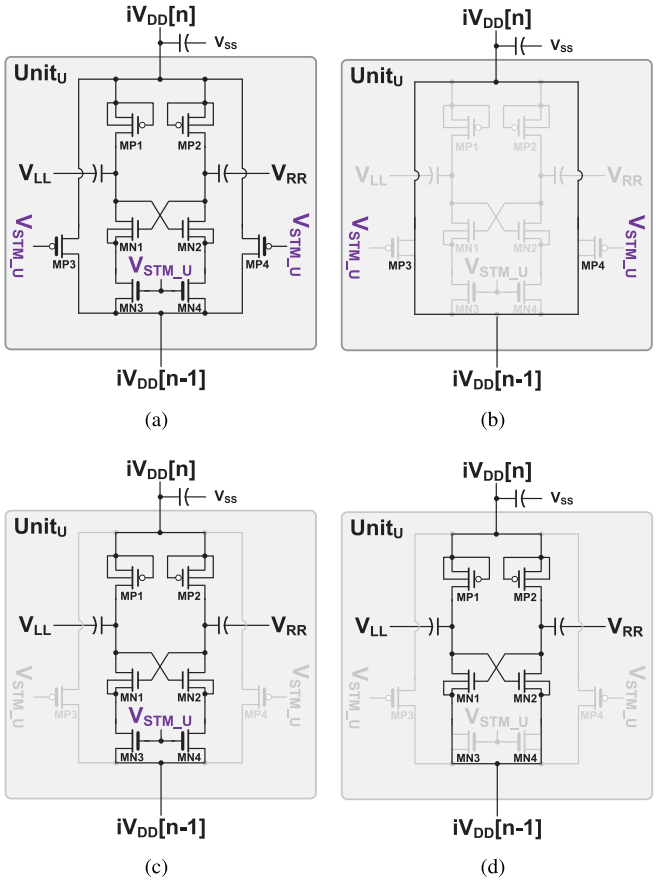


Fig. 10. (a) Circuit diagram of the unit cell of the adiabatic supply voltage generator. (b–d) Three operational phases of the unit cell.

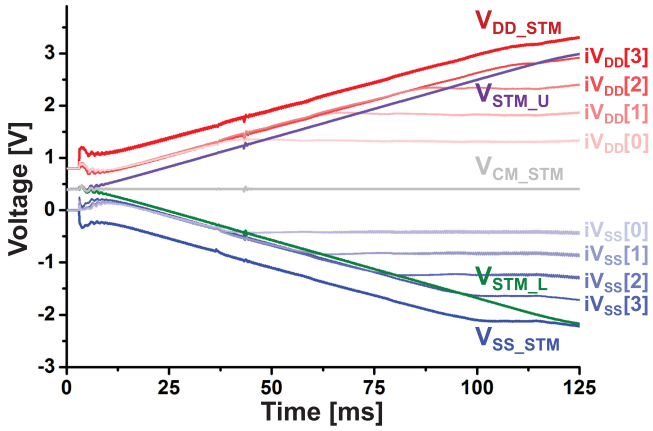


Fig. 11. Simulation results of the adiabatic supply voltage generator.

the threshold voltage of $MP3$ and $MP4$, $MP3$ and $MP4$ form short paths between the upper and lower internal V_{DD}s as shown in Fig. 10(b). When V_{STM_U} is in a similar range of the internal V_{DD}s, the outer paths are blocked and the inner part is activated as shown in Fig. 10(c). The on-resistances of $MN3$ and $MN4$ are controlled by V_{STM_U} generating a corresponding supply voltage between the upper and lower V_{DD}s. Finally, when V_{STM_U} is higher than the internal V_{DD}, this unit becomes a standard Dickson unit as shown in Fig. 10(d).

Simulated waveforms for the adiabatic supply voltage generator are shown in Fig. 11. As shown, V_{DD_STM} and V_{SS_STM} follow the electrode voltages V_{STM_U} and V_{STM_L} with a small voltage gap. All the while, the common-mode voltage V_{CM_STM} is kept constant. Initially, all the internal stages in the stack are folded near the common-mode voltage. As the electrode voltages V_{STM_U} and V_{STM_L} expand, the first stages become unfolded first and produce $iV_{DD}[0]$ and $iV_{SS}[0]$. After that, the next ones get unfolded one by one until all are unfolded. By doing so, V_{DD_STM} and V_{SS_STM} are generated.

Since the power supplies (V_{DD_STM}, V_{SS_STM}) of the stimulator are directly generated from the LC resonant tank, the overall performance of the circuit, including the maximum stimulation current and highest possible power supply rails is directly related to the LC tank's quality factor and total processed energy. More detailed strategies to achieve a high quality factor and power transfer efficiency in millimeter-sized implants are described in [52], [53]. Since the stimulator can draw a large instantaneous current from the LC tank, a large amount of power decoupling capacitors were placed both globally and locally near sensitive blocks. A rectifier design that can tolerate rapid variations in the input RF voltage can also help alleviate this issue.

IV. Experimental Validation

A prototype of ENIAC, including the proposed stimulator, was fabricated in a 0.18-μm CMOS silicon-on-insulator (SOI) process, and a die photo of the chip is shown in Fig. 12. The total chip dimensions are 3×3 mm^2, which includes a two-turn on-chip inductor along the perimeter of the chip, along

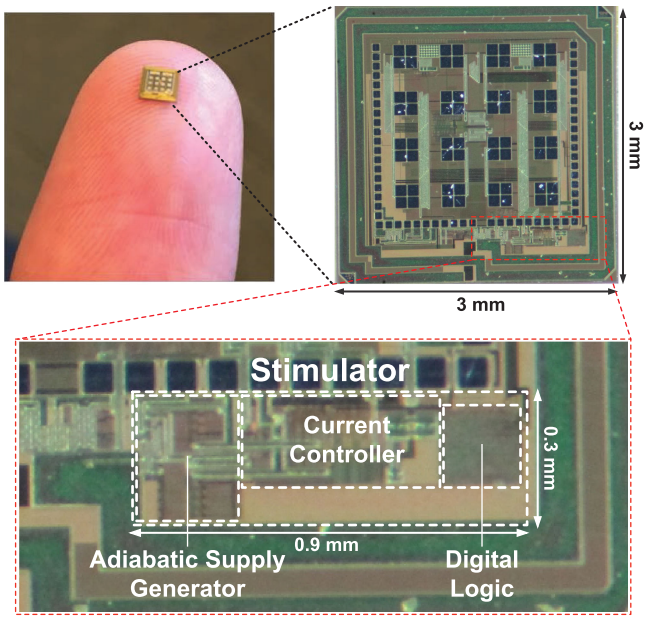


Fig. 12. Chip micrograph of the stimulator.

with 16 on-chip 250 × 250 μm^2 electrodes. The core area of the stimulator circuits occupy 0.22 mm^2. Simulated inductance and quality factor of the on-chip coil are 23.7 nH and 11.2, respectively.

For all measurement results presented in this section, a PCB-based transmitter was used to send out 190-MHz continuous RF field to power the chip wirelessly. The transmitter has a single turn coil with a passive matching network on a PCB. The coil has a radius of 25 mm, a width of 4 mm, and a quality factor of greater than 70 at the resonance frequency [39].

Fig. 13(a) shows measured 120-μA differential tri-phasic stimulation waveforms and the corresponding currents through RC-modeled electrodes, each composed of a 15 nF capacitor and a 900 Ω resistor in series. As shown in the figure, the two adiabatic supply voltages, V_{DD_STM} and V_{SS_STM}, closely follow the two electrode voltages, V_{STM_U} and V_{STM_L}, respectively, while maintaining a small voltage gap. V_{DD_STM} and V_{SS_STM} can reach up to −3.3 V and +3.9 V, respectively. Because the current controller described in Section III-C. makes sure that the two differential currents (I_{STM_U} and I_{STM_L}) are identical, the differential electrode voltages (V_{STM_U} and V_{STM_L}) should be symmetrical. However, the adiabatic supply voltages are generated by two distinct units within the adiabatic supply voltage generator (described in Section III-D.), and thus they may be less symmetrical than (V_{STM_U} and V_{STM_L}) as shown in Fig. 13(a). Due to this asymmetry, the current source on the V_{SS_STM} side appears to be in the triode region between 1.4 and 1.6 ms, so that the corresponding stimulation current was decreased slightly. A slightly larger RF field delivered to the coil, or a more symmetric design would help to eliminate this issue. As shown on the bottom side of Fig. 13(a), the stimulation current waveforms show several peaks, which are generated when the stimulator makes phase changes between the current provision and the energy replenishment phases.

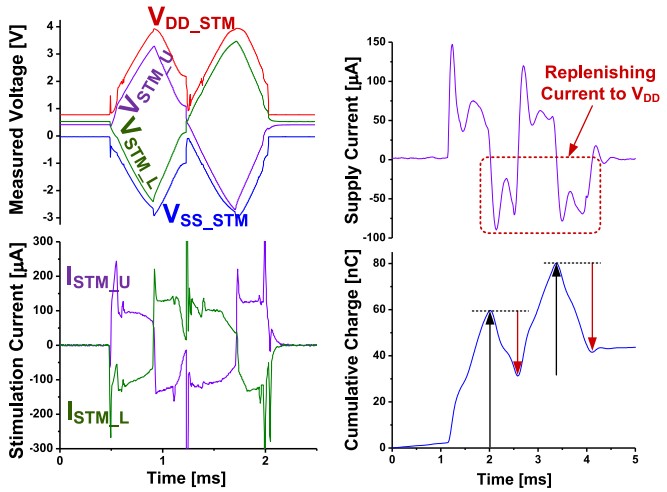


Fig. 13. (a) (Top) Measured voltage waveforms: adiabatic supply voltages V_{DD_STM} and V_{SS_STM} and electrode voltages V_{STM_U} and V_{STM_L}. (Bottom) The corresponding differential currents. (b) (Top) The current supplied from stimulator V_{DD}. The negative current indicates a replenished current back to the stimulator supply. (Bottom) Accumulated charge of the supply current. The positive ramps denoted with black arrows indicate the charge provided from the supply, and the negative ramps denoted with red arrows indicates the replenished charge.

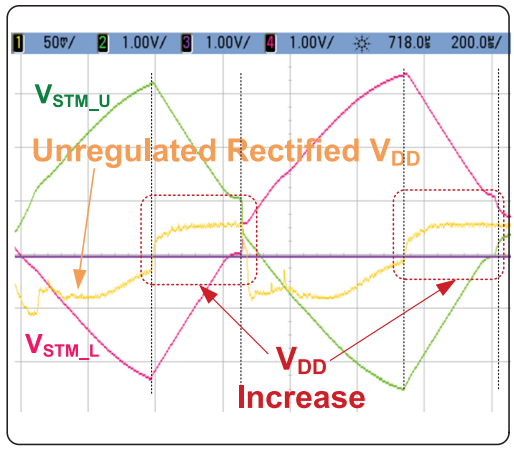
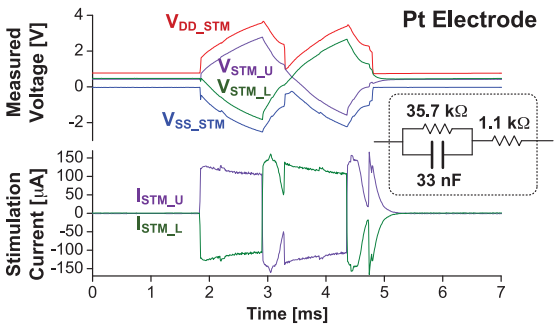


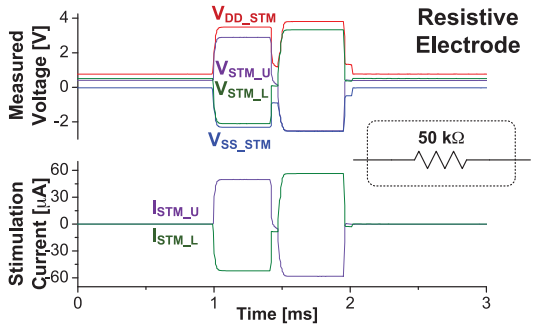
Fig. 14. A capture of measurement showing V_{DD} increase during the energy replenishing phase. V_{DD} was measured in AC-coupled mode.

The measured supply current from the stimulator is shown in Fig. 13(b). Here, negative current indicates energy is being replenished back to V_{DD}. As the computed cumulative charge (Fig. 13(b) (Bottom)) shows, more than 63% of charge is returned. As shown in Fig. 14, the rectified V_{DD} increases during the energy-replenishing phase, further validating the energy replenishment concept.

The stimulator was further validated across several representative electrode models. As shown in Fig. 15(a), bio-realistic in vitro mock electrode interface model based on measured electrode characterization [54] were used for proof-of-concept evaluation. The electrode interface model including components for bilayer capacitance, faradaic current, and solution resistance provides for ground truth in the characterization of electrical

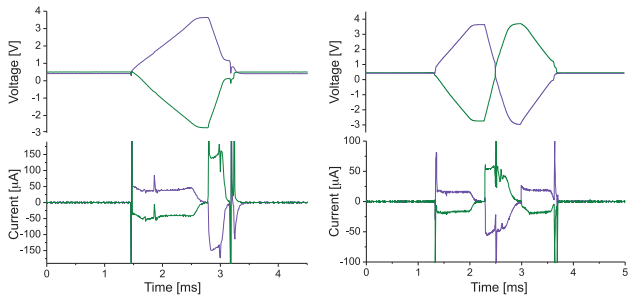


(a)



(b)

Fig. 15. Measurements with different electrode models. (a) Pt electrode [54] and (b) purely resistive electrode.



(a) (b)

Fig. 16. Measurement results with (a) bi-phasic and (b) tri-phasic waveforms.

parameters relevant to the biomedical circuits. The component values are based on an area of 250 × 250 μm^2. In addition, a purely resistive electrode of 50 kΩ was used for further validation as shown in Fig. 15(b). As shown in the figures, the stimulator works well not only with capacitive electrodes, but also with other types of electrodes.

In addition, this stimulator supports both tri-phasic and bi-phasic pulse stimulation as shown in Fig. 16. Also, it offers individual programmability on each phase's duration and current, and the gap time between the phases.

V. Benchmarking Stimulators

It is challenging to compare different stimulator designs because of different conditions on the operating environments such as electrode size, stimulation current, voltage rails, etc. To help more easily benchmark various stimulation approaches, a new figure of merit (FOM) that quantifies the energy efficiency of stimulation is proposed: the Stimulator Efficiency Factor (SEF). This FOM compares the net energy usage of a stimulator compared to one that uses an ideal current source attached to a supply voltage set to the maximum achievable voltage compliance. The net energy usage can be represented as:

$$E_{STIM} = \text{(Provided + Wasted – Replenished) Energy}, \quad (5)$$

where the provided energy is the energy that is delivered to the electrode and the tissue, the wasted energy is the energy that is dissipated in the stimulator such as across the current source, and the replenished energy is the energy that is delivered back to the supply from the energy accumulated in the electrode. Then, *SEF* can be expressed as:

$$SEF = \frac{E_{STIM}\,(\text{Ideal Current Source w/ fixed DC rail})}{E_{STIM}\,(\text{Stimulator under test})} \quad (6)$$

where E_{STIM} (Ideal Current Source w/ fixed DC rail) is the net energy usage of a stimulator using a ideal current source and a fixed supply voltage, and E_{STIM} (Stimulator under test) is of the stimulator under test. Thus, *SEF* represents how much more efficient the stimulator is compared to an ideal current source with fixed DC voltage rails.

Fig. 17 illustrates how SEF can be calculated for a stimulator. Here, the presented stimulator is chosen as an example. On the left side in Fig. 17, the stimulator's power supplies (V_{DD_STM} and V_{SS_STM}) and electrode voltage (V_{STM_U}) are drawn over a time period of one stimulation event. The shaded area represents the amount of provided (purple), wasted (gray), and replenished (orange) energies, respectively. In order to calculate SEF for this stimulator, a reference stimulator that uses ideal current sources tied to fixed voltages and injects the same amount of current to the same electrode as the stimulator under comparison (i.e., the stimulator that we would like to determine SEF for) must be analyzed. Thus, the electrode voltage of the ideal-current-source stimulator is exactly same as the electrode voltage (V_{STM_U}) of the stimulator under comparison. In addition, the positive supply of the ideal-current-source stimulator (V_{DD_High}) is set as the maximum of the electrode voltage and the negative supply (V_{SS_Low}) as the minimum. Based on these, the net energy usage of the reference ideal-current-source stimulator is calculated, and used for calculating SEF of the stimulator under comparison. By definition, the baseline of an ideal constant current source with DC voltage rails has an SEF of 1. Stimulators with real, non-ideal current sources will obtain an SEF less than 1.

As shown on the right side in Fig. 17, the presented stimulator offers further improvement both by the adapting adiabatic rails and by replenishing energy. In order to calculate SEF of the stimulator, the net energy usage was found for the following condition: 120 μA tri-phasic pulse, 1.5 ms duration, and electrodes with 15 nF and 900 Ω in series. The total provided energy was 144 nJ, the wasted energy 18.1 nJ and the replenished energy 27.9 nJ. Resulting E_{STIM} and SEF were 162 nJ and 4.99 without replenishment, respectively. With energy replenishment, E_{STIM} and SEF became 134 nJ and 6.02, respectively. From Eqs. (3,4), the theoretical maximum of the replenished energy E_R is 60.2 nJ. For an ideal case without

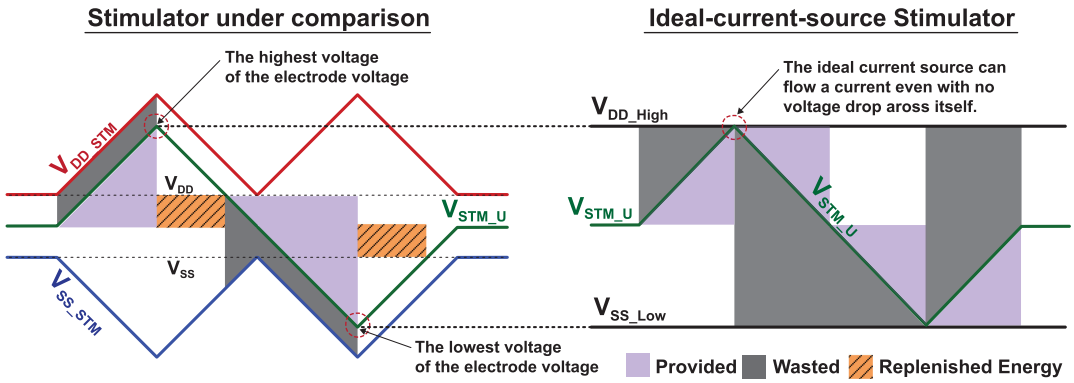


Fig. 17. Energy delivery, loss and replenishment for the presented adiabatic stimulator and a corresponding stimulator using ideal current sources from constant supply voltages for SEF calculation. V_{DD_High} the positive supply of the ideal-current-source stimulator, is set to the same voltage as the maximum of the electrode voltage. Likewise, V_{SS_Low} the negative supply is set to the same as the minimum of the electrode voltage.

TABLE I
COMPARISON OF STATE-OF-THE-ART ADIABATIC STIMULATORS

	[28]	[35]	[51]	[50]	This Work
Technology [μm]	1.5	0.35	0.18	0.065	0.18 SOI
IC Area [mm^2]	4.76[1]	<0.58[2]	0.11[2]	0.45[3]	0.22[2]
External Components	LC tank Capacitors, Electrodes	Inductor Electrodes	LC tank Electrodes	Electrode	None
Source of Stimulation Power	125 kHz External LC	V_{DD}	5 MHz External LC	V_{DD}	190 MHz On-Chip LC
Supply Voltage [V]	$\pm$1.75	3.3	N/A	1	0.8
Stimulation Supply Voltage Range [V]	$\pm$1.75 (1$\times V_{DD}$)	3.3 (1$\times V_{DD}$)	N/A	0 $\sim$ 8.7 (8.7$\times V_{DD}$)	-3.3 $\sim$ +3.9 (9$\times V_{DD}$)
Maximum Stimulation Current [μA]	400	450	140	>500	145
Charge Replenishing Ratio	N/A	N/A	N/A	N/A	63.1%
Stimulator Efficiency Factor	2.13 $\sim$ 2.94[4]	3.5[4]	1.33 $\sim$ 5[4]	N/A	4.99 (w/o replenishment) 6.02[5] (w/ replenishment)
Electrode Model	980nF+1.15kΩ	930nF+1kΩ	5.5nF//6kΩ+4kΩ	10nF+1kΩ	4nF+250Ω, 15nF+900Ω 50kΩ, 33nF//36kΩ+1.1kΩ

[1] Die area. [2] Active area. [3] Active area of the 1:7 DC-DC converter and one channel neural stimulator. [4] Estimated based on the reported numbers and figures. [5] Estimated.

any energy dissipation or voltage drop, E_{STIM} can be low as 83.8 nJ resulting in SEF of 9.65.

Table I shows a comparison of state-of-the-art adiabatic stimulators. In comparing this work with other adiabatic stimulators, note that this stimulator is directly powered by a 190 MHz resonant LC tank while other works are powered at frequencies below 10 MHz or from a DC power source. For wireless implantable applications, DC power requires rectification and regulation and additional steps of power conditioning to generate adiabatic power rails, each causing extra energy losses, which are not accounted for in the table. On the contrary, the proposed stimulator produces adiabatic power rails directly from the RF input, over a range that is 9 times larger than V_{DD}. While some other adiabatic stimulators require large external capacitors and inductors, the proposed design requires no external components. This chip achieves more than 60% of charge replenishing ratio, and a SEF of 6.02.

VI. CONCLUSIONS

This paper has presented and demonstrated an adiabatic stimulator that is fully integrated in a mm-sized stand-alone chip designed for neural interfacing applications. The proposed stimulator has two distinct advantages. First, the adiabatic stimulation supplies are directly generated from RF while conventional approaches require cascade power conditioning circuits, large external passives, or both, leading to lower overall efficiency. Second, it replenishes energy from the charged electrodes, resulting in more energy-efficient operation. For benchmarking the stimulator performance, a stimulator efficiency factor (SEF) is proposed. This FOM compares the stimulator with an ideal stimulator operating with current sources from constant voltage rails set at the minimum and maximum of the required stimulation voltage compliance. The proposed adiabatic stimulator achieves a measured SEF of 5 excluding replenished energy, and SEF of 6 with estimated replenished energy.

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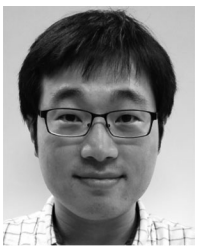
Sohmyung Ha (S'05–M'16) is Assistant Professor of Electrical Engineering at New York University Abu Dhabi, Abu Dhabi, UAE, and Global Network Assistant Professor of Electrical and Computer Engineering at New York University, Brooklyn, NY, USA. He received the B.S degree with *summa cum laude* and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2004 and 2006, respectively. From 2006 to 2010, he worked at Samsung Electronics as analog and mixed-signal circuit designer for commercial multimedia devices.

After this extended career in industry, he returned to academia as a Fulbright Scholar, and obtained the M.S. and Ph.D. degrees with the best Ph.D. thesis award for biomedical engineering from the Department of Bioengineering, University of California San Diego, La Jolla, CA, USA, in 2015 and 2016, respectively. Since 2016, he has been with New York University Abu Dhabi and New York University.

His research interests include integrated circuits and interfaces for implantable and wearable biosignal monitoring and actuation systems. He received the Fulbright Fellowship from 2010 to 2012.



Chul Kim (S'12–M'18) received the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2009, and the Ph.D. degree from the Bioengineering Department, University of California (UC) San Diego, La Jolla, CA, USA, in 2017.

From 2009 to 2012, he was with SK HYNIX, Icheon, South Korea, where he designed power management circuitry for dynamic random access memory. He is currently a Post-Doctoral Scholar with UC San Diego. His current research interests include ultralow-power integrated circuits and systems for fully wireless brain–machine interfaces and body-area networks.

Dr. Kim received the Gold prize in the 16th Human-Tech Thesis Prize Contest from Samsung Electronics, Suwon, South Korea, in 2010, and the 2017 to 2018 Shunichi Usami Ph.D. Thesis Design Award in the Bioengineering Department, UC San Diego. He was the recipient of the 2017 to 2018 IEEE Solid-State Circuits Society Predoctoral Achievement Award.

Jiwoong Park (S'15) received the B.Sc. degree (*summa cum laude*) in electronic and computer engineering from Hanyang University, Seoul, South Korea, in 2012, and the M.S. degree in electrical and computer engineering from the University of California San Diego, La Jolla, CA, USA, in 2014, where he is currently working toward the Ph.D. degree. His research interests include the design of ultralow power body area network systems and the design of miniaturized wireless power transfer systems for biomedical implants.

Gert Cauwenberghs (S'89–M'94–SM'04–F'11) is Professor of Bioengineering and Co-Director of the Institute for Neural Computation at UC San Diego, La Jolla CA. He received the Ph.D. degree in Electrical Engineering from California Institute of Technology, Pasadena in 1994, and was previously Professor of Electrical and Computer Engineering at Johns Hopkins University, Baltimore, MD, and Visiting Professor of Brain and Cognitive Science at Massachusetts Institute of Technology, Cambridge. He co-founded Cognionics Inc. and chairs its Scientific Advisory Board.

His research focuses on micropower biomedical instrumentation, neuromorphic silicon and brain-machine interfaces, neuromorphic engineering, and adaptive intelligent systems. He received the NSF Career Award in 1997, ONR Young Investigator Award in 1999, and Presidential Early Career Award for Scientists and Engineers in 2000. He was a Francqui Fellow of the Belgian American Educational Foundation, and is a Fellow of the American Institute for Medical and Biological Engineering. He served IEEE in a variety of roles including as Distinguished Lecturer of the IEEE CIRCUITS AND SYSTEMS SOCIETY, as General Chair of the IEEE Biomedical Circuits and Systems Conference (BioCAS 2011, San Diego), as Program Chair of the IEEE Engineering in Medicine and Biology Conference (EMBC 2012, San Diego), and as Editor-in-Chief of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS.

Patrick P. Mercier (S'04–M'12–SM'17) received the B.Sc. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada, in 2006, and the S.M. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2008 and 2012, respectively.

He is currently an Associate Professor in electrical and computer engineering with the University of California San Diego (UCSD), La Jolla, CA, USA, where he is also the Co-Director with the Center for Wearable Sensors. His research interest includes the design of energy-efficient microsystems, focusing on the design of RF circuits, power converters, and sensor interfaces for miniaturized systems and biomedical applications. He was the recipient of a Natural Sciences and Engineering Council of Canada (NSERC) Julie Payette fellowship in 2006, NSERC Postgraduate Scholarships in 2007 and 2009, an Intel Ph.D. Fellowship in 2009, the 2009 IEEE International Solid-State Circuits Conference (ISSCC) Jack Kilby Award for Outstanding Student Paper at ISSCC 2010, a Graduate Teaching Award in Electrical and Computer Engineering at UCSD in 2013, the Hellman Fellowship Award in 2014, the Beckman Young Investigator Award in 2015, the DARPA Young Faculty Award in 2015, the UCSD Academic Senate Distinguished Teaching Award in 2016, the Biocom Catalyst Award in 2017, and the NSF CAREER Award in 2018. Since 2013, he has been an Associated Editor for the IEEE TRANSACTIONS ON BIOMEDICAL INTEGRATED CIRCUITS. From 2015–2017, he was an Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION. He is currently a member of the ISSCC International Technical Program Committee (Technology Directions Subcommittee), the CICC Technical Program Committee, and the VLSI Symposium Technical Program Committee and is an Associate Editor for the IEEE SOLID-STATE CIRCUITS LETTERS. He was the Co-Editor of *Ultra-Low-Power Short Range Radios* (Springer, 2015) and *Power Management Integrated Circuits* (CRC Press, 2016).