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Broadband CMOS Power Amplifiers and Efficient Printed Circuit Antennas for D-Band Wireless Systems

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering

by

Md Hedayatullah Maktoomi

Dissertation Committee:
Associate Professor Hamidreza Aghasi, Chair
Professor Payam Heydari
Professor Ozdal Boyraz

2026

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DEDICATION

To my family.

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ABSTRACT OF THE DISSERTATION

Broadband CMOS Power Amplifiers and Efficient Printed Circuit Antennas for D-Band Wireless Systems

By

Md Hedayatullah Maktoomi

Doctor of Philosophy in Electrical Engineering

University of California, Irvine, 2026

Associate Professor Hamidreza Aghasi, Chair

The D-band (110–170 GHz) offers contiguous bandwidth that makes backhaul links exceeding 100 Gb/s attainable and enables sub-millimeter-resolution imaging and centimeter-resolution radar. Complementary metal-oxide-semiconductor (CMOS) technology is an attractive platform for these transmitters because it enables monolithic integration of the analog front end, digital baseband, and control circuitry on a low-cost die.

The first part of this dissertation introduces the design challenges of broadband D-band transmitters. At D-band frequencies, CMOS transistors operate near half of their maximum oscillation frequency, where available gain degrades rapidly, while their low breakdown voltage limits the saturated output power of a single-stage amplifier. Meanwhile, the antenna must maintain impedance matching over a wide bandwidth. Consequently, the communication range depends on both power amplifier (PA) output power and antenna gain.

The second part of this dissertation presents a three-stage broadband D-band PA fabricated in 65-nm bulk CMOS. A device-centric power model for cascode PA stages, incorporating mobility-induced transconductance compression, shows that maximum output power is achieved when the common-gate device is larger than the common-source device. Based on this observation, an enhanced power current-reuse cascode (EPCRC) stage is proposed,

where a third transistor reuses the excess current from the device size mismatch while improving power gain. To overcome the bandwidth limitation of conventional combiners with large impedance transformation ratios, a four-way slotline-based dual-coupled differential power combiner (DCDPC) is proposed. The PA achieves 19-dBm peak saturated output power, 15.3-dB peak gain, 5.3% power-added efficiency (PAE), and a 32.8-GHz 3-dB bandwidth from 110–142 GHz within 0.99×0.48 mm^2, with an error vector magnitude (EVM) of -21 dB or better up to 1024-quadrature amplitude modulation (1024-QAM).

In the third part of this dissertation, two wideband antennas on a flexible printed circuit (FPC) are presented for the WR-08 band (90–140 GHz). Conventional aperture-coupled stacked-patch (ACSP) designs fail to reach a large bandwidth here, and feedline-induced surface waves reduce the radiation efficiency at several resonances. A two-section wideband distributed network (TWBDN) therefore matches the input port to the slot aperture, a TWBDN matched stacked patch (TMSP) network based on constant voltage standing wave ratio (VSWR) circles extends it to the patches. A methodology to suppress the surface waves around the feedline through via arrays is studied, and a low-loss ground-signal-ground (GSG) transition facilitates measurement. The fabricated antenna measures a 7.95-dBi peak gain and S_{11} at or below -10 dB from 90 to 128.5 GHz. The surface waves launched by the radiating patches themselves, however, remain and limit the gain. A cavity-backed ACSP (CB-ACSP) is therefore proposed, in which one via-wall cavity confines these waves and a second cavity intercepts the leakage admitted by the FPC minimum via spacing. The measured CB-ACSP covers 91.5–134 GHz below -10 dB, a 37.7% fractional bandwidth—the highest reported among off-chip antennas above 100 GHz—with a peak gain of 8.1 dBi.

These results together establish heterogeneous integration of CMOS circuits with flexible antennas as a low-cost path to broadband high-power D-band transmitters.

Chapter 1

Introduction to D-Band CMOS Transmitter Design Challenges

1.1 The D-Band and Its Applications

Advances in transistor technology, manifested in increasingly high operating frequencies, have enabled the development of millimeter-wave and terahertz integrated circuits using standard CMOS and BiCMOS processes [1–10]. Higher data rates in wireless communication, and finer resolution in radar and imaging, both translate into a demand for bandwidth [11–24]. The D-band, spanning 110–170 GHz, is the most practically accessible of the sub-terahertz bands, and is pursued across the three application communities of Fig. 1.1. Point-to-point backhaul has reached multi-gigabit rates [25]. Imaging and sensing exploit the 2.1-mm wavelength at 140 GHz, half that at 77 GHz, halving the diffraction-limited spot size from a given aperture; integrated D-band imagers in 65-nm CMOS [26] and single-chip imaging radars resolving 7 mm in range [27] have both been demonstrated. In automotive sensing, advanced driver assistance system (ADAS) radars operate at 60 GHz and 76–81 GHz for functions such as adaptive cruise control and collision avoidance [28–32]; 140-GHz radar

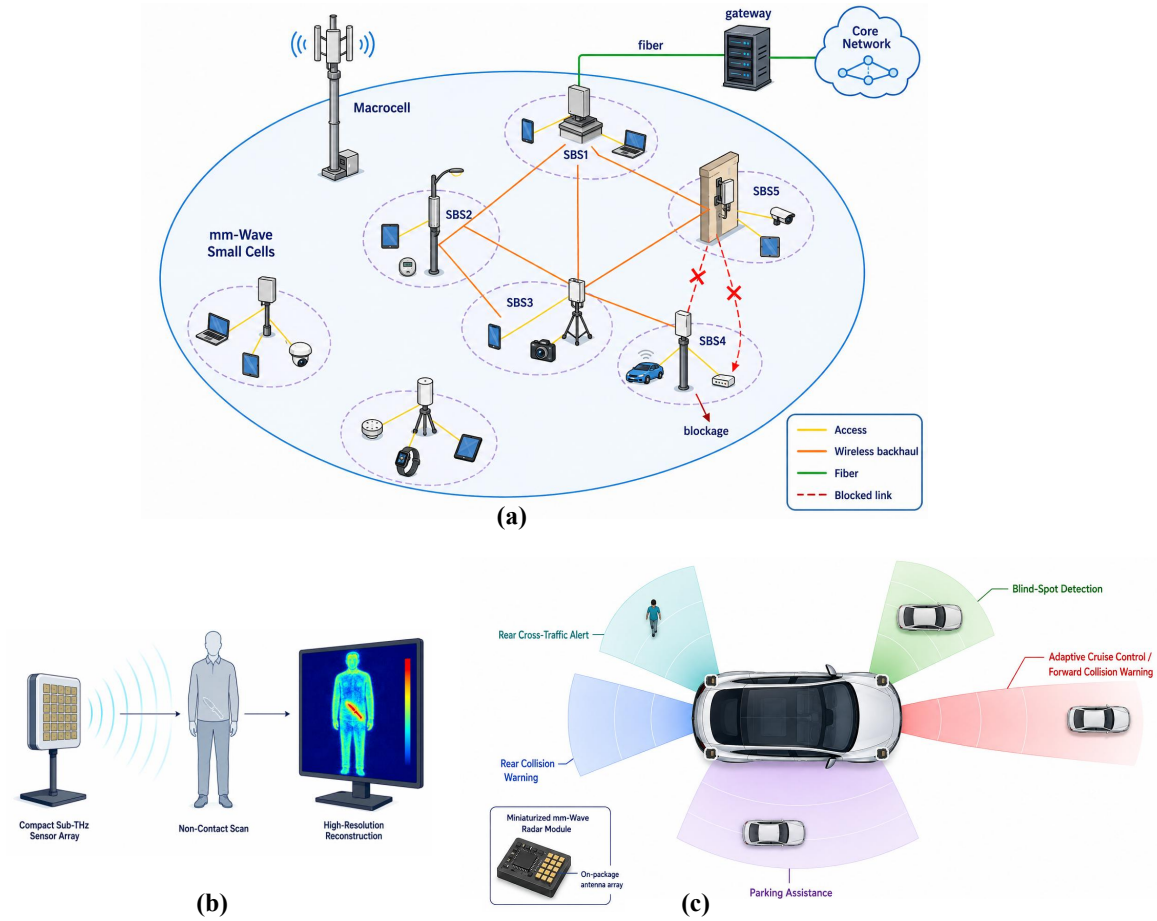

Figure 1.1: D-band applications: (a) point-to-point wireless backhaul, (b) sub-terahertz imaging and contactless sensing, and (c) high-resolution automotive radar.

is being evaluated as a complement, since range resolution follows the swept bandwidth, $\Delta R = c/2B$ so the 10-GHz sweep demonstrated at 140 GHz [33] yields 1.5 cm, against 3.75 cm for the 4 GHz available at 77 GHz.

1.2 Technology Choice and the Power Amplifier

Although III–V technologies offer superior transistor performance at D-band, complementary metal-oxide-semiconductor (CMOS) technology enables highly integrated, cost-effective transceivers, making it well suited to large phased-array systems. High free-space path loss demands both transmit power and antenna gain, combined as the effective isotropic radiated

power (EIRP),

$$\mathrm{EIRP} = P_{\mathrm{sat}} + G_{\mathrm{ant}} - L_{\mathrm{int}}, \tag{1.1}$$

where P_{sat} is the saturated output power of the power amplifier (PA), G_{ant} the antenna gain, and L_{int} the chip-to-antenna interface loss. A 6G base station above 100 GHz, for example, is projected to need close to 75 dBm EIRP from some 256 elements [34]. Because the per-element output power of state-of-the-art D-band CMOS PAs remains limited, high-gain antennas are essential to achieve the required EIRP.

1.3 Device Gain Near $f_{\max}$

The dominant difficulty in D-band CMOS design is limited device gain. The key figures of merit are

$$f_T \approx \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}, \qquad f_{\max} \approx \frac{f_T}{2\sqrt{R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}}, \tag{1.2}$$

where f_T and $f_{\max}$ are the unity-current-gain and unity-power-gain frequencies. The quantity of interest is the maximum available gain,

$$G_{\max} = \left|\frac{S_{21}}{S_{12}}\right| \left(k - \sqrt{k^2 - 1}\right), \tag{1.3}$$

defined for an unconditionally stable device with Rollett factor $k > 1$; for $k < 1$ the bound is the maximum stable gain $|S_{21}/S_{12}|$. Gain rolls off at roughly 20 dB/decade toward $f_{\max}$, and a widely used rule holds that $f_{\max}$ should exceed f_0 by two to three times. In 65-nm bulk CMOS, where $f_{\max} \approx 280$ GHz [35, 36], a 140-GHz amplifier sits at $f_{\max}/2$ with no margin. Both R_g and C_{gd} enter (1.2) directly and are inflated by the interconnect needed to contact the device, so the penalty worsens with the large peripheries a power stage requires. This makes the gain boosting at the device and stage level a prerequisite rather than an optimization.

1.4 On-Chip Power Combining

A single stage cannot deliver the required power: the low supply voltage of a scaled CMOS process drives the optimum drain load down to a few ohms, and transforming that up to a 50 Ω termination is itself lossy. Several cells must therefore be combined. Three on-chip topologies dominate, direct, or corporate, combining through a binary tree of Wilkinson or zero-degree junctions, and transformer combining in either parallel or series form, the latter two more compact because they absorb the matching network. All face the same three difficulties at D-band. Loss grows with the number of ways through longer routing and larger area; the impedance transformation ratio rises with it, narrowing bandwidth; and the branches must stay balanced, since any amplitude or phase mismatch reflects power at the combining node instead of delivering it to the load. Transformer structures are the most exposed to the last of these, because interwinding capacitance couples common-mode signal to the output: reported series combiners show input-impedance spread up to 40% and combining loss above 2 dB at millimeter-wave [37]. Loss, bandwidth and balance must therefore be co-designed rather than optimized in sequence.

1.5 The Antenna and Its Interface

The G_{ant} that must supply the balance of (1.1) is not available on-chip: a lossy, high-permittivity silicon substrate and a patch-to-ground separation of only 12–15 μm hold reported gains between -2 and 2 dBi while still consuming die area [38]. A printed circuit board (PCB) radiator inverts this, substrate thickness becoming a free design parameter: 7.95 dBi across 90–128.5 GHz above 75% efficiency [39].

The standing objection is L_{int}: the interface is lossy and sensitive to interconnect length, a 500-μm wirebond behaving as a quarter-wave line at 150 GHz. It is a design problem rather than a barrier — co-designing the bond with matching on both chip and board sides holds

interface loss below 1.5 dB across a 49–63-GHz radar front-end [29], and the approach has been carried to 146.7 GHz with a series-fed patch array [40], the bond inductance becoming an element of the matching network rather than a loss.

Chapter 2

A 19-dBm 110–142-GHz CMOS Power Amplifier With Device-Centric Power Boosting and Dual-Coupled Slotline Combiner

2.1 Introduction

The growing demand for higher data rates in next-generation wireless systems necessitates circuits with high bandwidth capabilities. The D-band (110–170 GHz) has emerged as a strong candidate, but limited device gain and high interconnect losses demand high-output-power transmitters, especially power amplifiers (PAs). While III-V-based PAs offer high $f_{\max}$ and superior performance, their cost and yield restrict scalability. In contrast, cost-effective silicon (Si) technologies like 65-nm CMOS enable integration with digital/analog circuits. To overcome CMOS limitations such as lower breakdown voltage and reduced speed, various gain-boosting techniques have been explored for >100 GHz PAs [41–45].

The capacitive-neutralized common-source (CS) stage improves gain by canceling C_{gd} and is widely used in PA designs, though its output power is limited by supply voltage. The cascode configuration offers higher reverse isolation and supports larger supply voltages due to its higher breakdown voltage, enabling greater output power [46]. Increasing transistor size in the cascode can further boost power but also increases parasitics and lowers output impedance, degrading gain and raising the impedance transformation ratio (ITR), which limits bandwidth [47]. Alternatively, stacking multiple transistors—as in [48], where five devices achieved 18.7 dBm at 200 GHz—can enhance output power, though at the cost of more intermediate-node parasitics that reduce both gain and bandwidth.

The output power of a single PA stage can be increased using power combiners (PCs), which combine outputs from multiple parallel stages. However, increasing the number of paths raises the ITR, limiting bandwidth. PCs are typically categorized as zero-order [49–55], Wilkinson-based [56–58], and transformer-based [59–65]. Zero-order PCs are structurally simple but suffer from rising ITR with added paths. Wilkinson PCs provide good input isolation but require large $\lambda/4$ lines, hindering scalability. Transformer-based designs offer wide bandwidth but face challenges like low-Q inductors, increased inter-winding capacitance, port imbalance, and poor common-mode rejection [37]. Slotline-based power combiners have recently gained attention for their improved bandwidth and excellent common-mode suppression [37, 66, 67]. A 2×1 single-ended (SE) combiner was demonstrated in [66], followed by a scalable 4×1 version in [37]. More recently, a 4×1 differential (8×1 SE) combiner was proposed in [67], achieving over 26.5 GHz bandwidth at 171 GHz with a peak P_{sat} of 13.9 dBm. To mitigate asymmetry, additional transmission line sections and stubs were used to balance port impedances, though insertion loss imbalance was not studied.

Rising data rate demands in next-generation wireless links call for spectrally efficient modulation beyond 64-quadrature amplitude modulation (QAM). Higher-order QAM poses key challenges for the power amplifier (PA): a high peak to average power ratio (PAPR), (typ-

ically $> 8\,\mathrm{dB}$) which requires significant back-off, necessitating a higher P_{sat} to maintain adequate average power, P_{avg}. As P_{avg} drops and noise increases with bandwidth ($kTBW$), boosting P_{avg} becomes essential to sustain throughput and achieve strict EVM.

To address the challenges of achieving higher output power, improved gain, and larger bandwidth for the D-band power amplifiers (PAs), this work introduces several key solutions built upon a new device-level nonlinear output power model that captures frequency-dependent transconductance compression due to mobility degradation [68]: (i) a current-reuse three-transistor cascode PA architecture with enhanced P_{sat} based on a device-centric output power maximization technique. The current difference between the common-gate (CG) and common-source (CS) transistors in the proposed PA is reused by a third transistor that further improves the gain, and (ii) a broadband slotline-based 4-way dual-coupled differential power combiner (DCDPC) with dual-layer stacked coupling yielding a small amplitude imbalance and high common-mode suppression to further enhance the output power across a large bandwidth. To demonstrate the effectiveness of the proposed solutions, the fabricated PA is examined under various orders of amplitude modulations up to 1024-QAM, where robust EVM performance is achieved. It is noteworthy that this work explores a mature CMOS technology with relatively high parasitics to demonstrate a systematic, device-level power enhancement approach for >100-GHz PAs. By mitigating parasitic effects through the above mentioned innovations, the design achieves state-of-the-art output power and bandwidth at this frequency range. The proposed methodology is also readily scalable to more advanced nodes, where reduced parasitics and higher $f_{\mathrm{T}}/f_{\mathrm{max}}$ can further enhance gain, bandwidth, and PAE.

The paper is organized as follows: Section 2.2 presents the device-centric model of output power along with the proposed enhanced-power current-reuse cascode PA architecture. Section 2.3 details the analysis and design of the broadband 4-way power combiner/divider. Section 2.4 describes the circuit implementation, and Section 2.5 discusses the measurement

results. Finally, Section 2.6 concludes the chapter.

2.2 Enhanced Power Current-Reuse Cascode (EPCRC) PA Stage

To achieve high output power in a multi-stage power amplifier, the final stage plays a critical role. This stage, commonly referred to as the PA stage, is primarily designed to meet power delivery requirements.

In the cascode stage, two sub-stages—typically a common-source (CS) and a common-gate (CG) transistor—are cascaded. In the conventional cascode configuration, both the CS and CG sub-stages use transistors of identical size, and the same dc bias current flows through both devices. Ideally, under class-A biasing, the RF current swing at the drain of top CG substage can reach up to twice the dc bias current [47], as illustrated in Fig. 2.1(a). A generalized representation of this PA stage, composed of two cascaded sub-stages is shown in Fig. 2.1(b). The input power P_{in1} applied to the CS sub-stage (Sub-stg$_1$) appears at its output as P_{out1}. Neglecting the matching loss between the two sub-stages input power of second sub-stage, P_{in2}, is equal to P_{out1}. Subsequently, P_{out2} is generated by the CG sub-stage (Sub-stg$_2$) upon receiving P_{out1} at its input terminal, which ultimately sets the power limit of the cascode stage. To examine the effect of transistor sizing on P_{out2}, the gain and output power characteristics of two scenarios of cascode configurations with different transistor widths, 32 μm and 48 μm, are presented in Fig. 2.1(c) where the CS width is kept invariant at 32 μm. When $P_{out1} = 7$ dBm at 125 GHz is applied to the CG sub-stage, employing a smaller transistor leads to gain compression, resulting in an output power of 7.46 dBm. However, for the larger CG transistor, the gain compression is reduced and an output power of 9.1 dBm is achieved.

This comparison shows that employing non-identical transistor sizes in a conventional cas-

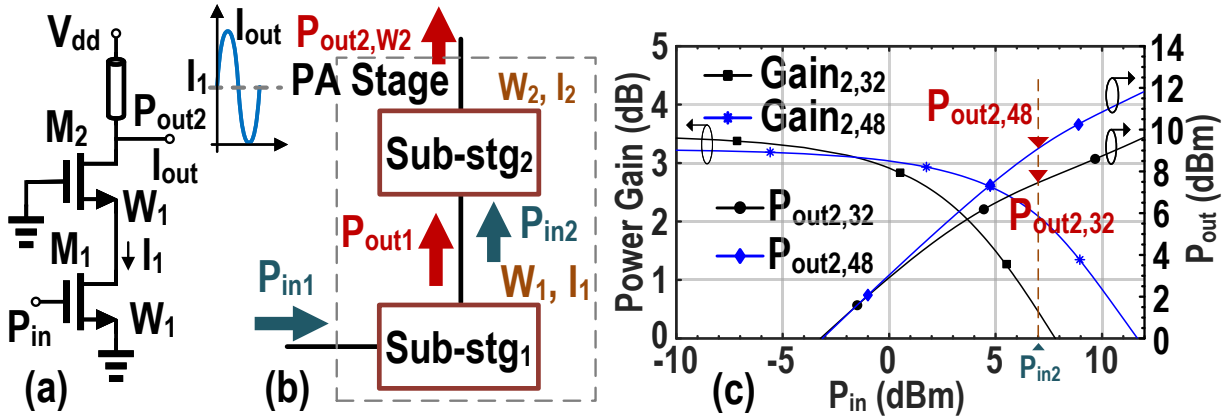

Figure 2.1: (a) Cascode stage with equal transistor widths, (b) cascode stage represented as a cascade of two sub-stages, and (c) gain and output power characteristics for CG sub-stages with widths of 32 μm and 48 μm.

code PA can boost output power, warranting deeper investigation for optimized design.

2.2.1 Device-Centric Nonlinear Output Power Model

A small-signal (SS) model for a transistor is shown in Fig. 2.2(a), where the parameters retain their conventional meanings. The model parameters can be extracted using a curve-fitting technique, as described in [48]. Small resistances R_g and R_d are included to enhance the model accuracy and account for metal routing losses at the gate and drain terminals, respectively. However, this SS model does not capture gain compression behavior when a large input signal is applied. In [48], large-signal effects are incorporated by manually substituting discrete transconductance values, g_{m0}, corresponding to various gain compression levels, into the SS model. These values are obtained through harmonic balance (HB) simulations under large-signal excitation. Alternatively, an extended small-signal (ESS) model can be developed by replacing the fixed g_m with an empirical function capturing its nonlinear behavior. A common approach approximates the nonlinear dependence of g_m on input using a Taylor series expansion [47], i.e.,

$$g_m(v_{gs}) = a_1 + 2a_2 v_{gs} + 3a_3 v_{gs}^2 + 4a_4 v_{gs}^3 + \cdots ,$$

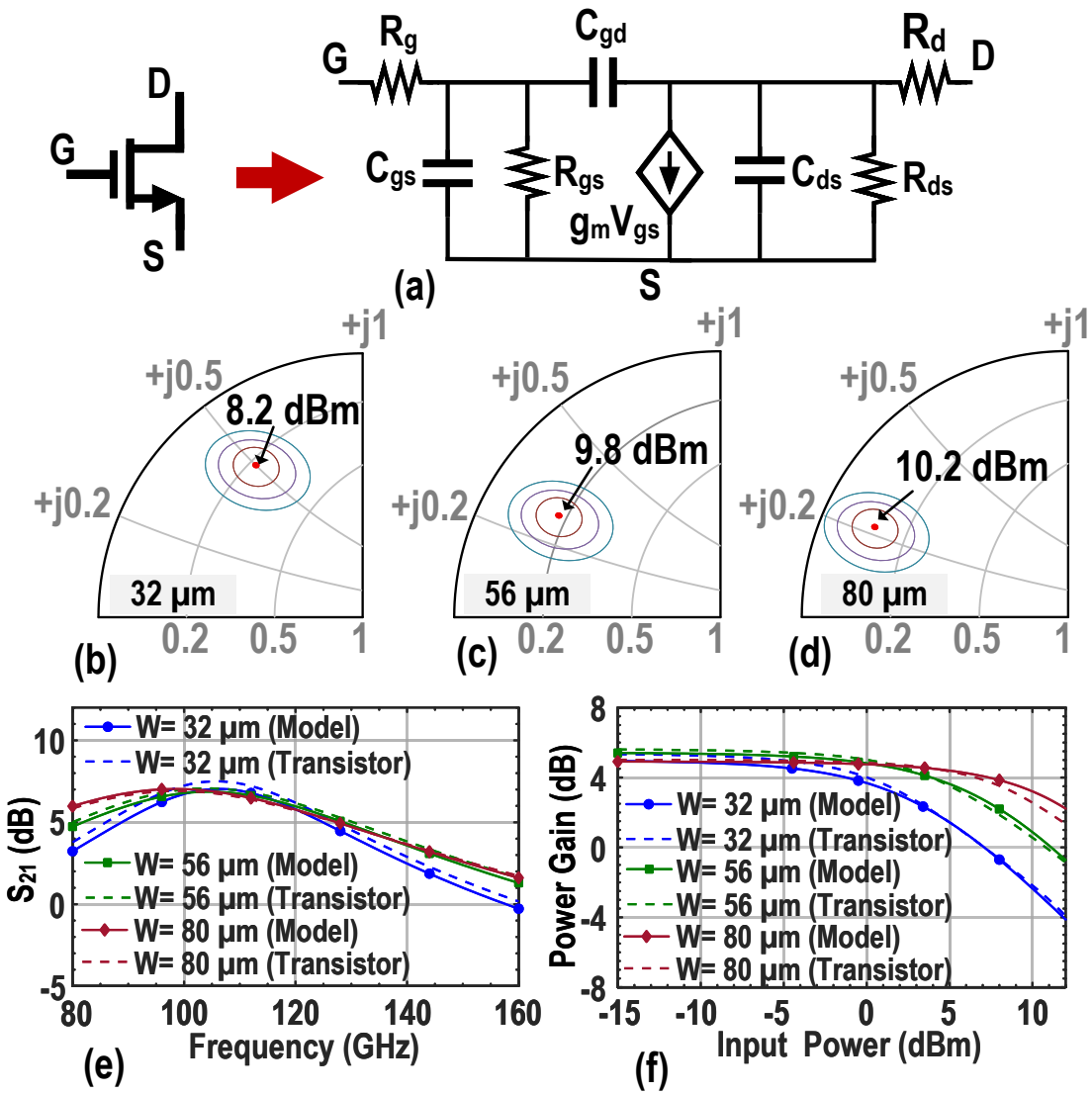

Figure 2.2: (a) Transistor and its small-signal equivalent model; (b)–(d) load-pull impedance for devices with $W = 32$ μm, 56 μm, and 80 μm, respectively; (e) comparison of small-signal gain; and (f) comparison of large-signal gain between the model and transistor simulations.

where a_i coefficients are obtained by empirical curve-fitting. While effective for small signals, the series diverges at higher input levels. To study output power, a more robust empirical model is required. We deploy a nonlinear g_m model based on mobility degradation at higher input voltages:

$$g_m(v_{gs}) = g_{m0}/(1 + \alpha v_{gs} + \beta v_{gs}^2) \tag{2.1}$$

Table 2.1: Model Parameter Values for Three Different Widths

W (μm)	R_g (Ω)	R_{gs} (kΩ)	C_{gs} (fF)	C_{gd} (fF)	g_{m0} (mS)	C_{ds} (fF)	R_{ds} (Ω)	R_d (Ω)	α	β
32	5.2	2.6	23.1	11.5	49	15.5	133.5	1.7	0.075	0.95
56	4.4	2.6	33.9	20.6	88	22.0	101.0	1.6	0.075	0.95
80	3.5	2.5	44.6	29.6	127	28.3	69.7	1.5	0.075	0.95

The rationale and derivation for this ESS model are detailed in Appendix A. In (2.1), the coefficients α and β are determined by fitting the large-signal behavior to the SS model results. As an illustration, model parameters for three transistor widths—32 μm, 56 μm, and 80 μm—are extracted and presented in Table 2.1. Notably, the parameters α and β remain fixed across different transistor sizes and gain compression levels as opposed to [48], simplifying the modeling process.

The loadpull impedances for three transistor widths, 32 μm, 56 μm and 80 μm are shown in Figs. 2.2(b)-(d). Using the output impedances from the loadpull simulations and the parameters listed in Table 2.1, both small- and large-signal responses of a CS amplifier stage are compared for 32 μm, 56 μm and 80 μm devices in Figs. 2.2(e) and 2.2(f), respectively. The comparison of small- and large-signal gains indicates that the model effectively captures both regimes.

2.2.2 Optimum Width W_2 of the CG Sub-Stage

A cascode stage employing a larger transistor for the CG sub-stage is shown in Fig. 2.3(a), where the excess current—defined as the difference between the currents in the CG and CS sub-stages—is drawn by an ideal current source. Intuitively, increasing the CG sub-stage transistor size raises the dc bias current, which in turn enables a larger current swing and higher output power. However, as shown in the following analysis, the output power does not increase monotonically beyond a certain point where excessive transistor sizing leads to

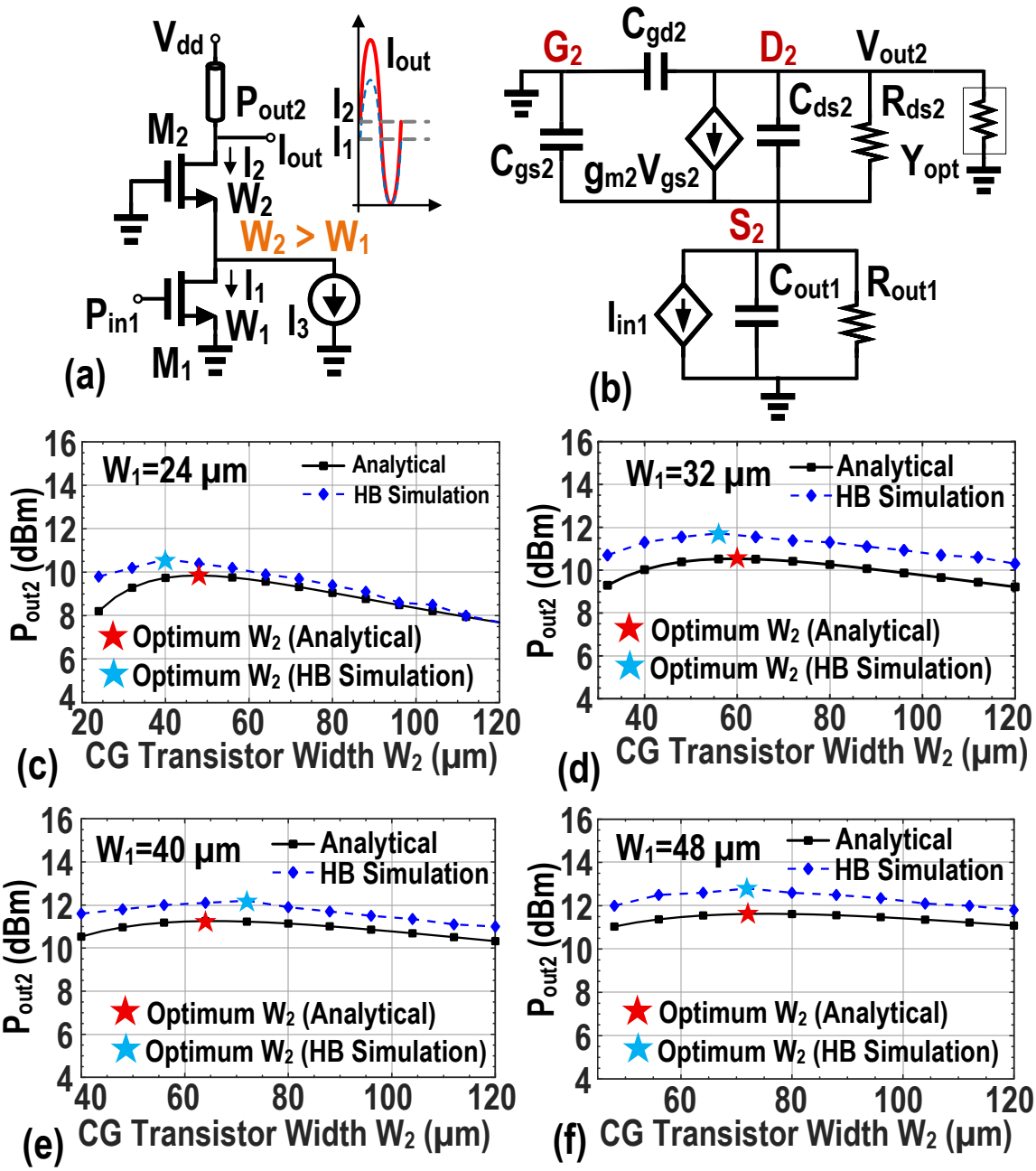

Figure 2.3: (a) Cascode stage schematic with enlarged CG transistor, (b) small-signal equivalent circuit, and comparison of P_{out2} from analytical modeling and simulation results for (c) $W_1 = 24\mu$m, (d) $W_1 = 32\mu$m, (e) $W_1 = 40\mu$m, and (f) $W_1 = 48\mu$m.

larger parasitics that lower the current swing and output power.

To enable analytical evaluation of the output power at the drain of the CG sub-stage, the CS sub-stage is modeled as a current source, $I_{\text{in1}} = g_{m1}V_{gs1}$, in parallel with an equivalent

output capacitance C_{out1} and resistance R_{out1}, as illustrated in Fig. 2.3(b). The CS sub-stage is assumed to operate in strong compression, which is captured using the ESS model for g_{m1}. In contrast, the CG sub-stage is assumed to be in the weak compression regime, and thus a SS model is employed.

The parameters C_{out1} and R_{out1} are extracted by terminating the CS-stage input with a matched impedance and evaluating the resulting drain admittance, modeled as a parallel combination of R_{out1} and C_{out1}. The CG sub-stage is terminated with the optimum admittance $Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}}$, where the $G_{\text{opt}} \approx I_{D2}/(V_{\text{DD}} - V_{\text{th2}})$ is the optimum conductance, and B_{opt} is intended to resonate with the total output capacitance [69]. To simplify the analysis, the small-valued series resistances R_{s2} and R_{d2}, along with the large parallel resistance R_{gs2}, are omitted from the equivalent circuit model. By Kirchhoff's current law (KCL) at node S_2 in Fig. 2.3(b):

$$I_{\text{in1}} + g_{m2}V_{s2} + (V_{s2} - V_{\text{out2}})(g_{ds2} + j\omega C_{ds2}) + V_{s2}(G_{\text{out1}} + j\omega(C_{gs2} + C_{\text{out1}})) = 0 \tag{2.2}$$

where $g_{ds2} = 1/R_{ds2}$ and $G_{\text{out1}} = 1/R_{\text{out1}}$.

Rearranging (2.2), the voltage at node S_2 is expressed as:

$$V_{s2} = \frac{-I_{\text{in1}} + g_{ds2}V_{\text{out2}} + j\omega C_{ds2}V_{\text{out2}}}{g_{ds2} + g_{m2} + G_{\text{out1}} + j\omega(C_{ds2} + C_{gs2} + C_{\text{out1}})} \tag{2.3}$$

I_{D2} and g_{m2} are related as derived in Appendix (B) for a short-channel transistor, and restated here for reference:

$$I_{D2} = (g_{m2}/\alpha) \cdot (V_{GS2} - V_{th2}) \tag{2.4}$$

where $\alpha = 1.22$, obtained from simulation for a 65 nm CMOS process. Subsequently, apply-

ing KCL at the drain node D_2 of the CG sub-stage leads to:

$$V_{\text{out2}}(Y_{\text{opt}} + j\omega C_{gd2}) + (V_{\text{out2}} - V_{s2})(g_{ds2} + j\omega C_{ds2}) - g_{m2}V_{s2} = 0 \tag{2.5}$$

The resulting output voltage V_{out2} is given by (2.6).

$$V_{\text{out2}} = \frac{jI_{\text{in}}\left(g_{ds2} + g_{m2} + j\omega C_{ds2}\right)}{-j\left[G_{\text{opt}}(g_{m2} + G_{\text{out1}}) + g_{ds2}G_{\Sigma}\right] + C_{\Sigma 2}\omega + jC_{\Sigma 1}\omega^2 + B_{\text{opt}}\left(G_T + j\omega(C_{ds2} + C_T)\right)} \tag{2.6}$$

where $C_T = C_{gs2} + C_{\text{out1}}$, $G_T = g_{ds2} + g_{m2} + G_{\text{out1}}$, $G_{\Sigma} = G_{\text{opt}} + G_{\text{out1}}$, $C_{\Sigma 1} = C_{gd2}C_T + C_{ds2}(C_{gd2} + C_T)$, and $C_{\Sigma 2} = C_T(g_{ds2} + G_{\text{opt}}) + C_{gd2}G_T + C_{ds2}G_{\Sigma}$.

The corresponding output power delivered to the optimal load is:

$$P_{\text{out2}} = (1/2)\,|V_{\text{out2}}|^2 G_{\text{opt}} \tag{2.7}$$

To investigate the influence of CG sub-stage transistor sizing on output power, the corresponding model parameters can be expressed as functions of the transistor width. For instance, C_{gs2} can be modeled using a linear relation, $C_{gs2} = C'_{gs2} \cdot W_2$. By comparing extracted values of C_{gs2} across different transistor sizes, the coefficients C'_{gs2} can be determined. Similarly, $g_{m2} = g'_{m2} \cdot W_2$, $C_{gd2} = C'_{gd2} \cdot W_2$, $C_{ds2} = C'_{ds2} \cdot W_2$ are assumed. By setting $\mathrm{d}P_{\text{out2}}/\mathrm{d}W_2 = 0$, the optimal W_2 can be evaluated. Figs. 2.3(c)–(f) compare the calculated and HB-simulated P_{out2} versus W_2 for $W_1 = 24$ μm, 32 μm, 40 μm, and 48 μm. The analytical results closely match the simulation- within 1.4 dBm, and locating the optimal W_2 within 4 μm-serving as the basis for the proposed current-reuse PA in the next subsection.

2.2.3 Proposed Three-Transistor Current-Reuse PA stage

To quantify the impact of device parasitics on the available power gain of the transistor, we evaluated GA_{max} for a fixed total device width of 48 μm realized with different parallel-

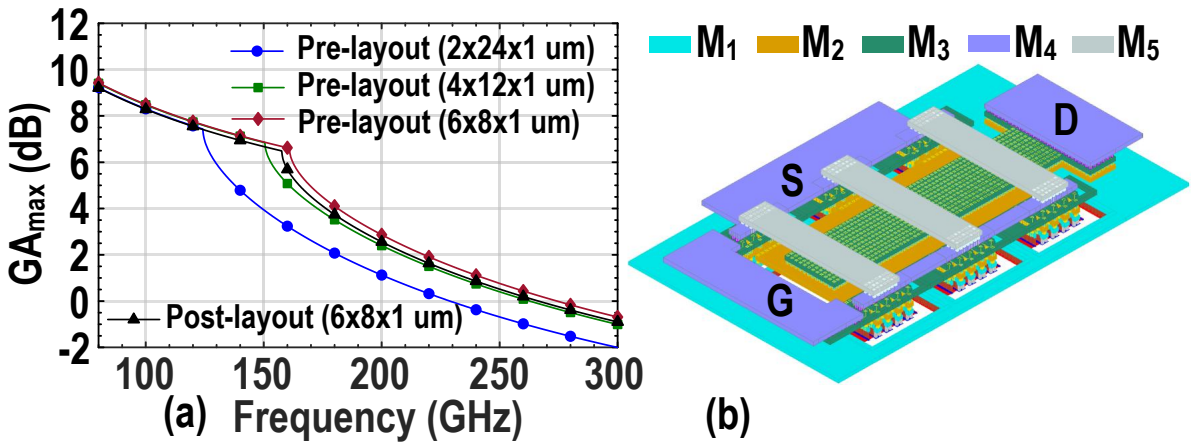

Figure 2.4: (a) $GA_{\max}$ for a 48-μm transistor realized as $2 \times 24 \times 1$ μm, $4 \times 12 \times 1$ μm, and $6 \times 8 \times 1$ μm; including the post-layout curve for $6 \times 8 \times 1$ μm. (b) Layout of the $6 \times 8 \times 1$ μm transistor cell.

unit/finger configurations: $2 \times 24 \times 1$ μm, $4 \times 12 \times 1$ μm, and $6 \times 8 \times 1$ μm. The shorthand $M \times NF \times WF$ denotes M parallel unit devices (multipliers), each having NF gate fingers of width WF (in μm); for example, $6 \times 8 \times 1$ μm corresponds to six parallel devices with eight 1 μm fingers each. The resulting $G\mathrm{A}_{\max}$ trends are shown in Fig. 2.4(a), where the $6 \times 8 \times 1$ μm option yields the highest $G\mathrm{A}_{\max}$. Its layout appears in Fig. 2.4(b). Post-layout parasitics were extracted (Calibre PEX) up to metal-4 (M4) on gate, source, and drain; the corresponding post-layout curve is also plotted in Fig. 2.4(a). Due to added metallization parasitics, $f_{\max}$ decreases from 274 GHz to 266.5 GHz. The same layout methodology is applied to all other transistor cells.

At frequencies above 100 GHz and near $f_{max}/2$, the power gain degrades due to the increased transistor parasitics [70]. In [71], a small-signal model is utilized to demonstrate the power gain degradation in a cascode LNA due to the parasitic capacitance at the drain of CS sub-stage. Building on top of the enlarged CG transistor cascode in Fig. 2.3(a) and to mitigate the gain degradation due to parasitics, the schematic of the proposed enhanced power current-reuse cascode PA stage (EPCRC) is shown in Fig. 2.5(a) where additional transistor M_3 replaces the ideal current source. This change (i) reuses the dc current dictated by the larger CG device M_2 and (ii) enables M_3 to contribute to the RF gain. To realize (ii),

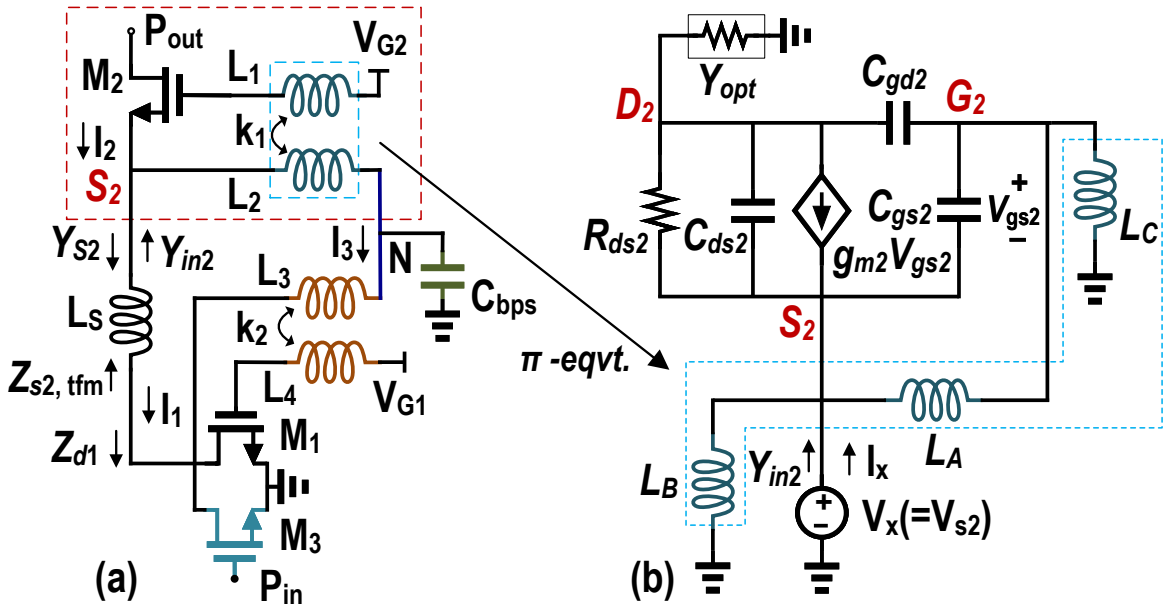

Figure 2.5: (a) Current-reuse cascode stage, and (b) small-signal equivalent model of M_2 with the π-model representation of coupled inductors L_1 and L_2.

the RF input is applied to the gate of M_3 (CS configuration) rather than to M_1; using M_3 solely as a current sink would dissipate power with no gain benefit. The device M_3 is sized to draw the excess dc current set by M_2, preserving the intended bias of the M_1, M_2 cascode; in this sense, M_3 reuses the excess current of M_2 in the dc domain. The drain of M_3 then excites the gate of M_1 through coupled inductors L_3 and L_4. Although L_3, L_4 introduce a small insertion loss, the additional CS gain contributed by M_3 more than compensates it, improving the overall stage gain.

Two design strategies are adopted to neutralize the parasitics of CS and CG sub-stages, 1) coupling the gate of M_2 to its source using coupled inductors L_1 and L_2 at a coupling coefficient k_1, 2) inserting inductor L_S between the drain of M_1 and source of M_2 to help improve the matching between M_1 and M_2. The neutralization strategy used to compensate M_2's parasitic capacitances is evaluated with its SS equivalent model, shown in Fig. 2.5(b). The analysis assumes the neutralization remains valid at large signal levels because the parasitics vary negligibly with transistor swing.

With the coupled inductor replaced by its equivalent π-model, as shown in Fig. 2.5(b), the relationships between the original inductors L_1, L_2 and the π-model components L_A, L_B, and L_C are given in (2.8)–(2.10) [72]. The mutual inductance is defined as $M_1 = k_1\sqrt{L_1 L_2}$. The bypass capacitor, C_{bps}, at node N in Fig.2.5(a) effectively acts as an RF short, which is a valid assumption especially when the differential version is realized. The coupled inductors L_3 and L_4, with a coupling coefficient k_2, are employed to provide impedance matching between transistors M_1 and M_3.

$$L_A = (L_1 L_2 - M_1^2)/M_1 \tag{2.8}$$

$$L_B = (L_1 L_2 - M_1^2)/(L_1 - M_1) \tag{2.9}$$

$$L_C = (L_1 L_2 - M_1^2)/(L_2 - M_1) \tag{2.10}$$

From the π-model equivalent of the coupled inductor in Fig. 2.5(b), the inductance L_A appears in parallel with C_{gs2}, effectively neutralizing its capacitive effect and thereby enhancing the power gain. As the next step, the input admittance looking into the source of transistor M_2 is considered. The drain of M_2 is terminated by an admittance Y_{opt}, and an external voltage source V_x is applied while measuring the resulting input current I_x. By applying KCL at the gate node G_2 the gate voltage V_{g2} can be expressed as,

$$V_{g2} = \frac{j\omega C_{gd2} V_{d2} + (j\omega C_{gs2} + 1/j\omega L_A)\, V_{s2}}{1/j\omega L_C + j\omega(C_{gd2} + C_{gs2})}. \tag{2.11}$$

Similarly, using KCL at node D_2, V_{d2} can be evaluated as,

$$V_{d2} = \frac{j\omega C_{gd2} V_{g2} + (g_{m2} + g_{ds2} + j\omega C_{ds2}) V_{s2}}{G_{opt} + jB_{opt} + g_{ds2} + j\omega(C_{ds2} + C_{gd2})} \tag{2.12}$$

where, $G_{opt} + jB_{opt} = Y_{opt}$ is the load admittance. The total current entering the source of M_2 is given by,

$$I_x = V_{s2}/(j\omega L_B) - (1/(j\omega L_A) + j\omega C_{gs2})V_{gs2} - g_m V_{gs2} + (g_{ds2} + j\omega C_{ds2})(V_{s2} - V_{d2}) \quad (2.13)$$

Using (2.11)–(2.13), the input admittance is determined as $Y_{\text{in2}} = I_{\text{x}}/V_{s2}$. The corresponding real and imaginary components expressed as $Y_{\text{in2}} = G_{\text{in2}} + jB_{\text{in2}}$, are given by:

$$G_{\text{in2}} = \underbrace{\frac{g_{m2}\left[-K_L\left((\omega/\omega_1)^2 - 1\right) + \left((\omega/\omega_2)^2 - 1\right)\right]}{(\omega/\omega_2)^2 - 1}}_{\text{Trm}_{A1}} + \underbrace{G_{opt}}_{\text{Trm}_{A2}} + \underbrace{g_{ds2}}_{\text{Trm}_{A3}} \quad (2.14)$$

$$B_{\text{in2}} = \underbrace{\frac{(\omega/\omega_3)^2 - 1}{\omega L_{AB}}}_{\text{Trm}_{B1}} - \underbrace{\frac{K_L\left((\omega/\omega_1)^2 - 1\right)^2}{\omega L_A\left((\omega/\omega_2)^2 - 1\right)}}_{\text{Trm}_{B2}} + \underbrace{\omega(C_{gd2} + C_{ds2})}_{\text{Trm}_{B3}} + \underbrace{B_{opt}}_{\text{Trm}_{B4}} \quad (2.15)$$

Here, $g_{ds2} = 1/R_{ds2}$. The effective inductances are defined as $L_{AC} = L_A L_C/(L_A + L_C)$ and $L_{AB} = L_A L_B/(L_A + L_B)$, with $K_L = L_{AC}/L_A$. The characteristic frequencies are defined as $\omega_1 = 1/\sqrt{L_A C_{gs2}}$, $\omega_2 = 1/\sqrt{L_{AC} C_{gs2}}$, and $\omega_3 = 1/\sqrt{L_{AB} C_{gs2}}$. These frequencies depend on C_{gs2} and the components L_1, L_2, and k_1, through L_A, L_B, and L_C. The real part G_{in2} comprises three components: Trm_{A1}, Trm_{A2}, and Trm_{A3}, while the imaginary part B_{in2} consists of four components: Trm_{B1} through Trm_{B4}. By tuning L_1, L_2, and k_1, both the magnitude of G_{in2} and the sign of B_{in2} can be adjusted. Perfect neutralization is achieved when $B_{\text{in2}} = 0$.

To better understand the input impedance behavior, the input resistance and reactance are plotted in Fig. 2.6(a) and (b), using impedance rather than admittance for improved interpretability. A load impedance of $Z_{opt} = 15 + j45\ \Omega$ is chosen, representative of typical

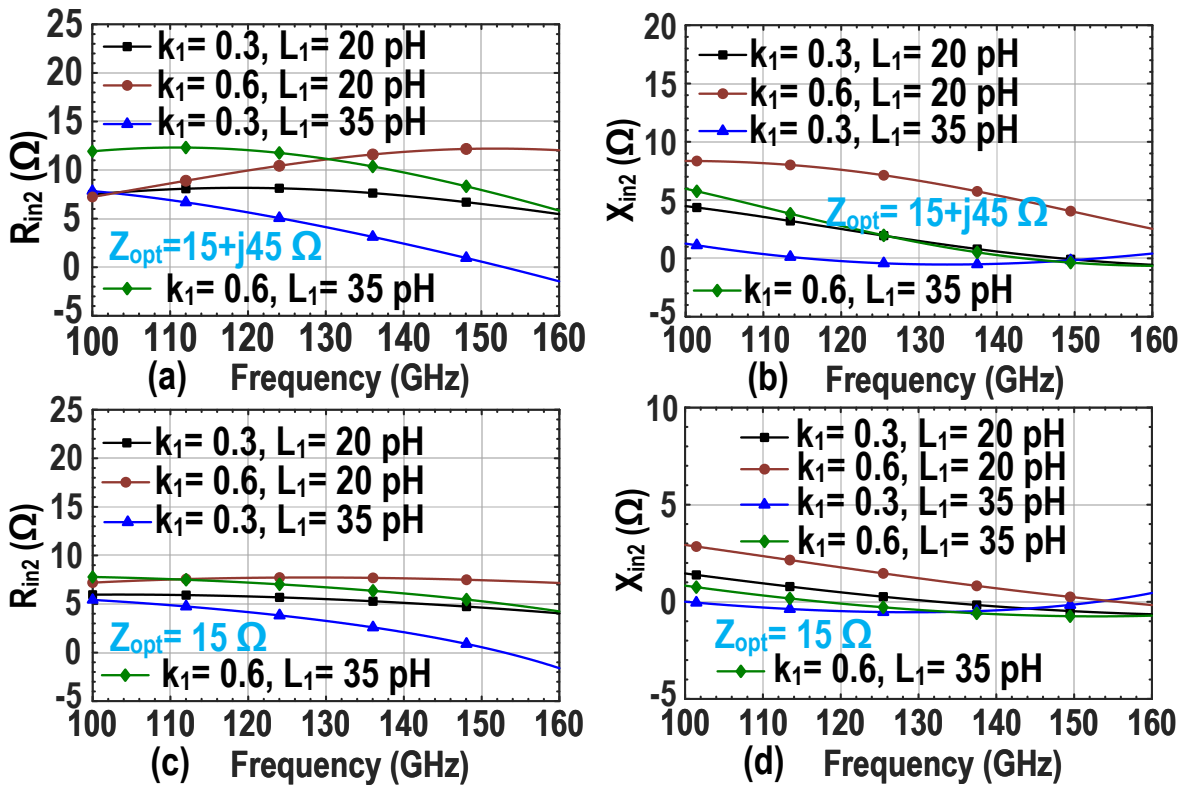

Figure 2.6: Real and imaginary components of the input impedance of the CG sub-stage: (a) R_{in2} and (b) X_{in2} for load impedance $Z_{opt} = 15 + j45\ \Omega$; (c) R_{in2} and (d) X_{in2} for purely resistive load $Z_{opt} = 15\ \Omega$.

PA output impedances with real and imaginary parts in the range of 10–20 Ω and 35–60 Ω, respectively. The analysis uses $L_1 = L_2$ and small-signal parameters from the 56 μm case in Table 2.1.

As shown in Fig. 2.6(a), R_{in2} remains positive but can become negative at higher frequencies for smaller k_1 and larger L_1. These two parameters provide effective control over R_{in2}. In Fig. 2.6(b), X_{in2} is initially positive, confirming the cancellation of C_{gs2}, but may turn negative at higher frequencies depending on k_1 and L_1. One might attribute the observed positive reactance to the large reactive component of the load; however, to isolate this effect, a purely resistive load of 15 Ω is also considered. The resulting plots in Fig. 2.6(c)–(d) show that a positive X_{in2} is still attainable, albeit smaller, through appropriate tuning of k_1 and L_1. This confirms that the positive input reactance is primarily due to the cancellation of

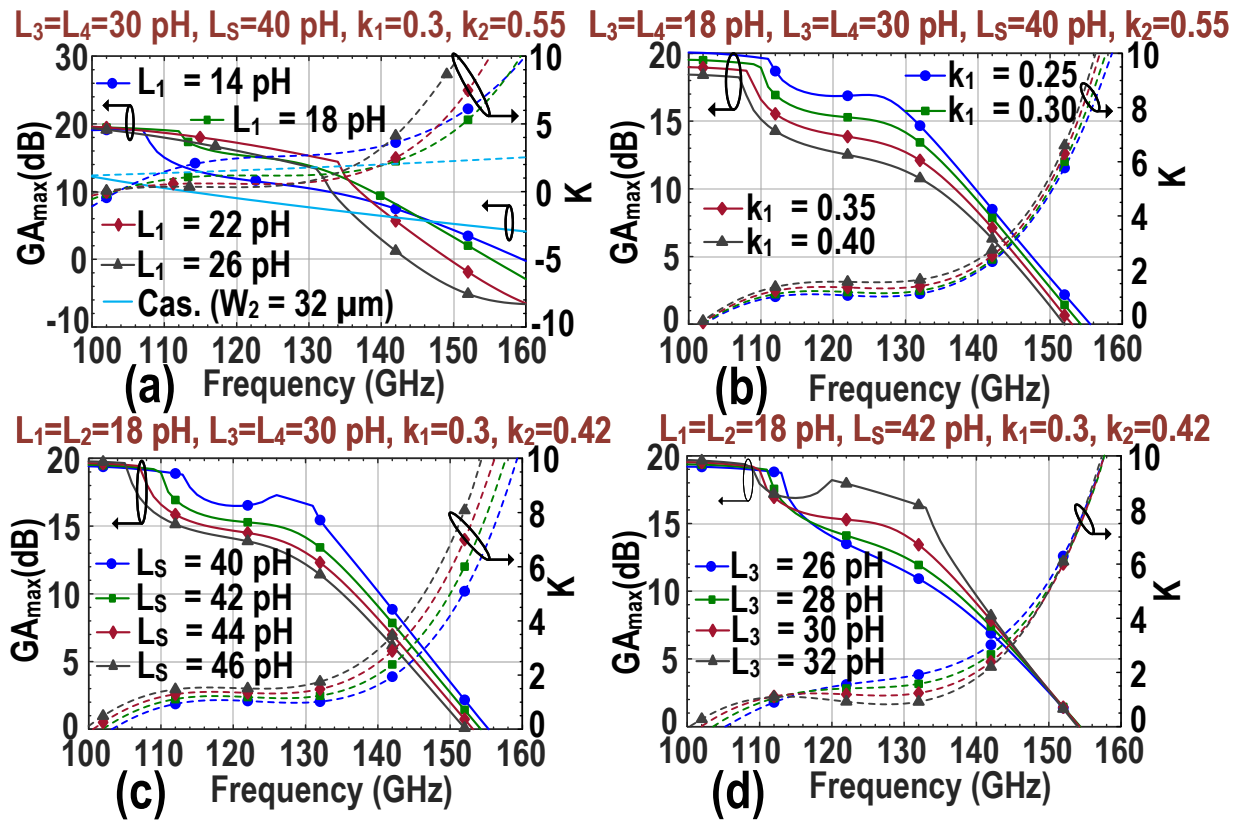

Figure 2.7: Plots of $GA_{\max}$ and K for variations in (a) L_1, (b) k_1, (c) L_S, and (d) L_3, with fixed parameters shown atop each. In (a), a reference for the cascode stage with $W_2 = 32$ μm is included alongside the single-ended design.

C_{gs2}. To better understand the second neutralization strategy, it is found that the input impedance of the CG-substage after undergoing transformation through L_S, $Z_{s2,tfm}$ in Fig. 2.5(a) becomes $R_{in2}+jX_{in2}+j\omega Ls$. In case when Z_{in2} is still left with some residual negative reactance X_{in2} despite employing the first neutralization technique, this added inductor L_S will help achieve neutralization without affecting the real part. To further validate the neutralization strategies detailed above within the schematic presented in Fig. 2.5(a), a PA stage is simulated with transistor widths selected as $W_1 = 32$ μm, $W_2 = 56$ μm, and $W_3 = 24$ μm. The simulations utilize post-layout transistor models extracted up to Metal 4. The variation of maximum available gain ($G_{\max}$) with different parameters is shown in Fig. 2.7. To avoid confusion with conductance terms, we adopt $GA_{\max}$ for the rest of this paper. The inductor values are chosen such that $L_1 = L_2$ and $L_3 = L_4$. The resulting plots

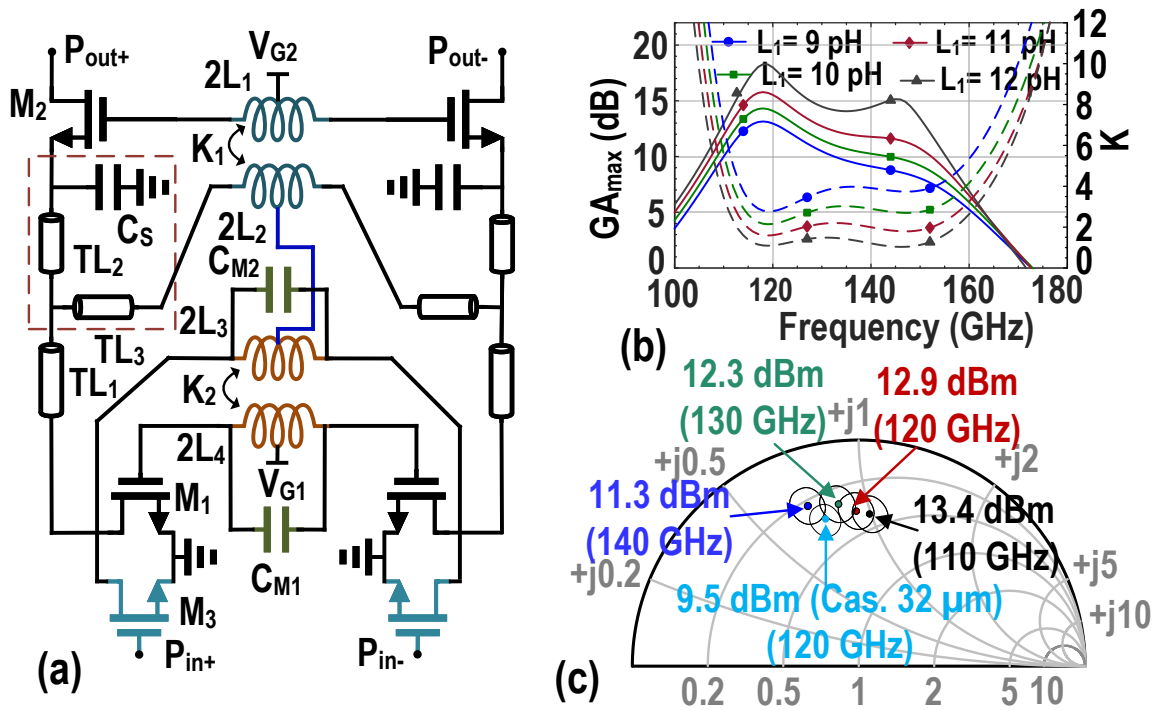

Figure 2.8: (a) Proposed differential EPCRC stage, (b) $GA_{\max}$ for varying $L_1 = L_2$, and (c) output power contours.

yield the following insights:

1). As shown in Fig. 2.7(a), increasing L_1 causes greater roll-off at high frequencies, while smaller L_1 improves $GA_{\max}$ at low frequencies and enhances stability.

2). Fig. 2.7(b) shows that larger k_1 improves low-frequency stability but reduces high-frequency gain.

3). Similar to k_1, increasing L_S enhances low-frequency gain, as seen in Fig. 2.7(c).

4). Fig. 2.7(d) highlights that proper tuning of L_3, which matches M_1 and M_3, ensures stable gain.

The above-mentioned trends confirm that with optimized parameters, $GA_{\max}$ exceeds 14 dB at 110 GHz and 9 dB at 140 GHz. For comparison, a cascode stage with $W_1 = W_2 = 32$ μm achieves only 10.5 dB at 110 GHz and less than 6.5 dB $GA_{\max}$ at 140 GHz, validating

the superior performance of the proposed design. The differential implementation of the proposed EPCRC PA stage in Fig. 2.5(a) is depicted in Fig. 2.8(a). In this structure, the inductor L_S is replaced by its transmission line (TL) equivalent, TL_1, which provides a higher quality factor [73]. To accommodate the layout footprint of the coupled inductors L_1 and L_2, additional TL segments, TL_2 and TL_3, are inserted between TL_1, the source of M_2, and inductor L_2. The increased inductance introduced by TL_2 is compensated by incorporating a shunt capacitor C_S at the source of M_2. For improved impedance matching between the drain of M_3 and the gate of M_1, matching capacitors C_{M1} and C_{M2} are introduced. A parametric sweep of L_1 and the corresponding $GA_{\max}$ response is shown in Fig. 2.8(b), demonstrating that with proper components that satisfy both neutralization strategies, the structure can achieve $GA_{\max}$ values exceeding 13.5 dB at 140 GHz. The load-pull contours in Fig. 2.8(c) further indicate that the proposed architecture achieves $P_{\mathrm{out}} = 13.4$ dBm. For comparison, a cascode stage with $W = 32$ μm achieves approximately 9.5 dBm at 120 GHz. The attainable P_{out} is slightly reduced by implementation losses, including transmission-line attenuation (≈ 1.68 dB/mm), Q of inductors, and additional metal-routing parasitics within the transistor cell.

2.3 4-Way Dual-Coupled Differential Power Combiner (DCDPC)

As discussed in Section 2.2, the proposed EPCRC PA stage boosts the power and gain by utilizing a configuration that mitigates the impact of device parasitics. However, increasing the CG transistor to a larger value introduces increased parasitic capacitance even in the presence of mitigation techniques and lowers the optimum output impedance. This, in turn, degrades gain and bandwidth, thereby limiting the maximum achievable power from a single PA stage. To overcome this limitation and further increase the output power, a slotline-based 4-way DCDPC is proposed.

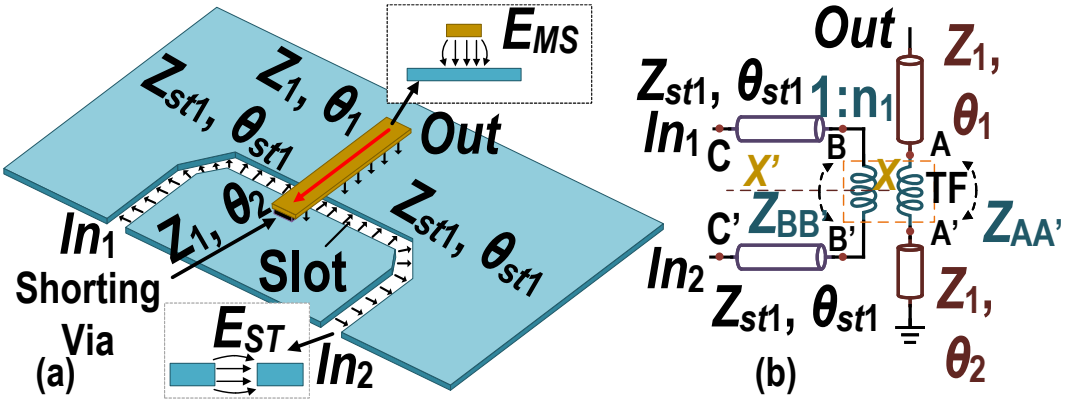

Figure 2.9: (a) Microstrip-to-slotline transition, (b) equivalent circuit.

2.3.1 Microstripline to slotline transition

The microstrip transmission line (MS-TL) to slotline transmission line (ST-TL) transition is illustrated in Fig. 2.9(a). In the MS-TL, the electric field is confined between the signal line and the underlying ground, while the magnetic field forms a loop around the line—supporting transverse electromagnetic (TEM) mode propagation. This TEM-mode signal couples to the ST-TL, which supports only transverse electric (TE) mode propagation. This coupling is represented by an ideal transformer (TF), as shown in its equivalent circuit in Fig. 2.9(b). The transformer turn ratio, n_1, is defined in (C.1) in Appendix C. As evident from (C.1), for a given technology with fixed permittivity, the coupling strength (or n_1) depends only on the MS and ST-TL widths and their elevation.

The output is terminated with a $Z_0 = 50\ \Omega$ load at the Out port. This load is transformed by the MS-TL, with impedance Z_1 and electrical length θ_1, to node A, resulting in:

$$Z_{AA'} = Z_1 \frac{Z_0 + jZ_1 \tan\theta_1}{Z_1 + jZ_0 \tan\theta_1} + jZ_1 \tan\theta_2 \tag{2.16}$$

This impedance is transferred to the secondary of the transformer across terminals BB' as:

$$Z_{BB'} = Z_{AA'}/n_1^2 \tag{2.17}$$

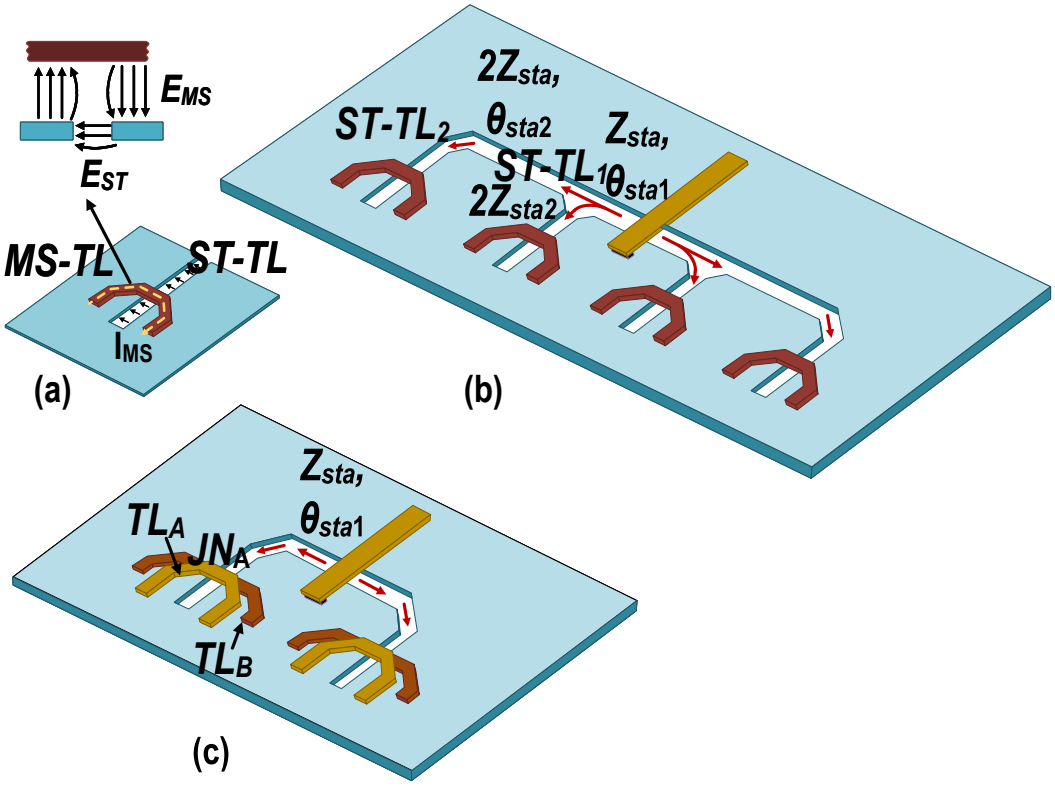

Figure 2.10: (a) Slotline to microstrip transition, (b) an alternative 4-way differential configuration, and (c) the proposed 4-way DCDPC

2.3.2 Combined 4-way DCDPC

Similar to the MS-TL to ST-TL transition, the TE-mode signal propagating along the slotline can couple to the MS-TL, as illustrated in Fig. 2.10(a). The TE-mode electric field interfaces vertically with the MS-TL above, inducing opposing E-fields on either side of the MS line, thereby generating a differential current, as shown in the inset of Fig. 2.10(a).

This differential-to-single-ended conversion mechanism, combined with the MS-TL to ST-TL interface, enables power combining of multiple differential signals. Prior work in [37, 66] demonstrated 2-way and 4-way single-ended slotline-based combiners in CMOS and SiGe technologies, respectively. To scale output power further, more differential paths can be added. However, increasing the number of branches also increases the ITR, reducing bandwidth. A 4-way differential (8-way single-ended) combiner offers higher power without significantly degrading ITR. One such configuration is shown in Fig. 2.10(b), where each slotline

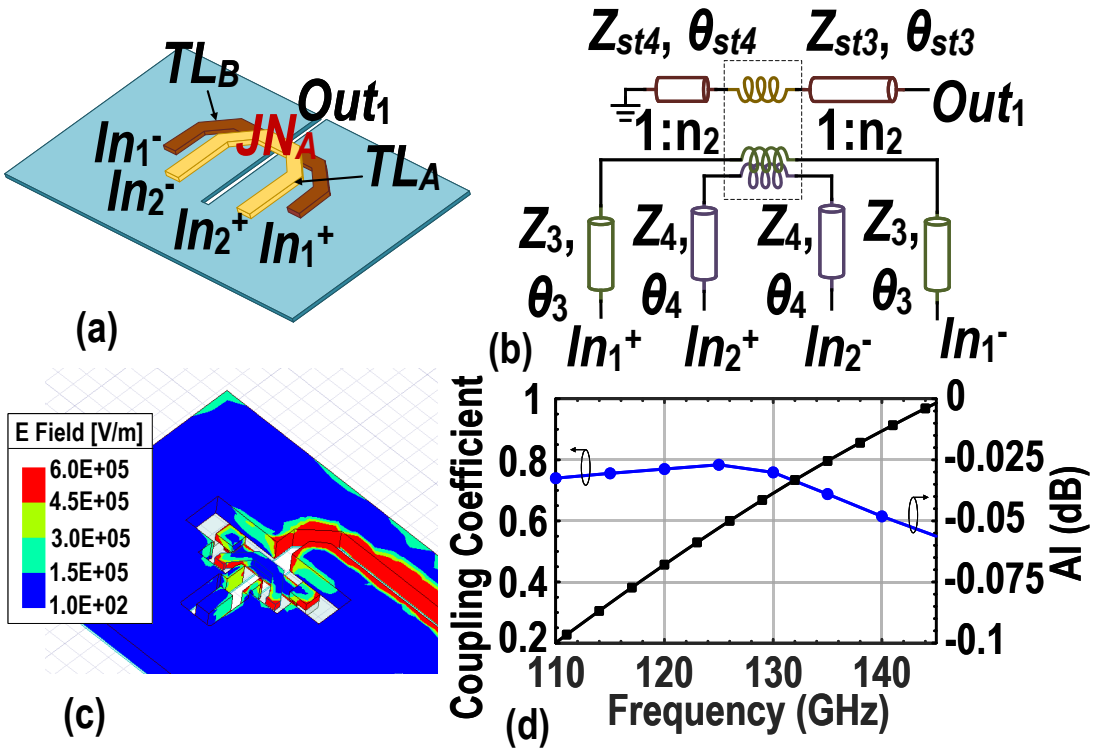

Figure 2.11: (a) Dual-coupled slotline-to-microstrip transition, (b) equivalent circuit, (c) electric field near the interface, and (d) plots for the amplitude imbalance (AI) and coupling coefficient between TL_A and TL_B versus frequency.

side is split into two to accommodate additional differential paths. This division doubles the impedance to $2Z_{\text{sta}}$, increasing ITR and creating port asymmetry due to unequal path lengths. The added slotline segment ST-TL_2 causes higher insertion loss for outer differential ports. A 4-way combiner addressing this asymmetry using additional lines and stubs was proposed in [67], though insertion loss mismatch remains unaddressed.

To overcome these limitations, we propose a 4-way slotline-based dual-coupled differential combiner, shown in Fig. 2.10(c). Here, two differential MS-TLs—TL_A and TL_B—are vertically stacked and coupled to the slotline. TL_A is routed on the top metal (M9), and TL_B on the adjacent lower layer (M8). This vertical coupling avoids slotline branching, preserving impedance balance and reducing loss. Since the dual-coupling can be modeled as two transformers, the ITR remains low compared to parallel slotline division. For example, splitting a 50 Ω line yields 100 Ω branches, whereas a 1:n transformer presents a $100/n^2$ Ω primary

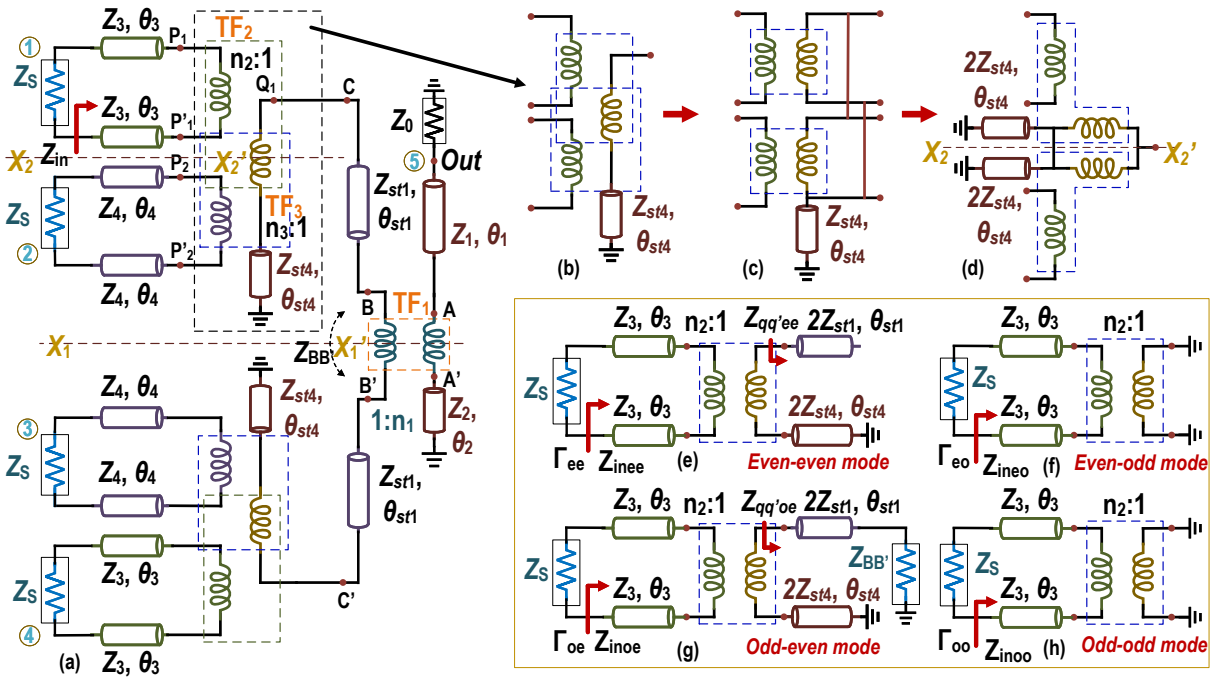

Figure 2.12: (a) Equivalent circuit of the 4-way DCDPC, (b)–(d) step-by-step transformation of the dual-coupled transformer, highlighting symmetry across X_2X_2' in (d), (e)–(h) even-odd mode decomposition showing the quarter-circuit representations of (e) even-even, (f) even-odd, (g) odd-even, and (h) odd-odd modes.

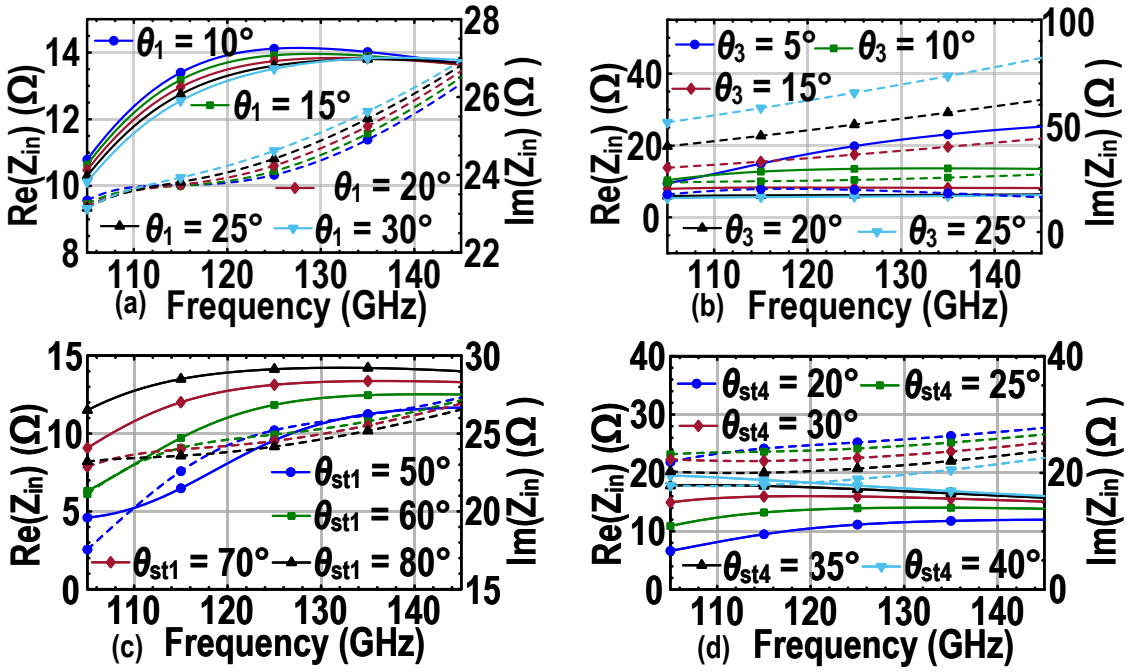

Figure 2.13: Plots of $Re(Z_{in})$ (solid, left axis) and $Im(Z_{in})$ (dotted, right axis): (a) versus θ_1, (b) versus θ_3, (c) versus θ_{st1}, and (d) versus θ_{st4}.

load, improving the bandwidth.

Additionally, the absence of extra slotline segments ensures insertion loss remains low and consistent across all differential ports. A simplified dual-coupling structure is shown in Fig. 2.11(a), with its equivalent transformer model in Fig. 2.11(b). $\mathrm{TL_A}$ and $\mathrm{TL_B}$ have characteristic impedances Z_3, Z_4 and electrical lengths $2\theta_3$, $2\theta_4$, respectively. The slotline leading to $\mathrm{Out_1}$ is modeled with Z_{st3} and θ_{st3}, while a shorted stub with Z_{st4} and θ_{st4} terminates the opposite end.

When identical differential signals are applied to both ports, the two lines behave as a single combined path with negligible mutual coupling. However, differences in elevation from the slotline introduce slight coupling imbalances, which can be minimized by adjusting the TL width and height. EM simulations in Fig. 2.11(c) show the E-field distribution with both TLs of equal length coupled to the slotline. $\mathrm{TL_B}$ transitions to the top metal through edge vias, while $\mathrm{TL_A}$'s width is tapered near the coupling region to balance the field distribution. As shown in Fig. 2.11(d), the coupling between them is more than 0.6, and the amplitude imbalance is below 0.1 dB across 110–140 GHz.

The equivalent circuit representation of the proposed 4-way dual-coupled differential power combiner (DCDPC), shown in Fig. 2.10(c), is illustrated in Fig. 2.12(a). Ports 1–4 represent the differential input ports, each terminated with a complex source impedance Z_S, while Port 5 is the single-ended output port terminated to $Z_0 = 50\ \Omega$.

The input impedance Z_{in} at each port is influenced not only by the transmission lines, transformers, and output terminations but also by the impedance terminations at adjacent ports due to the symmetrical nature of the structure. Specifically, the circuit exhibits two planes of symmetry—one along the axis X_1X_1' and another along the axis X_2X_2' which will become clear after redrawing the dual-coupled transformer. These symmetries enable the network to be decomposed into four equivalent quarter circuits using even–odd mode

analysis.

To illustrate symmetry across X_2X_2', the transformer and stub sections are redrawn in Figs. 2.12(b)–(d), with Fig. 2.12(d) explicitly revealing the symmetry about X_2X_2'.

With both X_1X_1' and X_2X_2' symmetries established, the network can be analyzed using four quarter circuits: even–even (ee), even–odd (eo), odd–even (oe), and odd–odd (oo), as illustrated in Figs. 2.12(e)–(h). Here, the two turn ratios are assumed to be equal. For each case, the input impedance $Z_{\text{in},ij}$ $(i, j \in \{\text{ee}, \text{eo}, \text{oe}, \text{oo}\})$ is calculated, and the corresponding reflection coefficients are given by:

$$\Gamma_{ij} = (Z_{\text{in},ij} - Z_S^*)/(Z_{\text{in},ij} + Z_S) \tag{2.18}$$

The overall S_{11} is then computed as:

$$S_{11} = (1/4) \sum \Gamma_{ij} \tag{2.19}$$

From this, the port input impedance is evaluated as:

$$Z_{\text{in}} = (-S_{11} Z_S - Z_S^*)/(S_{11} - 1) \tag{2.20}$$

For the even–even (ee) mode, shown in Fig. 2.12(e), the open stub of electrical length θ_{st1} and the shorted stub of length θ_{st4} appear in series across the secondary of the transformer. Their combined impedance is:

$$Z_{qq',\text{ee}} = -j\, 2Z_{st1}/\tan\theta_{st1} + j\, 2Z_{st4} \tan\theta_{st4} \tag{2.21}$$

This is reflected to the transformer primary as $n_2^2 Z_{qq',\text{ee}}$, and further transformed by the TL

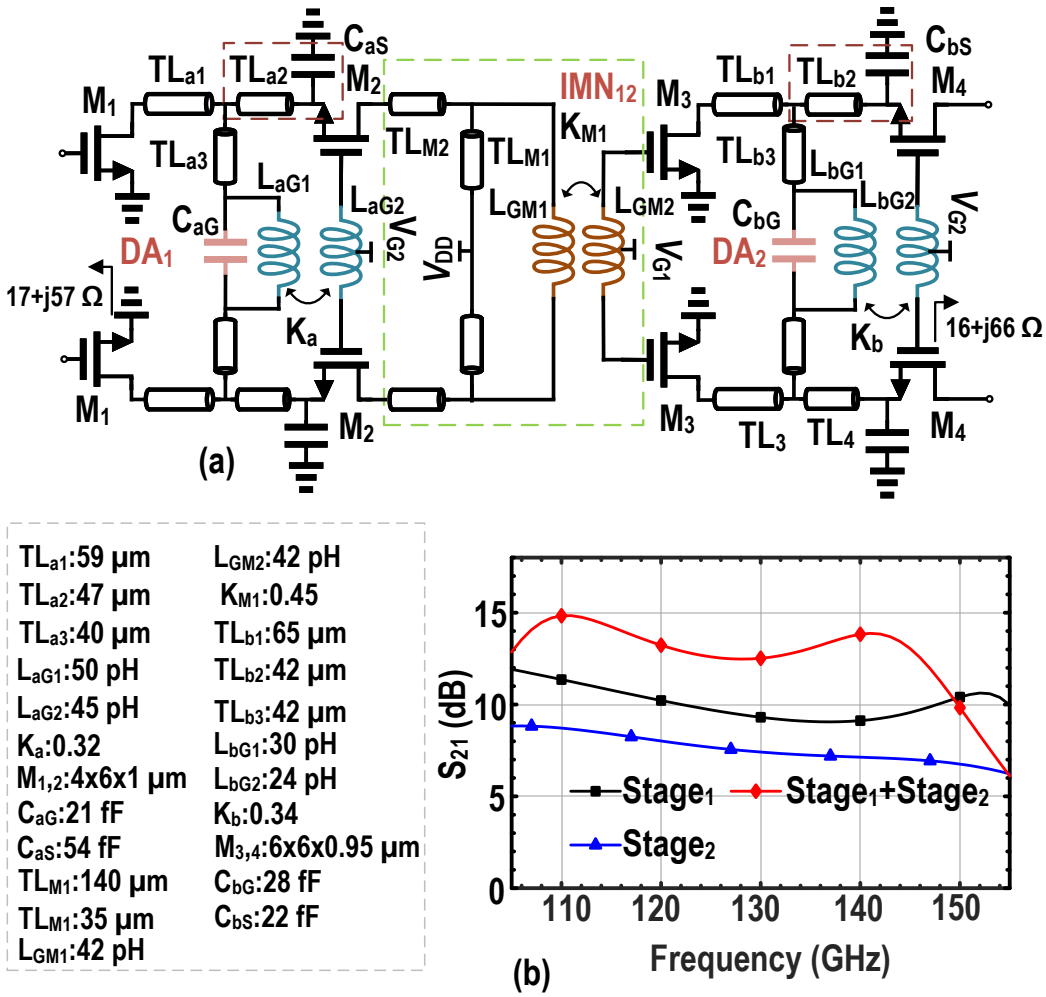

Figure 2.14: (a) Schematic for two-stage DA, and (b) small-signal gain for both stages along with the overall gain.

of length θ_3:

$$Z_{\text{in,ee}} = 2Z_3 \cdot \frac{(n_2^2 Z_{qq',\text{ee}})/2 + jZ_3 \tan\theta_3}{Z_3 + j(n_2^2 Z_{qq',\text{ee}})/2 \cdot \tan\theta_3} \tag{2.22}$$

In the even–odd (eo) mode, shown in Fig. 2.12(f), a short at the secondary results in a corresponding short at the primary. The resulting input impedance is:

$$Z_{\text{in,eo}} = j2Z_3 \tan\theta_3 \tag{2.23}$$

The odd–even (oe) mode, illustrated in Fig. 2.12(g), yields a combined impedance across the

secondary as:

$$Z_{qq',\text{oe}} = j2Z_{st4}\tan\theta_{st4} + 2Z_{st1}\cdot\frac{Z_{BB'} + j2Z_{st1}\tan\theta_{st1}}{2Z_{st1} + jZ_{BB'}\tan\theta_{st1}} \tag{2.24}$$

This becomes $n_2^2 Z_{qq',\text{oe}}$ at the primary, and the $Z_{in,oe}$ of:

$$Z_{\text{in,oe}} = 2Z_3\cdot\frac{(n_2^2 Z_{qq',\text{oe}})/2 + jZ_3\tan\theta_3}{Z_3 + j(n_2^2 Z_{qq',\text{oe}})/2\cdot\tan\theta_3} \tag{2.25}$$

Finally, the odd–odd (oo) mode as shown in Fig. 2.12(h) is identical to the even–odd mode due to the symmetric short-circuit condition, yielding:

$$Z_{\text{in,oo}} = j2Z_3\tan\theta_3 \tag{2.26}$$

The impact of various line lengths on the real and imaginary parts of Z_{in}, and its deviation from the real and imaginary parts of Z_S can be observed using (2.20). It is to be noted that all the line lengths are defined at the design frequency f_0, so any line with a length θ is defined as $\theta = \theta_0\cdot(f/f_0)$.

To achieve effective impedance matching, both the real and imaginary components of the Z_{in} must closely approximate those of the Z_S. As an illustrative example, consider $Z_S = 15 - j28\ \Omega$. The variation of $Re(Z_{in})$ and $Im(Z_{in})$ with respect to the electrical length θ_1 is shown in Figs. 2.13(a). A smaller θ_1 results in a closer alignment of $Re(Z_{in})$ with Z_S, while also minimizing the deviation in $Im(Z_{in})$. An electrical length $\theta_3 \approx 10°$ yields a favorable match in the real part with acceptable deviation in the imaginary part, as observed in Fig. 2.13(b).

However, increasing θ_3 leads to a reduction in $Re(Z_{in})$ and a significant increase in $Im(Z_{in})$ (Figs. 2.13(b). In practical layouts, the slotline sections interfacing the differential input

and the output termination are typically longer. As depicted in Figs. 2.13(c), such increased length helps align both the real and imaginary parts of Z_{in} more closely with Z_S, and also reduces its deviation over the frequency. An electrical length θ_{st4} in the range of 25°–35° offers a good compromise, as illustrated in Figs. 2.13(d). These results confirm that, through careful selection of transmission line parameters, Z_{in} can be effectively matched to the desired source impedance Z_S across a relatively large bandwidth. This S-parameter-based even-odd mode analysis assumes a single-port excitation at a time and for the condition that all four input ports inject equal in-phase power, only the odd-even mode is excited, and $S_{11} = \Gamma_{oe}$.

2.4 Circuit Implementation

To increase the gain offered by the EPCRC PA stage, two driver amplifier (DA) stages are inserted preceding the final PA stage. These driver amplifiers use differential stages, and the inter-stage matching between them is designed with transformers to leverage the wideband performance.

2.4.1 DA and PA Stages Design

To increase the gain of DA stages, the gain boosting techniques as discussed in Section 2.2.3, where the gate of the cascode transistor is coupled with its source, are adopted in these stages as well. The complete schematic of the two-stage DA is shown in Fig. 2.14(a). In this design, to accurately account for the loss of transmission line (TL), sections with a loss of 1.68 dB/mm at 120 GHz are utilized. The small-signal gain, S_{21}, of the driver stages is shown in Fig. 2.14(b). The peak gain for the two stages is 14.8 dB.

Following the methodology in Section 2.2, the EPCRC PA stage is implemented; the corresponding schematic is shown in Fig. 2.15(a). Owing to proximity and routing restrictions among transmission lines and inductors due to DRC rules, the effective values of the passive elements slightly deviate from their nominal schematic targets. To mitigate this, all reactive

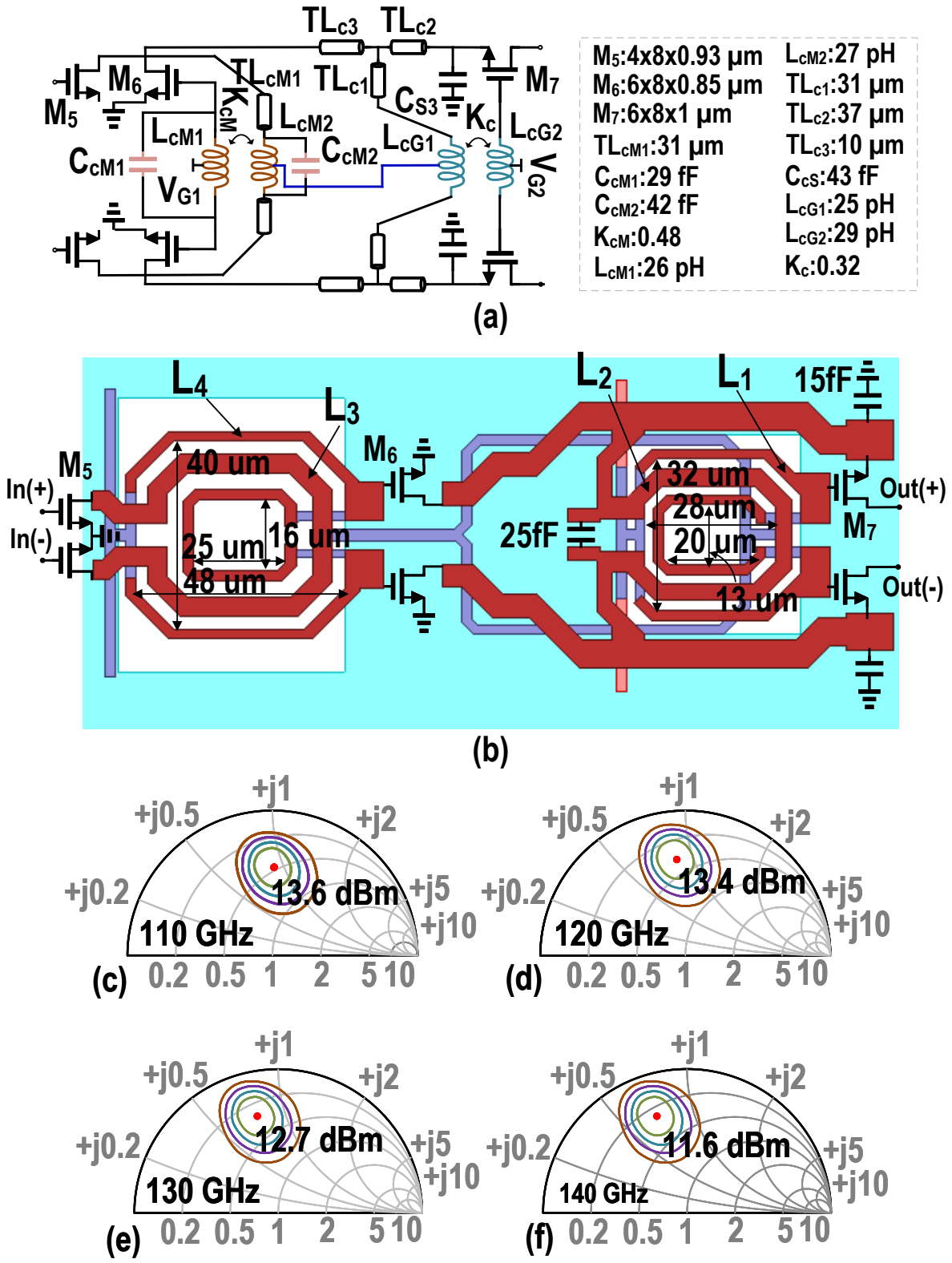

Figure 2.15: (a) Schematic for the EPCRC PA stage, and (b) layout; load-pull contours at (c) 110 GHz, (d) 120 GHz, (e) 130 GHz, and (f) 140 GHz.

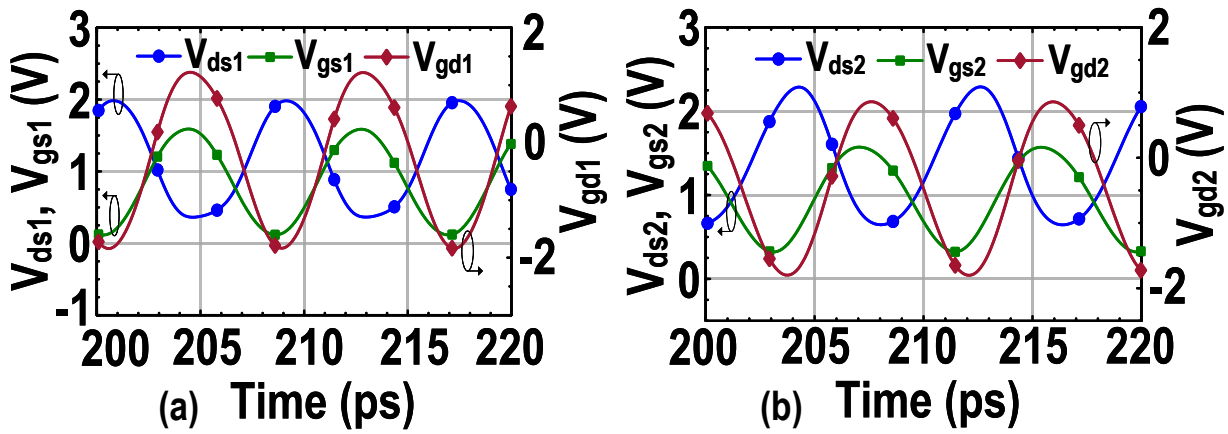

Figure 2.16: (a) Simulated transient waveforms V_{ds}, V_{gs}, and V_{gd} for the CS transistor M_6; (b) corresponding waveforms for the CG transistor M_7.

components are refined using an EM-driven co-simulation. This procedure is intended to better capture the distributed loss, parasitic coupling, and current redistribution. The finalized layout is presented in Fig. 2.15(b). The coupled inductors L_{cM1} and L_{cM2} are realized as two parallel, larger-diameter loops to obtain the required small inductance while ensuring adequate mutual coupling. A single small-diameter loop provides too little coupling at low inductance; the parallel-loop topology enlarges the effective overlap area and introduces dual coupling paths, thus meeting the target coupling. During EM extraction, the capacitors C_{cM1} and C_{cM2} are absorbed into the transformer representation, simplifying the layout. Similarly, the inductor L_{cG1} employs a single turn, whereas L_{cG2} uses two parallel turns. The finalized shunt capacitance is $C_{\mathrm{cS}} = 15\,\mathrm{fF}$, and an additional 25 fF is placed along L_{cG1} to bring the impedance matching conditions for the EM-extracted layouts closer to the schematic.

The Load-pull (LP) simulations are conducted across frequency to determine the optimum load impedance for maximizing output power. The LP contours at 110, 120, 130, and 140 GHz are illustrated in Fig. 2.15(c)–(f). From the LP results, output power levels between 13.6 dBm and 11.6 dBm are achievable across 110-140 GHz. Moreover, the LP contours indicate that the optimum load impedance at the PA drain varies between 23.5 Ω to 13.2 Ω (real part) and 45.2 Ω to 35.1 Ω (imaginary part) from 110 to 140 GHz. It is noteworthy

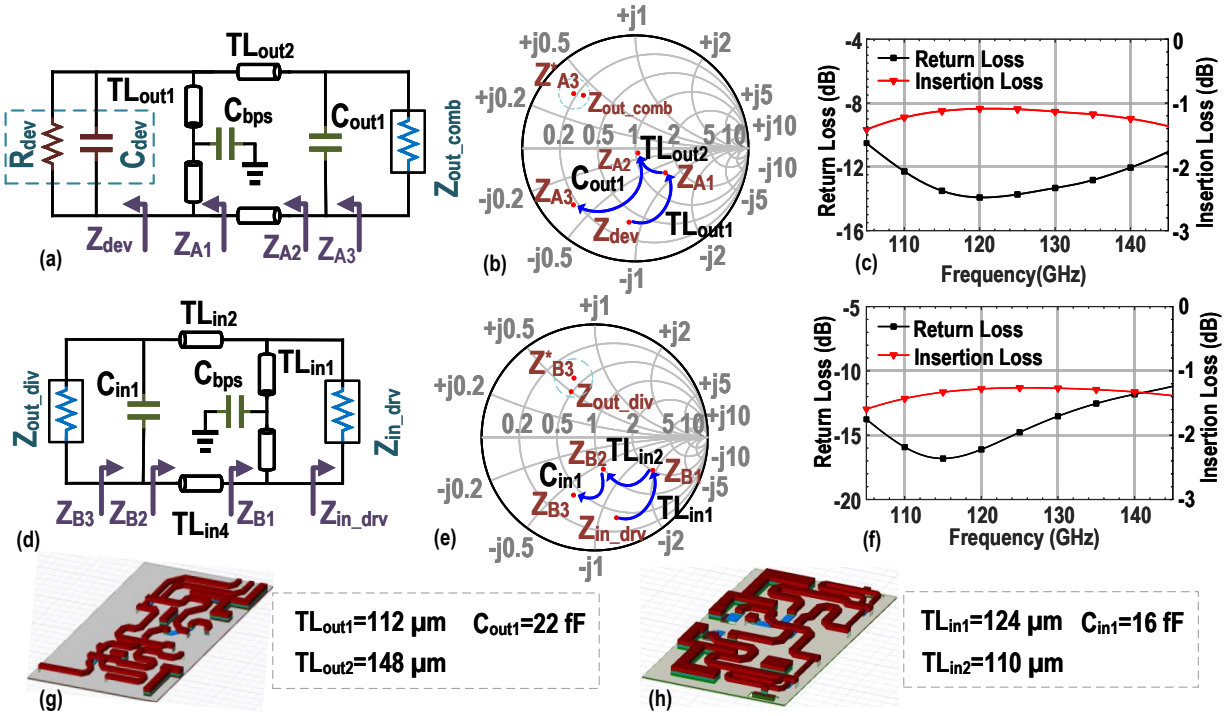

Figure 2.17: (a) PA to DCDPC routing lines, (b) matching trajectory, (c) return and insertion loss for DCDPC, (d) PA to DCDPD routing lines, (e) matching trajectory for DCDPD, (f) return and insertion loss for DCDPD, and layout for (g) DCDPC routing lines (half section), and (h) DCDPD routing lines.

that the Z_{opt} used in Section 2.2.3 (15+j45Ω) lies within the loadpull optimum impedance range.

The simulated transient waveforms of V_{ds}, V_{gs}, and V_{gd} for the CS transistor (M_6) and the CG transistor (M_7) are shown in Fig. 2.16(a)–(b). The peak-to-peak gate–drain swing of the CS device is approximately 3.04 V, which is near the nominal breakdown level [74].

2.4.2 Output and Input Routing Lines

In light of the loadpull discussions in the previous subsection, by approximating the drain impedance as a parallel RC network, the corresponding capacitance and resistance are 25.2 fF and 110.5 Ω at 110 GHz, and 28.37 fF and 106.5 Ω at 140 GHz, respectively. For preliminary matching, an average capacitance (C_{dev} = 26.75 fF) and resistance (R_{dev} = 109 Ω) are selected to model the output impedance Z_{dev}. Co-design of the combining lines and the

4-way DCDPC is essential to minimize loss and improve matching.

Fig. 2.17(a) shows the schematic of the output routing section, where Z_{dev} is an equivalent series resistance and reactance:

$$R_{\text{dev_seq}} = R_{\text{dev}} / \left(1 + (2\pi f R_{\text{dev}} C_{\text{dev}})^2\right),$$
$$X_{\text{dev_seq}} = 2\pi f C_{\text{dev}} R_{\text{dev}}^2 / \left(1 + (2\pi f R_{\text{dev}} C_{\text{dev}})^2\right)$$

The input impedance of the 4-Way DCDPC ($Z_{\text{out_comb}} = 12 + j20\ \Omega$) is matched to Z_{dev} through a shorted stub of 112 μm, resulting in Z_{A1} in the figure, a series TL of 148 μm (yielding Z_{A2}), and a shunt capacitor of 22 fF (giving Z_{A3}). The impedance transformation trajectory is illustrated in Fig. 2.17(b). EM simulations in Fig. 2.17(c) show a return loss better than 10.3 dB and an insertion loss between 1.1–1.24 dB.

For the input side, the driver stage exhibits minimal impedance variation with frequency. Therefore, a constant $Z_{\text{in_drv}} = 19.26 - j61.5\ \Omega$ is assumed. The input routing lines connecting the 4-Way dual-coupled differential power divider (DCDPD) to the driver stage are designed similarly. The schematic and impedance transformation are shown in Fig. 2.17(d)–(e), with $Z_{\text{out_div}} = 23 - j24.5\ \Omega$ representing the divider output impedance. EM results in Fig. 2.17(f) indicate a return loss below 11.8 dB and insertion loss between 1.26–1.32 dB. The half-circuit for the DCDPC and DCDPD are shown in Fig. 2.17(g) and (h), respectively.

2.4.3 Design of 4-Way DCDPC and DCDPD

The layout of the 4-way DCDPC is shown in Fig. 17(a), and the corresponding electric field distribution is clearly illustrated in Fig. 17(b). Following the detailed derivations provided in Section 2.3.2, a systematic procedure to design the 4-way DCDPC can be outlined as follows:

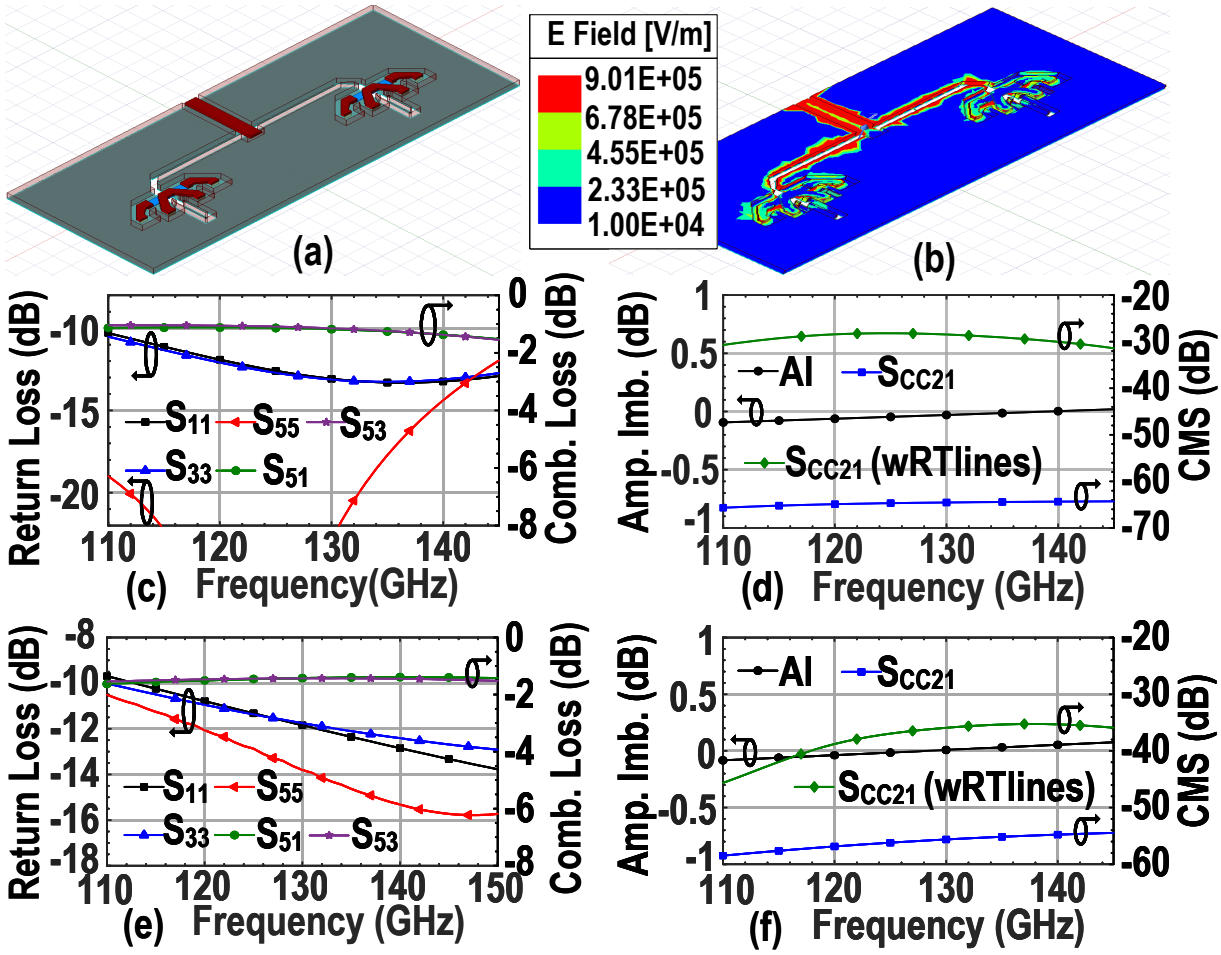

Figure 2.18: (a) Layout, (b) E-field pattern, (c) S-parameters and combining loss, and (d) AI and CMS of the DCDPC; (e) S-parameters and combining loss, and (f) AI and CMS of the DCDPD.

Step 1: Design the driver and PA stages and lay out the four parallel paths. Based on the minimum spacing permitted by the DRC rules, estimate the slotline length θ_{st1} in Fig. 2.12(a).

Step 2: Set initial turn ratios n_1 and n_2 for TF_1 and TF_2 between 0.9 and 1.0. To offset the excess series capacitance from the shorted stub, use $\theta_2 = 0°$–$5°$. Intermediate electrical lengths θ_1, θ_3, and θ_{st4} can be set between 10° and 15°. Although higher-impedance lines reduce loss, limits on current density and metal width must be considered; thus, select a characteristic impedance of 45–55 Ω.

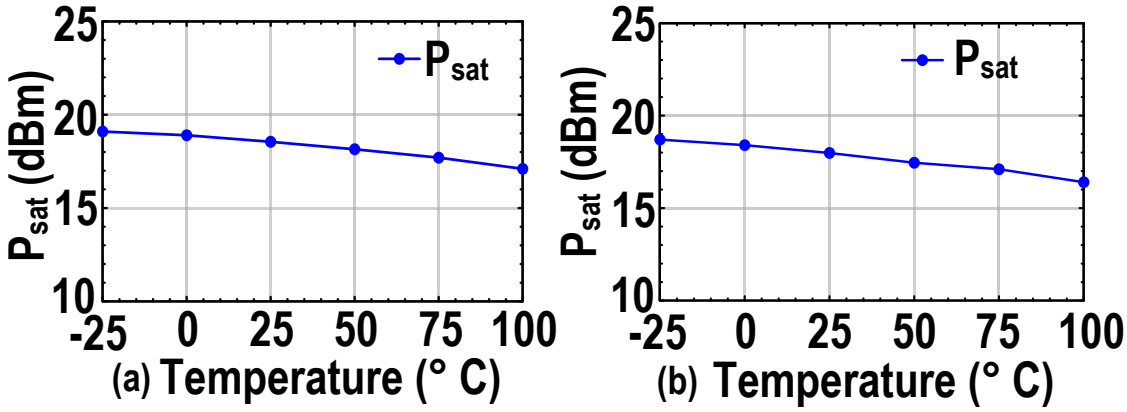

Figure 2.19: Saturated output power P_{sat} versus temperature at (a) 120 GHz and (b) 130 GHz.

Step 3: Using the initial parameters, calculate $Z_{BB'}$ from (2.17), and select a preliminary Z_S with a real part between 10–20 Ω and an imaginary part between 15–25 Ω.

Step 4: Decompose the circuit into four quadrants as shown in Fig. 2.12(e)–(h), and compute Z_{in} using (2.19) and (2.20).

Step 5: Adjust line lengths and characteristic impedances to align the real and imaginary parts of Z_{in} with those of Z_S, following the approach in Fig. 2.13. This optimization can be carried out using a numerical solver such as MATLAB.

Step 6: Once satisfactory matching between Z_{in} and Z_S is achieved, perform EM simulations to capture parasitic effects.

For a target $Z_{\text{out,comb}} = 12 + j20\ \Omega$, the EM results shown in Fig. 2.18(c) demonstrate a return loss better than 10.5 dB and insertion loss ranging from 1.13–1.37 dB. The amplitude imbalance is below 0.1 dB, and common-mode suppression (CMS) exceeds 64 dB as shown in Fig. 2.18(d). The CMS, when considering the routing line, reduces to below 28 dB as shown in Fig. 2.18(d).

Applying the same methodology, a 4-Way Dual-Coupled Differential Power Divider (DCDPD) is also designed. As shown in Fig. 2.18(e) and (f), the return loss is better than 11.1 dB,

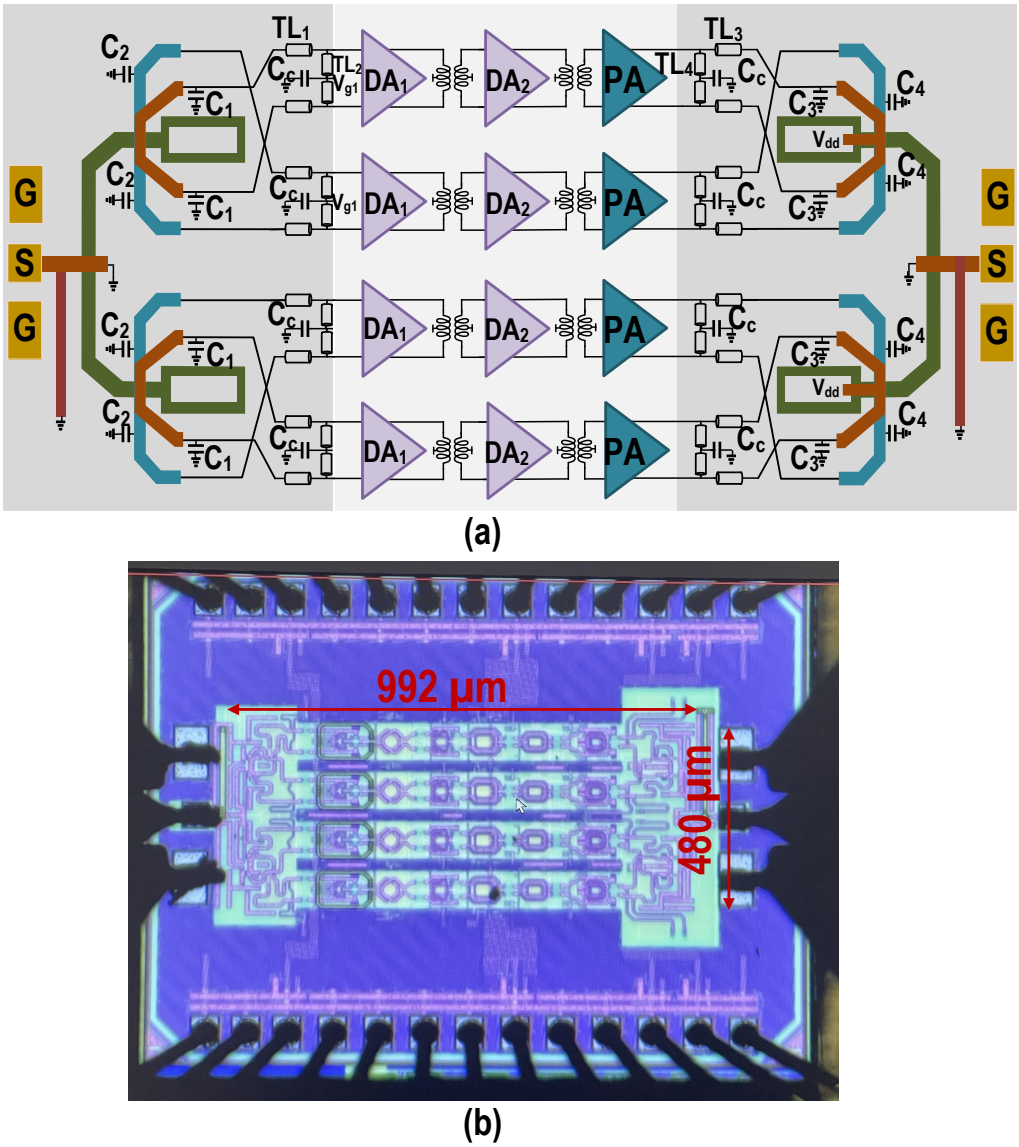

Figure 2.20: (a) Schematic of the proposed amplifier, (b) micrograph of the chip.

insertion loss ranges from 1.26–1.43 dB, amplitude imbalance remains below 0.13 dB, and CMS exceeds 54 dB. When taking the routing lines also into the account, the CMS reduces to below 35 dB as demonstrated in Fig. 2.18(f).

The temperature dependence of the saturated output power is plotted in Fig. 2.19(a) and (b) at 120 GHz and 130 GHz, respectively. As the temperature increases from −25°C to 100°C, P_{sat} decreases by about 2 dB at 120 GHz and 2.3 dB at 130 GHz.

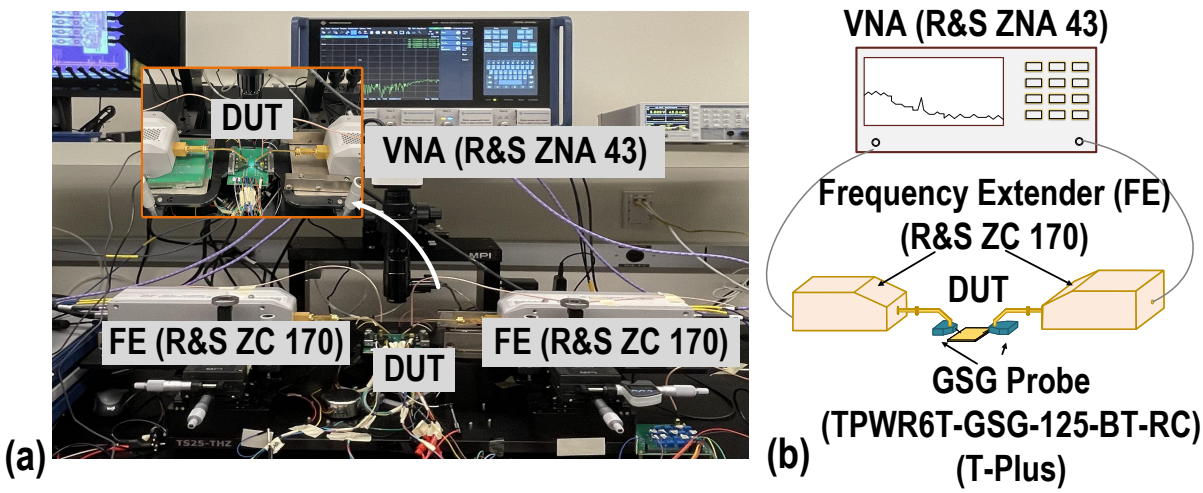

Figure 2.21: S-parameter and large signal CW (a) setup and (b) block diagram.

2.5 Measurement Results

The PA is fabricated in 65 nm CMOS process. The complete schematic of the designed PA is shown in Fig. 2.20(a). To compensate for the pad capacitance, parallel short-stubs with the pads are added. The chip micrograph is shown in Fig. 2.20(b), occupying a core area of 0.99 mm $\times$ 0.48 mm.

2.5.1 Small-signal Measurement Results

The small-signal measurement setup is shown in Fig. 2.21(a) with the corresponding block diagram in Fig. 2.21(b). A Rohde & Schwarz ZNA-43 vector network analyzer (VNA) drives and measures the PA through D-band frequency extenders (R&S ZC170), providing 110–170 GHz coverage. On-wafer S-parameters are acquired using 125-μm-pitch GSG probes (T-Plus). For calibration, a thru–reflect–line (TRL) procedure is performed on a vendor impedance standard substrate (ISS); the thru, short (reflect), and through line are used to place the reference plane at the probe tips. After TRL, we verify the calibration by measuring the ISS thru and 50-Ω load, and by repeating a loopback check using the through lines to confirm stability across the 110–170 GHz band.

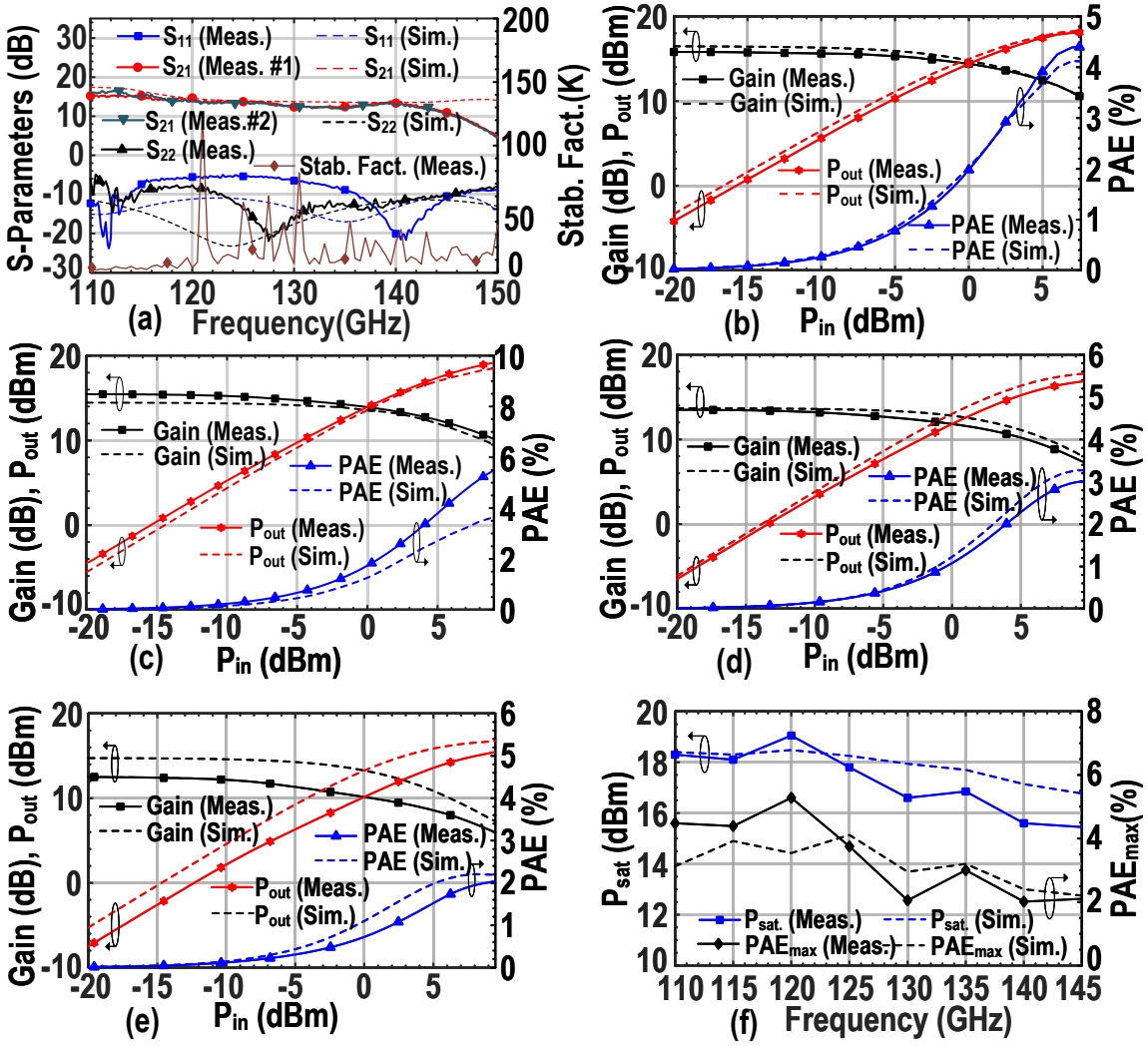

Figure 2.22: (a) Measured (solid lines) and simulated (dashed lines) S-parameters and measured stability factor. Measured (solid lines) and simulated (dashed lines) Gain vs. P_{in}, P_{out} vs. P_{in}, and PAE vs. P_{in} at (b) 115 GHz, (c) 120 GHz, (d) 135 GHz, and (e) 145 GHz. (f) P_{sat} and $PAE_{max.}$ versus frequency.

The measured small-signal S-parameters are presented in Fig. 2.22(a). Two chip samples with different placements of the supply decoupling capacitors on the PCB at a supply voltage of $V_{\text{DD}} = 2.6$ V are characterized. A peak gain of 14.9 dB is measured at 110 GHz, while some samples exhibit higher peak gain between 110 and 115 GHz. The best measured 3-dB bandwidth is 26.5 GHz. The stability factor, K, remains greater than unity across the frequency range. A slight frequency shift is observed between the measured and simulated small-signal responses, particularly toward the upper end of the band, likely caused by PDK

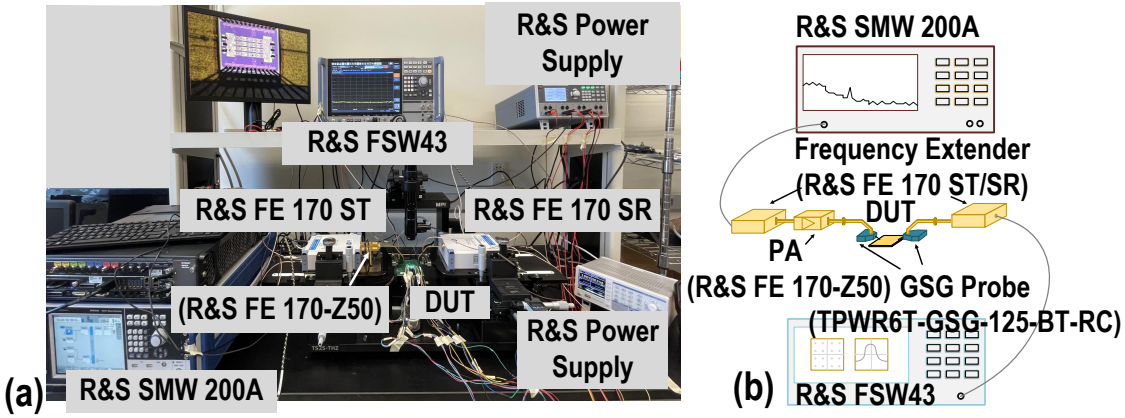

Figure 2.23: (a) Large-signal modulation signal setup and (b) block diagram.

modeling limitations. Furthermore, probe-to-probe coupling may become non-negligible at such high frequencies, as discussed in [75].

2.5.2 Large-signal Continuous-wave (CW) Measurement Results

For the large-signal measurements, we use the same setup as in Fig. 2.21(a). An additional power-calibration step is performed for CW tests. In particular, in addition to the probe-tip TRL calibration, an R&S NRP170TWG power sensor is used to calibrate the absolute power level at D-band. Following this calibration, a through line is measured to verify the delivered/received power and confirm the reference-plane consistency at the probe tips. The input power sweep measurements showing the large-signal power gain, output power, and power added efficiency (PAE) at 115 GHz, 120 GHz, 135 GHz and 145 GHz are demonstrated in Fig. 2.22(b), (c), (d) and (e), respectively. The maximum PAE of 5.3 % is achieved at 120 GHz. The measured output power is similar to the simulated ones at the lower end of frequencies but deviates a little as the frequency increases beyond 135 GHz. The measured saturated output power, and PAE_{max} versus frequency are shown in Fig. 2.22(f). It can be observed from this plot that a maximum saturated output power of 19 dBm is attained at 120 GHz. The 3-dBm saturated power bandwidth is $\geq$ 30 GHz.

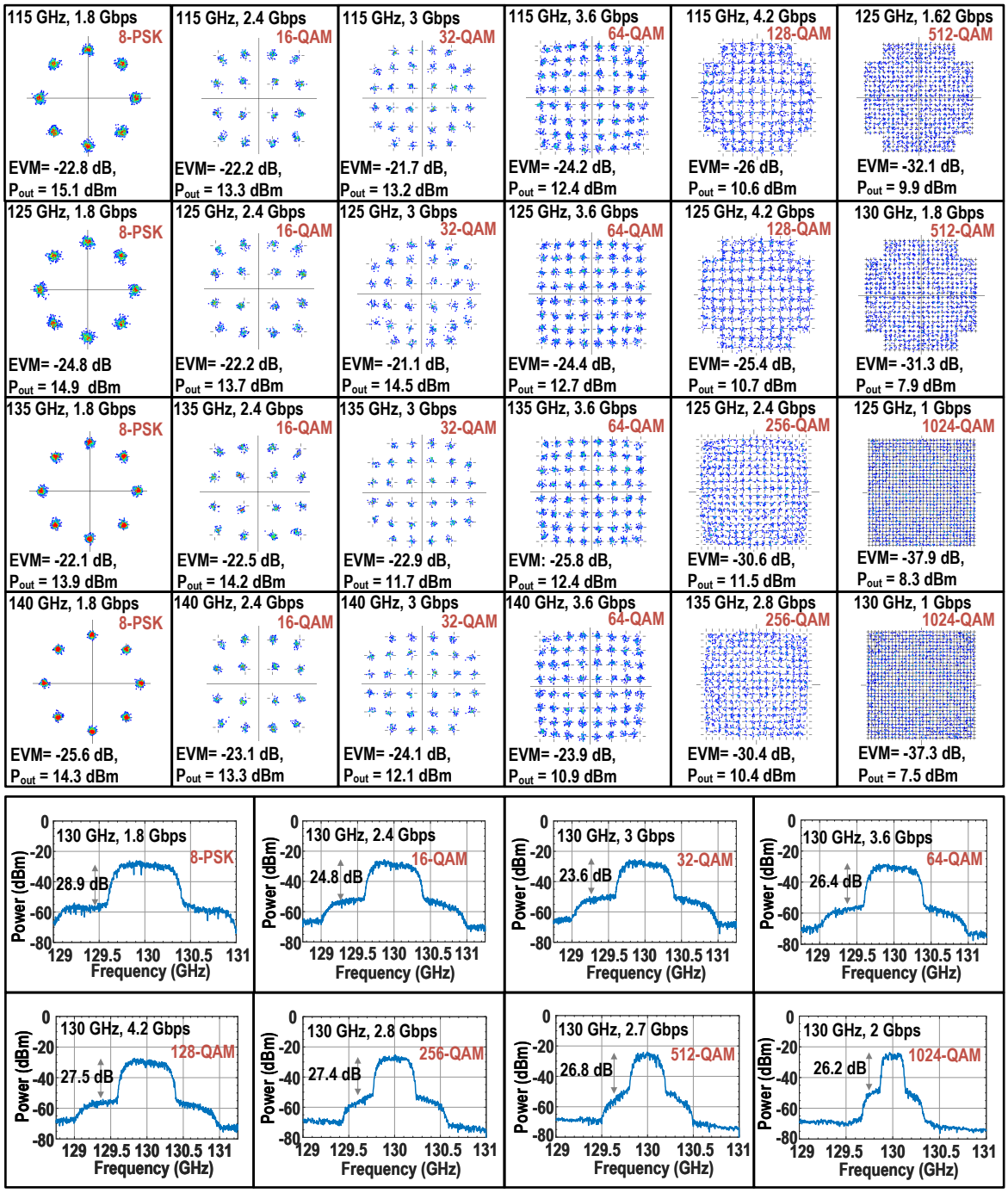

Figure 2.24: (Left) Measured constellation diagrams from 8-PSK through 1024-QAM at various frequencies, and (Right) the spectra corresponding to different orders of modulations at 130 GHz.

2.5.3 Large-signal Modulation Measurements

The fabricated PA is examined under various types of modulations in a separate test-bench as shown in Fig. 2.23. The modulation waveform generated by the R&S SMW 200A vector signal generator (VSG) is up-converted to the D-band frequency range using R&S FE170ST frequency extender and the waveguide probe on the input side excites the chip with the modulated waveform across a carrier frequency between 115-140 GHz. A power amplifier, R&S FE 170-Z50 is used to bring up the input power level to desired values after up-conversion, while the attenuation level is set by the frequency extender. Due to the high measurement frequencies, the equipment available to us was limited to a maximum modulation bandwidth of 600 MHz. On the output side, the amplified modulated waveform is down-converted by the R&S FE170SR frequency extender, which also controls the attenuation level. The down-converted signal is fed to the R&S FSW43 signal and frequency analyzer. The entire set-up is calibrated to measure the output power. The input signal is pulse shaped using root-raised cosine (RRC) filter with a roll-off factor of 0.35. The measurement is carried out without using any pre-distortion, and only the R&S internal equalization method is used. The vector signal analysis bandwidth of the FSW unit is limited to 2 GHz which can detect the modulated waveforms.

The PA performance under various amplitude modulations ranging from 16-quadrature amplitude modulation (QAM) (4 bits/symbol) to 1024-QAM (10 bits/symbol) is examined as shown in Fig. 2.24. The PA response to phase-shift keying modulations, i.e., 8-PSK constellation is also tested. The measurement results for various carrier frequencies, modulation orders, and data rates are shown in Fig. 2.24. A higher P_{sat} provides the output-power headroom required to run the PA several dB below saturation—sufficient to absorb the larger peak-to-average-power ratio (PAPR) of higher order QAMs—without clipping the signal peaks. Because the measured gain remains essentially flat up to the 1-dB compression point as shown in Fig. 2.22, the amplifier operates in a highly linear region at that backed-off power

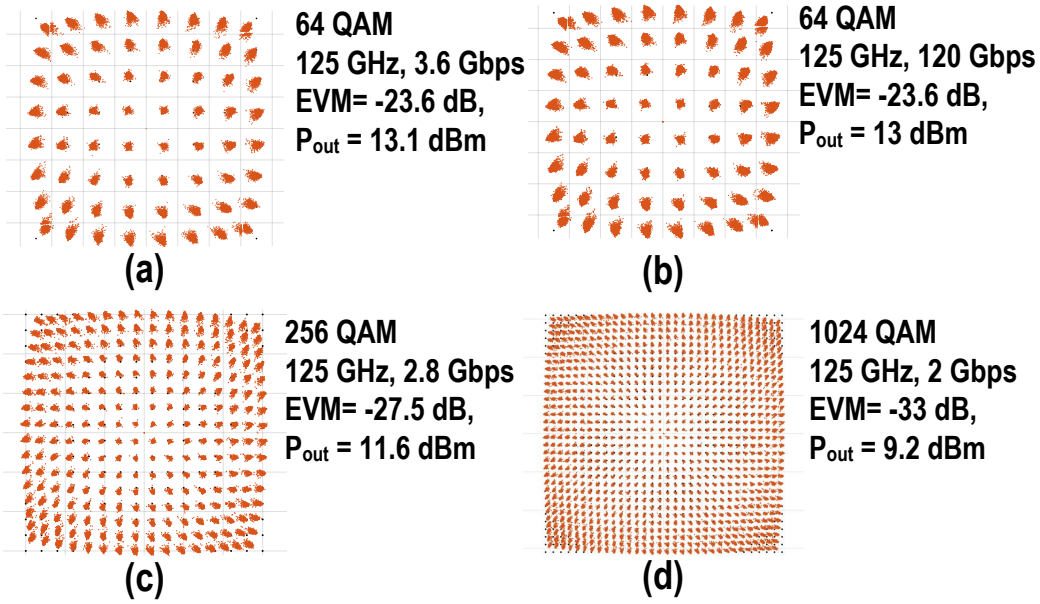

Figure 2.25: Simulated results for modulated signal (a) 3.6 Gbps 64-QAM, (b) 120 Gbps 64-QAM, (c) 2.8 Gbps 256-QAM, and (d) 2 Gbps 1024-QAM

level, keeping the resulting EVM within the stringent limits demanded by higher-order constellations. The output-power levels at which this PA sustains various modulation orders with low EVM are near or above 10 dBm which can be critical for wireless communication systems.

To evaluate the broadband performance, the amplifier is simulated in post-layout using various QAM modulation schemes, as shown in Fig. 2.25. A root-raised-cosine (RRC) filter with a roll-off factor of 0.35 is applied for pulse shaping. QAM schemes ranging from 64-QAM to 1024-QAM are evaluated at data rates of up to 120 Gb/s, as summarized in Fig. 2.25. In particular, 64-QAM operation at 120,Gb/s is demonstrated in Fig. 2.25(b), achieving an EVM of -23.6 dB.

2.5.4 Comparison with Prior Art

A comparison table with state-of-the arts PAs is shown in Table II. When comparing with the same process technology, the proposed design stands out in terms of output power with a decent small-signal 3-dB bandwidth, and attains the highest gain when compared with

the three-stage PAs. To compare the PA performance with the state of the art PAs, various figures of merit (FoM) are deployed. The first FoM is defined as [37],

$$\begin{aligned}\mathrm{FoM}_A = P_{\mathrm{sat}}\,(\mathrm{dBm}) + G\,(\mathrm{dB})/N + 10\log_{10}(\mathrm{PAE}\,\%)\\ + 20\log_{10}(\mathrm{Freq}/f_{\max}) + 10\log_{10}(\mathrm{BW}/\mathrm{Freq})\end{aligned} \tag{2.27}$$

Here, P_{sat}, G, N, $Freq$, and BW represent the saturated output power, small-signal power gain, number of amplifier stages, center frequency, and 3-dB bandwidth of the gain, respectively.

Since passive components implemented in bulk CMOS are generally more lossy compared to advanced processes such as CMOS SOI, an additional figure of merit, FoM_B, is proposed as

$$\mathrm{FoM}_B = P_{\mathrm{sat}} \cdot G^{1/N} \cdot (Freq/f_{\max})^2 \cdot (\mathrm{BW}/Freq) \tag{2.28}$$

The various FoMs are summarized in Table 2.2. While some recent designs in advanced SiGe and 22-nm SOI technologies achieve higher values in certain FoMs, the proposed PA, implemented in 65-nm CMOS technology, remains competitive with the state of the art across the three FoMs, demonstrating the effectiveness of the proposed design approach.

2.6 Conclusion

This chapter presents a three-stage wideband power amplifier (PA) implemented in a 65-nm CMOS process, featuring enhanced output power performance. A power-boosted current re-use cascode stage is introduced, which simultaneously improves both output power and gain. To further enhance the output capability, a wideband slotline-based dual-coupled 4-way differential power combiner/divider is employed. The fabricated PA achieves a measured

Table 2.2: Performance Comparison With State-of-the-Art Power Amplifiers

Ref.	**Process**	**Freq.** (GHz)	$f_{\max}$ (GHz)	P_{sat} (dBm)	$OP_{1\text{dB}}$ (dBm)	**Gain** (dB)	**PAE** (%)	$BW_{3\text{dB}}$ (GHz)	**Stages**	FoM_A	FoM_B
This Work	**65nm CMOS**	**126.4**	**280**	**19**	**13.7**	**14.9**	**5.3**	**26.5**	**3**	**17.52**	**10.65**
[49]	65nm CMOS	140	280*	13.2	9.9	15	14.6	30	4	15.88	2.65
[76]	45nm CMOS SOI	152.5	350*	8.8	5	18	6.8	17.5	4	5.01	0.47
[77]	40nm CMOS	140	350*	14.8	10.7	20.3	8.9	17	3	13.94	2.79
[65]	65nm CMOS	109	280*	12.9	9.6	12.2	8.2	16	3	9.58	1.11
[78]	65nm CMOS	93.5	280*	14	12	18	4.5	33	6	9.48	1.97
[79]	40nm CMOS	120	280*	14.6	9.3	16	9.4	38.5	3	17.37	5.80
[80]	130nm SiGe	152.5	450	8	6	17	1.6	35	3	-0.08	0.61
[81]	65nm CMOS	144	280*	5.7	5	20.6	3.6	33	3	5.96	1.09
[82]	45nm CMOS SOI	139	250	13.2	NA	14.9	2.8	19	4	7.66	2.08
[83]	40nm CMOS SOI	135	350	18.5	13.5	24.8	11	15	4	17.30	4.88
[84]	28nm CMOS	144.5	350*	13	9.1#	15	4.2#	30*	4	8.47	1.67
[85]	22nm FDSOI	140.5	350*	14.6	11.4	16	10.6	21	4	12.67	1.74
[86]	45nm CMOS SOI	133	350*	19.2	13.8	32.1	12.2	5	3	18.11	5.31
[87]	22nm FDSOI	135	350*	10.3	9.6	14.2	7.9	20	3	7.44	0.70
[88]	65nm CMOS	140	280*	10.7	7.2	27.3	6.4	10	5	6.74	0.74
[56]	90nm SiGe	127.5	350	21.9	18.6	18.2	12.5	35	2	27.58	45.86
[89]	130nm SiGe	121	450	22.7	NA	21.8	18.7	28	2	28.55	38.33
[90]	55nm SiGe	135	370*	19.7	19.2	22.5	12.1	37	4	21.77	12.43
[91]	22nm FDSOI	130	368	17.5	NA	13.5	16.5	38	3	19.8	5.78
[92]	22nm FDSOI	117.5	368*	18.6	NA	12	21.6	15	2	19.09	3.75
[93]	40nm CMOS	122	360	20.9	17.6	21.3	7.6	14	4	16.23	5.53

*Estimated, #Simulated results

peak saturated output power (P_{sat}) of 19 dBm and a peak small-signal gain of 15.3 dB over the 110–142.8 GHz frequency range. The design methodology and the proposed PA are deemed useful for high-resolution radar and broadband communication systems beyond 100 GHz.

Chapter 3

Wideband Stacked-Patch Antennas on a Flexible Printed Circuit for Sub-Terahertz 6G Applications

3.1 Introduction

The rapid growth in the field of cellular mobile communication has led to many breakthrough research achievements in the last decade, especially the development of high-data-rate communication links with impressive data rates of more than 10 Gbps (up to 100 GHz [94]) for wireless transceiver systems [95–97]. Fueled by this incredible growth, efforts are now being made to extend cellular mobile communication to emerging data-intensive applications, such as extended reality (XR), driverless vehicles, enhanced mobile broadband plus (eMBB-Plus), and Big Communication (BigCom)[98–100]. To cater to high data rate requirements for these services, the state-of-the-art proposes to raise the operation frequency towards the higher end of mm-wave frequency range (above 100 GHz), where licensed bands are very sparse and more bandwidth is thus available. The WR-08 band (90-140 GHz) will satisfy the bandwidth

requirement for 6G communication systems and is designated as the target frequency range in this work. A transceiver capable of establishing broadband wireless connectivity in the WR-08 band essentially requires a wideband antenna.

Owing to their lightweight, low cost, low profile, and conformal characteristics, microstrip-based antennas are the most favorable choice, which have been widely investigated for lower frequencies both in printed circuit board (PCB) and low-temperature co-fired ceramic (LTCC) technologies [101–104]. However, PCB antennas provide lower bandwidth[105, 106] in their basic form and many alternative structures have been reported to broaden the bandwidth. Among those, E-shaped patch [107–111], L-probe feed [112–116], Cavity backed slot [117–121], and magnetoelectric dipole (ME) [122–125] structures are popular. However, only few reported works exist in the WR-08 band[126–133]. Moreover, majority of reported antennas in the WR-08 band are on chip with poor gain and radiation efficiency. Only recently, one work has implemented a PCB antenna for this frequency range [133].

In a basic patch antenna, the feedline is on the same plane as the patch, which causes the weaker radiation from the feedline to interfere with the radiation from the patch. To overcome this issue, an alternate solution was conceived by [134], in which the feedline is placed on the other side of the ground layer, while the patch is coupled to it electromagnetically through a small slot in the ground plane[134–143]. Since a patch element excites a fundamental mode resonance, stacking more patch elements to construct an ACSP will create closely separated resonances, leading to broadband performance. The ACSPs have been investigated at lower frequencies [144–148]. In [148], the authors proposed an ACSP antenna on thick substrates of Duroid and Foam with low dielectric constants of 2.2, and 1.07, respectively, and a low loss tangent of 0.0009 for both substrates. The antenna achieves a state-of-the-art bandwidth of around 69% at a center frequency of 7.7 GHz, which is one of the highest values of bandwidth reported for ACSP antennas. In order to study the feasibility of this antenna, the scaled/optimized version of this design is simulated at WR-08

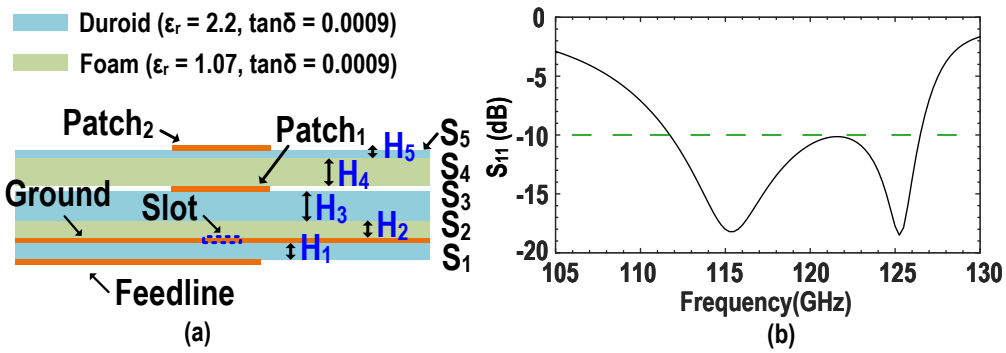

Figure 3.1: (a) side view of the scaled version of [148] for FPC substrate, and plot for simulated (b) S_{11}.

band using the deployed FPC substrate in this work, as shown in Fig. 3.1(a). Although, a low dielectric constant is favorable to achieve better bandwidth performance, the S_{11} plot in Fig. 3.1(b) shows that this antenna only achieves 12.34% bandwidth from 111.77 GHz to 126.47 GHz, which is not sufficient to satisfy the target data-rate requirements for 6G communication.

In a conventional ACSP antenna, the bottom feedline will radiate from the backside and will thus impact the broadside radiation. To achieve 100+ Gbps, as anticipated by 6G wireless, in a transceiver employing 64-QAM modulation, for example [149], more than 30% of fractional bandwidth across the WR-08 frequency band is required. Since in WR-08 band the intrinsic gain of the device is relatively low, the generated output power by the power amplifier (PA) inside a transmitter can be very low. To increase the power level, parallel PA cell combining technique, incorporating multiple PAs, might be preferred [50], which requires a *single-ended* antenna.

The design of a broadband ACSP antenna, in the absence of any analytical formulation or with non-availability of initial design values, is largely based on tuning various dimensions which is very time- consuming. This further gets aggravated due to increased sensitivity of the parameters in the WR-08 band as a result of reduced wavelength. Since, the antenna in the WR-08 band is highly miniaturized in dimension, an on-probe 50 Ω G-S-G input port

needs to be added for the measurability of the performance. Therefore, vias need to be added to connect the 50 Ω G-S-G input port with the feedline. As the power generated by the active devices in the WR-08 band is already very low, losses in the via transition is very critical, and must be minimized for an efficient system-level integration of the antenna. Therefore, to overcome these challenges, a wideband ACSP antenna is proposed at the WR-08 band which exhibits the following features:

1. A two-section dual-band matching technique based on an analytical methodology is proposed to design a wideband impedance matching distributed network that matches the 50 Ω input port impedance to the complex slot impedance. This technique also provides three different solution regions corresponding to better impedance matching, poor impedance matching, and a region of non-feasible design parameters. To the best of our knowledge, this is the first PCB antenna above 100 GHz that is designed based on this systematic impedance matching.

2. A design technique to match the slot impedance trajectory to the patch impedance trajectory based on constant VSWR circles is proposed that achieves a broadband impedance matching between the slot and the patch.

3. Proposing a technique that provides a transition from a 50 Ω G-S-G port to a 50 Ω feedline with low insertion loss, low return loss, and broadband performance from 85 GHz to 135 GHz.

4. A discussion section explaining the parallel plate mode generation, and introducing the techniques for their suppression.

In Section 3.2, we propose an analytical design approach to choose the various components of the broadband ACSP antenna and explain how the ground via configuration can suppress the excitation of unwanted modes. We also discuss the antenna simulation results in Section 3.2 and explain how a uniform broadside radiation pattern with small cross-polarization is

achieved. The measurement results and their comparison with simulations are included in Section 3.3. In Section 3.4, the design is extended into a cavity-backed structure that suppresses the surface waves launched by the radiating patches and further widens the measured bandwidth to 91.5–134 GHz. The chapter is concluded in Section 3.5.

3.2 Analysis and Design of Antenna

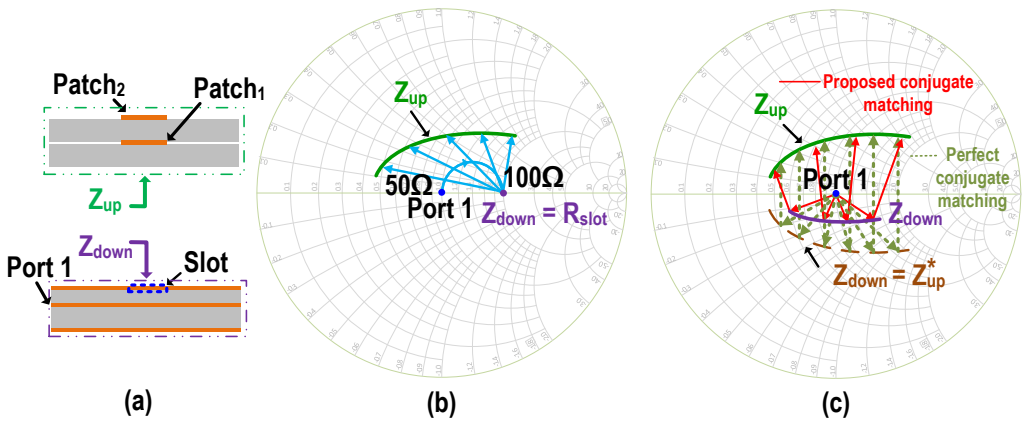

Figure 3.2: (a) ACSP antenna partitioned into two separate structures, (b) conventional matching technique, and (c) proposed broadband matching technique.

Fig. 3.2(a) shows the ACSP antenna partitioned into two separate structures, where the lower structure constitutes the feedline and slot, and the upper structure consists of patches. Impedance looking up from below the patch structure is Z_{up} and the impedance looking down the slot is Z_{down}. In a conventional ACSP antenna, the input 50 Ω port is matched to the slot by assuming a fixed resistive slot impedance, $Z_{down} = R_{slot}$, e.g., $R_{slot} = 100\ \Omega$ in [148]. Subsequently, the R_{slot} is matched to the complex impedance of the patch, which varies substantially across a large frequency bandwidth as shown in Fig. 3.2(b). However, the impedance on the slot end is complex-valued in nature, resulting in limited bandwidth when matching a 50 Ω input port to R_{slot}. For a perfect matching, the impedance Z_{down} needs to be complex conjugate of the Z_{up} that is $Z_{down} = Z^*_{up}$ as illustrated in Fig. 3.2(c). To realize a broadband ACSP antenna with sufficient return loss (e.g., $S_{11} \leq -10$ dB), the value of Z_{down} must be a frequency-dependent complex impedance that follows a similar

trajectory as Z_{up}. Fig. 3.2(c) shows the proposed idea of impedance matching, where the 50 Ω input port is matched to a frequency-dependent complex impedance, Z_{down}.

3.2.1 Proposed broadband TWBDN based on dual-band matching technique

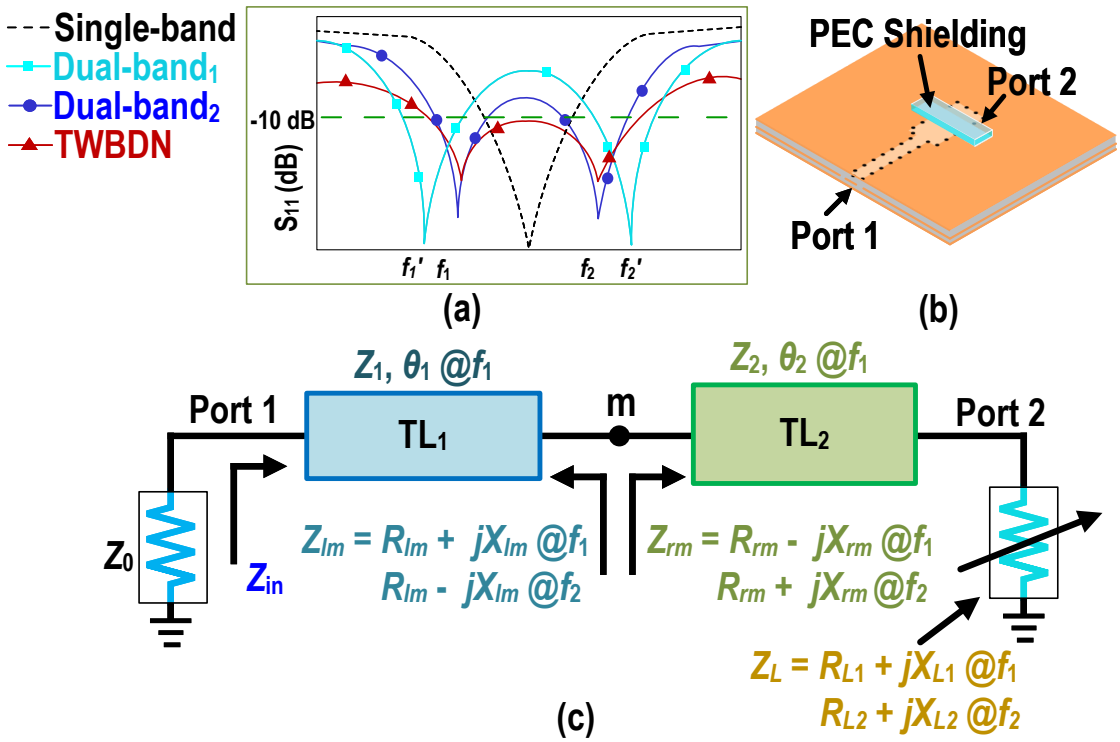

Figure 3.3: (a) Return loss profiles for single-band, dual-band, and TWBDN; (b) structure representing TWBDN, and (c) schematic of the TWBDN.

As mentioned previously, the conventional design of ACSPs relies on software optimizations and fails to lead to broadband performance at higher frequencies. To overcome these issues, an accurate systematic design approach should be adopted for the sub-terahertz antenna design so that the sensitivity to parametric variations is minimized. To save the simulation time, the adopted design approach should also provide the initial design values to start with minimal reliance on iterative parametric simulations. At lower frequencies, many RLC circuit-based equivalent circuits for the ACSP antenna have been proposed [150, 151]. These circuits simplify the understanding of antenna, but do not offer any evaluation of antenna

parameters (a model of ACSP is presented in Appendix I). A two-port distributed network theory that can explain the transmission of signal from the input port to the slot will be necessary to closely match with the actual antenna design, which lumped RLC circuit models do not offer.

In the proposed design, a two-section transmission line theory is employed to achieve a broadband impedance matching between a 50 Ω input source impedance and a frequency-dependent complex-valued slot impedance. To achieve this goal, first a two-section dual-band impedance matching network with lower and upper bands within the desired radiation bandwidth, located at f_1 and f_2, is designed. Next, a two-section wideband distributed network (TWBDN) is designed to attain broadband performance by reducing the frequency ratio, $r = f_2/f_1$, and relaxing the impedance matching according to Bode-Fano criterion [152–156]. Fig. 3.3(a) illustrates the comparison of return loss profiles of conventional single-band, dual-band (Dual-band$_1$), dual-band with reduced r (Dual-band$_2$), and TWBDN. It can be observed that with TWBDN, a much wider impedance matching bandwidth (more than 250% improvement) can be achieved compared to conventional single-band design. Fig. 3.3(b) demonstrates the structure designed in HFSS representing the signal propagation from input port through TWBDN to the slot aperture. Here, the input port, Port 1, is excited as a wave-port source, and another wave-port, Port 2, which acts as a terminating impedance is mounted on top of the slot. Port 2 is shielded by a perfect electrical conductor (PEC) material to provide separation from the radiation boundary. Fig. 3.3(c) shows the schematic of the proposed TWBDN, where TL$_1$ and TL$_2$ represent two sections of the feedline transmission line (TL), and Z_L is the general complex load impedance representing the impedance looking up towards the slot from the feedline. It should be noted that the value of Z_L in this formulation includes the coupling between the slot and feedline, which allows to later use it for the complete design of antenna in Section 3.2.3. The characteristic impedance and electrical lengths of TL$_1$ and TL$_2$ are Z_1, θ_1 and Z_2, θ_2, respectively, and Z_L obtains two values of $Z_{L1} = R_{L1} + jX_{L1}$ at f_1 and $Z_{L2} = R_{L2} + jX_{L2}$ at f_2, respectively.

The impedance looking right of the node m in Fig. 3.3(c) is,

$$Z_{rm} = Z_2 \frac{Z_L + jZ_2 \tan\theta_2}{Z_2 + jZ_L \tan\theta_2}. \tag{3.1}$$

Similarly, the impedance looking left of the node m is,

$$Z_{lm} = Z_1 \frac{Z_0 + jZ_1 \tan\theta_1}{Z_1 + jZ_0 \tan\theta_1}. \tag{3.2}$$

For dual-band impedance matching, TL_1, and TL_2 are chosen such that the impedances Z_{rm} and Z_{lm} are complex conjugate at both f_1 and f_2, that is,

$$Z_{rm} = R_{rm} \mp X_{rm},$$
$$Z_{lm} = R_{lm} \pm X_{lm}.$$

For impedance matching at node m, the real and imaginary part of the Z_{rm} and Z_{lm} become,

$$R_{rm} = R_{lm}, \tag{3.3}$$
$$X_{rm} = X_{lm}. \tag{3.4}$$

If the terminating impedance, Z_L, is known at f_1 and f_2, then Z_2 and θ_2 can be evaluated as [157–159],

$$Z_2 = \sqrt{R_{L1}R_{L2} + X_{L1}X_{L2} + \frac{(X_{L1} + X_{L2})(R_{L1}X_{L2} - R_{L2}X_{L1})}{R_{L2} - R_{L1}}} \tag{3.5}$$

$$\theta_2 = \frac{k\pi + \arctan\left(\dfrac{Z_2(R_{L1} - R_{L2})}{R_{L1}X_{L2} - R_{L2}X_{L1}}\right)}{r+1}, \qquad k \in \mathbb{N}. \tag{3.6}$$

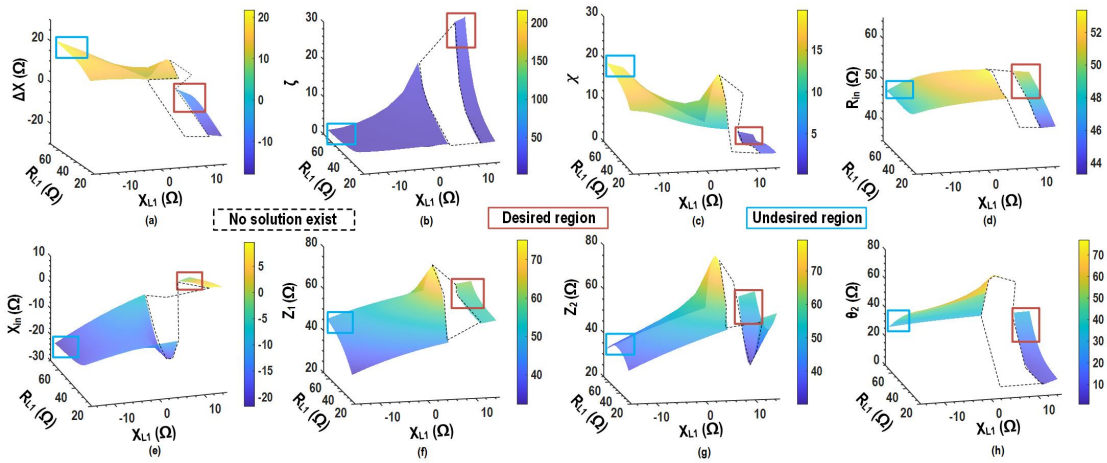

Figure 3.4: Surface plot for (a) ΔX, (b) ζ, (c) χ, (d) R_{in}, (e) X_{in}, (f) Z_1, (g) Z_2, and (h) θ_2 for variations in R_{L1} and X_{L1}.

Upon substituting Z_2 and θ_2 from (3.5) and (3.6) in (3.1), R_{rm} and X_{rm} can be evaluated as,

$$R_{rm} = \mathfrak{Re}[Z_{rm}] = \frac{R_{L1} Z_2^2 \left(1 + \tan^2 \theta_2\right)}{Z_2^2 - 2 Z_2 X_{L1} \tan \theta_2 + \left(R_{L1}^2 + X_{L1}^2\right) \tan^2 \theta_2}, \tag{3.7}$$

$$X_{rm} = \mathfrak{Im}[Z_{rm}] = \frac{Z_2 \left(Z_2^2 - R_{L1}^2 - X_{L1}^2\right) \tan \theta_2 + Z_2^2 X_{L1} \left(1 - \tan^2 \theta_2\right)}{Z_2^2 - 2 Z_2 X_{L1} \tan \theta_2 + \left(R_{L1}^2 + X_{L1}^2\right) \tan^2 \theta_2}. \tag{3.8}$$

The 50 Ω Port 1 impedance is transformed into a complex conjugate impedance Z_{lm} through a transmission line of length,

$$\theta_1 = \frac{n\pi}{1 + r}. \qquad n \in \mathbb{N} \tag{3.9}$$

Substituting θ_1 into (3.2), R_{lm} and X_{lm} can be evaluated as,

$$R_{lm} = \mathfrak{Re}[Z_{lm}] = \frac{2 Z_0 Z_1^2}{Z_0^2 + Z1^2 + \left(Z_1^2 - Z_0^2\right) \cos 2\theta_1}, \tag{3.10}$$

$$X_{lm} = \mathfrak{Im}[Z_{lm}] = \frac{Z_1 (Z_1^2 - Z_0^2) \sin 2\theta_1}{Z_0^2 + Z_1^2 + \left(Z_1^2 - Z_0^2\right) \cos 2\theta_1}. \tag{3.11}$$

R_{rm} from (3.7) and R_{lm} from (3.10) are used to satisfy (3.3) and to evaluate the value of Z_1. So far, we have evaluated all four unknown parameters, namely Z_1, Z_2, θ_1, and θ_2,

which can be used to design a dual-band matching network. However, merely satisfying (3.3) does not necessarily mean that (3.4) is also satisfied; that is, proper imaginary component cancellation is still required at node m to further reduce the reflection coefficient S_{11}. To design dual-band matching for applications such as an amplifier, mixer, or other active circuits where the terminating impedance is fixed, an open or short dual-band stub should be added at node m [157]. This helps satisfy (3.4) by cancelling the excess imaginary part ($|\mathfrak{Im}[1/Z_{rm}] - \mathfrak{Im}[1/Z_{lm}]|$) left after satisfying (3.3). From a broadband impedance matching perspective, however, stub addition is not a suitable choice as it offers a narrowband excess imaginary component cancellation. For ACSP antenna, where the slot represents an intermediate node between input source and the output patch, it is possible to change Z_L by varying the slot and coupled patch dimensions. This added design feature facilitates meeting the required condition in (3.4) without the need of extra stub at node m.

For TWBDN design, the two bands are brought closer by reducing the frequency ratio (r), and introducing mismatches by loosely satisfying (3.3) or (3.4). In other words,

$$R_1 \leq [\Delta R = R_{rm} - R_{lm}] \leq R_2,$$
$$X_1 \leq [\Delta X = X_{rm} - X_{lm}] \leq X_2,$$

where R_1, R_2 and X_1, X_2 represent the boundaries of mismatches ΔR, and ΔX.

Since the input port is a real-valued 50 Ω impedance, we select for a broadband matching to fully satisfy only (3.3) ($\Delta R = 0$), and introduce the mismatches by leaving (3.4) to be unsatisfied ($\Delta X \neq 0$). A mismatch of few ohms in ΔX at node m improves the bandwidth, but along with it, impedance transformation $t = Z_0/R_{rm}$ in case $Z_0 > R_{rm}$ or $t = R_{rm}/Z_0$ when $R_{rm} > Z_0$, and $Q_r = X_{rm}/R_{rm}$ should also be considered. The value of t should be closer to one, and Q_r at node m should be low. Among the different feasible solutions

obtained for various Z_L, a quantity ζ is defined in terms of t and quality factor Q_r as,

$$\zeta = \sqrt{(t/Q_r)^2 - 1}.$$

A higher value of ζ is preferred for better bandwidth among different solutions obtained. This happens when R_{in} in Fig. 3.3(c) is closer to 50 Ω. However, if we also consider the $\mathfrak{Im}[Z_{in}]$, X_{in}, to be smaller for better matching performance, another parameter is defined as,

$$\chi = |Z_0 - R_{in}| - |X_{in}|. \tag{3.12}$$

A lower value of χ is desired for better impedance matching at Port 1. To demonstrate the

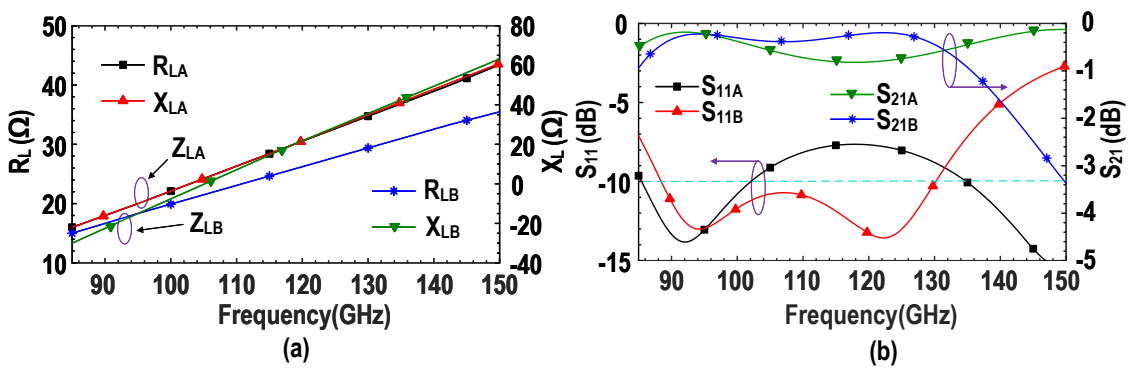

Figure 3.5: (a) Simulated profiles of two loads (Z_{LA} and Z_{LB}) for $r = 1.5$ and $f_1 = 95$ GHz, and $r = 1.25$ and $f_1 = 95$ GHz with real part and imaginary part R_{LA} and R_{LB} and X_{LA} and X_{LB}, respectively, and the corresponding (b) simulated S-parameters S_{11A}, S_{11B}, S_{21A}, and S_{21B}.

feasibility of the presented theory, an example is considered with $f_1 = 95$ GHz and $f_2 = 120$ GHz, which are both within the WR-08 band. The values of R_{L1} and X_{L1} are varied from 25 Ω to 65 Ω and -15 Ω to 15 Ω, respectively with a fixed $R_{L2} = 55$ Ω and $X_{L2} = 15$ Ω. The evaluated length of TL_1 is $\theta_1 = 79.53°$ (only dependent on r and calculated using (3.9)), and Figs. 3.4(a)-(h) show the surface plots for the rest of parameters, i.e., ΔX, ζ, χ, R_{in}, X_{in}, Z_1, Z_2, and θ_2 against the variations in R_{L1} and X_{L1}. The values corresponding

to desired regions are obtained when ΔX is small, ζ is large, and χ is small as denoted by red enclosed rectangles in Fig. 3.4. This can also be verified from the plots of R_{in} and X_{in} in Fig. 3.4(d) and Fig. 3.4(e), respectively, where R_{in} and X_{in} are deviated from 50 Ω and zero by 5-10 Ω, respectively. An undesired mismatched region is also indicated in Fig. 3.4 by blue enclosed rectangles, where the value ζ is very small and that of χ is very large. In this region, although R_{in} is only slightly lower than 50 Ω, the value of X_{in} is below -20 Ω which degrades the matching substantially. The solutions in this region should be avoided. From Fig. 3.4(a)-(h), it is clear that the solutions are realizable for a wide range of R_{L1} and X_{L1}. There are regions of R_{L1} and X_{L1} for which solutions do not exist, as covered by the dotted lines in Fig. 3.4(a)-(h). These regions correspond to non-physical values of impedances Z_1 and Z_2. It is noteworthy that the prediction of non-existing solutions is impossible with simulator-based optimizations. Based on the values of ζ, χ and ΔX in Fig. 3.4(a)-(c), the best initial design parameters corresponding to desired regions can be readily chosen to design a broadband TWBDN.

As another example to examine the effect of frequency ratio (r) on TWBDN, two extra cases are considered for $r = 1.5$ and $r = 1.25$ with $f_1 = 95$ GHz. Based on solutions obtained from the governing equations for Z_{L1} and Z_{L2}, the interpolated load profile from 85 GHz to 150 GHz is shown in Fig. 3.5(a). The real and imaginary parts for $r = 1.5$ are R_{LA} and X_{LA}, and for $r = 1.25$ are R_{LB} and X_{LB}. The corresponding return loss and insertion loss for the two cases of $r = 1.5$ and $r = 1.25$ are shown in Fig. 3.5(b) as $S_{11\mathrm{A}}$, $S_{11\mathrm{B}}$, and $S_{21\mathrm{A}}$, $S_{21\mathrm{B}}$, respectively. As it can be observed, a significant improvement is obtained in terms of bandwidth with a lower value of $r = 1.25$ compared to $r = 1.5$ while maintaining a low value of insertion loss.

The proposed design approach to design TWBDN provides analytical formulations to find initial design parameters for TL_1 and TL_2. From a pool of solutions for different values of Z_L, quantities ΔX, ζ, and χ should be utilized to find the initial values of parameters of

TL_1 and TL_2 that provide maximum bandwidth with a substantially low level of return loss. This way, the presented technique greatly simplifies the task to design a broadband matching network between a 50 Ω input port and a complex slot impedance. It is also noteworthy that the proposed distributed network theory does not capture secondary detrimental phenomena such as propagation of undesired parallel-plate modes in the substrate, and therefore these unwanted effects should be separately studied, as discussed in Section 3.2.4.

3.2.2 Proposed G-S-G port to feedline transition

In the proposed ACSP antenna, the feedline is located between two ground layers (bottom and slot layers). To connect with a 50 Ω input port, the conventional approach employed at lower frequencies suggests to add a CPW port at the top of the structure by using long vias to connect with the feedline and ground layer, as illustrated in Fig. 3.6(a). However, this technique is not suitable for mm-wave and sub-THz antennas. In a GCPW configuration with an added upper ground layer, the electric field is confined between the central conductor and side, bottom, and top ground layers. For a via based transition from the feedline to the top of the structure, the two ground vias, V_{g1} and V_{g2} in Fig. 3.6(a) represent only side ground conductors which is equivalent to a CPW line without ground layers. That is, in the absence of two (top and bottom) ground layers in the via transition, the field configuration is greatly altered, which makes an efficient and broadband transition difficult to achieve. In addition, in the target WR-08 band, in the absence of proper confinement of electric fields, the signal propagating through the via leaks into the substrate, which makes this via transition more lossy. The leakage phenomenon is discussed in more detail in section (3.2.4).

Aside from the different field configuration, the feedline width in WR-08 band is lower than minimum required pad dimension prescribed by the fabrication process. For example, with an $\epsilon_r = 3.1$, substrate height of 50 μm on both sides of the transmission line and a gap spacing of 50 μm from the ground conductors, the width of a 50 Ω line is less than 80 μm

while the minimum required diameter of via pad is 300 μm. This large difference in the width of TL, and the diameter of pad makes impedance matching a very complex task and will result in poor matching with a higher insertion loss. Moreover, for a fixed value of characteristic impedance, the line width increases with the substrate height. In a multi-layer configuration, if the input CPW port is designed at the top of the structure, it will require a wider TL. For measurement in the WR-08 band, the standard pitch size (center-to-center distance between the tips) of the probe tip are either 100 μm or 150 μm. With the same substrate, and the same gap spacing, the line width for a substrate height of 170 μm is greater than 180 μm. This leaves little room for the probe landing, and requires an additional matching section on the top layer. And finally, in a multi-layer configuration, for a case when fabrication technology does not support direct via placement from the top of the structure to the feedline layer, multiple via transitions are required between different layers. Multiple via fabrication is prone to sliding and shifting of the connected layers, which results in excess loss and degradation of performance.

Considering all the above-mentioned design challenges, for an effective transition in the WR-08 band, vertical via-based transition is avoided in the proposed antenna. Instead, a sub-THz-compliant design with a little modification in field pattern in the transition region is sought to achieve a smooth transition. The proposed G-S-G port transition is shown in Fig. 3.6(b). In this configuration, the GCPW line with top ground layer is converted to a simple GCPW by removing the top ground layer near the port. Fig. 3.6(c) shows the transition and associated capacitances and inductances. Since the characteristic impedance is defined as $Z = \sqrt{L/C}$, for a GCPW with top ground layer, total capacitance is $C = C_a + 2C_b + C_c$, where C_a, C_b, and C_c are the coupling capacitances between feedline and a) bottom ground layer, b) side ground layer, and c) top ground layer, respectively. In the GCPW, total capacitance is reduced by C_c in the absence of top ground layer, leading to a new impedance $Z' = \sqrt{L/(C - C_c)}$. To maintain the same line impedance, the line width is increased ($W \propto 1/Z'$) and is tapered to match to the the GCPW with top ground layer.

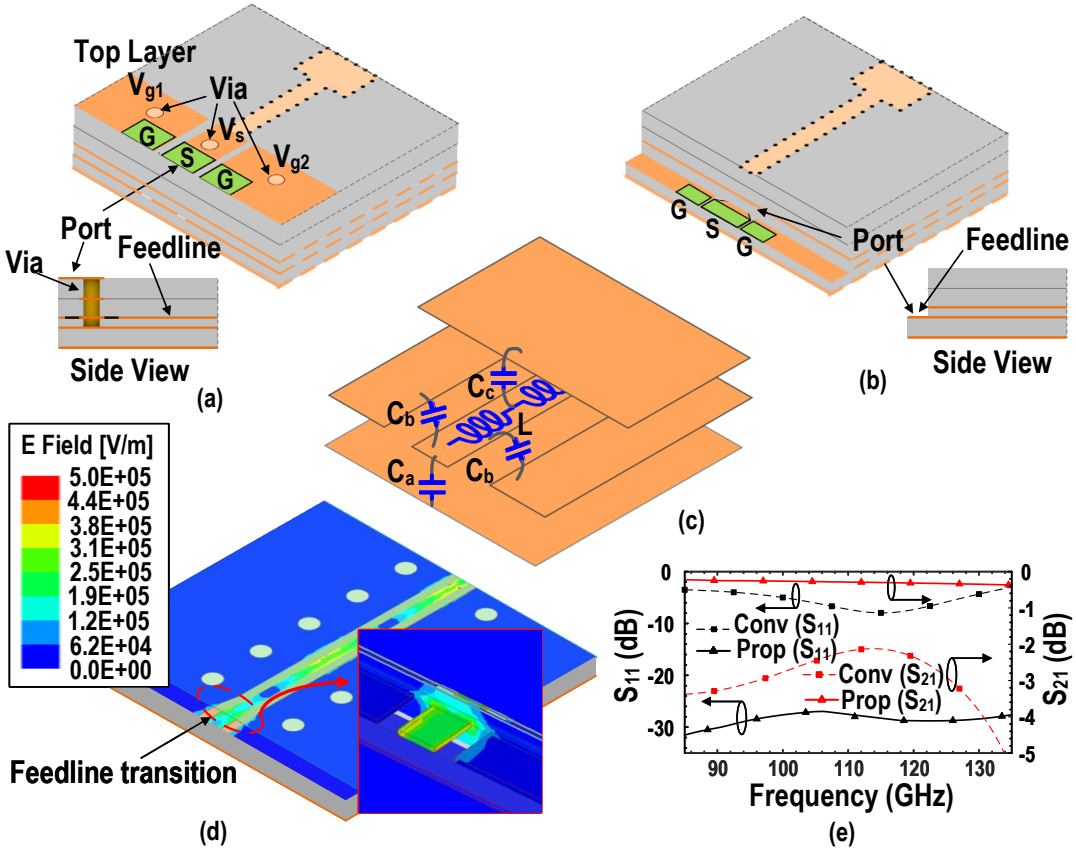

Figure 3.6: Input port configuration of a (a) conventional design using long via from top of the structure to the bottom, (b) proposed GSG port design, (c) different capacitances associated with the GCPW and GCPW with a top ground layer, (d) electric field on the input port and feedline, and (e) S_{11} and S_{21} plots for the conventional and proposed designs.

As an example, a transition from a 50 Ω port impedance to a 50 Ω feedline impedance is designed as shown in Fig. 3.6(d). The electric field around the feedline shows a smooth transition, which is also verified using two-port S- parameter simulation. In Fig. 3.6(e), the proposed design is compared against the conventional via based design of Fig. 3.6(a) for an equal length of 1.55 mm in the frequency range of 85 GHz to 135 GHz. As evident from the Fig 3.6 (e), an impedance matching with $S_{11} < -25$ dB and an insertion loss between 0.2 and 0.55 dB are achieved by the proposed design compared to the minimum return loss of 8 dB and the maximum insertion loss of 2.12 dB attained by the conventional via-based design. Therefore, the proposed design offers a significant advantage compared to the via-based transition in the WR-08 band.

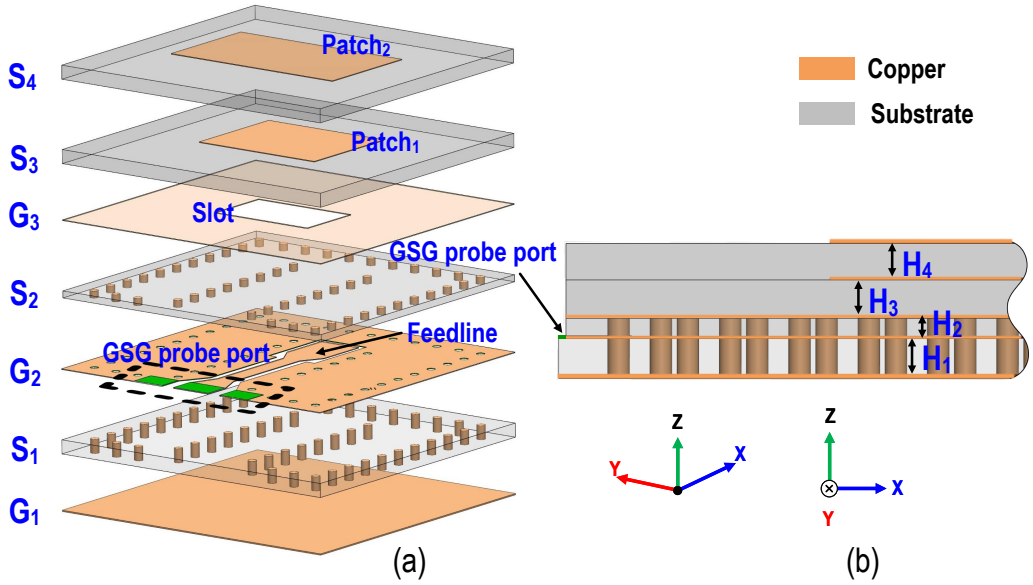

Figure 3.7: Configuration of the proposed antenna. (a) Perspective view, and (b) side view.

3.2.3 Antenna design

The expanded and side views of the proposed antenna are shown in the Figs. 3.7(a) and (b), respectively. The antenna is designed on a flexible substrate with a dielectric constant of 3.1 and a loss tangent of 0.003. Different substrate layers are attached using layers of adhesive material, each with a thickness of 20 μm and a dielectric constant of 3.2 with a loss tangent of 0.0035. The thicknesses of S_1 (H_1), S_3 (H_3), and S_4 (H_4) layers are 50 μm, and that of S_2 (H_2) is the minimum allowable value of 25 μm. This thickness strikes a compromise between coupled electromagnetic energy and bandwidth. The feedline is on the G_2 layer bordering the S_1 and S_2 layers, and the patch antennas metal layers are implemented on top of S_3 and S_4. The copper cladding layers are 12 μm thick, and the pad-open layer for the GSG pads is Gold. The pads are situated on top of G_2 layer, and the width of the signal pad is 50 μm (minimum requirement for WR-08 probe landing).

In mm-wave integrated circuits, signal routing on grounded coplanar waveguide (GCPW) is preferred over microstrip [7] due to enhanced lateral isolation from adjacent circuits. Therefore, to avoid unwanted transition losses between the chipset and the high-frequency

antenna, we deploy GCPW feedline in this design. Compared to a planar microstrip antenna where the feedline radiation may disturb the desired radiation from the antenna, in an aperture-coupled structure, feedline and antennas are on the opposite sides of ground layer, which allows for mitigation of unwanted radiation from the feedline. In the case of antennas co-integrated with a transmitter chipset, the back-side radiation of the feedline will severely disturb the chip functionality if conventional ACSP antenna is used. Therefore, in this structure we added substrate S_1 with an explicit ground layer G_1 underneath to properly shield the feedline. Despite these advantages, a GCPW feedline is prone to excitation of unwanted lateral modes. The details of these modes and the proposed technique to mitigate them are provided in the sub-section 3.2.4.

Based on the theory presented in Section 3.2.1, initial design parameters are evaluated to design TWBDN for $f_1 = 95$ GHz, and $r = 1.26$. Fig. 3.8(a) illustrates the layout design with labeled dimensions of the TWBDN. A small tapered section of transmission line is used to bridge the two sections of the feedline corresponding to TL_1 and TL_2 as it helps improve the bandwidth performance [152]. To design the input port and its transition into the feedline, the design approach presented in Section 3.2.2 is followed. The simulated value of Z_L is plotted over the Smith chart from 85 GHz to 135 GHz, as shown in Fig. 3.8(b). After a broadband TWBDN is designed, two stacked patches are chosen to be added to complete the antenna design. The choice of two patches is based on the fact that a single patch provides lower bandwidth, and addition of a third patch is not feasible in the employed fabrication process. A structure comprising of two patches and matched to TWBDN over a broad frequency range, called TWBDN matched stacked patches (TMSP), is designed and show in Fig. 3.9(a). As illustrated in Fig. 3.9(a), the impedance looking into the TWBDN network is denoted by Z_{down}, and the impedance looking up into the TMSP is indicated as Z_{up}. In the conventional design philosophy, both Z_{down} and Z_{up} are individually matched to a 100 Ω impedance. Since, Z_{up} and Z_{down} are frequency-dependent impedances, matching them to 100 Ω limits the achievable bandwidth. Therefore, in the proposed design, these

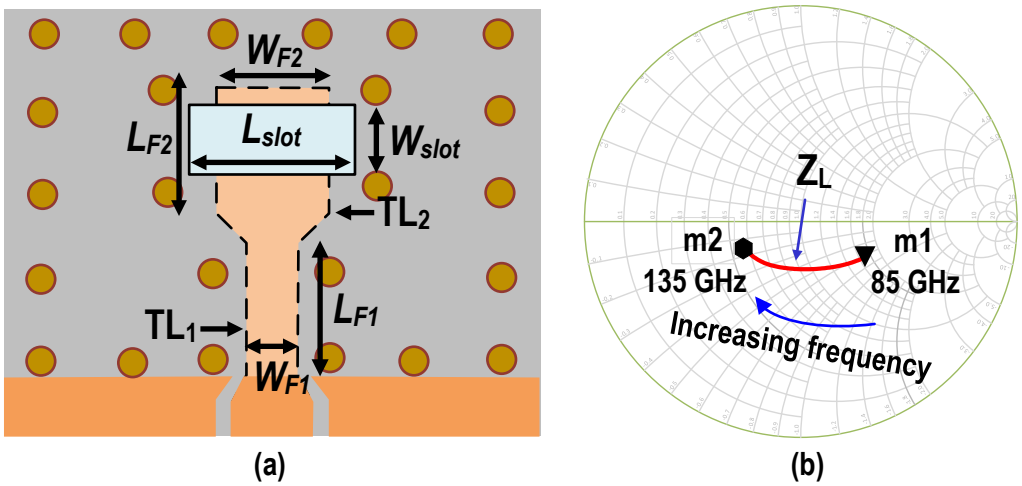

Figure 3.8: (a) schematic diagram, and (b) load trajectory across 85 GHz to 135 GHz.

two impedances are directly matched to each other across the frequency band. For a perfect matching ($S_{11} = 0$), these two impedances must be conjugate matched over the band of frequencies, that is $Z_{up}(f) = Z^*_{down}(f)$. However, a relaxed matching of $S_{11} \leq -10$ dB is sufficient to attain good performance from an antenna. To choose the substrate height H_3 and H_4 of the TSMP in Fig. 3.9(a), three cases are considered. Case I for $H_3 = 25$ μm and $H_4 = 25$ μm, Case II for $H_3 = 50$ μm and $H_4 = 25$ μm, and case III for $H_3 = 50$ μm and $H_4 = 50$ μm. Fig. 3.9(b) shows the impedance trajectories of $Z_{up}(f)$ for the three cases along with the conjugate of $Z_{down}(f)$, $Z^*_{down}(f)$. To obtain the initial patch dimensions, the target VSWR is set to 2.2, which corresponds to $S_{11} \approx -8.5$ dB. In 3.9(b), constant VSWR = 2.2 circles are plotted over the Smith chart (Γ-plane) overlapping the trajectory of $Z^*_{down}(f)$ using the following relation [160],

$$|\Gamma - C_v| = R_v, \tag{3.13}$$

where C_v and R_v are the center and radius of the constant VSWR circles, respectively. From Fig. 3.9(b), it can be observed that among the three cases, case III provides the best matching performance, as the VSWR circle includes the Z^*_{down} trajectory from 95.5 GHz to 130 GHz.

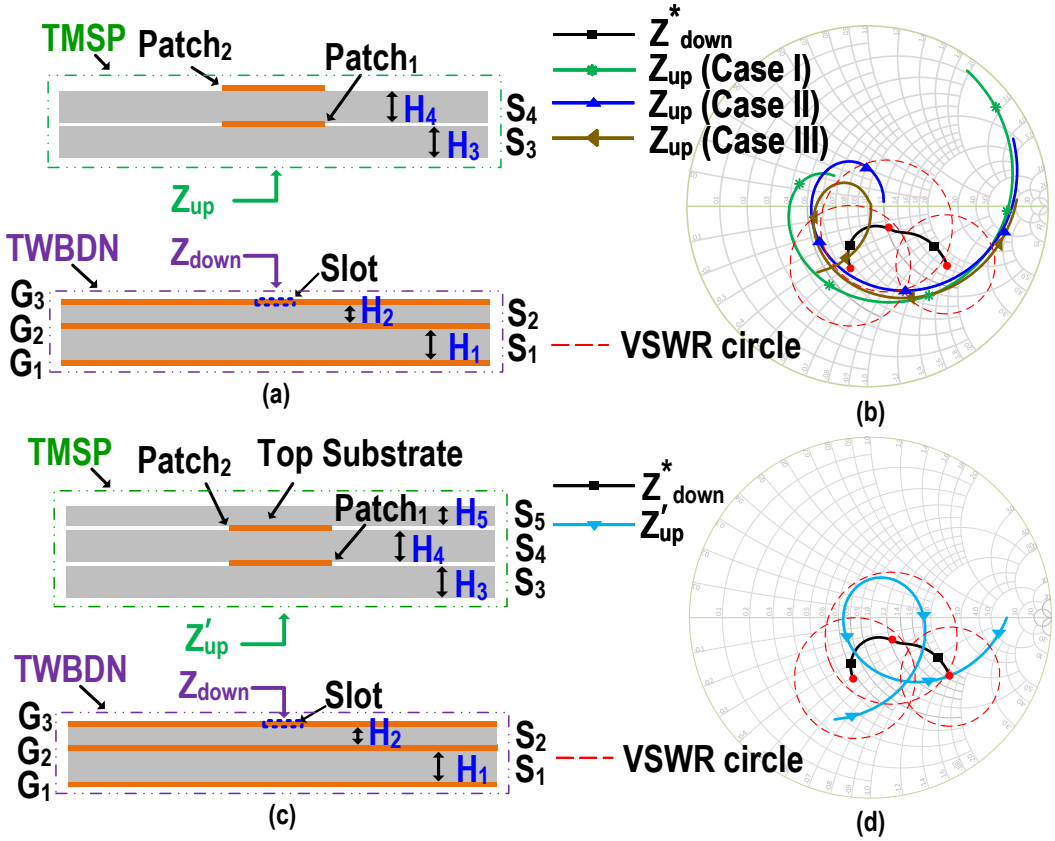

Figure 3.9: (a) side view of the TWBDN and TMSP, (b) impedance trajectories of Z^*_{down}, and Z_{up} for Case I, Case II, and Case III, (c) addition of substrate layer on top of TMSP, and (d) impedance trajectories for Z^*_{down} and Z'_{up}.

To further improve the matching towards the lower frequencies, a substrate, S_5, with a height of 40 μm is added on top of $Patch_2$ as shown in Fig. 3.9(c). The corresponding impedance trajectory for Z'_{up} in this case is shown in Fig. 3.9(d). The addition of substrate layer, S_5, improves the in-band matching performance, and extends the lower frequency response down to 93 GHz. This S_5 layer also protects the upper patch from post-fabrication sliding, and from any other physical damages.

In the final design, the two structures TWBDN and TMSP are combined, and the top view of the final structure is shown in Fig. 3.10(a) with labelled dimensions. After combination, the return loss profile is slightly (up to 5%) deviated, which can be attributed to slight mismatches in field strength of the slot. The final S_{11} plot is shown in Fig. 3.10(b). The

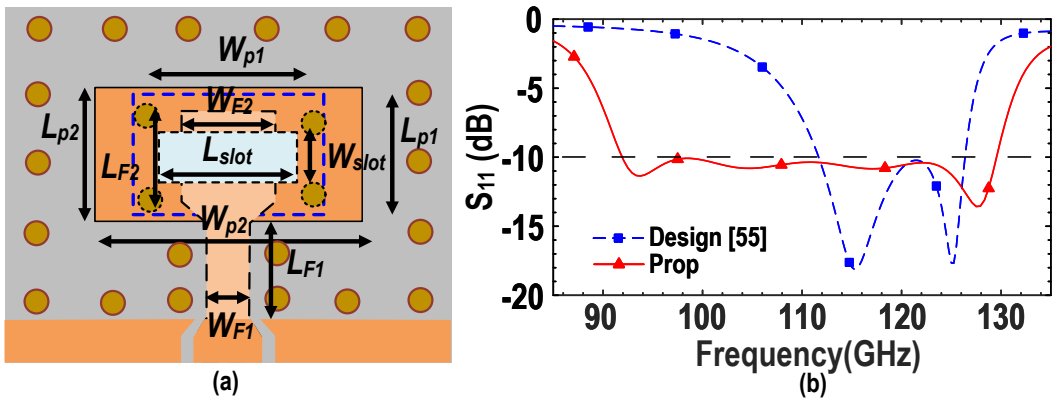

Figure 3.10: (a) top view of the proposed antenna, and (b) simulated S_{11} of the proposed and scaled versions of the antenna in [148]

four minimas in the S_{11} in Fig. 3.10(b) can be explained as: two minimas that correspond to resonances of the two patches, and the other two minimas are due to the dual-band matching nature of the TWBDN. The return loss is lower than 10 dB from 91.94 GHz to 129.53 GHz, which is equivalent to a 37.59 GHz bandwidth. As discussed in section 3.1, a bandwidth of more than 30% in the WR-08 band can provide the target 100+ Gbps data rate for the upcoming 6G wireless communication links. The presented systematic design approach paves the path towards the design of mm-wave ACSP antennas above 100 GHz with unprecedented bandwidth performance, while substantially reducing the optimization task by providing the initial design values.

3.2.4 Undesired modes and their mitigation to improve broadband efficiency performance

The presence of ground planes below and above the feedline alters the wave propagation characteristics in the CPW transmission line. The modes supported by this structure can be grouped as mainly (a) the mode guided by the CPW line, (b) the parallel-plate mode guided between CPW and the lower ground plane, and (c) the parallel-plate mode guided between the CPW and the upper ground plane [161]. These unwanted parallel-plate modes are problematic at mm-wave frequencies [161, 162]. In order to achieve the desired antenna

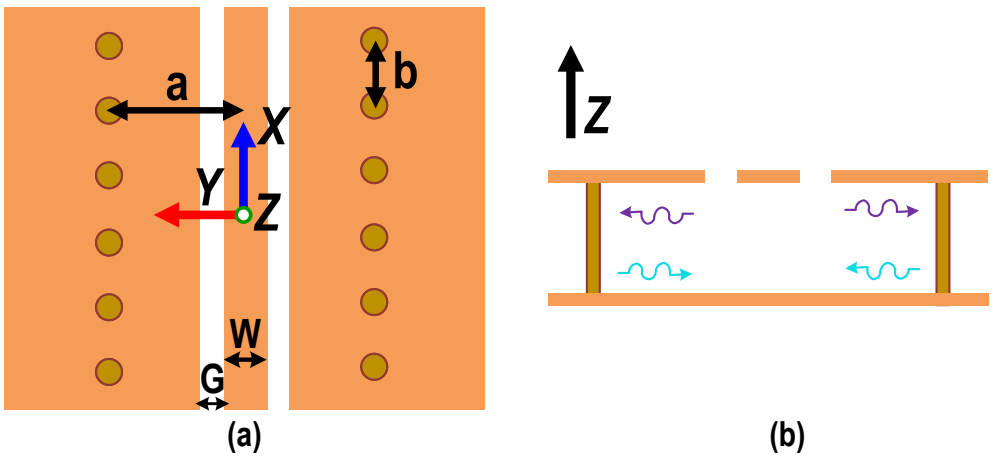

Figure 3.11: GCPW line with via arrays (a) Top view, and (b) side view.

performance, the root causes of unwanted mode excitation must be investigated, and practical solutions that avoid or reduce these unwanted modes to a minimum acceptable level should be introduced.

In a GCPW, parallel-plate mode is excited in the substrate and propagate like a semi-cone with an angle, θ, relative to the X-axis (CPW propagation direction)[163].

$$\cos\theta = \sqrt{\epsilon_{eff}/\epsilon_r} \tag{3.14}$$

where ϵ_{eff} and ϵ_r are the effective and nominal dielectric constants of the substrate, respectively. The parallel-plate mode consists of a TEM mode with zero cut-off frequency whose phase velocity is lower than the guided CPW mode. Its coupling with the guided mode results in power loss. Referring to Fig. 3.11, if $(W+2G)$ is smaller than wavelength, the attenuation constant, α, is given by [163]

$$\alpha = \frac{\pi^2 Z_0 (W+2G)^2}{2h\eta_d \lambda_d^2}\sqrt{1-\epsilon_{eff}/\epsilon_r} \tag{3.15}$$

where Z_0 is the characteristic impedance of the CPW line and $\eta_d = 377/\sqrt{\epsilon_r}$ is the wave impedance of the dielectric. In addition to TEM, other modes such as TE_1 and TM_1 might

also be present depending on the ground plane dimensions as well as the substrate thickness.

There are two ways to reduce/avoid the unwanted mode. One way is to reduce the width of the ground plane along the slot, thus creating a finite-width GCPW (FW-GCPW) structure [161, 164]. In a FW-GCPW, higher order modes are suppressed by reducing the ground width such that $\max[h, (W/2+G+W_g)] \leq 1/(f_{max}\sqrt{2\mu_0\epsilon_0(\epsilon_r - 1)})$, where h is the substrate thickness, W_g is the ground conductor width, and f_{max} is the maximum operating frequency [164] of the transmission line. Although this results in reduced unwanted modes, at higher frequencies several parallel-plate resonances might occur due to the reflection from the open ground end[165, 166], which will substantially degrade the radiation efficiency. Another way to reduce the unwanted mode involves adding an array of vias along the central CPW line at some distance [167], as illustrated in Fig. 3.11(a). In this configuration, the via arrays prevent the lateral propagation of the parallel-plate mode, and therefore, eliminate the coupling with the forward-traveling CPW-guided mode. However, the presence of finite gaps between vias would always result in some leakage [167]. Also, if the center-to-center distance between vias, b, is large, multiple modes will be created that can couple to the CPW line. To avoid the propagation of these modes[167]

$$b \leq \frac{\pi}{k_0\sqrt{\epsilon_r}} = \frac{\lambda_0}{2\sqrt{\epsilon_r}} \tag{3.16}$$

where λ_0 is the free space wavelength. Furthermore, to reduce the attenuation, α, via arrays should be as close as possible to the central CPW conductor. However, placing the via arrays too close to the slot edge would disturb the bound field of the CPW line. There is an excessive attenuation, when the distance between via array and the CPW line exceeds a critical value of

$$a_c = \frac{\pi}{\sqrt{k_0^2\epsilon_r - \beta^2}}. \tag{3.17}$$

This attenuation will be sometimes even more than the losses associated with a line without any via array. This is one of the major problems in any high-frequency stacked patch antenna

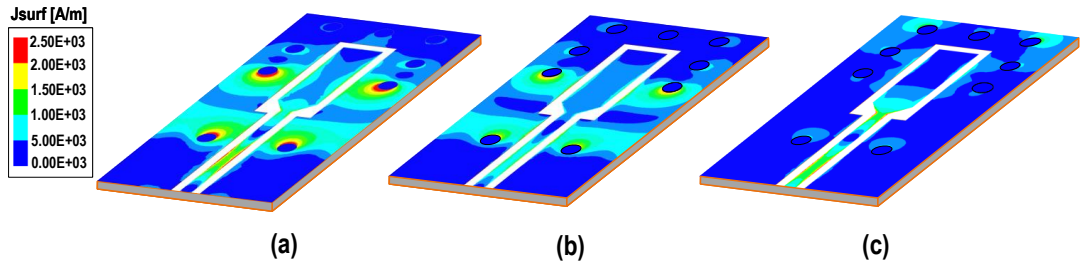

Figure 3.12: Surface current for arbitrary via location at (a) 105.95 GHz, (b) 114.66 GHz, and (c) 125.78 GHz.

design and requires extra care with the configuration of the feedline and vias. The parallel-plate mode excited by the central CPW conductor line experiences multiple reflections. At a=a_c, the transversal propagation distance between the central line and via array approaches $\lambda/4$. This phenomenon can be further explained, as follows:

The wave propagating laterally along the X-axis reflects back from the via array located at $a/2$. The reflected wave then arrives in phase at GCPW feedline since it has traveled a distance of $\lambda/2$. This reflected wave will constructively add with the -Y-directed wave. The -Y propagating wave will also reflect back from the via array located at -$a/2$ with the same phase, and constructively add with the Y-directed wave, as shown in Fig. 3.11(b). These multiple transmissions and reflections of laterally propagating waves will result in resonances, and lead to excessive loss around $a = a_c$[167]. These resonances can occur at multiple frequencies for different resonance modes. In our design, $\lambda_g/2 = 0.65$ mm at 130 GHz. Therefore, the via separation should be less than this value. In Fig. 3.12(a), surface current is plotted for the G_2 layer (comprising both ground layer and feedline) at 105.95 GHz frequency. It is evident that there is a significant amount of surface current around the guided signal on feedline due to the unwanted parallel-plate mode. This corresponds to a drop in the radiation efficiency as low as 30% at 105.95 GHz. Similarly, low efficiencies are also observed at 114.66 GHz and 125.78 GHz, where the efficiency drops to 63% and 69%, respectively. From the profile of the surface current components in Fig. 3.12, it is clear that at 105.95 GHz a stronger parallel-plate resonance with higher energy occurs, which

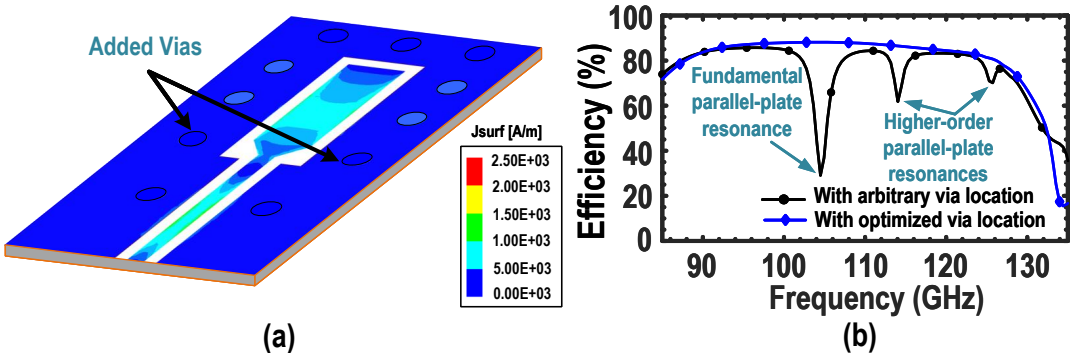

Figure 3.13: (a) Mitigation of surface waves by adding vias in close proximity, and (b) changes in radiation efficiency by mitigation of surface waves.

leads to a more significant drop in efficiency. The resonances at the other two frequencies are higher-order modes with less energy, and thus, reduced impact on efficiency. With

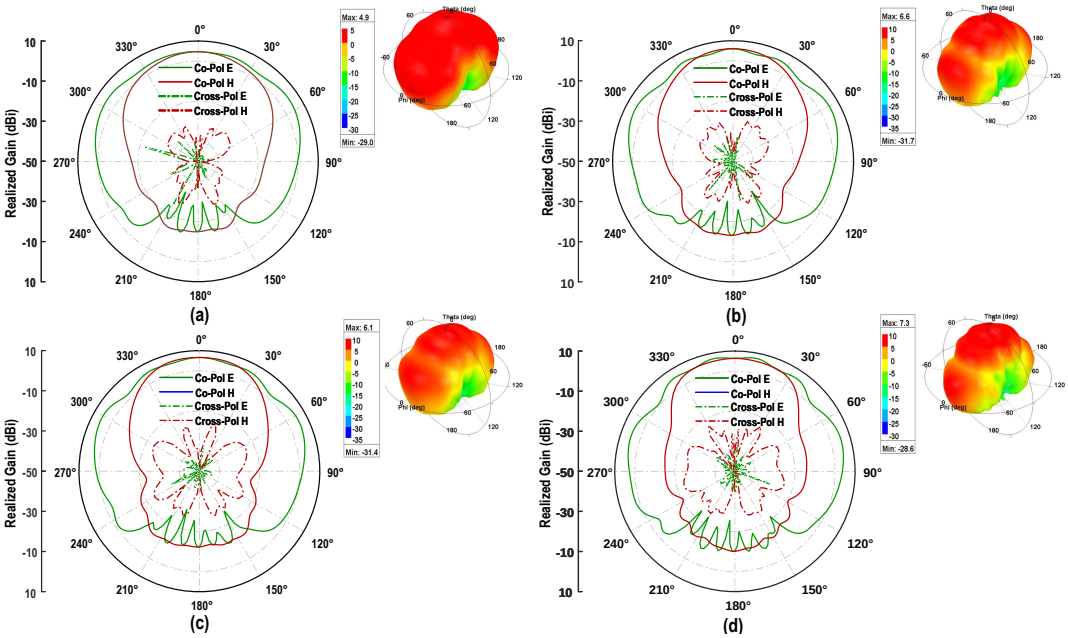

Figure 3.14: Simulated radiation pattern at (a) 100 GHz, (b) 110 GHz, (c) 120 GHz, and (d) 130 GHz.

the placement of vias properly and according to [167], significant improvement in radiation efficiency is achieved, as shown in Figs. 3.13(a) and (b). According to the simulation results, the radiation efficiency is higher than 75% from 89.23 GHz to 127.66 GHz, with a peak efficiency of 89%.

3.2.5 Antenna simulation

The core area of the proposed antenna was initially 3.5×3.5 mm^2. However, measurement of an antenna structure of such small size using a probe station would lead to disturbance in the antenna's radiation characteristics from the GSG probe itself and other metallic components of the probe station. This will, in turn, yield an erroneous result for the gain and S-parameter measurements. While a small-sized antenna is well suited for integration with a transmitter/receiver chip, where the probe is not landed directly on the antenna, the standalone testing mandates a larger footprint of the antenna. Therefore, for this purpose, the antenna size is enlarged to 11.22×11.22 mm^2 for the final fabricated prototype.

Apart from achieving a superior performance in terms of bandwidth, efficiency, and gain, an antenna must also exhibit a uniform radiation pattern and provide low cross-polarization levels across the achieved bandwidth. The generated surface wave between the patch and the ground undergoes diffraction at the edge of the patch, which causes dips in the boresight ($\theta = 0°$) direction of the radiated wave. For an antenna with a large ground plane, the possibility of distortion in radiation pattern is higher [168]. Considering the measurement challenges for a smaller-sized stand-alone antenna at mm-wave frequency, the reduction in dimension is not the best solution. The other possible method to minimize the surface wave is to reduce the substrate thickness. In a linearly polarized antenna, the co-polarization fields are aligned with the dimension of the resonating element. On the other hand, the fringing fields across the non-radiating element may excite cross-polarized fields, which is more likely to occur in a wideband antenna due to transversal currents of the higher-order modes [106, 169]. The cross-polarization also decreases with the reduced substrate thickness. Moreover, in an aperture-coupled antenna, cross-polarization is lower for a rectangular patch compared to a square counterpart (L_P=W_P) [170]. In the proposed antenna, a substrate thickness of 50 μm and rectangular-shape patches were utilized, where the latter helps maintain a good radiation pattern in the boresight and reduce the cross-polarization significantly across the band. Fig.

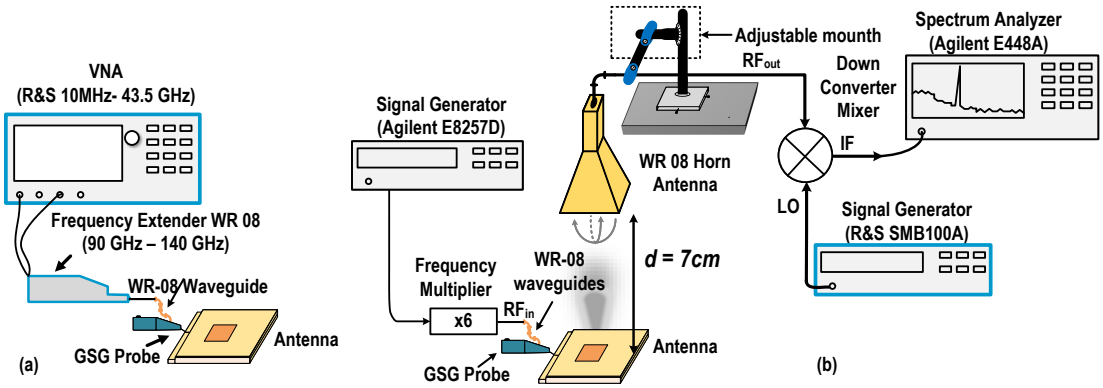

Figure 3.15: Block diagram of the setup for (a) S_{11}, and (b) gain and radiation pattern measurement.

3.14 shows the simulated E- and H-plane pattern along with 3-D radiation pattern at 100-, 110-, 120- and 130-GHz. The peak realized gains in the boresight direction are 4.65-, 6.02-, 6.59-, and 6.34-dBi at 100-, 110-, 120-, and 130-GHz, respectively. Furthermore, a front-to-back ratio of more than 16 dB is attained across the band. The achieved radiation pattern is very uniform across the whole band, and does not show any dip in the boresight direction. This corroborates the earlier theory that studied the reduction in surface wave due to a reduction substrate thickness.

3.3 Prototype and Measurement Results

The proposed antenna structure is fabricated by MFLEX Inc. on a flexible PCB with a total dimension of 11.22×11.22 mm^2, and the spacing for GSG probe pad, implemented on G_2 layer (*cf.* Fig. 3.7), is 100 μm.

3.3.1 Measurement setup

The block diagrams of the measurement setup to evaluate S-parameter, gain, and radiation pattern are shown in Figs. 3.15(a) and (b), respectively.

A Rohde & Schwarz's R&S-ZNA vector network analyzer accompanied by a WR-08 band fre-

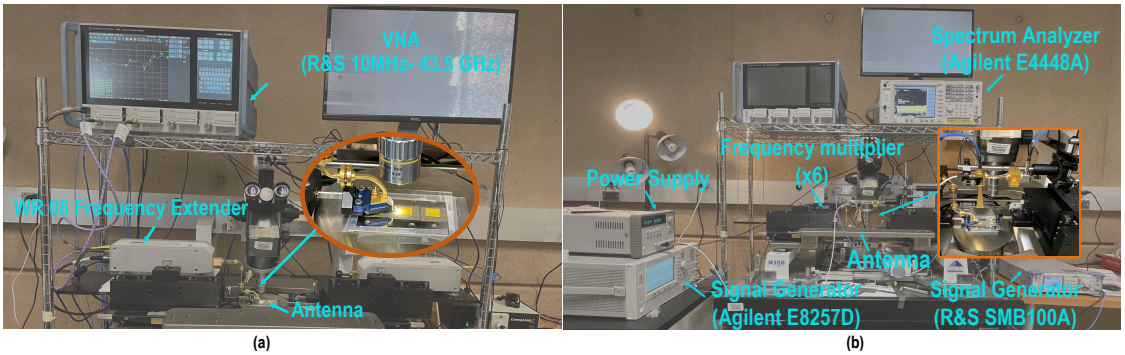

Figure 3.16: Measurement setup for (a) S_{11}, and (b) gain and radiation pattern measurement.

quency extender was used for the S-parameters measurement. This band extender upgrades the frequency range of the VNA from a lower frequency band to the desired WR-08 band (90-140 GHz). For the gain measurement, a $\times 6$ frequency multiplier was used to up-convert the low frequency signal from the Agilent E8257D signal generator to WR-08 band. The output of the multiplier was injected into the antenna-under-test (AUT) through a GSG probe, and the physical connection between the frequency multiplier and probe was established with WR-08 waveguide connectors. Once properly excited, the radiated signal by the AUT was then received through a high-gain diagonal horn antenna located at a distance, $d = 7$ cm, and subsequently down-converted by a third harmonic mixer. The local oscillator (LO) and intermediate frequency (IF) ports of the mixer were connected to the Rohde & Schwarz SMB 100A signal generator and Agilent E4448A spectrum analyzer, respectively. The LO signal was set at a frequency of 35 GHz and the received RF signal was at a frequency of 100 GHz. The output signal measured by the spectrum analyzer was therefore at an IF frequency of $35\times3\text{-}100 = 5$ GHz.

In order to account for the path-loss and connectors' attenuation during measurement, in a calibration phase, horn antennas were first employed on both the transmitter and receiver sides at a fixed distance of $d = 28$ cm, and the received output power across the entire WR-08 band was measured with 2-GHz steps. In the next step, the transmitting antenna was replaced by the fabricated AUT at a reduced distance of $d = 7$ cm, as the AUT provides

lower gain compared to the diagonal horn antenna with a Gain of 26 dBi. For the gain measurement, we employed the Friis free-space path-loss equation,

$$P_r(d)|_{dBm} = P_t|_{dBm} + G_t|_{dBi} + G_r|_{dBi} + 20log_{10}(\lambda) - 20log_{10}(4\pi d),$$

where P_r is the received power, P_t is the transmitted power, λ is the free-space wavelength, and G_t and G_r are the antenna gains of the transmitter and receiver, respectively. For the calibration phase, both G_t and G_r are 26 dBi. Based on the Friis free-space path-loss equation, the expected received power for the diagonal horn receiver at $d = 7$ cm is calculated ($P_{r,h}(7cm)$) and once compared with the receiver power from AUT at the same distance ($P_{r,AUT}(7cm)$),

$$P_{r,h}(7cm) - P_{r,AUT}(7cm) = 26 - G_{AUT}, \tag{3.18}$$

was used to find the gain of the proposed antenna, G_{AUT}. It is noteworthy that due to the limitation of the Friis equation to planar waves, $d = 7$ cm was chosen to be substantially larger than the mm-scale Fraunhofer distance ($d = 2D^2/\lambda$), which is 2.6 mm for a 130 GHz radiating antenna with $D = 1.73$ mm. This allows the gain estimations based on Friis equation for the AUT. Furthermore, extra loss contributed by the GSG probe was also accounted for using the data sheet provided by the manufacturer of the GSG probe.

In the gain measurement setup, the receiver horn antenna was mounted on a movable arm, as shown in Fig. 3.15(b). This facilitates its rotation in both the E-and the H-plane, independently. E-and H-plane gain measurements were carried out by rotating the antenna in the corresponding plane with a step of 5° angular movement. However, due to the movement blockage in both planes by the surrounding equipment, measurements were carried out only up to an angular rotation of 40° which was sufficient to evaluate the broadside radiation pattern.

Table 3.1: Comparison With State-of-the-Art Antennas Above 100 GHz

References	**Freq.** (GHz)	**BW** (GHz / %)	**Peak Gain** (dBi)	**Gain Var.** (dB)	**Peak Rad. Eff.** (%)	**Layers**	**Dim.** (λ_0^2)	**Tech.**
[126] (DI)*	106–114	8/7.2	2.7	−5–2.7	47	5	NA	0.18 μm BiCMOS
[127] (SE)	126–144**	18/13	3.7	NA	62*	3	0.3×0.4	0.18 μm CMOS
[129] (SE)	135–165	>20/14	5.1	3.1–5.1**	76	3	1×1	0.13 μm BiCMOS
[130] (SE)	89.2–95.7	6.5/6.91	13.3	3–13.3**	NA	2	3.13×3.13	LTCC
[131] (SE)*	112–135	23/18.6	5	3–5	NA	2	$0.48 \times 0.8^{\dagger}$	0.13 μm BiCMOS
[132] (SE)	84.5–93.5**	9/10.11**	1.61	1.61–6.88**	NA	2	0.35×0.4	0.13 μm BiCMOS
[133] DI	100.3–133.5	33/28.5	9.5	4.5**–9.5	88*	5	2.8×2.8	PCB
[133] SE*	115–140**	25/19.2	7.3	4.6**–7.3	82	5	2.8×2.8	PCB
This Work (SE)	**90–128.5**	**38.5/35.2**	**7.95**	**4.1–7.95**	**89***	**4**	$\mathbf{1.28 \times 1.28^{\ddagger}}$	**Flexible PCB**

*Simulated, **Estimated from graph, †Estimated from figure, ‡Initial design, SE: single-ended, DI: differential

The actual physical test-bench for S-parameter and gain measurement are shown in Figs. 3.16(a) and (b), respectively. As highlighted in Fig. 3.16(a), due to the sensitivity of probes, we mounted three samples of the AUT on the same host board, and S_{11} measurements were carried out consecutively by landing and lifting the probe for each sample without disturbing the rest of measurement set up. This allowed us to minimize error induced by set-up fluctuations in the measurement of different samples, which was critical for performance verification. Also, as shown in Fig. 3.16(b), the probe-station microscope head and lenses have been the main obstacles ahead of receiver antenna rotation in the radiation pattern measurements. Given the small beam-width of the radiation signal by the AUT and the mechanical perturbations that were inevitable in the measurements, a slight discrepancy was observed between the measured and simulated radiation patterns.

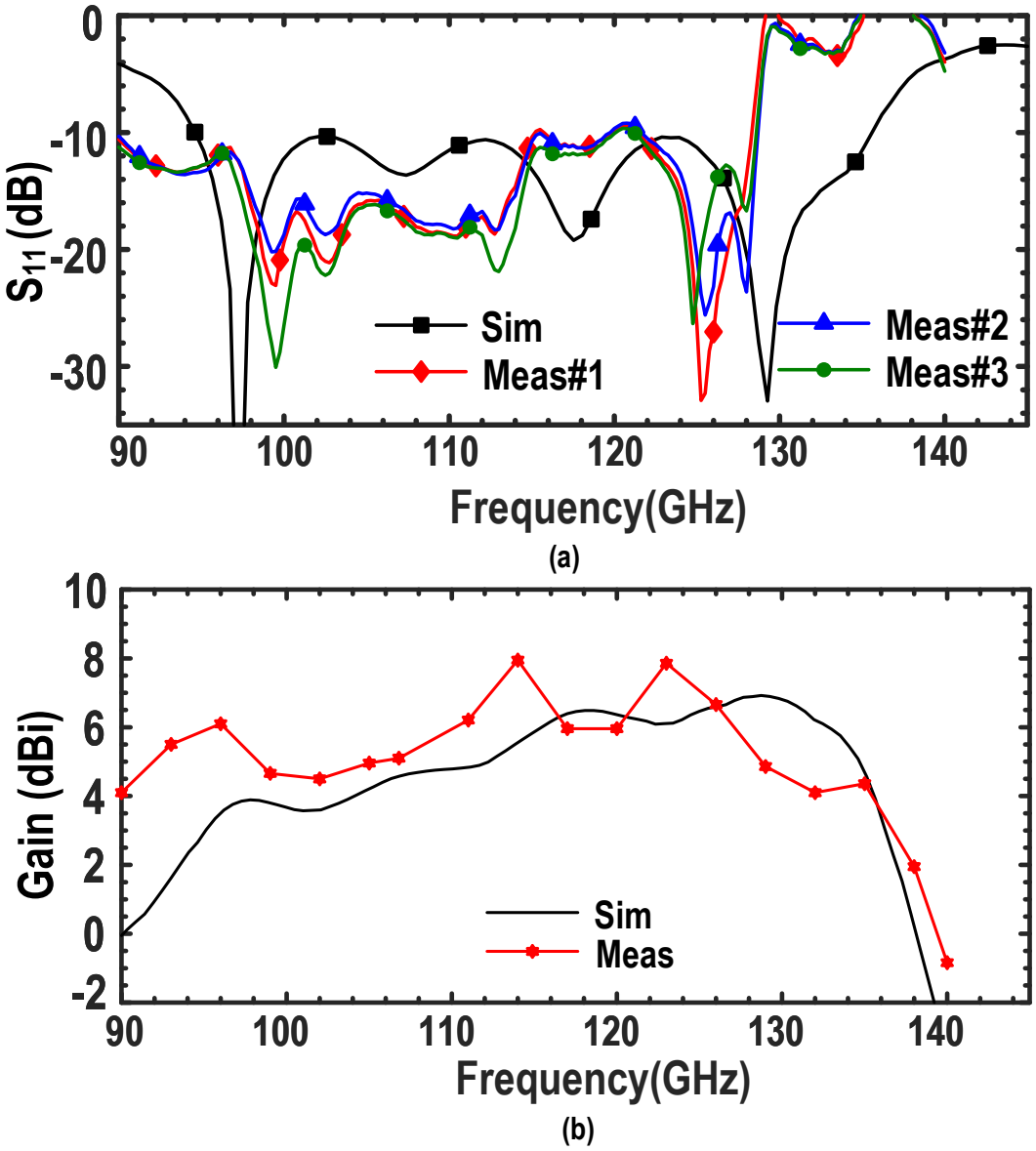

Figure 3.17: Simulated and measured (a) S_{11}, and (b) gain.

3.3.2 Comparison of measurement and simulation results

For comparison purpose, simulated and measured S_{11} and gain are overlaid on the same plots in Figs. 3.17(a) and (b), respectively. To verify the S_{11}, we measured three samples of the fabricated antenna, which exhibit very similar profiles, as shown in Fig. 3.17(a). The measured S_{11} of the three samples exhibit almost identical bandwidths. In particular, the S_{11} of Sample 1 is below -10 dB from 90- to 115-GHz, 115.75- to 119.75-GHz, and 121.5- to

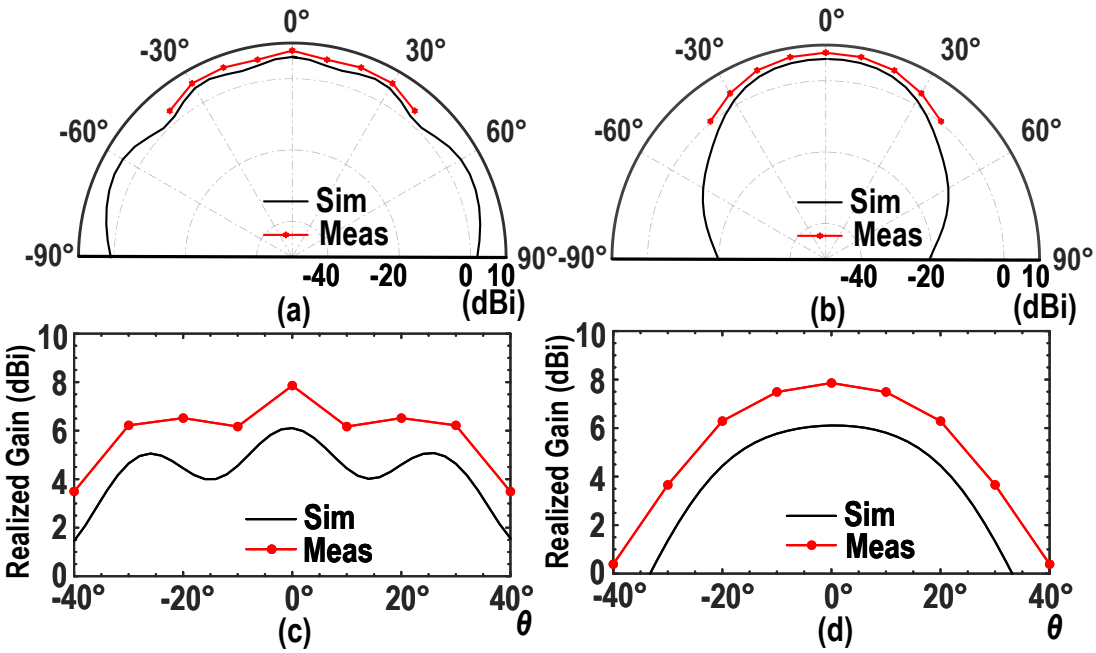

Figure 3.18: Simulated and measured gain for E-plane (a) rectangular plot. (b) polar plot and for H-Plane (c) rectangular plot. (d) polar plot.

128.25-GHz, which is equal to 35.75-GHz bandwidth as compared to the simulated bandwidth of 40.8 GHz from 94.7- to 135.5-GHz (simulated bandwidth of 44.99 GHz in [171] for $\epsilon_r = 2.6$). For Sample 2 and Sample 3, the measured bandwidth is 36.25 GHz and 37.5 GHz, respectively. The slight variations in these three measured S_{11} profiles are mainly caused by two inevitable factors: (a) It is extremely hard to obtain identical probe-landing profile (location of the probe on the pads) across all the samples in this probe-based measurement, and due to fragility of the high-frequency probe, multiple lifting and landing over a sample to adjust the probe location is not advisable. (b) The PCB samples exhibit fabrication-induced variations such as movement of slot and patch layers with respect to the feedline. Fig. 3.17(b) shows a comparison between measured and simulated gains. The measured gain is higher than 4.1 dBi from 90- to 132-GHz with a peak measured gain of 7.95 dBi at 114 GHz. Similar to the S_{11} plot, there is also a slight mismatch between the measured and simulated gain values due to the proximity effect of measurement setup on the radiation pattern. A similar mismatch is observed in [133] which also performs a probe-based measurement. The

measured E- and H-plane radiation patterns at 123 GHz is shown in Fig. 3.18(a) and (b), respectively. The plot shows a close match between the measured and simulated radiation patterns in both E and H-planes as shown in more detail in Fig. 3.18(c) and (d). The difference between measured and simulated radiation patterns is between 1.35-2.33 dB in the E-plane and 1.68-2.32 dB in the H-plane.

The performance of the proposed antenna is compared against the prior art in Table 3.1. Comparing with the single-ended structures, including the single-ended version in [133], the proposed antenna achieves the highest radiation bandwidth, a competitive gain, very small gain variation, and one of the highest radiation efficiencies among the antennas operating in 90-170 GHz range. The dimension of the proposed antenna is increased from an initially designed value of 1.28× 1.28 λ_0^2 to 4.12×4.12 λ_0^2 for the accuracy and feasibility of measurement. Since the probe tip lands farther from the radiating element, measurement becomes possible to carryout and also the results are more accurate as the disturbance from the probe tip is reduced.[133] offers two types of antennas, a differential-fed structure with more than 28.5% bandwidth (for S_{11} below -9.4 dB) and 9.5 dBi peak gain, and a single-ended version with 19.2% fractional bandwidth and 7.3 dBi peak gain. It is worth noting that two possibilities for routing the signal from a transceiver chipset to a differential-fed antenna can be conceived: (1) The transceiver chipset is fully differential. In this case, additional PCB/die pads (e.g., GSSG or GSGSG) are required. This will readily increase the layout complexity, and the parasitics associated with the pads will further complicate the impedance matching. (2) The input/output signals to/from the transceiver are single-ended. In this case, an off-chip balun is required to generate differential signals to the antenna. However, a balun experiences inherent amplitude/phase imbalance across large bandwidths. In addition, its inevitable insertion loss adversely impacts the overall radiated power by a transmitter. This is why a single-ended structure was adopted in this work.

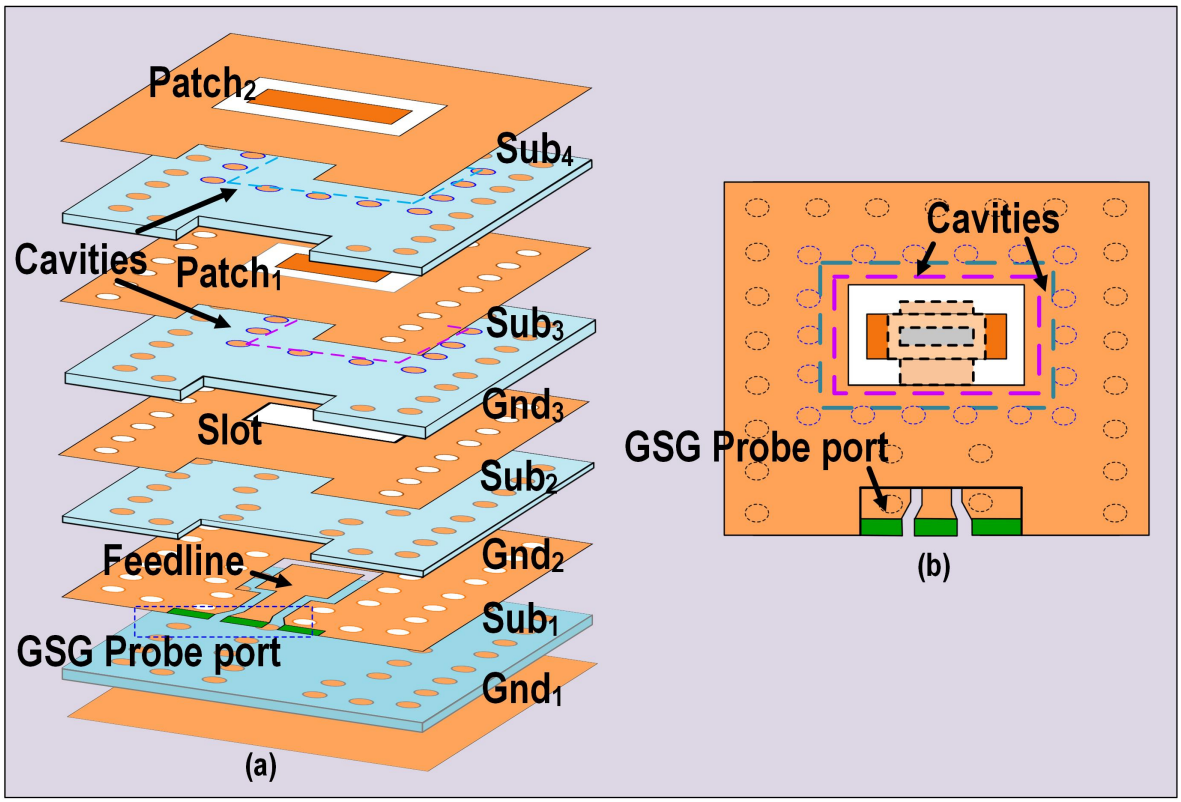

Figure 3.19: (a) Proposed broadband antenna, (b) the designated cavities help with the surface wave cancellation.

3.4 Broadband Cavity-Backed ACSP Antenna

The antenna presented in the preceding sections achieves a measured bandwidth of 38.5 GHz and a peak gain of 7.95 dBi with a peak efficiency of 89%. To enable 6G high-speed communication above 100 GHz, further enhancement of the radiation bandwidth is desirable, and to this end, we present in this section an FPC-based broadband cavity-backed aperture-coupled stacked patch antenna (CB-ACSP) operating across the 91.50-134 GHz frequency range. Flexible board technologies enable the physical deformation of the antennas and passive structures, which find applications in emerging communication systems such as flexible phased arrays [172]. This antenna can be used for beyond 5G communication transceivers as well as next-generation high-resolution sensing systems.

The three-dimensional view of the proposed antenna in Fig. 3.19 (a) shows the different di-

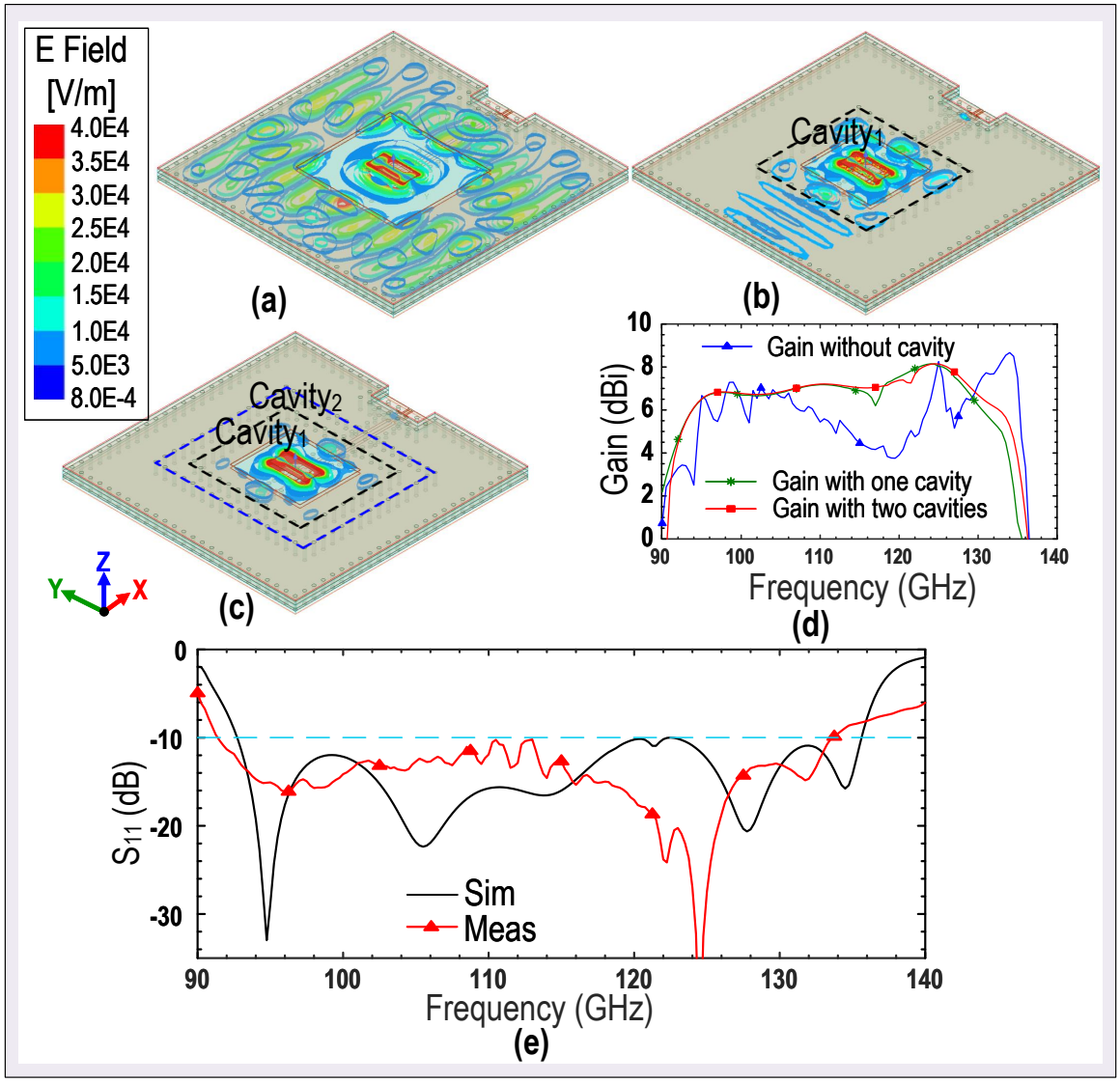

Figure 3.20: Electric field around the patches (a) without any cavity at 120 GHz, (b) with a single cavity at 135 GHz, and (c) with two cavities at 135 GHz, and (d) corresponding gain plots, and (e) measured and simulated S_{11} plot.

electric and metal layers, and Fig.3.19 (b) shows the top view of the antenna. All the ground and patch layers employ a 12 μm thin copper cladding, and the dielectric substrates have ϵ_r = 2.6 and loss tangent of 0.003. Since a thicker substrate is favorable for wideband performance, the substrate layers Sub_1, Sub_3, and Sub_4 use the maximum permissible thickness of 50 μm in the FPC technology. A reduced thickness of 25 μm is employed for Sub_2, which attains substantial coupling between feedline and the slot aperture. A G-S-G probe port is

designed in the Gnd_2 layer and is attached to the feedline. The feedline is configured as a grounded co-planar waveguide (GCPW) which achieves compatibility with the G-S-G probe port. To provide wideband matching between the input G-S-G port and the slot, the feedline is designed as a two-section transmission line. One section with 50 Ω impedance matches to the 50 Ω port, while a wider low-impedance section matches to the impedance of slot aperture. The presence of conductor layers above and below the feedline introduces the unwanted parallel-plate modes which resonate at several discrete frequencies. These unwanted modes cause a substantial drop in the radiation efficiency, and subsequently reduce the gain of the antenna. To suppress these unwanted modes, top-down vias are added around the feedline following the approach of the preceding sections [39, 171], as demonstrated in Fig. 3.19(a). However, in addition to these feedline-induced parallel-plate modes, another major source of surface waves is the radiating patches, which is not addressed in the design of Section 3.2 [39, 171]. By reducing these surface waves around the patches, the gain performance of the antenna can be further improved. Therefore, in the proposed design, two cavities are added that help to suppress the surface waves around the patches.

The cavity is formed by employing arrays of vias to form a conductor wall around the patches. Since the fabrication process dictates the minimum gap allowed between the vias, some amount of surface waves manages to leak through the gap between the vias. This issue becomes more problematic, especially when designing a broadband antenna. In a broadband antenna, for the upper range of frequencies, the wavelength becomes smaller, and requires the vias to be placed closer together compared to the lower range of frequencies. In the FPC technology, the minimum allowed separation between vias is 0.32 mm, which is insufficient to contain all the surface waves in the cavity over the broad range of frequencies. To suppress the propagation of leaked surface waves in the substrate, another cavity can be employed at a distance from the first cavity. In Fig. 3.20(a)-(d), the electric field in the substrate and the corresponding gain plots across the frequency are plotted for the antenna without any cavity, the antenna with a single cavity, and the antenna with two cavities. In Fig. 3.20(a), the

electric field for the antenna without any cavity is plotted at 120 GHz. It can be observed that a substantial electric field propagates in the substrate, which results in the drop in gain, as also evident from the corresponding gain plot in Fig. 3.20(d). After employing a cavity around the patches, marked as Cavity_1, the electric field is reduced in the substrate as shown in Fig. 3.20(b), where electric field is plotted at 135 GHz. With the addition of another cavity, Cavity_2, the electric fields are confined well within the cavities as shown by the electric field plot at 135 GHz in Fig. 3.20(c). The gain plots for the antenna with two cavities in Fig. 3.20(d) show the reduced fluctuations in the gain compared to the antenna without a cavity and with a single cavity. The simulated and measured S_{11} plots are also shown in Fig. 3.20(e). The simulated -10 dB return loss bandwidth extends from 92.7 GHz to 135.6 GHz, while the measured bandwidth extends from 91.5 GHz to 134 GHz, which is equivalent to 37.69% fractional bandwidth. The slight shift in frequency range could be attributed to the variation in permittivity of the substrate, or the placement of the probe tip at some distance from the actual port location during the measurement. The measured peak gain is 8.1 dBi, which is close to the simulated peak gain of 8.16 dBi.

In Table 3.2, the performance of the proposed antenna is compared with the state-of-the-art antennas. It is observed that the proposed antenna provides better gain and bandwidth compared to most of the reported works. The proposed antenna provides a slight improvement in gain over the antenna presented in the preceding sections [39]. In terms of bandwidth, the presented antenna improves the bandwidth by an additional 4 GHz. As compared to the antenna in [133], the presented antenna achieves a 9.5 GHz of higher bandwidth. Moreover, the antenna in [133] employs an additional substrate layer, which is not common among commercial board technologies.

Table 3.2: Performance Comparison of the CB-ACSP With State-of-the-Art Antennas

Ref.	**Frequency** (GHz)	**Gain** (dBi)	**Bandwidth** (GHz / %)	**3-dB BW** (GHz)	**Layers**	**Technology**
[129]	135–165	5.1	>20/14	>30	3	0.13 μm SiGe BiCMOS
[130]	89.2–95.7/6.91	13.3	6.5/6.91	3	2	LTCC
[133]	100.3–133.5	9.5	33/28.5	31	5	PCB
Sec. 3.2 [39]	90–128.5	7.95	38.5/35.2	29.5	4	Flexible PCB
[173]	150–165*	6	15/9.5	40	2	0.13 μm SiGe BiCMOS
[174]	86–89.5*	0.7	3.5/3.9	10*	3	0.13 μm CMOS
[175]	89–97*	3	8/8.6	7.75*	3	0.13 μm CMOS
This work (CB-ACSP)	**91.5–134**	**8.1**	**42.5/37.69**	**41.56**†	**4**	**Flexible PCB**

Ref.: reference, BW: bandwidth, *estimated from plot, †preliminary result

3.5 Conclusion

Two above-100-GHz wideband stacked-patch antennas on a flexible printed circuit were presented. For the first antenna, the broadband design approach, the low-loss G-S-G to feedline transition, the mitigation of unwanted surface waves, and the simulation and measurement results were provided and studied. The measurement results confirm a 38.5 GHz bandwidth from 90 to 128.5 GHz with a close match between simulated and measured radiation pattern and antenna gain. Building upon this design, the CB-ACSP antenna suppresses the surface waves launched by the radiating patches through two via-wall cavities, and extends the measured bandwidth to 42.5 GHz across 91.5–134 GHz, which is equivalent to a 37.69% fractional bandwidth—to the best of our knowledge, the highest reported among off-chip antennas above 100 GHz—with a peak gain of 8.1 dBi. The proposed antenna prototypes unfold the realm of off-chip radiation above 100 GHz with superior efficiency, gain, and attainable bandwidth compared to on-chip counterparts, enabling realization of transceiver links for 6G communication.

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Appendix A

Nonlinear Transconductance (g_m) Model

In short-channel CMOS, mobility degradation due to vertical electric fields introduces nonlinearity in transconductance. It is often modeled as:

$$\mu_{\text{eff}} = \mu_0 / \left(1 + \theta(V_{GS} - V_{th})\right)$$

where μ_0 is the low-field mobility and θ accounts for surface scattering. To capture higher-order effects, with θ_1 and θ_2 representing first- and second-order degradation under strong inversion, the model is extended as [176]:

$$\mu_{\text{eff}} = \mu_0 / \left(1 + \theta_1(V_{GS} - V_{th}) + \theta_2(V_{GS} - V_{th})^2\right)$$

Since $g_m \propto \mu_{\text{eff}}$, similar compression occurs in transconductance. For modeling, we adopt the empirical rational form:

$$g_m(v_{gs}) = g_{m0} \big/ \left(1 + \alpha v_{gs} + \beta v_{gs}^2\right)$$

This form captures both initial linear behavior and higher-order compression, offering a simple yet effective model for nonlinear circuit simulation.

Appendix B

g_m–I_D Relation for Short-Channel Transistors

As described in [177], the drain current in short-channel transistors is modeled as

$$I_D = K(V_{GS} - V_{th})^{\alpha} \tag{B.1}$$

where $\alpha \in [1.2, 1.3]$. The corresponding transconductance is

$$g_m = (dI_D/dV_{GS}) = \alpha K(V_{GS} - V_{th})^{\alpha-1} \tag{B.2}$$

Rearranging gives the current in terms of g_m as

$$I_D = (g_m/\alpha)(V_{GS} - V_{th}) \tag{B.3}$$

Appendix C

Turn Ratio for MS–ST TL Transition Transformer

For a microstrip-to-slotline (MS–ST) transition with MS width W_m and ST width W_s, the transformer turn ratio is [178]:

$$n = \left[J_0\left(k_{es}W_m/2\right) J_0\left(k_{em}W_s/2\right) \big/ \left(k_{es}^2 + k_{em}^2\right)\right] \cdot \Psi \tag{C.1}$$

where $J_0(\cdot)$ is the zeroth-order Bessel function, and Ψ is:

$$\begin{aligned} \Psi = {} & k_{em}^2 k_2 \varepsilon_r / (k_2 \varepsilon_r \cos(k_1 h) - k_1 \sin(k_1 h)) \\ & + k_{es}^2 k_1 / (k_1 \cos(k_1 h) + k_2 \sin(k_1 h)) \end{aligned} \tag{C.2}$$

The wavevectors are given by

$$k_1 = k_0\sqrt{\varepsilon_r - \varepsilon_{res} - \varepsilon_{rem}}, \quad k_2 = k_0\sqrt{\varepsilon_{res} + \varepsilon_{rem} - 1}$$

$$k_{es} = k_0\sqrt{\varepsilon_{res}}, \quad k_{em} = k_0\sqrt{\varepsilon_{rem}},$$

where ϵ_r, ϵ_{res}, and ϵ_{rem} are the effective permittivity of the free space, slotline and microstrip line and k_0 is the air propagation constant.

Appendix D

Lumped Equivalent Model of ACSP antenna

To simplify the understanding of stacked patch antenna, various circuits based models have been proposed, e.g., cavity model, and transmission line model[105, 106]. The results obtained from these models are close to the full-wave analysis solution. Circuit models for aperture coupled antennas have also been developed by extending circuit models of the patch employing cavity or transmission line models [150]. In a simplified circuit model, patch and slot are modeled as a RLC resonant circuit[151], and magnetic coupling between feedline and slot, and slot and patch are realized in the form of coupled inductors. The coupling between lower and upper patches is represented by a capacitor. The equivalent circuit model for design III is shown in Fig. D.1.

Transmission line (TL) section with impedance Z_1 and θ_1 represent feedline, and the portion of feedline crossing the slot acts as an open stub with length θ_{st}. This stub helps cancel the imaginary part of the impedance before it. An inductor L_f is used to couple energy from the feedline to the aperture which consists of the equivalent circuit elements L_s, C_s and R_s,

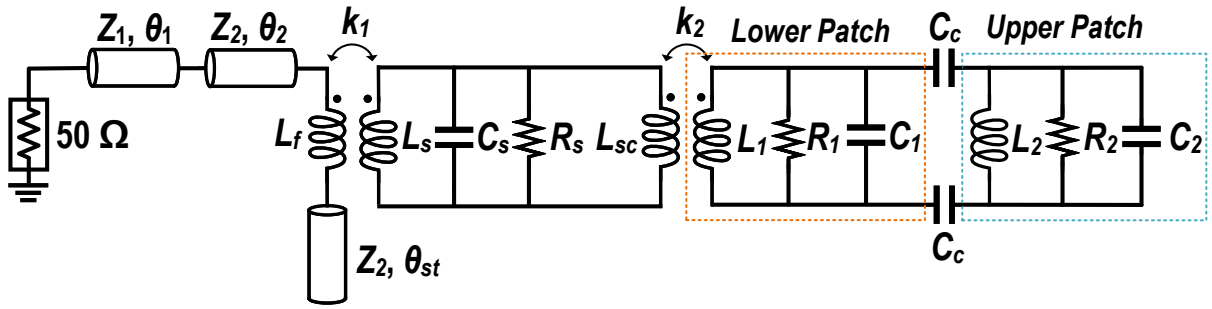

Figure D.1: Circuit equivalent model of design III.

and k_1 represents the coupling coefficient between them. L_1, C_1, and R_1, and L_2, C_2, and R_2 forms the equivalent circuit model of the lower and the upper patches, respectively [150, 151]. The magnetic coupling between slot and lower patch is achieve through an inductor L_{sc} with a coupling co-efficient of k_2, and the electric coupling between upper and lower patches is realized through the capacitors C_c.