UNIVERSITY OF CALIFORNIA

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Broadband Sub-THz Low Noise Amplifier Design in Silicon

A thesis submitted in partial satisfaction

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Master of Science in Electrical and Computer Engineering

by

Sidharth Thomas

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ABSTRACT OF THE THESIS

Broadband Sub-THz Low Noise Amplifier Design in Silicon

by

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Master of Science in Electrical and Computer Engineering
University of California, Los Angeles, 2022
Professor Aydin Babakhani, Chair

The THz band (0.1 - 10 THz) holds several applications such as high-speed communication, 3D imaging radars, and spectroscopy. A high-sensitivity receiver is crucial for fully utilizing this broad untapped spectrum. Advancements in silicon technologies now enable transistors with maximum oscillation frequency (f_{max}) beyond 400 GHz, enabling silicon THz ICs.

This thesis presents two ultra-wideband low noise amplifiers in the THz band, designed using silicon technologies. Several key concepts are discussed, such as optimal bias selection, passive circuit modeling, bandwidth enhancement, circuit-EM co-simulation approaches, and THz probe-based testing. The first design is a 7-stage cascaded common-emitter LNA with more than 80 GHz of 3-dB bandwidth, covering the entire WR5 frequency band (140-220 GHz). It has a measured peak gain of 15.5 dB and a simulated NF of 6.8 dB at 180 GHz, with 46 mW DC power consumption, and is implemented in the IHP 130 nm SiGe BiCMOS process. The second design is a cascaded 12-stage common-emitter LNA with 45 GHz of 3-dB bandwidth, from 190 GHz to 235 GHz. This design achieves a peak gain of 216 GHz, a sub 10 dB noise figure, DC power consumption of 19.9 mW, and is implemented in GlobalFoundries 22nm FDSOI process.

The thesis of Sidharth Thomas is approved.

Behzad Razavi

Mau-Chung Frank Chang

Aydin Babakhani, Committee Chair

University of California, Los Angeles

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To my late grandmother ...

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VITA

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CHAPTER 1

Introduction

The millimeter-wave (mm-Wave) and THz spectrum is broadly defined as the range of frequencies lying between 0.1 THz - 10 THz. This band has attracted a lot of interest in recent years, with applications ranging from imaging, spectroscopy, and high-speed communications. Fig. 1.1 [1] illustrates the THz spectrum, which lies between RF and optical frequencies.

Traditionally, circuits designed in the RF and millimeter-wave frequencies deal with wavelengths that are orders of magnitude larger than the size of an integrated circuit. The wavelength of a 1 GHz signal in silicon dioxide dielectric is 150 mm. However, at 100 GHz and 1 THz, the wavelengths are 1.5 mm and 150 um, respectively. This suggests the possibility of incorporating distributed structures such as transmission lines and even antennas on chip, opening up huge possibilities. Fig. 1.2 [2] shows how the size of an array scales with frequency. A terahertz array is a million times smaller than a megahertz array.

1.1 THz Generation and Detection

Complex and expensive optical setups drove THz technology for a long time. Fig. 1.3 [3] shows several terahertz sources with the expected output power. Traditionally, expensive optical instruments such as photoconductive antennas, femtosecond lasers, quantum cascade lasers, and even III-V compound semiconductors. With the advancement of silicon transistor technology, commercial fabrication facilities now offer processes with transistors having

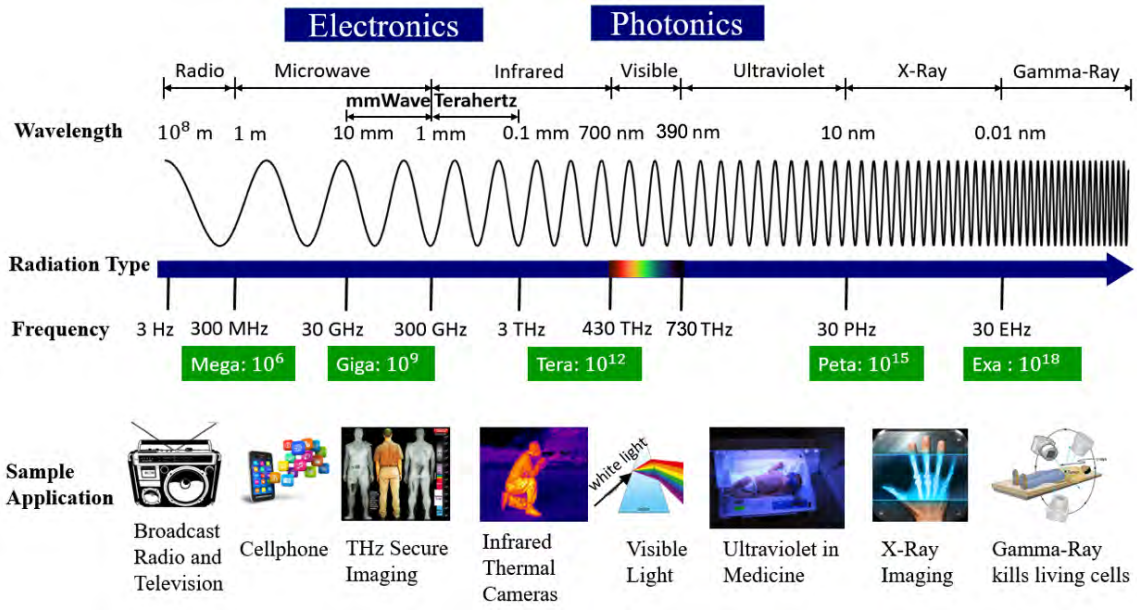

Figure 1.1: The electromagnetic spectrum and its applications

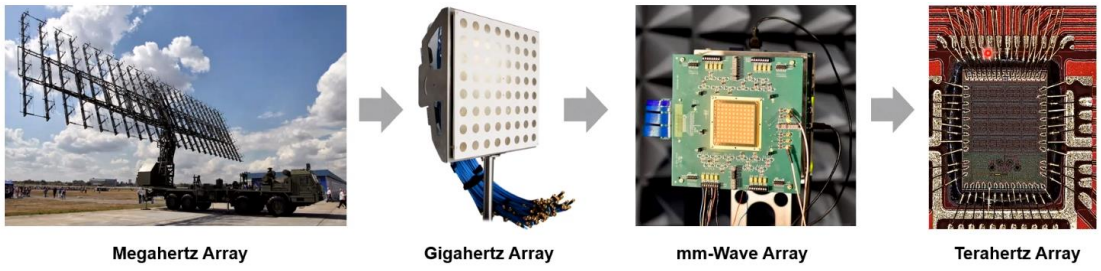

Figure 1.2: A MHz array vs a THz array. Since antenna size scales with wavelength, THz arrays are orders of magnitude smaller than a MHz array.

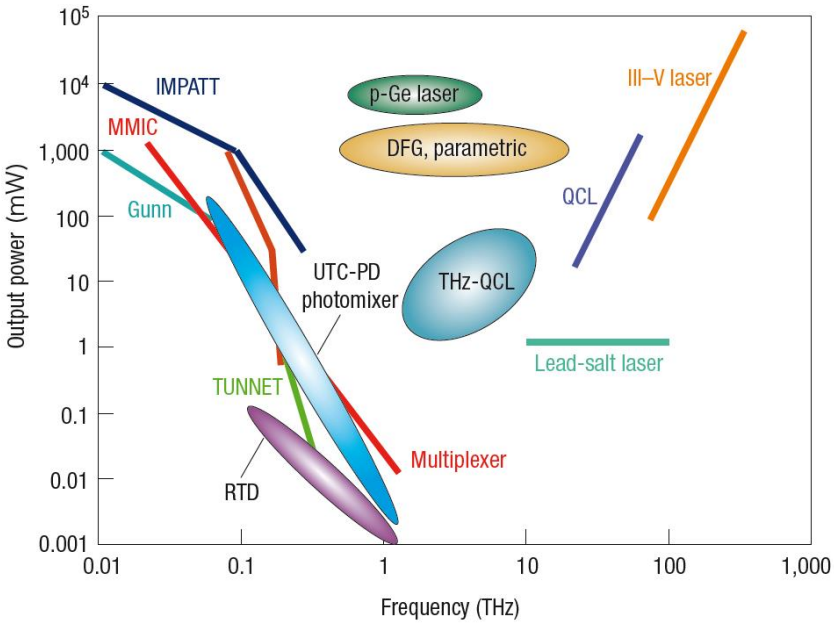

Figure 1.3: Various THz sources and their output power

f_T/f_{max} approaching 500 GHz [4]. This has now enabled silicon THz ICs. Fundamental oscillators have been reported in the literature at 300 GHz [5]. Through innovations in the circuit and antenna side, it is possible to radiate good power beyond Fmax, even at 1 THz in Silicon [6, 7, 8]. Detection at 1 THz has also been achieved [9] by using the plasma wave instability phenomenon in FETs.

1.2 THz Applications

One of the unique applications of THz frequencies is spectroscopy. Due to transitions between rotational states, large polar molecules present unique spectral signatures in THz frequencies. This enables the detection of various gases by studying the transmittance spectrum. A chip-scale spectrometer is demonstrated in [10]. In [11], the authors demonstrate carbon monoxide detection using a custom-designed impulse radiator chip. Transitions between energy bands of a molecule can also be used for precise timekeeping. An ultra-stable chip-scale

molecular clock that uses the spectroscopic properties of carbonyl sulfide is demonstrated in [12]. Different materials have different transmission spectrums in THz frequencies. A machine learning-assisted frequency comb is used for intelligent material classification in [13]. Plasma shows unique spectral properties in the THz region. A frequency comb is used for characterizing the temporal evolution of plasma density in [14].

THz waves travel through most non-metallic and non-polar media. This finds several applications in imaging. The imaging resolution limit, which manifests from diffraction, is inversely proportional to frequency. Thus, compared to using mm-wave waves, THz imaging provides much better spatial resolution. THz waves penetrate common materials such as paper and clothing. This has applications in security screening and concealed weapon detection [15]. Chip scale THz imaging arrays can potentially replace bulky and expensive security scanners. THz also enables non-destructive material classification, which is helpful for the detection of drugs [16]. THz dual-comb hyper-spectral imaging using a custom impulse transmitter and receiver is demonstrated in [17]. High-resolution 3D imaging is possible with THz using synthetic aperture and beamforming algorithms [18]. THz sources typically have a large bandwidth (of several GHz), despite having low fractional bandwidth. The range resolution of FMCW (frequency modulated continuous wave) radars depend on bandwidth. Thus, FMCW radars implemented using THz can achieve even sub-mm range resolutions [19]. THz vibrometry is another sensing technique. It is based on the micro-doppler effect. When reflected from a target, radar waves are modulated by the vibration of the target. These reflected waves can be used to detect the signature of the vibrations. The Micro-doppler effect is more pronounced at THz frequencies. Thus THz based vibrometers have high sensitivity and can precisely pick up even minute vibrations. As an example, multiple frequency tones produced by a speaker were captured and reconstructed using vibrometry, in [20].

THz finds applications in bio-sensing and medical imaging. Due to the low photon energy and non-ionizing properties, THz waves can be a safe substitute for X-rays in medical

imaging. Cancer diagnosis based on THz imaging has been well studied and is a possibility in the future [21]. An emerging application of THz is in bio-sample detection. The size of most bio-samples are magnitudes smaller than the wavelength of THz radiation. A 1 THz wave has a wavelength of 300 um in air. However, this detection sensitivity can be improved by designing metasurface reflectors. By covering a metasurface with a bio-sample, detection of viruses such as MS2, having a size of size 30 nm, has been demonstrated [22, 23].

The available spectrum in RF frequencies is heavily crowded with stringent rules on radiated power levels. THz frequency bands are sparse and aplenty. These bands can be used for high-speed multi-Gbps communication links. According to Shannon's theorem of channel capacity, the achievable data rate in a channel is directly proportional to the bandwidth. Thus, even by employing the most straightforward modulation schemes, THz bands can outperform conventional 4G and even newly deployed 5G links. Since the size of antennas scales inversely with frequency, it is possible to have multi-element chip-scale phased arrays in silicon at THz frequencies. An energy-efficient transmitter array, achieving a data rate of 30 Gbps, with a carrier at 225 GHz, is demonstrated in [24]. A transmitter-receiver with QPSK modulation with a data rate of 10 Gbps is demonstrated in [25, 26]. One of the key issues with using THz transceivers is the increasing atmospheric attenuation at high frequencies. However, the authors in [27] demonstrate that by collimating the signal source, it is possible to transmit a THz signal, generated in a Silicon IC, over tens of meters of distance. This opens up huge possibilities in high-speed, long-distance communication.

1.3 Organization

The rest of this thesis is organized as follows. Chapter 2 describes some fundamentals of mm-wave/THz design. Chapter 3 focuses on the first generation LNA design, which covers 140-220 GHz band. Chapter 4 discusses the second generation LNA, which covers 190-235 GHz band. The thesis is concluded the thesis in Chapter 5.

CHAPTER 2

Fundamentals of mm-wave/THz amplifiers

Circuit operation at mm-wave/THz frequencies is very different from that at analog and RF frequencies. This is mainly due to a combination of parasitic effects which become dominant at these frequencies. This chapter is devoted to explaining the operation of a transistor at mm-wave/THz frequencies. Some of the fundamentals of amplifier design are also explained.

This chapter is written with CMOS as the focus. The concepts described here are also applicable to SiGe HBTs.

2.1 CMOS Technology

GaAs and InP technologies provide much superior speed compared to standard silicon processes. CMOS process, however, offers the advantage of integration. It is possible to make complex digital logic and processing into CMOS ICs.

However, there are several limitations to the CMOS. The substrate resistivity in most digital CMOS processes is of the order of 10-15 Ωcm. This means that signals can easily couple to this low resistivity substrate which can cause significant loss at mm-wave/THz frequencies.

The back-end features in silicon processes (especially advanced nodes) also affect mm-wave performance. While fabricating the BEOL, chemical mechanical polishing is done to planarize the metal layers. This requires uniform density, which is met by adding dummy fillers. These fills can severely de-Q on-chip inductors and transmission lines, which can affect

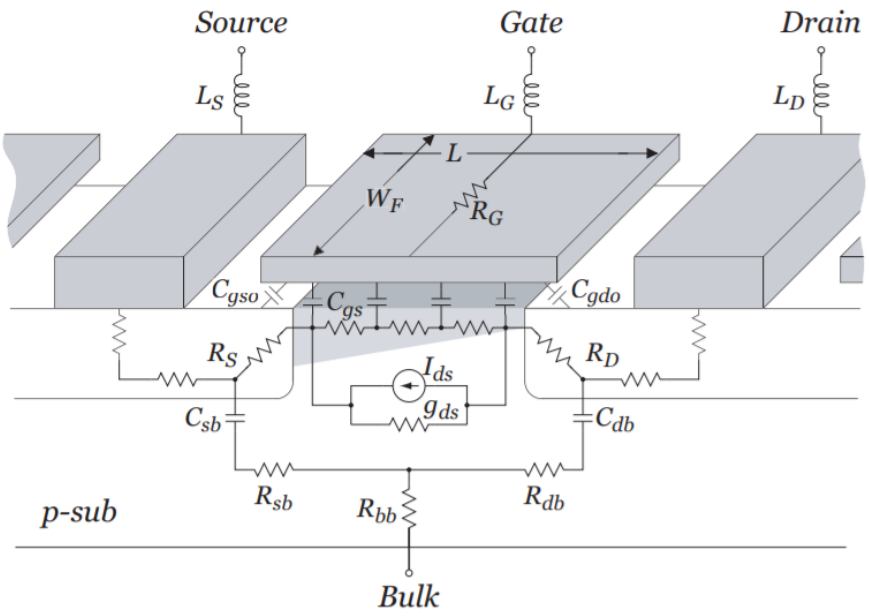

Figure 2.1: NMOS transistor with the associated parasitics

performance. Skin effect, which becomes prominent at high frequencies, can also cause high loss.

2.2 Transistor Design

An NMOS transistor with all the layout associated parasitics is shown in Fig. 2.1 [28]. These parasitics limit the speed of the transistor and ultimately determine high-frequency performance. These are often not present in the base device model. The 22nm PDK used in this process is modeled up to 110 GHz, below the band of interest. EM simulations need to be performed to extract the parasitics for best accuracy beyond this frequency.

Two figures of merit usually characterize the high-frequency performance of a transistor: f_t and f_{max}. The transit frequency, F_t, also called the unity current gain frequency, is the frequency at which the gate to drain current gain becomes unity. It is the frequency at which the hybrid parameter H21 drops to 0 dB. The maximum oscillation frequency, F_{max},

is the frequency where power gain drops to zero. Theoretically, it is impossible to obtain any power gain beyond this frequency. It is also not possible to design oscillators beyond this frequency.

2.3 Amplifier Design

Designing amplifiers at mm-wave/THz frequencies is different from regular analog/RF amplifiers. This is mainly because of two reasons: (1) The power gain is very low at these frequencies. Hence amplifiers require conjugate matching at the input/output and the interface between stages. (2) The physical dimensions of the layout become comparable to the wavelength. Hence transmission line effects need to be addressed, and proper impedance matching is necessary. Some of the terminology associated with amplifier design is described below.

2.3.1 Simultaneous Conjugate Matching

For maximum power transfer between two systems, they need to be conjugate matched at the interface. This is easily done in a single port system. However, in a 2-port system, both the input and output need to be matched. This can be challenging due to the non-unilateral two-port ($S21 \neq 0 or S12 \neq 0$). Here, a simultaneous conjugate match needs to be performed. This has closed-form expressions, which can be found in [29].

2.3.2 Stability

A system that has a reflection coefficient greater than unity is unstable. Conditional stability refers to a system that remains stable when presented with the required impedance. Stability circles can be plotted to see the region of conditional stability. Unconditional stability refers to a system that is stable irrespective of the termination impedance.

Unconditional stability is characterized using the Rollet stability test. The necessary and sufficient requirement for an unconditionally stable system is $K > 1$ and $|\Delta| < 1$.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \tag{2.1}$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{2.2}$$

2.3.3 Unilateral gain

For a linear 2-port system, unilateral gain, also known as Mason's invariant, is as follows:

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{12}G_{21})} \tag{2.3}$$

For any linear, lossless embedding around the 2-port system, the quantity U remains invariant. Thus, it is a fundamental property of the 2-port. At f_{max} U drops to 0 dB. Mason also showed that, U is the maximum power gain that can be obtained if the reverse transmission Y_{12} drops to zero.

2.3.4 Maximum available gain/Maximum stable gain

The maximum transducer power gain, which can be obtained under simultaneous input and output conjugate matching, is given by:

$$G_{T,ma} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{2.4}$$

In this equation, K is the Rollet stability factor.

For a 2-port at the edge of stability, stability factor K is unity. This gives the maximum stable gain (MSG), G_{ms}, which is the figure of merit. For an unconditionally stable 2-port, the maximum available gain (MAG), given by Eqn. 2.5 is the figure of merit. Fig. 2.2 gives the various power gains of a transistor. The sharp change in G_{ma}/G_{ms} at k=1 is the transition from MAG to MSG.

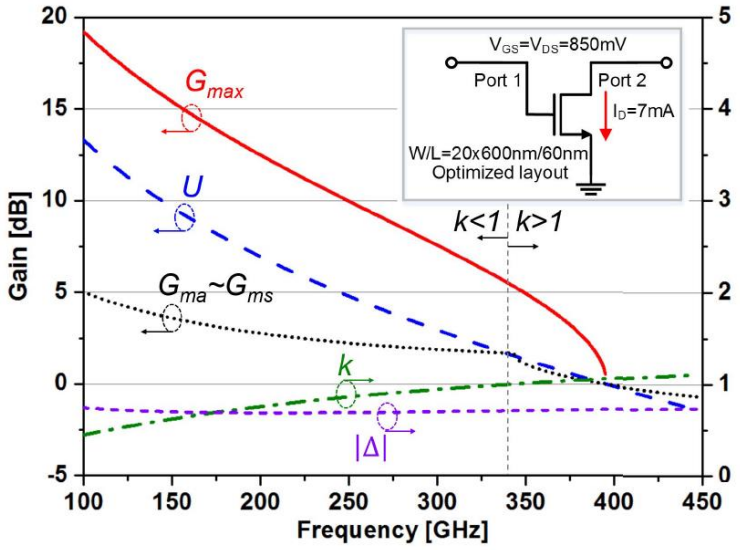

Figure 2.2: Various power gains associated with a 2-port network

2.3.5 Gmax

At very high frequencies, close to the f_{max}, MAG is quite low. Canceling the reverse transmission by resonating out C_{GD}, also called unilateralization, is one technique to get better gain. But this does not improve gain beyond U (Fig. 2.2 [30]). It can be proved that the maximum achievable power gain is much higher than this [31], and is

$$G_{max} = (2U - 1) + 2\sqrt{U(U - 1)} \approx 4U \tag{2.5}$$

The optimal embedding required to achieve this is given in [32].

2.4 Low Noise Amplifier Design

A low noise amplifier (LNA) is typically the first block in a receiver chain. The key role of an LNA is to amplify the received signal without incurring much distortion from the noise. The basic design philosophy of an LNA is explained in this seciton.

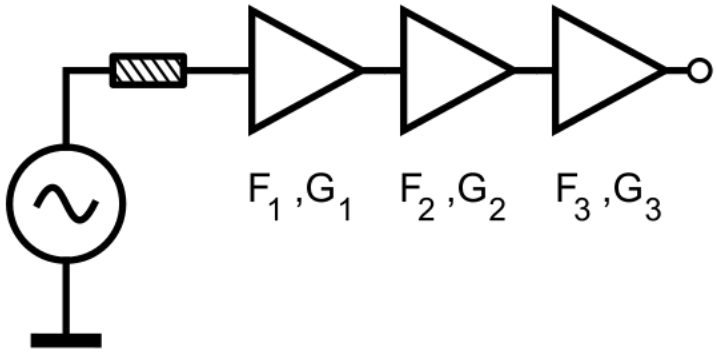

Figure 2.3: Amplifier cascade chain with the associated gain and noise figure

2.4.1 Friis' cascaded noise figure

The first stage in an amplifier chain is the most critical one in setting the noise performance. Consider the cascade of amplifiers given in Fig. 2.3. Assuming simultaneous conjugate matching between all the stages, the overall noise figure, given by the Friis' noise formula,

$$F = F_1 + \frac{F_2 - 1}{G_1} + ... + \frac{F_N - 1}{G_1 G_2 .. G_{N-1}} \tag{2.6}$$

Thus to reduce the noise figure of the overall system, the first block should have a low noise figure and high gain.

2.4.2 Optimum Noise Impedance

The noise figure of a system depends on the input impedance. There is an optimal impedance at which the noise figure can be minimized (derviation: [33]). This choice of optimum source impedance, G_{opt} and B_{opt} (conductance and susceptance), gives the minimum noise figure F_{min}.

For a non-optimal source impedance, the noise figure can be written as:

$$F = F_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \tag{2.7}$$

In eqn. 2.7, G_s and B_s are the source conductance and suseptance, R_n is the noise resistance of the circuit.

It should be noted that the optimal noise impedance of the circuit is unrelated to the conjugate matching impedance. Thus minimizing noise figure can come at the cost of reducing power gain and a poor S_{11}.

CHAPTER 3

A 140-220 GHz LNA in 130nm SiGe BiCMOS

This chapter describes the first generation LNA, designed in the IHP 130 nm SiGe BiCMOS process. A broadband LNA with 80 GHz of measured 3-dB bandwidth is presented here. Several THz circuit design techniques are discussed in this chapter.

3.1 Technology Overview

Some of the salient features of the technology used for this project are described in this section. Understanding these features and their implications is important for efficient design at THz frequencies.

The 130-nm SiGe BiCMOS process from IHP (SG13G2) provides high performance NPN HBTs with f_t/f_{max} of 300 GHz/500 GHz. Fig. 3.1 shows the stack-up of this process [34]. The process offers eight metal layer options stacked on a 280 um, 50 Ωcm silicon substrate. The bottom four copper layers have a thickness of 0.4um, while the upper two copper layers have a thickness of 3um. This is followed by aluminum layers having a thickness of 0.6um and 2.8um, respectively. A MIM capacitor is realized in between the top 2 metals layers, and it offers a density of $2\,fF/um^2$. Thicker metal layers offer less resistance. Also, copper has lesser resistivity than aluminum. Thus, thick copper layers would be the best choice for designing transmission lines and other distributed passives.

Device parasitics are very critical, at THz frequencies, and can reduce the f_t/f_{max} of a device even by 100s of GHz. Thus, it is critical to include parasitics in the device model

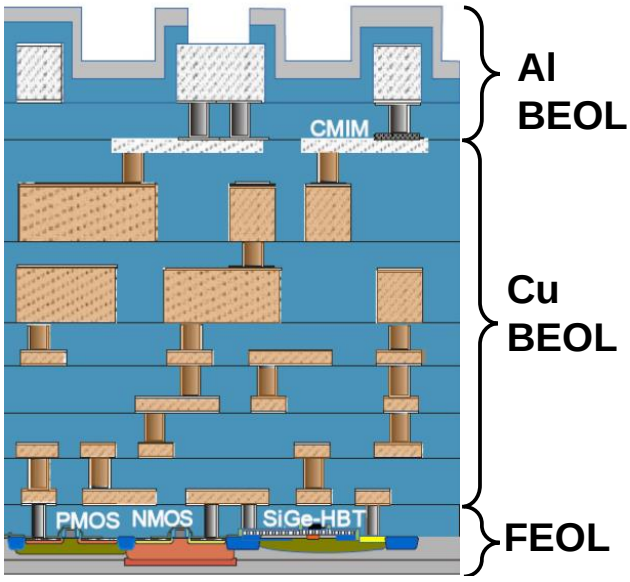

Figure 3.1: Layer stack of the IHP 130nm SiGe BiCMOS Process

while designing circuits. Since the distributed passives are in the ThkCu2 layer, contacts must be brought up from the core BJT to the ThkCu2 layer. Fig. 3.2 (a), (b) shows the layout of an NPN BJT. EM simulations are performed on this layout to characterize the parasitics. These EM extracted parasitics are included, while plotting Fig. 3.2 (c), where the F_{max} is plotted vs current density (J). The F_{max} of this technology node exceeds 450 GHz.

3.2 Circuit Design

An LNA requires unit stages with low noise figure (NF) and high gain. Cascode stages provide superior gain as compared to commmon emitter (CE) stages. However, at frequencies close to $f_{max}/2$, parasitic capacitances at the common node of the CE and the common-base of the cascode present a low impedance path to ground [35]. The noise of the common-base transistor thus manifests at the output, resulting in high NF. Differential CE stages with capacitive neutralization is another popular approach for high gain amplifiers [36].

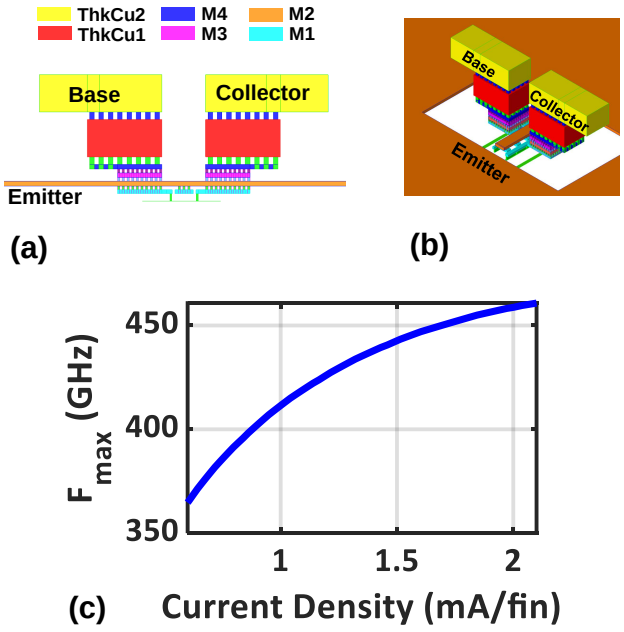

Figure 3.2: (a), (b) Layout of the CE BJT amplification stage (c) F_{max} versus current density

However, differential architectures may require a front-end balun, the insertion loss of which significantly increases the NF. At mm-Wave frequencies, the neutralization capacitors suffer from a low-quality factor, increasing the NF, making capacitive neutralization not feasible.

3.2.1 Optimal Bias Selection

A single-ended CE stage is used as the unit amplification stage in this design. The maximum available gain (G_{max}) and minimum noise figure (NF_{min}) of the CE stage are studied by varying the current density and collector-emitter voltage (V_{CE}). EM extracted layout parasitics are included in these simulations. Fig. 3.3 (a) shows the variation of G_{max} and NF_{min} versus J at 200 GHz. For current densities below 1.1 mA/fin, G_{max} increases faster than NF_{min}. Beyond this bias, NF_{min} increases faster. Thus, the noise-critical stages at the front-end of the LNA are biased at a current density of 1.1 mA/fin. The gain-critical stages are biased at 1.8 mA/fin. It should also be noted that when V_{CE} is reduced from 1.5 V to 0.9 V, the gain decreases by less than 0.6 dB, while the noise performance improves (3.3 (b)

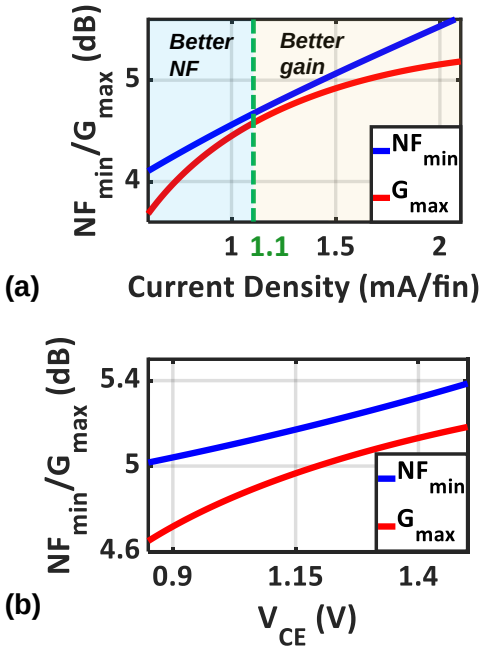

Figure 3.3: (a) NF_{min} and G_{max} versus current density at 200 GHz. G_{max} increases faster than NF_{min} when $J < 1.1mA/fin$ (implying better noise performance), and vice-versa (b) NF_{min} and G_{max} versus V_{CE} at 200 GHz

), providing some flexibility over the choice of V_{CE}.

3.2.2 Amplifier Design

Fig. 3.4 shows the structure of the seven-stage single-ended LNA. Following Friss' formula, the initial three stages are optimized for noise, while the succeeding stages are optimized for gain. The individual stages are stagger tuned to different center frequencies across the WR5 band to improve the overall bandwidth (Fig. 2 (b)). The interstage matching networks are implemented using grounded coplanar waveguide (GCPW) transmission lines (TLs) and metal-insulator-metal (MIM) capacitors. The MIM capacitors have low Q at the frequency of interest. This degrades the NF, and hence, MIM capacitors have been avoided in the noise-optimized stages.

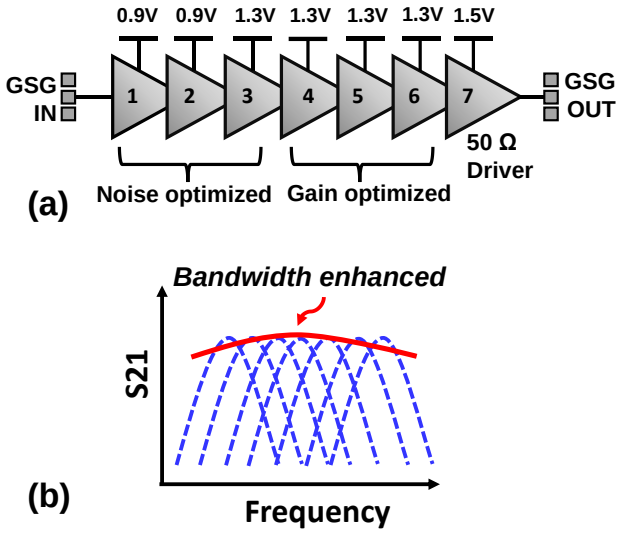

Figure 3.4: (a) Seven stage LNA design (b) Stagger tuning individual stages to increase bandwidth

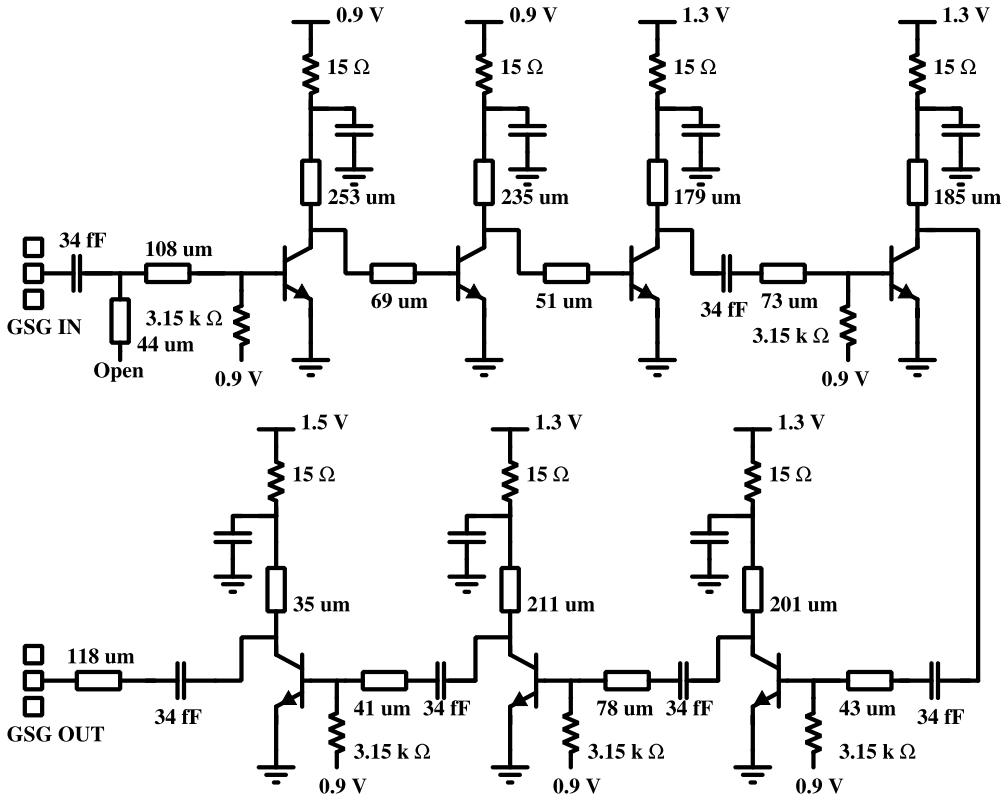

Figure 3.5: Circuit schematic of the seven stage LNA

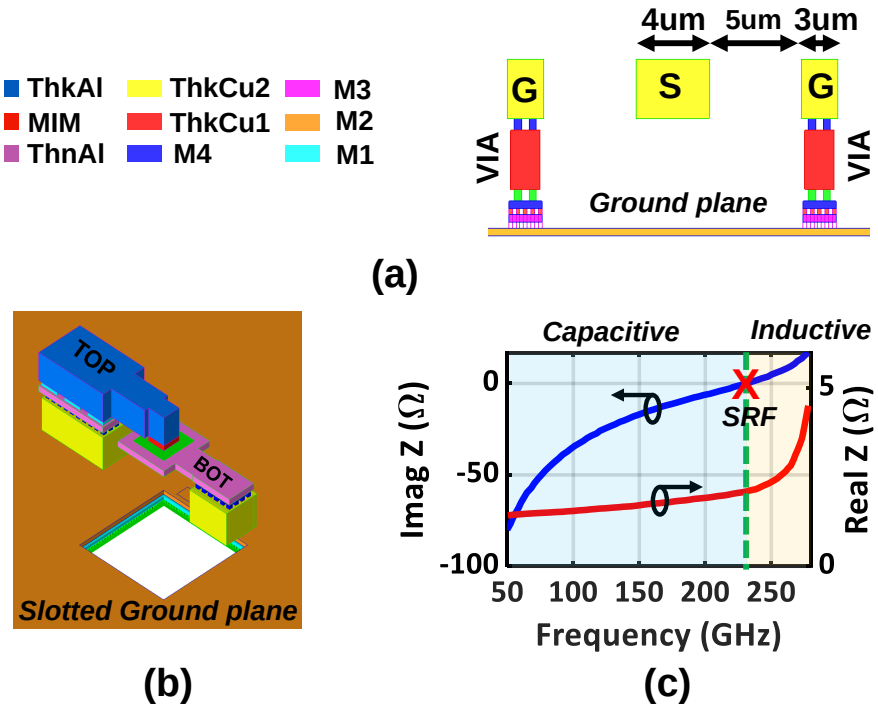

Figure 3.6: (a) Cross section of custom GCPW TL (b) Layout of MIM capacitor (c) Resistance and reactance of MIM capacitor from EM simulations

Fig. 4.4 shows the schematic of the proposed WR5 LNA. The initial three stages of the cascade chain are DC coupled. The current density for these stages is set to 1.1 mA/fin by adjusting V_{BE}. Due to DC coupling, V_{CE} of the previous stage is also set to V_{BE}. However, the flexibility in choosing V_{CE} (Fig. 1 (c)) ensures that this choice of V_{CE} does not affect the NF. The subsequent four stages in the cascade are AC coupled to control V_{BE} and V_{CE} individually. These stages are biased at a J of 1.8mA/fin to maximize the gain performance.

3.2.3 Circuit Design - Passives

All the passive structures used in the design are extensively EM simulated using Keysight Momenutm and Ansys HFSS. Fig. 3.6 (a) and (b) show the structure of the 50 Ω GCPW transmission line and the MIM capacitor. EM simulations show that at 180 GHz, the

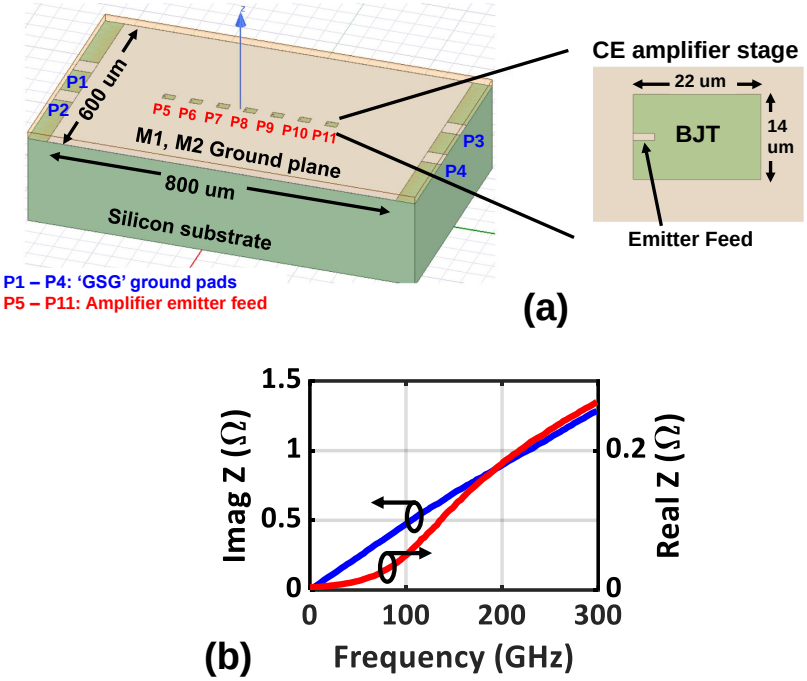

Figure 3.7: (a) The EM simulated ground structure. It consists of eleven ports. (b) Simulated resistance and reactance of the ground network

designed 34 fF MIM capacitors have a quality factor of 6, with an effective series resistance of 1.8 Ω (Fig. 3.6 (c)). Hence AC coupling MIM capacitors were avoided in the initial noise-sensitive stages.

Non-zero ground impedance can degenerate the single-ended CE stage, affecting gain and bandwidth. To reduce degeneration, a low-impedance ground plane is implemented across the entire chip (Fig. 3.7 (a)) using the bottom metal layers M1 and M2. These layers need to be slotted to meet the layout density requirements. They are then offset from each other to ensure a continuous ground plane. EM simulations are performed to calculate the impedance seen at the emitter feed of unit amplification stages. Simulations results (Fig. 3.7 (b)) show that this impedance is close to 1 Ω at 200 GHz, resulting in minimal degeneration effects.

Power traces can behave as TLs at mm-Wave frequencies, causing stability issues. To alleviate this, low characteristic impedance (Z_0) 'zero-ohm transmission lines' (ZOTLs) are

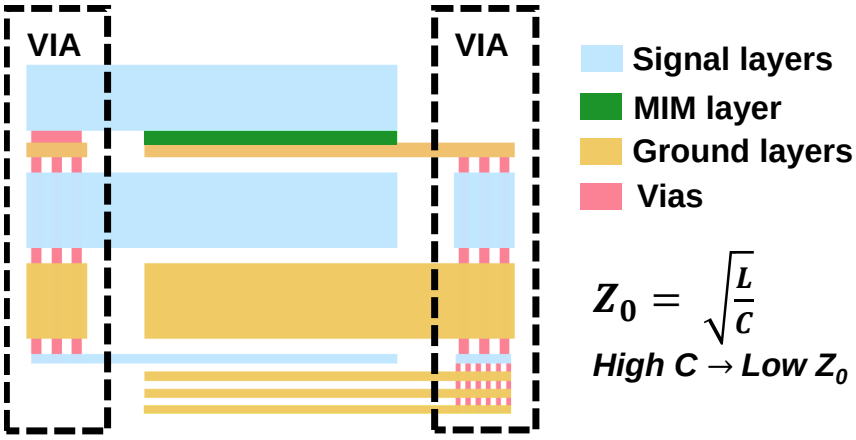

Figure 3.8: Layer stack-up of the custom zero-ohm transmission line (ZOTL)

used to implement power traces. ZOTLs have a stacked structure with alternate signal and ground layers and a MIM dielectric layer drawn between the top two metal layers, reducing Z_0 (Fig. 3.8). The low Z_0 guarantees that the ZOTL has low input impedance, irrespective of the termination, and eliminates the transmission-line effects of the power traces. ZOTLs are also loaded with lumped MIM capacitors of different sizes to provide adequate decoupling across a broad range of frequencies.

3.3 Measurements

The designed LNA was fabricated in a 130nm SiGe BiCMOS process. The die area with and without including pads is 0.7 mm^2 and 0.48 mm^2, respectively. Fig. 3.9 shows a micrograph of the fabricated IC. The measured DC power consumption of the IC is 46 mW.

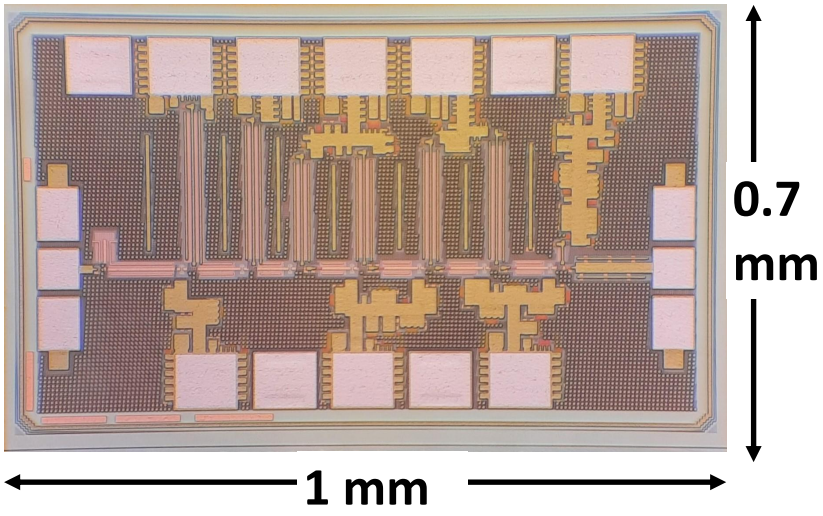

Figure 3.9: Chip micrograph

3.3.1 Calibration techniques - TRL/LRL

3.3.2 Measurement Results

The LNA is tested using ground-signal-ground (GSG) probes. Fig. 3.10 shows the small-signal test setup. A Keysight E8364B PNA network analyzer is connected to OML WR5 VNA extension modules to probe-test the chip. WR5 probes with 75um pitch from Cascade Microtech are used, and the probes are connected to the VNA extenders through WR-5 S-bends.

Before measuring the S-parameters of the DUT, calibration needs to be performed. At lower mm-wave frequencies, SOLT (short-open-line-termination) is popularly used. However, it is tough to design accurate opens and terminations at THz frequencies. Hence TRL (thru-reflect-line) calibration is more popular.

A two-step calibration is performed for this measurement. First, the impedance standard substrate (ISS 005-018) provided by the probe vendor is used. Using this as a reference, the setup is again calibrated using on-chip custom-designed TRL structures. This removes the

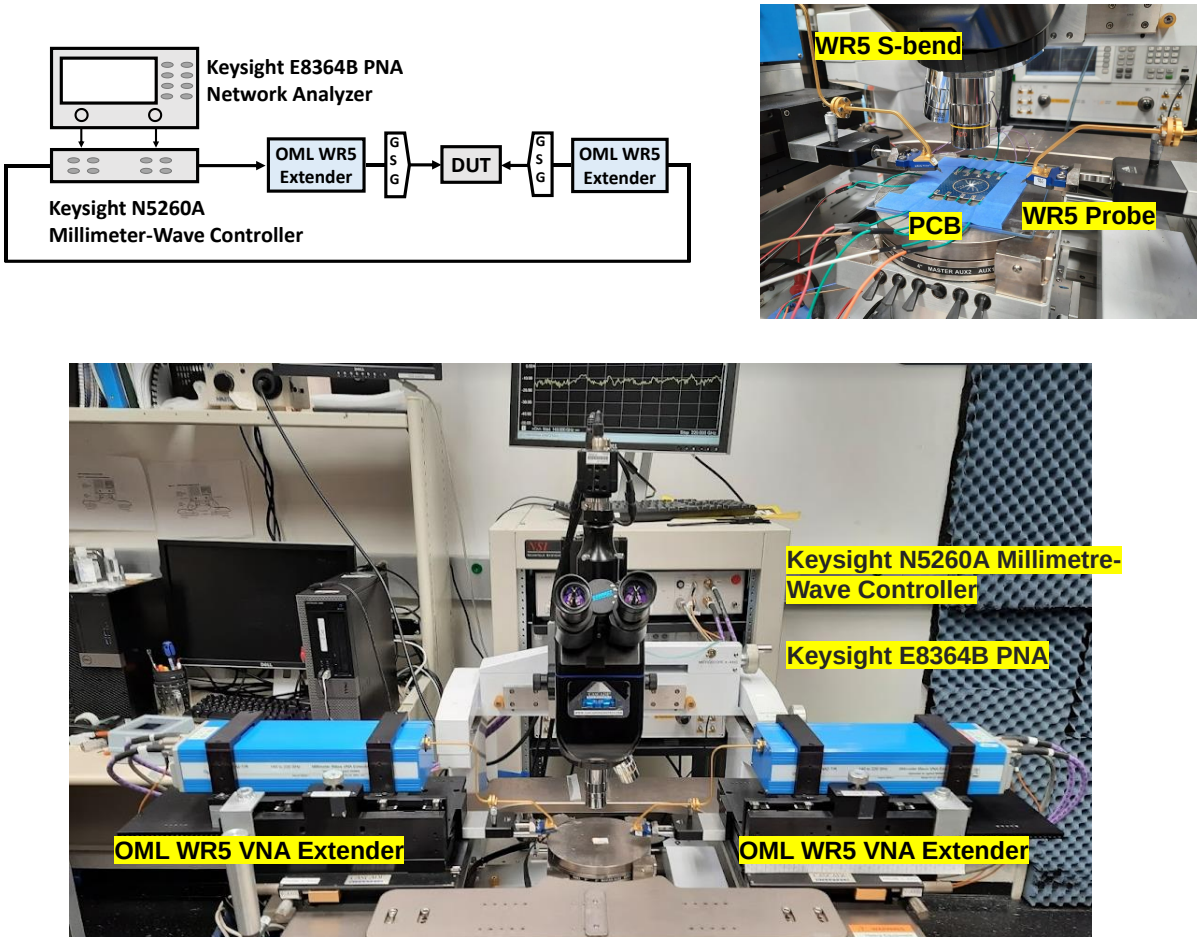

Figure 3.10: Small signal wafer-probing measurement setup, with VNA extenders

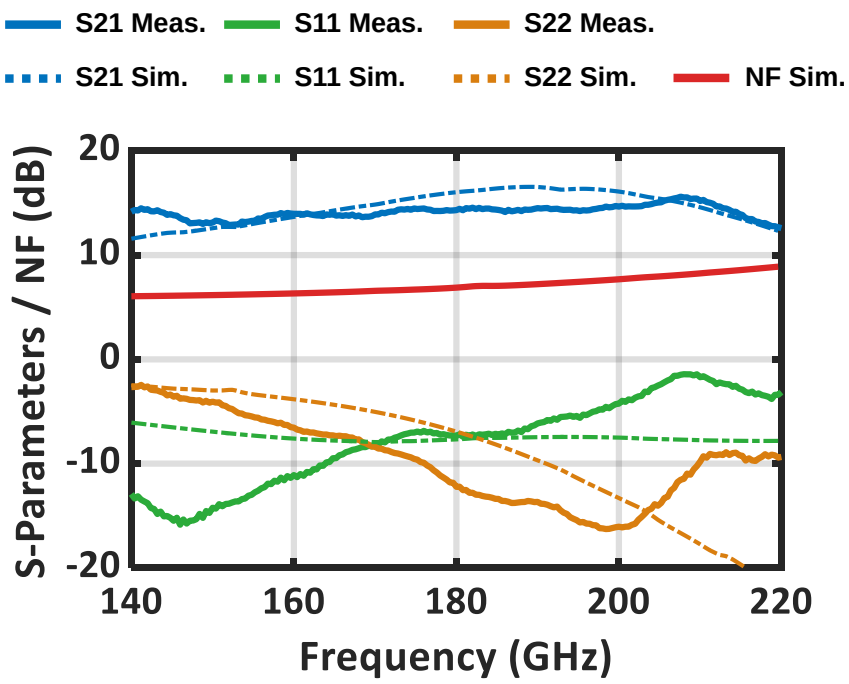

Figure 3.11: Measured s-parameter results, and simulated noise figure in the WR5 band

effects of the bond pads. Upon measurements, it was shown that TRL calibration gave physically wrong results for a 50 Ω line ($S11 > 0dB$, $S12 \neq S21$). We suspect probe-to-probe coupling, which can take place while probing the thru (since the probes have to be very close while measuring thru). Hence instead of TRL, LRL (line-reflect-line) calibration is performed, where two lines of different lengths are used.

The measured s-parameters are plotted in Fig. 3.11 The LNA shows a peak measured gain of 15.5 dB at 207 GHz. This is in close agreement with the simulation results, and any deviation would have resulted from active-device modeling inaccuracies and the effect of filler cells. The measured 3-dB bandwidth covers the entire WR5 frequency range, from 140-220 GHz. This is a fractional bandwidth of over 44%. The measured reverse isolation ($|S_{12}|$) is greater than 35 dB, and the LNA is unconditionally stable through the measured frequency range. Simulation results show an NF of 6 dB, 6.8 dB, and 8.8 dB at 140, 180, and 200 GHz, respectively (Fig. 7 (b)).

References	This Work	[1] T-MTT'16	[2] JSSC'14	[3] JSSC'20	[4] T-MTT'17	[5] MWCL'21	[6] EUMIC'17
f_0 (GHz)	180	183	210	190	155	230	190
Gain (dB)	15.5	17.2	18	23.5	15.7	21.8	24.7
3 dB BW (GHz)	> 80 (Beyond 140-220)	35 (165-200)	15 (205-220)	34	23 (143-166)	35 (209-244)	16
Fractional BW (%)	> 44.4	19	7.1	17.8	14.8	15.2	8.4
Noise Figure (dB)	6* @140 GHz 6.8* @180 GHz 8.8* @220 GHz	8	11-12 **	7.7*	8.5	10.5*	9.8*
P_{DC} (mW)	46	16.1	44.5	3.2	32	66	37.2
Area (mm^2)	0.48	0.765***	0.26	1.05***	0.34	1.53***	0.48
Technology	130 nm SiGe HBT	130 nm SiGe HBT	32 nm SOI CMOS	130 nm SiGe HBT	28 nm FDSOI CMOS	130 nm SiGe HBT	130 nm SiGe HBT

** Simulated ** System measurement *** Total area*

Table 3.1: Comparison among state of the art sub-THz LNAs

Table 3.1 compares the performance metrics of this design with other existing LNA designs [35, 36, 37, 38, 39, 40]. A record fractional bandwidth of 44% is achieved, with a sub-7 dB NF at the center of the WR5 band. To the best of the authors' knowledge, this design reports the highest 3-dB bandwidth, of over 80 GHz, among all mm-Wave LNAs. The noise figure obtained is also better than other designs at these frequencies.

3.4 Conclusion

A broadband LNA has been demonstrated in a 130 nm SiGe BiCMOS process. Compared to state-of-the-art, this paper achieves the widest bandwidth of 80 GHz, covering the entire WR5 band. This is obtained through stagger-tuned interstage matching networks. The designed LNA achieves a low noise figure of 6.8 dB at 180 GHz through an optimal selection of the device operating point. Due to its broadband nature, this LNA can be used as a WR5 band receiver or phased-array front-end, incorporating multiple bands and channels.

CHAPTER 4

A 190-235 GHz LNA in 22nm CMOS

This chapter describes the second generation LNA, designed in the GlobalFoundries 22nm FDSOI process. A broadband LNA with 45 GHz of 3-dB bandwidth is presented here. Several THz circuit design techniques are discussed in this chapter.

4.1 Technology Overview

Some of the salient features of the technology used to design the LNA are described in this chapter. The GlobalFoundries 22nm process comes with a fully depleted silicon on insulator (FDSOI) MOSFETS. Fig. 4.1 (c) shows an NFET transistor from this process. Notice the presence of the buried oxide layer (BOX) below the channel. The transistors and enclosed by P-wells and deep N-wells, which allow independent body biasing. The p-well acts as a 'back-gate' and can be used for the threshold voltage modulation. Since there is no source/drain to substrate diodes (such as in bulk processes), the back gate voltage can be increased beyond the VSS to reduce the threshold. Moreover, compared to a bulk process with similar dimensions, FDSOI provides low leakage and bias independent source-drain capacitances. The BEOL comes with ten layers, including one thick copper layer (3.3 um thickness) and one thick Aluminium layer (2.8 um thickness). It also has a dedicated mm-wave library with optimized device layouts and on-wafer characterization up to 110 GHz. As mentioned in the previous chapter, device parasitics can severely impact the f_t/f_{max} of a transistor. Thus, it is critical to include parasitics in the device model while designing circuits. Fig. 4.1 (a) shows the layout of an NFET transistor from the mm-wave library. This transistor

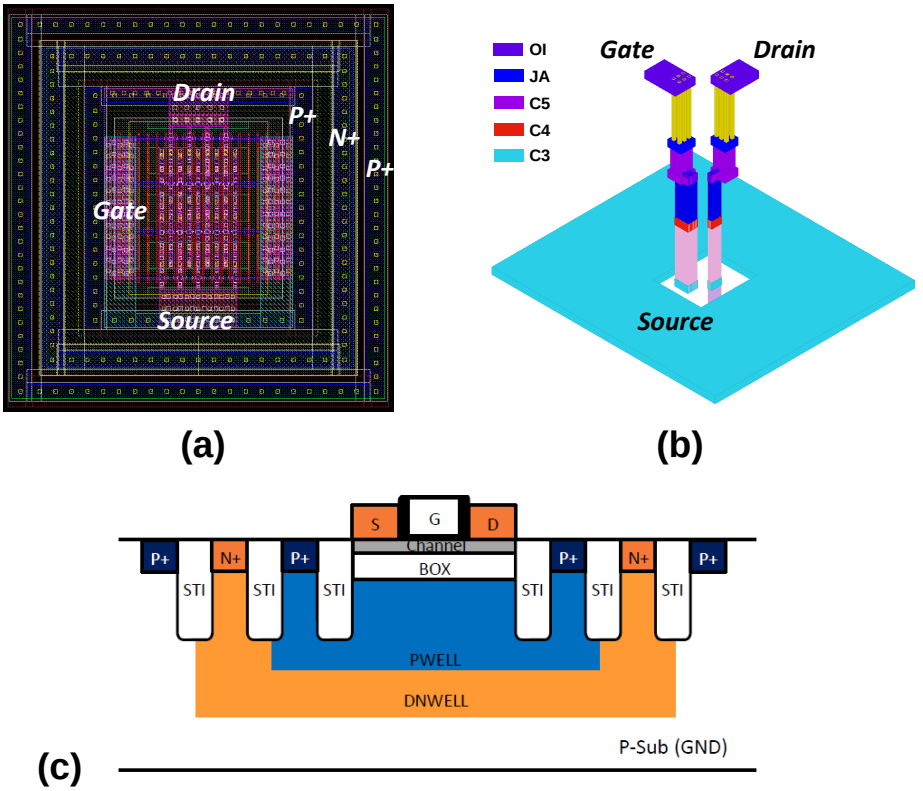

Figure 4.1: (a) Layout of the NFET in the mm-wave library. (b) Gate Drain contacts and ground shield which would be surrounding the core transistor (c) FDSOI NFET transistor

has a length of 20nm, finger width of 300nm, with eight horizontal fingers in 3 rows. The layout is optimized for mm-wave performance, using a double contact gate and increased gate-to-contact spacing for lowering the parasitics. The parasitics till the 5th layer, C3, are included in the model.

The gate and drain contacts on the core transistor used for EM simulations is shown in Fig. 4.1 (b). The gate and drain are brought up to the 9th layer OI. This is required since all matching network capacitors and transmission lines are in the OI layer. The top layer LB is avoided since that layer has higher sheet resistance than OI. A ground plane consisting of C3 covers the region surrounding the NFET, and the source is connected to it.

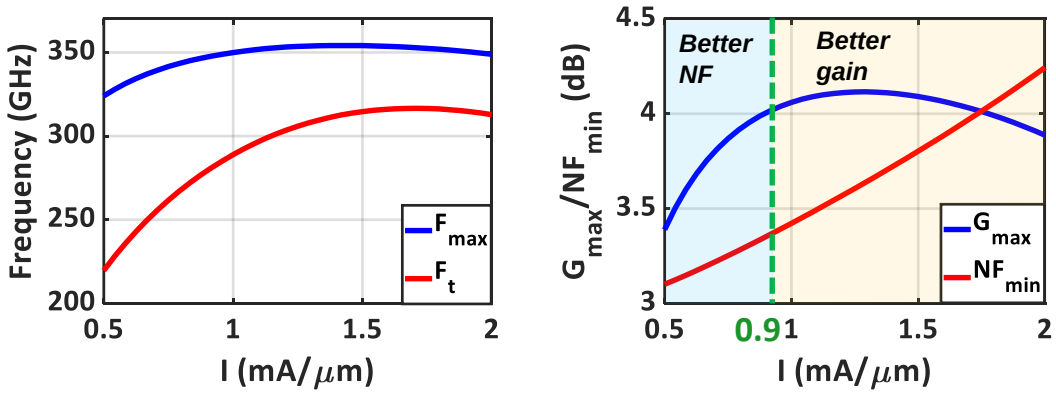

Figure 4.2: (a) F_t and F_{max} versus current density (b) G_{max} and NF_{min} versus current density at 220 GHz. For current densisties below 0.9 mA/um, G_{max} increases faster than NF_{min}, suggesting better noise performance, and vice versa.

Fig. 4.2 (a) shows the simulated F_t and F_{max} of the transistor. The EM extracted parasitics are included in this simulation. Both F_t and F_{max} peak, at different current densities, and then drop. The peak F_{max} of this technology node exceeds 350 GHz.

4.2 Circuit Design

As mentioned in Chapter 3, cascode topologies do not fare well while designing LNAs, close to f_T. This is because of the parasitic capacitance at the intersection of the common source and common drain transistor. Differential topologies require a front-end balun, whose loss comes directly into the noise figure. Hence common source stages were used in this design.

4.2.1 Optimal Bias Selection

Once the topology is chosen, the next step is to choose the bias. Fig. 4.2 (b) shows the variation of G_{max} and NF_{min} versus current density. For current densities less than 0.9 mA/um, G_{max} increases faster than NF_{min} suggesting better noise performance. Based on the Friss formula, the initial stages of a cascade contribute to noise performance. Hence the

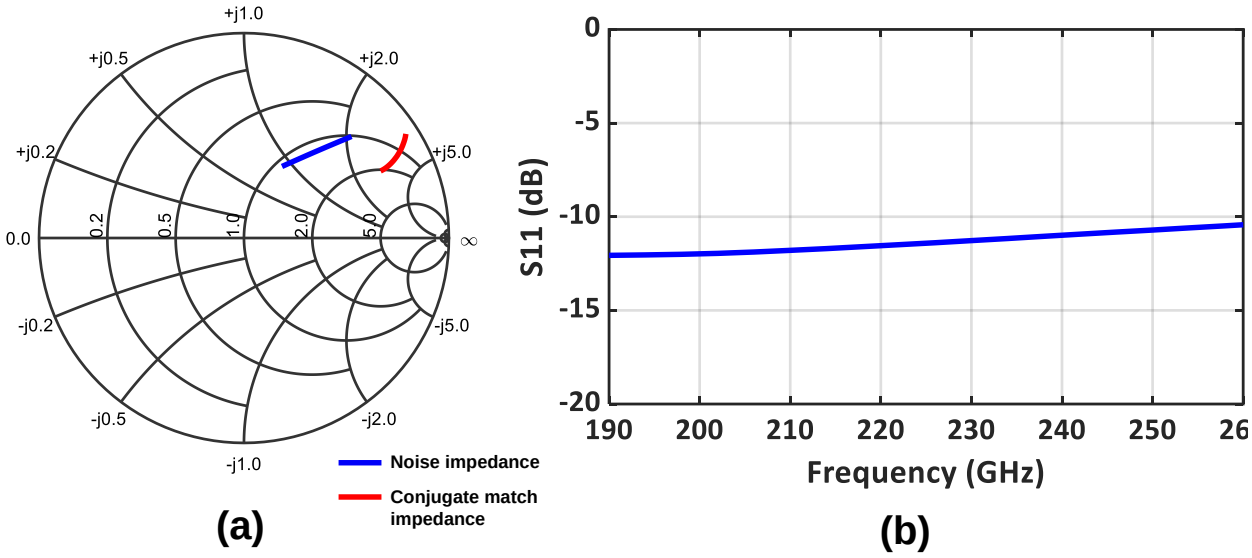

Figure 4.3: (a) Noise impedance of a common source stage, and the impedance satisfying simultaneous conjugate match (b) S11, assuming the impedance is matched to the noise impedance, at all frequencies

initial noise-sensitive stages are biased at 0.9 mA/um. The later stages are biased at a higher current density of 1.25 mA/um for better gain. Also, note that the initial noise-sensitive stages are DC coupled to avoid the noise coming from lossy DC blocking capacitors.

4.2.2 Amplifier Design

The next step in designing the LNA is to choose the input impedance. While designing an LNA, there is a trade-off between noise figure and gain. As explained in Chapter 2, the best noise performance is observed for a source impedance equalling the noise impedance. The best gain performance is obtained for a source impedance satisfying simultaneous conjugate matching. These impedances, for a common source stage, are plotted in Fig. 4.3 (a). EM simulated transistor parasitics are included in this simulation. It can be observed that these impedances are close for the common source stage under consideration. Fig. 4.3 (b) is a plot of the S11, assuming the input is set to the noise impedance at all frequencies. It can

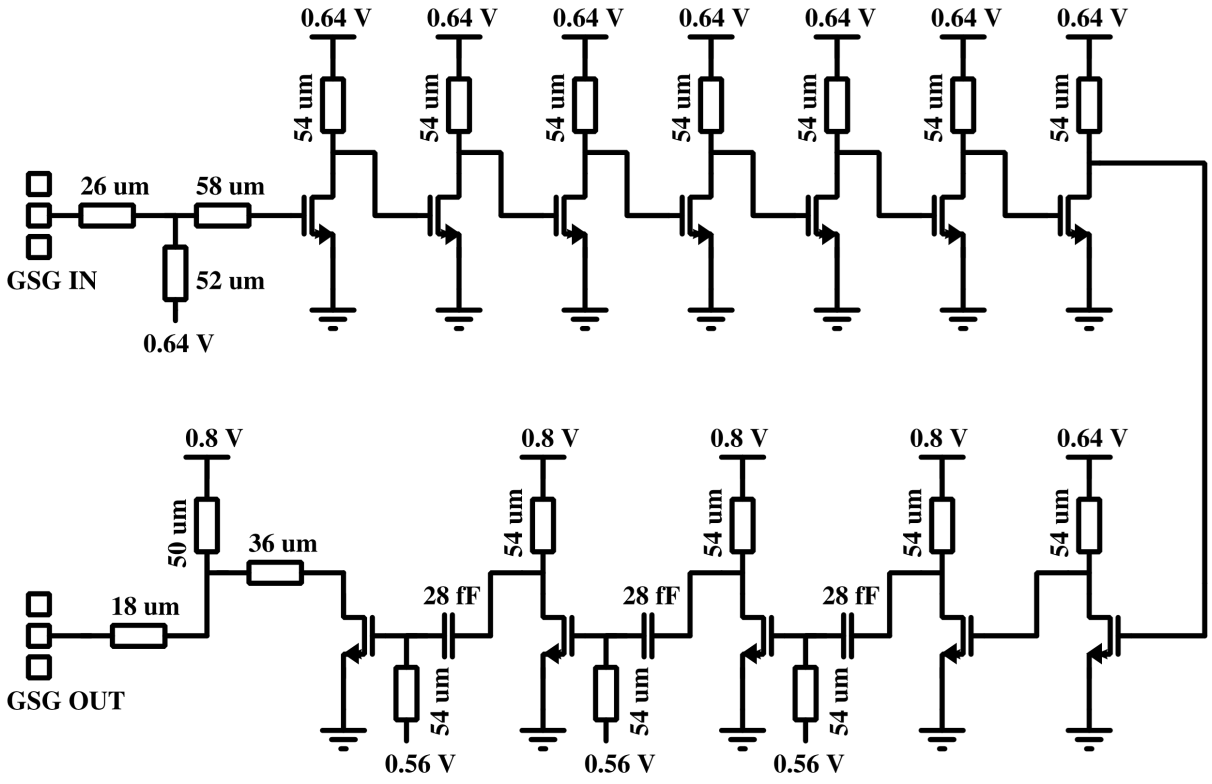

Figure 4.4: Schematic of the 12 stage LNA

be observed that the S11 is below -10 dB. Hence, the input impedance of the first stage is matched to the noise impedance. The output impedance is matched to the simultaneous conjugate matching impedance. A similar procedure is followed for the remaining noise-sensitive stages.

Fig. 4.4 shows the schematic of the 12 stage LNA. The initial nine stages of the LNA are designed using the procedure described in the above paragraph. These stages are all DC coupled to improve noise performance. These stages give good gain and noise performance. Fig. 4.5 shows the gain profile at the output of the LNA stages. It can be observed that, after stage 8, the gain peaks slightly below 200 GHz but rolls off sharply. This is due to the inherent roll-off in transistor G_{max}, making this design narrowband.

The final 3 AC coupled stages are tuned to the simultaneous conjugate matching impedance

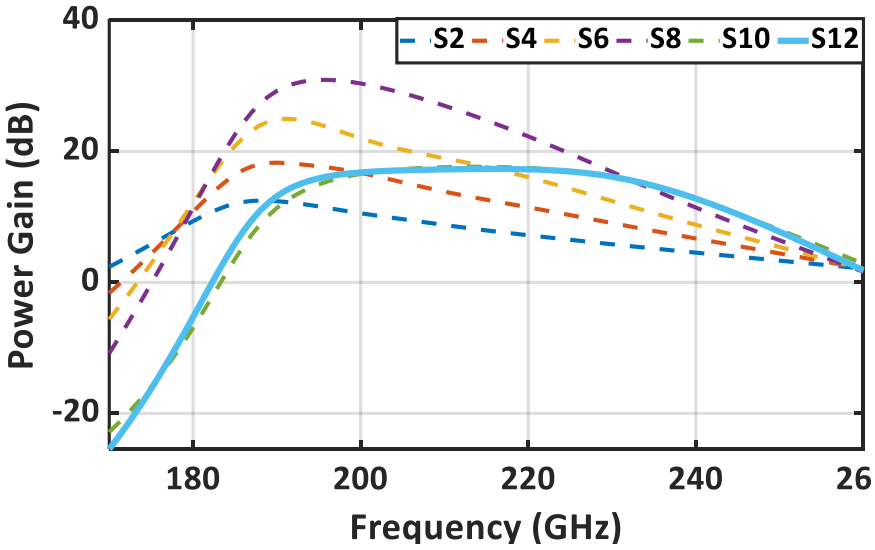

Figure 4.5: Power gain after each of the stages. S2, S4, S6, S8, S10, S12 represent the gain at the output of the 2nd, 4th, 6th, 8th, 10th and 12th stage respectively.

at 230 GHz to combat this. This flattens the gain profile and improves the 3-dB bandwidth. The final 3-dB bandwidth at the end of the cascade chain is 45 GHz, from 190 GHz to 235 GHz.

4.2.2.1 Circuit Design - Passives

The foundry models for passives are often unreliable, with unrealistically high Qs at mm-wave/THz frequencies. These have to be modeled using an EM simulator. All the passive structures used in the design are extensively EM simulated using Keysight Momenutm.

A ground plane covers the entire chip, using layers C1, C2, and C3. This ensures a proper low impedance path to ground. This also prevents unnecessary substrate coupling and loss. The ground plane is slotted to meet the local and global density requirements.

The 22nm process does not offer a MIM dielectric layer. Hence MOM capacitors are used. Fig. 4.6 (a), (b) shows the layout of the custom-designed MOM capacitor. The MOM fingers

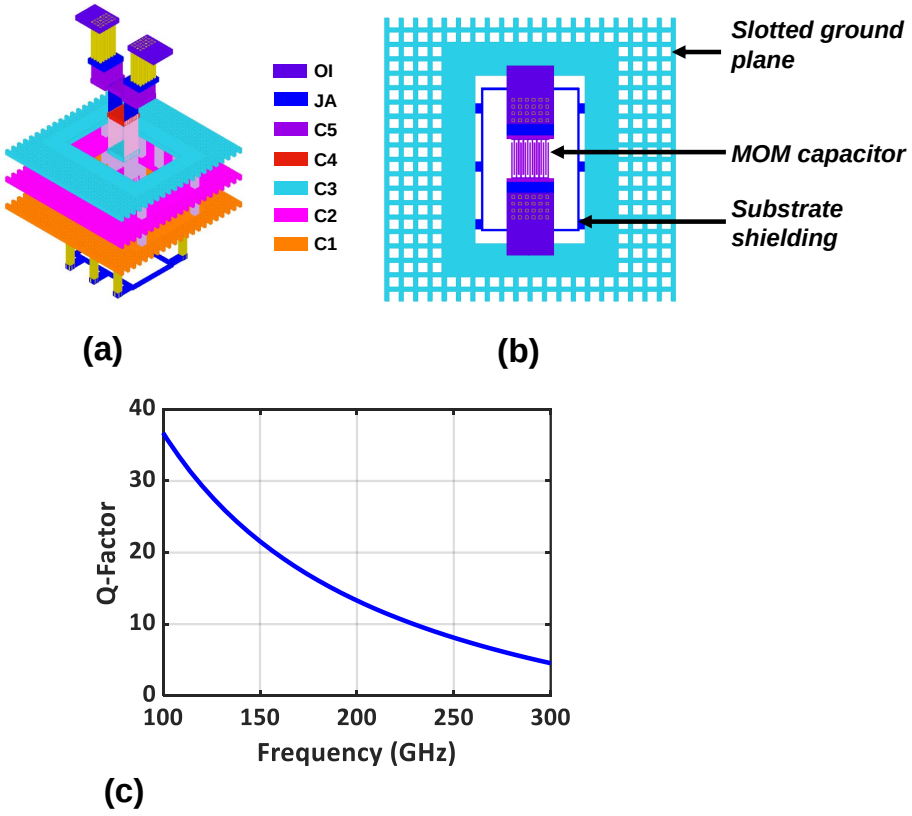

Figure 4.6: (a) Layout of the MOM capacitor (b) Top view of the MOM capacitor (c) Simulated Q factor of the MOM capacitor

are spread across five layers, C1, C2, C3, C4, and C5, to reduce the parasitic resistance. A slotted ground plane is also included in this simulation. Since these capacitors are designed for AC coupling, they should have very little shunt capacitance to the ground. Hence the ground plane is kept at a distance from the central MOM capacitor. Fig. 4.6 (c) shows the simulated Q factor of the capacitor.

The matching networks are designed using transmission lines. Hence, it is necessary to choose low-loss lines. Microstrip lines are quite lossy at these frequencies due to lack of side shielding. Coplanar waveguides, too, are lossy due to lack of substrate shielding.

Grounded coplanar waveguides (GCPW) are a good choice. Fig. 4.7 (a) shows the structure of a GCPW. It comes with a central signal layer and two side shields. The side

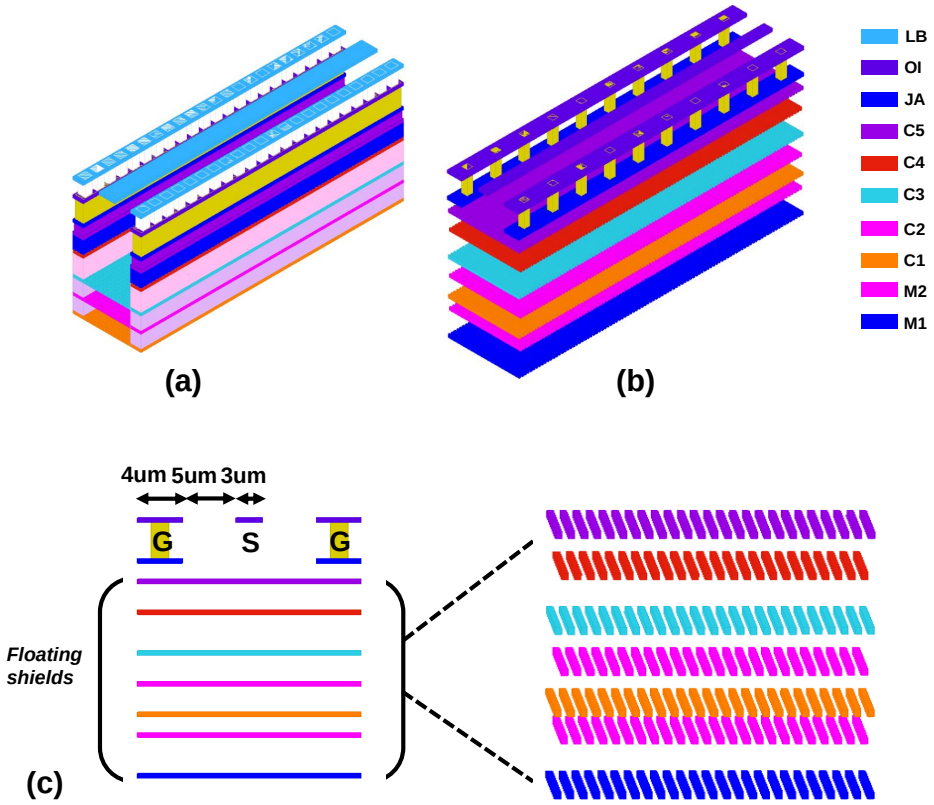

Figure 4.7: (a) Grounded coplanar waveguide (GCPW) (b) Slow wave coplanar waveguide (SCPW) (c) Cross section of the SCPW, highlighting the floating metal layers

shields are connected to a bottom ground layer, though extensive vias. However, GCPW has certain issues, especially in advanced CMOS nodes. Advanced nodes have very tight local density rules. To meet these requirements, dummy filler cells need to be added, which can severely de-Q the lines. In 4.7 (a), dummy cells in layers JA, C5, C4 need to be added inside the GCPW.

Another alternative to GCPW is using slow-wave coplanar waveguides (SCPW). Fig. 4.7 (b), (c) shows the structure of an SCPW. An SCPW has the typical structure of a CPW but with additional "floating" metal shields. These metal shields are not connected to any DC and are hence floating. In fact, these shields are made of small strips of metal (as seen in the inset in Fig. 4.7 (c)). These strips are offset in each layer to shied the top signal line

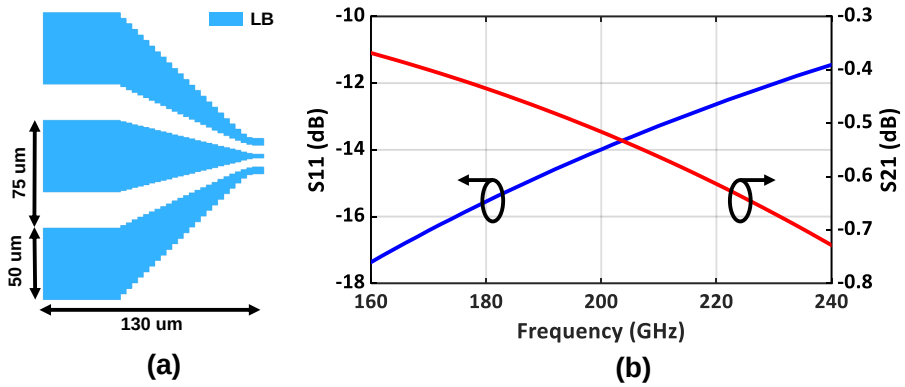

Figure 4.8: (a) Layout of the cutom GSG bondpads (b) EM simulation results: return loss and insertion loss of the bondpad

from the lossy substrate. Since floating shields of all layers are added, there will not be any density violations. Due to the "slow-wave" action, SCPW has a higher phase constant β, which reduces the length of the line required, thus reducing insertion loss of the matching network.

The designed LNA is meant to be probed with GSG probes having 75 um pitch. Fig. 4.8 (a) show the structure of the custom-designed GSG bond pads, with the taper. Fig. 4.8 (b) shows the EM simulation results. The simulated S11 of the bond pad is below -10 dB, suggesting good matching. The insertion loss is below 1 dB. This loss will be de-embedded during measurements.

4.3 Simulation Results

The designed LNA was fabricated in a 22 nm FDSOI process. The die area with and without including pads is 0.35 mm^2 and 0.09 mm^2, respectively. Fig. 4.9 shows a micrograph of the fabricated IC. The simulated DC power consumption of the IC is 19.9 mW.

Fig. 4.10 shows the simulated s-parameters. The simulated 3 dB bandwidth is 45 GHz, from 190 GHz to 235 GHz. A peak gain of 17.3 dB is obtained at 216 GHz. The simulated

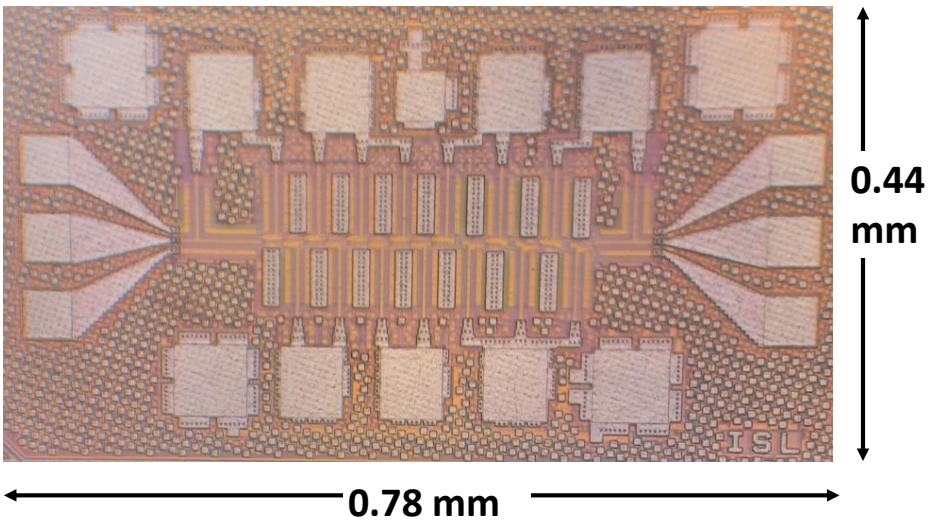

Figure 4.9: Die Micrograph

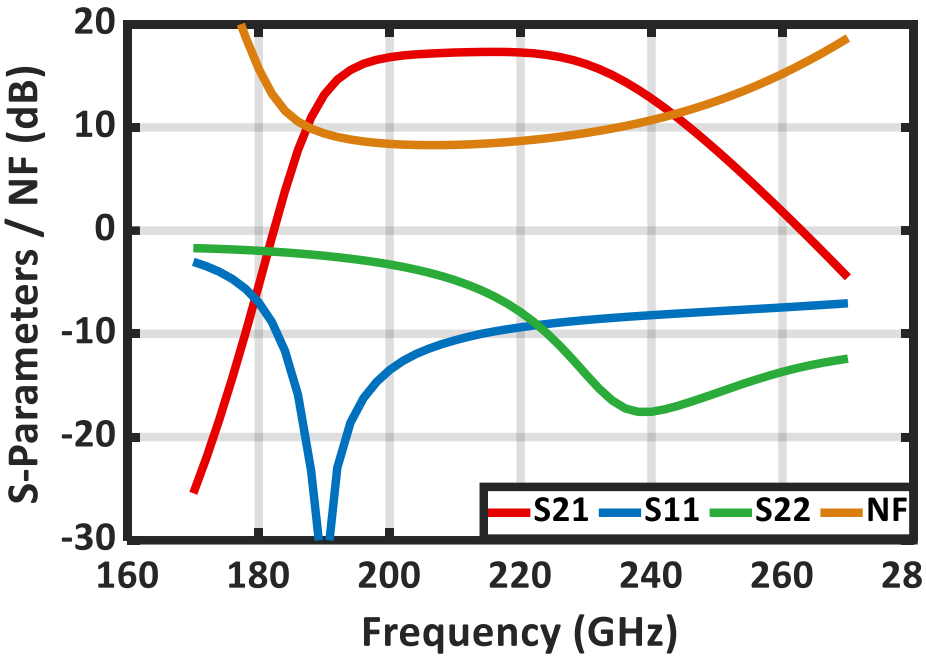

Figure 4.10: Simulated s-parameters and noise figure

noise figure is flat and is below 10 dB within the bandwidth. The minimum noise figure is 8.28 dB at 206 GHz.

This design has the highest bandwidth and least noise figure among all CMOS LNAs above 200 GHz based on the simulated numbers. The VNA measurements for this chip are currently being performed.

CHAPTER 5

Summary and Future Directions

In this thesis, two broadband low noise amplifiers are presented. The first generation LNA was designed and fabricated in IHP 130 nm SiGe and has 80 GHz bandwidth, covering the entire WR5 band, from 140 to 220 GHz. It has a noise figure of 6.8 dB at 180 GHz. The second-generation LNA was designed and fabricated in the GlobalFoundries 22nm FDSOI process. It has a 45 GHz bandwidth, from 190 to 235 GHz, and a sub-10 dB noise figure through the band. Several design strategies for mm-wave/THz design are also analyzed in this thesis. Measurement and calibration techniques are also discussed.

This project's future research work involves performing small-signal VNA measurements on the 22nm LNA. This measurement is currently underway. Also, noise figure measurements need to be performed on both the LNAs. The Y-factor method is typically used for this. Noise measurements are challenging and require a noise source and low-loss mixer. These pieces of equipment are currently being procured.

Potential future directions involve building a complete receiver with the proposed LNAs. This can have a broadband on-chip antenna for signal reception. A mixer and baseband amplifiers can be designed to complete the receiver system. Radiometric receivers with power detectors can also be designed. A large bandwidth is advantageous in such systems. These ideas can be expanded further by developing a phased array with advanced features such as 2D beam-steering.

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