UNIVERSITY OF CALIFORNIA SAN DIEGO

# Hybrid DC-DC Converters for Smart Integrated Power Delivery

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Casey L. Hardy

Committee in charge:

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2022

The Dissertation of Casey L. Hardy is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

To my wife, Molly.

In memory of Dad, Ryan, Mel, and Marshall.

# EPIGRAPH

When you do things right,
people won't be sure you've done anything at all.

*Futurama, Godfellas, S3 Ep. 20*

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C. Hardy, Y. Ramadass, K. Scoones, and H.-P. Le, "A Flying-Inductor Hybrid DC-DC Converter for 1-Cell and 2-Cell Smart-Cable Battery Chargers," IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3292–3305, Dec. 2019.

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C. Hardy and H. Le, "11.5 A 21W 94.8%-Efficient Reconfigurable Single Inductor Multi-Stage Hybrid DC-DC Converter," 2023 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, Feb. 2023.

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C. Hardy and H. Le, "11.5 A 21W 94.8%-Efficient Reconfigurable Single Inductor Multi-Stage Hybrid DC-DC Converter," Feb. 2023 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2023.

C. Hardy, H. Pham, M. Jatlaoui, F. Voiron, T. Xie, P. Chen, S. Jha, P. Mercier, and H. Le, "11.1 A Scalable Heterogeneous Integrated Two-Stage Vertical Power Delivery Architecture for High Performance Computing," 2023 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2023.

H. Pham, R. Das, C. Hardy, D. Kimball, P. Asbeck, and H. Le, "Adjustable 4-Level Hybrid Converter for Symbol Power Tracking in 5G NR," 2023 IEEE Applied Power Electronics Conference - (APEC), Orlando, FL, USA, 2023.

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C. Hardy, “A Low Power, Filter-Less Class D Audio Amplifier For Headphone Applications,” M.S. thesis, Dept. Elect. Eng., San Francisco State Univ., San Francisco, CA, USA, 2015.

ABSTRACT OF THE DISSERTATION

Hybrid DC-DC Converters for Smart Integrated Power Delivery

by

Casey L. Hardy

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2022

Professor Hanh-Phuc Le, Chair

The continual increase in performance and feature densities of small form factor mobile products has driven the need for high-capacity batteries and thus battery charger solutions with higher power-delivery densities to meet the demand for reduced charging times. The USB-C power delivery specification was developed to meet these higher demands by providing a programmable $V_{BUS}$ voltage range of 5–20 V with up to 100 W of power delivery, which serves as the input voltage ($V_{IN}$) for the battery charger. A DC-DC converter that efficiently takes advantage of this wide $V_{IN}$ range while providing an output voltage ($V_O$) range suitable for battery charging (e.g. 2.8V–4.2V) is challenging but highly desirable for space constrained products.

Hybrid converters provide a path to meet these challenges by leveraging the benefits of both switched-capacitor (SC) and switched-inductor (SI) techniques to reduce inductor size and efficiently provide high $V_{IN}/V_O$ voltage conversion ratios (VCRs). The former is important since inductors have substantially lower energy storage densities compared to modern capacitor technologies. Therefore, inductors tend to be the largest occupiers of board space and bill-of-material cost out of all the converter passives. Additionally, die-level or package-level integration of high quality inductors can be challenging when compared to capacitors.

This work intends to address these challenges by introducing new hybrid converter topologies that reduce the energy processing required by the inductor while still achieving the VCRs needed to take advantage of the benefits offered by higher $V_{IN}$ charging. This reduces the reliance on large, high quality inductors to maintain high power efficiency. The first part of this dissertation provides background regarding charge-based converter analysis. The next part presents a flying inductor hybrid topology that relocates the inductor from the high output current location to lower input current location while providing multiple outputs for 1-cell and 2-cell charging. The last part presents a single inductor multi-stage hybrid converter that utilizes an inductor to couple two SC stages to provide soft-charging benefits to each stage while leveraging reconfiguration to efficiently provide a wide range of VCRs.

# Chapter 1

# Introduction

## 1.1 The Need for High Power Delivery Density for Mobile Products

The performance and feature densities of mobile products continue to increase on an annual basis. Every year, new devices arrive with higher performance processors, higher quality cameras/displays, and additional features such as contact-less payments, facial recognition, and other biometrics just to name a few. To give some perspective on this, Figure 1.1 provides some data points regarding the evolution of laptops and mobile phones over the decades since their initial release. From these examples it should be evident that while performance improves and feature lists increase, some consumer expectations remain constant with each new product introduction: battery life should increase, charging times should decrease, and products should become smaller and lighter. Whether these expectations are met is largely dependent on the energy conversion and space efficiencies of the internal power electronics that must operate within the thermal constraints of the product.

## 1.2 High Input Voltage Charging and Power Delivery

The battery life challenge can be partially alleviated with the utilization of higher capacity batteries. However, this often comes at the cost of a reduction in available space for power electronics and requires higher power density battery chargers to meet the demand for reduced


**Figure 1.1.** Examples of mobile device evolution over the years.

charging times. The Universal Serial Bus Type-C (USB-C) 3.0 power delivery specification [1] was created to enable higher power delivery and faster charge times by providing a range of fixed $V_{BUS}$ voltages of 5V, 9V, 15V, and 20V, which serves as the input voltage ($V_{IN}$) for the battery charger. These higher $V_{IN}$ voltage settings also minimize input current levels and associated $I^2R$ losses across the USB-C cable, preserving overall system efficiency while charging at these higher power levels. A DC-DC converter that efficiently takes advantage of this wide $V_{IN}$ range while providing an output voltage ($V_O$) range suitable for battery charging (e.g. 2.8V–4.2V for a single cell Li-ion battery) is challenging but highly desirable for these thermally constrained, small form factor products.

## 1.3 Energy Density Challenges of Inductors

The magnetic components present a multitude of design challenges for conventional switched inductor (SI) DC-DC converters. Specifically, the inductors in conventional step-down converter topologies are typically located at the output of the converter and must conduct the full current provided to the load. Due to the high-power demands of applications such as fast charging of high capacity batteries, this means the inductor must process significant levels of current. This typically requires the physical size of the inductor to be large or the inductor component count to be increased to minimize conduction losses associated with winding resistances (DCR); increasing board space requirements, PCB routing complexity, and cost. On top of that, the saturation current rating ($I_{SAT}$) of the inductor must be greater than the expected maximum current (i.e. load current plus ripple current) seen by the inductor. Increases in $I_{SAT}$ rating also typically translates into increases in physical size. As discussed in [2], the energy storage densities of inductors can be multiple orders of magnitude lower than capacitors. This translates to inductors being one of the largest consumers of board space and any increase in physical size can be challenging for space constrained products such as modern smart phones or tablets.

## 1.4 Switched-Capacitor Converter Advantages and Disadvantages

An obvious solution around the limitations of low energy density of inductors is to eliminate need for them completely through the use of switched-capacitor (SC) converters. The high energy density of modern capacitor technology has allowed SC converters to become one potential avenue for promoting further system integration and area reduction. However, as described in [3], when capacitors transfer or receive charge through an ideal or non-ideal interconnect (i.e. a power switch) there is an unavoidable charge transfer loss due to the high rate of voltage change across the capacitors (i.e. high $^{dV}/_{dt}$) during the charge transfer, resulting in impulse shaped current flow in the capacitors. This loss is proportional to the square of the resulting voltage ripple across the capacitor during the charging and discharging events also known as hard charge losses. SC converter topologies can achieve high power efficiencies but only when operating near an optimal fixed voltage conversion ratio (VCR). Other VCRs can only be achieved by effectively increasing the voltage ripple across the capacitors. Therefore, voltage regulation beyond the ideal VCR for a given topology can only be achieved by incurring substantial energy losses and efficiency penalties.

Reconfigurable SC converter techniques can be leveraged to address this limitation by introducing the capability of changing the SC topology [4] or cascading and stacking of SC unit cells or combination of both [5]. However, these techniques come at the cost of additional power switches and control complexity. While this may be feasible for low voltage applications where advanced technology nodes allow high switch count with manageable die area impact, substantial increases in switch count may not be feasible for high voltage converter applications where many switches may need to interface with high voltage domains. This demands higher voltage ratings for these switches and dramatic increases in required area. Additionally, these larger devices introduce significant increases in gate and parasitic capacitances; placing practical limitations on maximum switching frequencies and associated switching losses.

## 1.5 Hybrid Power Converters

Hybrid power converters that leverage the benefits of both SI and SC topologies provide a viable path to address these challenges. Hybrid power conversion has been a very active area of recent power electronics research [6–17] and has already seen some commercial adoption [18–20] thanks to its potential benefits such as inductor size reduction and high VCRs at high power efficiencies. In general terms, these beneficial characteristics are largely enabled by utilizing the capacitor voltages in a SC network to provide:

- Additional $V_{IN}$ reduction $\rightarrow$ Higher $V_{IN}/V_O$ step-down VCRs [9, 10, 12, 14, 17]
- Additional $V_O$ increase $\rightarrow$ Higher $V_O/V_{IN}$ step-up VCRs [16]
- Reduced voltage blocking rating for power switches $\rightarrow$ Higher switching frequency and less switching losses $\rightarrow$ Reduced inductor size/current ripple [6–8, 14, 16, 21]
- Reduced inductor voltage swing $\rightarrow$ Reduced inductor size/current ripple [6–8, 21]

while utilizing inductor currents for charging/discharging of SC network capacitors to:

- Reduce or eliminate capacitor hard charge losses $\rightarrow$ Smaller capacitors while maintaining high power efficiency [6–8, 12, 14, 16]
- Efficient continuous $V_O$ control $\rightarrow$ Wider range of efficient VCRs [6–8, 22]

It should be noted that while these are all potential benefits offered by hybrid conversion techniques, whether all or only some are fully or partially achieved is highly dependent on the topology and design implementation. The importance and overall impact of each benefit are also highly dependent on the application space needs and priorities.

One of the simplest examples that illustrates many of these points is to compare a traditional 2-level to its closes hybrid counterpart, the 3-level buck converter. As shown Figure 1.2, the 2-level buck has two unique switching states that allow two levels of voltage at the LX node

($V_{IN}$ and 0V) resulting in a step-down VCR equal to the duty cycle, D, of switch SW1 which is defined as the portion of the switching period, $T_S$, that SW1 is on ($T_{ON}$). As can be observed in the switching states and LX switching node voltage, $V_{LX}$, of Figure 1.2 each switch would require a voltage rating greater than or equal to $V_{IN}$ since it must block this voltage when in the off state. It can also be readily shown from the inductor voltage, $V_L$, the resulting peak-to-peak inductor current ripple as a function of D (i.e. VCR) and $V_{IN}$ is

$$\Delta i_{L-2L} = \frac{V_{IN} D (1-D)}{L f_S} \tag{1.1}$$

where $f_S = 1/T_S$ is the converter switching frequency and $L$ is the inductor value.

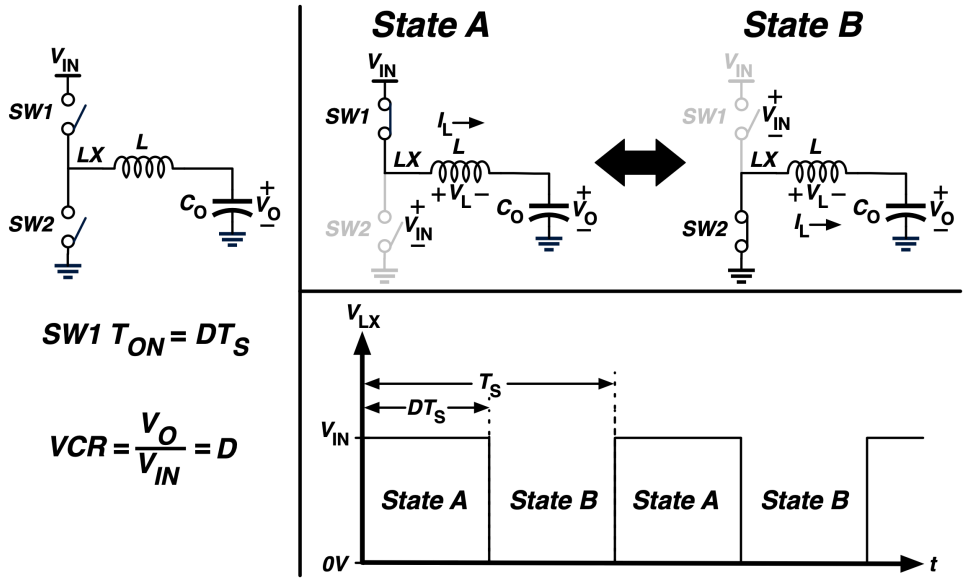



**Figure 1.2.** Conventional 2-level buck converter power stage, switching states, and LX switching node voltage.

In the case of the 3-level buck shown in Figure 1.3, a 2:1 series-parallel SC network is inserted in front of the inductor by adding two switches and a flying capacitor, $C_F$, which is assumed to have a steady-state DC voltage of $V_{IN}/2$, and includes four unique states that allow three levels of voltage at the LX node ($V_{IN}$, $V_{IN}/2$, and 0V). As with the 2-level buck, the resulting step-down VCR is equal to the duty cycle, D, of switch SW1. However, it can be seen in

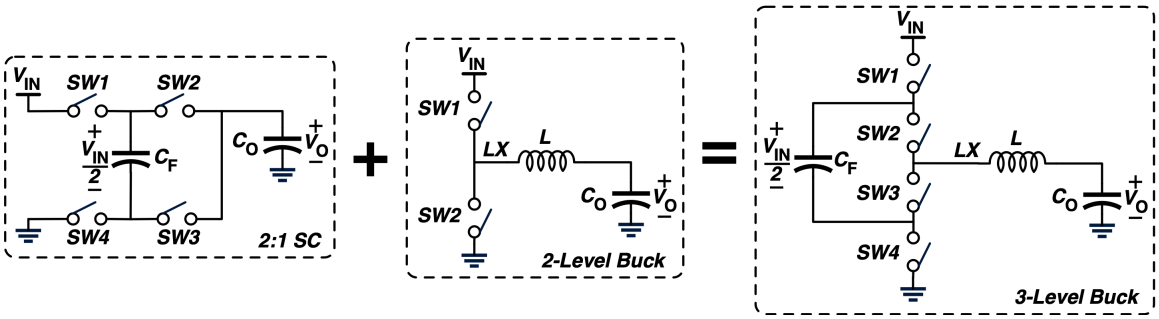



**Figure 1.3.** Formation of a 3-level buck converter power stage.

Figure 1.4 and the $V_{LX}$ waveforms in Figure 1.5, the additional voltage blocking provided $C_F$'s voltage reduces the minimum switch voltage rating to $V_{IN}/2$ and enables the possibility of significant switch area and energy loss savings through the use of higher conductance density switches with lower associated gate and parasitic capacitances. This also reduces the voltage swing of $V_L$ and the resulting peak-to-peak inductor current ripple which can shown as a function of D and $V_{IN}$ as

$$\Delta i_{L-3L} = \frac{V_{IN} D(1-2D)}{2Lf_S} \tag{1.2}$$

for $0 < D < 0.5$ and

$$\Delta i_{L-3L} = \frac{V_{IN}(1-D)(2D-1)}{2Lf_S} \tag{1.3}$$

for $0.5 < D < 1$ with the ripple approaching zero at $D = 0.5$. Figure 1.6 plots the inductor ripple currents normalized by the maximum 2-level buck value to further illustrate the substantial reduction provided by the 3-level buck. As can be seen, there is a 4x reduction in the maximum peak-to-peak value when compared the 2-level buck. It should be noted this is also aided by the fact there is an effective doubling in the switching frequency seen by the inductor as implied in the waveforms of Figure 1.5 with the net effect being the opportunity for significant inductor size/value reduction over the traditional 2-level solution.

The operating behaviors presented here in the context of a 3-level buck reinforces the potentially significant gains of hybrid converter techniques. As shown, merging a simple series-parallel SC topology with the operation of a conventional buck converter reduced the required

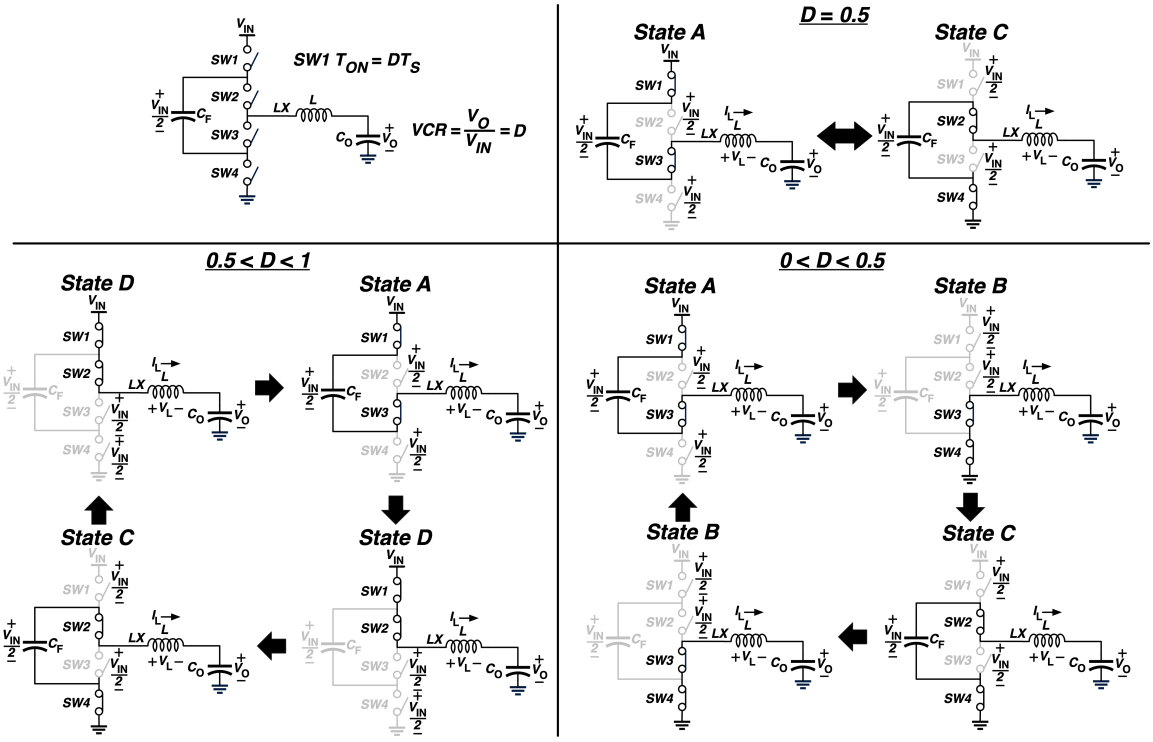



**Figure 1.4.** 3-level buck converter power stage and switching states for different duty cycle values.

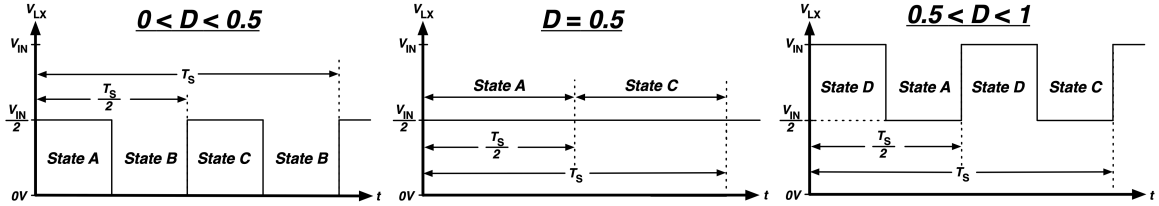



**Figure 1.5.** 3-level buck converter LX switching node voltages for different duty cycle values.

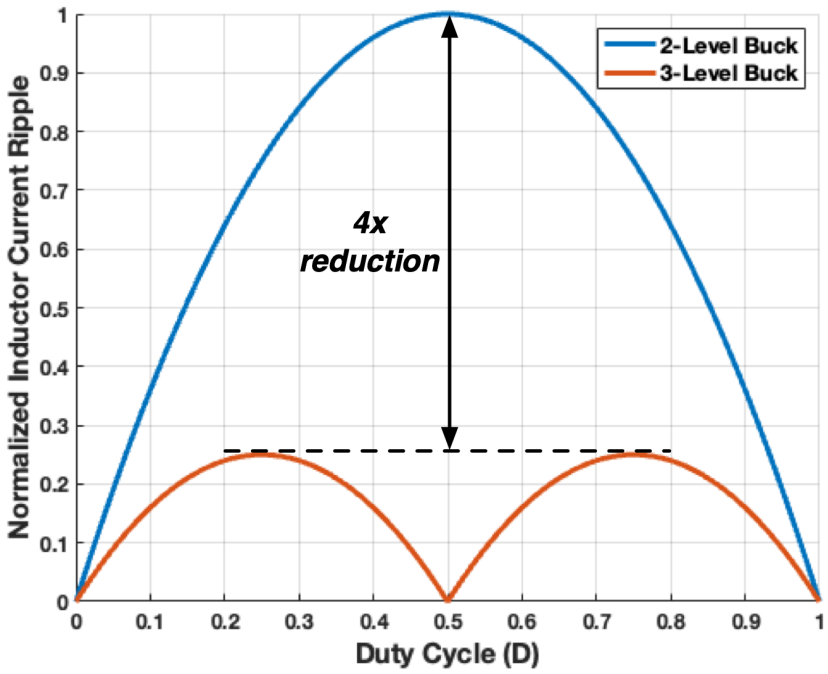



**Figure 1.6.** Normalized peak-to-peak inductor current ripple vs. duty cycle of 2-level and 3-level buck converters.

the switch voltage ratings and inductor ripple current while also increasing the effective inductor switching frequency; creating a pathway to substantial efficiency and circuit area benefits. Extensions of these techniques and resulting benefits will be illustrated further in Chapters 3 and 4.

## 1.6 Organization and Contributions of Dissertation

The exploration of the discussed properties of hybrid converters in the previous section and their demonstrated advantages in both academic research [6–17] and commercial products [18–20] is the basis of the research conducted for this dissertation. This work aims to leverage these properties for the exploration of new topologies, perspectives, and implementation concepts of hybrid converters. The term "smart" in the title of this dissertation is intended to describe a holistic approach to hybrid converter design that:

- Explores the usage of parasitic reactive elements already present in systems for power conversion.
- Flexibility and extension of VCRs to provide a single, power efficient, hardware solution for multiple application use cases.
- Not only leverages the benefits of merging SC and SI operation but also explores the benefits of merging multi-stage operation.
- Reduces the reliance on low energy density components such inductors to promote integration and size reduction.

In order to provide some background regarding the modeling approach of the converter prototypes discussed in this dissertation, Chapter 2 provides an overview of charge flow based analysis of conventional converters and how it can be easily extended to hybrid topologies. This is intended to demonstrate the utility of the analysis method in the estimation of the loss modeling which are then utilized in the design and optimization of the converters presented in Chapters 3 and 4. Chapter 3 presents a new step-down hybrid converter topology that utilizes an input flying inductor and a SC network to provide two outputs suitable for 1-cell and 2-cell battery charging from a 9V input. The topology prototype is also demonstrated while using the parasitic inductance of a USB cable in place of a discrete inductor to facilitate its integration into a proposed smart-cable architecture. Chapter 4 presents a reconfigurable single inductor multi-stage hybrid step-down converter that efficiently provides the VCRs needed for 1-cell battery charging across a wide input voltage range of 5V–24V while moving the inductor away from the high output current path. The inductor is used to couple two synchronous SC stages to provide soft charging benefits to each stage and extends reconfigurable SC and merged multi-stage operation concepts. Finally, a summary of the contributions and conclusions of this work will be provided in Chapter 5.

# Chapter 2

# Charge Flow Based Analysis of Converters

## 2.1 DC Transformer and Loss Model of Converters.

As derived in [23], a DC-DC converter in steady-state can be modeled as an ideal DC transformer shown in Figure 2.1 where the ideal VCR of the converter is

$$M = \frac{V_{O-ideal}}{V_{IN}} = \frac{I_{IN}}{I_O} \tag{2.1}$$

where $I_{IN}$ and $I_O$ represent the DC input and output currents of the converter, respectively. In Figure 2.1, $R_L$ is the converter load resistance and $R_O$ is a lumped output resistance that models the total load dependent conduction losses of the converter and is also equivalent to the open loop output resistance of the converter. The resulting open loop (i.e. unregulated) $V_O$ can then be found by

$$V_O = V_{O-ideal} - I_O R_O \tag{2.2}$$

if the value of $I_O$ is known. As discussed in [4], other losses such as quiescent current related losses and switching losses can also be modeled as an equivalent shunt loss element, but these losses are omitted for this discussion.

As can be seen from this simple model, $R_O$ should be minimize to maximize power efficiency. Additionally, in the case of a closed loop regulator implementation, $M$, $R_O$, or a combination of both could be adjusted by the control loop to regulate $V_O$ to the target output

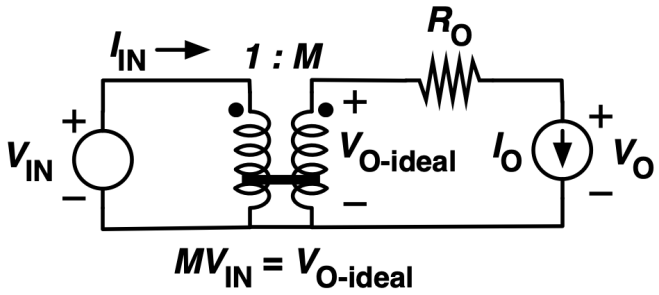



**Figure 2.1.** Ideal DC transformer based loss model of a DC–DC converter.

voltage.

## 2.2 Analysis Example: Switched-Capacitor Converters

Given that SC converters are essentially charge processors that operate by transferring discrete packets of charge from input to output, a charge flow based approach greatly simplifies the analysis and derivations of their salient features [3]. To clearly illustrate how the ideal VCR, $M$, and hard charge conduction losses associated with a flying capacitor can be evaluated by just examining the charge transfer behavior of a converter, a simple parallel 1:1 SC converter will be used as an initial example for demonstrating some principles of the analysis method. The 1:1 SC converter and corresponding operating states are shown in Figure 2.2. Note the output capacitor is assumed to be large in value and emulates the behavior of a DC voltage source. From the properties of an ideal transformer and the fact that current is a transfer of charge per unit time, equation (2.1) can easily be re-written in terms of charge as

$$M = \frac{I_{IN}}{I_O} = \frac{q_{IN}/T_S}{q_O/T_S} = \frac{q_{IN}}{q_O} \tag{2.3}$$

where $q_{IN}$ and $q_O$ are the total amounts of input charge and output charge transferred over one switching period, $T_S$, respectively. As shown in the flying capacitor voltage waveform ($V_C$) of Figure 2.2, the flying capacitor, C, is charged to $V_{IN}$ in State A and discharged to $V_O$ in State B. It is also assumed each state lasts for $T_S/2$ (i.e. 50% duty cycle) and the duration of each state is

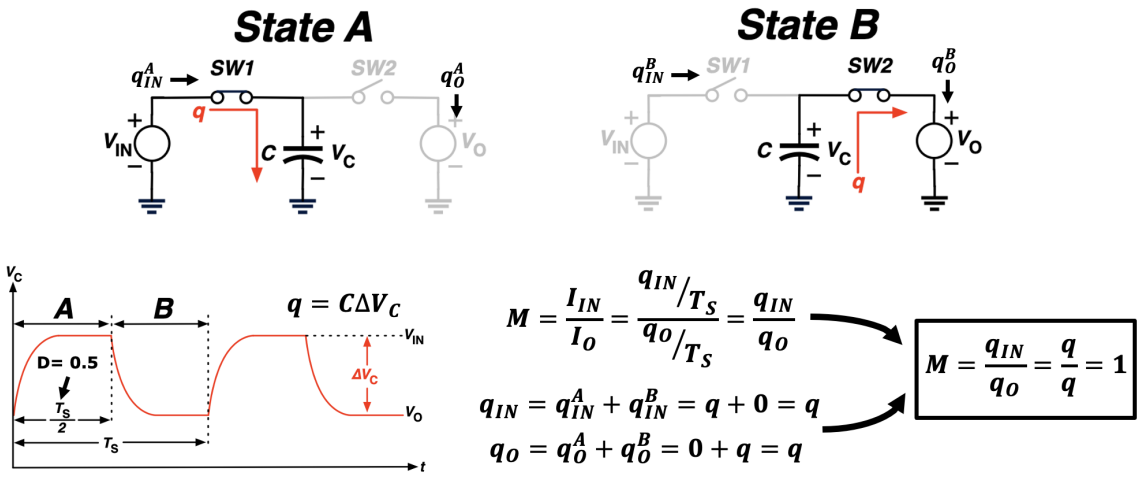



**Figure 2.2.** Operating states, flying capacitor voltage, and charge flows for a 1:1 switched-capacitor converter.

much longer than the RC time constants of the flying capacitor and switch on-resistances (i.e. switches are ideal). When the capacitor is charged to $V_{IN}$ it accumulates a unit charge, $q$, that is proportional to $\Delta V_C$ which must then be discharged into $V_O$ in order for the converter to be in steady-state and remain charge balanced [23]. Summing the total input and output charge transfers during each switching state and substituting into equation (2.3) results in

$$q_{IN} = q_{IN}^{A} + q_{IN}^{B} = q + 0 = q$$

$$q_{O} = q_{O}^{A} + q_{O}^{B} = 0 + q = q$$

$$M = \frac{q}{q} = 1$$

where the superscripts in the charge terms correspond to the charge transfers corresponding to those respective switching states.

To understand the origin of the hard charge losses associated with the flying capacitor, Figure 2.3 provides the analysis of the energy lost when the capacitor, C, transitions from state A to state B where it is again assumed the switches are ideal. To find the loss during this during

this transition, the energy delivered by the $V_{IN}$ source is first found as

$$E_{IN} = V_{IN}C(V_{IN} - V_O)$$

and then the energy received by the capacitor in state A is found as

$$E_C^A = C\left(\frac{(V_{IN})^2}{2} - \frac{(V_O)^2}{2}\right).$$

The energy lost during the charge transfer is then the difference of the energy delivered by the source and the energy received by the capacitor:

$$E_{LOSS}^A = E_{IN} - E_C^A = \frac{1}{2}C(V_{IN} - V_O)^2 = \frac{1}{2}C(\Delta V_C)^2.$$

Repeating the analysis for the transition to state B yields the same result of

$$\frac{1}{2}C(\Delta V_C)^2.$$

Therefore the total energy lost over the switching periods is

$$E_{LOSS} = E_{LOSS}^A + E_{LOSS}^B = C(\Delta V_C)^2 \tag{2.4}$$

Now that we have an expression for the energy loss of the flying capacitor over a switching period, Figure 2.4 shows how this loss can be related back to the equivalent converter $R_O$ resistance shown in the ideal DC transformer model (Figure 2.1). Since the change in the capacitor voltage is also

$$\Delta V_C = \frac{q}{C}$$

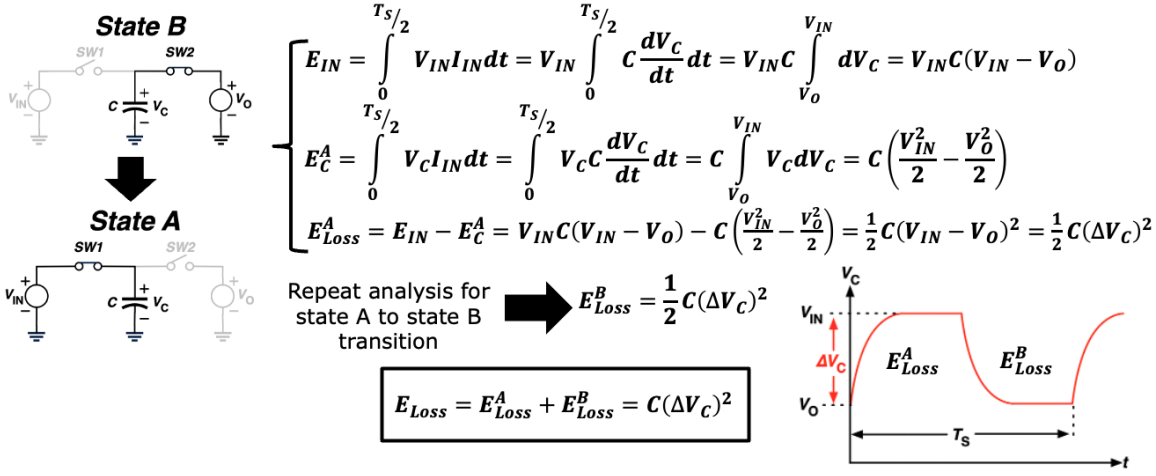



**Figure 2.3.** Flying capacitor energy loss for a 1:1 switched-capacitor converter.

where $q$ is the charge accumulated or removed from it, (2.4) can be re-written as

$$E_{LOSS} = \frac{q^2}{C}$$

and the resulting power loss for the capacitor is

$$P_{LOSS} = \frac{E_{LOSS}}{T_S} = \frac{q^2}{CT_S} \tag{2.5}$$

As shown in Figure 2.4, we can also define the equivalent conduction power loss from the DC transformer model as

$$P_{LOSS} = (I_O)^2 R_O = \left(\frac{q_O}{T_S}\right)^2 R_O \tag{2.6}$$

since the DC output current is the total output charge transferred over one switching period. Equating equations (2.5) and (2.6) and solving for $R_O$ yields what is known as the slow-switching limit output resistance of the 1:1 SC converter

$$R_{SSL} = \left(\frac{q}{q_0}\right)^2 \frac{1}{f_S C} = \left(\frac{q}{q}\right)^2 \frac{1}{f_S C} = \frac{1}{f_S C} \tag{2.7}$$

where $f_s$ is the switching frequency of the converter ($f_S = 1/T_S$). The $R_{SSL}$ is the equivalent

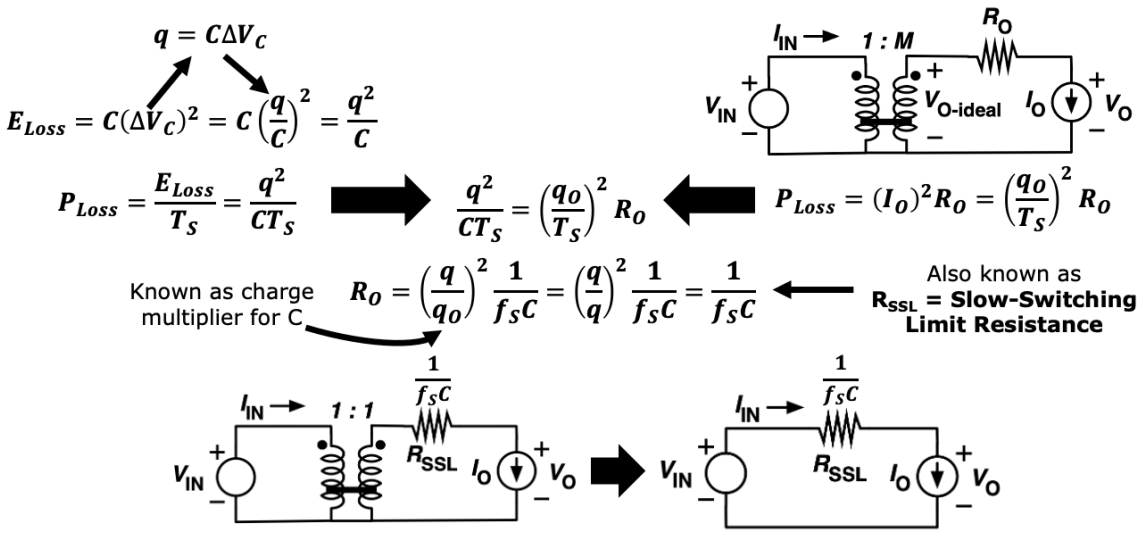



**Figure 2.4.** Finding $R_{SSL}$ from the flying capacitor power loss for a 1:1 switched-capacitor converter.

conduction loss output resistance due to the hard charging losses of the flying capacitor, C. In other words, this is the equivalent output resistance contribution of the flying capacitor due to the voltage ripple ($\Delta V_C$) across it. It should be noted that the $q/q_O$ term in Figure 2.4 is also known as the charge multiplier for flying capacitor, C, for this topology as described in the generalized SC analysis approach described in [3].

Now that some of the basic charge flow concepts have been demonstrated for the VCR and $R_{SSL}$ derivations for one of the most elementary of SC topologies, let us now apply them to a slightly more complicated 2:1 topology which will then be used to illustrate the derivation of the remaining conduction loss elements. The 2:1 SC converter, corresponding operating states, and charge flows are provided in Figure 2.5. Following the same procedures from the preceding example, it can be seen that the flying capacitor, C, again processes a unit $q$ of charge when charging and discharging. The major difference now is that, when it is charged, it also allows the same charge to pass to the output. Summing the total input and output charges of the switching cycles yields

$$q_{IN} = q_{IN}^{A} + q_{IN}^{B} = q + 0 = q$$

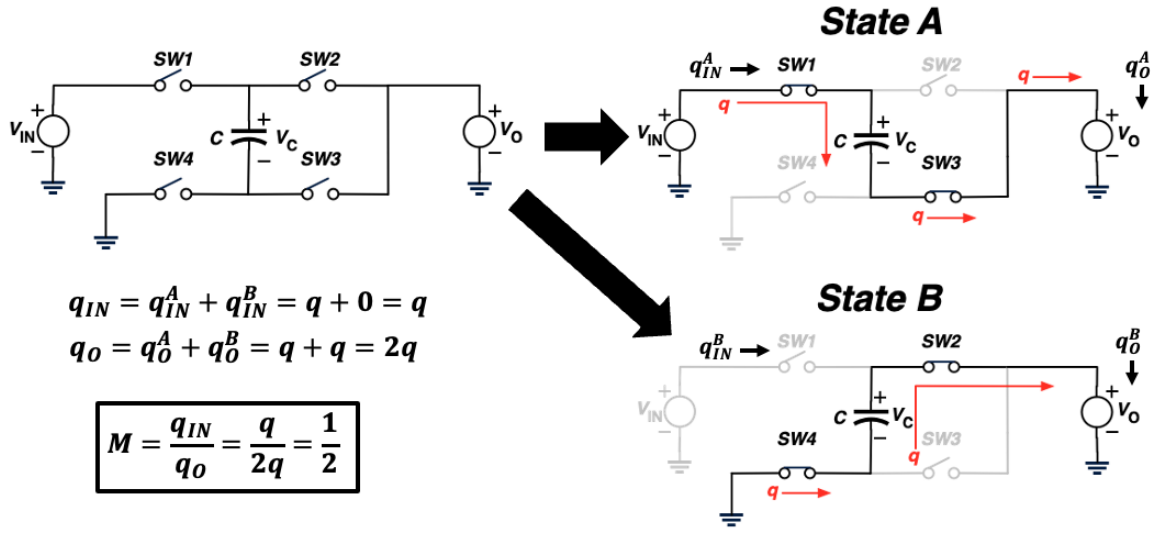



**Figure 2.5.** Operating states and charge flows for a 2:1 switched-capacitor converter.

$$q_O = q_O^A + q_O^B = q + q = 2q$$

with a resulting ideal VCR of

$$M = \frac{q_{IN}}{q_O} = \frac{q}{2q} = \frac{1}{2}.$$

Again, as shown in Figure 2.6, the $R_{SSL}$ resistance can be derived by equating the $\Delta V_C$ ripple related power loss of the flying capacitor to the ideal transformer $R_O$ related conduction losses resulting in

$$R_{SSL} = \left(\frac{q}{q_0}\right)^2 \frac{1}{f_S C} = \left(\frac{q}{2q}\right)^2 \frac{1}{f_S C} = \left(\frac{1}{2}\right)^2 \frac{1}{f_S C} = \frac{1}{4 f_S C} \tag{2.8}$$

which shows that as with the 1:1 SC converter the $R_{SSL}$ related loss is inversely proportional with the switching frequency but is a 4x smaller for the same $f_S$ and flying capacitor value. This illustrates one of the interesting topology dependencies that is further discussed in [2, 3]. It should also be noted that while the 1:1 and 2:1 SC converters presented here have a single flying capacitor that happen to process a single $q$ of charge in the charge flow analyses, there are many other topologies with a larger number of flying capacitors that may each process different amounts of $q$ in their operation [3, 24, 25].

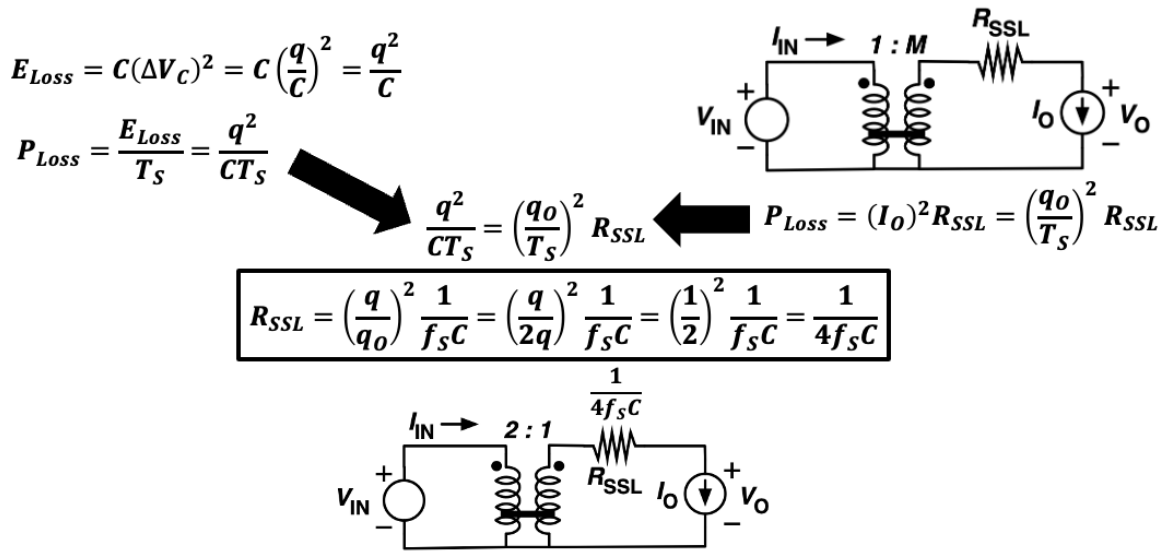



**Figure 2.6.** Finding $R_{SSL}$ from the flying capacitor power loss for a 2:1 switched-capacitor converter.

Since $R_{SSL}$ related losses are caused by the flying capacitor ripple voltage and are inversely proportional to $f_S$ for a given capacitor value, it is understandable to expect the efficiency to be maximized if $f_S$ is maximized if switching losses are ignored. However, as previously mentioned, the analysis for the slow-switching limit (SSL) related losses assumed ideal switches and that the RC time constants of the switch on-resistances and flying capacitor were much shorter than the switching period. Figure 2.7 shows the simulated $V_C$, SW1 current ($I_{SW1}$), and SW2 current ($I_{SW2}$) for an example 2:1 SC converter at different $f_S$ values. As can be seen in Figure 2.7(a), $T_S$ is long enough to allow the flying capacitor to almost completely charge/discharge during each switching state, resulting in noticeable $V_C$ ripple, and the switch currents have impulse-like shapes with exceptionally high peaks that are only limited by the small switch resistances in charging/discharging paths and the corresponding voltages across them. Therefore, the converter is clearly in SSL operation. However, as $f_S$ is increased in Figure 2.7(b) the switch currents begin to lose their impulse-like shape due to the finite switch on-resistances and the corresponding time constants formed with the flying capacitor in each state being on par with the switching state durations. It can also be seen the $\Delta V_C$ ripple is

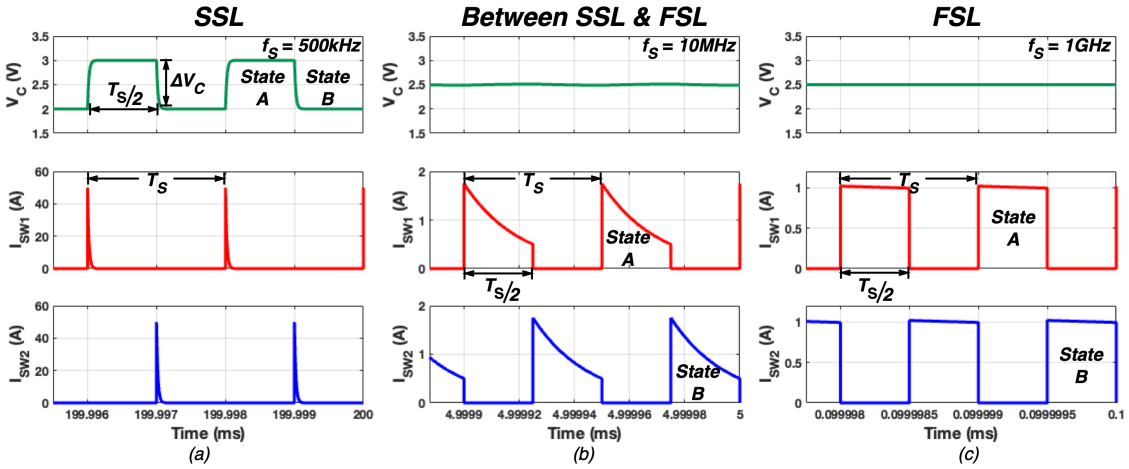



**Figure 2.7.** Comparison flying capacitor voltage and switch current behavior for (a) SSL, (b) SSL-to-FSL transition, and (c) FSL operating regions of a 2:1 switched-capacitor converter.

substantially reduced, implying the $R_{SSL}$ related losses are also substantially reduced. Finally, if $f_S$ is further increased to an exceptionally high value as shown in Figure 2.7(c), it can be seen that the switch and capacitor time constants are much longer that switching state durations, resulting in the switch currents to be nearly constant when on and there to be near zero $\Delta V_C$ ripple across the capacitor. This region of operation is known as the fast-switching limit (FSL) whereas the region of operation in Figure 2.7(b) lies somewhere between the SSL and FSL regions. Since the $\Delta V_C$ ripple across the capacitor in FSL is near zero, this would imply there is little to no SSL related losses. However, as can be seen from the switch current waveforms in Figure 2.7(c), during FSL operation there is clearly current flow through the switches which have finite on-resistances. Therefore, there must still be some conduction energy dissipated by the switches when on.

In order to derive a new expression for this FSL related conduction loss, we can re-visit the charge flows for each state shown in Figure 2.8 with a focus on the charges processed by each of the power switches and leveraging the fact that the switch currents are nearly constant during FSL operation as shown in Figure 2.7(c) to greatly simplify the derivation. It should be noted that while the exact value of the unit charge, $q$, processed by each circuit element in the converter may be drastically different in SSL vs. FSL operation (as made apparent in the

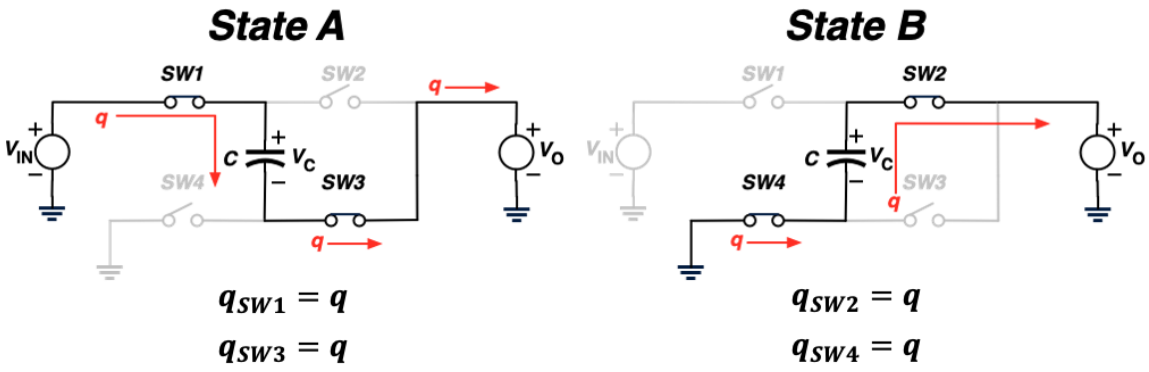



**Figure 2.8.** Switch charge flows for a 2:1 switched-capacitor converter.

significantly different switch current shapes and time durations in Figure 2.7), the actual value of the charges is unimportant as we only need to know the charge processed by each circuit element and how to relate that back to energy loss for the operating region of interest (i.e. SSL or FSL). As shown in Figure 2.8, each switch processes a $q$ amount of charge since the flying capacitor acquires a $q$ amount of charge in state A and discharges a $q$ amount of charge in state B to maintain steady-state charge balance as was the case for during SSL operation.

Figure 2.9 illustrates how the power loss of the switches can be easily found by taking advantage of the fact the switch currents are nearly constant when on. This approximation makes it easy to derive an expression for the total charge processed by the switch through a simple integration calculation (i.e. the red shaded area of $I_{SW1}$ waveform in Figure 2.9) which is

$$q = I_{SW1}\frac{T_S}{2}$$

where $I_{SW1}$ is the peak current value of SW1. This can then be used to build the expression for the switch energy loss during its on-time in terms of $q$ and $T_S$:

$$E_{SW1} = P_{SW1}\frac{T_S}{2} = (I_{SW1})^2 R_{ON1}\frac{T_S}{2} = \left(\frac{q}{T_S/2}\right)^2 R_{ON1}\frac{T_S}{2} = \frac{2q^2}{T_S}R_{ON1}$$

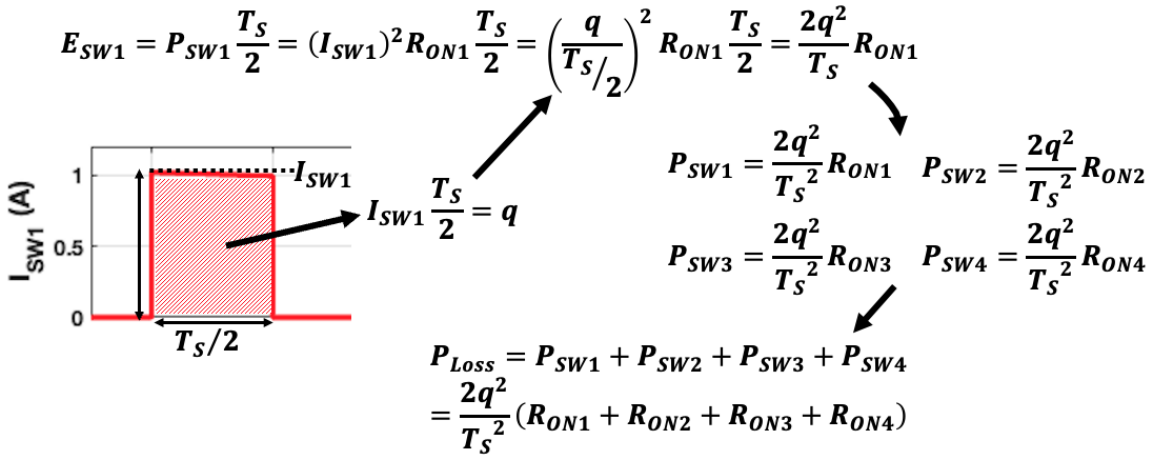



**Figure 2.9.** Switch power loss during FSL operation for a 2:1 switched-capacitor converter.

and the power dissipated by SW1 is

$$P_{SW1} = \frac{2q^2}{T_S^2}$$

where $R_{ON1}$ is the on-resistance of SW1. This is the same power loss expression for the remaining switches, since each switch in this converter example processes the same amount of charge as shown in Figure 2.8. Note that other topologies may have switches that processes unequal amounts of charge [3, 24, 25]. Summing the total power loss for all the switches results in

$$P_{LOSS} = P_{SW1} + P_{SW2} + P_{SW3} + P_{SW4} = \frac{2q^2}{T_S^2}(R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}). \tag{2.9}$$

As illustrated in Figure 2.10, we can again use the ideal DC transformer conduction loss model to derive the FSL conduction loss element by equating equations (2.6) and (2.9) and solving for the equivalent output resistance, resulting in

$$R_{FSL} = \frac{1}{2}(R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}) \tag{2.10}$$

where $R_{FSL}$ is the lumped equivalent conduction loss output resistance due to the power switch on-resistances for the 2:1 SC converter operating in the FSL region. As also annotated in Figure 2.10, each switch also has its own charge multiplier term that can be used in the generalized analysis

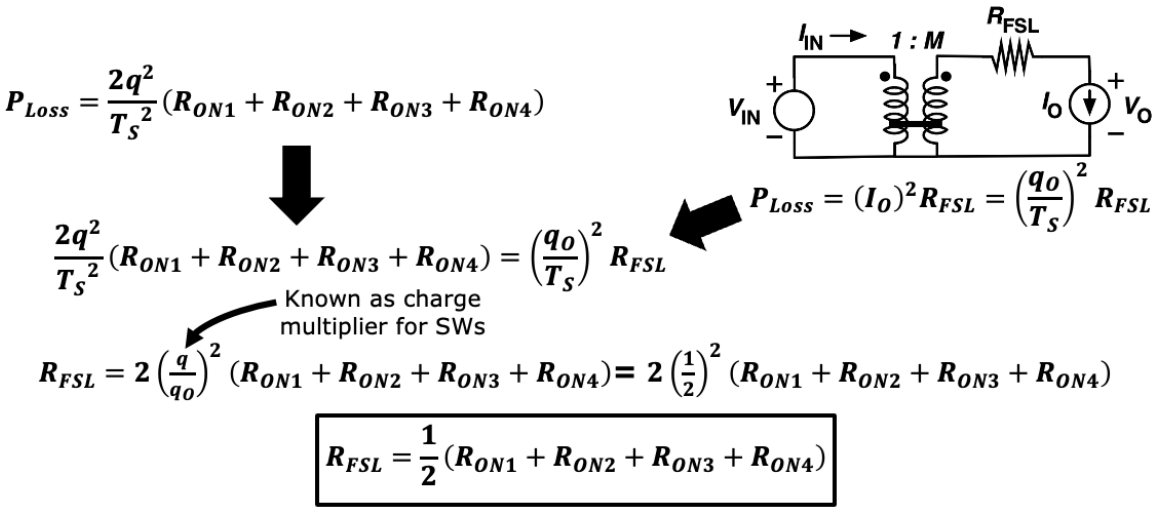



**Figure 2.10.** Finding $R_{FSL}$ from the switch power losses for a 2:1 switched-capacitor converter.

provided in [3]. It should also be noted that the loss contributions of any component equivalent series resistances (ESRs), parasitic layout resistances, etc. can also be analyzed in the same manner and integrated into the final $R_{FSL}$ expression if needed and as will be discussed later in Chapters 3–4.

Up to now, it has been shown that the derivations of the flying capacitor hard charge losses and power switch conduction losses can be easily derived with charge flow analysis. However, we now have separate conduction loss elements, $R_{SSL}$ and $R_{FSL}$, that have been derived in two different switching frequency extremes. While charge flow analysis greatly simplifies the analyses of each loss mechanism, we must utilize a method of integrating them into the loss model while still accurately capturing their impact on the overall converter efficiency regardless of the switching frequency as it is unlikely and impractical to assume the converter would operate entirely in one or the other of these two extremes in practical applications. As discussed in [26], there are many estimation techniques to accomplish this with the direct linear summation being one of the more conservative methods [24, 27] and the empirically derived summation in quadrature form [3, 28] which provides better accuracy:

$$R_O \approx \sqrt{(R_{SSL})^2 + (R_{FSL})^2}. \tag{2.11}$$

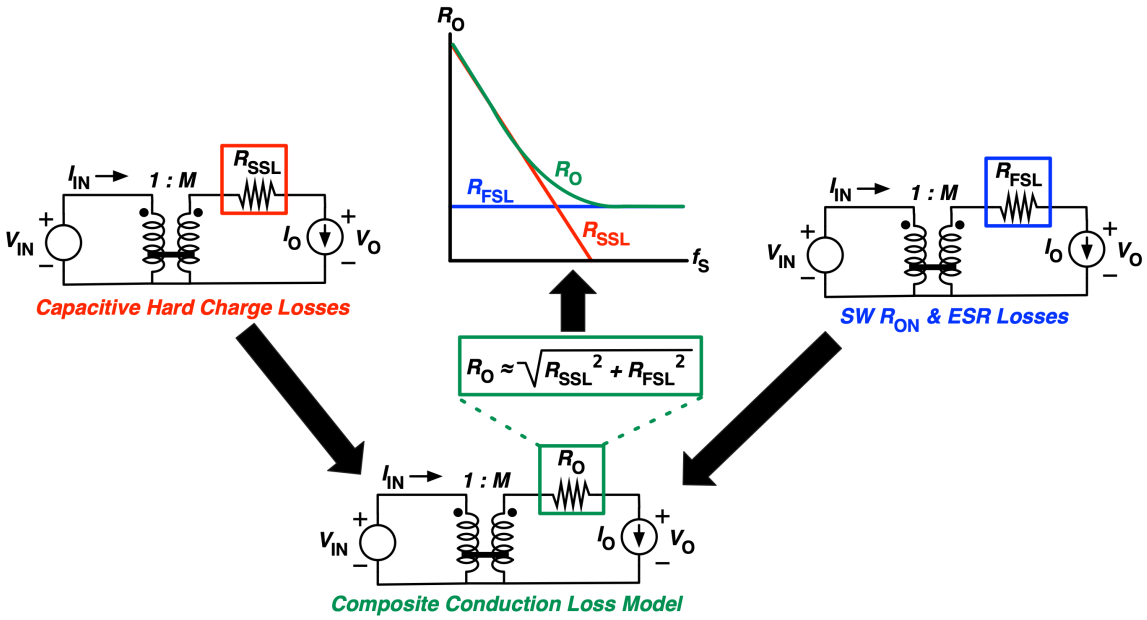



**Figure 2.11.** Combining $R_{SSL}$ and $R_{FSL}$ into a single $R_O$ for a switched-capacitor converter.

The work in [29] shows that even more accuracy can be obtained by using a Minkowski distance form of (2.11). For this work, equation (2.11) will be used since it provides reasonable accuracy in a concise analytical expression. Figure 2.11 illustrates this method of combing the $R_{SSL}$ and $R_{FSL}$ into a composite $R_O$ from equation (2.11) including a plot of the magnitude of all three resistances versus frequency. The plot shows the $R_{SSL}$ resistance forms an asymptote that is inversely proportional with frequency (red curve) while the $R_{FSL}$ resistance forms a horizontal asymptote (blue curve) that is independent of frequency since it is only dependent on resistances present in the charging or discharging paths (i.e. switch resistance, capacitor ESRs, etc). The resulting $R_O$ approximation from (2.11) is also plotted (green curve) showing that it closely emulates the dominance of SSL losses at low frequencies and the dominance of FSL losses at high frequencies.

A plot of the calculated and simulated output resistances versus switching frequency for an example 2:1 SC converter is shown in Figure 2.12 to illustrate the accuracy of (2.11). It should be noted the plot also implies that there is an optimal maximum $f_S$ in the region where $R_O$ transitions from SSL to FSL (~15MHz in this example) where there is no longer any further

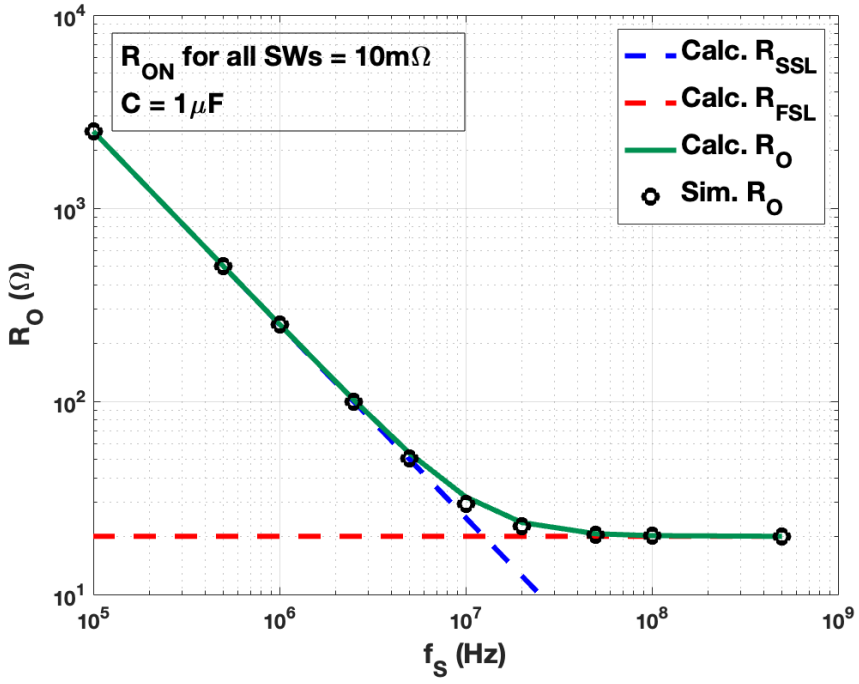



**Figure 2.12.** Calculated vs. Simulated $R_O$ for an example 2:1 switched-capacitor converter.

reduction in $R_O$ with increasing $f_S$ as it is $R_{FSL}$ limited. In a practical implementation, the converter would only incur additional switching losses with further increases in $f_S$ beyond this point.

## 2.3 Analysis Example: Switched-Inductor Converters

While charge flow analysis is commonly applied to simplify the analysis of SC converters, it can also be readily applied to facilitate the steady-state analysis of SI converters as an alternative to the volt-sec balance based approach covered in [23]. As an example, Figure 2.13 shows a conventional pulse width modulation (PWM) controlled 2-level buck converter and its corresponding charge flows for each state assuming continuous conduction mode operation [23] while conducting some non-zero DC load current. It is also assumed the converter $f_S$ is high enough such that the inductor current appears to be nearly constant (i.e. small ripple approximation). This assumption makes it quite simple to calculate the equivalent charge flows

for each state and is similar to the FSL scenario of a SC converter described in 2.2. The primary difference here being the duty cycle is no longer assumed to be fixed at 0.5 since it would be varied by means of PWM to set the output voltage. As shown in Figure 2.13, the charge processed by the inductor in states A and B are

$$q_L^A = I_L D T_S$$

$$q_L^B = I_L (1-D) T_S$$

where $I_L$ is the DC value of the inductor current, which is equivalent to the DC output current in this example. The total input and output charges over a switching period are then

$$q_{IN} = q_{IN}^A + q_{IN}^B = q_L^A + 0 = I_L D T_S$$

$$q_O = q_O^A + q_O^B = q_L^A + q_L^B = I_L D T_S + I_L (1-D) T_S = I_L T_S \tag{2.12}$$

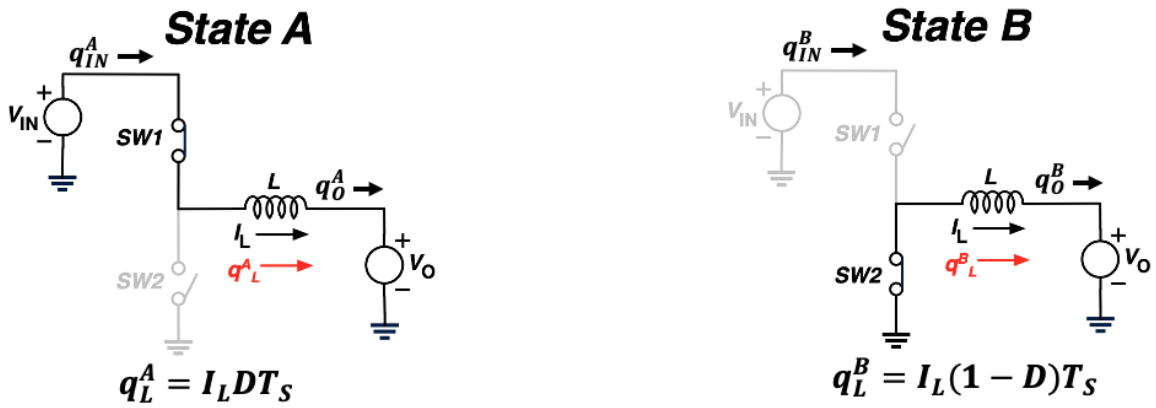
resulting in an ideal VCR of

$$M = \frac{q_{IN}}{q_O} = \frac{I_L D T_S}{I_L T_S} = D \tag{2.13}$$

which is equivalent to the results obtained from the volt-sec balance approach.

Since there are no hard charge capacitive losses in this example, we only need to develop an expression for the power losses associated with the power switches in the same manner as the FSL switch losses of the SC converter example in Section 2.2. As shown in Figure 2.14, the energy losses of each switch are

$$E_{SW1} = (I_L)^2 R_{ON1} D T_S \tag{2.14}$$




$$q_{IN} = q^A_{IN} + q^B_{IN} = q^A_L + 0 = I_L D T_S$$

$$q_O = q^A_O + q^B_O = q^A_L + q^B_L = I_L D T_S + I_L(1-D)T_S = I_L T_S$$

$$\boxed{M = \frac{q_{IN}}{q_O} = \frac{I_L D T_S}{I_L T_S} = D}$$

**Figure 2.13.** Operating states and charge flows analysis 2-level buck converter.

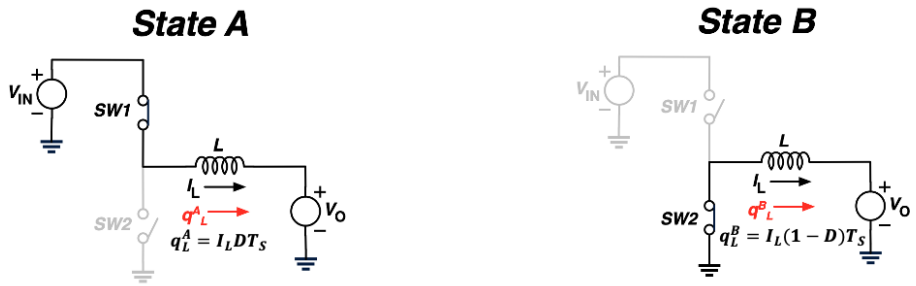
$$E_{SW2} = (I_L)^2 R_{ON2}(1-D)T_S \tag{2.15}$$

where $R_{ON1}$ and $R_{ON2}$ are the on-resistances for SW1 and SW2, respectively. The resulting total conduction power loss for the switches is

$$P_{LOSS} = \frac{E_{SW1} + E_{SW2}}{T_S} = (I_L)^2[R_{ON1}D + R_{ON2}(1-D)]. \tag{2.16}$$

It should be noted that for this simple converter example, the switch energy loss expressions (2.14) and (2.15) could be readily derived by inspection without the intermediate relations back to charge shown in Figure 2.14 since the switch currents are solely determined by the inductor current, but have been included here since this relation of inductor current and equivalent charge will be revisited in the loss modeling presented in Chapters 3 and 4.

To find the equivalent $R_O$ for the loss model, we can simply equate (2.16) to the conduction loss expression (2.6) from the ideal transform model and solve for $R_O$ as illustrated in




$$E_{SW1} = I_{SW1}^2 R_{ON1} DT_S = \left(\frac{q_L^A}{DT_S}\right)^2 R_{ON1} DT_S = \left(\frac{I_L DT_S}{DT_S}\right)^2 R_{ON1} DT_S = I_L^2 R_{ON1} DT_S$$

$$E_{SW2} = I_{SW2}^2 R_{ON2}(1-D)T_S = \left(\frac{q_L^B}{(1-D)T_S}\right)^2 R_{ON2}(1-D)T_S = \left(\frac{I_L(1-D)T_S}{(1-D)T_S}\right)^2 R_{ON2}(1-D)T_S = I_L^2 R_{ON2}(1-D)T_S$$

$$P_{Loss} = \frac{E_{SW1} + E_{SW2}}{T_S} = I_L^2[R_{ON1} D + R_{ON2}(1-D)]$$

**Figure 2.14.** Charge flows and switch power losses for a 2-level buck converter.

Figure 2.15 resulting in

$$R_O = R_{ON1} D + R_{ON2}(1-D). \tag{2.17}$$

Note that $I_L = I_O$ in this example which is also implied by (2.12). As can be seen in (2.17), each switch loss term is scaled dependent on the duty cycle value where the $R_{ON1}$ related losses increase at higher duty cycles while the $R_{ON2}$ related losses decrease and vice versa for decreasing duty cycles. This intuitively makes sense since the longer a particular switch is on then the more time it spends conducting the output current and dissipates energy.

To corroborate the accuracy of (2.17), Figure 2.16 shows the calculated and simulated $R_O$ for an example 2-level buck where the switch on-resistances have been set to unequal values to help illustrate their influences. As can be seen, the output resistance increases with increasing duty cycle due to SW1's higher on-resistance. The charge flow and loss modeling techniques presented here and in Section 2.2 will be extended and applied to the hybrid converters discussed in Chapters 3 and 4.

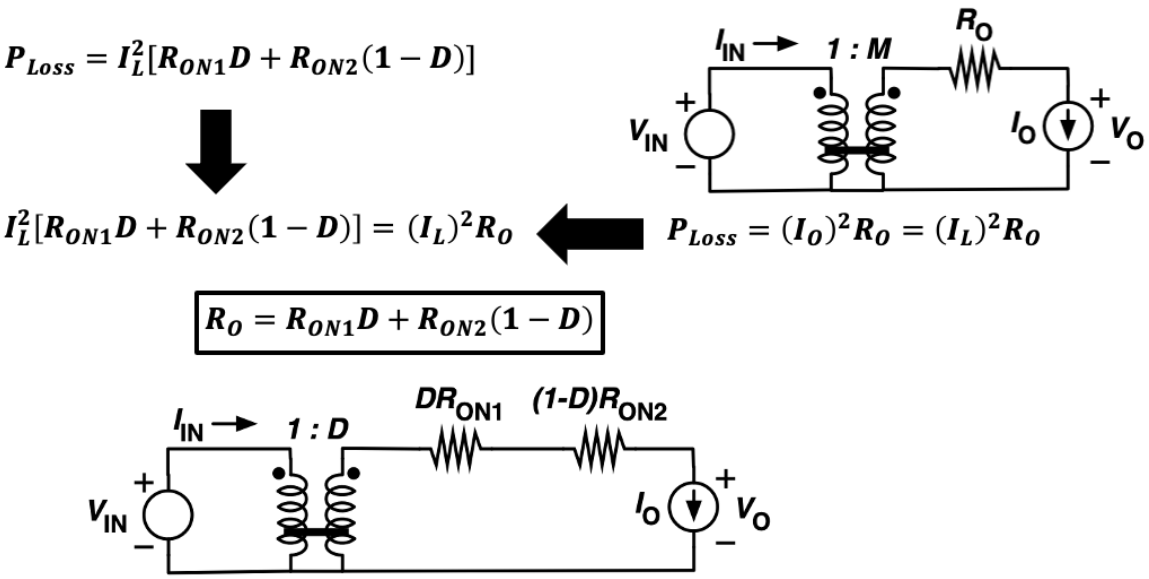



**Figure 2.15.** Finding $R_O$ from the switch power losses for a 2-level buck converter.

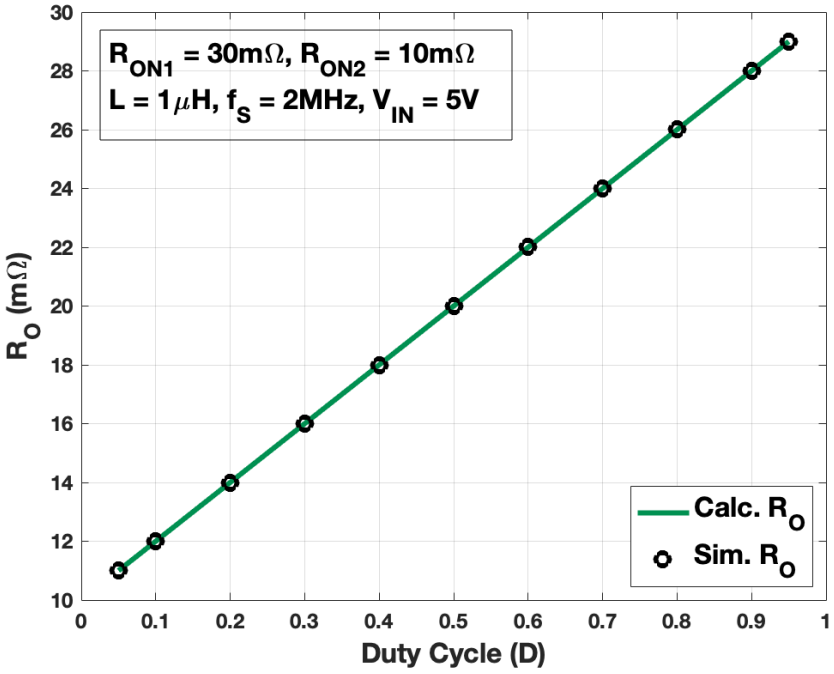



**Figure 2.16.** Calculated vs. Simulated $R_O$ for a 2-level buck converter.

# Chapter 3

# A Flying Inductor Hybrid Converter for 1-Cell and 2-Cell Battery Chargers

## 3.1 Background and Motivation

The feature count and performance of consumer mobile products have been increasing each year while their form factors continue to shrink. This annual increase in feature and performance densities has driven the need for higher-capacity batteries and thus battery charger solutions with higher power delivery capacity to maintain the trend of reduced charge times. The USB-C power-delivery (PD) specification [1] was developed to meet these higher demands by providing a programmable $V_{BUS}$ voltage range of 5V to 20V with up to 100W of power delivery which serves as the input source for the battery charger. These higher voltage settings also minimize input current levels and associated IR drops across the USB-C cable, preserving overall system efficiency while charging at these higher power levels. In order to take advantage of the benefits of USB-C power delivery for 1-cell (1S) and 2-cell series stack (2S) batteries found in many mobile phones and laptops, the DC-DC converter used for the charging solution needs to be efficient in both board space and power in order to meet product form-factor and on-board thermal management constraints.

While the traditional buck converter [30] has been a ubiquitous charger solution for most consumer products, recent hybrid step-down converter topologies that leverage the combinations of inductive pulse width modulation (PWM), switched capacitor (SC), and/or resonant operation

[9, 12, 13, 31–33] have presented themselves as potential candidates for these applications. However, similar to buck converters, these hybrid architectures require an inductor unfavorably located at the output side of the converter while the output current demand keeps increasing for faster charging. This necessitates an inductor with low DCR to minimize conduction losses and a high saturation current to ensure sufficient inductance is provided at full load; both of which imply larger component size. As is illustrated in Fig. 3.1, the DCR of compact surface-mount inductors of same value trends to an exponential increase as component volume shrinks. A similar undesirable trend can be found with saturation current ratings that diminishes dramatically with volume decrease. To address this challenge, multi-phase buck converters have been a viable option by dividing the total load current between multiple smaller inductors [34, 35]. Unfortunately, this solution increases the quantity of relatively expensive magnetic components required and the exponential increase in DCR of the smaller footprint inductors can still contribute significant conduction losses since the inductors process the full output current. In addition, any losses incurred by the inductor(s) for these solutions will generate heat within the product and further exacerbate the thermal management challenges in small form-factor designs.

To overcome this drawback of the conventional buck-like converters, it would be advantageous to utilize a topology that relocates the inductor to the lower-current input side while still achieving efficient step-down functionality with a continuous output voltage range. Doing so scales down the average current through the inductor by the converter step down ratio (M) resulting in a reduction in conduction losses in the inductor by a factor of $M^2$, simultaneously easing saturation current and DCR requirements for the inductor. Furthermore, moving the inductor to the input opens the possibility of utilizing the parasitic inductance of an input USB cable to replace the discrete inductor, completely removing the most bulky component from within the product and distributing its associated heat loss across the length of the cable. The concept of moving the inductor to the input has been explored in [36–40] with [36] demonstrating that the

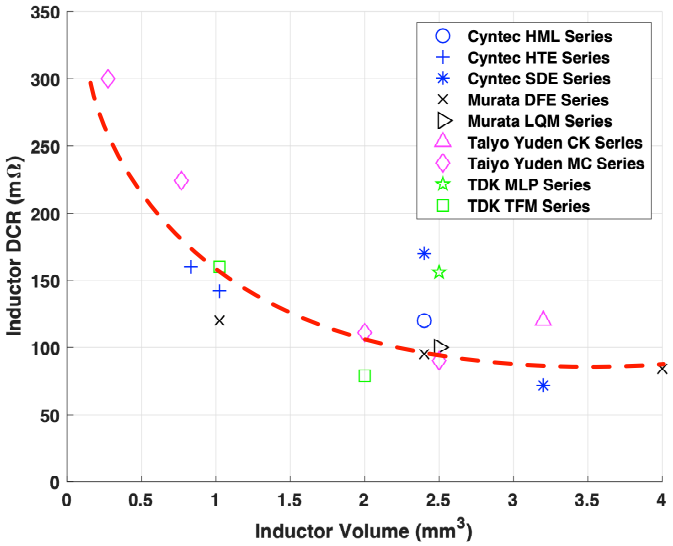



**Figure 3.1.** Survey of DCR vs. component volume for commercially available 1µH surface-mount inductors.

USB cable can be used to replace the role of the on-board inductor. However, the topologies proposed in these works do not provide conversion ratios or operating ranges suitable for 1S charging applications while taking advantage of the higher $V_{BUS}$ settings enabled by the USB-C PD specification.

In this chapter, we present a new hybrid converter topology that not only moves the inductor to the lower current input side, but also provides the conversion ratios needed to support

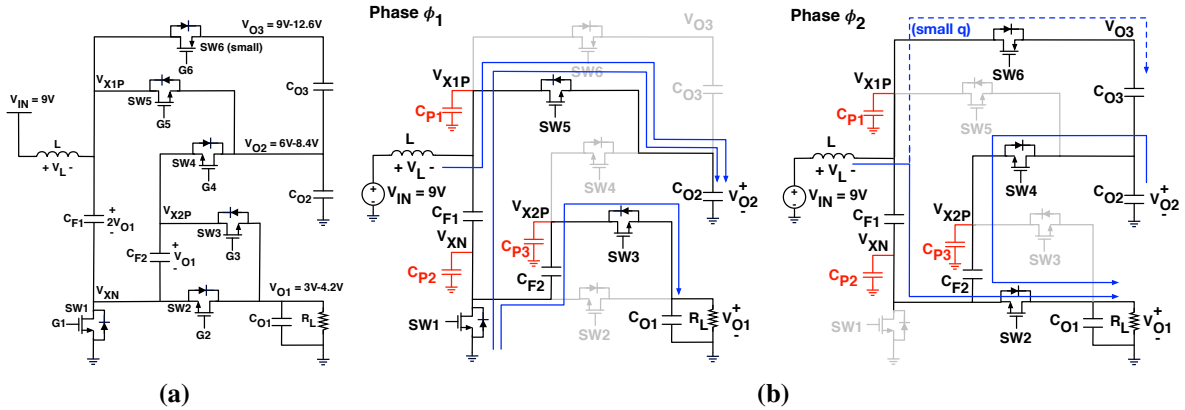



**Figure 3.2.** (a) Power stage of the proposed converter. (b) Operating phases and current flow when $V_{O1}$ is loaded.

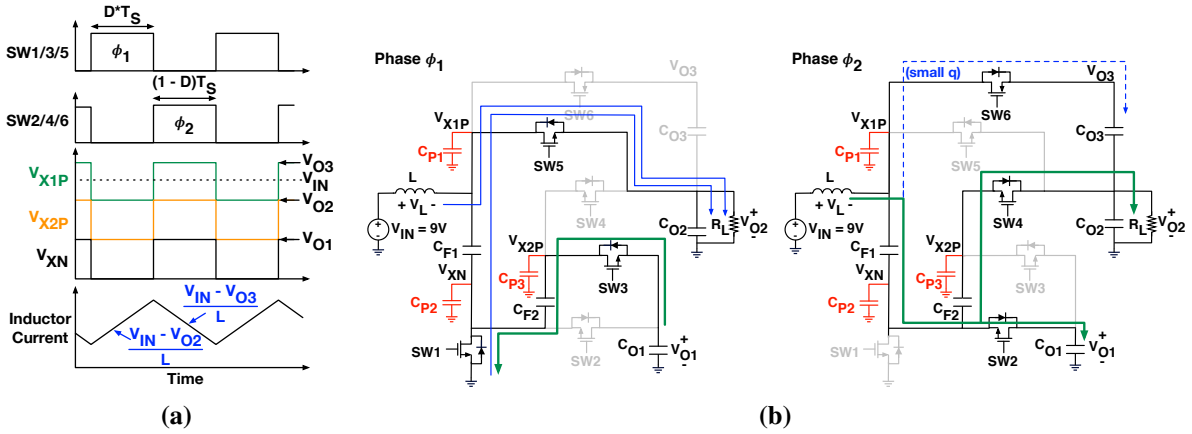



**Figure 3.3.** (a) Ideal switching waveforms. (b) Operating phases and current flow when $V_{O2}$ is loaded.

1S and 2S voltage ranges while operating from the higher 9V $V_{BUS}$ setting offered by USB-C PD [41]; providing a single converter solution for multiple charging applications. In Section 3.2, the fundamental operation of the power stage and the resulting conversion ratios for the multiple output paths will be discussed. A detailed loss analysis of the converter is then provided in Section 3.3. Implementation details of the converter prototype and critical sub-blocks are covered in Section 3.5. The measured performance of the fabricated prototype is reported in Section 3.6 with a discrete on-board inductor as well as with the inductor replaced by an off-the-shelf USB cable. Finally, in Section 3.7 we conclude the chapter with a brief summary of the salient points of this work.

## 3.2 Power Stage Topology and Operation

Figure 3.2a shows the power stage of the proposed converter. It consists of an input inductor, L, that directly feeds current into a SC network while providing partial soft charging benefits [9, 42]. The SC network is comprised of two flying capacitors, $C_{F1}$ and $C_{F2}$, and six switches (SW1-SW6). NMOS switches, SW1 through SW5, form the main power stage of the converter while a small PMOS switch, SW6, is used to source a small amount of charge to $C_{O3}$ which is used to power internal circuitry (to be discussed in Section 3.5). $V_{O1}$ and $V_{O2}$ are the

main outputs intended for 1S and 2S battery loads, respectively. Figure 3.2a illustrates the $V_{O1}$ loaded case.

Output voltage regulation is accomplished by duty cycle control in a two-phase operation. The two operating phases, $\phi_1$ and $\phi_2$, for the $V_{O1}$ loaded configuration are shown in Fig. 3.2b. The respective ideal timing waveforms are shown in Fig. 3.3a. During $\phi_1$, the inductor is connected between $V_{IN}$ and $V_{O2}$, where $V_{O2}$ is lower than $V_{IN}$, allowing the inductor current to ramp up at a rate of

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{O2}}{L} \tag{3.1}$$

During this phase, $C_{O2}$ receives charge from the inductor current and $C_{F1}$ while $C_{F2}$ discharges into $V_{O1}$. During $\phi_2$, the inductor is connected between $V_{IN}$ and $V_{O3}$, where $V_{O3}$ is higher than $V_{IN}$, allowing the inductor current to ramp down at a rate of

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{O3}}{L} \tag{3.2}$$

During this time, $C_{F1}$ is soft charged by the inductor current and passes charge to $V_{O1}$ while $C_{O2}$ charges $C_{F2}$ and also passes charge to $V_{O1}$. SW6 is also on during this phase to draw a small amount of charge to $C_{O3}$ to power internal circuitry. Since SW6 is small, it does not affect the soft-charging operation for $C_{F1}$. The soft charging and hard discharging behavior of $C_{F1}$ is illustrated in Fig. 3.4. Inserting a dead-time between phases also allows the parasitic capacitances $C_{P1}$, $C_{P2}$, and $C_{P3}$ to be soft charged by the inductor current during the $\phi_1$-to-$\phi_2$ transition, providing partial soft switching benefits to the converter.

As shown in Fig. 3.3a, the inductor is always tied to the top plate of $C_{F1}$ and flies between the $V_{O2}$ and $V_{O3}$ nodes, hence the name Flying-Inductor Hybrid (FIH) DC-DC Converter. Performing volt-sec balance analysis on the inductor yields the following conversion ratios for each output path

$$M_1 = \frac{V_{O1}}{V_{IN}} = \frac{1}{3-D} \tag{3.3}$$

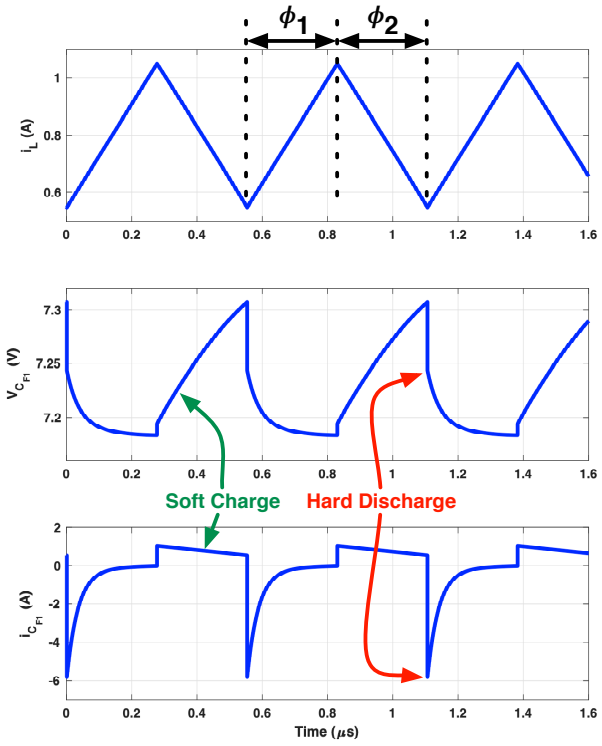



**Figure 3.4.** Soft charging and hard discharging waveforms of $C_{F1}$.

$$M_2 = \frac{V_{O2}}{V_{IN}} = \frac{2}{3-D} \tag{3.4}$$

$$M_3 = \frac{V_{O3}}{V_{IN}} = \frac{3}{3-D} \tag{3.5}$$

where $D$ is the duty cycle of SW1, SW3, and SW5. Evaluating equations (3.3), (3.4), and (3.5) across duty cycle, it can be seen that the two main output power paths through $V_{O1}$ and $V_{O2}$ provide step-down conversions while the $V_{O3}$ path provides a step-up conversion. Expressions (3.4), (3.5) and (3.3) shows that $M_2$ and $M_3$ are integer multiples of $M_1$, implying that the nominal $V_{O2}$ and $V_{O3}$ voltages are two and three times the unloaded $V_{O1}$ voltage, respectively. This also results in the maximum blocking voltage needed for each switch to be equal to $V_{O1}$, enabling the potential use of low-voltage switches, e.g. 5V, rather than high voltage devices to save die area and minimize switching and conduction losses.

The $V_{O2}$ loaded scenario is shown in Fig. 3.3b. The operation is primarily the same as the $V_{O1}$ loaded case except that the charge flow processing of $C_{F2}$ is different. As highlighted in green in Fig. 3.3b, during $\phi_1$ $C_{F2}$ is now charged by $C_{O1}$. During $\phi_2$, the inductor current now partially soft discharges $C_{F2}$ while passing charge to the load. This is not a complete soft discharge due to the voltage mismatches between $V_{O1} + V_{C_{F2}}$ and $V_{O2}$ similar to what was discussed in [12, 43].

From (3.1) and (3.4), the peak-to-peak inductor current ripple can be found to be

$$\Delta i_{L-hybrid} = \frac{DV_{IN}(1-M_2)}{Lf_S} \tag{3.6}$$

where $f_S$ is the switching frequency of the converter. From Fig. 3.3a and (3.6), two interesting observations can be made for the proposed topology:

1. The input current is continuous (similar to a boost converter) unlike a buck converter that exhibits high $di/dt$ due to discontinuities of pulsed input current. This characteristic of the

proposed hybrid converter promises advantages of low conducted EMI noise and minimal input filter similar to a boost converter while supporting a step-down functionality of a buck converter.

2. For the same inductance value and switching frequency $f_S$, the proposed converter exhibits significantly less peak-to-peak inductor current ripple over the conventional buck converter for the conversion ratios needed for 1S charging from a 9V input. To illustrate this, we first re-arrange (3.6) in terms of conversion ratio M

$$\Delta i_{L-hybrid} = \frac{V_{IN}(3M-1)(1-2M)}{MLf_S} \tag{3.7}$$

where M is the conversion ratio needed to provide a 1S output voltage range from a 9V input. Similarly, the inductor current ripple for a conventional buck can be expressed as

$$\Delta i_{L-buck} = \frac{V_{IN}M(1-M)}{Lf_S}. \tag{3.8}$$

By taking the ratio of (3.7) over (3.8) we have

$$\frac{\Delta i_{L-hybrid}}{\Delta i_{L-buck}} = \frac{(3M-1)(1-2M)}{M^2(1-M)} \tag{3.9}$$

A plot of (3.9) versus conversion ratio, M, is shown in Fig. 3.5 where it can be seen that at least a 2.4x reduction in current ripple is achievable over the necessary conversion ratios for 1S charging. For a discrete inductor implementation, this implies less magnetic AC losses and further reductions of the inductor overall RMS current.

## 3.3 Loss Analysis

In integrated power converter design, loss analysis is crucial to exposing the converter characteristics and giving insights to guide integrated circuit design. Therefore, this section

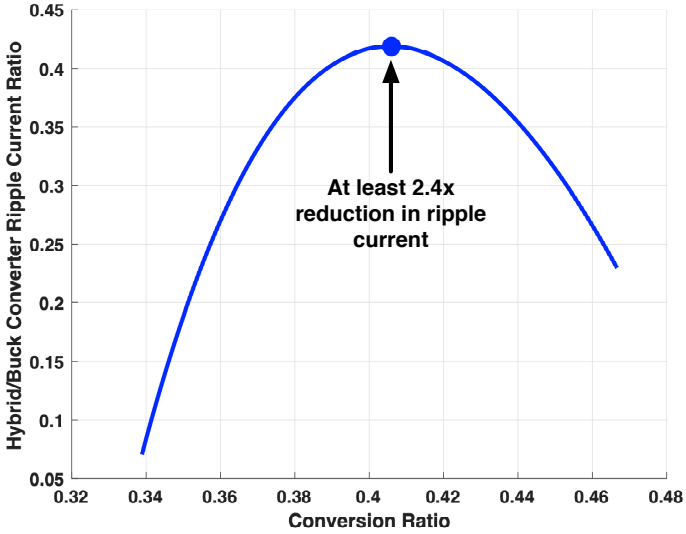



**Figure 3.5.** Inductor current ripple ratio of the proposed FIH Converter to buck converter versus conversion ratios necessary for 1S charging from a 9V input.

of the chapter is dedicated to analyzing key loss components and the output resistance of the proposed FIH converter, applying a similar method detailed in [3] with unique operations of the proposed converter. The converter design optimization using this loss analysis, however, is out of the scope of this chapter and will be presented in another suitable publication.

As described in Section 2.1 and [23], a DC-DC converter can be modeled as an ideal DC transformer whose turns ratio, $M$, is equal to the ideal conversion ratio of the converter as shown in Fig. 2.1. Since the proposed topology exhibits both soft charging and hard charging characteristics, these must be accounted for in the loss analysis. The output resistance, $R_O$, represents the output current dependent conduction losses of the converter which can be approximated as

$$R_O \approx \sqrt{(R_{SSL})^2 + (R_{FSL})^2} \tag{3.10}$$

where $R_{SSL}$ is the slow-switching limit (SSL) resistance which represents the conduction losses due to hard charge induced capacitor voltage ripple and $R_{FSL}$ is the fast-switching limit (FSL) which represents the conduction losses due to switch on-resistances and the parasitic equivalent

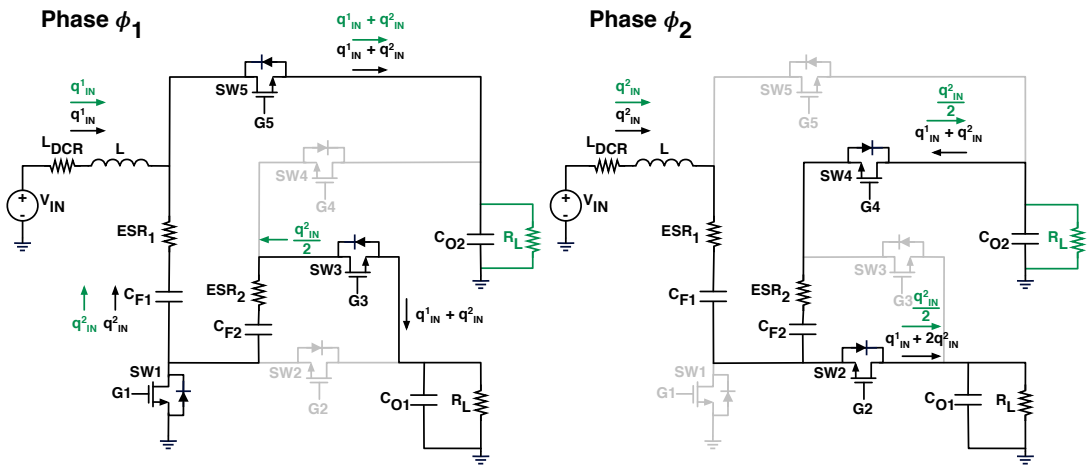



**Figure 3.6.** Charge flows for $V_{O1}$ loaded case. Differences of charge flows for $V_{O2}$ loaded case are in green text.

series resistances (ESR) of the reactive elements [3]. Parasitic layout resistances can also be accounted for by adding them to the appropriate component resistances. A charge flow based analysis can be applied to estimate the contributions of each of these loss mechanisms to the equivalent output resistance of the converter [3, 44]. Switching losses associated with the switch gate charge losses and switching node capacitance losses can also be approximated and summed with the conduction losses to estimate the overall efficiency of the converter.

Note that since the main power stage consists only of SW1 to SW5 and the two flying capacitors, SW6 and $C_{O3}$ have been omitted from the following loss analysis as their loss contributions are negligible.

### 3.3.1 SSL Resistance Contributions, $V_{O1}$ Loaded

The charge flows for the $V_{O1}$ loaded case are shown in Fig. 3.6 in black text. To facilitate the $R_{SSL}$ analysis, it is assumed that the inductor and output capacitors are of large value and the inductor behaves as a current source in both phases. With this assumption, the input charges $q^1_{IN}$ and $q^2_{IN}$, are defined as

$$q^1_{IN} = I_{IN} D T_S \tag{3.11}$$

$$q_{IN}^2 = I_{IN} D' T_S \tag{3.12}$$

where the superscripts in $q_{IN}^1$ and $q_{IN}^2$ indicate the operating phases, $I_{IN}$ is the inductor current, $D' = 1 - D$, and $T_S$ is the switching period. Analyzing the loss contribution of $C_{F1}$ first, it can be seen that $C_{F1}$ is soft-charged with a charge of $q_{IN}^2$ during $\phi_2$ and hard discharges that same charge in $\phi_1$ as illustrated in Fig. 3.4. This results in a voltage ripple across $C_{F1}$ equal to

$$\Delta V_{C_{F1}} = \frac{q_{IN}^2}{C_{F1}}. \tag{3.13}$$

Since $C_{F1}$ is softly charged during $\phi_2$ as described in Section 3.2, its power loss is

$$P_{loss,C_{F1},V_{O1}} = \frac{1}{2} C_{F1} (\Delta V_{C_{F1}})^2 f_s = \frac{(I_{IN} D')^2}{2 C_{F1} f_s} \tag{3.14}$$

where the $\frac{1}{2}$ factor in (3.14) accounts for the soft charging behavior.

Similarly, $C_{F2}$ is charged with $q_{IN}^1 + q_{IN}^2$ during $\phi_2$ and discharges that same charge during $\phi_1$ resulting in a voltage ripple across $C_{F2}$ equal to

$$\Delta V_{C_{F2}} = \frac{q_{IN}^1 + q_{IN}^2}{C_{F2}}. \tag{3.15}$$

Since in both phases this charge transferral occurs as a hard charge/discharge, the power loss associated with $C_{F2}$ is

$$P_{loss,C_{F2},V_{O1}} = C_{F2} (\Delta V_{C_{F2}})^2 f_S = \frac{(I_{IN})^2}{C_{F2} f_S}. \tag{3.16}$$

Therefore, the total $R_{SSL}$ loss for the $V_{O1}$ loaded case is

$$P_{SSL,V_{O1}} = \frac{(I_{IN} D')^2}{2 C_{F1} f_s} + \frac{(I_{IN})^2}{C_{F2} f_S}. \tag{3.17}$$

| Path | $a_{sw_1}$ | $a_{sw_2}$ | $a_{sw_3}$ | $a_{sw_4}$ | $a_{sw_5}$ |
|---|---|---|---|---|---|
| $V_{O1}$ | $(M_1)^2\frac{(2-D)^2}{D}$ | $(M_1)^2\frac{(2-D)^2}{D'}$ | $(M_1)^2\frac{1}{D}$ | $(M_1)^2\frac{1}{D'}$ | $(M_1)^2\frac{1}{D}$ |
| $V_{O2}$ | $(M_1)^2\frac{(D')^2}{D}$ | $(M_1)^2D'$ | $(M_1)^2\frac{(D')^2}{D}$ | $(M_1)^2D'$ | $(M_2)^2\frac{1}{D}$ |

**(a)**

| Path | $a_{esr_1}$ | $a_{esr_2}$ | $a_{dcr}$ |
|---|---|---|---|
| $V_{O1}$ | $(M_1)^2(D')^2\left(\frac{1}{D}+\frac{1}{D'}\right)$ | $(M_1)^2\left(\frac{1}{D}+\frac{1}{D'}\right)$ | $(M_1)^2$ |
| $V_{O2}$ | $(M_2)^2(D')^2\left(\frac{1}{D}+\frac{1}{D'}\right)$ | $(M_1)^2(D')^2\left(\frac{1}{D}+\frac{1}{D'}\right)$ | $(M_2)^2$ |

**(b)**

**Figure 3.7.** (a) FSL scale factors for each switch. (b) FSL scale factors for flying capacitor ESRs and inductor DCR.

From the ideal DC transformer model, we know that

$$I_{IN} = M_1 I_O \tag{3.18}$$

and substituting $R_O$ with $R_{SSL-V_{O1}}$ that

$$P_{SSL,V_{O1}} = (I_O)^2 R_{SSL-V_{O1}}. \tag{3.19}$$

Substituting (3.18) into (3.17), equating (3.17) to (3.19), and solving for $R_{SSL-V_{O1}}$, the output resistance contribution of the flying capacitors when $V_{O1}$ is loaded is

$$R_{SSL,V_{O1}} = \frac{(M_1)^2}{f_s}\left(\frac{(D')^2}{2C_{F1}} + \frac{1}{C_{F2}}\right). \tag{3.20}$$

### 3.3.2 FSL Resistance Contributions, $V_{O1}$ Loaded

Again using the charge flows annotated in black text in Fig. 3.6, the FSL contributions of the switch on-resistances, inductor DCR, and flying capacitors ESRs can be estimated. For this analysis, output capacitors $C_{O1}$ and $C_{O2}$ are assumed large and their ESR contributions are negligible. The inductor current ripple is again assumed small and the inductor is modeled as a current source.

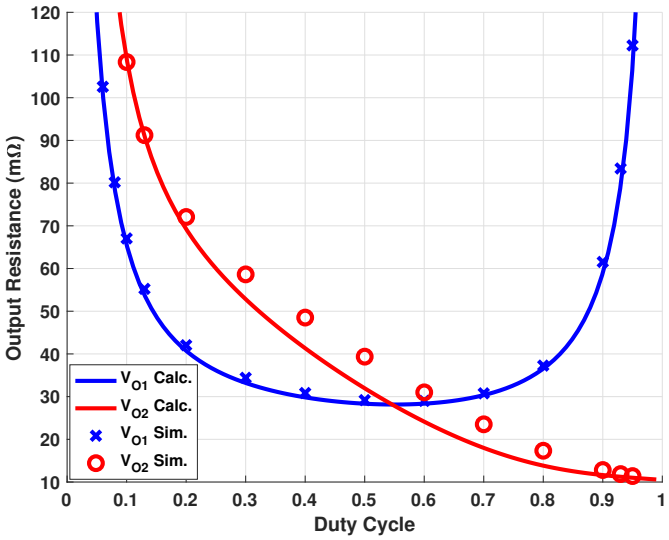



**Figure 3.8.** Output resistance vs. duty cycle for an example converter.

Turning to the switch loss contributions first, the energy loss of each switch is

$$E_{loss,sw_i} = (I_{sw_i})^2 R_{on_i} \Delta t_i \tag{3.21}$$

where $I_{sw_i}$ is the current flowing through $\mathrm{SW_i}$ while it is on, $R_{on_i}$ is the on-resistance of $\mathrm{SW_i}$, and $\Delta t_i$ is the time duration that $\mathrm{SW_i}$ is on. In FSL operation $I_{sw_i}$ can be approximated as a constant current [45]. Therefore, the current through $\mathrm{SW_i}$ is

$$I_{sw_i} = \frac{q_{sw_i}}{\Delta t_i} \tag{3.22}$$

where $q_{sw_i}$ is the charge processed by $\mathrm{SW_i}$. Substituting (3.22) into (3.21) and multiplying by $f_S$, the power loss associated with $\mathrm{SW_i}$ is

$$P_{loss,sw_i} = \left(\frac{q_{sw_i}}{\Delta t_i}\right)^2 R_{on_i} \Delta t_i f_S = \frac{(q_{sw_i})^2}{\Delta t_i} R_{on_i} f_S \tag{3.23}$$

For example, in the case of SW1, a total charge of $q_{sw1} = q_{IN}^1 + 2q_{IN}^2$ is processed by the switch and the switch is on for $\Delta t_i = DT_S$ amount of time where $q_{IN}^1$ and $q_{IN}^2$ are defined by (3.11) and

(3.12) respectively.

The same analysis can be repeated to calculate the losses of the capacitor ESRs, but taking into account that the ESRs process their respective flying capacitor charges in both phases. It can then be shown that their loss contributions are

$$P_{loss,ESR_1} = (q_{IN}^2)^2 (f_S)^2 ESR_1 \left( \frac{1}{D} + \frac{1}{D'} \right) \tag{3.24}$$

$$P_{loss,ESR_2} = (q_{IN}^1 + q_{IN}^2)^2 (f_S)^2 ESR_2 \left( \frac{1}{D} + \frac{1}{D'} \right) \tag{3.25}$$

where $ESR_1$ and $ESR_2$ are the ESRs of $C_{F1}$ and $C_{F2}$ respectively at the switching frequency.

Since the inductor DCR ($L_{DCR}$) always processes the inductor current charge, its loss contribution is simply

$$P_{loss,L_{DCR}} = (I_{IN})^2 L_{DCR} \tag{3.26}$$

Summing together (3.23), (3.24), (3.25), and (3.26) provides the total FSL power loss for the $V_{O1}$ loaded case.

$$P_{FSL,V_{O1}} = \sum_{i=1}^{5} P_{loss,sw_i} + \sum_{k=1}^{2} P_{loss,ESR_k} + P_{loss,L_{DCR}} \tag{3.27}$$

Also, from the ideal transformer model and substituting $R_O$ with $R_{FSL,V_{O1}}$,

$$P_{FSL,V_{O1}} = (I_O)^2 R_{FSL,V_{O1}} \tag{3.28}$$

Equating (3.27) and (3.28), substituting in (3.11), (3.12), and (3.18), and solving for $R_{FSL,V_{O1}}$ yeild the total FSL power loss as

$$R_{FSL,V_{O1}} = \sum_{i=1}^{5} a_{sw_i} R_{on_i} + \sum_{k=1}^{2} a_{esr_k} ESR_k + a_{dcr} L_{DCR} \tag{3.29}$$

where $a_{sw_i}$, $a_{esr_k}$, and $a_{dcr}$ are duty-cycle-dependent scale factors for each output-referred

resistive loss element. The values of each scale factor are summarized in Tables 3.7a and 3.7b.

### 3.3.3 SSL & FSL Resistance Contributions, $V_{O2}$ Loaded

The same charge flow analysis can be repeated for the $V_{O2}$ loaded scenario. However, the differences in charge flow from the $V_{O1}$ loaded configuration should be accounted for which are illustrated in green text in Fig. 3.6. Note that the analysis also omits any partial hard discharging of $C_{F2}$ due to voltage mismatches between $V_{O1} + V_{C_{F2}}$ and $V_{O2}$, which only has a minor impact on efficiency for this application.With this assumption, the output resistance contribution of the flying capacitors when $V_{O2}$ is loaded can be calculated as

$$R_{SSL,V_{O2}} = \frac{(M_2)^2 (D')^2}{2 f_S} \left( \frac{1}{C_{F1}} + \frac{1}{4 C_{F2}} \right). \tag{3.30}$$

The FSL resistance, $R_{FSL,V_{O2}}$, for the $V_{O2}$ loaded case has the same expression as (3.29) with different scale factors that are summarized in Tables 3.7a and 3.7b. Combining SSL and FSL resistances in (3.10) yields the output resistance.

### 3.3.4 Output Resistance Dependency on Duty Cycle

Constructing the output resistances for the $V_{O1}$ loaded and $V_{O2}$ loaded cases with equations (3.10), (3.20), (3.29), (3.30) using results in Tables 3.7a and 3.7b, it can be seen that the output resistances for both $V_{O1}$ and $V_{O2}$ loaded cases are dependent on duty cycle and the converter operating point, i.e. conversion ratio. This duty cycle dependency is a unique characteristic of this hybrid converter. It agrees with the utilization of the inductor in the converter, while being different from the analytical result for the SC converters in [3] using a similar approach of charge-based analysis.

To illustrate this phenomenon and the differences in effective output resistance for each output path, the relationship between output resistance and duty cycle for an example converter is plotted in Fig. 3.8.

## 3.4 Optimization Methodology

Having expressions for the loss mechanisms provides the opportunity to optimize the converter design in terms of power efficiency with minimal area. For this work, a Lagrange multiplier based optimization similar to [46] was utilized for the $V_{O1}$ loaded path with a target output of 3.6V and 5A.

### 3.4.1 Optimal Flying Capacitor Values

To find expressions for the optimal flying capacitor values for a given area, we first define the function we want to minimize as (3.20). A constraint expression in terms of area budget for the flying capacitors can be defined as

$$A_{C,tot} = \sum_{k=1}^{2} A_{C_k} = \frac{1}{2} \sum_{k=1}^{2} \frac{C_{Fk} V_{rk}^2}{m_{ck}} \tag{3.31}$$

where $A_{C_k}$ is the total area allowed for flying capacitor $C_{Fk}$, $V_{rk}$ is the voltage rating for capacitor $C_{Fk}$, and $m_{ck}$ is the energy storage density capability of the capacitor technology used for $C_{Fk}$. Setting (3.31) to zero and inserting it along with (3.20) into the Lagrange optimization equation results in

$$\mathscr{L} = \frac{M_1^2 (D')^2}{2 f_S} \frac{1}{C_{F1}} + \frac{M_1^2}{f_S} \frac{1}{C_{F2}} + \lambda \left( \frac{1}{2} \sum_{k=1}^{2} \frac{C_{Fk} V_{rk}^2}{m_{ck}} - A_{C,tot} \right). \tag{3.32}$$

Setting the partial derivatives of (3.32) with respect to $C_{F1}$, $C_{F2}$, and $\lambda$ to zero, and then solving the resulting system of equations results in the expressions for the optimal flying capacitor values for a given area.

$$C_{F1,opt} = \frac{D'}{V_{r1}} \frac{2 A_{C,tot} \sqrt{m_{c1}}}{\frac{D' V_{r1}}{\sqrt{m_{c1}}} + \frac{\sqrt{2} V_{r2}}{\sqrt{m_{c2}}}} \tag{3.33}$$

$$C_{F2,opt} = \frac{\sqrt{2}}{V_{r2}} \frac{2 A_{C,tot} \sqrt{m_{c2}}}{\frac{D' V_{r1}}{\sqrt{m_{c1}}} + \frac{\sqrt{2} V_{r2}}{\sqrt{m_{c2}}}} \tag{3.34}$$

### 3.4.2 Optimal Power Switch Sizes

To find expressions for the optimal switch sizes, we define the function to be minimized as

$$R_{FSL-V_{O1}} = \sum_{i=1}^{5} a_{sw_i} R_{on_i}. \tag{3.35}$$

A constraint expression in terms of switch area budget can be defined as

$$A_{sw,tot} = \sum_{i=1}^{5} \frac{G_{sw_i} V_{r,sw_i}^2}{m_{sw_i}} \tag{3.36}$$

where $G_{sw_i}$ is the conductance for SWi and $m_{sw_i}$ is the V-A product density for SWi. Inserting (3.35) and (3.36) into the Lagrange expression yields

$$\mathscr{L} = \sum_{i=1}^{5} \frac{a_{sw_i}}{G_{sw_i}} + \lambda \left( \sum_{i=1}^{5} \frac{G_{sw_i} V_{r,sw_i}^2}{m_{sw_i}} - A_{sw,tot} \right). \tag{3.37}$$

Setting the partial derivatives of (3.37) with respect to $G_{sw_i}$ and $\lambda$ to zero and solving the resulting system of equations provides the optimal switch conductances for a given area.

$$G_{sw_i,opt} = \frac{A_{sw,tot}}{\sum_{i=1}^{5} \left( \frac{\sqrt{a_{sw_i}} V_{r,sw_i}}{\sqrt{m_{sw_i}}} \right)} \frac{\sqrt{a_{sw_i} m_{sw_i}}}{V_{r,sw_i}} \tag{3.38}$$

### 3.4.3 Optimization Process & Results

The optimal flying capacitor values for a target area budget can be found by making use of (3.33) and (3.34). For this implementation, an initial target area for the flying capacitors was approximately equivalent to the areas of a single 0603 component and single a 0402 component. The estimated capacitance values for these capacitors after DC bias derating were approximately 3µF. The resulting optimal capacitor values were 1.5µF for $C_{F1}$ and 7.8µF for $C_{F2}$. However, since the capacitors are external to the chip the nearest value discrete capacitor that provides a biased value greater than or equal to the optimal value would need to be used. There would

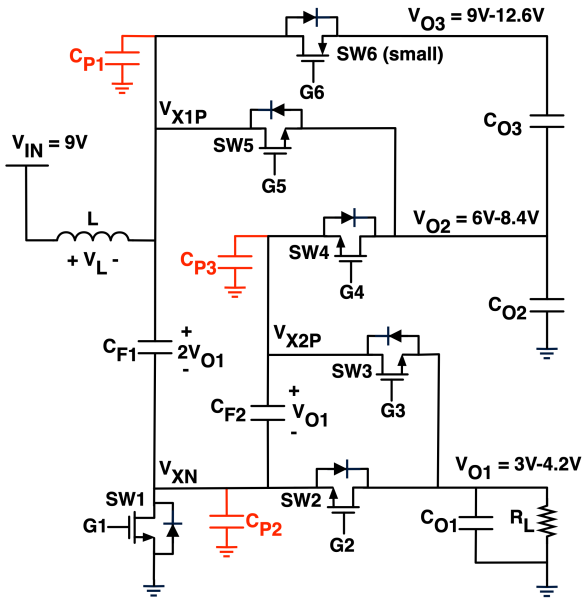



**Figure 3.9.** FIH power stage with switching node parasitic capacitors.

also be a compromise in the resolution of available case sizes to meet the optimal values so the initial capacitor area used in the optimization should only be considered an initial first pass approximation.

Fig. 3.9 shows the power stage with the parasitic flying node capacitances. Since each switching node has a voltage swing approximately equal to $V_{O1}$, the switching losses for the power stage can be estimated as

$$P_{SW} = f_S \left( \sum_{i=1}^{5} C_{gg_i} (V_{GS_i})^2 + \frac{(V_{O1})^2}{2} (C_{P1} + C_{P2} + C_{P3}) \right) \tag{3.39}$$

where $C_{gg_i}$ and $V_{GS_i}$ are the equivalent gate capacitance and gate-to-source voltage swing for SWi, respectively. Equation (3.39) neglects the gate charge loss related to SW6 since its size is negligible compared to the main power switches. It should also be noted that the factor of ½ in (3.39) is from the assumption that there is enough dead-time between $\phi_1$-to-$\phi_2$ transition for the parasitic capacitances $C_{P1}$, $C_{P2}$, and $C_{P3}$ to be soft charged by the inductor current.

After finding the capacitor values, the optimal switch sizes/area and switching frequency

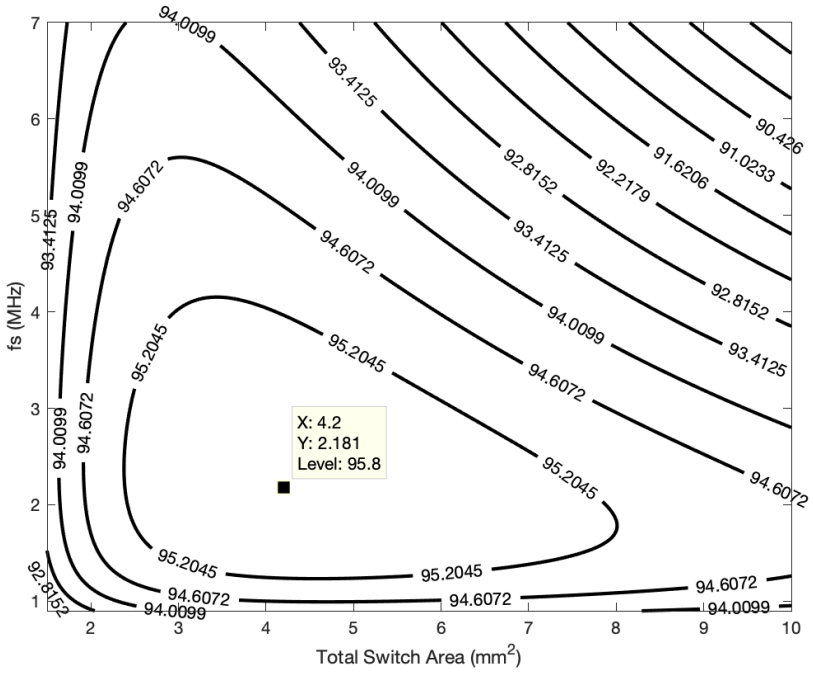



**Figure 3.10.** Contour plot of power efficiency optimization.

were found by employing (3.38), (3.39), and the loss model discussed in Section 3.3. The switch area and switching frequency were swept while calculating the estimated efficiency at each step and then identifying the global maxima efficiency value and corresponding switch area and switching frequency. A contour plot of the optimization with curves of constant efficiency and the annotated optimal sizing/operating point are shown in Fig. 3.10.

## 3.5 Implementation Details

The loss analysis details and insights above were used to guide the design of a converter prototype [41]. The system block diagram for the converter prototype is shown in Fig. 3.11 which is drawn assuming the $V_{O1}$ loaded scenario. For this initial prototype, a voltage mode control feedback loop was realized with an integrated OTA-based error amplifier (EA). A programming register was provided to allow optimization of switching frequency and dead-times during verification testing. A commercial version of the converter would require additional

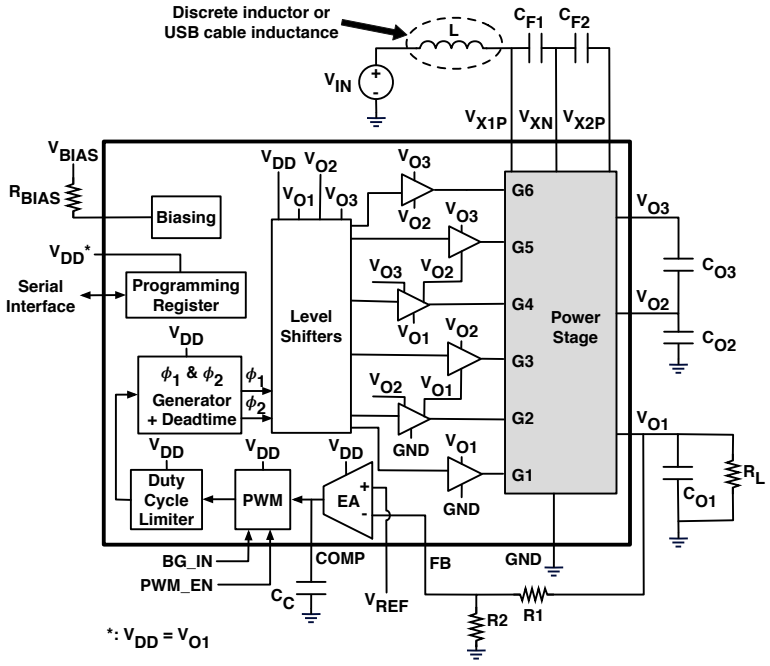



**Figure 3.11.** System block diagram of prototype converter.

support circuitry for converter start-up. However, for this initial prototype, external circuitry was employed to ensure proper start-up.

This section covers design details of key circuits and sub-blocks, including: 1) control signal routing and gate drivers, 2) gate signal level shifters, 3) a frequency generator, 4) a pulse width modulator with duty cycle limits to ensure robust operations of the power stage at minimum and maximum duty cycle extremes, and 5) non-overlapping clock generators. The error amplifier employs a standard folded-cascode structure as described in [47] and thus is not included in this chapter.

### 3.5.1 Control Signal Routing & Gate Drivers

The general control routing scheme for the power stage control is illustrated in Fig. 3.12. The design leverages the output voltages, $V_{O1}$, $V_{O2}$, and $V_{O3}$, generated by the converter to ensure power switch operation within the 5V gate oxide ratings for the majority of the power switches.

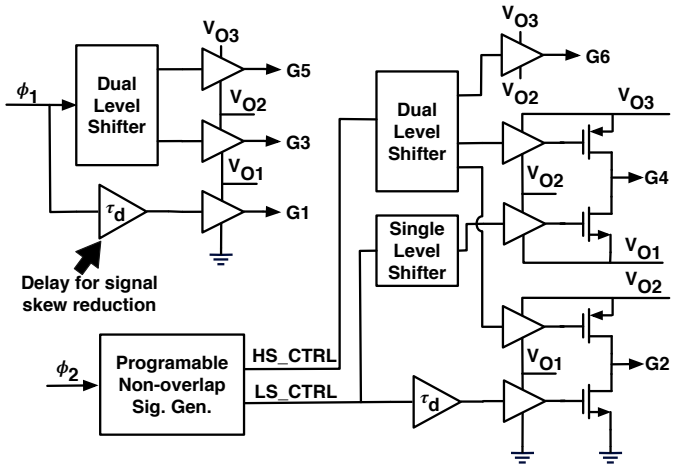



**Figure 3.12.** Control signal routing for power stage.

The gate drive signals G1, G3, G5, and G6 for switches SW1, SW3, SW5, and SW6, respectively, can be a version of $\phi_1$ or $\phi_2$ in $V_{O1}$-to-0V, $V_{O2}$-to-$V_{O1}$, or $V_{O3}$-to-$V_{O2}$ voltage domains taken directly from the level shifter outputs. Different from the other switches, SW2 and SW4 are unique in that they require their gate signals, G2 and G4, to cross two voltage domains, i.e. $V_{O2}$ to 0V or $V_{O3}$ to $V_{O1}$. In order to meet these signal ranges while not exceeding the device gate oxide rating, independently-controlled push-pull gate driver stages are utilized with a dedicated non-overlap signal generator to minimize shoot-through currents. Tuned delay blocks were also added to the shortest control signal paths to minimize signal skew between the various control signal paths.

### 3.5.2 Level Shifters

In order to provide the gate signals between different voltage domains described in Section 3.5.1 above, two varieties of level shifters whose schematics are shown in Fig. 3.13 are used. The core topologies for both level shifters are based on a cascode structure that feeds into a latch in a higher voltage domain, similar to the one reported in [48]. The latch is implemented using cross-coupled full CMOS inverters to ensure rail-to-rail signal swings at the level shifter outputs. To reduce latency while keeping the level shifter area small, MIM capacitors were used

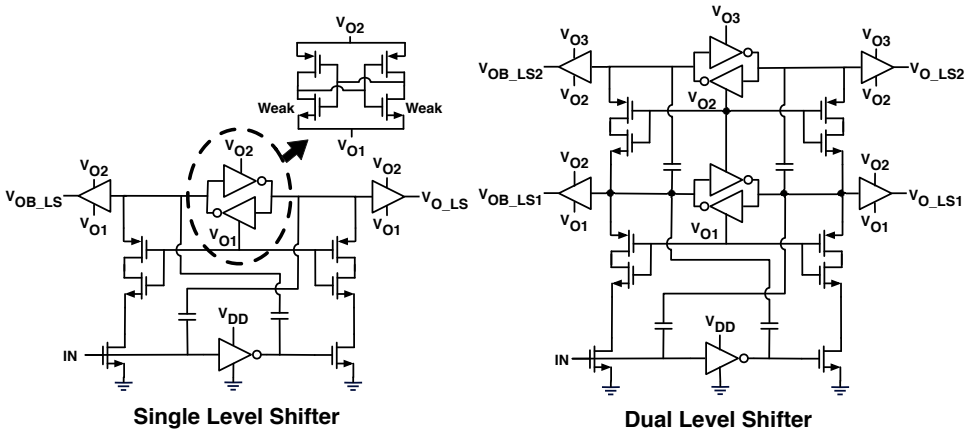



**Figure 3.13.** Single and dual level shifter schematics.

to couple signals between the different voltage domains. The NMOS devices in the latch were made weak to prevent excessive voltage drop across the MIM capacitors and additional losses during signal transitions. The dual level shifter is an extension of the single level version with the MIM capacitors connected in a stacked configuration across the voltage domains to ensure they operate within their specified voltage ratings, i.e. 5V in this technology.

### 3.5.3 Frequency Generator and Pulse Width Modulator with Duty Cycle Limits

The schematics of the frequency generator and the pulse width modulator with duty cycle limits are shown in Fig. 3.14. The frequency generator employs a CMOS relaxation oscilator with a casode current source (M4-M5) and a cascode current sink (M0-M1) generate the sawtooth oscillator waveform by charging a tune-able capacitor, $C_{OSC}$, through switches M2 and M3 [49]. The cascode current source and sink structures not only reduce variation in the ramp up/down times of the oscillator waveform, but also provide isolation for the NBIAS and PBIAS nodes from any switching noise generated by M2 and M3 for accurate frequency generation. Switches M2 and M3 are controlled by an RS latch that is driven by the outputs of the PCOMP comparators which compare the $C_{OSC}$ voltage to the BG_IN and REF_L voltages and determine the peak-to-peak swing of the oscillator waveform. The waveform is then level

shifted by a source follower stage (M6) to ensure the final output waveform OSC-OUT remains within the optimal input common mode range of the NCOMP comparator and the range of the OTA error amplifier output COMP, i.e. at the top plate of the compensation capacitor shown in Fig. 3.11.

The PWM signal is generated by comparing the error amplifier output COMP with the oscillator output OSC. A duty cycle limiter is added with logic gates U1-U3, an inverter, and a delay block to ensure robust operation of the power stage. The minimum on-time of the modulator, i.e. minimum duty cycle, is generated by the active high one-shot formed by the delay block, inverter, and U2 which is triggered by the RAMP output signal of the oscillator block. The minimum off-time, i.e. maximum duty cycle, is dictated by the values of the current sink and $C_{OSC}$ in the oscillator which determine the amount of time the RAMP signal, and thus PWM_OUT, is low. The duty cycle of PWM_OUT was designed to be within 5% and 95% to guarantee robust operations for the level shifters and power stages.

The PCOMP and NCOMP blocks consist of cross-coupled hysteretic comparators with push-pull output stages [50]. Their schematics are show in Fig. 3.15.

### 3.5.4 Non-overlapping Clock Generators

The schematic for the $\phi_1$ and $\phi_2$ non-overlapping clock generator is shown in Fig. 3.16. It consists of two logic gates and a programmable delay block. The programmable delay block is implemented with a chain of bypass-able coarse and fine delay sub-blocks that are enabled/disabled with the thermometer encoded control bits CS3-CS0 and FS3-FS0, respectively. The connection scheme allows the delay introduced by each coarse delay sub-block to be extended by the subsequent four fine delay blocks; allowing fine delay step sizes in between each coarse setting. The coarse delay sub-block consists of a set of MOS capacitors (M0-M1), a set of inverters, and an additional MIM capacitor, $C_{LONG}$, that can be inserted in the delay path by the LONG_EN control bit to further extend delay lengths. The fine delay blocks are similar in design except the MOS capacitors are omitted and the $C_{LONG}$ capacitor is of smaller value.

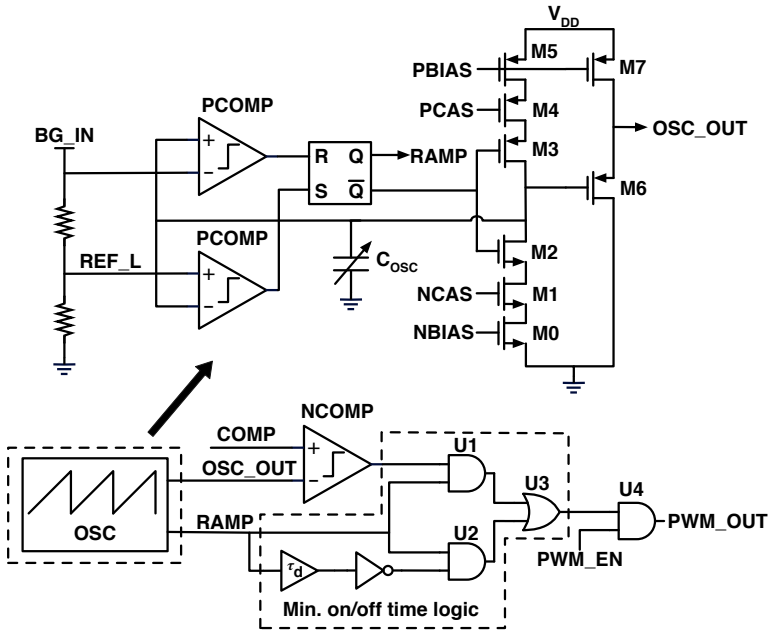



**Figure 3.14.** Schematics of a frequency generator and a pulse width modulator with duty cycle limits.

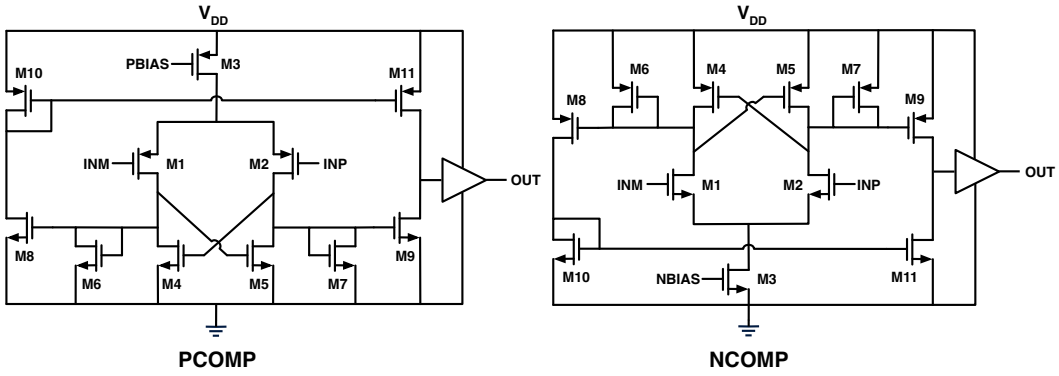



**Figure 3.15.** Oscillator and PWM comparator schematics.

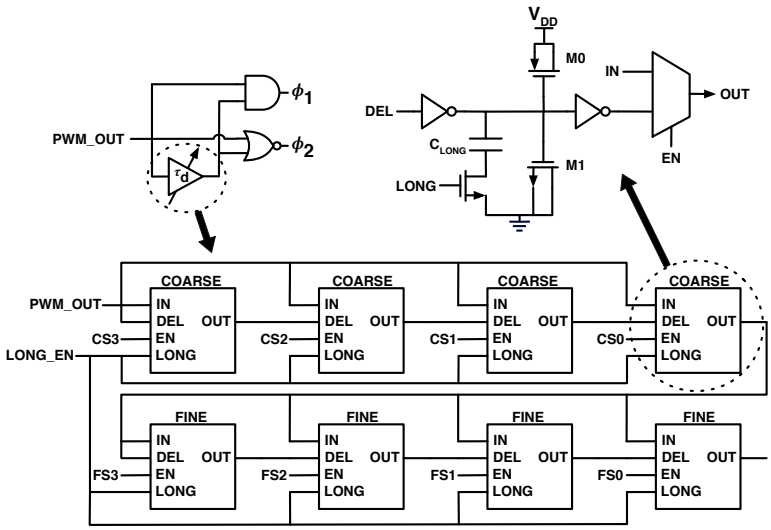



**Figure 3.16.** $\phi_1$ and $\phi_2$ non-overlapping clock generator schematic.

The delay block is designed for delays up to 5ns in 250ps steps when LONG_EN is disabled, or to 10ns in 500ps steps when LONG_EN is enabled. The same non-overlapping clock circuit is used for the generation of the HS_CTRL and LS_CTRL signals in Fig. 3.12 except the delay block only consists of the fine delay sub-blocks.

## 3.6 Experimental Verification

To verify the proposed converter architecture, a prototype was implemented in 7.37mm$^2$ of a 0.13µm BCD process applying the loss analysis, design insights, and circuit blocks presented above. Figure 3.17 shows the die micrograph with key block annotations. Flip-chip bumping was used to minimize package and PCB parasitics and associated losses. The chip pinout structure shown on the PCB footprint in Fig. 3.17 followed a careful design such that key power paths have short, low-loss access to PCB power traces and the converter could be evaluated on a low-cost PCB fabrication process, i.e. 220µm bump pitch and 3mil minimum spacing.

### 3.6.1 Performance with a Discrete Inductor

The design was first tested with a discrete 1µH inductor with 5.5mΩ of DCR to characterize the maximum performance of the chip. Two 0603 22µF and four 0402 10µF were

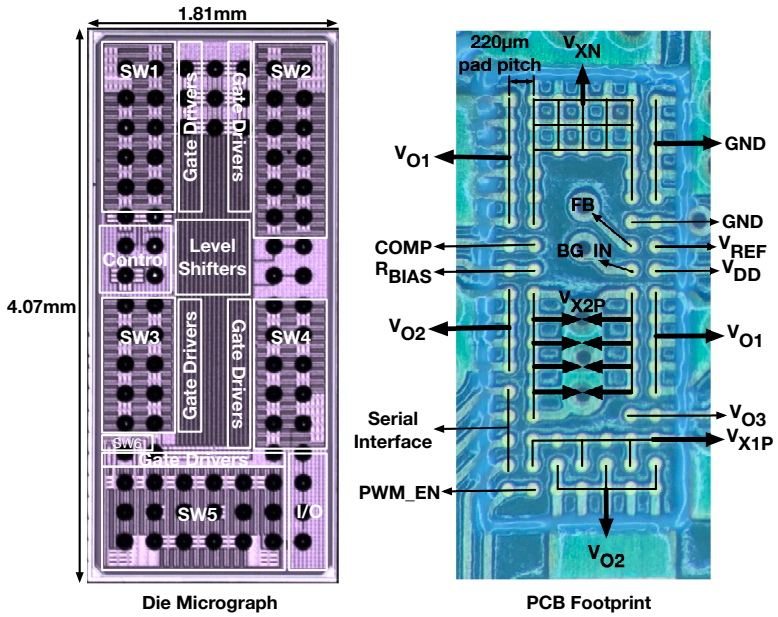



**Figure 3.17.** Die micrograph and PCB footprint with signal routing.

**Table 3.1.** Key components used for experiments with discrete inductor

| Component | Details |
|---|---|
| L | 1µH, 5.5mΩ, Coilcraft XFL4030 |
| $C_{F1}$ | 2 x 22µF, 10V 0603 (6.6µF) |
| $C_{F2}$ | 4 x 10µF, 6.3V 0402 (13µF) |
| $C_{O1}$ | 2 x 22µF, 10V 0603 (15µF) |
| $C_{O2}$ | 4 x 22µF, 10V 0603 (12µF) |
| $C_{O3}$ | 1 x 22µF, 10V 0603 (7.5µF) |

used for $C_{F1}$ and $C_{F2}$ to meet the recommended values determined in subsection 3.4.3 and to minimize the ESR loss contributions. The capacitors were chosen after an exhaustive search of available off-the-shelf components that have the best compromise of compact size, sufficient voltage ratings, and highest possible capacitance density. Table 3.1 provides a summary of the key components used for testing. The values in parentheses are the estimated effective total capacitances with DC bias. As the results show, the capacitance numbers above are approximately 65%-85% of the nominal unbiased values at normal operating conditions of the converters. It is also worth noting that the self resonant frequency (SRF) of the capacitors should be taken into consideration when selecting components to ensure the components remain capacitive at the operating frequency of 1.8–2.3 MHz.

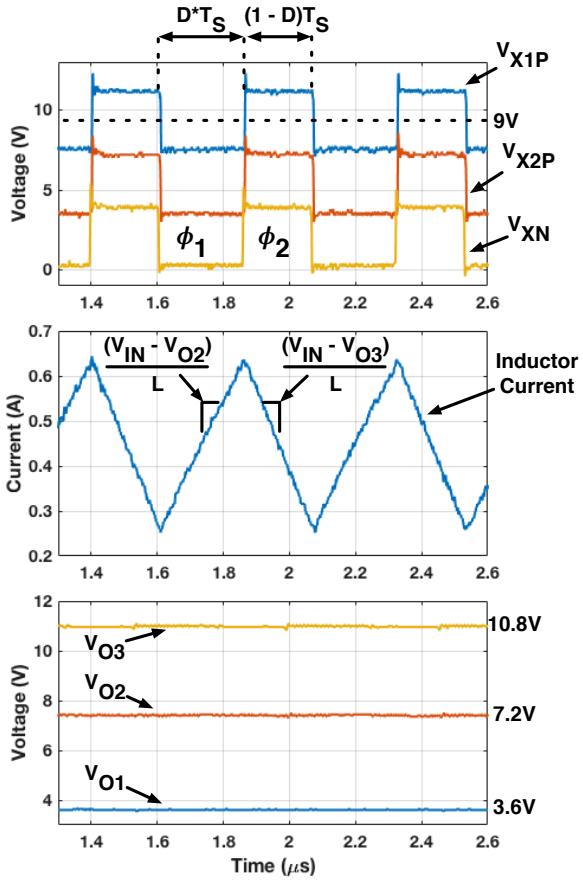
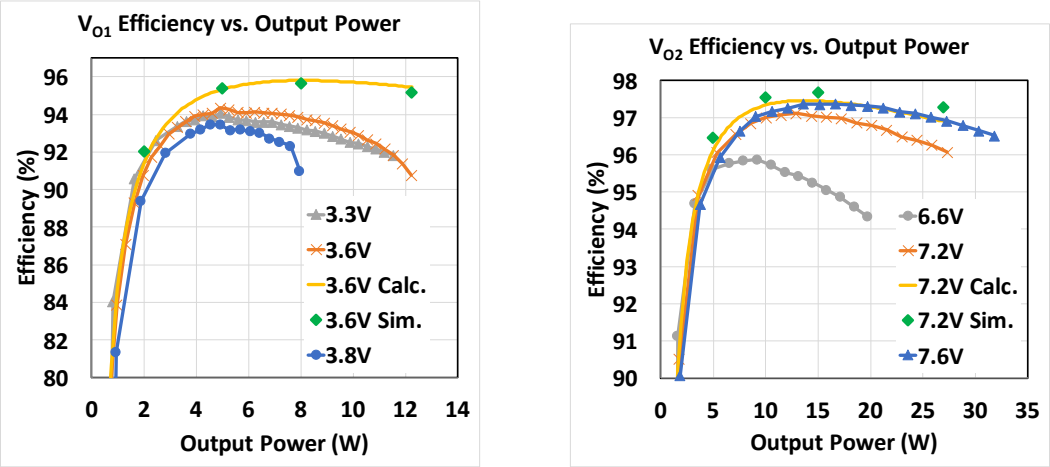



**Figure 3.18.** Measured steady-state waveforms with $V_{O1}$ regulated at 3.6V/1A.

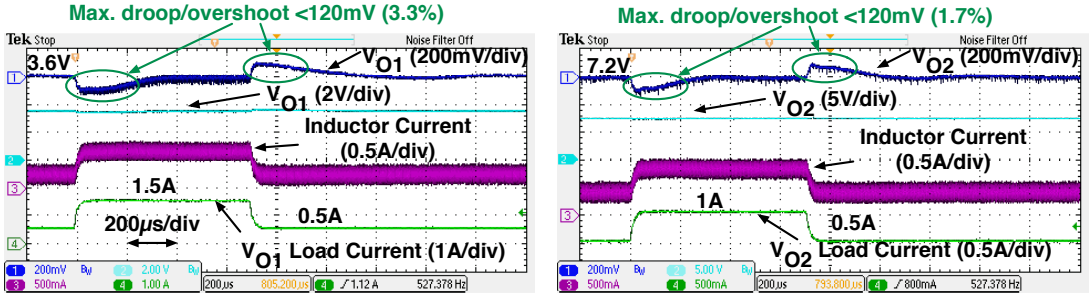
Figure 3.18 shows the measured steady state waveforms with $V_{O1}$ regulated to 3.6V while providing 1A of output current. The inductor node, $V_{X1P}$, flies between the $V_{O2}$ and $V_{O3}$ outputs, the inductor current slopes have the expected values, and the output voltages are near their nominal 50% duty cycle values, reflecting the theoretical operation shown in Fig. 3.3a.

The measured efficiency for the output power range of 1W up to ~12W for the $V_{O1}$ path at various output voltages is shown in Fig. 3.19a together with the analytically estimated and Spectre simulated efficiencies. At 3.6V output, the converter's peak efficiency of 94.3% was measured at 4.9W and its peak output power was 12.2W at 90.8% efficiency. It can be seen that the measured efficiency correlates well with the analytical model up until approximately 5W. It is believed that weaker than expected connections between the flip chip and evaluation PCB




(a) (b)

**Figure 3.19.** Measured efficiency (a) when $V_{O1}$ is loaded and (b) when $V_{O2}$ is loaded.




(a) (b)

**Figure 3.20.** Closed-loop load transient responses for (a) $V_{O1}$ and (b) $V_{O2}$.

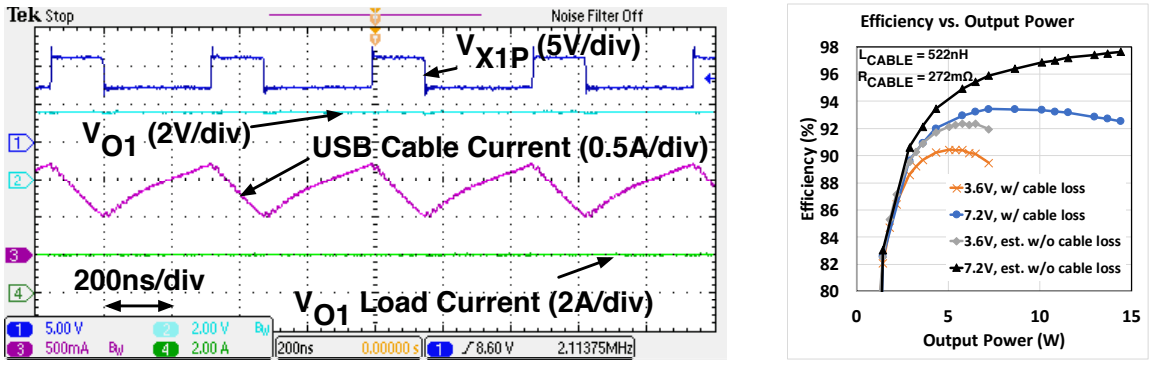
for the $V_{O1}$ path led to higher than expected conduction losses at the higher $V_{O1}$ output power range.

The measured power efficiencies for the $V_{O2}$ loaded case are shown in Fig. 3.19b. A peak efficiency of 97.4% was achieved at 7.6V/13.6W output and the maximum output power was 31.9W at 96.5% efficiency. As can be seen, the measured and analytical calculations match well with measured results. As explained in Sections 3.2 and 3.3, for the $V_{O2}$ path the charge is transferred more directly from the input to the output with less processing by the converter, leading to less current following in and out of the chip and thus less interconnect losses. This contributes to better converter performance and matching between analytical calculations and measured results. In Fig. 3.19b, there is a noticeable increase in efficiency at the higher output voltage levels for the $V_{O2}$ loaded case. This result reflects and agrees well with the output resistance versus duty cycle trend shown in Fig. 3.8 and related loss analysis in Section 3.3.

The closed loop dynamics for both outputs were also evaluated. For this prototype, a simple voltage mode Type-1 compensator was implemented for closed loop regulation. The loop is closed around the $V_{O1}$ or $V_{O2}$ output depending on the load connection. Figure 3.20 shows the measured transient responses at 1A and 0.5A load steps when the converter is regulated at $V_{O1}$=3.6V (Fig. 3.20a) or $V_{O2}$=7.2V (Fig. 3.20b), respectively. The output droops and overshoots are maintained below 120mV, or 3.3% of its nominal value, for $V_{O1}$ at 3.6V and 120mV, or 1.7% of its nominal value, for $V_{O2}$ at 7.2V.

### 3.6.2 Performance with a USB Cable - Smart-Cable Architecture

The converter was tested with the on-board inductor replaced by the parasitic inductance of a 1m USB cable that was measured at 522nH of inductance and 272m$\Omega$ of series resistance. The works in [36, 51] provide additional data on the range of inductances available across a variety of cables and consistency of values versus the physical orientation of the cable. A shorter cable with lower parasitic inductance could be utilized but at the cost of degraded efficiency due to higher current ripples.




(a) (b)

**Figure 3.21.** Measured (a) steady-state waveforms and (b) efficiency with a 1m USB cable.

The measured steady-state waveforms of the converter operating with the USB cable while the $V_{O1}$ output is regulated to 3.6V and delivering 7.2W is shown in Fig. 3.21a. For this test, the converter switching frequency was increased to 2.3MHz to help reduce the cable current ripple due to the reduced inductance. The measured efficiency with the USB cable is reported in Fig. 3.21b, including the overall efficiency with the cable losses as well as an estimate of the on-board efficiency without the cable losses. Accounting for only the on-board power losses, i.e. on-board heat dissipation, as the inductor-related losses are distributed across the cable, the converter achieved a peak on-board efficiency of 92.4% and maximum power of 7.2W when loaded at $V_{O1}$, limiting the on-board power dissipation to 630mW. When loaded at $V_{O2}$, the converter achieved a peak on-board efficiency of 97.6% and maximum output power of 14.4W, limiting the on-board power dissipation to 348mW. The slightly higher $V_{O2}$ peak on-board efficiency with the USB cable over the similar discrete inductor test scenario is likely caused by the fact that the converter operates at a higher duty cycle in the USB cable configuration (to compensate for additional cable IR drop) and thus results in a slightly lower effective output resistance for the converter compared to the discrete inductor test case, as explained in Section 3.3.

In order to confirm that USB communications can still be maintained while the converter is operating with the cable inductance, a file transfer experiment was performed while the

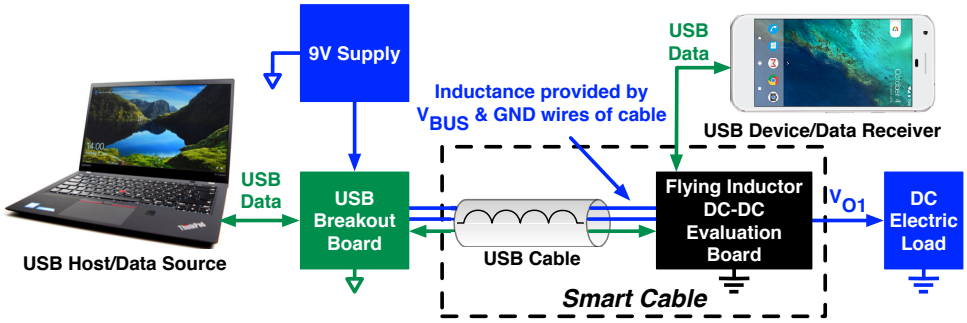



**Figure 3.22.** Block diagram of USB file transfer test setup.

converter was providing 6.5W at a regulated 3.6V. An illustration of the file transfer test setup is shown in Fig. 3.22. With this test setup, it was confirmed that a large media file could be reliably transferred between the USB host and USB device with no noticeable delay compared with a normal direct USB file transfer without converter operation. A video demonstration of the data transfer and measured power efficiency can be in the website media section of [21] for [52].

The USB cable in this demonstration can not only transmit data and deliver power but it is also a part of the power conversion stage for the battery charger, in which the significant loss associated with the inductor can be conveniently dissipated over the large surface of the cable. Therefore, this is called Smart-Cable architecture. It should be noted that this architecture does not require any external input bypass capacitors unlike a conventional buck converter since the flying node, $V_{X1P}$, is connected directly to the cable. Additionally, the proposed converter and Smart-Cable architecture enable the possibility of integrating the converter into the connector housing PCB; removing the charger converter, its associated passives and heat completely from the product. In this scenario, the converter would be permanently paired with a known cable inductance. The system could also detect whether a 1S or 2S device is connected to the Smart-Cable and connect it to the $V_{O1}$ or $V_{O2}$ outputs depending on the battery configuration; providing a single hardware solution for multiple charging applications.

### 3.6.3 EMI Performance with a USB Cable - Smart-Cable Architecture

In the Smart-Cable architecture described above, the USB cable is connected to a converter flying node and is being utilized to replace the inductor for power conversion. In this configuration, it is natural to suspect that radiated and conducted EMI would be a concern. To get a sense of the emissions performance of the converter in the Smart-Cable architecture, precursory EMI testing at a certified EMC lab was also conducted.

For radiated emissions, performance is highly dependent on the quality of the cable shielding and how it is terminated to the connector housings [53]. In typical USB cables, dedicated shields are provided for each of the data pairs in the wire bundle assembly in addition to a braid shield that wraps around the entire wire bundle [54, 55]. However, a dedicated shield is not provided for the $V_{BUS}$ and ground wires in the cable which are utilized as the converter inductor for this application. Since the $V_{BUS}$ wire is connected to a flying node ($V_{X1P}$) in this application, the $V_{BUS}$ and ground wire pair should also include a dedicated shield similar to the data pairs. For testing purposes, this was replicated by providing an additional shield around the cable that was terminated on each end to the respective power source and converter board grounds. Fig. 3.23 shows the block diagram and picture of the radiated EMI test setup and the resulting radiated quasi-peak measurement results are shown in Fig. 3.24 with the $V_{O1}$ output regulated at 3.6V and delivering 7.2W.

As it can be seen, with a properly shielded cable the converter's radiated noise is below the CISPR 22/32 Class B limits for both vertial and horizontal scans [53, 56]. Conventional EMI mitigation techniques such as spread-spectrum modulation of the switching frequency [57] could be used in future prototypes to further improve EMI performance and provide even more margin between the measured results and test limits.

As mentioned in Section 3.2, the continuous input current of the proposed topology should provide significant conducted EMI benefits over the conventional buck converter. To validate this, conducted EMI testing [53, 58] was also performed with a consumer grade 9V

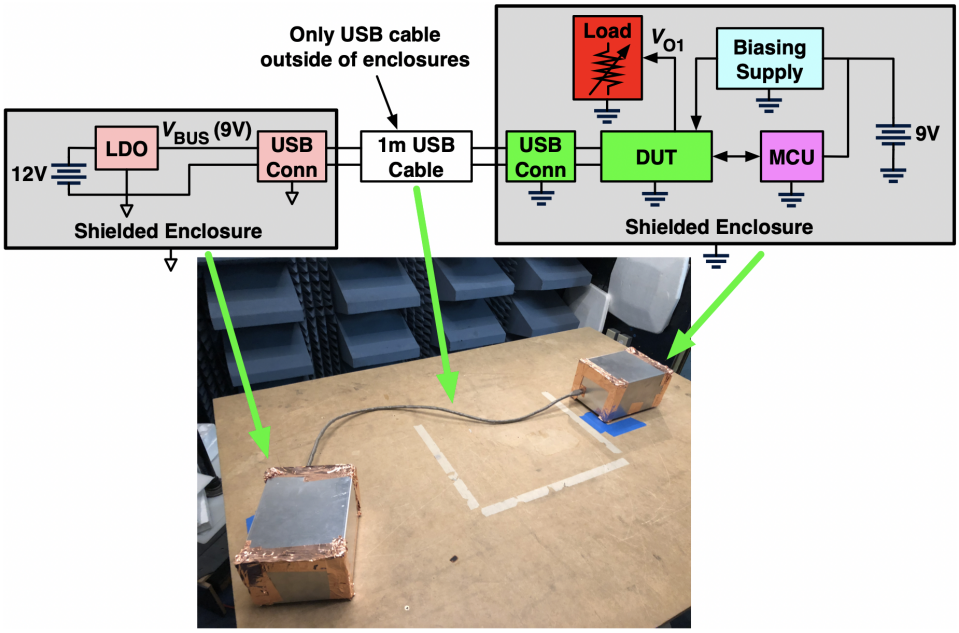



**Figure 3.23.** Block diagram and picture of radiated EMI test setup.

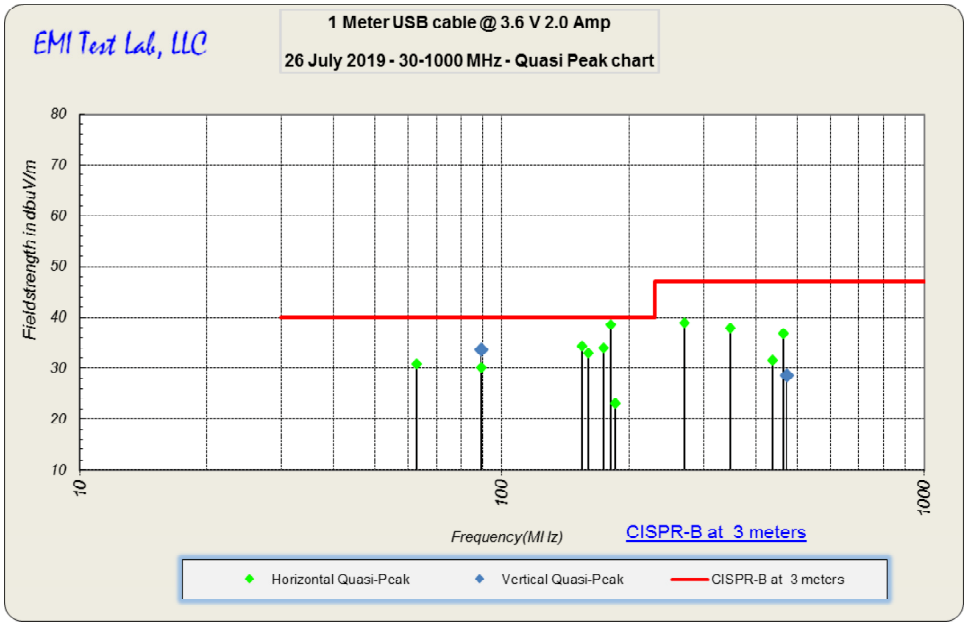



**Figure 3.24.** Radiated EMI test results with $V_{O1}$ delivering 7.2W.

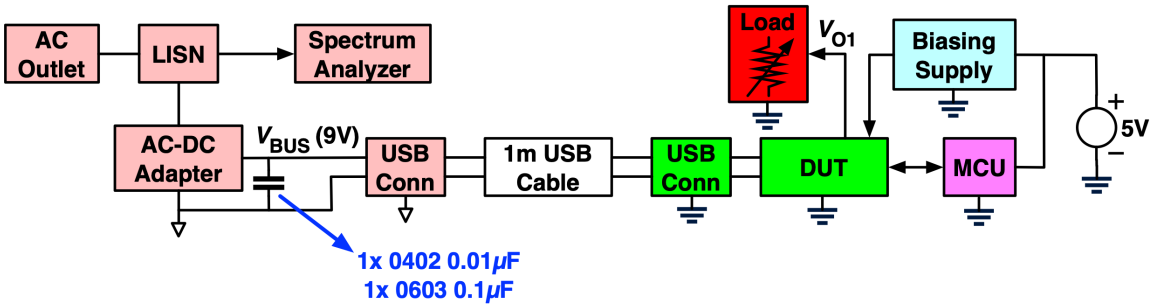



**Figure 3.25.** Block diagram of conducted EMI test setup.

AC-DC power supply. For this testing, a single 0402 0.01µF and a single 0603 0.1µF were added between the 9V supply output and ground at the AC-DC power supply. Fig. 3.25 shows the block diagram of the conducted EMI test setup. The quasi-peak and average results of the conducted line wire emissions testing are shown in Fig. 3.26 with the $V_{O1}$ output regulated at 3.6V and delivering 7.2W. As shown in the figure, the converter's conducted noise meets both the quasi-peak and average limits of the CISPR 22/32 Class B limits. It should be noted that compliance was achieved with as little as 110nF of additional bypass capacitance added to the input supply of the converter. This is signficantly less that what is typically required for a conventional buck to meet conducted EMI compliance [59]. The conducted neutral wire emissions were also tested and yielded similar performance.

### 3.6.4 Comparison to Prior Work

Table 3.2 provides a comprehensive comparison to the prior works reported in [9, 31, 36, 39, 59]. The converters presented in [9, 31, 59] provide reasonably high conversion ratios, but have their inductors located at the higher output current side which would require large component sizes for high current applications. The converter in [31] was also shown to have a very limited output range making it unsuitable for battery charging applications. [36, 39] both presented hybrid converters with input-located inductors, however [36] was demonstrated as a discrete implementation and did not provide conversion ratios necessary for 1S battery charging from a 9V input while [39] was limited for low voltage applications.

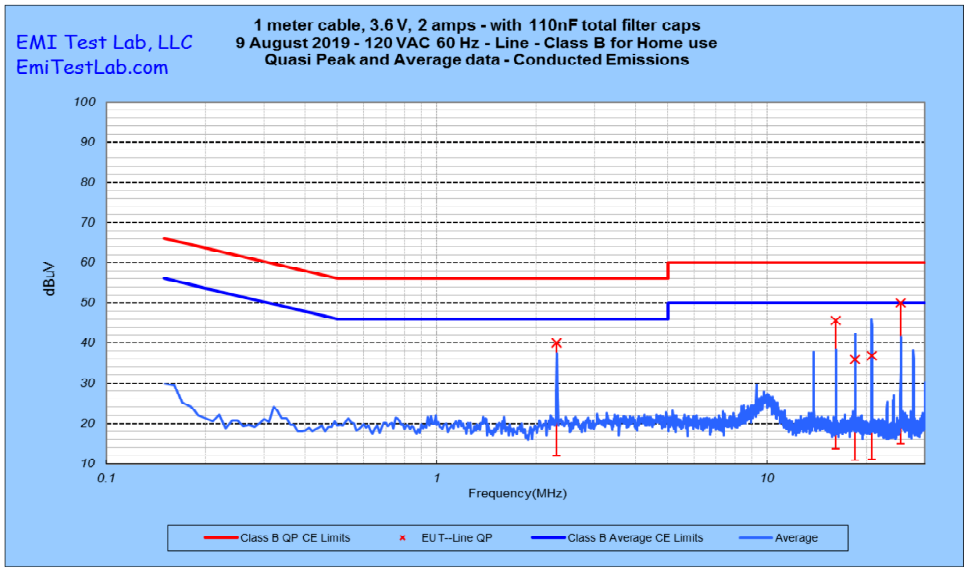



**Figure 3.26.** Conducted EMI test results with $V_{O1}$ delivering 7.2W.

**Table 3.2.** Comparison with Prior Works

| | **This Work** | TI TPS84621 | W. Liu ISSCC '17 | C. Schaef JESTPE '18 | G. Seo APEC '17 | A. Abdulslam ISSCC '19 |
|---|---|---|---|---|---|---|
| Topology | **Hybrid** | Buck | Hybrid | ReSC | Hybrid | Hybrid |
| Inductor location | **Input** | Output | Output | Output | Input | Input |
| Input voltage [V] | **9** | 4.5 - 14.5 | 3 - 4.5 | 12 | 5 | 1.8 |
| Output voltage [V] | **3 - 4.2 (6 - 8.4)** | 0.6 - 5.5 | 0.3 - 1 | 3.5 - 3.8 | 3.3 - 3.8 | 0.5 - 1.5 |
| Integrated regulation | **Yes** | Yes | Yes | Yes | No | Yes |
| Peak output power [W] | **12.2 (31.9)^** | 30* | 1.24* | 4.62 | 15** | 3.5* |
| Peak efficiency w/ discrete inductor [%] | **94.3 (97.4)^** | 95* | 94.2 | 87 | — | 94 |
| Peak on-board efficiency w/ USB [%] | **92.4 (97.6)^^** | — | — | — | 91.5* | — |
| Peak power density, die area only [W/mm$^2$] | **1.66 (4.33)^** | — | 0.31* | 0.47* | — | 1.89* |
| Peak power density, die + passives [W/mm$^2$] | **0.35 (0.69)**** | 0.14 | 0.12 | 0.38 | — | 0.64 |
| Peak output current [A] | **3.4 (4.2)** | 6 | 1.53 | 1.24* | 3.9 | 2.5 |
| Supports two-cell charging*** | **Yes** | No | No | No | No | No |
| Switching frequency [MHz] | **1.8 - 2.3** | 0.25 - 0.78 | 0.2 - 5 | 1.7 | 2 | 6.5 |
| Process | **130nm BCD** | — | 65nm CMOS | 180nm CMOS | Discrete | 180nm CMOS |

*Estimation from reported measurement results, **With USB cable, ***Capable of providing 2S output voltage range from 9V input.
^1µH discrete inductor, ^^522nH cable inductance, all values in parenthesis are for the $V_{O2}$ output

This work has demonstrated one of the first integrated circuit implementations of a hybrid step down converter with the inductor located at the lower input current side. It efficiently achieves the conversion ratios needed to take advantage of the higher 9V USB-C $V_{BUS}$ setting while delivering high output powers utilizing a discrete input inductor or the parasitic inductance of a USB cable and zero on-board magnetics. Additionally, the same converter can be employed for both 1S and 2S battery charging applications.

## 3.7 Conclusion

As mobile product sizes and charge times continue to shrink while power, performance, and feature counts continue to increase year over year, there is a clear need for battery charger solutions to evolve with the products they support. This chapter has demonstrated a new hybrid topology that could be used to bridge this gap. By moving the inductor to the input and taking advantage of the benefits of SC networks, this new converter not only efficiently delivers the conversion ratios needed for charging 1S and 2S batteries from a USB-C source but also enables the possibility of eliminating all on-board magnetics associated with the charger converter with the Smart-Cable architecture.

A detailed loss analysis was provided for this new topology as well as simulation and measurement results to corroborate the expected output powers and efficiencies. Closed loop regulation and dynamics were demonstrated indicating stable operation for both main output power paths. Radiated and conducted EMI testings were performed to prove the system solution can pass the stringent CISPR 22/32 Class B compliance limit. Additionally, a large media file was transferred across the USB cable during converter operation, demonstrating a new potential charger solution where the USB cable is not only used for data transmission and power delivery, but also for power conversion.

## 3.8 Acknowledgment

Chapter 3 is based on and mostly a reprint of the following publications [41, 52]:

- C. Hardy and H. Le, "8.3 A 10.9W 93.4%-Efficient (27W 97%-Efficient) Flying-Inductor Hybrid DC-DC Converter Suitable for 1-Cell (2-Cell) Battery Charging Applications," in 2019 IEEE International Solid- State Circuits Conference - (ISSCC), Feb. 2019, pp. 150–152.

- C. Hardy, Y. Ramadass, K. Scoones, and H.-P. Le, "A Flying-Inductor Hybrid DC-DC

Converter for 1-Cell and 2-Cell Smart-Cable Battery Chargers," IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3292–3305, Dec. 2019.

The dissertation author is the primary author of these publications and the co-authors have approved the use of the material for this dissertation.

# Chapter 4

# A Reconfigurable Single Inductor Multi-stage Hybrid Converter for 1-Cell Battery Chargers

## 4.1 Background and Motivation

The ongoing demand for smaller form factors and faster charging times of mobile products continue to drive the need for efficient, high-density power delivery (PD) for charging with a wide input voltage ($V_{IN}$) range of 5V–20V, offered by USB-C PD. A converter solution that efficiently takes advantage of this wide $V_{IN}$ range while providing an output voltage ($V_O$) range suitable for battery charging (2.8V–4.2V) remains challenging but highly desirable. Hybrid converters and their associated benefits provide a path to meet this challenge.

The advantages of reduced voltage blocking requirements for power switches and higher effective switching frequency to promote reduced inductor sizes have been demonstrated in [7, 8, 18] but with limited $V_{IN}$ ranges that are unable to support the full USB-C PD range. Many recent works have also explored hybrid converters that merge operation of more complex switched capacitor (SC) and switched inductor (SI) topologies with the goal of efficiently realizing higher $V_{IN}/V_O$ step-down voltage conversion ratios (VCRs) in mind [10, 14, 15, 17, 60]. However, these examples have limited VCR ranges as they are solely focused on achieving high step-down VCRs. Other new topologies such as the ones presented in [51, 52] move the inductor to the

lower input current side of the converter while still achieving step-down VCRs. While these examples provide significant inductor current reductions proportional to their respective VCRs, they do no provide high enough step-down VCRs to support the full USB-C PD voltage range.

The work presented in this chapter attempts to address these shortcomings by extending the concepts of merged multi-stage hybrid converters. It also extends the concepts of power stage reconfigurability for efficient VCR realization, which is something that has been demonstrated extensively for SC converters [4, 5, 24, 61] but not yet explored for hybrid converters.

## 4.2 Topology Concepts

Fig. 4.1 provides simplified high level concepts for various hybrid step-down converter configurations as well as some implementation examples. As shown in each configuration in the top of Fig. 4.1 it is assumed there is a circuit element present that can emulated the behavior of a current source to provide soft-charging benefits to the SC stages. If the converters operate at a high enough switching frequency ($f_S$) for given inductor value (L) such that a small ripple approximation can be applied to the inductor current [23] then the current sources in each configuration can be realized with an inductor.

Fig. 4.1(a) shows what is likely the most common configuration where the current source/inductor is placed at the output. The simplest topology example of this configuration is the 3-level buck converter [7, 8, 18]. In this particular example, the flying capacitor (C) is completely soft charged and discharged by the inductor current while providing the additional benefits of higher effective $f_S$, reduced voltage blocking requirements for the power switches, and a wide theoretical step-down VCR range of 0–1 but at the expense of having the inductor at the high output current path. Fig. 4.1(b) shows a less common step-down configuration where the current source/inductor is located at the input. An early example topology of this configuration was proposed in [37] and was further expanded up in [51] where it was referred to as the S-Hybrid converter which is shown in Fig. 4.1(b). Another discrete implementation

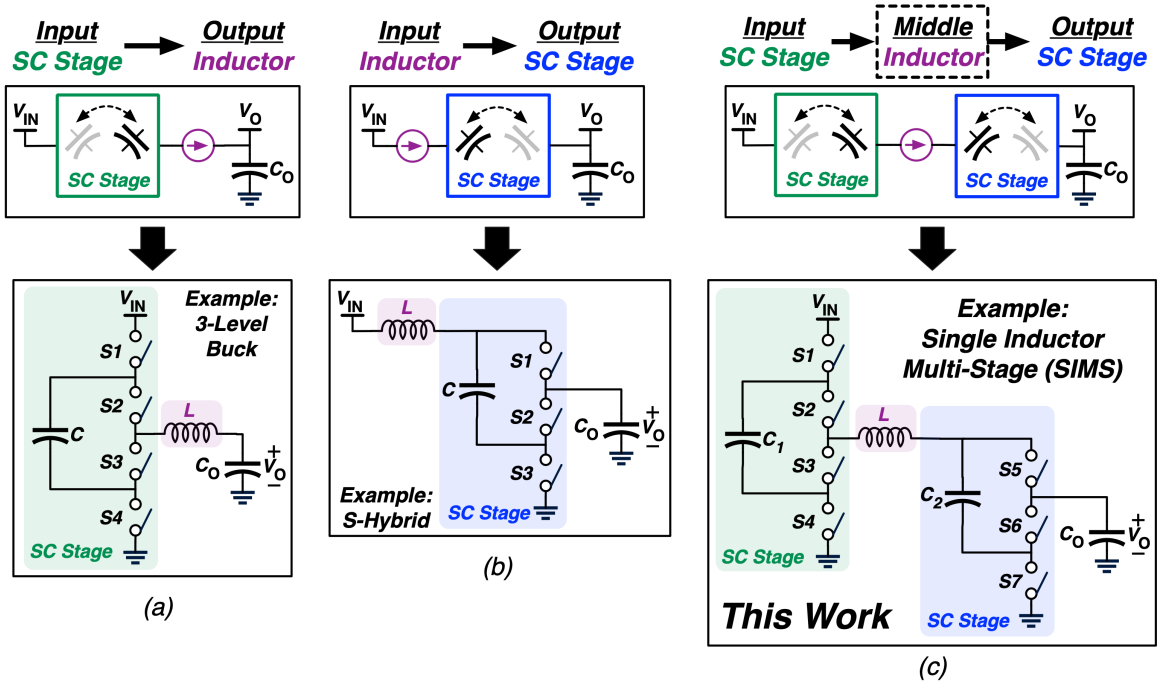



**Figure 4.1.** High level diagrams and examples of hybrid converter configurations with the inductor at the output (a), input (b), and in the middle (c).

including a detailed loss analysis was discussed in [38] and an integrated implementation was also demonstrated in [40]. The topology provides the added benefits of DC inductor current reduction proportional to its VCR, partial soft charging benefits of the flying capacitor (C), and reduction of the switch blocking voltage requirements to $V_O$. However, its theoretical step-down VCR range is limited to 0.5–1. This work is focused on the new configuration shown in Fig. 4.1(c) where the current source/inductor is used to couple two SC stages to further extend the VCR capabilities of the converter while also providing soft charging benefits to each stage, reducing the DC inductor current, and reducing switch voltage blocking requirements. The proposed example implementation of this configuration, which will be the focus of the remainder of this chapter, is also shown in Fig. 4.1(c). At initial inspection, it can be seen that it utilizes the topologies shown in Figs. 4.1(a) and 4.1(b). However, as will be shown in subsequent sections, it also leverages SC reconfiguration concepts to maintain high efficiencies over an extended VCR range.

## 4.3 Power Stage and Operating Modes

The power stage with the power switch device implementation is shown in Fig. 4.2. During steady-state operation the first stage flying capacitor voltage ($V_{C1}$) is equal to $V_{IN}/2$ or $V_{IN}$ depending on the operating mode and the second stage flying capacitor voltage ($V_{C2}$) is equal to $V_O$ for all operating modes. As indicated the figure, each side of the inductor is connected to a switching node that is capable of providing multiple voltage levels depending on the mode of operation. The LX switching node has three possible voltage levels ($V_{IN}$, $V_{IN}/2$, or 0V) while the C2P switching node has two possible voltage levels ($V_O$ or $2V_O$). Since the inductor is located between the two SC stages, the DC inductor current ($I_L$) reduced to a level equal to output current ($I_O$) scaled down by the conversion ratio of the second stage. The converter has 4 primary operating modes: Lower Series-Parallel (LSP), Lower Parallel-Series (LPS), Upper Parallel-Series (UPS), and Bypass Parallel-Series (BPS) which will be described in more detail the following subsections. It should be noted that for all modes, the duty cycle (D) is defined as the duration of $T_S/2$, that is used to energize the inductor where $T_S$ is the converter switching period. This is slightly different from other conventional switching converters where D corresponds to the on-time duration of a specific power switch.

### 4.3.1 Lower Series-Parallel Mode (LSP) Operation

Fig. 4.3 shows the LSP mode operating states and switching waveforms. As shown in Fig. 4.3a, this mode has 3 unique switching states. The steady-state DC voltages across the flying capacitors, $C_1$ and $C_2$, are $V_{IN}/2$ and $V_O$ respectively. During State A, both $C_1$ and $C_2$ are soft charged by the inductor current ($I_L$) and the inductor current ramps up at a rate of

$$\frac{V_{IN}/2 - 2V_O}{L}.$$

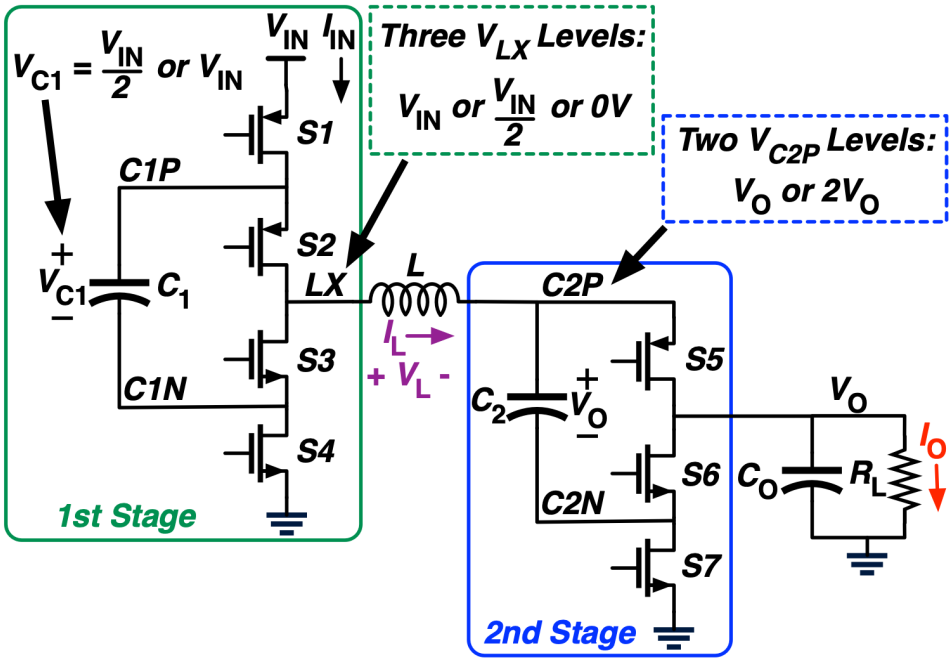



**Figure 4.2.** SIMS converter power stage, switching node voltage levels, and voltage conversion ratios.

During State B, $C_2$ is hard discharged into $V_O$ and the inductor current ramps down at a rate of

$$\frac{-V_O}{L}.$$

In State C, $C_1$ is soft discharged by $I_L$ while $C_2$ is soft charged and the inductor current ramps up at rate equal to that of State A. Finally, State B is repeated to complete the full switch period ($T_S$). Performing volt-sec balance analysis over the switching period results in a VCR of

$$M_{V-LSP} = \frac{V_O}{V_{IN}} = \frac{D}{2(1+D)} \tag{4.1}$$

while analyzing the charge flow for the inductor and flying capacitors results in

$$M_{I-LSP} = \frac{I_L}{I_O} = \frac{1}{1+D} \tag{4.2}$$

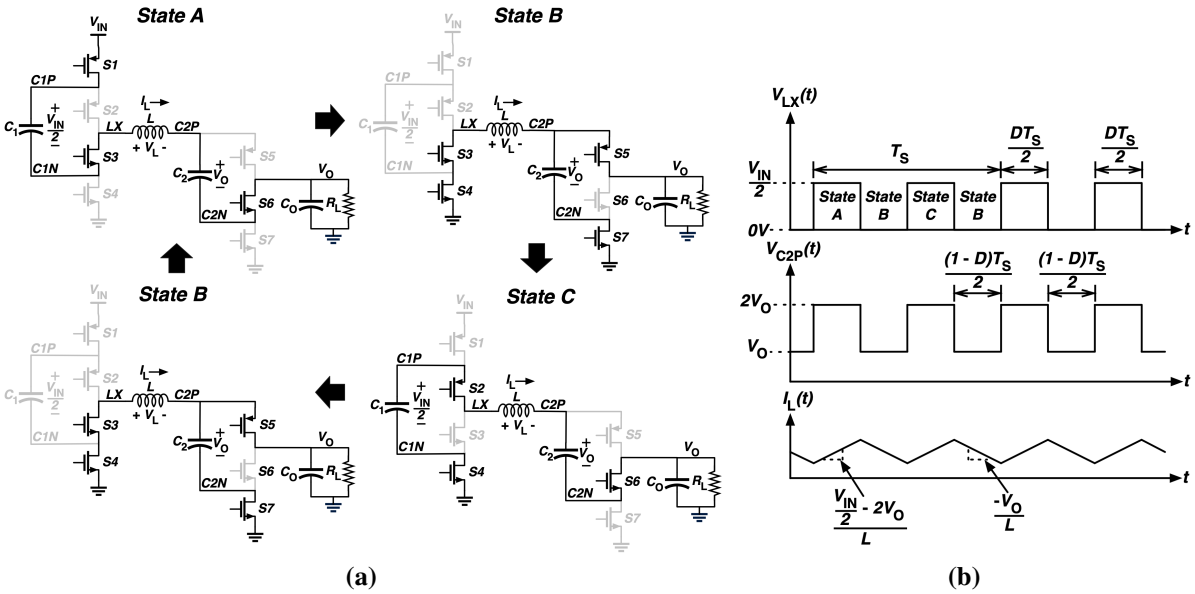



**Figure 4.3.** LSP mode (a) operating states and (b) switching node and inductor current waveforms.

where $I_L$ and $I_O$ are the DC inductor and output currents, respectively. From the inductor current ramp rate expressions and (4.1) is can also be shown that the peak-to-peak inductor current ripple is

$$\Delta i_{L-LSP} = \frac{V_{IN}}{2Lf_S} \frac{M_{V-LSP} - 4(M_{V-LSP})^2}{1 - 2M_{V-LSP}} \tag{4.3}$$

where $f_S$ is the switching frequency ($f_S = 1/T_S$).

### 4.3.2 Lower Parallel-Series Mode (LPS) Operation

Fig. 4.4 shows the LPS mode operating states and switching waveforms. This mode is almost identical to LSP mode except that the second stage operating phase is inverted. As shown in Fig. 4.4a, this mode also has 3 unique switching states and the steady-state DC voltages across the flying capacitors are the same as in LSP mode. During State A, $C_1$ is soft charged by the inductor current while $C_2$ is hard discharged to the output and the inductor current ramps up at a rate of

$$\frac{V_{IN}/2 - V_O}{L}.$$

During State B, $C_2$ is soft charged by the inductor current while it ramps down at a rate of

$$\frac{-2V_O}{L}.$$

In State C, $C_1$ is soft discharged by $I_L$ while $C_2$ is hard discharged and the inductor current ramps up at a rate equal to that of State A. Finally, State B is repeated to complete the full switching period. Performing volt-sec balance analysis over the switching period results in a VCR of

$$M_{V-LPS} = \frac{V_O}{V_{IN}} = \frac{D}{2(2-D)} \tag{4.4}$$

while analyzing the charge flow for the inductor and flying capacitors results in

$$M_{I-LPS} = \frac{I_L}{I_O} = \frac{1}{2-D} \tag{4.5}$$

and the resulting peak-to-peak inductor current ripple is

$$\Delta i_{L-LPS} = \frac{V_{IN}}{2Lf_S} \frac{2M_{V-LPS} - 4(M_{V-LPS})^2}{1+2M_{V-LPS}}. \tag{4.6}$$

### 4.3.3 Upper Parallel-Series Mode (UPS) Operation

Fig. 4.5 shows the UPS mode operating states and switching waveforms. As shown in Fig. 4.5a, this mode also has 3 unique switching states and the steady-state DC voltages across the flying capacitors are the same as the LSP and LPS modes with the major difference in this mode being that the LX node is connected directly to $V_{IN}$ during State A. In this state, the inductor current ramps up at a rate of

$$\frac{V_{IN} - V_O}{L}$$

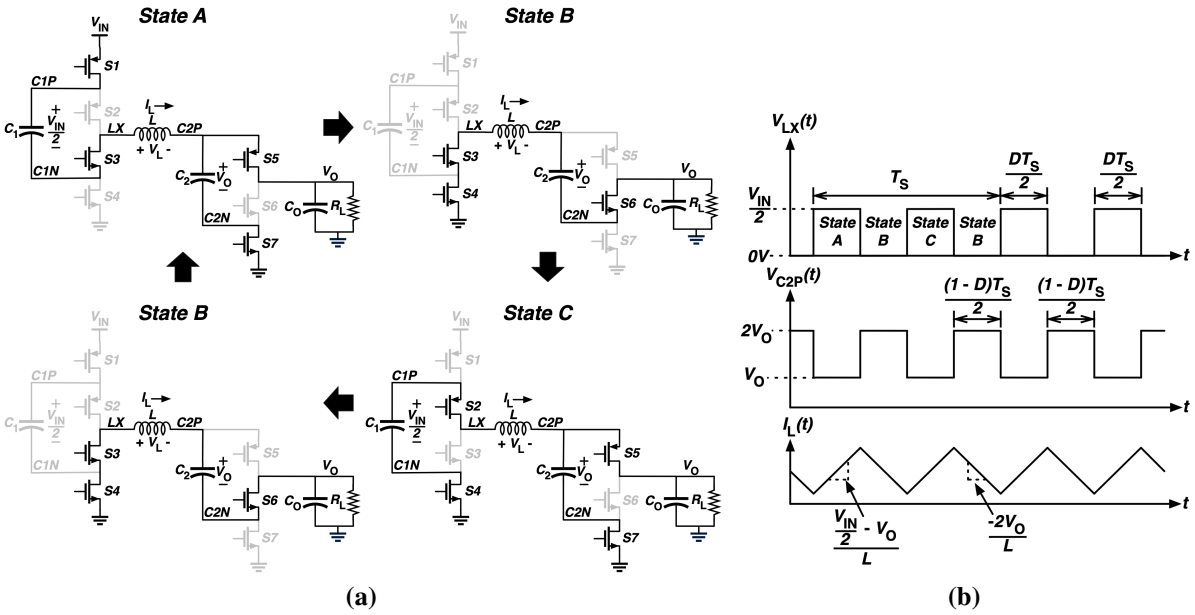



**Figure 4.4.** LPS mode (a) operating states and (b) switching node and inductor current waveforms.

while $C_2$ is hard discharged to the output. In State B, both flying capacitors are soft charged by the inductor current which ramps down at a rate of

$$\frac{V_{IN}/2 - V_O}{L}.$$

State A is then repeated and the inductor current ramps down while $C_2$ is again hard discharged to the output. Finally, State C soft discharges $C_1$ while $C_2$ is soft charged to complete the full switching period. Performing volt-sec balance analysis over $T_S$ results in a VCR of

$$M_{V-UPS} = \frac{V_O}{V_{IN}} = \frac{1+D}{2(2-D)} \tag{4.7}$$

while analyzing the charge flow for the inductor and flying capacitors results in

$$M_{I-UPS} = \frac{I_L}{I_O} = \frac{1}{2-D} \tag{4.8}$$

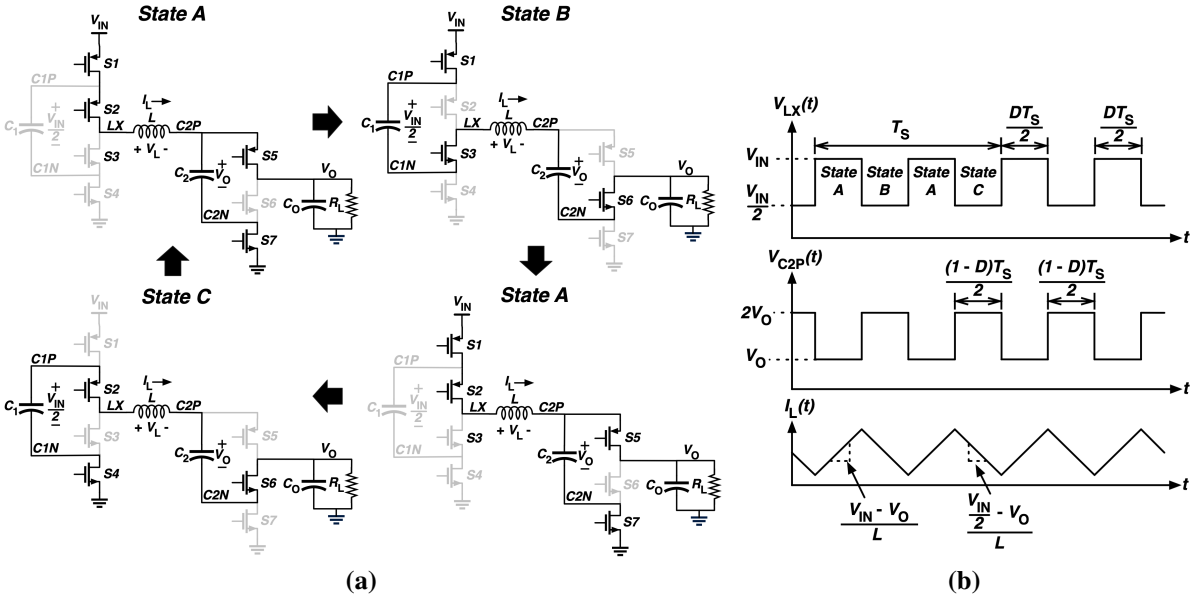



**Figure 4.5.** UPS mode (a) operating states and (b) switching node and inductor current waveforms.

and the resulting peak-to-peak inductor current ripple is

$$\Delta i_{L-UPS} = \frac{V_{IN}}{2Lf_S}(1 - M_{V-UPS})\left(\frac{4M_{V-UPS} - 1}{2M_{V-UPS} + 1}\right). \tag{4.9}$$

### 4.3.4 Bypass Parallel-Series Mode (BPS) Operation

The operating states and switching waveforms for the final primary mode, BPS mode, are shown in Fig. 4.6. As can be seen, this mode consists of only two unique switching states and $C_1$ is repurposed as an additional input bypass capacitor with the LX node voltage fixed at $V_{IN}$. Therefore, $C_1$ has a voltage of $V_{IN}$ across it while $C_2$ continues to have a steady-state DC voltage of $V_O$ as with the other modes. Note that in order to maintain consistency in the timing conventions used in the converter analysis and expressions for all modes, the $T_S$ is still defined as the time needed to complete for state transitions (i.e. 2 cycles of States A and B in Fig. 4.6b

for one $T_S$). In State A, the inductor current ramps up at a rate of

$$\frac{V_{IN} - V_O}{L}$$

while $C_2$ is hard discharged to the output. Then in State B, the inductor soft charges $C_2$ while the inductor current ramps down at a rate of

$$\frac{V_{IN} - 2V_O}{L}.$$

States A and B are then repeated to complete the $T_S$ switching period. Performing volt-sec balance analysis over $T_S$ results in a VCR of

$$M_{V-BPS} = \frac{V_O}{V_{IN}} = \frac{1}{2-D} \tag{4.10}$$

while analyzing the charge flow for the inductor and flying capacitors results in

$$M_{I-BPS} = \frac{I_L}{I_O} = \frac{1}{2-D} \tag{4.11}$$

and the resulting peak-to-peak inductor current ripple is

$$\Delta i_{L-BPS} = \frac{V_{IN}}{2Lf_S}\left(3 - \frac{1}{M_{V-BPS}} - 2M_{V-BPS}\right). \tag{4.12}$$

### 4.3.5 Summary of Conversion Ratios Across Modes

Fig. 4.1 provides a summary of all the main converter modes including simplified representations of the switching states. To illustrate the versatility the different modes offer from the perspective of VCRs, Fig. 4.7 shows the ideal VCR vs. D and modes where $M_{V\text{-}x}$ is general variable representing the VCR for the various modes. As can be seen from the plot,

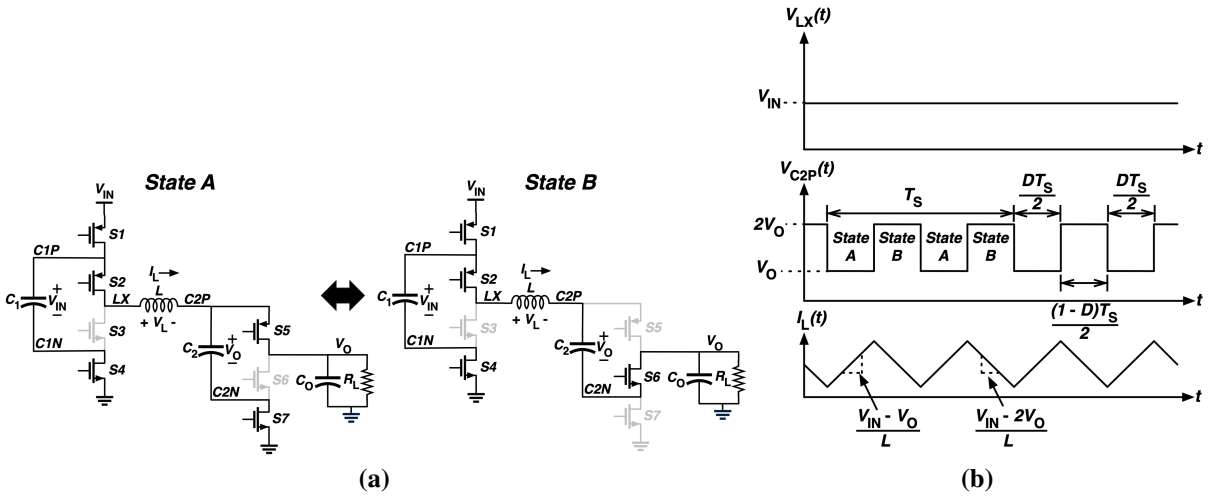
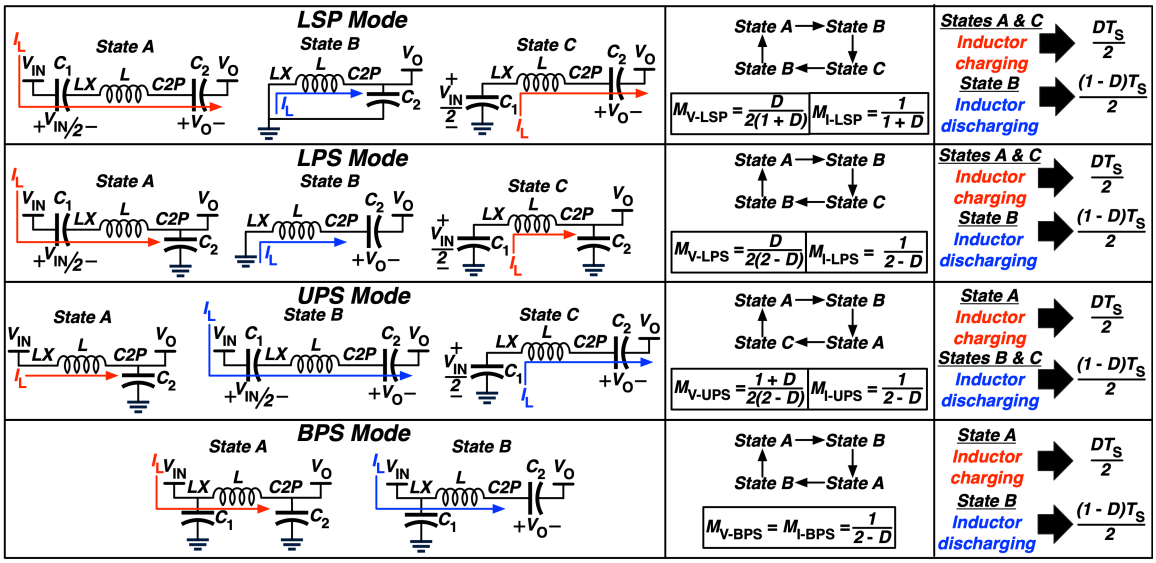



**Figure 4.6.** BPS mode (a) operating states and (b) switching node and inductor current waveforms.

the various modes are theoretically capable of realizing VCRs from 0–1. However, up to this point it is still unclear which mode should be utilized in the cases where multiple modes are theoretically capable of providing the same VCR. This will be addressed with the loss analysis across modes in Section 4.4 which will also provide some criteria for determining the optimal mode based on operating range requirements. It should also be noted that in the cases where there is an intersection between the VCRs, as is the case for the LSP and LPS modes at the D = 0.5 point, provides and opportunity to extend the VCR range when traversing different D values. For example, if the converter is initially operating in LSP mode at D $<$ 0.5 and the D value continues to increase, the converter could switch to the LPS mode near the D = 0.5 point to extend the maximum achievable VCR beyond the maximum possible VCR for LSP mode (i.e. max. VCR would be extended from 0.25 to 0.5). This will be covered more in Sections 4.4 and 4.6.

**Table 4.1.** Summary of operating mode switching states and conversion ratios.



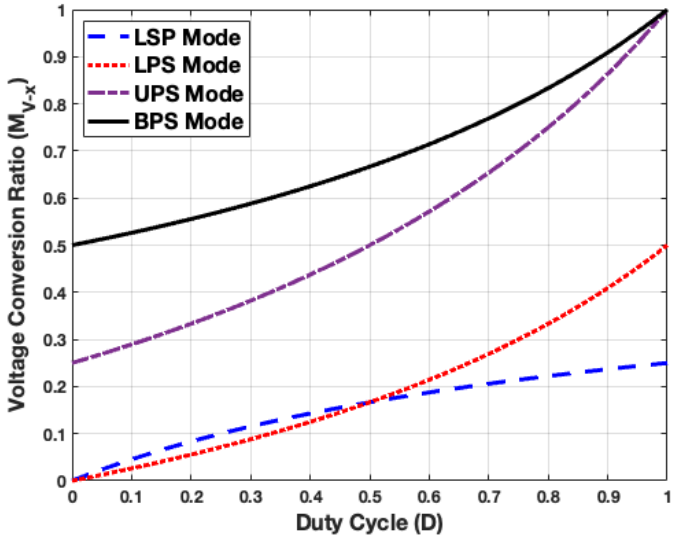




**Figure 4.7.** Ideal VCR vs. duty cycle vs. main operating modes.

### 4.3.6 Inductor Current Comparison to 2-level and 3-level Buck Converters

As can be seen from the $I_L/I_O$ equations (4.2), (4.5), (4.8), and (4.11) for each mode, the DC inductor current is equal to the output current scaled down by the VCR of the second SC stage. This results in a reduction in the inductor conduction losses by the second stage VCR squared. This could translate into significant loss reductions for high DCR inductors and help ease saturation current requirements when compared to conventional 2-level and 3-level buck converters where the inductors must conduct the full output current.

To illustrate these potential benefits, example plots of the peak-to-peak inductor currents ($\Delta i_L$) and the maximum inductor current values for the SIMS converter, 2-level buck, and 3-level buck are shown in Fig. 4.8 for the same output current, inductor value, and switching frequency. The maximum inductor currents are defined as the DC current plus half of the peak-to-peak ripple value. The portions of the curves that correspond to the VCRs needed for charging a 1-cell battery (i.e. $V_O$ = 2.8V–4.2V) are highlighted in solid blue. In all of the example scenarios, both the inductor current ripple and maximum inductor current are significantly less than the 2-level buck converter over the required VCR ranges. When compared to the 3-level buck, this is only true for some of the ripple current scenarios. However, it should be noted that the maximum inductor current is consistently less in all cases by virtue of the DC output current being scaled down by the SIMS second stage VCR when referred back to the DC inductor current level.

## 4.4 Conduction Loss Analysis and Characteristics Across Modes

The conduction loss analysis utilizes the same charge flow techniques and DC transformer model $R_O$ presented in Section 3.3. Therefore, a detailed step-by-step analysis for the SIMS converter modes will not be covered and this section will focus on the results and the resulting $R_O$ behavior across modes and VCRs.

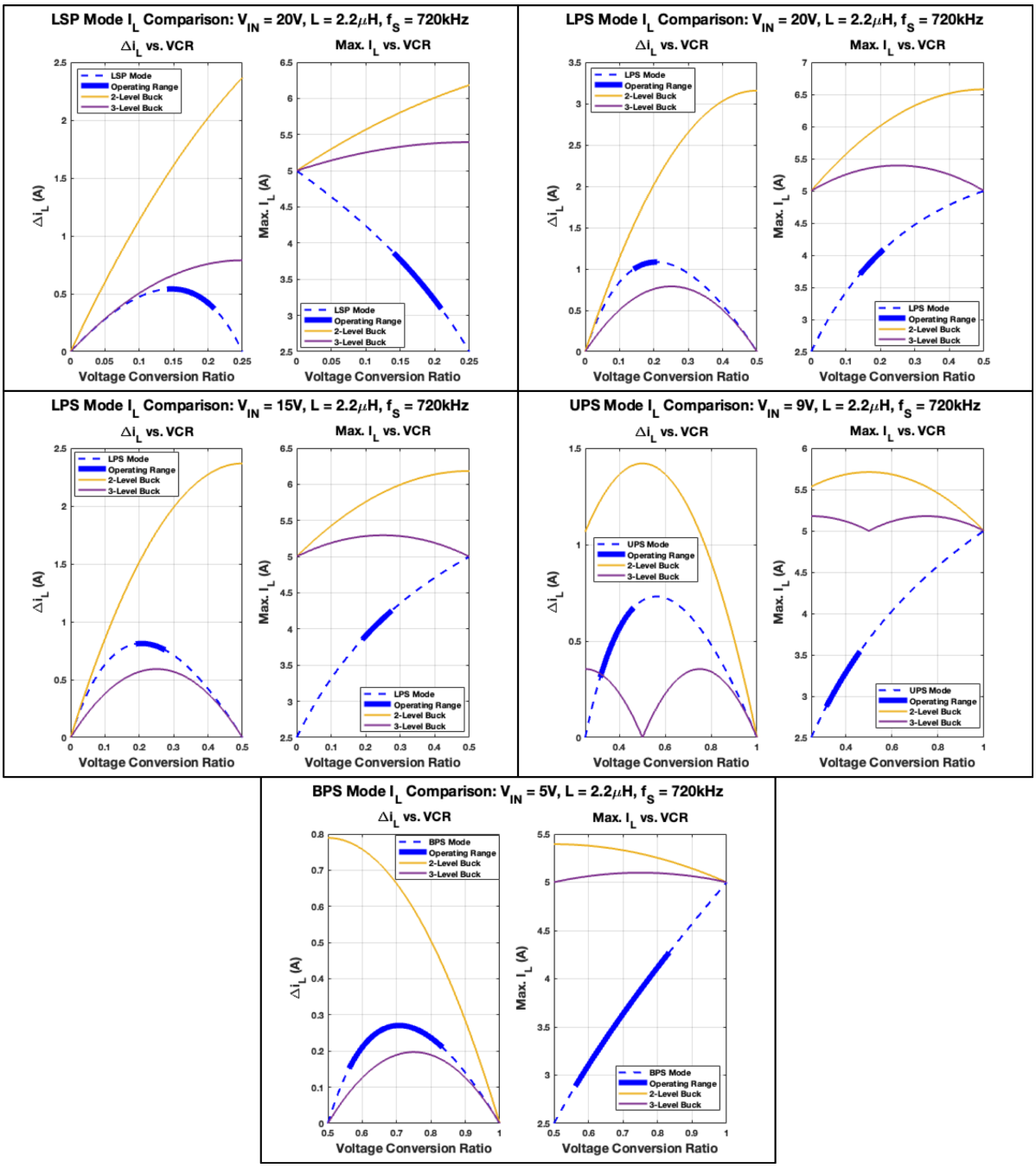



**Figure 4.8.** Comparison of SIMS, 2-level buck, and 3-level buck peak-to-peak inductor current ripple and maximum inductor current value vs. VCR with $I_O$ = 5A.

Since $C_2$ is only partially soft charged in two of the switching states, its hard discharge losses are be accounted for in the resulting SSL losses. The equivalent SSL output resistance for each mode are

$$R_{SSL-LSP} = \frac{(M_{I-LSP})^2 D^2}{4C_2 f_S} \tag{4.13}$$

$$R_{SSL-LPS} = \frac{(M_{I-LPS})^2 (1-D)^2}{4C_2 f_S} \tag{4.14}$$

$$R_{SSL-UPS} = \frac{(M_{I-UPS})^2 (1-D)^2}{4C_2 f_S} \tag{4.15}$$

$$R_{SSL-BPS} = \frac{(M_{I-BPS})^2 (1-D)^2}{4C_2 f_S}. \tag{4.16}$$

For the FSL related conduction losses, the general expression for the equivalent FSL output resistance across all modes is

$$R_{FSL-x} = \sum_{i=1}^{7} a_{S_i} R_{ON_i} + \sum_{k=1}^{2} a_{esr_k} ESR_k + a_{dcr} L_{DCR} \tag{4.17}$$

where $a_{S_i}$, $a_{esr_k}$, and $a_{dcr}$ are the duty cycle dependent scale factors for each output-referred resistive loss element, $R_{ON_i}$ is the on-resistance for power switch $S_i$, $ESR_k$ is the equivalent series resistance for flying capacitor $C_k$, and $L_{DCR}$ is the DC resistance of the inductor. Since $C_1$ is fully soft charged/discharged, only the conduction losses associated with its ESR are included in the $R_{FSL}$ for the modes where it is actively switching. Note that since $C_1$ is not active during BPS mode, its ESR related losses along with switch S4's losses are ignored in this mode. Additionally, since switch S3 is off in BPS mode its losses are also ignored.

The resulting equivalent output resistance can then be estimated as

$$R_O \approx \sqrt{(R_{SSL-x})^2 + (R_{FSL-x})^2} \tag{4.18}$$

where $R_{SSL-x}$ and $R_{FSL-x}$ are the effective SSL and FSL output resistances for each mode, respectively.

### 4.4.1 Mode Selection Determination for Optimal Performance

Equations (4.14) – (4.18) and the FSL scale factors provided in Fig. 4.9 can now be utilized to gain some more insight on optimal mode selection for a given set of operating range requirements. Fig. 4.10(a) shows the ideal VCRs vs. duty cycle while Fig. 4.10(b) shows the normalized $R_O$ vs. VCR relationship for an example converter across different modes. Fig. 4.10(b) shows there is an asymmetry to $R_O$ for each of the main modes of operation where $R_O$ increases dramatically and approaches a vertical asymptote as the hard charge loss of the second stage begins to dominate. By selecting a mode that meets VCR requirements with smaller $R_O$, these regions can be avoided. Ideally, in the case of a closed loop regulator, a mode would be selected such that the regulation loop would move the duty cycle in trajectory away from the regions of high $R_O$ as the loop increases the duty cycle with increasing output current levels.

Additionally, modes with intersecting VCRs provide an opportunity to extend the VCR range while also minimizing conduction losses. More specifically, when operating in the LSP and LPS modes this can be achieved by automatically detecting when D = 0.5 and simply inverting the second stage operating phases. This automatic mode (Auto mode) is a fifth mode in addition to the other four primary modes that can be leveraged for simultaneous VCR extension and minimization of conduction losses as highlighted in the overlayed Auto Mode curve in Fig. 4.10. As shown in Fig. 4.10(a), by transitioning from LSP mode to LPS mode at D = 0.5 the maximum theoretically achievable VCR can be increased from 0.25 to 0.5. While Fig. 4.10(b) shows that when transitioning from LSP mode to LPS mode at D = 0.5 the vertical asymptote in $R_O$ can be avoided. The same is also true for when transitioning from LPS to LSP mode with decreasing VCR.

However, care must be taken during this transition to minimize the possibility of significant $V_O$ perturbations since at D = 0.5 the inductor ripple current of LPS mode is twice that of

| **Mode** | $a_{s_1}$ | $a_{s_2}$ | $a_{s_3}$ | $a_{s_4}$ |
|---|---|---|---|---|
| LSP | $(M_{I-LSP})^2\left(\frac{D}{2}\right)$ | $(M_{I-LSP})^2\left(\frac{D}{2}\right)$ | $(M_{I-LSP})^2\left(\frac{2-D}{2}\right)$ | $(M_{I-LSP})^2\left(\frac{2-D}{2}\right)$ |
| LPS | $(M_{I-LPS})^2\left(\frac{D}{2}\right)$ | $(M_{I-LPS})^2\left(\frac{D}{2}\right)$ | $(M_{I-LPS})^2\left(\frac{2-D}{2}\right)$ | $(M_{I-LPS})^2\left(\frac{2-D}{2}\right)$ |
| UPS | $(M_{I-UPS})^2\left(\frac{1+D}{2}\right)$ | $(M_{I-UPS})^2\left(\frac{1+D}{2}\right)$ | $(M_{I-UPS})^2\left(\frac{1-D}{2}\right)$ | $(M_{I-UPS})^2\left(\frac{1-D}{2}\right)$ |
| BPS | $(M_{I-BPS})^2$ | $(M_{I-BPS})^2$ | 0 | 0 |

**(a)**

| **Mode** | $a_{s_5}$ | $a_{s_6}$ | $a_{s_7}$ |
|---|---|---|---|
| LSP | $(M_{I-LSP})^2\left(\frac{1}{1-D}\right)$ | $(M_{I-LSP})^2 D$ | $(M_{I-LSP})^2\left(\frac{D^2}{1-D}\right)$ |
| LPS | $(M_{I-LPS})^2\left(\frac{1}{D}\right)$ | $(M_{I-LPS})^2(1-D)$ | $(M_{I-LPS})^2\frac{(1-D)^2}{D}$ |
| UPS | $(M_{I-UPS})^2\left(\frac{1}{D}\right)$ | $(M_{I-UPS})^2(1-D)$ | $(M_{I-UPS})^2\frac{(1-D)^2}{D}$ |
| BPS | $(M_{I-BPS})^2\frac{1}{D}$ | $(M_{I-BPS})^2(1-D)$ | $(M_{I-BPS})^2\frac{(1-D)^2}{D}$ |

**(b)**

| **Mode** | $a_{esr_1}$ | $a_{esr_2}$ | $a_{dcr}$ |
|---|---|---|---|
| LSP | $(M_{I-LSP})^2 D$ | $(M_{I-LSP})^2\left(\frac{D}{1-D}\right)$ | $(M_{I-LSP})^2$ |
| LPS | $(M_{I-LPS})^2 D$ | $(M_{I-LPS})^2\left(\frac{1-D}{D}\right)$ | $(M_{I-LPS})^2$ |
| UPS | $(M_{I-UPS})^2(1-D)$ | $(M_{I-UPS})^2\left(\frac{1-D}{D}\right)$ | $(M_{I-UPS})^2$ |
| BPS | 0 | $(M_{I-BPS})^2\frac{1-D}{D}$ | $(M_{I-BPS})^2$ |

**(c)**

**Figure 4.9.** (a) FSL scale factors for switches S1–S4 (b) FSL scale factors for switches S5–S7 (c) FSL scale factors for flying capacitor ESRs and inductor DCR.

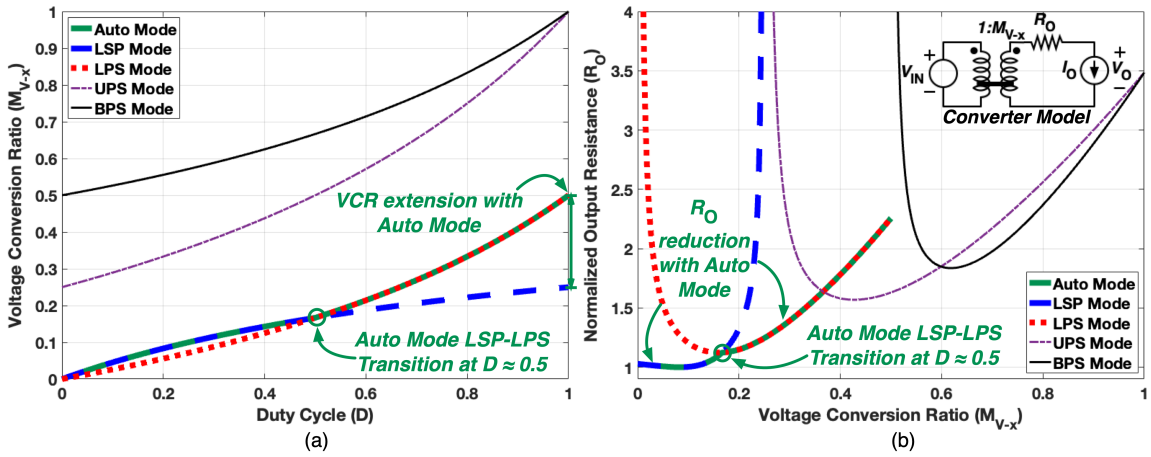



**Figure 4.10.** (a) Ideal VCRs vs. D and (b) normalized $R_O$ vs. VCR for an example SIMS converter.

LSP mode as can be shown by evaluating equations (4.3) and (4.6) when D = 0.5. The methods to address this will be covered in Subsection 4.6.8.

## 4.5 Power Switch Optimization

By utilizing equation (4.17) and the FSL scale factors provided in Fig. 4.9, the same Lagrange multiplier based optimization from Subsection 3.4.2 and [46] can be used to derive an expression for the optimal power switch sizing for a given switch area constraint. The switch area constraint is defined as

$$A_{s,tot} = \sum_{i=1}^{7} \frac{G_{s_i}}{G_{den,s_i}} \tag{4.19}$$

where $G_{s_i}$ and $G_{den,s_i}$ are the on-state conductance and conductance density of switch $S_i$, respectively, and equation (4.17) is the function to be minimized. Inserting (4.17) and (4.19) into the Lagrange optimization expression yields

$$\mathscr{L} = \sum_{i=1}^{7} \frac{a_{s_i}}{G_{s_i}} + \lambda \left( \sum_{i=1}^{7} \frac{G_{s_i}}{G_{den,s_i}} - A_{s,tot} \right). \tag{4.20}$$

Setting the partial derivatives of (4.20) with respect to $G_{s_i}$ and $\lambda$ to zero and solving the resulting system of equations provides the optimal switch conductances for a given area as

$$G_{s_i,opt} = \frac{A_{s,tot}\sqrt{a_{s_i}G_{den,s_i}}}{\sum_{i=1}^{7}\sqrt{\frac{a_{s_i}}{G_{den,s_i}}}}. \tag{4.21}$$

## 4.6 Implementation Details

The block diagram for the SIMS converter prototype is shown in Fig. 4.11. For this initial prototype, a voltage mode control feedback loop was utilized for output regulation. All circuitry required for $V_O$, $V_{C1}$ balancing, PWM generation, mode/timing control, and power switch driving were included in the test chip. Compensation and $V_O$ feedback components were provided externally to facilitate tuning of the regulation and $V_{C1}$ balancer performance. A programable test register was included to allow mode control and optimization of switching frequency, dead-times, and timing of each power stage during verification testing.

### 4.6.1 Power Switches, Gate Drivers, and Level Shifters

The power stage and gate driving implementation is shown in Fig. 4.12. Switches S1–S4 are implemented with high voltage (HV) 12V devices since they must block $V_{IN}/2$ when off, while S5-S7 are implemented with 5V devices since they only need to block $V_O$ when off (i.e. 2.8V–4.2V). The schematic for the level shifters is also shown in Fig. 4.12 and consists of a current controlled push-pull output stage with the HV devices functioning as HV blocking cascodes. When idling, the state of the level shifter is maintained with a small bias current, $I_{BL}$, to reduce quiescent current. During output or flying domain supply ($V_{DDH}$/$V_{SSH}$) transitions, the HC_PUL signal briefly pulses a high bias current, $I_{BH}$, to increase speed and provide high $dV/dt$ immunity.

The high-side regulator (HS REG) generates a voltage ~5V below $V_{IN}$ to power the

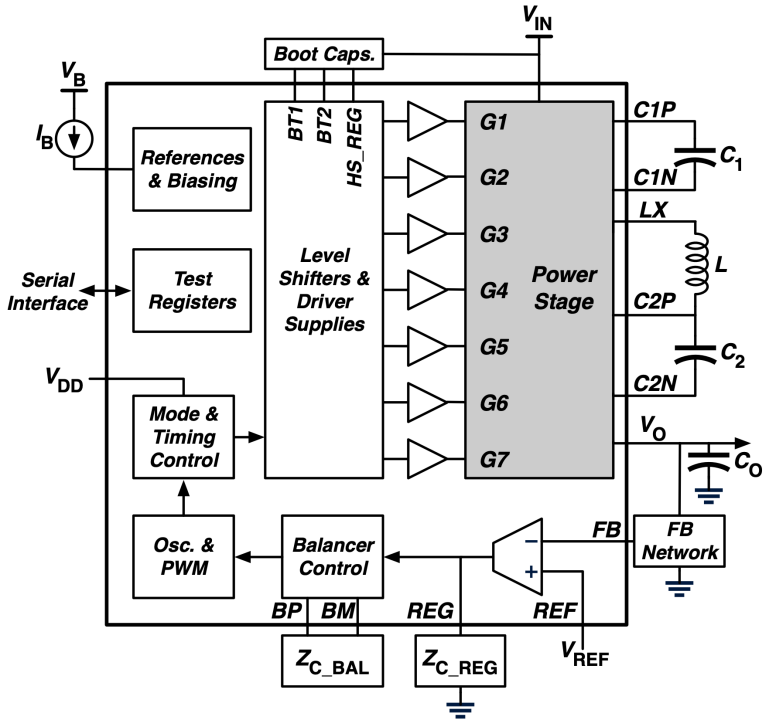



**Figure 4.11.** Block diagram of the SIMS converter prototype.

S1–S2 gate drivers while also limiting the gate drive swing below their maximum source to gate voltage ($V_{SG}$) ratings. It is also used to refresh S2's bootstrap capacitor ($C_{B2}$) through diode D0 when S1 is on. S3's gate driver is powered by $C_{B3}$ and is refreshed by $V_{DD}$ and D1 when S4 is on. Bootstrap diodes, D0–D1, are implemented with integrated Schottky diodes. The gate drivers for S5–S6 are powered from C2 while S7's driver is powered from $V_O$.

The simplified schematic for the HS REG block is shown in Fig. 4.13. It consists of a $V_{IN}$ referenced Zener diode based shunt regulator. A small low-side bias current ($I_{B\_LS}$) keeps the Zener in break over and provides a light load bias for the pass transistor (M0) while the the HV devices (M1–M2) function as HV blocking cascodes for the low voltage (LV) 5V devices used for the $I_{B\_LS}$ current sinks. The Zener and high-side biasing PMOS are implemented with LV devices in a HV N-well biased at $V_{IN}$. An option to connect the drain of M0 to $V_{DD}$ via the HS Charge Recycler block is also included to re-direct the pass device current to the $V_{DD}$ domain sub-blocks and reduce the source to drain ($V_{SD}$) when operating at high $V_{IN}$ voltages.

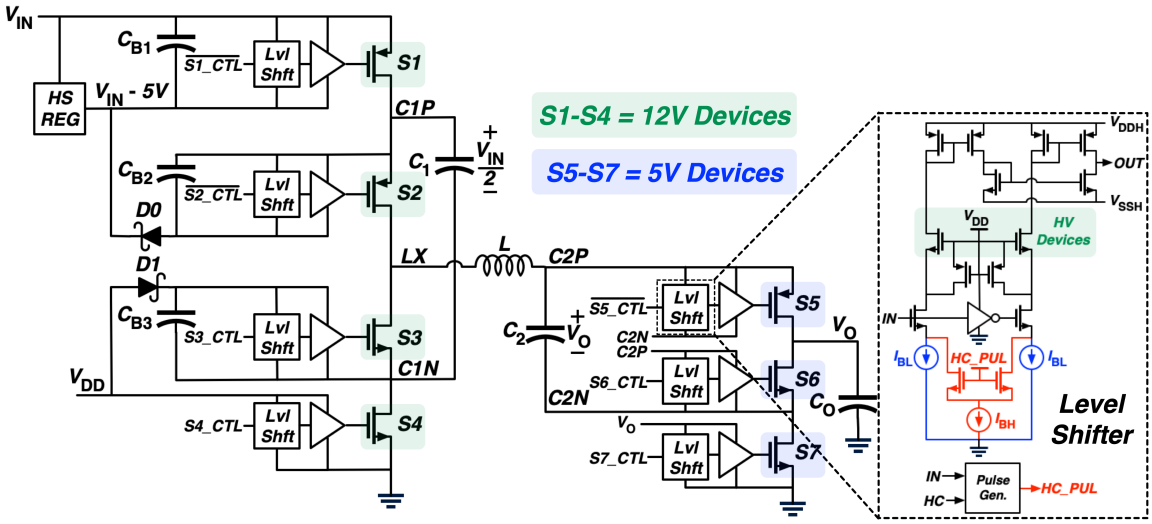



**Figure 4.12.** Power stage, gate driving, level shifter implementations.

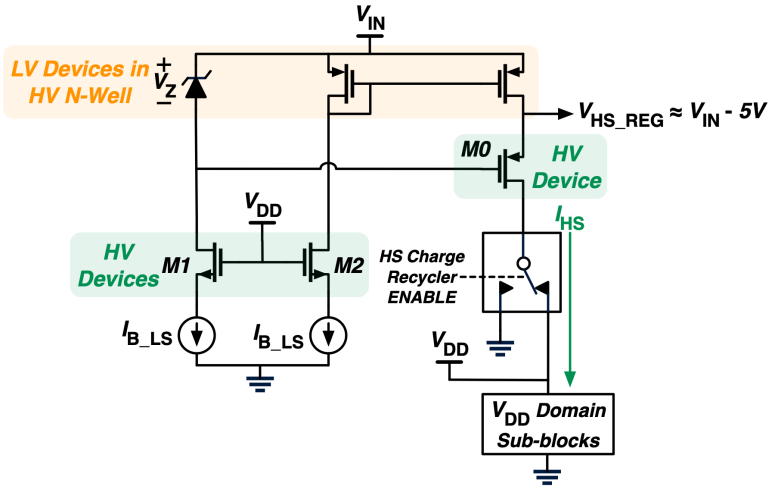



**Figure 4.13.** High side shunt regulator and charge recycler.

### 4.6.2 $V_O$ Regulation and $V_{C1}$ Balancer

While C2 does not require active voltage balancing since it is hard discharged to $V_O$ each cycle, C1 does when the converter is in a mode where it is actively switching since it is fully soft charged/discharged by the inductor current and is susceptible to $V_{C1}$ drift due to power stage timing and impedance mismatches in its charging and discharging paths. The balancer and $V_O$ regulation implementation, shown in Fig. 4.14, utilizes a modified approach from [8] where the $V_O$ loop sets the common mode of the error signals, BP and BM, that are sampled by the pulse width modulator (PWM) which then determines the duty cycles of the PWM1, PWM2, and switch control signals. The balancer sense amplifier continuously measures an attenuated value of the $V_{C1}$ voltage and its output (C1_SNS) is compared to a scaled referenced voltage ($V_{B\_REF\_LS}$) derived from $V_{IN}$. If an imbalance exists, the balancer loop then produces a small differential voltage between BP and BM ($\Delta V_B$) to finely adjust the switch timing to regulate $V_{C1}$ to $V_{IN}/2$ by slightly adjusting the charging and discharging times of $C_1$. This allows the balancer and $V_O$ loops to be independently compensated since the balancer compensation ($Z_{C\_B}$) does not appear in the common mode path of the $V_O$ loop. For this prototype, a simple Type-1 compensation network was utilized for the $V_O$ regulation loop by implementing $Z_C$ with a shunt capacitor to set the bandwidth of the loop [23, 62, 63]. The $V_O$ regulation error amplifier (EA) is implemented with a basic single stage folded cascode topology while the sense amplifier is implemented with a simple two stage op-amp with a source follower for the output stage. Therefore, their implementation details are not covered here. Subsection 4.6.4 provides a detailed analysis of the balancer loop and $Z_{C\_B}$ network turning that is dependent on some of the internal components of the balancer EA sub-block. Therefore, the balancer EA implementation is covered in some detail in subsection 4.6.3.

The other signals shown in Fig. 4.14 associated with the Auto Mode Detect and control signal generation block will be covered in subsections 4.6.6 and 4.6.8, respectively.

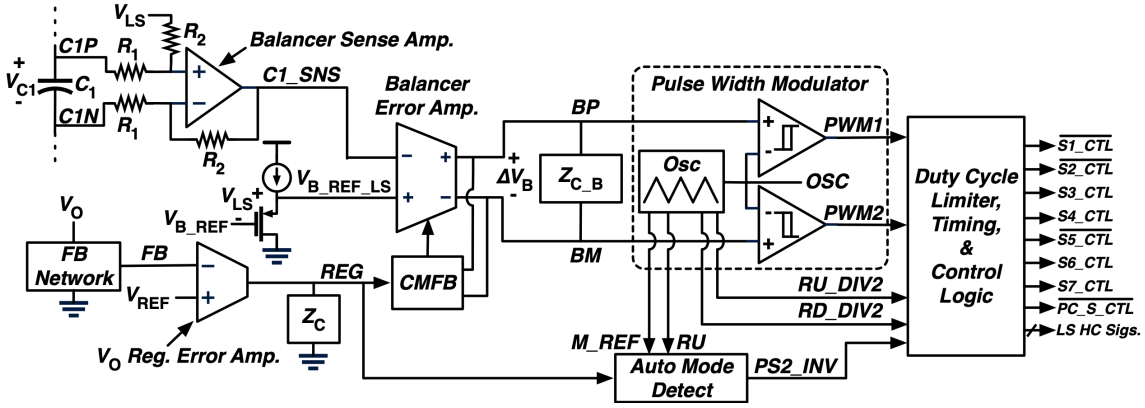



**Figure 4.14.** $V_O$ and $V_{C1}$ balancer control diagram.

### 4.6.3 $V_{C1}$ Balancer Error Amplifier

Fig. 4.15a shows the schematics for the balancer EA and common mode feedback (CMFB) circuit. As described in subsection 4.6.2, the balancer EA's output common mode (CM) is set by the $V_O$ regulation EA output (REG) which drives the CM_REF input of the CMFB sub-block as shown in Fig. 4.15b which also shows the analog switches used for enabling and disabling the balancer loop for testing purposes (drawn in the state where the balancer is enabled). The output CM is sensed by a resistive CM detector formed by $R_{CM}$ and $C_{CM}$. Capacitors $C_C$ are small local compensation capacitors to ensure the balancer EA remains stable when the balancer loop is disabled. To ensure the balancer EA starts up properly even when the balancer is disabled and its outputs are at 0V, a CM output start-up sub-circuit is also included in the EA and CMFB sections which are formed by devices M0–M5. In the situation that both outputs are near 0V and the balancer is disabled, this means the EA's inputs are shorted together by SW2, INM is shorted to OUTP through SW0, and INP is shorted to OUTM through SW1. Therefore, INP and INM are also at 0V and there is no bias current flow in the EA initially. This also causes M1 to be off and the SU_CTL signal is pulled up to $V_{DD}$, resulting in switches M2 and M3 to be turned on and a small about of bias current ($I_{SU}$) is allowed to conduct through M4 and M5. This then pulls down the PG0 and PG1 nodes which causes the OUTP and OUTM nodes to come up and the EA enters normal operation.

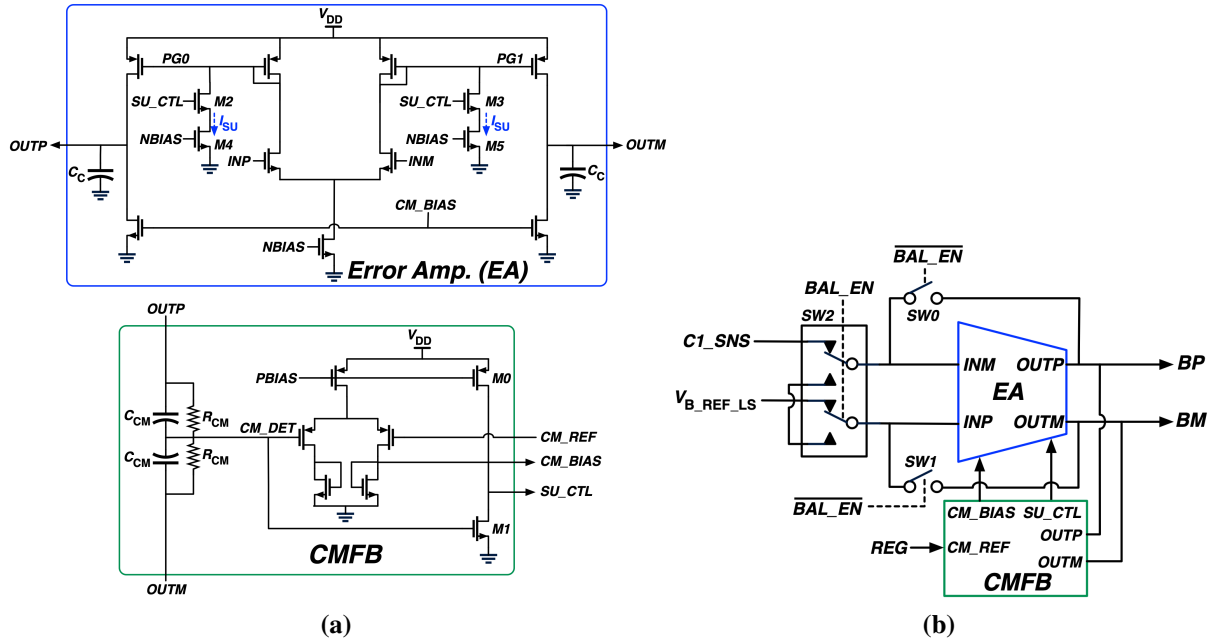



**Figure 4.15.** (a) Balancer error amplifier schematic and (b) enable/disable connections.

### 4.6.4 $V_{C1}$ Balancer Small Signal Analysis and Compensation

As mentioned in subsection 4.6.2, the C1 balancer loop regulates $V_{C1}$ to the correct $V_{IN}/2$ by slightly adjusting the charging and discharging times of $C_1$. In the ideal case where there are no mechanisms that would induce a $V_{C1}$ imbalance, these charging and discharging time durations would be equal to

$$\frac{DT_S}{2}.$$

For example, these would be equal to the time durations of States A and C when operating in LSP mode (Fig. 4.3). However, in a practical implementation where these sources of imbalance are unavoidable, the D values for each of these states would be slightly unequal in order to properly regulate $V_{C1}$ or due to timing mismatches. In this case, we can define the $C_1$ charging state duty cycle as $D_{CHG}$ and the discharging state duty cycle as $D_{DIS}$. Since a drift in the $V_{C1}$ voltage implies that the average current flowing through $C_1$ is not equal to zero, we can start by

first defining the average C1 current as

$$\bar{I}_{C1} = \frac{D_{CHG}(T_S/2)I_L - D_{DIS}(T_s/2)I_L}{T_S} = \frac{I_L}{2}(D_{CHG} - D_{DIS}) = \frac{I_L}{2}\Delta D. \tag{4.22}$$

From state-space averaging and knowing that $I_{C1} = C_1 \frac{dV_{C1}}{dt}$, we can then perturb and linearize [23] the $\Delta D$ and $V_{C1}$ terms and arrive at the small signal control to C1 voltage transfer function as

$$G_{vb}(s) = \frac{\hat{v}_{c1}}{\Delta\hat{d}} = \frac{I_L}{2sC_1} \tag{4.23}$$

where $\Delta\hat{d}$ is the small signal perturbation in the difference of the C1 charging and discharging duty cycles, $\hat{v}_{c1}$ is the resulting small signal perturbation response, and $s = j\omega$. Note that the DC inductor current, $I_L$, can also be related to the DC output current through equations (4.2), (4.5), and (4.8). The resulting unity gain cross-over frequency for (4.23) can also be derived as

$$f_{c\_vb} = \frac{I_L}{4\pi C_1}. \tag{4.24}$$

Note that (4.23) and (4.24) indicate that $G_{vb}(s)$ follows an ideal integrator response whose scales with the DC inductor current (and the output current) which will need to be accounted for in the stability analysis and compensation of the balancer loop.

Fig. 4.16 shows the small signal block diagram of the balancer loop where $H_b(s)$ is the transfer function of the $C_1$ sense amplifier, $G_b(s)$ is the combined transfer function of the balancer EA and $Z_{C\_B}$, and $G_{pwm}$ is the small signal gain of the pulse width modulator which can be shown as

$$G_{pwm} = \frac{1}{V_M} \tag{4.25}$$

where $V_M$ is the peak-to-peak voltage swing of the PWM oscillator signal used to sample the BP

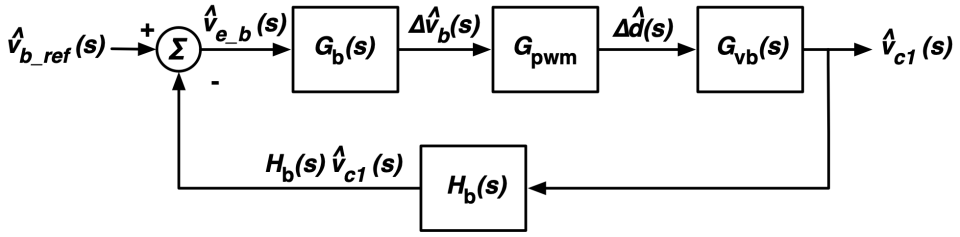



**Figure 4.16.** $V_{C1}$ balancer small signal control loop block diagram.

and BM signals. From Fig. 4.16 , the balancer loop gain can be defined as

$$T_b(s) = H_b(s)G_b(s)G_{pwm}G_{vb}(s) = H_b(s)G_b(s)\left(\frac{1}{V_M}\right)\left(\frac{I_L}{2C_1}\right)\left(\frac{1}{s}\right). \tag{4.26}$$

The $C_1$ flying capacitor will have voltage ripple across it with a frequency equal to $f_s$. Since the BP and BM signals will be sampled by the pulse width modulator, we must ensure the switching is adequately attenuated before being sampled by the modulator. This can be easily achieved by placing a differential filtering capacitor, $C_b$ between the BP and BM nodes. However, this will also introduce another pole, $f_p$, in the loop response in addition to the pole already preset at DC from (4.23) resulting in the possibility of instability. Additionally, the resulting loop gain cross-over frequency, $f_c$ will be influenced by the values of $I_L$ and $C_1$. Specifically, for a given $C_1$ value, $f_c$ will increase with increasing output current, $I_O$, since $I_L$ is dependent on $I_O$ so $f_p$ must be placed at a sufficiently high enough frequency to ensure adequate phase margin but low enough to provide adequate attenuation of the $V_{C1}$ voltage ripple.

In order to meet these requirements, the $f_c$ can also be tuned by controlling the effective gain of the balancing EA by placing an additional differential gain setting resistor, $R_B$ between the BP and BM nodes. Fig. 4.17 shows the resulting differential mode compensation network that can be used for the balancer loop. To derive the resulting balancer EA and compensation, the equivalent differential mode (DM) half circuit is drawn in Fig. 4.18 where $g_m$ and $r_o$ is the equivalent DM half circuit transconductance and output resistance of the balancer EA,

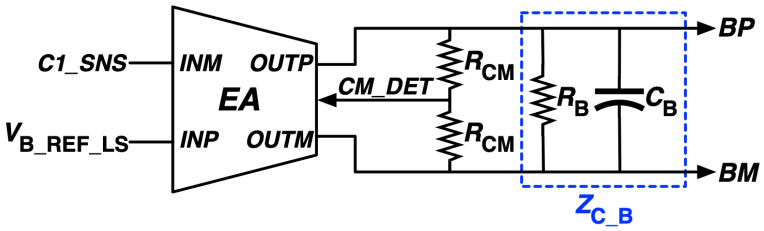



**Figure 4.17.** $V_{C1}$ balancer error amplifier and compensation components.

respectively. The resulting transfer function for for the balancer EA with the $Z_{C\_B}$ network is

$$G_b(s) = \frac{\Delta\hat{v}_b(s)}{\hat{v}_{e\_b}(s)} = -g_m r_t \left(\frac{1}{2r_t C_B s + 1}\right) = -G_{bo}\left(\frac{1}{\frac{s}{\omega_p} + 1}\right) \tag{4.27}$$

where

$$r_t = r_o || R_{CM} || \frac{R_B}{2} = \frac{1}{\frac{1}{r_o} + \frac{1}{R_{CM}} + \frac{2}{R_B}} \tag{4.28}$$

$$G_{bo} = g_m r_t \tag{4.29}$$

$$\omega_p = \frac{1}{2r_t C_B} \tag{4.30}$$

$$f_p = \frac{1}{4\pi r_t C_B}. \tag{4.31}$$

$G_{bo}$ is the DC gain of the balancer EA while $\omega_p$ and $f_p$ are the values of the second pole in the $G_b(s)$ response that is needed to attenuate the $V_{C1}$ switching ripple in radians per second and Hertz, respectively. As discussed in [23, 62, 63], setting $f_p$ to approximately $\frac{f_s}{10}$ is typically adequate to provide enough switching noise attenuation. Note that the $C_C$ capacitor in Fig. 4.15a has been neglected here since its value is assumed to be much smaller than $C_B$. However, it could be accounted for by adding it in parallel with the $\frac{1}{2C_B s}$ component in Fig. 4.18 if needed.

Assuming the $C_1$ sense amplifier bandwidth is large, $H_b(s)$ can be approximated as a

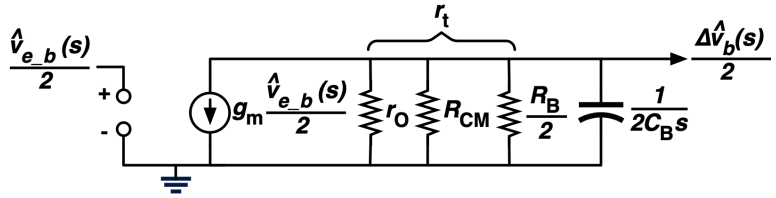



**Figure 4.18.** Equivalent $V_{C1}$ balancer error amplifier differential mode half circuit with compensation network.

fixed gain equal to $H_b$. Equation (4.26) can now be re-written as

$$T_b(s) = H_b G_{bo} \left(\frac{1}{V_M}\right) \left(\frac{I_L}{2C_1}\right) \left(\frac{1}{s}\right) \left(\frac{1}{\frac{s}{\omega_p}+1}\right) = T_{bo} \left(\frac{1}{s}\right) \left(\frac{1}{\frac{s}{\omega_p}+1}\right) \tag{4.32}$$

where

$$T_{bo} = H_b G_{bo} \left(\frac{1}{V_M}\right) \left(\frac{I_L}{2C_1}\right) \tag{4.33}$$

is the DC loop gain. The magnitude of (4.32) can be found as

$$|T_b(j\omega)| = T_{bo} \left(\frac{1}{\omega}\right) \left(\frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_p}\right)^2}}\right). \tag{4.34}$$

If the desired values for $f_p$ and loop phase margin ($PM$) are known, then the require $f_c$ can be found from

$$PM = 180^\circ - 90^\circ - tan^{-1}\left(\frac{f_c}{f_p}\right) \tag{4.35}$$

and solving for $f_c$

$$f_c = (f_p) tan(90^\circ - PM). \tag{4.36}$$

The value for $G_{bo}$ can then be found by setting (4.34) equal to 1 and substituting in the value of $\omega_c$ for $\omega$ where $\omega_c$ is the cross-over frequency in radians per second, resulting in

$$G_{bo} = \left(\frac{1}{H_b}\right) V_M \left(\frac{I_L}{2C_1}\right) \omega_c \sqrt{1+\left(\frac{\omega_c}{\omega_p}\right)^2}. \tag{4.37}$$

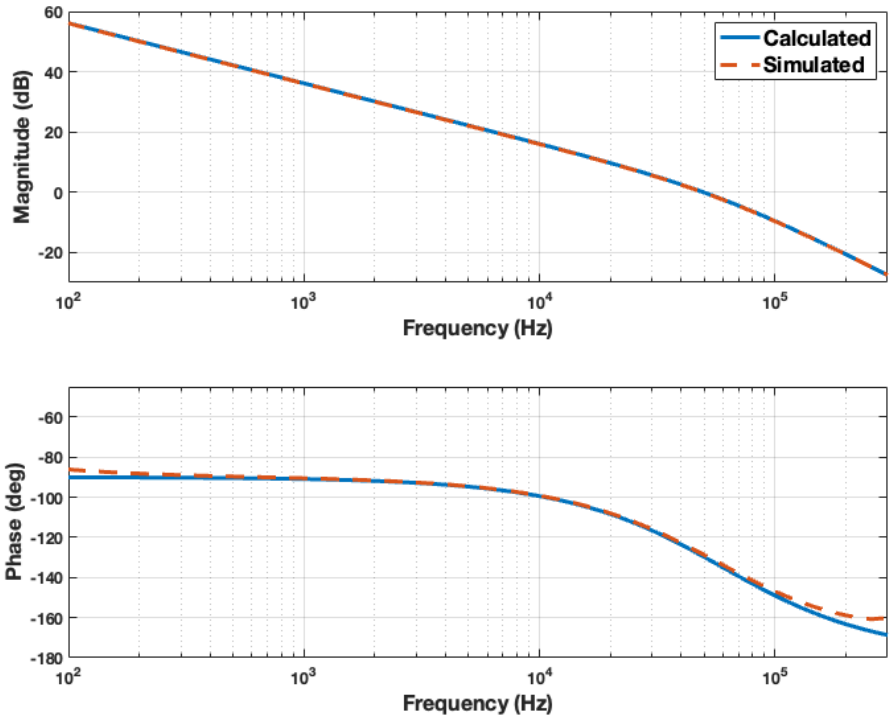



**Figure 4.19.** Calculated and simulated $V_{C1}$ balancer loop gain vs. frequency example.

The value for $r_t$ can then be found from (4.29) which can then be used to find the value of $R_B$ from (4.28) and the value for $C_B$ can be found from (4.31). Fig. 4.19 shows the calculated and simulated frequency responses for an example compensation tuning with $R_B = 37.8k\Omega$ and $C_B = 80$pF resulting in $f_c = 49.4$kHz with $PM = 50.5°$. The parameters and design target values used for this example are summarized in Table 4.2.

### 4.6.5 Pulse Width Modulator Oscillator and Reference Signal Generation

Fig. 4.20 shows the schematic for the oscillator sub-block used for PWM generation. It utilizes a similar to the topology used in [52] to generate a triangle waveform at the OSC_PRE node whose frequency ($f_{OSC}$) is equal to $2f_S$ and is tune-able via $C_{OSC}$ and test register bits. This signal is then level shifted to the output (OSC) by the source follower stage formed by M4. This helps ensure the balancer EA inputs remain within its CM operating range when the

**Table 4.2.** Component and converter parameters used for Fig. 4.19 plot.

| Parameter | Value | Description |
|---|---|---|
| $H_b$ | $\frac{1}{6}\frac{V}{V}$ | $C_1$ sense amplifier gain |
| $V_M$ | $1.3V_{p-p}$ | Peak-to-peak PWM oscillator swing |
| $C_1$ | 7.4µF | First stage flying cap. value |
| $I_L$ | 3.4A | DC inductor current |
| $PM$ | 50° | Target phase margin |
| $f_p$ | 60kHz | Target second pole frequency |
| $f_c$ | 50kHz | Target loop gain cross-over frequency |
| $g_m$ | 815µS | Transconductance of balancer EA |
| $r_o$ | 428kΩ | Small signal output resistance of balancer EA |
| $R_{CM}$ | 200kΩ | Common mode detector resistance of balancer EA |

balancer loop is disabled since the inputs of the balancer EA are shorted to its output when disabled (Fig. 4.15) and the output CM is set by the output of the regulation EA output (REG in Fig. 4.14). The reference voltages for the oscillator that set the voltage swing of the OSC output are derived from the externally supplied reference voltage, $V_{BG}$, and ground which are then level shifted by the source follower stack formed by M0–M2. The voltage divider formed by resistors $R_{BG}$ and $V_{BG}$ is used to derive M_PRE which is then level shifted again by M3 to match the level shift ($V_{LS}$) at OSC produced by M4. This was to help ensure M_REF voltage accurately follows the mid-point of the OSC output swing as it is used to detect when D≈0.5 during Auto mode operation. The RU signal, whose frequency is also equal to $f_{OSC}$, is also utilized in the Auto mode detection implementation which indicates when the triangle oscillator waveform is ramping up from its minimum to maximum value. The usage of these signals is covered in more detail in subsection 4.6.8.

Complimentary to the RU signal, the RD signal indicates when the triangle oscillator waveform is ramping down from its maximum to minimum value. Both the both signals are

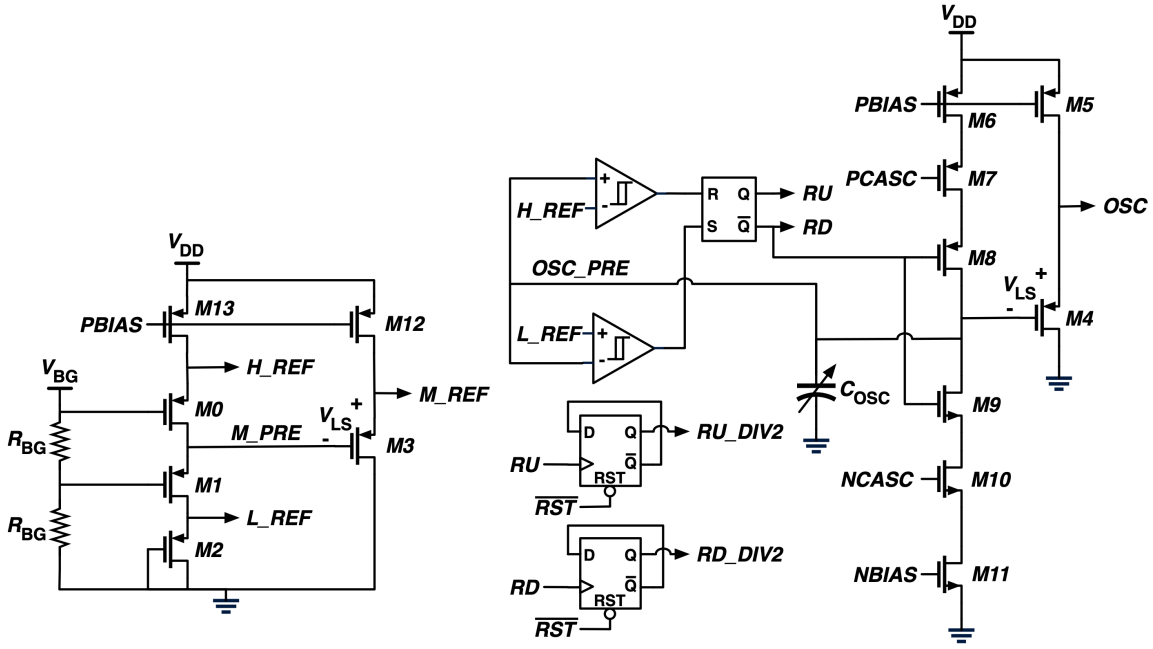



**Figure 4.20.** PWM Oscillator and reference signal generation schematic.

divided down in frequency by 2 to generate the RU_DIV2 and RD_DIV2 clock signals which are then used in the control signal generation for the power switches. This is covered in more detail in subsection 4.6.6.

### 4.6.6 Control Signal Generation

Fig. 4.21 shows the schematic for the PWM signal generator that produces all of the PWM signals that are used to derive the power switch control signals for each of the modes. The pulse width modulator sub-block first produces the master PWM signals, PWM1 and PWM2, as well as their complements, $\overline{\text{PWM1}}$ and $\overline{\text{PWM2}}$ which operate at a frequency of $2f_S$ since the PWM oscillator frequency is $2f_S$. The PWM1 and PWM2 are used to derived the control signals for LSP, LPS, and BPS modes while $\overline{\text{PWM1}}$ and $\overline{\text{PWM2}}$ are used to derive the control signals for UPS mode. PWM1 and PWM2 are time division multiplexed by the PWMA_EN and PWMB_EN frame signals while $\overline{\text{PWM1}}$ and $\overline{\text{PWM2}}$ are time division multiplexed by the PWMC_EN and PWMD_EN frame signals. Both sets of signals are generated by their own non-overlap signal generator blocks. The non-overlapping function ensures the previous frame ends before the next

one begins, avoiding momentary erroneous switch operation. The non-overlap of the frame signals also functions as a minimum off-time generator (i.e. maximum duty cycle limiter) for the LSP, LPS, and BPS modes and minimum on-time generator for the UPS mode (i.e. minimum duty cycle limiter). For the LSP, LPS, and BPS modes, the minimum on-time (i.e. minimum duty cycle limiter) is enforced by the one-shot pulse generator via the L_TON_MIN signal which is logically OR'd with the master PWM1 and PWM2 signals. For the UPS mode, the minimum off-time (i.e. maximum duty cycle limiter) is enforced by the same one-shot pulse generator via the U_TOFF_MIN signal which is logically OR'd with the master $\overline{\text{PWM1}}$ and $\overline{\text{PWM2}}$ signals.

Since the frame signals are derived from the RD_DIV2 and RU_DIV2 which operate at half the frequency of $f_{OSC}$, this means the frame signals operate at $f_S$. Hence, the PWM1, PWM2, $\overline{\text{PWM1}}$, $\overline{\text{PWM2}}$, and their respective frame signals are used to derive the first stage switch control signals. Specifically, PWM1, PWM2, PWMA_EN, and PWMB_EN are used to generate the PWMA and PWMB signals which are eventually used to derive the switch S1 and S2 control signals when in LSP, LPS, or BPS modes. In a similar manner, $\overline{\text{PWM1}}$, $\overline{\text{PWM2}}$, PWMC_EN, and PWMD_EN are used to generate the PWMC and PWMD signals which are eventually used to derive the S1 and S2 control signals when in UPS mode. The PWM signals used for the second stage switches are generated by logically OR'ing or NOR'ing the PWMA and PWMB or PWMC and PWMD pairs. The PWMAB_PS2 signal is used for the second stage switches when in LSP mode while the $\overline{\text{PWMAB\_PS2}}$ signal is used for the second stage when operating in LPS or BPS modes. PWMCD_PS2 is used for the second stage switches when operating in UPS mode.

The output AND gates are used to mute the PWM signals when PWM is disabled (e.g. during pre-charging of $C_1$). The OR and NOR gates that have a single input grounded are included to help match timing skew between the PWM signals.

The PWM operating waveforms for LSP, LPS, and UPS modes are illustrated in Fig. 4.22. For BPS mode, the signals are identical except the PWMA and PWMB signals are not utilized

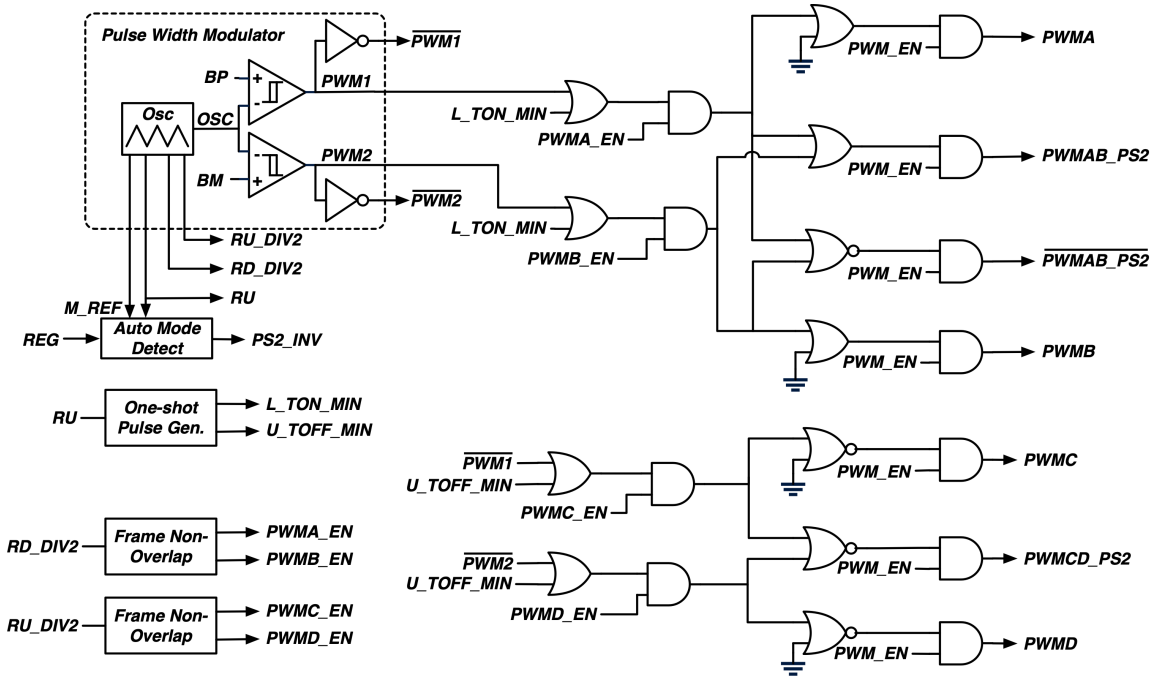



**Figure 4.21.** PWM control signal generator schematic.

since S1, S2, and S4 are forced to an on state while S3 is forced to an off state by the controller. Note that when the first stage is active, the control signals for S1 and S4 are complementary while the control signals for S2 and S3 are also complementary. In the second stage, the control signals for S5 and S7 are the same while S6 is complementary to S5 and S7.

Once all of the necessary PWM signals are generated, they are sent to the power switch control signal generator and selector shown in Fig. 4.23. This section of the controller includes multiple banks of signal multiplexers to properly route the PWM signals to the power switch level shifters. The mode decoder logic block controls the multiplexer banks as does the PC control and Auto mode detect blocks. The programmable non-overlap generation of the switch control signals is also handled here. Specifically, S1 is non-overlapped with S4, S2 is non-overlapped with S3, and S5/S7 is non-overlapped with S6. A set of programmable delay blocks for the first and second stage PWM signals are also included to allow de-skewing of the control signals if needed.

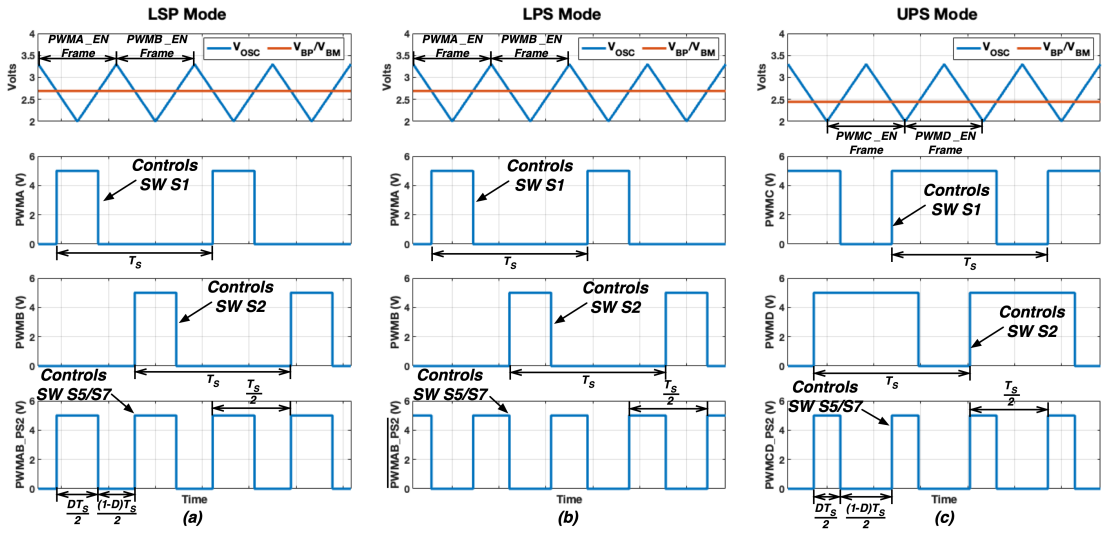



**Figure 4.22.** PWM control signals for (a) LSP, (b) LPS, and (c) UPS modes.

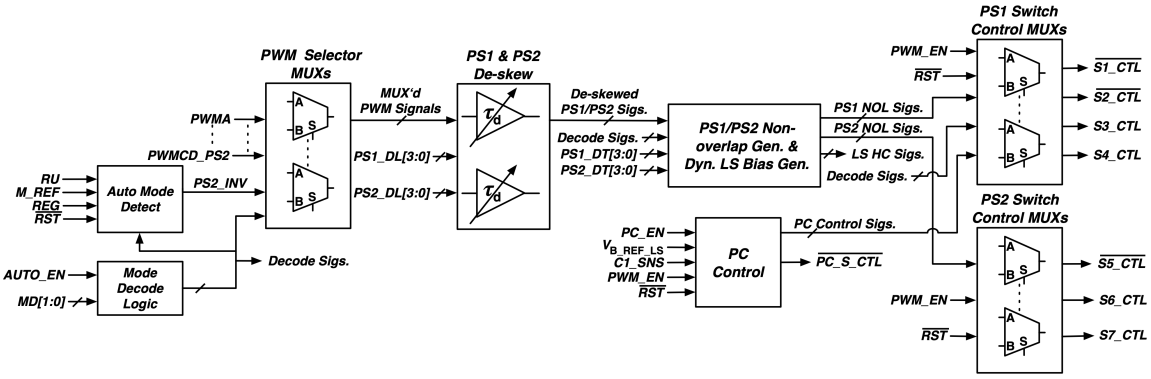



**Figure 4.23.** Power switch control signal generator/selector schematic.

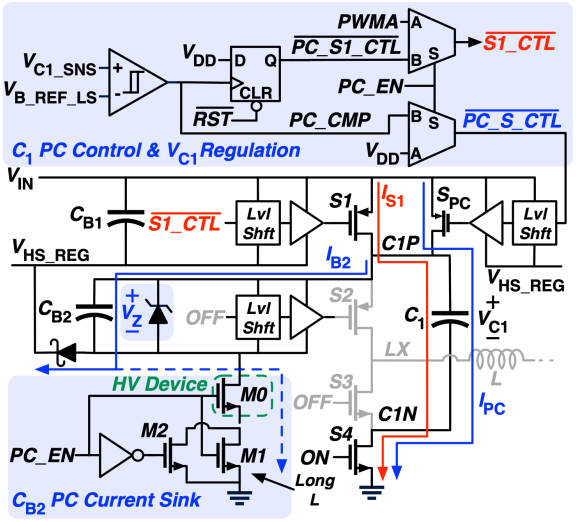



**Figure 4.24.** $C_1$ pre-charge control diagram.

### 4.6.7 $C_1$ Pre-charge Control

For modes that utilize the first stage (i.e. LSP, LPS, and UPS modes), pre-charging (PC) is necessary during start up to ensure no switches are stressed as $V_{IN}$ turns on and $V_{C1}$ is near $V_{IN}/2$ before PWM begins. The implementation of the first stage PC circuit is shown in Fig. 4.24. When PC is enabled (PC_EN = 1), switches S1, S4, and $S_{PC}$ are on where $S_{PC}$ is a small switch that is only active during PC operation. This ensures $V_{C1}$ tracks $V_{IN}$ until it reaches $V_{IN}/2$. S1 is then turned off and $V_{C1}$ is regulated to $V_{IN}/2$ by the comparator loop and the small switch $S_{PC}$. $C_{B2}$ is also pre-charged to ensure that S2 remains off during start-up and its gate driver is properly powered before PWM begins. While S1 or $S_{PC}$ can refresh $C_{B2}$ when on, a current sink also produces a small bias current to ensure it remains charged regardless of the states of S1 and $S_{PC}$ by drawing charge from C1. The Zener diode ensures the voltage of $C_{B2}$ remains near 5V.

### 4.6.8 Automatic Mode and Active Current Shaping

As previously noted in subsection 4.4.1, to extend the VCR range while minimizing $R_O$, Auto mode can be utilized to switch between LSP and LPS modes by detecting when D $\approx$ 0.5 and inverting the second stage operation from the previous mode. However, care must

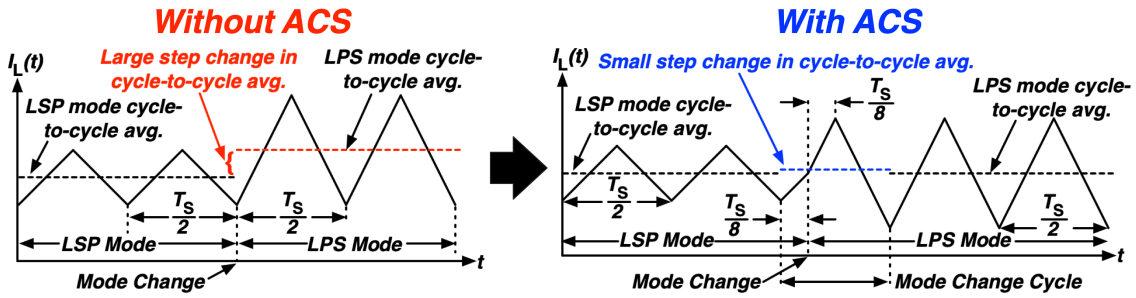



**Figure 4.25.** Auto mode transition examples without and with ACS.

be taken during this transition since at D = 0.5 the $I_L$ ripple of LPS mode is twice that of LSP mode. An example LSP-to-LPS transition is shown in Fig. 4.25 where a mode transition occurs synchronously but results in a large step change in the cycle-to-cycle average value of $I_L$ which could result in significant $V_O$ perturbations. To minimize the magnitude of this step change, an active current shaping (ACS) technique shown in Fig. 4.25 is employed where $I_L$ is gradually transitioned to the nominal peak value for the subsequent mode. The ACS implementation and relevant waveforms are shown in Fig. 4.26. A hysteretic comparator is used to detect when the $V_O$ regulation error amplifier output, $V_{REG}$, is above or below $V_{M\_REF}$ which is equal to the average of the PWM oscillator waveform, $V_{OSC}$ (i.e. the point of D = 0.5). The comparator output is gated by the RU signal from the oscillator which forces the converter to remain in the previous mode for $T_S/8$ before transitioning to the next mode by asserting the PS2_INV signal, resulting in the inversion of the operation of the second stage for the next mode.

## 4.7 Experimental Verification

The annotated die micrograph of the prototype SIMS converter is shown in Fig. 4.27. It was fabricated in a 180nm HV BCD process with 9.4mm$^2$ of die area. 220µm pitch flip chip bumping was used to minimize package and PCB parasitics related losses at high output currents.

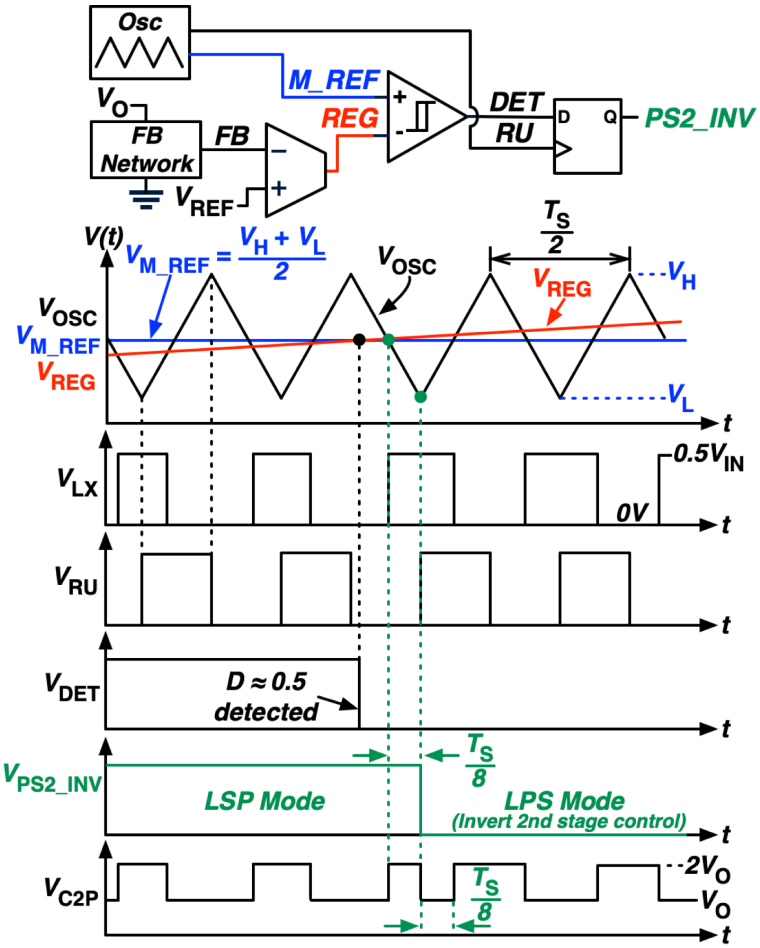



**Figure 4.26.** Auto mode duty cycle detection and ACS circuit and control waveforms.

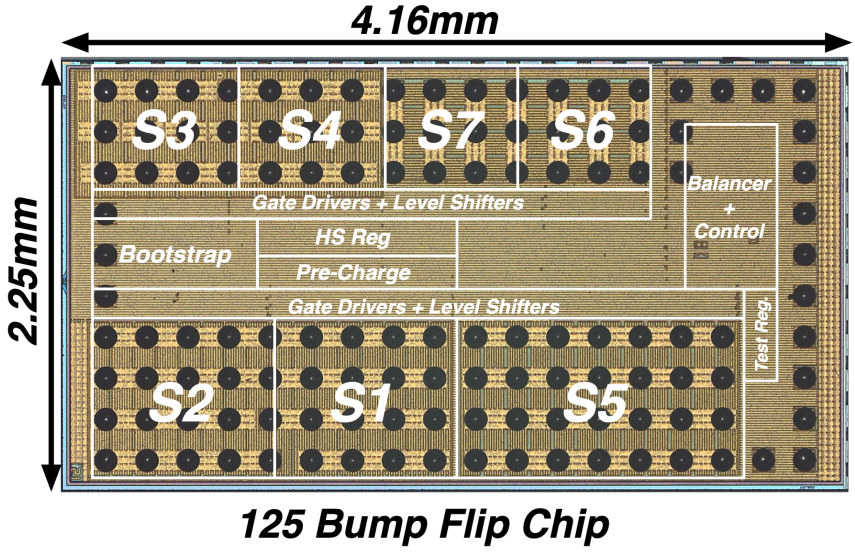



**Figure 4.27.** Annotated die micrograph for SIMS converter test chip.

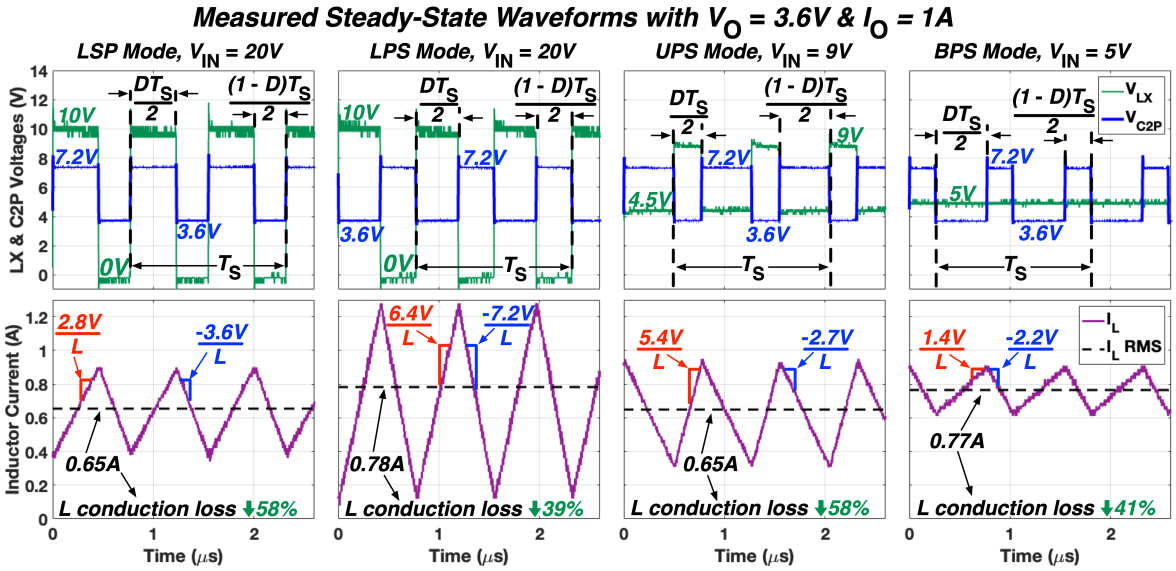



**Figure 4.28.** Measured steady-state operating waveforms and RMS inductor current for each mode.

### 4.7.1 Steady-State Operation Measurements

The measured steady-state waveforms for each mode with $V_O$ = 3.6V at 1A output current are shown in Fig. 4.28 confirming the proper operating voltage levels at the LX/C2P switching nodes and inductor current slopes/levels. The RMS values of the inductor currents for each mode are also annotated along with the estimated inductor conduction loss reduction values when compared to a topology using the same inductor at the output with comparable ripple. The estimates indicate a potentially significant loss reduction even at moderate output current levels. These savings would continue to quadratically increase at higher loads.

### 4.7.2 $V_{C1}$ Balancer Performance

Fig. 4.29 shows the measured performance of the $C_1$ active voltage balancer with $V_{IN}$ = 20V, $V_O$ = 3.6V at 0.7A of output current while operating in LPS mode. As can be see in the top of Fig. 4.29, when the balancer is disabled the $V_{C1}$ is not properly maintained at $V_{IN}/2$ which results in an imbalance in the observed LX node voltage ($V_{LX}$) and increased inductor current ($I_L$) peak-to-peak ripple. When the balancer is enabled, as shown in the bottom of the figure,

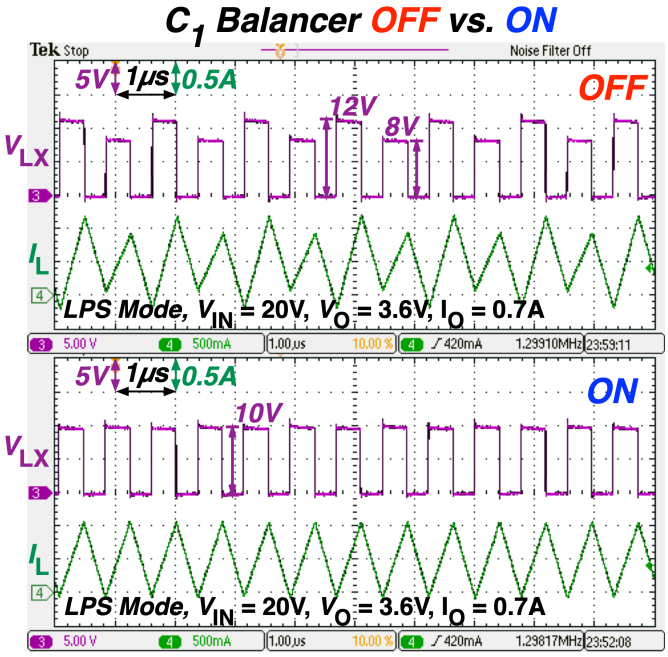



**Figure 4.29.** Measured $C_1$ voltage balancer performance with balancer off vs. on.

$V_{C1}$ is properly regulated to $V_{IN}/2$, resulting in balanced $V_{LX}$ switching and reduced $I_L$ ripple.

### 4.7.3 $V_{C1}$ Pre-charge and Start Up Measurements

The $C_1$ pre-charging and start-up sequece for the converter were verified and are demonstrated in Fig. 4.30 for a $V_{IN}$ = 20V start-up scenario while in LPS mode. As can be seen, $V_{C1}$ initially tracks $V_{IN}$ until it reaches 10V (i.e. $V_{IN}/2$). $V_{IN}$ then continues to 20V while $V_{C1}$ is regulated to 10V by the pre-charge control loop. PWM is then enabled (PC_EN = 0) and the $V_O$ regulation reference voltage, $V_{REF}$, is ramped up to its final value. The 2nd stage gradually enters normal operation as $V_O$ ramps up.

### 4.7.4 Automatic Mode and ACS Performance

The measured Auto mode with ACS performance during a load step induced LSP-to-LPS transition is shown in Fig. 4.31, where $I_L$ is properly shaped to the next mode. The $V_O$ droop, which includes the combined effects of the load current and mode change, is limited to 200mV. The same test was repeated for the fixed LSP and LPS modes which resulted in 160mV of droop

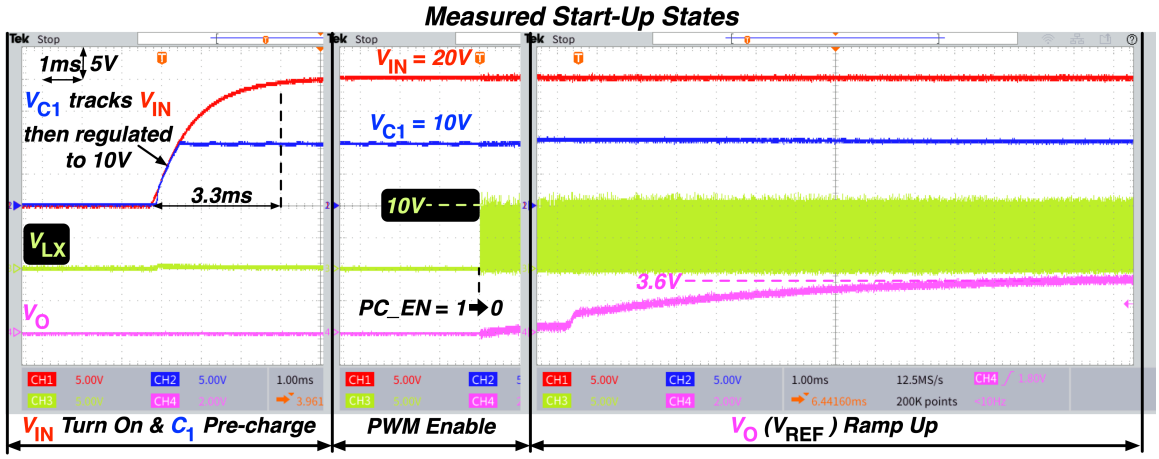



**Figure 4.30.** Measured $C_1$ pre-charge and start-up waveforms.

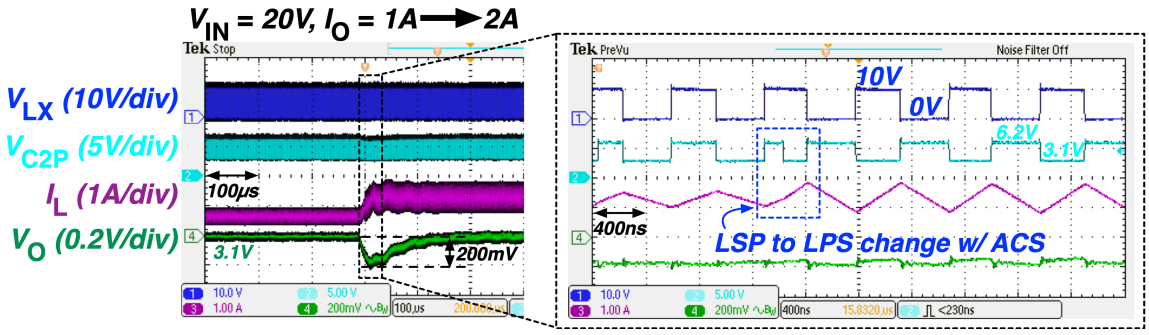



**Figure 4.31.** Measured LSP-to-LPS Auto Mode with ACS transition during a load step change.

as shown in Fig. 4.32, indicating the Auto mode with ACS transition adds only ~40mV of droop to the transient response. The same test was performed for the LPS-to-LSP transition with similar results as shown in Fig. 4.33.

### 4.7.5 Power Efficiency Performance vs. Modes and Operating Points

The measured power efficiency vs. $I_O$ vs. $V_{IN}$ plots across all modes with a 2.2µH (35mΩ DCR) 1210 case size chip inductor and $f_S$ = 600kHz (1.2MHz at inductor) in Fig. 4.34 show it achieves a peak efficiency of 94.8% and a peak output power of 21W while maintaining peak efficiencies >89.5% across all modes from a $V_{IN}$ of 5V–24V. The LSP and LPS mode plots with $V_{IN}$ = 20V also illustrate the VCR extension provided by Auto mode.

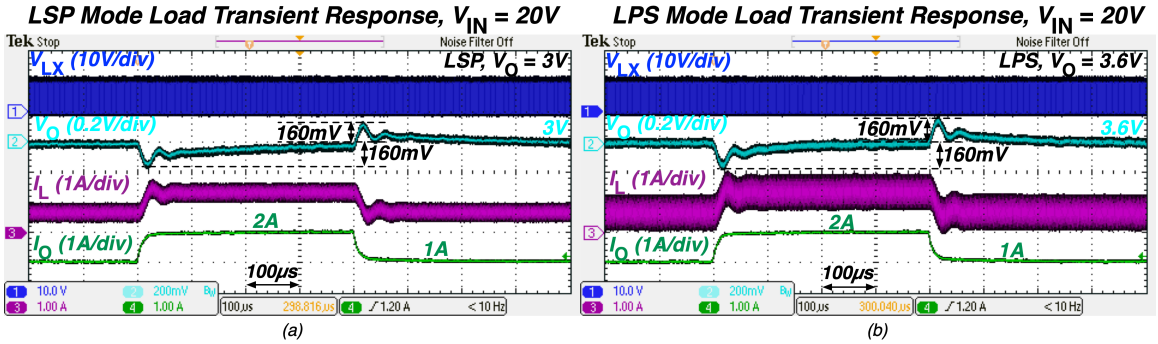



**Figure 4.32.** Measured load step response for fixed (a) LSP and (b) LPS modes.

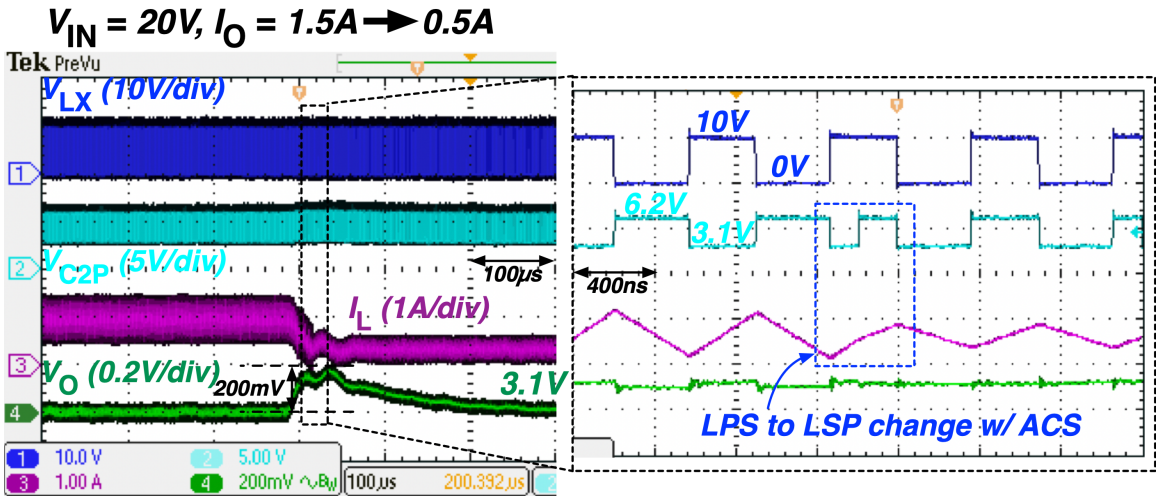



**Figure 4.33.** Measured LPS-to-LSP Auto Mode with ACS transition during a load step change.

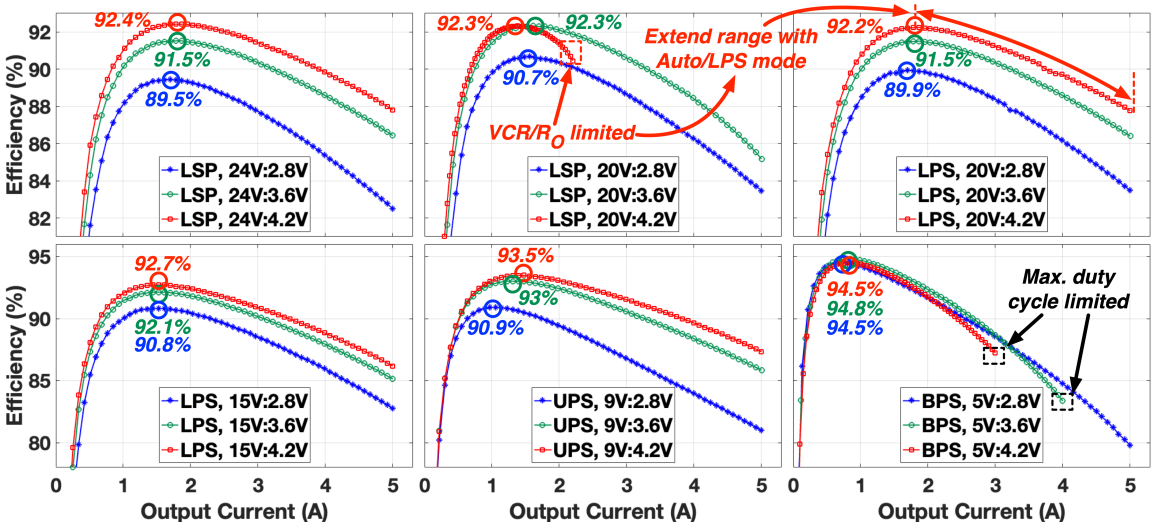



**Figure 4.34.** Measured power efficiency vs. output current vs. modes and input voltage.

**Table 4.3.** SIMS Converter performance comparison to prior works.

| | TI BQ25910 | Z. Xia ISSCC '21 | K. Wei ISSCC '20 | C. Hardy JSSC '19 | **This work** |
|---|---|---|---|---|---|
| Topology | 3-level Buck | Hyb. Casc. SC | Tri-State DSD | FIH | **Re-Cfg SIMS** |
| Technology | NR | 180nm | 180nm BCD | 130nm BCD | **180nm BCD** |
| Inductor Location | Output | Output | Output | Input | **Middle** |
| $V_{IN}/V_O$ Range | 3.9-14V/2-4.8V | 4-6V/0.4-1.2V | 12-24V/1V | 9V/3-4.2V† | **5-24V/2.8-4.2V** |
| Peak $I_O/P_O$ | 6A/22W^ | 1A/1.1W | 3A/3W | 3.4A/12.2W† | **5A/21W** |
| Pre-Charge? | Yes | Yes | Yes | No | **Yes** |
| Est. DC biased $C_{FLY}$ | 5.8µF^ | 3.2µF+6.4µF | 1µF+1µF†† | 6.6µF+13µF | **5.8µF+10µF** |
| Inductor (DCR) | 0.47µH (17mΩ) | 0.24µH (NR) | 2x560nH (NR) | 1µH (5.5mΩ)† | **2.2µH (35mΩ)** |
| Max. Power Density* | 1.64W/mm²^ | 0.1W/mm² | 0.48W/mm²** | 0.44W/mm²†^ | **0.86W/mm²** |
| Max. Eff. (at VCR) | 95.4% (0.76) | 96.9% (0.24) | 91.2% (0.08) | 94.3% (0.4)† | **94.8% (0.72)** |
| Min. VCR (at Eff.) | 0.14 (NR)^ | 0.08 (85.5%) | 0.04 (88.3%) | 0.33 (NR) | **0.12 (89.5%)** |

^ Estimated from reported data. NR: Not reported
* Area counts flying caps., inductors, and die areas. † Reported $V_{O1}$ performance with discrete inductor.
** Area counts die area only. †† Only nominal values reported.

### 4.7.6 Comparison to Prior Work

A comparison table is provided in Table 4.3. The prototype extends the $V_{IN}$ range by >88% compared to [18] and achieves wider VCR ranges over [52, 64, 65] while reducing inductor conduction losses.

## 4.8 Acknowledgment

Chapter 4, in part, has been accepted for publication of the material as it may appear in [22]:

C. Hardy and H. Le, "11.5 A 21W 94.8%-Efficient Reconfigurable Single Inductor Multi-Stage Hybrid DC-DC Converter," 2023 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, Feb. 2023.

The dissertation author is the primary author of these publications and the co-authors have approved the use of the material for this dissertation.

# Chapter 5

# Conclusion

In order to provide some background regarding the modeling approach of the converter prototypes discussed in this dissertation, Chapter 2 provided an overview of charge flow based analysis of conventional converters. This was intended to demonstrate the utility of the analysis method in the estimation of the loss modeling which were then utilized in the design and optimization of the converters presented in Chapters 3 and 4.

Chapter 3 presented a new step-down hybrid converter topology that uses an input flying inductor and a SC network to generate output voltages suitable for charging 1-cell or 2-cell batteries. The proposed topology relocates the inductor from the high-current output to the low-current input, while providing step-down conversion ratios that take advantage of the higher voltage settings of USB-C power delivery. Moreover, moving the inductor to the input allowed the parasitic inductance of a USB cable to be utilized in place of a discrete inductor in proposed a smart-cable architecture, eliminating the need for on-board magnetics and reducing on-board power dissipation. The converter prototype is implemented in 7.37 $mm^2$ of a 130nm BCD process and provides two outputs with ranges of 3–4.2 V and 6–8.4 V from a 9V input. With a 1µH discrete inductor, the prototype achieved peak powers of 12.2W and 31.9W and peak efficiencies of 94.3% and 97.4% for each output, respectively. The prototype was also demonstrated in a smart-cable architecture to limit on-board dissipation to 630 mW while delivering 7.2W at the first output or 350mW while delivering 14.4W at the second output.

Simultaneous data and power transfer and electromagnetic interference tests were also provided to support the feasibility of integration into a smart-cable architecture.

Chapter 4 presented a reconfigurable single inductor multi-stage hybrid step-down converter that efficiently provided the VCRs needed for 1-cell battery charging across a wide input voltage range of 5V–24V while moving the inductor away from the high output current path. The inductor is used to couple two synchronous SC stages to provide soft charging benefits to each stage. It extended reconfigurable SC and merged multi-stage operation concepts to deliver a maximum output current of 5A and achieved peak efficiencies of 94.8% and 92.4% from 5V and 24V input supplies, respectively.

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