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Thin-Body SOI Capacitorless DRAM Cell Design Optimization and Scaling

By

Min Hee Cho

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Tsu-Jae King Liu, Chair
Professor Ming C. Wu
Professor Junqiao Wu

Fall 2012

Thin-Body SOI Capacitorless DRAM Cell Design Optimization and Scaling

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by

Min Hee Cho

Abstract

Thin-Body SOI Capacitorless DRAM Cell Design Optimization and Scaling
by

Min Hee Cho

Doctor of Philosophy in Engineering – Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Tsu-Jae King Liu, Chair

Capacitorless dynamic random access memory (DRAM) is a promising solution to cell-area scalability and complex fabrication process issues for conventional DRAM. The thin body SOI transistor, which suppresses the short channel effect and also minimizes variability, is selected for the capacitorless DRAM cell structure. The impact of substrate doping concentration on capacitorless DRAM cell performance is studied and a novel selective well structure is proposed.

A capacitorless DRAM cell design with BJT-based operation (BJT mode) is known to have larger sensing margins and longer retention times. Controlling band-to-band tunneling leakage (BTBT) related to the electric field plays a key role in limiting retention time. In the BJT mode, BTBT in the Hold 0 state limits data retention time (D0 failure). By optimizing the underlap between the front gate and the source/drain regions as well as the operating voltages, retention time exceeding 1 second should be attainable for a cell with 25 nm gate length. The scaling limits of optimized capacitorless DRAM cells are also investigated through the analysis of variations. Signal sense margin analysis indicates that the ultimate scaling limit is 13 nm (gate length) for embedded DRAM applications and 16.5 nm for stand-alone DRAM applications.

The positive feedback MOSFET (PF-FET) was fabricated on thin body (10 nm) and UTBOX (10 nm) SOI structure. Positive feedback occurs as a result of both the BJT operation and the floating body effect from weak impact ionization. It exhibits very steep subthreshold slope of 0.03 mV/dec. Wide hysteresis enables the PF-FET to be utilized for memory application. The sensing margin is 62 μA/μm and retention time is greater than 4 seconds.

To my family for their unbounded love and encouragement,
to my sons for their great pleasure to me,
and to my wife, JiHye, for her devoted love and support.

Contents

Table of Contents ii

List of Figures vii

List of Tables x

Acknowledgements xi

Table of Contents

Chapter 1: Introduction ……………………….....………..……………1

1.1 Dynamic Random Access Memory (DRAM) …..………………………………..1

1.1.1 Conventional DRAM and Limitation ………….…..………….…..…………...1

1.1.2 Operating Principles of Capacitorless DRAM ..………..…………………….4

1.2 Structure Design and Simulation Models ...……………………….…………..….7

1.2.1 Thin Film SOI with UTBOX …..……………….………………………….7

1.2.2 Simulation Methodology …….…….….….……………………………………..10

1.2.3 Random Dopant Fluctuations (RDF) ..……….….………………….………..12

1.3 Dissertation Outline …………………………..…………………………..…13

1.4 References ……………………………………………………….…………...14

Chapter 2: The Characteristics of MOSFET-based Capacitorless DRAM with UTBOX FDSOI Structure ……………………….......16

2.1 Introduction ………..…………………….………………………………16

2.2 Device Structure and Operation …………………..………………......16

2.3 Optimization of Substrate Doping ……………..…………………......18

2.3.1 Simulation Approach ……………………………………………..18

2.3.2 Substrate Doping Effect ….……...…………………………………19

2.3.3 Random Dopant Fluctuations (RDF) …….……………………………20

2.4 Selective Well Design ....………..……………………….....................22

2.5 Summary ……………………...………………………………...................24

2.6 References ……………………………..25

Chapter 3: Design Optimization of BJT-based Thin-Body Capacitorless DRAM Cell …………………………………………………....27

3.1 Introduction ………………………..……………………………………27

3.2 Cell Design and TCAD Simulation …..……..…………………………......27

3.3 Mechanism of Data Retention Failure ……..………………………………........29

3.4 Methods for Improving Retention Time ……......……………….…………….....32

3.5 Impact of Random Dopant Fluctuations ……......……………….……………........35

3.6 Summary ….……………………………..……….....................................40

3.7 References ….……………………………………….................................41

Chapter 4: Implications of Variation ……...……….……………..……...43

4.1 Introduction …………………………..………………………………………43

4.2 Device Structure and Operation ……………………………………………...43

4.3 Sources of Variation ….……...………………………………………………....44

4.4 RDF effect ….………………………….……………………………………..45

4.5 Dimension Variation Effects …….………………….…………………………..46

4.6 Summary …….……………………………………………………………….49

4.7 References ……………………….……………………………………………..50

Chapter 5: Variation-Aware Study with Scaling Limit …….……........52

5.1 Introduction …………………………..………………………………………52

5.2 Body Thickness Limitation ………………...54

5.2.1 Reference Cell (25 nm Gate length) Design ……………………....54

5.2.2 Body Thickness Scaling ……….................………..……………....54

5.3 Design Optimization of Scaled Cells …….……………….........................56

5.3.1 Scaling Constraints ……..........….................……….…..………....56

5.3.2 Optimization of Cell Operating Voltages …....……..……..………....56

5.4 Scaling Limitation in Terms of Variation Factors ….………..........................62

5.4.1 Variation Factors ……....................………………..……………...62

5.4.2 Dimension Variation Effects with Scaling ………..……………………62

5.5 Summary …….……...………………………………………………….70

5.6 References ……….……………….…………………………………………..71

Chapter 6: Positive Feedback SOI Transistor and Its Capacitorless DRAM Application ……………………………………….……..74

6.1 Introduction ……………………………..……………………………………74

6.2 Principles ….………………………………………………….....................75

6.3 Positive Feedback Modeling & Properties ……..………….........................76

6.3.1 Simulation Modeling ……………………………………….………76

6.3.2 Simulated Structure …………………………………………..….77

6.3.3 Positive Feedback Characteristics ……………………………..…..……79

6.4 Device Structure and Fabrication ….…………..86

6.5 Measurement Configuration ….…………………..88

6.6 Experimental I-V Characteristics ….……………….......................................89

6.7 Capacitorless DRAM Application ….………………......................................91

6.8 Summary …….……………………………………………………….………94

6.9 References ………………………….……………………………………..…..95

Chapter 7: Conclusion ……………………………………………..…………97

7.1 Summary and Conclusion ……..…………………..……………………97

7.2 Contributions of This Work …..…………...99

7.3 Suggested Future Works …..……………..99

7.3.1 Overcoming Scaling Limits with 3D Structures/ New materials …..….99

7.3.2 Low Power Positive Feedback-FET ………………..……………..…101

7.3.3 Nonvolatile Memory Applications ……………………….…..…..…102

7.4 References ………………………..……………………………………..104

List of Figures

1.1 DRAM in semiconductor industry 2
1.2 Conventional 1T1C DRAM structure 2
1.3 A/R of storage node 3
1.4 Typical capacitorless DRAM 4
1.5 Capacitorless DRAM operation (MOSFET mode) 4
1.6 Ids-Vgs curve of Capacitorless DRAM (MOSFET mode) 5
1.7 Capacitorless DRAM operation (BJT mode) 6
1.8 BJT mode schematic 6
1.9 Cross section view of PDSOI transistor and FDSOI transistor 8
1.10 Characteristics of PDSOI and FDSOI 8
1.11 Thin film SOI (TEM and Cross-sectional view) 9
1.12 Thin film SOI transistor process flow 9
1.13 Randomly distributed dopants in an N-MOSFET 12

2.1 Simulated Read 1 and Read 0 currents for a FDSOI capacitorless DRAM cell 18
2.2 Hole density profile 19
2.3 Maximum band-to-band tunneling rate *vs.* peak electric field 20
2.4 Retention characteristics for a FDSOI capacitorless DRAM cell 20
2.5 Kinetic Monte Carlo (KMC) simulation 21
2.6 Standard deviation of threshold voltage distribution 21
2.7 Selective well cross section view 22
2.8a Electric field profile within the SOI film 23
2.8b BTBT rate within the SOI film 23
2.9 Various p-well widths for selective wells 23
2.10 Comparison of retention time for various widths of the p-well 24

3.1 Electric field contour maps for a BJT mode cell in the Hold state 29
3.2 Maximum electric field in the gate oxide during a Hold operation 29
3.3 Relationship between electric field and BTBT 30
3.4 Band-to-band tunneling rate contour maps 30
3.5 Energy band diagrams of D1 Hold state and D0 Hold state 31
3.6 Read current *vs.* hold duration 31
3.7 Electric field profile within the body 32
3.8 Read current *vs.* hold duration for various values of gate-sidewall spacer width 33

3.9a Retention time *vs.* spacer width 34
3.9b Retention time *vs.* front-gate bias during Hold operation 34
3.9c Retention time *vs.* drain bias during Read operation 34
3.10 3-dimensional view of a capacitorless DRAM cell 35
3.11 Capacitorless DRAM cell designs used for KMC simulations 36
3.12 Read 1 and Read 0 current distributions at 1μs Hold duration 37
3.13 Normal probability plots for Read 1 and Read 0 currents 38-39
3.14 Comparison of retention characteristics 39

4.1 Doping contour map showing variation Factors 44
4.2 Measured SOI film thickness across a wafer 45
4.3 Simulated retention characteristics showing the impact of RDF 46
4.4 Sigma sensitivity plots for capacitorless DRAM read current 47
4.5 Band diagrams 1nm below gate oxide at the Read 0 state 48
4.6 Signal sense margin (SSM) and median sensing current 49

5.1 Process for determining scaling limit of the BJT mode capacitorless DRAM cell 53
5.2 Retention characteristics for each body thickness 55
5.3 Cross sectional view of contour plots for hole density 55
5.4 Optimization for L_g=25 nm 57
5.5 Optimization for L_g=20 nm 57
5.6 Optimization for L_g=15 nm 58
5.7 Optimization for L_g=12 nm 58
5.8 Optimization for L_g=10 nm 59
5.9 Optimization for L_g=9 nm 59
5.10 Electric field for optimized operating voltages for each gate length 60
5.11 Median retention time with gate length 61
5.12 Gate length= 25 nm for sigma sensitivities, and signal sense margin 64
5.13 Gate length= 20 nm for sigma sensitivities, and signal sense margin 65
5.14 Gate length= 15 nm for sigma sensitivities, and signal sense margin 66
5.15 Gate length= 12 nm for sigma sensitivities, and signal sense margin 67
5.16 Gate length= 9 nm for sigma sensitivities, and signal sense margin 68
5.17 Time to Zero SSM (TZS) *vs.* gate length 69

6.1 Positive feedback flow 76
6.2 Cross-sectional doping contour map 78

6.3 I_{ds}-V_{gs} curve with double sweep 79
6.4 I_{ds}-V_{gs} curve with different gate oxide thicknesses (double sweep) 81
6.5 Gate oxide thickness effect on forward trigger voltage and Window 81
6.6 I_{ds}-V_{gs} curve with different body thicknesses (double sweep) 82
6.7 Body thickness effect on forward trigger voltage and Window 82
6.8 I_{ds}-V_{gs} curve with different BOX thicknesses (double sweep) 83
6.9 BOX thickness effect on forward trigger voltage and Window 83
6.10 I_{ds}-V_{gs} curve with different gate lengths (double sweep) 84
6.11 Gate length effect on forward trigger voltage and Window 84
6.12 I_{ds}-V_{gs} curve with different drain voltages (double sweep) 85
6.13 Drain voltage effect on forward trigger voltage and Window 85
6.14a The relation between V_{TF} and Window 86
6.14b Slopes for each factor 86
6.15 Cross-section view of a thin body SOI with UTBOX device 87
6.16 Process flow of device fabrication 87
6.17 The measurement setup 88
6.18 I_{ds}-V_{gs} curve for positive feedback transistor 89
6.19 I_{ds}-V_{gs} curve with various V_{ds} 90
6.20 I_{ds}-V_{ds} curve with various V_{gs} 90
6.21 Capacitorless DRAM operating conditions 92
6.22 Sensing current *vs.* Hold time plots for capacitorless DRAM operation 93
6.23 Retention characteristics of PF-FET capacitorless DRAM 93

7.1 Illustration of multi-gate MOSFET structures 100
7.2 Vertical capacitorless DRAM structure using band gap engineering 101
7.3 The tentative concept for NVM application using PF-FET 102
7.4 I_{ds}-V_{gs} curves for NVM using PF-FET 102

List of Tables

1.1 DRAM technologies 3
1.2 Optimized dimension parameters for thin film SOI transistor with UTBOX 9

2.1 FD-SOI capacitorless DRAM cell design parameters 17
2.2 FD-SOI capacitorless DRAM cell biasing conditions 17

3.1 Capacitorless DRAM cell design parameters 28
3.2 Operating voltages for BJT mode 28
3.3 Operating voltages for MOSFET mode 28
3.4 Optimized operating conditions for BJT mode 35
3.5 Summary of RDF simulation results 40

4.1 Capacitorless DRAM cell operating voltages 44
4.2 Parameter variations are considered 45

5.1 Capacitorless DRAM cell operating voltages 54
5.2 Optimized operating voltages for each gate length 60
5.3 Retention time and electric field for each gate length 61
5.4 Variation factors used for device simulations 62

6.1 The summary of selected parameters for positive feedback simulation 77
6.2 Positive feedback transistor cell design parameters 78
6.3 PF-FET capacitorless DRAM cell biasing conditions 92

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Chapter 1

Introduction

1.1 Dynamic Random Access Memory (DRAM)

1.1.1 Conventional DRAM and Limitation

Dynamic random access memory (DRAM) is the most common kind of random access memory for mobile/personal computers and workstations. Memory is defined as a device (as a chip) or a component of a device in which information especially for a computer can be inserted and stored and from which it may be extracted when wanted. Random access allows stored data to be accessed in any order. A conventional DRAM cell has simple structure, which is composed of one transistor and one capacitor (1T1C) per bit [1]. The transistor acts as a switch for input and output. Different from static RAM (SRAM), DRAM is dynamic in operation; it needs to have its storage cells refreshed every few milliseconds. Since real capacitors and transistors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. DRAM is also volatile, since it loses its data when the power supply is removed. Because of the DRAM cell structure (1T1C) its size is smaller than a SRAM cell which has six transistors. This allows DRAM to reach very high density. The DRAM market in the semiconductor industry occupies a large portion, as shown in **Fig. 1.1** [2, 3], which means that more innovative research is needed to in order to maintain a competitive edge.

Fig. 1.2 shows the conventional DRAM structure (capacitor over bit line (COB) type) [4]. At the sub-30nm half pitch, conventional DRAM cells might suffer from technological scaling issues, as shown in **Table 1.1** and **Fig. 1.3** [5]. It is harder to build a capacitor in a small cell-area with sufficient capacitance, usually 20~25 fF [5] to provide enough signal-to-noise ratio, as compared with transistor scaling. Novel high dielectric-constant (high κ)

materials or capacitor structures have been proposed to overcome scaling issues and have become the main focus for current DRAM technologies [6]. DRAM designers have pioneered the use of high-k dielectrics (*e.g.,* ZrO_2, HfO_2, or $SrTiO_3$ *etc.*), and extreme capacitor geometry (*e.g.*, trench, fin, and stack). Despite this comprehensive approach, however, the scaling of 1T1C DRAM cells has significant obstacles due to the capacitor.

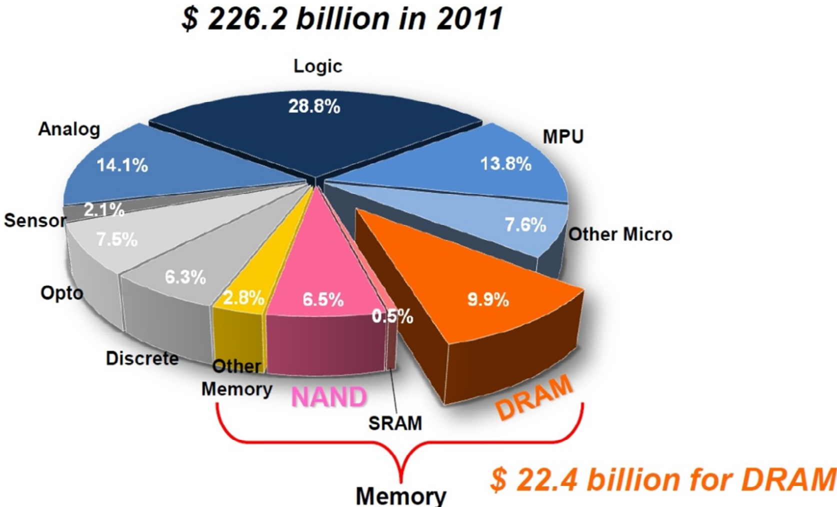


Figure 1.1. DRAM in semiconductor industry [2, 3].

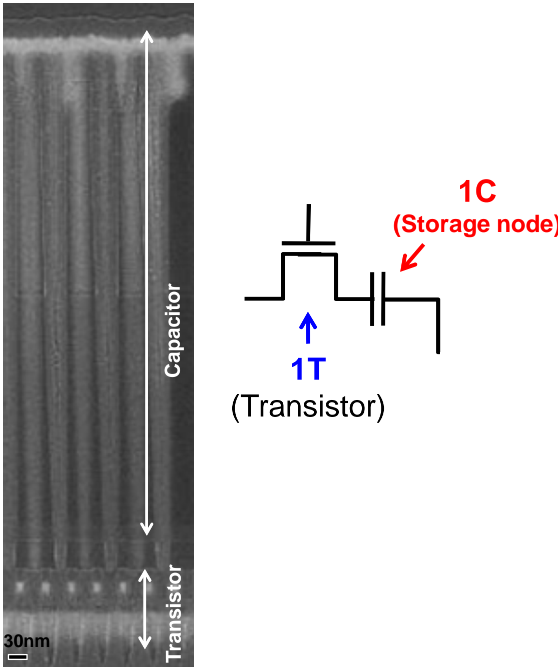


Figure 1.2. Conventional 1T1C DRAM structure. Each cell has one transistor (switch) and one capacitor (storage node) [4].

Besides the fact that the fabrication process for DRAM of several gigabits and beyond is becoming more and more difficult, the development and manufacturing costs are increasing drastically. A significant portion of the technology developed for DRAM is not extendible to other products. In order to overcome cell-area scalability and the process complexity issues of traditional DRAM technology, the concept of capacitorless DRAM was introduced in the early 1990s [7].

Year	Half Pitch (nm)	Cell Size (μm^2)	A/R of SN	A/R of SN (out) for cell plate deposition
2010	45	0.0122	47.3	74.5
2011	40	0.0096	57.5	97.5
2012	36	0.0078	44.4	77.5
2013	32	0.0061	56.2	108.3
2014	28	0.0047	73.5	163.2
2015	25	0.0038	76.9	199.9
2016	22	0.0029	99.4	330.5
2017	20	0.0024	108.3	351.9

Legend
Manufacturable solutions exist
Manufacturable solutions are known
Manufacturable solutions are NOT known

Table 1.1. DRAM technologies. Half pitch, aspect ratio (A/R) of capacitor (storage node: SN), and A/R of SN (out) for cell plate (upper electrode) deposition are shown in table. Source; International Technology Roadmap for Semiconductors (ITRS) 2011 [5]. White = Manufacturable solutions exist, yellow = Manufacturable solutions are known, and red = Manufacturable solutions are NOT known.

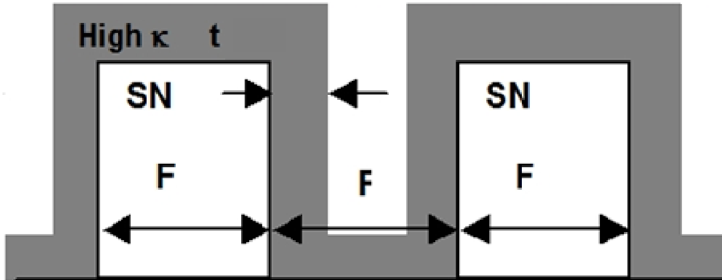


Figure 1.3. A/R of storage node is calculated as (SN height) / F, and A/R of SN (out) is calculated as (SN height) / (F – 2×t). F = minimum feature size, t = physical high k dielectric layer thickness [5].

1.1.2 Operating Principles of Capacitorless DRAM

Fig. 1.4 shows a cross section view of a typical capacitorless DRAM [8]. Its structure is very simple – one transistor on a silicon-on-insulator (SOI) wafer. Capacitorless DRAM can provide important advantages to chip manufacturers, who are reluctant to add any new material to their already complex and delicate processes [9]. Extra processing steps are highly undesirable for memory chip producers, because they increase manufacturing costs, often greatly. Thus this is a major advantage of capacitorless DRAM. Each memory cell is just a single transistor. For comparison, conventional on-chip memories (SRAM) typically use six transistors per memory cell, so we can fit more cells into the space occupied by conventional embedded memory. This increases the amount of memory on the chip and thereby improves its performance, making the chip a lot smaller and less expensive [9].

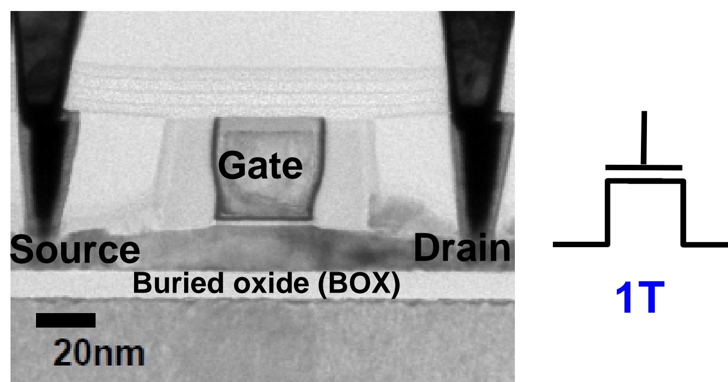
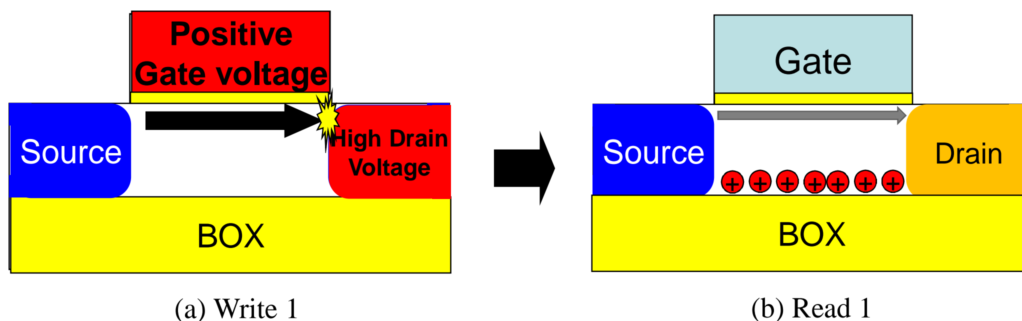


Figure 1.4. Typical capacitorless DRAM [8]. Only one transistor on SOI wafer.



(a) Write 1 (b) Read 1

Figure 1.5. Capacitorless DRAM operation (MOSFET mode). (a) Write 1 (*i.e.* programming). N-MOSFET turns on and high drain voltage (usually > 2V) is applied in order to induce impact ionization. (b) Read 1 (Read programmed cell state). Due to floating body effect, threshold voltage (V_T) is lowered. Higher current flow compared to Read 0 state (No charge stored state: V_T is high).

The original concept of capacitorless DRAM utilizes the floating-body effect of a SOI transistor [7]. In capacitorless DRAM, the conventional storage capacitor can be replaced by the body capacitance of the transistor. **Figs. 1.5 (a)** and **(b)** show Write 1 (*i.e.* programming) and Read 1 (*i.e.* reading programmed cell state) processes. When the transistor turns on and high drain voltage is applied, impact ionization occurs and electron-hole pairs are generated due to the high electric field. When excess holes exist in the floating body, the cell state can be defined as "1" (Data 1 state). On the other hand, when excess holes are swept out of the floating body through the forward bias on the body - drain junction, the cell state can be defined as "0" (Date 0 state). By measuring the drain current difference between the Read 1 and Read 0 states of the cell, we can sense whether the holes are accumulated in the floating body as shown in **Fig. 1.6.** In other words, a logic state is defined by creating an excess or a shortage of the majority carriers (ΔQ) inside the body of the transistor. When a number of majority carriers are stored in the SOI, the body effect changes the transistor threshold voltage (V_T) and hence its on-state drive-current. This is the basic method that the capacitorless DRAM uses to distinguish two states. Okhonin *et al.* referred to this MOSFET operation mode with floating body effect (MOSFET mode) Generation 1 mode (Gen1) [10]. In the last 20 years, several research groups and companies have published researches about MOSFET mode [8, 11, 12], and it is investigated here, in chapter 2. This mode provides stable operations in partially depleted SOI (PDSOI), and operating voltage conditions (front gate, back gate bias) are very similar to the normal MOSFET operation.

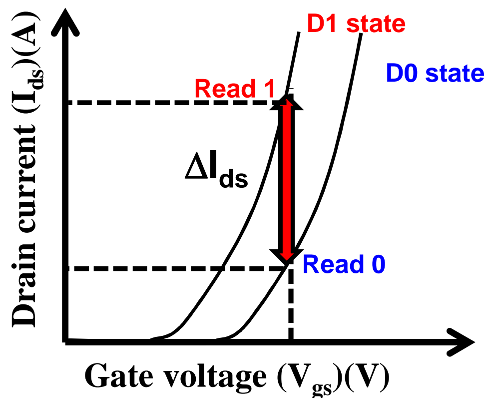


Figure 1.6. I_{ds}-V_{gs} curve of Capacitorless DRAM (MOSFET mode). In data 1 state (D1), high current flows due to floating body effect. V_T is high in data 0 state (D0).

More recently, Okhonin *et al.* introduced the bipolar junction transistor (BJT) based operation mode (BJT mode) of capacitorless DRAM [10]. While the MOSFET mode uses the triode operation of MOSFET in the Read state, the BJT mode is largely based on the parasitic BJT which is present in the MOS structure (**Fig. 1.7**). The basic Write operation uses the punch-through effect in Write 1 (**Fig. 1.7(a)**). Negative gate and high positive drain biases are applied. Impact ionization occurs as a result of the punch-through current

(not the inversion current in the channel) and majority charges are accumulated near the front gate rather than the buried oxide (BOX) interface, as shown in **Fig. 1.7(b)**. In the case of an N-channel device, the N+ source, the P-type body, and the N+ drain form the emitter, the base, and the collector of an NPN bipolar transistor, respectively. In a floating body SOI device, the body (*i.e.* the base of the bipolar transistor) is used as a storage node (**Fig. 1.8**) [10]. The Read operation is performed by sensing the bipolar current in contrast to the MOSFET mode capacitorless DRAM, where the channel current is used. During the Read operation, the bipolar transistor is in a state of turn-on when the cell state is Data 1. It is in a state of turn-off when there are very few holes left, which means that the potential barrier from the source (emitter) to the drain (collector) is high enough to prevent on-current.

The BJT mode improves sensing margin [10] (*i.e.* the difference between Read 1 and Read 0 current) due to the higher current gain of the BJT [11]. Data retention time is expected to increase [10]. Because the capacitive coupling to the body of the front gate is higher than that of the back gate, it is much more effective to retain holes in the body using the front gate. The higher margin provides much shorter data read times and better device scalability. This improvement also broadens the range of applications that can take advantage of the high density of a capacitorless DRAM chip.

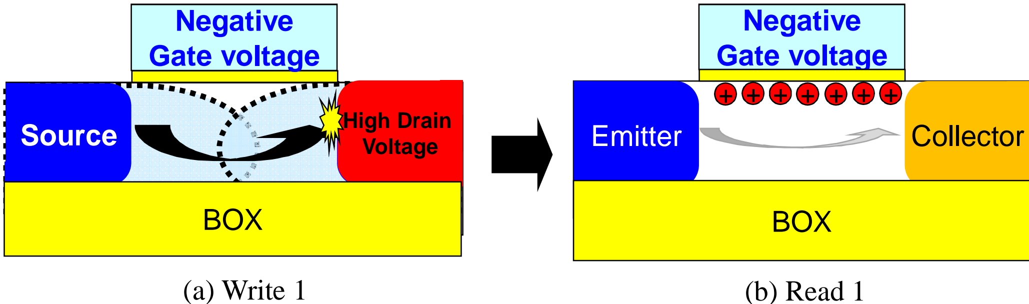


Figure 1.7. Capacitorless DRAM operation (BJT mode). (a) Write 1. High drain voltage (usually > 2V) is applied and punch-through occurs, which induces impact ionization. (b) Read 1. Negative gate bias retains holes below gate oxide. Under the BJT operation mode, BJT current flow through emitter (source) to collector (drain).

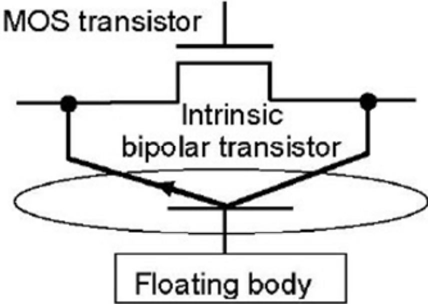


Figure 1.8. BJT mode schematic [10].

1.2 Structure Design and Simulation Models

1.2.1 Thin Film SOI with UTBOX

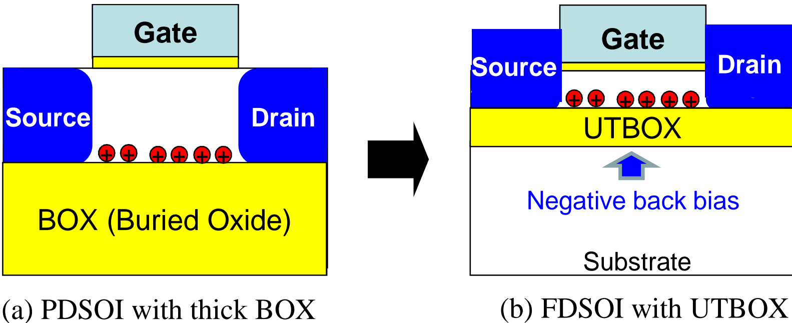
Planar bulk and/or PDSOI technology face many obstacles to widespread adoption. They suffer from the short channel effect (V_T reduction with decreasing gate length) with sub-surface leakage paths and drain induced barrier lowering (DIBL). Increasing variability in transistor and circuit performance for these structures require more complex chip design. In order to suppress off-state leakage, heavy channel doping can be used [11]. As the channel doping and/or halo doping in conventional planar bulk/PDSOI MOSFETs is increased with scaling to suppress short-channel effects, random-dopant-fluctuation (RDF)-induced variation also increases. Rather than doping the channel heavily to suppress off-state leakage, body thickness can be reduced substantially [12]. As a result, the channel/body region is so thin (with a thickness less than 1/3 of the gate length) that it is fully depleted of mobile charge carriers when the transistor is in the off state. Due to high coupling of the gate, the short channel effect of the transistor can be suppressed effectively with fully depleted SOI (FDSOI) structure. The use of a lightly doped SOI MOSFET structure with an ultra-thin (~10 nm-thick) buried oxide (UTBOX) and a heavily doped substrate has been reported to be effective for suppressing this variation [13, 14]. RDF-induced V_T variation can be dramatically lower in a FDSOI MOSFET since light channel/body doping can be used. Simple structure and fabrication processes of FDSOI are also advantages. With a thin film SOI substrate, FDSOI is easily implemented [15].

For memory applications, the floating body effect is essential for V_T shift. The floating body effect, however, is negligible in an FDSOI MOSFET because there is no quasi-neutral body region which serves as a potential well to hold majority carriers [16, 17]. UTBOX is essentially back-gated MOSFET. With the control of the back bias (Vbg), it is possible to retain excess hole in the body. This pseudo-floating body effect enables the utilization of FDSOI in capacitorless DRAM.

The thin body may induce higher source/drain resistance, which reduces the on-current. The raised-source/drain structure provides a good solution for minimizing source/drain series resistance [18]. The problems of PDSOI MOSFET and the characteristics of FDSOI MOSFET as a solution are explained in **Figs. 1.9** and **1.10**. The thin film SOI using UTBOX technology can meet requirements for capacitorless DRAM applications with regard to scalability, memory effect (floating body effect), low variability, and manufacturability.

Fig. 1.11 (a) shows a cross-sectional view of the reference structure (transmission electron microscope (TEM) image [18]), and a simulated N-channel MOSFET structure, based on fabricated MOSFET (**Fig. 1.11 (a)**) is shown in **Fig. 1.11(b)**. An implantation-free process is used in order to avoid dopant-atom straggle as well as defects in the body region, and to minimize RDF-induced variations, as follows [18]: in order to decrease series resistance with reducing gate-sidewall capacitance, faceted raised source/drain (RSD) processes are selectively grown. This structure can be formed with a low-temperature, zero-

silicon-loss epitaxial growth process, with in-situ doping (around $10^{20}cm^{-3}$). Dopant atoms from the raised-source/drain regions diffuse into the channel and form the lightly doped source/drain extension regions.



(a) PDSOI with thick BOX (b) FDSOI with UTBOX

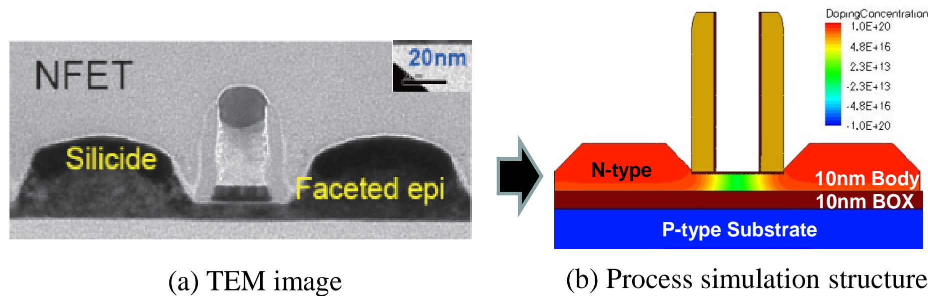
Figure 1.9. Cross section view of (a) partially depleted SOI (PDSOI) transistor and (b) fully depleted SOI (FDSOI) transistor with raised source/drain and ultra-thin BOX (UTBOX).

PDSOI problems	Solution : FDSOI
Short Channel Effect (SCE)	Coupling of gate ↑ → Suppress SCE
Random Dopant Fluctuation (RDF)	Intrinsic Channel → Less RDF

FDSOI problems	Solution
No floating body effect (no memory effect)	Ultra Thin BOX (< 20nm) & Back bias
Small current (from high S/D resistance)	Raised S/D

Figure 1.10. Characteristics of PDSOI and FDSOI. Raised source/drain with UTBOX FDSOI is proposed as a solution.

Physical and operating parameters (gate length, gate oxide thickness, supply voltage, *etc.*) are taken from the International Technology Roadmap for Semiconductors for low operating power (LOP) technology at the 22 nm node [5]. The initial width of the gate-sidewall spacers (W_{spacer}) is selected to be 13 nm, based on the gate-to-contact spacing design rule for recent study (6-T SRAM cell) [14]. The gate work function values were then selected to adjust the nominal V_T values in order to meet the off-state leakage current (I_{OFF}) specification, 3 nA/μm. The fabrication processes are shown in **Fig. 1.12** and the optimized dimension parameters for the device are summarized in **Table 1.2**.



(a) TEM image (b) Process simulation structure

Figure 1.11. (a) TEM (transmission electron microscope) image of thin film SOI with UTBOX (reference structure [15]). (b) Cross-sectional view of simulated n-channel MOSFET structure based on (a).

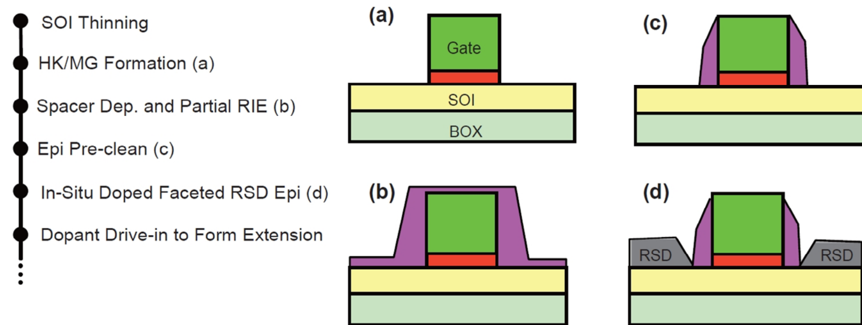


Figure 1.12. Thin film SOI transistor process flow: no Si loss is achieved by an optimized partial spacer dry etch; The remaining nitride is removed during epi-precleaning. An in-situ doped *faceted* RSD is formed to minimize parasitic capacitance. Extensions are formed by dopant drive-in from in-situ doped RSD to avoid implant damage to transistor [18].

	Dimension
Physical gate length (Lg)	25nm
Physical gate width	50nm
Spacer width (W_{spacer})	13nm
Gate oxide (T_{OX})	1nm
Body thickness (T_{Si})	10nm
BOX thickness (T_{BOX})	10nm
Channel doping	Intrinsic
Source/Drain doping	$10^{20}cm^{-3}$
Substrate doping	$10^{18}cm^{-3}$
Gate work function	4.6eV

Table 1.2. Optimized dimension parameters for thin film SOI transistor with UTBOX

In this simulated structure, the *Sentaurus Process* is used and it provides a complete and highly flexible, multidimensional, process modeling environment [19]. Calibrated to a wide range of the latest experimental data using proven calibration methodology, this computer-aided design (TCAD) tool offers unique predictive capabilities for modern silicon and non-silicon technologies.

1.2.2 Simulation Methodology [20]

In this study, the Sentaurus Device is chosen as the TCAD simulation tool [20]. Proper physical models are selected to embody capacitorless DRAM, which allows for the possibility to simulate real phenomena. This section describes the selected physical models and the reasons why they are chosen.

1) Electrostatic Potential

Ionized dopants or traps (immobile charges) and electrons/holes (mobile charges) play key roles in all semiconductor devices. These charges and the electrostatic potential determine the electrostatic potential, and vice versa. Physical phenomena in semiconductor devices can be complicated and depends on charge distribution, microscopic physics, the applied bias, and the structure of the device. All charges in the device interact with each other and should be calculated with the electrostatic potential. These are calculated based on Poisson's equation, which is:

$$\nabla \cdot \left(\varepsilon \nabla \phi + \bar{P} \right) = -q(p - n + N_D - N_A) - \rho_{\text{trap}} \qquad (1)$$

Where:

ε : the electrical permittivity

$\bar{P}$: the ferroelectric polarization

q : the elementary electronic charge.

n and p : the electron and hole densities.

N_D and N_A: the concentration of ionized donors and acceptors

ρ_{trap} : the charge density contributed by traps and fixed charges

2) Hydrodynamic Transport Model: Hydrodynamic (eTemperature)

Characteristics of state-of-the-art scaled semiconductor devices cannot be described properly using the conventional drift-diffusion transport model. In particular, the drift-diffusion approach cannot reproduce velocity overshoot and often overestimates the impact ionization generation rates. The hydrodynamic (or energy balance) model provides a very adequate compromise. It takes into account an average of the carrier temperature as well as the lattice temperature, which can be useful in devices where the carrier diffusion is important. This model can also reduce possible convergence errors and simulation times.

3) Semiconductor Band Structure

The most fundamental property of a semiconductor is its band structure. Realistic band structures are complex and can only be fully accounted for in Monte Carlo simulations. The band structure is simplified to several quantities: the energies of the conduction and valence band edges, and the density-of-states masses for electrons and holes. The silicon band-gap narrowing model determines the intrinsic carrier concentration. In this simulation, *OldSlotboom* model is selected, which is based on measurements of in n-p-n transistors, because the BJT mode is used in capacitorless DRAM.

4) Mobility

The Sentaurus Device uses a modular approach for the description of the carrier mobility. The mobility is a function of both phonon scattering and coulombic scattering. The lattice temperature mobility model is called the constant mobility model and it should only be used for undoped materials. For doped materials, the carriers scatter with impurities. This leads to a degradation of the mobility. The mobility degradation at interfaces, (*e.g.* the silicon/oxide interface in the channel region of a MOSFET) is also considered. These models account for the scattering of surface phonons and surface roughness. Additionally, this simulation includes the effects of carrier–carrier scattering and electric fields.

5) Recombination:

Generation and recombination processes are very important in device physics, and in particular, for capacitorless DRAM devices. These processes exchange carriers between the conduction and valence bands. For each individual generation or recombination process, the electrons and holes involved appear or vanish at the same location. The only exception is the band-to-band tunneling (BTBT) model.

Shockley–Read–Hall (SRH) recombination: Recombination through deep defect levels in the gap is usually labeled as SRH recombination. SRH lifetimes depend on doping, temperature, electric field, *etc.*

Surface SRH Recombination: The surface SRH recombination model can be activated at the interface between two different materials or two different regions.

Auger Recombination: At high carrier densities the Auger recombination is very important. Because high current are induced in the Write 1 state in capacitorless DRAM, it should be considered when conducting simulations.

Avalanche Generation: The floating body effect comes from a generated electron-hole pair. It is one of key models for Write 1. Electron–hole pair production due to avalanche generation (impact ionization) requires certain threshold field strength and the possibility of acceleration, that is, wide space charge regions. If the width of a space charge region is greater than the mean free path between two ionizing impacts, charge multiplication occurs, which can cause electrical breakdown. The reciprocal of the mean free path is called the ionization coefficient.

Band-to-Band Tunneling Models: Band-to-Band Tunneling (BTBT) leakage is a main reason for the degradation of retention time in capacitorless DRAM. Because capacitorless

DRAM has little junction leakage (due to the SOI structure) and no dielectric leakage of capacitor, there are fewer leakage path in the structure compared to conventional DRAM. However, holes should be retained in the body, which is acutely affected by BTBT leakage. Phonon-assisted band-to-band tunneling cannot be neglected in steep p-n junctions or in high electric fields of MOS structures. Due to this factor, defect-assisted tunneling (SRH) is also considered for the device simulations.

6) Quantum Well

With scaling, quantum confinement effect is another factor that should be considered. The Quantum Well (QW) sub-band model, the QW transport model, and the scattering model are all activated in this simulation.

1.2.3 Random Dopant Fluctuations (RDF)

Fig. 1.13 shows randomly distributed dopant atoms in an n-channel MOSFET [21]. Previous experiments and simulation have confirmed RDF as one of the obstacles to continued transistor scaling [14, 21-25]. It is well known that RDF-induced V_T variation is inversely proportional to $(W \times L)^{0.5}$, where W and L are the transistor channel width and length, respectively [26]. Recently, in a 100,000-sample 3-dimensional simulation study [23], the complete V_T distribution caused by RDF was constructed through the discrete convolution of a Poisson distribution with the mean (N) of the number of dopants in channel region, and a Gaussian distribution of V_T for a fixed N. Because the channel doping is intrinsic in FDSOI, there are fewer issues for random dopant fluctuations (RDF) compared to PDSOI or bulk transistor. RDF is still one of main variation factors in ultra-scaled devices though RDF is suppressed effectively in FDSOI [22]. Randomly distributed dopants affect not only V_T variation but also the impact ionization rate and the local BTBT rate, which can influence retention time and sensing current.

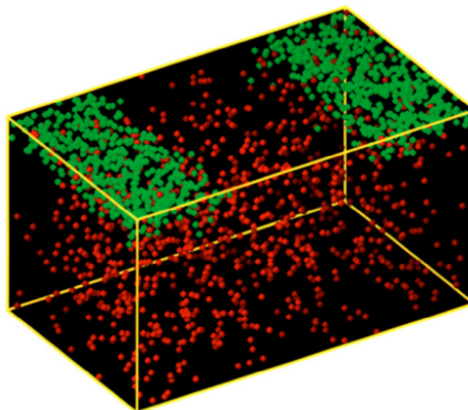


Figure 1.13. Randomly distributed dopants in an N-MOSFET with channel length of 30 nm and channel width of 50 nm [23]. Green atoms are donors and red colored atoms are acceptors.

1.3 Dissertation Outline

Thin body SOI with UTBOX structure is very a promising design for scaled technologies. It suppresses the short channel effect and minimizes variability. The application of thin body SOI with UTBOX MOSFET to capacitorless DRAM is important because this device has many advantages such as simple processes, high scalability, and reduced variability. This research focuses on the optimization, analysis, and scalability of capacitorless DRAM with highly scaled (22nm-node) technologies.

In chapter 2, the impact of substrate doping on back-gated FDSOI capacitorless DRAM cell performance is investigated to provide guidance for design optimization. In this chapter, the basic capacitorless operating mode (MOSFET mode) is focused upon. In order to optimize the tradeoff between increasing sensing margin and degraded retention time, the peak doping concentration is investigated

In chapter 3, a capacitorless DRAM cell design using BJT mode is studied. The impact of gate-sidewall spacer width and operating voltages is investigated to reduce BTBT leakage. Kinetic Monte Carlo (KMC) simulations are used to compare the effects of RDF on the read current distributions of cells designed for BJT-mode *vs.* MOSFET-mode operation. It is found that BJT-based operation is more robust to RDF effects than metal-oxide-semiconductor field-effect transistor (MOSFET)-based operation.

In chapter 4, variability in back-gated thin-body capacitorless DRAM cell performance is investigated. Sources of variability considered include variations in front gate oxide thickness, body thickness, buried oxide thickness, and gate-sidewall spacer width, as well as RDF. The BJT mode is most sensitive to variations in body thickness and buried oxide thickness. Reduced retention time, taking into account process-induced variations, is predicted in this chapter.

In chapter 5, the scaling limitation of capacitorless DRAM is investigated. Based on the analysis method in chapter 4, dimension variations are simulated. After body thickness limit is investigated, optimized conditions for each scaled device are achieved using the constant electric field rule. Design parameters (W_{spacer}, T_{Si}, T_{BOX}, and T_{OX}) and RDF are considered as variation factors. In this study, the scaling limit of capacitorless DRAM is predicted.

In chapter 6, positive feedback MOSFET is tested experimentally with SOI transistor. The device was fabricated on thin body (10 nm) and thin BOX (10 nm) SOI structure. Positive feedback occurs as a result of both the BJT operation and the floating body effect from weak impact ionization. Steep sub-threshold slope is achieved with positive feedback. Positive feedback properties are investigated utilizing TCAD simulation. Positive feedback and wide hysteresis window are measured, which enables the PF-FET to potentially serve as a memory device. The PF-FET capacitorless DRAM characteristics (retention time and sensing current) are measured experimentally.

Chapter 7 summarizes the key results and contributions of this dissertation; future research directions are also suggested.

1.4 References

[1] R.H. Dennard, “Field-Effect Transistor Memory”, U.S. patent 3,387,286, 1968.

[2] S. Y. Cha “DRAM Technology - History & Challenges,” *IEDM short course*, 2011.

[3] World Semiconductor Trade Statics (WSTS). [Online]. Avalable: 2011 http://www.wsts.org/

[4] T. Schloesser, F. Jakubowski, J. v. Kluge, A. Graham, S. Slesazeck, M. Popp, P. Baars, K. Muemmler, P. Moll, K. Wilson, A. Buerke, D. Koehler, J. Radecker, E. Erben, U. Zimmermann, T. Vorrath, B. Fischer, G. Aichmayr, R. Agaiby, W. Pamler, T. Schuster, W. Bergner, and W. Mueller, “A $6F^2$ Buried Wordline DRAM Cell for 40nm and Beyond,” *IEDM Tech. Dig.*, Dec. 2008, pp. 1 – 4.

[5] International Technology Roadmap for Semiconductors (ITRS). [Online]. Available: http://public.itrs.net

[6] S. Hong, “Memory technology trend and future challenges,” *IEDM Tech. Dig.*, Dec. 2010, pp. 12.4.1 - 12.4.4.

[7] H.-J. Wann and C. Hu, “Capacitorless DRAM Cell on SOI Substrate,” *IEDM Tech. Dig.*, Dec. 1993, pp. 635 – 638.

[8] S. Kim, R. J. Tseng, W. Rachmady, B. Jin, U. Shah, I. Ban, U. E. Avci, and P. L..D. Chang, “Silicon on Replacement Insulator (SRI) Floating Body Cell (FBC) Memory,” *VLSI Symp. Circuit Dig.*, Jun. 2010, pp. 165-166.

[9] S. K. Moore, “Master of memory”, *IEEE Spectrum*, Jan. 2007, pp. 45-49.

[10] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni, “New Generation of Z-RAM,” *IEDM Tech. Dig.*, Dec. 2007, pp. 925-928.

[11] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices. Cambridge, U.K.: Cambridge Univ. Press, 2006.

[12] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, “Ultra-thin body SOI MOSFET for deep-sub-tenth micron era,” *IEDM Tech. Dig.*, Dec. 1999, pp. 919–921.

[13] T. Ohtou, N. Sugii, and T. Hiramoto, “Impact of parameter variations and random dopant fluctuations on short-channel fully depleted SOI MOSFETs with extremely thin BOX,” *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 740–742, Aug. 2007.

[14] C. Shin, M. H. Cho, Y. Tsukamoto, B.-Y. Nguyen, B. Nikolić, and T.-J. K. Liu, “SRAM yield enhancement with thin-BOX FD-SOI,” *Proc. IEEE Int. SOI Conf.*, Oct. 2009, pp. 1–2.

[15] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris, “Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications,” *IEDM Tech. Dig.*, Dec. 2009, pp. 1-4.

[16] C. L. Chen, R.T. Chang, P.W. Wyatt, C. K. Chen, D.-R. Yost, J. M. Knecht, and C. L. Keast, “Floating body effects on the RF performance of FDSOI RF amplifiers,” *IEEE International SOI Conference*, Oct. 2005, pp. 44-46.
[17] J. B. Kuo and K.-W. Su, CMOS VLSI Engineering Silicon-on-Insulator (SOI), Kluwer Academic Publishers, 1998.
[18] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Kanakasabapathy, S. Schmitz, A. Reznicek, T. Adam, Y. Zhu, J. Li, J. Faltermeier, T. Furukawa, L. F. Edge, B. Haran, S.-C. Seo, P. Jamison, J. Holt, X. Li, R. Loesing, Z. Zhu, R. Johnson, A. Upham, T. Levin, M. Smalley, J. Herman, M. Di, J.Wang, D. Sadana, P. Kozlowski, H. Bu, B. Doris, and J. O’Neill, “Fully depleted extremely thin SOI technology fabricated by a novel integration scheme featuring implant-free, zero-silicon-loss, and faceted raised source/drain,” *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 212–213.
[19] Sentaurus Process User Guide, Synopsys, Inc., Mountain View, CA, version E-2010.12, Dec. 2010.
[20] Sentaurus Device User Guide, Synopsys, Inc., Mountain View, CA, version D-2010.03, Mar. 2010.
[21] A. Asenov, “Random dopant induced threshold voltage lowering and fluctuations in sub 50 nm MOSFETs: a statistical 3D ‘atomistic’ simulation study,” *IOP Semiconductor Science and Technology*, vol. 10, no. 2, pp. 153-158, Feb. 1999.
[22] A. Asenov, “Simulation of statistical variability in nano MOSFETs,” *VLSI Symp. Tech. Dig.*, Jun. 2007, pp. 86-87.
[23] D. Reid, C. Millar, G. Roy, S. Roy, and A. Asenov, “Analysis of threshold voltage distribution due to random dopants: A 100 000-sample 3-D simulation study,” *IEEE Trans. Electron Devices*, vol. 56, no. 10, pp. 2255-2263, Oct. 2009.
[24] T. Mizuno, J.-I. Okamura, and A. Toriumi, “Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFETs,” *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216-2221, Nov. 1994.
[25] R. W. Keyes, “Physical limits in digital electronics,” *Proc. of the IEEE*, vol. 63, no. 5, pp. 740-767, May 1975.
[26] C. Shin, “Advanced MOSFET Designs and Implications for SRAM Scaling,” Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., University of California, Berkeley, CA, 2011.

Chapter 2
The Characteristics of MOSFET-based Capacitorless DRAM with UTBOX FDSOI Structure

2.1 Introduction

Variability in transistor threshold voltage (V_T) is now widely recognized as a critical challenge for continued CMOS technology scaling and memory yield [1, 2]. The fully depleted silicon-on-insulator (FDSOI) MOSFET design with a very thin (~10 nm-thick) buried oxide (BOX) layer has been shown to be effective for reducing the impact of transistor parameter variations and random dopant fluctuations (RDF), due to its excellent electrostatic integrity and light body doping [1, 3]. The capacitorless DRAM cell design is a candidate for future high-density embedded memories because of its relatively small layout area (as compared to a conventional SRAM cell) and simple fabrication process [4-6]. Back-gated FDSOI capacitorless DRAM devices have recently been demonstrated with sub-50 nm gate length (L_g) [7], and heavy sub-BOX substrate (back gate) doping has been shown to be beneficial for enhanced read margin [8]. In this chapter, the effects of substrate doping concentration and profile on back-gated FDSOI capacitorless DRAM cell performance are investigated via a three-dimensional (3-D) Technology Computer-Aided Design (TCAD) process and device simulation [9, 10] to provide guidance for design optimization.

2.2 Device Structure and Operation

The capacitorless DRAM cell structure in this study is essentially a back-gated FDSOI MOSFET. Based on recent publications (*e.g.,* [3]), cell dimensions at the 22 nm

technology node are selected for this study: the Si body thickness and BOX thickness are each set to be 10 nm, the physical gate length is 25 nm, and the equivalent gate oxide thickness (Tox) is 1 nm. The body is undoped, and the sub-BOX substrate underneath the body is doped p-type. The device parameters are summarized in **Table 2.1**.

Four operations are simulated herein for the capacitorless DRAM cell: Write 1, Write 0, Hold, and Read. To form a potential well within the body for hole storage, a negative back bias of -2.5 V is applied. Holes are generated and stored during a Write 1 operation, or removed during a Write 0 operation, by appropriately biasing the other three terminals of the cell (**Table 2.2**). The state of the cell is read-out via the MOSFET current: if holes are stored in the body, then the source potential barrier (hence V_T) is lowered so that the Read 1 current is high; if holes are not stored in the body, then the Read 0 current is low. The durations of the program/erase and read operations are each 20 nano seconds (ns).

Parameter	Value
Gate length (L_g)	25 nm
Effective gate length (L_{eff})	35.6 nm
Gate oxide thickness (T_{ox})	1 nm
Body thickness (T_{Si})	10 nm
BOX thickness (T_{BOX})	10 nm
Channel width (W)	32 nm
Spacer width (W_{SPACER})	15 nm
Gate work function(Φ_M)	4.45 eV
Channel dopant concentration	Intrinsic
Source/Drain doping concentration	10^{20} cm^{-3}
Substrate dopant concentration	p-type :10^{12} ~ 10^{20} cm^{-3}

Table 2.1. FD-SOI capacitorless DRAM cell design parameters. Extensions are formed by dopant drive-in from in-situ doped raised source/drain to avoid implant damage to transistor [3].

	W1 (program)	W0 (Erase)	Hold	Read
V_{gs} (V)	1.0	0.9	-0.5	0.8
V_{bg} (V)	-2.5	-2.5	-2.5	-2.5
V_{ds} (V)	2.0	-0.5	0	0.6
V_s (V)	0	0	0	0

Table 2.2. FD-SOI capacitorless DRAM cell biasing conditions.

2.3 Optimization of Substrate Doping

2.3.1 Simulation Approach

In capacitorless DRAM, the conventional storage capacitor can be replaced by the body capacitance of a SOI. In this chapter, the basic capacitorless operating mode (MOSFET mode) is focused [11-13]. The concept of MOSFET mode utilizes the floating-body effect of a SOI transistor. In these simulated structures, *Sentaurus Process* is used in order to provide a complete and highly flexible, and process modeling environment [10]. The process parameters follow the 22 nm-technology node with faceted source/drain FDSOI fabrication [14, 15]. The channel and source/drain doping concentrations are the same as each other. Only substrate doping concentrations change.

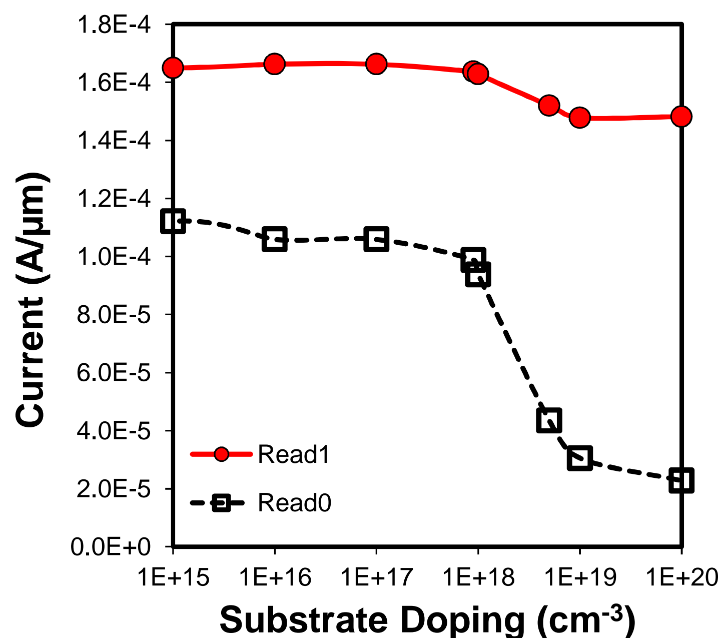


Figure 2.1. Simulated Read 1 and Read 0 currents for a FDSOI capacitorless DRAM cell, as a function of sub-BOX substrate dopant concentration. Read currents are measured at 1μs Hold time.

2.3.2 Substrate Doping Effect

Fig. 2.1 shows the impact of substrate dopant concentration on the Read 0 and the Read 1 current levels. As p-type concentration is increased in the substrate, V_T increases due to increased depletion charge [16] and hence the Read 0 current decreases. The Read 1 current is a much weaker function of substrate doping, due to a compensating effect: as the dopant concentration in the substrate increases, the potential well for holes in the body region becomes deeper so that it can store more holes upon a Write 1 operation (**Fig. 2.2**) – but this results in greater lowering of the source potential barrier so that the net difference in 1-state source potential barrier is relatively small. The sensing margin is defined as the difference between Read 1 and Read 0 currents, and it can be seen to increase with substrate doping, consistent with experimental observations [8].

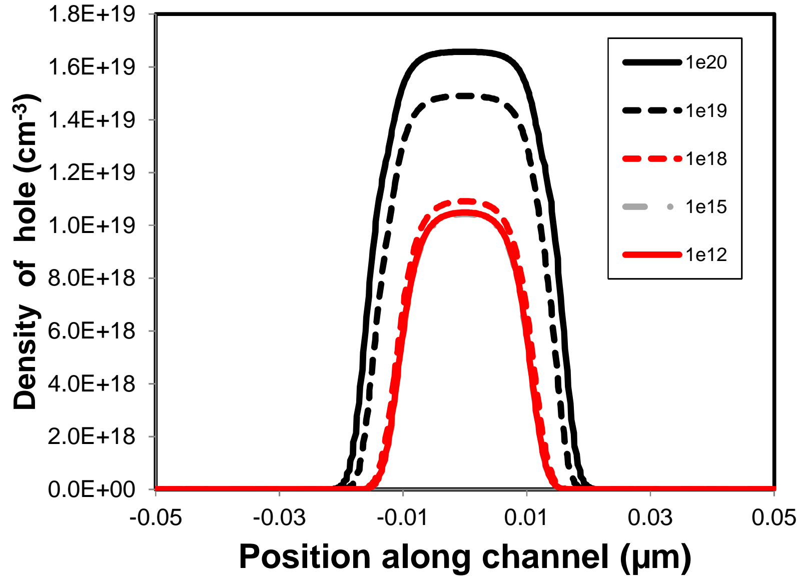


Figure 2.2. Hole density profile within a programmed FDSOI capacitorless DRAM cell in the hold state, for various substrate dopant concentrations (cm^{-3}).

In the hold state, electrons can leak away from the body due to band-to-band tunneling (BTBT), to degrade the cell retention time. This problem is more severe for higher substrate doping due to higher peak electric field at the source/drain junctions (**Fig. 2.3**). **Fig. 2.4** compares the retention characteristics of cells with different substrate doping levels. Negative gate bias and substrate (back gate) bias are applied to hold positive charges in the Hold state as shown in **Table 2.1**. For high substrate doping ($\geq 10^{19}$ cm^{-3}), the sensing margin degrades more rapidly with Hold time even though it is initially higher due to higher BTBT leakage.

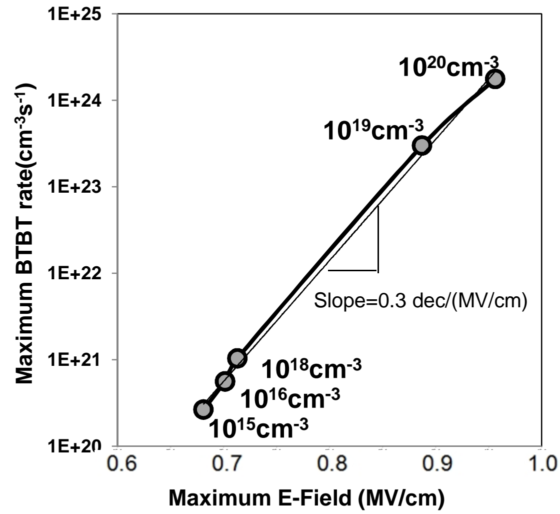


Figure 2.3. Maximum band-to-band tunneling (BTBT) rate *vs.* peak electric field within a programmed FDSOI capacitorless cell in the hold state. The corresponding substrate doping concentrations for various peak electric field strengths are indicated.

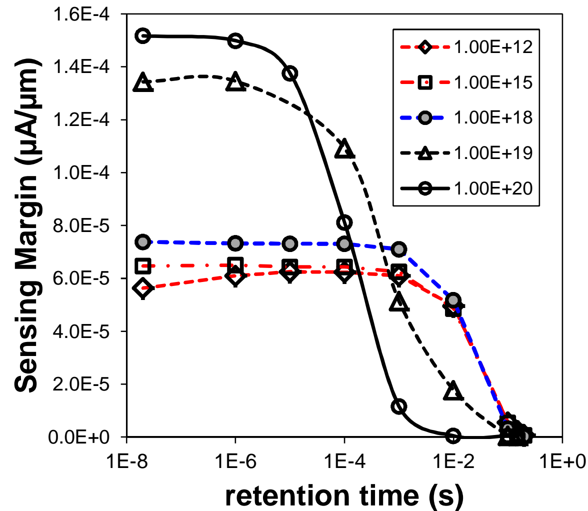


Figure 2.4. Retention characteristics for a FDSOI capacitorless DRAM cell, using various substrate dopant concentrations (cm^{-3}). Although higher substrate doping results in larger current sense margins at short retention times, the retention time is degraded due to increased BTBT.

2.3.3 Random Dopant Fluctuations (RDF)

Another issue for high substrate doping is the V_T variation induced by random dopant fluctuations (RDF), since the substrate doping affects V_T when the BOX is thin [2]. 3-dimension (3-D) Kinetic Monte Carlo (KMC) process simulations [9] were used to

examine the impact of RDF in this work. The simulated process uses low-temperature, zero-silicon-loss epitaxial growth to form faceted *in-situ*-doped (10^{20} cm^{-3}) raised-source/drain regions. Dopants are diffused to form the lightly doped source/drain extensions to reduce series resistance with minimal increase in sidewall gate capacitance [3]. **Fig. 2.5** shows one instance of a simulated structure. In order to distinguish the effect of substrate RDF, all of the simulated structures have the same source and drain atomistic dopant profiles (to eliminate the effects of source/drain RDF).

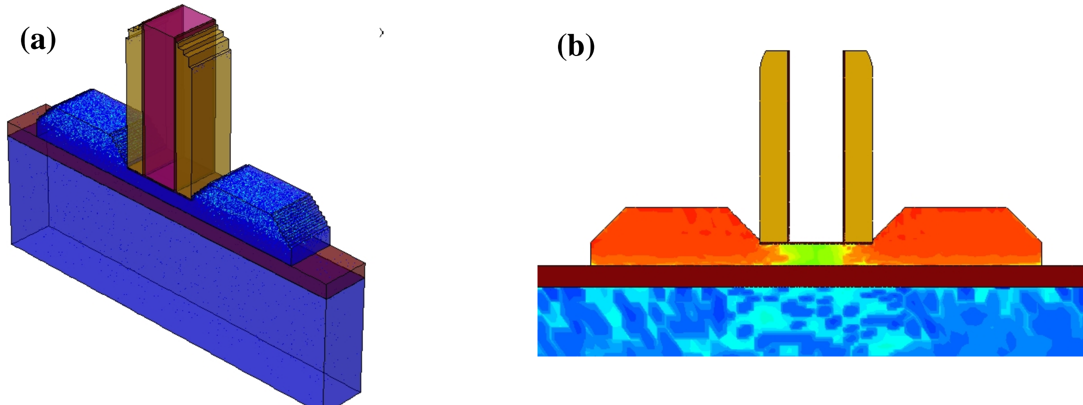


Figure 2.5. Kinetic Monte Carlo (KMC) simulation: (a) FDSOI capacitorless DRAM cell (W = 32 nm) structure showing dopant particle distribution, and (b) cross-sectional doping contour map.

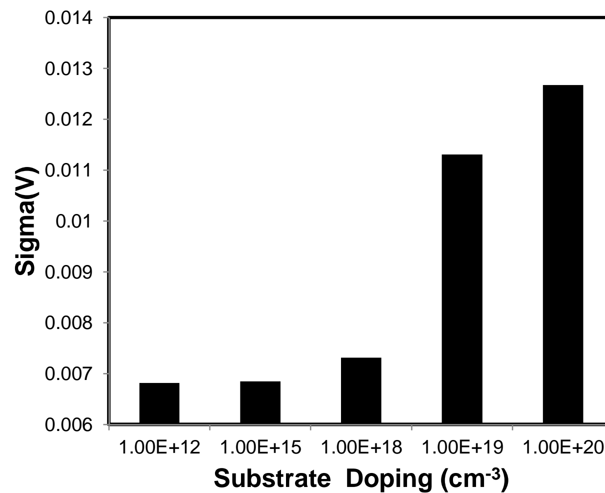


Figure 2.6. Standard deviation of threshold voltage distribution due to RDF-induced variation, for various substrate dopant concentrations.

The standard deviation of the V_T distribution (σ_{VT}) extracted from these simulations (I_{ds}-V_{gs} curves for Read 0 bias conditions), is plotted in **Fig. 2.6**, using various nominal substrate dopant concentrations. Clearly, σ_{VT} becomes significant for substrate doping $\geq 10^{19}$ cm^{-3}. Given the tradeoff between sensing margin and retention time, and RDF-induced V_T variation, the optimal substrate doping appears to be ~10^{18} cm^{-3}.

2.4 Selective Well Design

As noted above, high peak electric fields at the source/drain junctions result in degraded retention time due to BTBT leakage. If the p-type substrate doping is lowered - or even made of the opposite type (n-type) - in the regions directly beneath the source/drain junctions, then this problem can be somewhat mitigated. Therefore, a selective well design is proposed herein to improve the retention behavior of the FDSOI capacitorless DRAM cell: p-type doping is used in the substrate beneath the channel region, while n-type doping (10^{18} cm^{-3}) is used beneath the source and drain regions as shown in **Fig. 2.7**. Such a structure can be formed in a straightforward manner by self-aligned deep ion implantation of n-type dopants. In **Fig. 2.8** the electric field distribution within the SOI film in the Hold 0 state is compared for uniform p-type substrate doping *vs.* selective p-well doping. The peak electric field is reduced for the selective well structure and BTBT leakage is reduced as shown in **Fig. 2.8(b).**

The effect of the width of the selective well is studied via simulation (**Fig. 2.9**). Although a wider p-well is more effective for retaining holes (positive charges), it can result in larger peak electric field, which degrades retention time. An excessively narrow p-well also results in short retention time due to an insufficient well for retaining holes. As is evident in **Fig. 2.10**, the optimal width of the p-well is comparable to the gate length, for which the retention time exceeds 100 ms. This represents a ~9% improvement over the uniform substrate doping case.

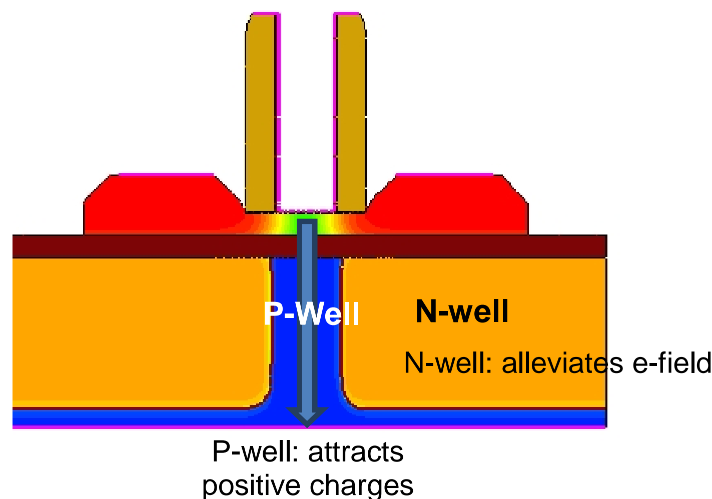


Figure 2.7. Selective well cross section view. The p-well has a role in attracting positive charges. The n-well alleviates the peak electric field at the source/drain junction, which improves retention time.

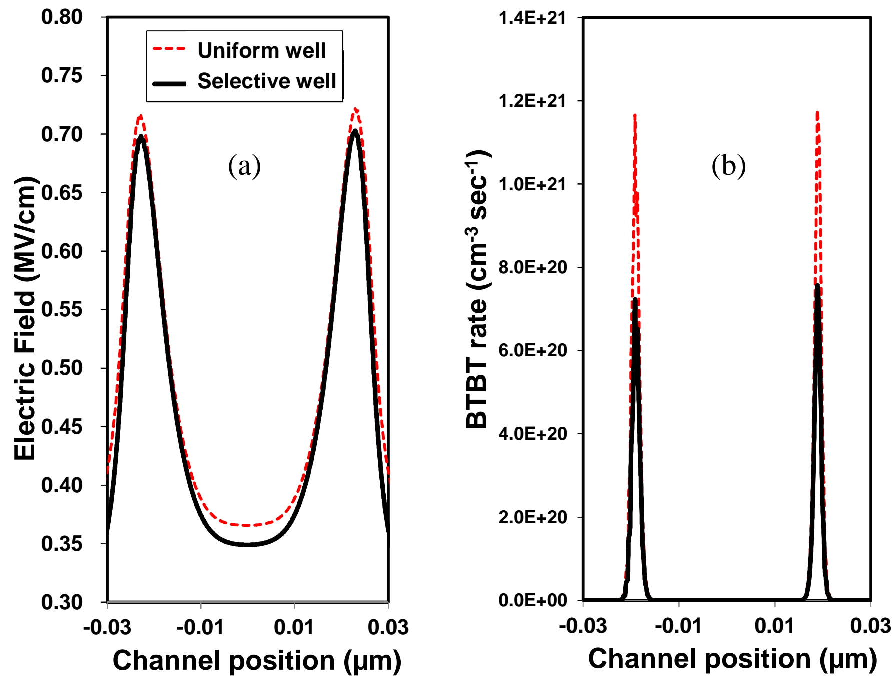


Figure 2.8. (a) Electric field profile and (b) BTBT rate within the SOI film, 1nm above the BOX, in the Hold 0 state. The n-wells are electrically floating within the p-type substrate. The p-type substrate (p-well) is biased at -2.5 V, the source and drain regions are biased at 0V, and the gate is biased at -0.5 V.

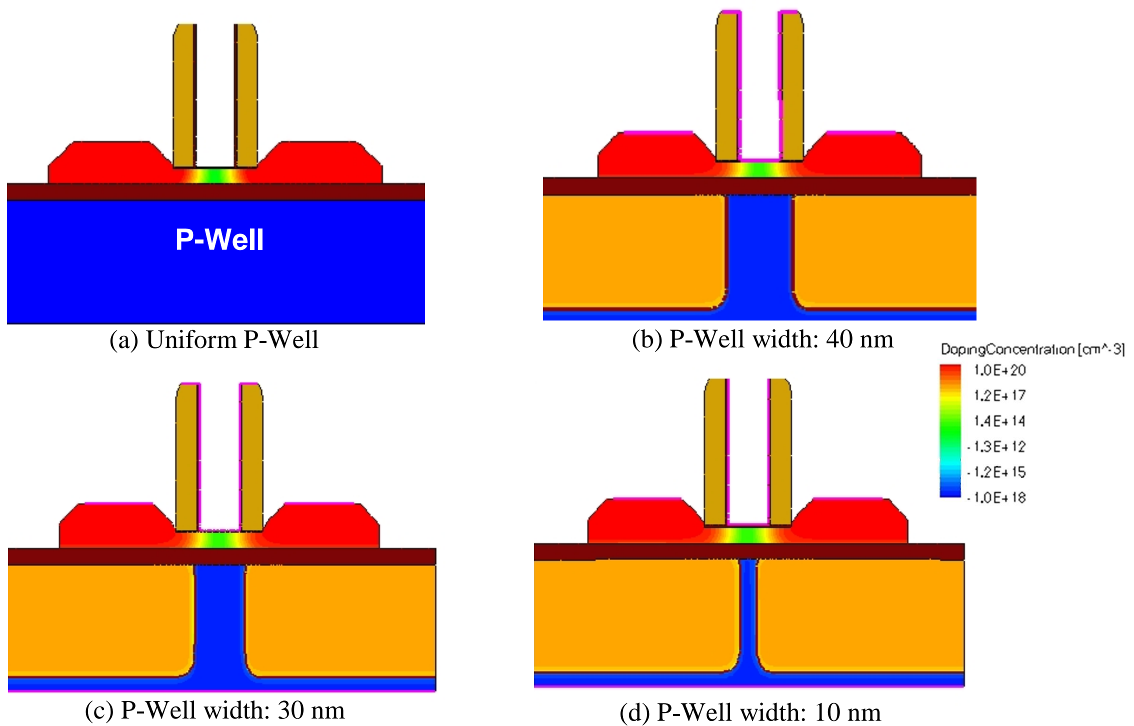


Figure 2.9. Various p-well widths for selective wells.

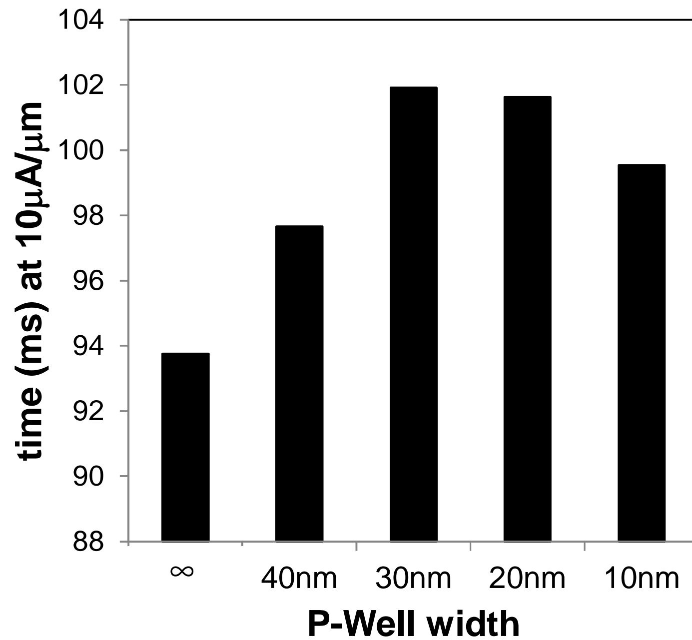


Figure 2.10. Comparison of retention time (for 10 μA/μm minimum sensing margin) for various widths of the p-well centered beneath the channel region.

2.5 Summary

The peak doping concentration and lateral doping profile within the substrate of a FDSOI capacitorless DRAM cell can greatly affect the cell retention time. As the peak doping concentration increases, the sensing current increases but at the cost of reduced retention time due to BTBT and increased V_T variability due to RDF. The optimal peak doping concentration is found to be ~10^{18} cm^{-3}. A selective well structure (the p-well only underneath the channel region) can be used to reduce the peak electric field at the source/drain junctions in order to improve retention time by ~9% for 25 nm gate length.

2.6 References

[1] Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin , F. Boeuf , D. Delprat, K. Bourdelle, B.-Y. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," *IEDM Tech. Dig.,* Dec. 2008, pp. 1-4.

[2] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, " Parameter variations and impact on circuits and microarchitecture," *Proc. Design Autom. Conf.,* 2003, pp. 338–342.

[3] C. Shin, M. H. Cho, Y. Tsukamoto, B.-Y. Nguyen, B. Nikolić, and T.-J. K. Liu, "SRAM yield enhancement with thin-BOX FD-SOI," *Proc. IEEE Int. SOI Conf.*, Oct. 2009, pp. 1–2.

[4] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, " A SOI capacitor-less 1T-DRAM concept," *Proc. IEEE Int'l SOI Conf.*, Oct. 2001, pp. 153-154.

[5] R. Ranica, A. Villaret, C.Fenouillet-Beranger, P. Malinge, P. Mazoyer, P. Masson, D. Delille, C. Charbuillet, P. Candelier and T. Skotnicki, " A capacitor-less DRAM cell on 75nm gate length, 16nm thin Fully Depleted SOI device for high density embedded memories," *IEDM Tech. Dig.,* Dec. 2004, pp. 277–280.

[6] D. Fisch, "Innovative Approach to drive Floating Body Z-RAM® Embedded Memory to 32 nm and beyond, " *Proc. IEEE Int'l SOI Conf.,* Oct. 2007, pp. 101-102.

[7] I. Ban, U. E. Avci, D. L. Kencke, P. Tolchinsky, and P.L.D. Chang, " Integration of Back-Gate Doping for 15-nm Node Floating Body Cell (FBC) Memory," *IEEE Symp. VLSI Tech. Dig.,* Jun. 2010, pp. 159 – 160.

[8] S. Kim, R. J. Tseng, W. Rachmady, B. Jin, U. Shah, I. Ban, U. E. Avci, and P.L.D. Chang, " Silicon on Replacement Insulator (SRI) Floating Body Cell (FBC) Memory," *IEEE Symp. VLSI Tech. Dig.,* Jun. 2010, pp. 165 – 166.

[9] Sentaurus Device User Guide, Synopsys, Inc., Mountain View, CA, version D-2010.03, Mar. 2010.

[10] Sentaurus Process User Guide, Synopsys, Inc., Mountain View, CA, version E-2010.12, Dec. 2010.

[11] H.-J. Wann and C. Hu, "Capacitorless DRAM Cell on SOI Substrate," *IEDM Tech. Dig.*, Dec. 1993, pp. 635 – 638.

[12] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, and E. Faraoni, "New Generation of Z-RAM," *IEDM Tech. Dig.*, Dec. 2007, pp. 925-928.

[13] I. Ban, U. E. Avci, D. I. Kencke, P. L. D. Chang, "Scaled Floating Body Cell (FBC) Memory with High-k+Metal Gate on Thin-Silicon and Thin-BOX for 16-nm Technology Node and Beyond," *VLSI Symp. Circuit Dig.*, Jun. 2008, pp. 92-93.

[14] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Kanakasabapathy, S. Schmitz, A. Reznicek, T. Adam, Y. Zhu, J. Li, J. Faltermeier, T. Furukawa, L. F. Edge, B. Haran, S.-C. Seo, P. Jamison, J. Holt, X. Li, R. Loesing, Z. Zhu, R. Johnson, A. Upham, T. Levin, M. Smalley, J. Herman, M. Di, J.Wang, D. Sadana, P. Kozlowski, H. Bu, B. Doris, and J. O'Neill, "Fully depleted extremely thin SOI technology fabricated by a

novel integration scheme featuring implant-free, zero-silicon-loss, and faceted raised source/drain," *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 212–213.

[15] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris, "Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications," *IEDM Tech. Dig.*, Dec. 2009, pp. 1-4.

[16] J. B. Kuo and K.-W.Su, CMOS VLSI Engineering Silicon-on-Insulator, Kluwer Academic Publishers, 1998.

Chapter 3
Design Optimization of BJT-based Thin-Body Capacitorless DRAM Cell

3.1 Introduction

The concept of a single-transistor dynamic random access memory (DRAM) cell was proposed to address the challenge of reducing memory cell area with reduction in minimum feature size [1]. The bipolar junction transistor (BJT)-based operation (BJT mode) of a thin-body capacitorless DRAM cell is advantageous compared to the metal-oxide-semiconductor field-effect transistor (MOSFET)-based operation (MOSFET mode) because it provides for higher current sensing margin and longer data retention times [2]. However, band-to-band tunneling (BTBT) leakage due to high internal electric field can degrade the retention time in scaled BJT-based cells [3]. Thus, in this chapter, methods for improving the retention time of a scaled BJT mode capacitorless DRAM cell are investigated via technology computer-aided design (TCAD) simulation [4, 5]. Kinetic Monte Carlo (KMC) simulations then are used to compare the effects of random dopant fluctuations (RDF) on the read current distributions of cells designed for the BJT mode *vs*. the MOSFET mode.

3.2 Cell Design and TCAD Simulation

The capacitorless DRAM cell in this study comprises a back-gated thin-body MOSFET. The initial values of various cell design parameters (**Table 3.1**) are selected as appropriate for the 22 nm complementary metal–oxide–semiconductor (CMOS) technology node [6]. The simulated fabrication method uses a low-temperature, zero-silicon-loss epitaxial growth process to form faceted in-situ-doped (10^{20} cm^{-3}) raised-source/drain regions – from which dopants are diffused (at 1473 K for 0.08 s) to form lightly doped source/drain extensions – in order to reduce series resistance with minimal increase in sidewall gate

capacitance. [7]. The Sentaurus software package [4, 5] is used to simulate the various cell operations (*i.e.,* Write, Hold, and Read) at room temperature (300 K), assuming 3 μs minority-carrier lifetime within the body. The operating voltages for BJT mode and MOSFET mode are summarized in **Table 3.2** and **Table 3.3** respectively: W1 denotes the program operation (*i.e.,* writing data 1 into a cell); W0 indicates the erase operation (*i.e.,* writing data 0 into a cell); *Hold* refers to data retention, and *Read* signifies the sensing of stored data. The durations of the Write and Read operations are each 20 ns.

Gate length (nm)	25 or 41
Gate-sidewall spacer width (nm)	13-25
Gate-oxide thickness (nm)	1 or 3
Body thickness (nm)	10
Buried oxide thickness (nm)	10
Body dopant concentration: intrinsic (cm^{-3})	0
Substrate dopant concentration (cm^{-3})	10^{18}
Gate work function (eV)	4.6

Table 3.1. Capacitorless DRAM cell design parameters

	W1	**W0**	**Hold**	**Read**
V_{gs}	-1	0	-1.7	-1
V_{bg}	2.5	2.5	2.5	2.5
V_{ds}	1.7	-0.5	0	1.2
V_s	0	0	0	0

Table 3.2. Operating voltages for BJT mode (unit: Volts).

	W1	**W0**	**Hold**	**Read**
V_{gs}	1	0.9	-0.5	0.8
V_{bg}	-2.5	-2.5	-2.5	-2.5
V_{ds}	2	-0.5	0	0.6
V_s	0	0	0	0

Table 3.3. Operating voltages for MOSFET mode (unit: Volts).

3.3 Mechanism of Data Retention Failure

When a BJT mode cell is in the Hold 1 state, holes are stored below the gate oxide. This increases the vertical electric field (e-field), which is a concern for gate-oxide reliability. **Fig. 3.1** shows Hold state electric field contour maps for a cell with 1 nm gate-oxide thickness (T_{OX}) and 13 nm gate-sidewall spacer width (W_{spacer}). The peak electric field at the gate oxide is almost 16 MV/cm in the Hold 1 state (**Fig. 3.2**). A thicker oxide (3 nm) should be used to guarantee a gate-oxide lifetime of more than 10 years [8]. This is possible because the BJT mode does not require a very thin gate oxide [9].

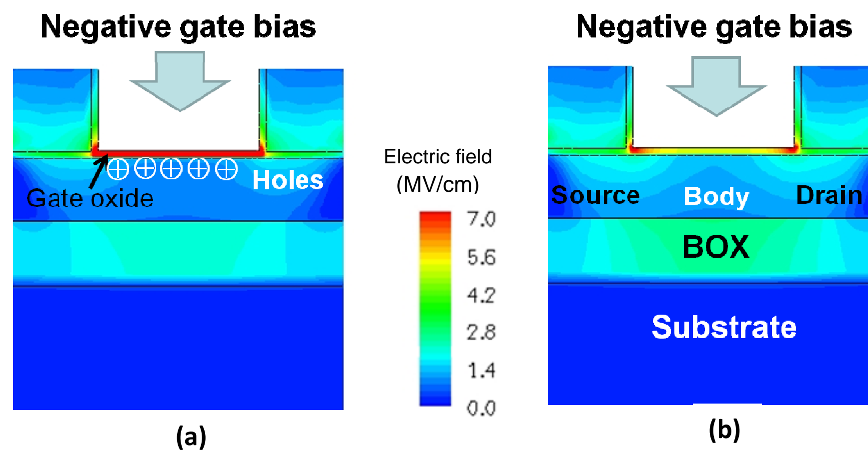


Figure 3.1. Electric field contour maps for a BJT mode cell in the Hold state. W_{spacer} = 13 nm and Tox = 1 nm. (a) Hold 1 state (D1 Hold): When holes are stored in the body, the electric field is relatively high in the gate oxide. (b) Hold 0 state (D0 Hold): When no holes are stored in the body, the electric field is relatively high at the body-source/drain junctions.

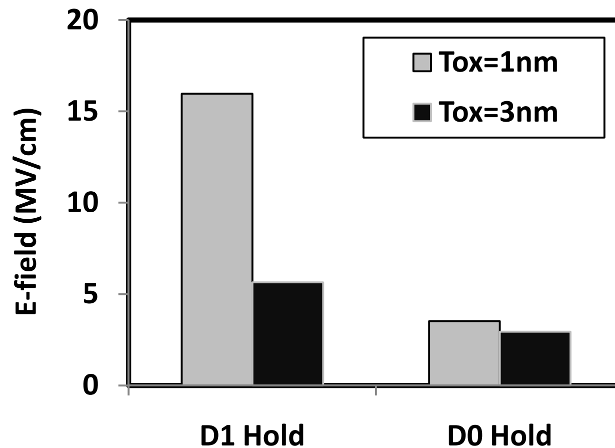


Figure 3.2. Maximum electric field in the gate oxide during a Hold operation. W_{spacer} = 13 nm.

The relationship between the electric field and BTBT is investigated in silicon. The BTBT rate increases exponentially with electric field as shown in **Fig. 3.3.** **Fig. 3.4** shows BTBT contour maps for a BJT mode cell in the Hold 1 and Hold 0 states. A negative bias is applied to the gate in order to retain holes in the Hold state. In the D1 Hold state, the hole density is much higher compared to the D0 Hold state. Positive charges (holes) reduce the potential well depth in the D1 Hold state (**Fig. 3.5 (a)**). The probability of recombination of electrons and holes is low, due to the low peak electric field in the body. In contrast, for a cell in the Hold 0 state, the BTBT at the source/drain junctions is relatively high. When there are very few holes in body (D0 Hold), electrons tunnel through the energy band gap and holes are generated in the body (**Fig. 3.5 (b)**). High electric field induce high BTBT rate, as shown in **Fig. 3.4 (b)**. Due to BTBT, holes are injected into the body so that the Read 0 current increases with Hold duration (**Fig. 3.6**). Thus, the ***D0 failure*** limits the retention time of BJT-based capacitorless DRAM cells.

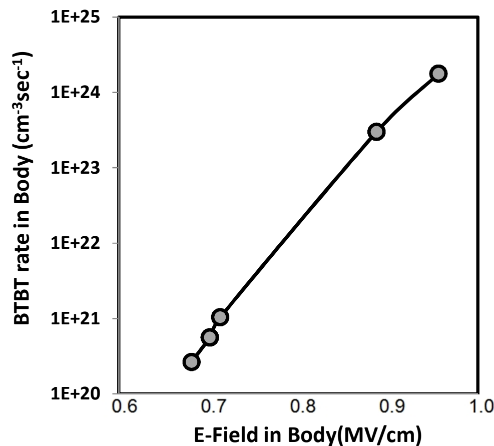


Figure 3.3. Relationship between electric field and BTBT. BTBT rate increases exponentially when measured in relation to the electric field.

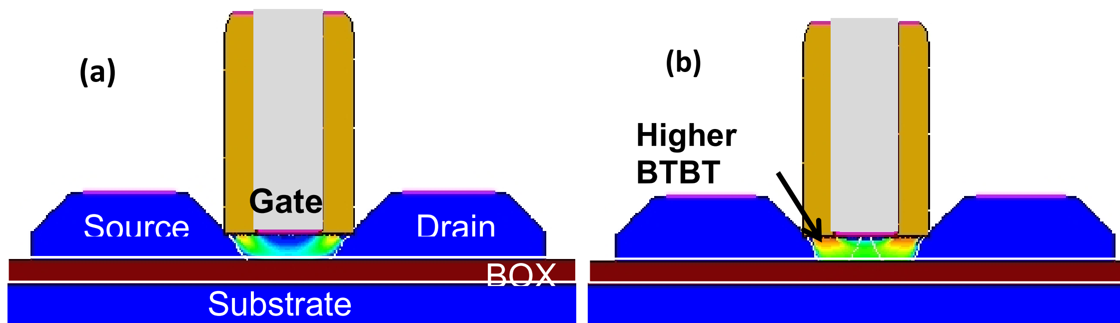


Figure 3.4. Band-to-band tunneling rate contour maps for a cell with W_{spacer} = 13 nm and Tox = 1 nm. (a) Hold 1 state. (b) Hold 0 state. During a Hold 0 operation, there is significant BTBT, which eventually leads to D0 hold failure.

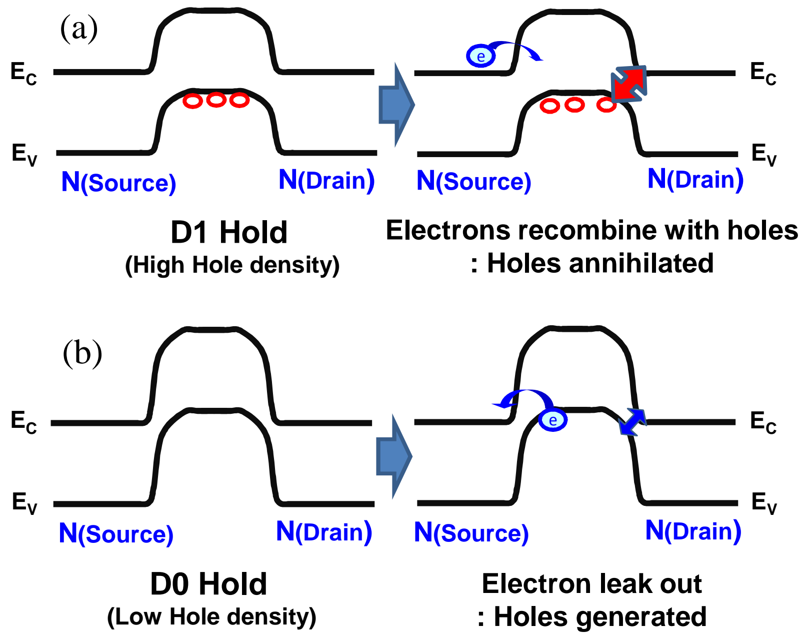


Figure 3.5. Energy band diagrams. (a) D1 Hold state. Red arrow in top right figure indicates wider tunneling distance, which induces low BTBT rate. (b) D0 Hold state. Due to narrow tunneling distance (high electric field), BTBT rate is higher than that of D1 Hold state.

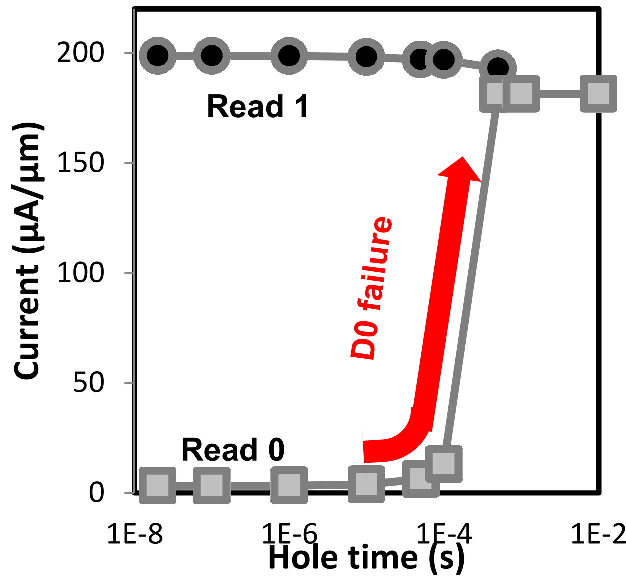


Figure 3.6. Read current *vs.* hold duration, for a cell with W_{spacer} = 13 nm and Tox = 1 nm. D0 hold failure limits the retention time.

3.4 Methods for Improving Retention Time

In order to reduce BTBT in the Hold 0 state, the peak electric field at the source/drain junctions should be reduced. This can be achieved by offsetting the source/drain regions from the edges of the gate electrode, which is achieved by increasing the width of the gate-sidewall spacers. **Fig. 3.7** shows how the peak electric field decreases as the spacer width is increased from 17 nm to 25 nm, and **Fig. 3.8 (a)** illustrates the resulting improvement in Read 0 current. As the width of the spacer is increased, cell programming efficiency degrades (because the impact ionization rate during a Write 1 operation is reduced) so that Read 1 currents decrease, as shown in **Fig. 3.8 (b).** The retention time (*i.e.,* the Hold duration at which the difference between Read 1 and Read 0 currents falls below 60 μA/μm) is maximized for a spacer width of 21 nm (**Figs. 3.8 (c)** and **3.9 (a)**).

Another approach to reducing BTBT in the Hold 0 state is to optimize the front-gate bias voltage. There is tradeoff between charge loss due to thermionic emission in the Hold 1 state (which decreases Read 1 current) for small gate bias and BTBT charge injections in the Hold 0 state (which increases Read 0 current) for large gate bias. Retention time is maximized at a Hold gate bias of -1.6 V (**Fig. 3.9 (b)**). Optimization of the drain bias voltage during the Read operation can provide for larger current sensing margins (**Fig. 3.9 (c)**). A higher Read drain bias provides for larger sensing currents. However, the Read 0 current can increase significantly if the Read drain bias is too high. 1.01 s retention time is projected for the optimized BJT mode capacitorless DRAM cell design and the optimized operating voltages summarized in **Table 3.4**.

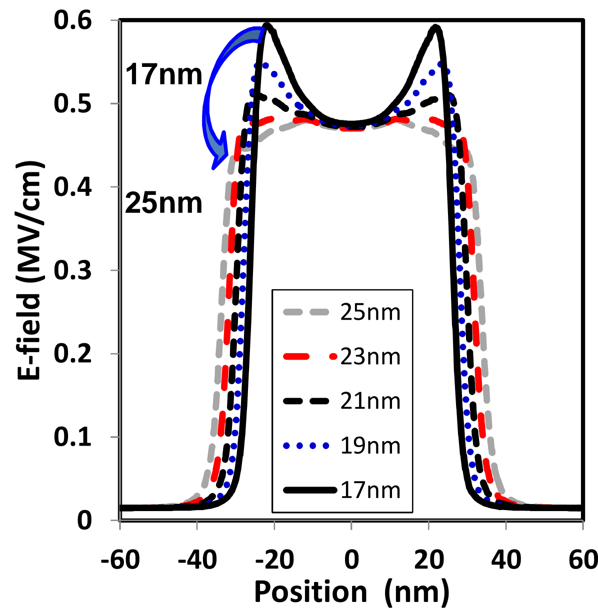
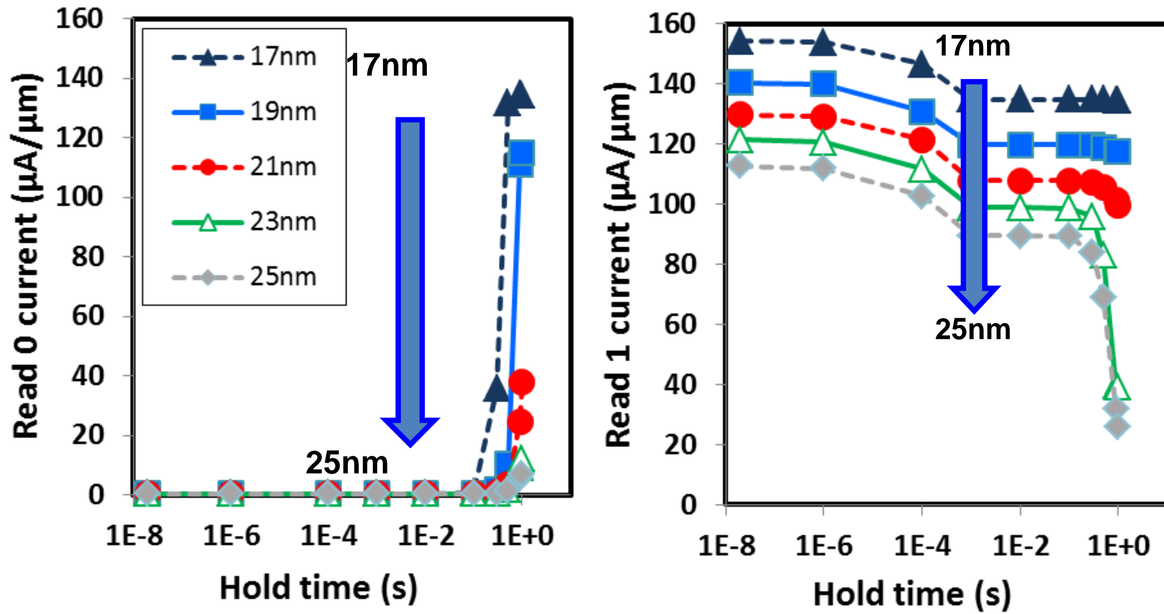
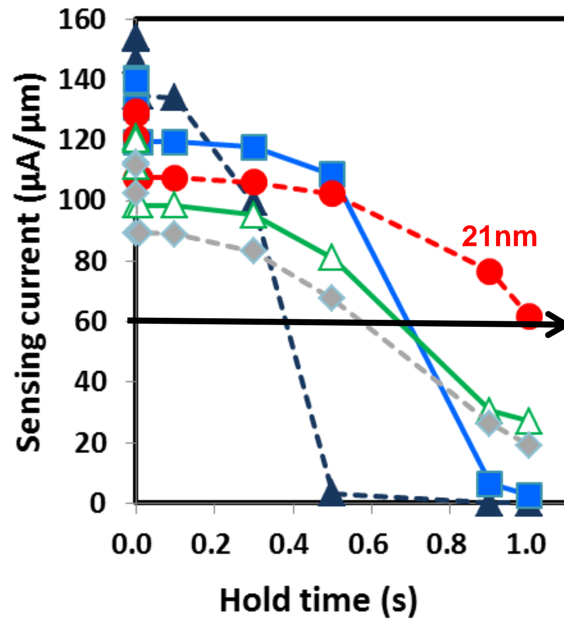


Figure 3.7. Electric field profile within the body (1 nm below the gate oxide), for various widths of the gate-sidewall spacers. Tox = 3 nm.

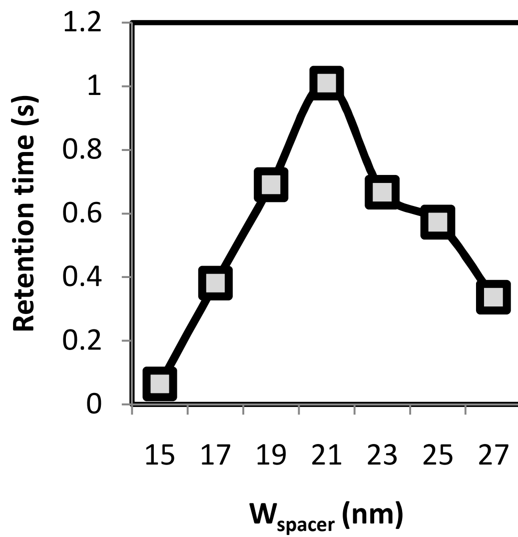


(a) (b)

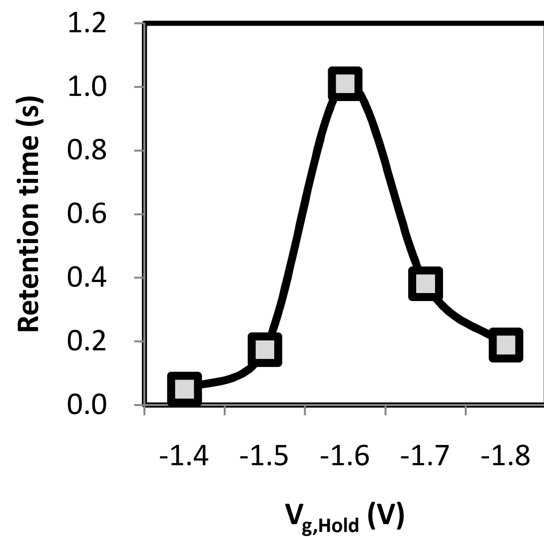


(c)

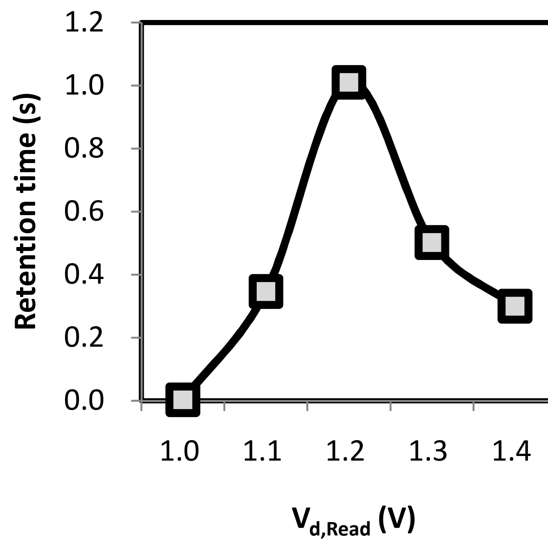
Figure 3.8. Read current *vs.* hold duration for various values of gate-sidewall spacer width. (a) Read 0 current. (b) Read 1 current. (c) Sensing current (Read 1 current – Read 0 current). The horizontal arrow indicates the lower limit (60 μA/μm), which determines the cell retention time.



(a)



(b)



(c)

Figure 3.9. (a) Retention time *vs.* spacer width (W_{spacer}). (b) Retention time *vs.* front-gate bias during Hold operation ($V_{g,Hold}$). (c) Retention time *vs.* drain bias during Read operation ($V_{d,Read}$)

	W1	W0	Hold	Read
V_{gs}	-1	0	-1.6	-1
V_{bg}	2.5	2.5	2.5	2.5
V_{ds}	1.7	-0.5	0	1.2
V_s	0	0	0	0

Table 3.4. Optimized operating conditions for BJT mode (unit: Volts).

3.5 Impact of Random Dopant Fluctuations

Although the impact of RDF-induced performance variations in fully depleted MOSFETs has been studied for static random access memory (SRAM) or logic device applications [6, 10], there have been very few studies on capacitorless DRAM applications [11]. **Fig. 3.10** shows an example of a KMC simulated three-dimensional (3D) cell structure used to assess the impact of RDF in this work. The results of 3D fine-grid statistical device simulations are used together with compact analytical current voltage (I-V) models to predict an RDF-induced performance variation in deep sub-micron devices [12, 13].

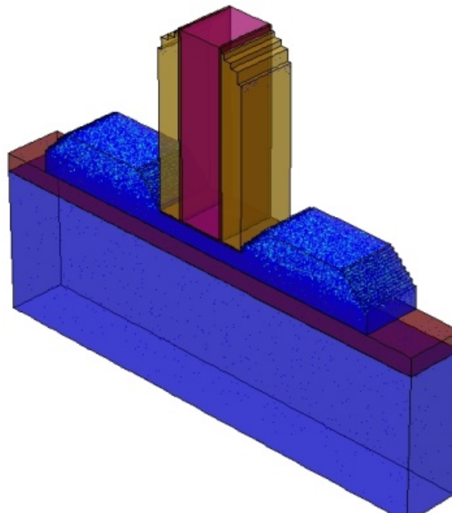


Figure 3.10. 3-dimensional view of a capacitorless DRAM cell with atomistic source/drain doping.

Fig. 3.11 shows examples of KMC-simulated structures for four cell designs: (a) Case A: optimized design for BJT mode (25 nm gate length, 3 nm gate-oxide thickness, and 21 nm-wide gate-sidewall spacers), (b) Case B: longer gate length (41 nm) BJT mode with narrower spacers (13 nm) to compensate for the longer gate length, 3 nm gate-oxide thickness, (c) Case C: optimized design for MOSFET mode (25 nm gate length, 13 nm spacers, and 1 nm gate-oxide thickness), and (d) Case D: MOSFET mode with the same gate length and spacer width as Case B (41 nm and 13 nm, respectively) but with thin gate oxide (1 nm). Read 1 and Read 0 current distributions at 1 μs Hold duration are compared in **Fig. 3.12**.

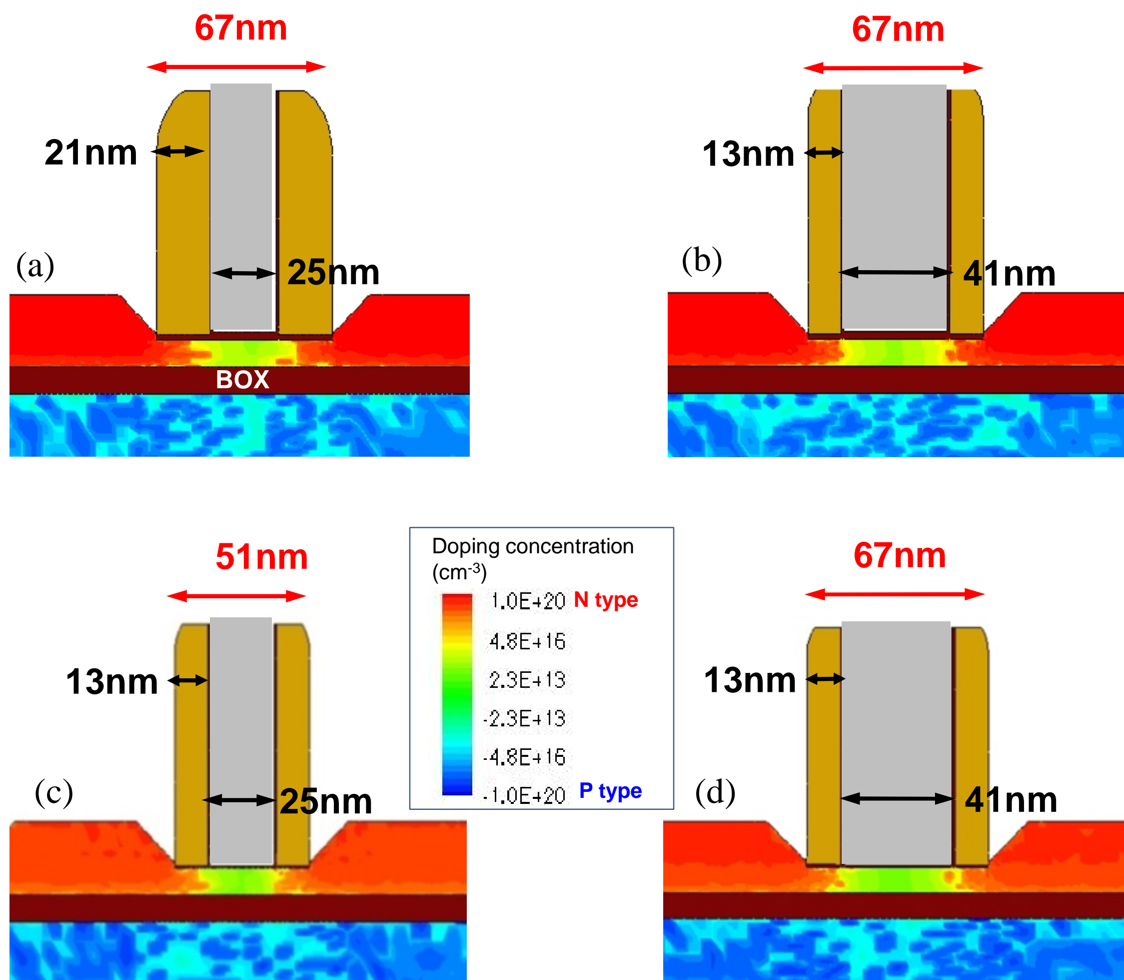
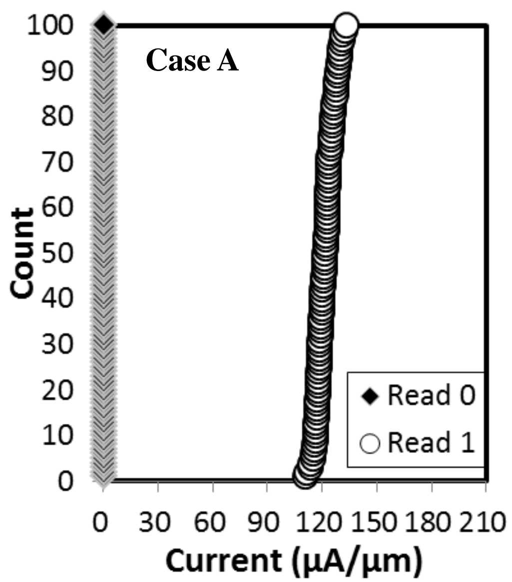
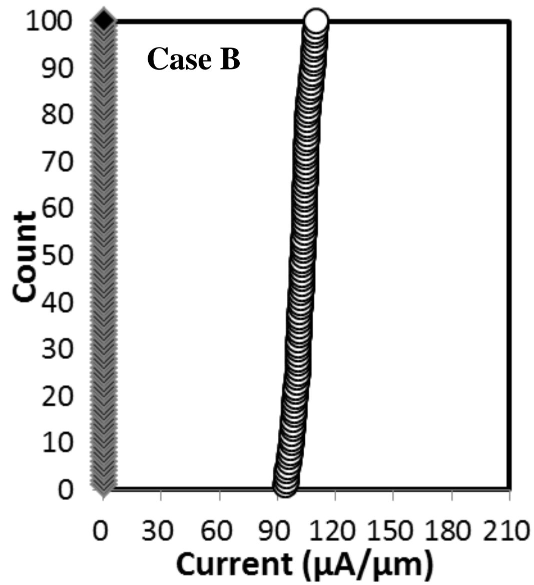


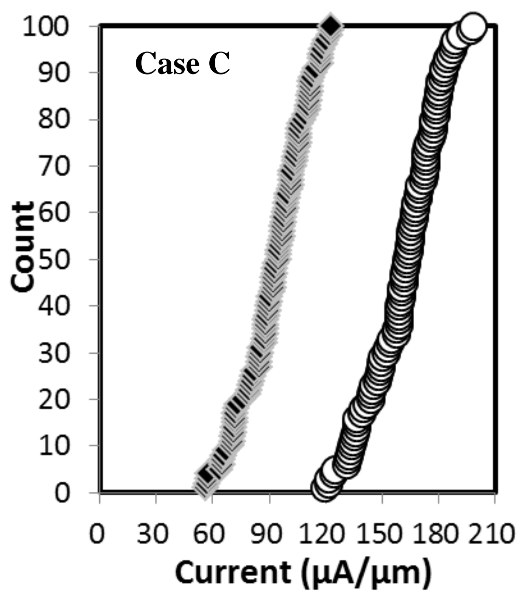
Figure 3.11. Capacitorless DRAM cell designs used for KMC simulations: (a) Case A: Optimized BJT mode design (L_g = 25 nm, W_{spacer} = 21 nm, T_{OX} = 3 nm), (b) Case B: Longer- L_g BJT mode design (L_g = 41 nm, W_{spacer} = 13 nm, T_{OX} = 3 nm), (c) Case C: Optimized MOSFET mode design (L_g = 25 nm, W_{spacer} = 13 nm, and Tox = 1 nm), (d) Case D: Longer- L_g MOSFET mode design (L_g = 41 nm, W_{spacer} = 13 nm, and T_{OX}= 1 nm).



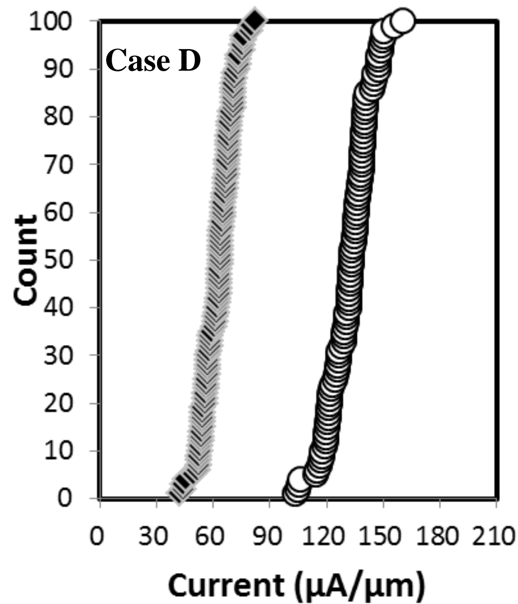
(a)



(b)



(c)



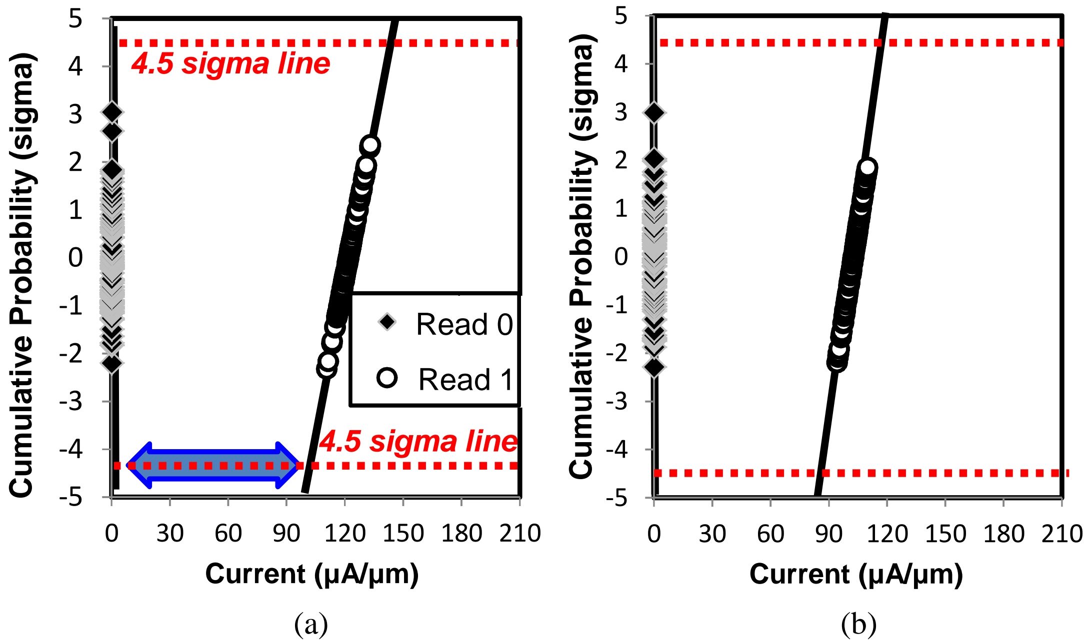
(d)

Figure 3.12. Read 1 and Read 0 current distributions at 1μs Hold duration. (a) Case A, (b) Case B, (c) Case C, and (d) Case D.

Matsuoka et al. introduced the signal sense margin (SSM) metric, based on measured variation data [14], which is defined as:

$$(SSM)_{Icell} = <\Delta I_{cell}> - 4.5 \times (\sigma_{Read0} + \sigma_{Read1}) \quad (1)$$

where $<\Delta I_{cell}>$ is the average sensing margin (the difference between Read 1 and Read 0 currents), σ_{Read0} is the standard deviation for Read 0 currents, and σ_{Read1} is the standard deviation for Read 1 currents. The factor 4.5 is appropriate if 64 redundancy cells are used for a 16 Mb array. SSM > 0 is desirable. The Read current distributions are converted into normal probability plots to more clearly illustrate SSM in **Fig. 3.13**. The difference between the Read 1 current at 4.5 sigma below its mean and the Read 0 current at 4.5 sigma above its mean is the SSM. SSM is much larger for the optimized BJT-based capacitorless DRAM cell design because σ_{Read0} is small (< 3 nA/μm) and the BJT operation is less sensitive to RDF (The BJT current flows through a larger volume (the entire body region) as compared to the MOSFET current which flows through an inversion layer at the surface of the body region). From **Figs. 3.13 (c)** and **3.13 (d),** it can be seen that SSM < 0 for the MOSFET mode cell designs at 1 μs Hold duration. The retention behavior of the four cell designs are compared in **Fig. 3.14**; their retention times and SSM values are summarized in **Table 3.5**. For narrow gate-sidewall spacer width (13 nm), the retention time is short (< 10 ms), regardless of the cell operation mode or gate length. The optimized BJT mode cell design shows the best retention behavior, with a nominal retention time of 1.01 s. Accounting for RDF-induced variations, SSM is projected to fall below zero at a hold duration of 0.6 s. This result indicates that RDF-induced variations effectively reduce the retention time by approximately 40%.



(a) (b)

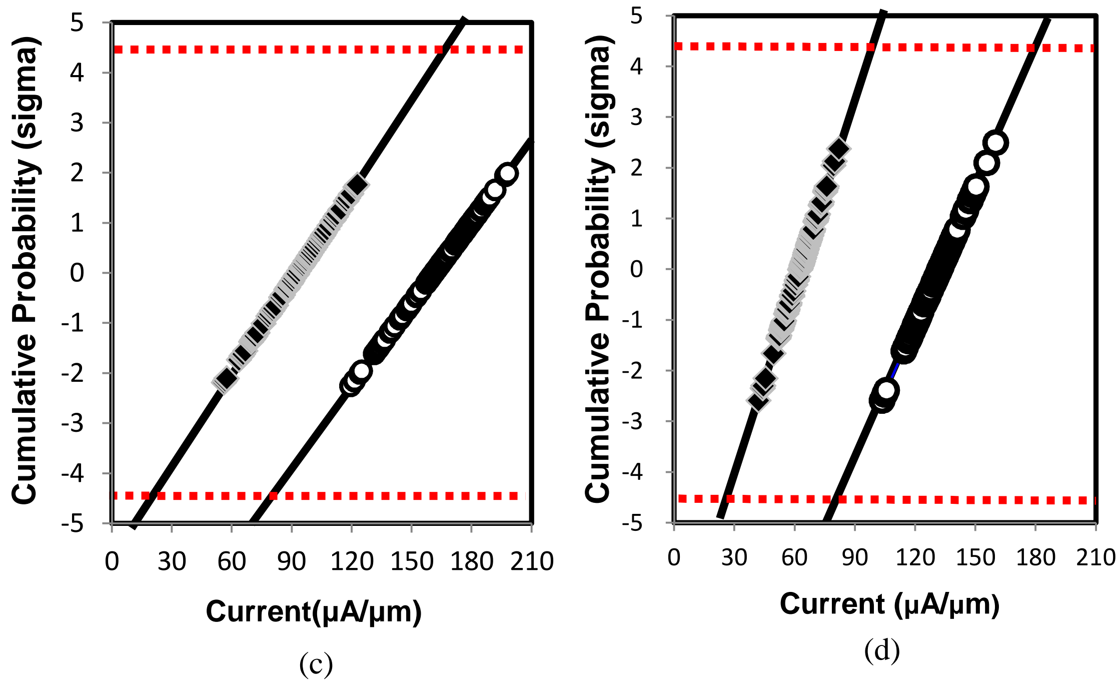


Figure 3.13. Normal probability plots for Read 1 and Read 0 currents at 1μs Hold duration. (a) Case A, (b) Case B, (c) Case C, and (d) Case D. The arrow in (a) indicates the SSM.

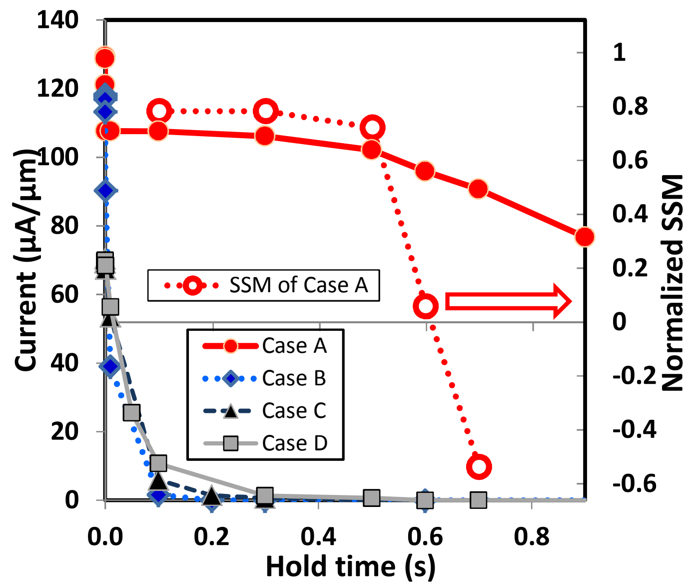


Figure 3.14. Comparison of retention characteristics (Sensing current *vs.* Hold duration) for the four capacitorless DRAM cell designs in Fig. 3.11. Wider gate-sidewall spacers are more effective than longer gate length for improving retention time. The right y-axis indicates normalized SSM for the best cell design (Case A), which drops below zero after 0.6 s.

Case	SSM at 1μs hold duration (μA/μm)	Nominal retention time (ms)
A	107.4	1010
B	100.4	6.3
C	-91.3	5.8
D	-18.8	7.3

Table 3.5. Summary of RDF simulation results.

3.6 Summary

A relatively thick gate oxide (*e.g.,* 3 nm) should be used in a BJT-based capacitorless DRAM to mitigate gate oxide reliability issues. Band-to-band tunneling in the Hold 0 state limits data retention time. By optimizing the *underlap* between the front gate and the source/drain regions as well as the operating voltages, retention time exceeding 1 second should be attainable for a cell with 25 nm gate length. The current sense margin for the optimized BJT-based capacitorless DRAM cell design is relatively large, because random-dopant-fluctuation-induced variations in Read 0 current are negligible.

3.7 References

[1] S. Okhonin, M. Nagoga, J. M. Sallese, and P. Fazan, "A SOI capacitor-less 1T-DRAM concept," *IEEE International SOI Conference*, Oct. 2001, pp. 153–154.

[2] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni, "New Generation of Z-RAM", *IEDM Technical Dig.*, Dec. 2007, pp. 925-928.

[3] K.-W. Song, H. Jeong, J.-W. Lee, S. I. Hong, N.-K. Tak, Y.-T. Kim, Y. L. Choi, H. S. Joo, S. H. Kim, H. J. Song, Y. C. Oh, W.-S. Kim, Y.-T. Lee, K. Oh, and C. Kim, "55 nm capacitor-less 1T DRAM cell transistor with non-overlap structure," *IEDM Technical Dig.*, Dec. 2008, pp. 1-4.

[4] Sentaurus Process User Guide, Synopsys, Inc., Mountain View, CA, version E-2010.12, Dec. 2010.

[5] Sentaurus Device User Guide, Synopsys, Inc., Mountain View, CA, version D-2010.03, Mar. 2010.

[6] C. Shin, M. H. Cho, Y. Tsukamoto, B.-Y. Nguyen, B. Nikolić, and T.-J. K. Liu, "SRAM yield enhancement with thin-BOX FD-SOI," *Proc. IEEE Int. SOI Conf.*, Oct. 2009, pp. 1–2.

[7] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Kanakasabapathy, S. Schmitz, A. Reznicek, T. Adam, Y. Zhu, J. Li, J. Faltermeier, T. Furukawa, L. F. Edge, B. Haran, S.-C. Seo, P. Jamison, J. Holt, X. Li, R. Loesing, Z. Zhu, R. Johnson, A. Upham, T. Levin, M. Smalley, J. Herman, M. Di, J.Wang, D. Sadana, P. Kozlowski, H. Bu, B. Doris, and J. O'Neill, "Fully depleted extremely thin SOI technology fabricated by a novel integration scheme featuring implant-free, zero-silicon-loss, and faceted raised source/drain," *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 212–213.

[8] E. Wu, W. Lai, M. Khare, J. Sune, L.-K. Han, J. McKenna, R. Bolam, D. Harmon, and A. Strong, "Polarity-dependent oxide BD of NFET devices for ultra-thin gate oxide," in *Proc. IEEE IRPS*, 2002, pp. 60–72.

[9] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, W. Schwarzenbach, O. Bonnin, K. K.Bourdelle, B.-Y. Nguyen, C. Mazure, L. Altimime, and M. Jurczak, "A Novel Low-Voltage Biasing Scheme for Double Gate FBC Achieving 5s Retention and 10^{16} Endurance at 85℃," *IEDM Tech. Dig.*, Dec. 2010, pp. 12.3.1-4.

[10] A. Asenov, S. Roy, R. A. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M. F. Bukhori, X. Wang, and U. Kovac, "Advanced simulation of statistical variability and reliability in nano CMOS transistors," *IEDM Tech. Dig.*, Dec. 2008, pp. 1-4.

[11] H. Furuhashi, T. Shino, T. Ohsawa, F. Matsuoka, T. Higashi, Y. Minami, H. Nakajima, K. Fujita, R. Fukuda, T. Hamamoto, and A Nitayama, "Scaling scenario of floating body cell (FBC) suppressing Vth variation due to random dopant fluctuation," *Proc. IEEE Int. SOI Conf.*, Oct. 2008, pp. 33-34.

[12] C. Shin, "Advanced MOSFET Designs and Implications for SRAM Scaling," Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., University of California, Berkeley, CA, 2011.

[13] C. Shin, A. Carlson, X. Sun, K. Jeon, and T.-J. K. Liu, "Tri-gate bulk MOSFET design f or improved robustness to random dopant fluctuations," *IEEE Silicon Nanoelectronics Workshop*, Jun. 2008, pp. S1150.
[14] F. Matsuoka, T. Ohsawa, I. Higashi, H. Furuhashi, K. Hatsuda, K. Fujita, R. Fukuda, N. Ikumi, T. Shino, Y. Minami, H. Nakajima, T. Hamamoto, A. Nitayama, and Y. Watanabe, "FBC's Potential of 6F2 Single Cell Operation in Multi-Gbit Memories Confirmed by a Newly Developed Method for Measuring Signal Sense Margin," *IEDM Tech. Dig.,* 2007, p. 39.

Chapter 4

Implications of Variation

4.1 Introduction

The thin-body silicon-on-insulator (SOI) MOSFET with a very thin (~10 nm-thick) buried oxide (BOX) layer has been shown to be an advantageous transistor design for reducing the impact of dimensional variations and random dopant fluctuations (RDF), because of its excellent electrostatic integrity and light body doping [1]. Although the implications of these variations in thin-body SOI MOSFETs have been studied for SRAM applications [1], there have been very few studies for capacitorless DRAM applications [2, 3]. In this chapter, the implications of process-induced variations for back-gated thin-body SOI capacitorless DRAM data retention time and sensing current are investigated via device simulations [4, 5].

4.2 Device Structure and Operation

The capacitorless DRAM cell structure comprises a back-gated thin-body SOI MOSFET. In this study, cell dimensions appropriate for the 22 nm CMOS technology node are selected, based on recent publications (*e.g.* [1]). The Si body thickness and BOX thickness are each 10 nm, the channel width is 50 nm, and the physical gate length is 25 nm. The equivalent gate oxide thickness is 3 nm and the gate-sidewall spacer width is 21 nm, as previously found to be optimal for the bipolar junction transistor mode operation (BJT mode) [3]. The BJT mode of operation provides for larger sensing margins and longer retention characteristics [6]. The structure is fabricated using an implantation-free process

to avoid dopant straggling and damage-induced defects in the thin body region [1]. The undoped body reduces RDF-induced variations. The sub-BOX substrate is doped p-type (10^{18} cm^{-3}).

Sentaurus (version 2010.03) [4, 5] is used to simulate basic cell operations (Write, Hold, and Read) at room temperature. The applied voltages for the BJT-mode operation are shown in **Table 4.1**.

	W1	W0	Hold	Read
V_{gs}	-1	0	-1.7	-1
V_{bg}	2.5	2.5	2.5	2.5
V_{ds}	1.7	-0.5	0	1.2
V_s	0	0	0	0

Table 4.1. Capacitorless DRAM cell operating voltages (Volts). W1 (Write 1: Programing), W0 (Write 0: Erasing), Hold, and Read.

4.3 Sources of Variation

In order to estimate the impact of dimensional parameter variations on capacitorless DRAM performance, appropriate values of standard deviations in front gate oxide thickness (T_{OX}), body thickness (T_{Si}), buried oxide thickness (T_{BOX}), and spacer width (W_{Spacer}) are selected from previous reports [7-9] (**Figs. 4.1** and **4.2**). These are summarized in **Table 4.2**. Each parameter is assumed to have a normal distribution, and ±4.5 sigma is the variation limit (appropriate for 16 Mb array units, each with 64-cell redundancy [10]). Random dopant fluctuation (RDF) effects are investigated via Kinetic Monte Carlo (KMC) TCAD simulation.

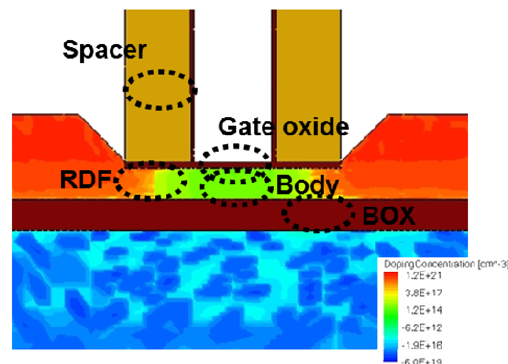


Figure 4.1. Doping contour map showing variation Factors. Spacer width (W_{spacer}), Gate oxide thickness (T_{OX}), Body thickness (T_{Si}), BOX thickness (T_{BOX}), and Random Dopant Fluctuations are considered.

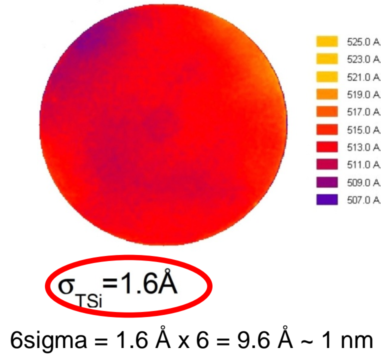


Figure 4.2. Measured SOI film thickness across a wafer [8].

Item	T_{Si}	T_{BOX}	T_{OX}	W_{Spacer}
Median	10 nm	10 nm	3 nm	21 nm
Sigma	1σ=1.6 Å	1σ=1.6 Å	1σ=0.4 Å	1σ= 3.5 Å
Reference	[7, 8]	[7, 9]	[7]	3σ = 5%
LL (-4.5σ)	9.28 nm	9.28 nm	2.82 nm	19.43 nm
UL (+4.5σ)	10.72 nm	10.72 nm	3.18 nm	22.58 nm

Table 4.1. Parameter variations are considered. Upper limit of 4.5 σ (UL) and lower limit of -4.5 σ (LL) are summarized.

4.4 RDF effect

The thin body SOI transistor has excellent immunity to variation compared to partially depleted SOI or bulk transistors [1], which is one of the main reasons for choice of thin body SOI structure in this study. However, retention characteristics in thin body SOI capacitorless DRAM can be affected by RDF, as shown in **Fig. 4.3**. RDF results in variation of the threshold voltage (V_T) as well as variation in the impact ionization rate during the Write 1 operation and thereby affects the Read 1 current [2]. Hole generation in the body region due to band-to-band tunneling leakage (BTBT) is significant in the Hold 0 state for the BJT-mode operation [3], which causes the Read 0 current to increase with Hold time. RDF also affects local electric fields (*i.e.* BTBT) which, in turn, induce retention time variation.

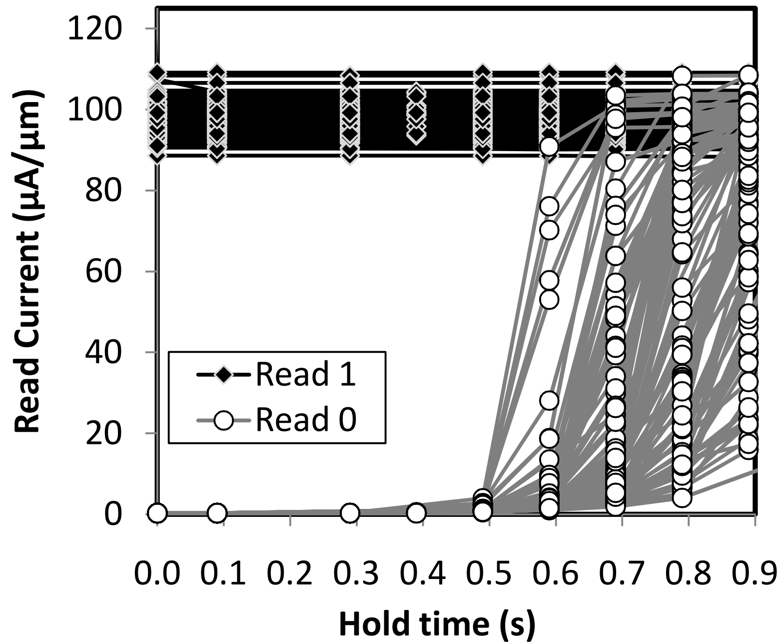


Figure 4.3. Simulated retention characteristics showing the impact of RDF. 100 cases are simulated using the KMC method.

4.5 Dimension Variation Effects

Fig. 4.4 shows how 1-sigma variations in the dimensional parameters independently contribute to the standard deviation in Read current as a function of the Hold time. (The effect of a 1-sigma change in a parameter is assumed to be independent of the values of the other parameters.) Significantly, the Read 1 current is most sensitive to body thickness variation, as shown in **Fig. 4.4 (a)**. A reduction in body thickness results in reduced impact ionization during the Write 1 operation so that fewer holes are stored in the Hold 1 state [11]. Thus, there is a design tradeoff between improved immunity to other sources of variation and reduced current sensing margins. (Note that the effect of RDF on the Read 1 current is relatively suppressed due to the thin body design.) It can be seen in **Fig. 4.4 (b)** that the variation in the Read 0 current is negligible until the Hold time reaches 0.5 s, after which it increases more rapidly than the variation in the Read 1 current.

It is interesting to note that Read currents of BJT mode capacitorless DRAM are more sensitive to variation in the buried oxide thickness than to variation in the front gate oxide thickness, as shown in **Fig. 4.4 (a)**. **Fig. 4.5** shows band diagrams at 1 nm below the gate oxide at the Read 0 state. The BOX induces larger band diagram deviation compared to the

front gate oxide. There are two explanations for this: First, the larger magnitude of variation in T_{BOX} results in larger variation in the potential drop across the buried oxide layer and hence, larger variation in the body potential. Second, since holes accumulate in the body at the front gate oxide interface, an increase in hole concentration during the Hold operation due to a reduction in T_{OX} compensates for (*i.e.* shields against) the increased electric field across the front gate oxide, so that there is reduced impact on the body potential; holes do not shield against changes in the electric field across the back gate oxide.

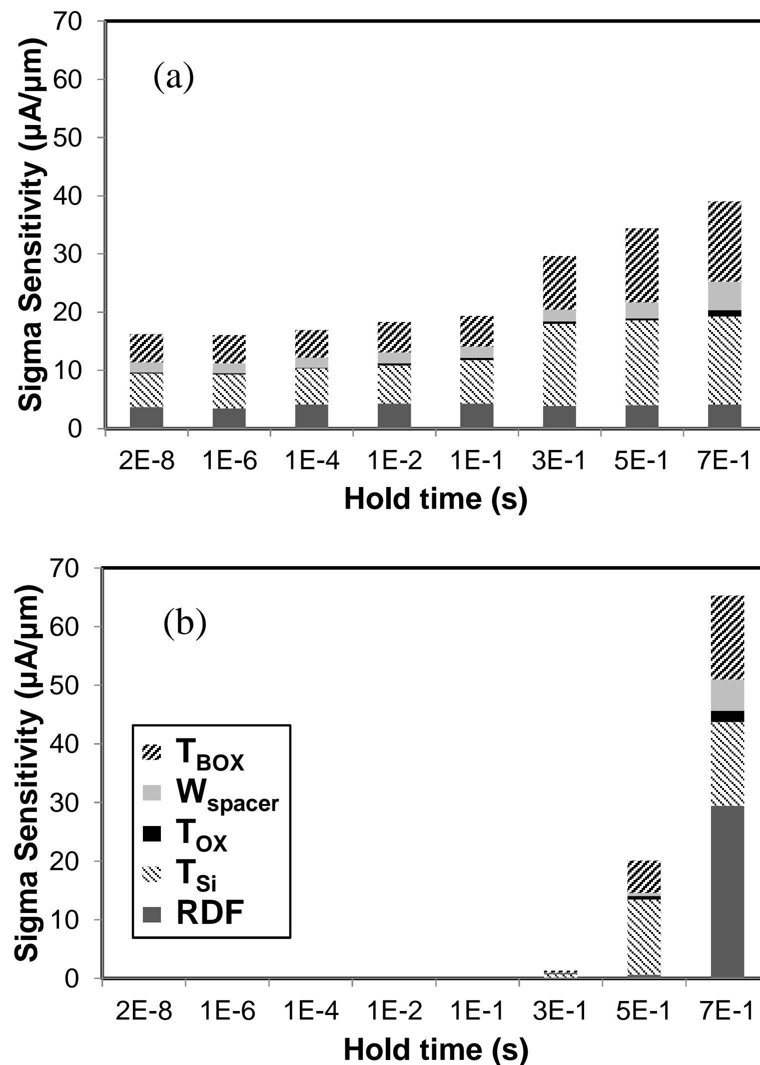


Figure 4.4. Sigma sensitivity plots for capacitorless DRAM read current. The impact of 1-sigma variation is shown for each parameter, along with the impact of RDF, as a function of the data Hold time. (a) Read 1 and (b) Read 0.

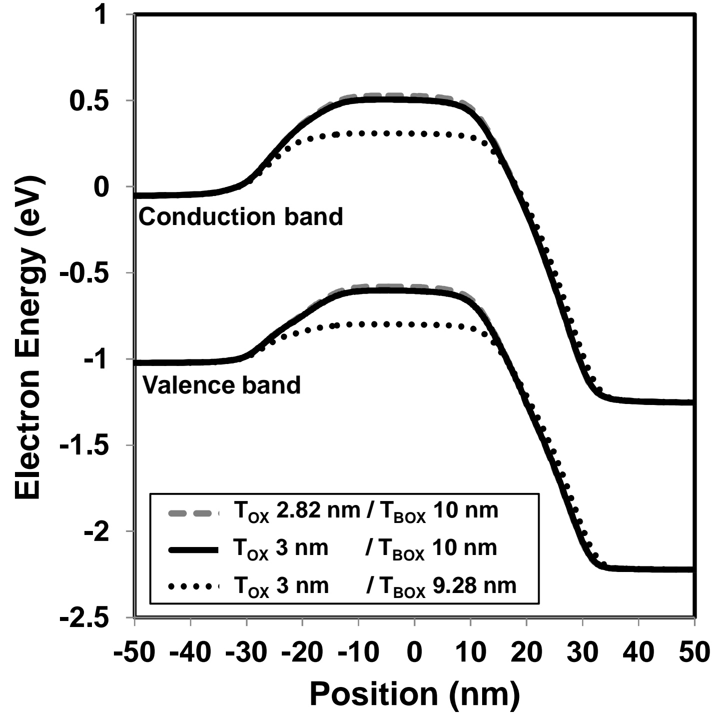


Figure 4.5. Band diagrams 1nm below gate oxide at the Read 0 state. (0.7 s Hold duration time). Reference structure has T_{OX} =3 nm and T_{BOX} =10 nm.

Matsuoka *et al*. introduced a signal sense margin (SSM) metric, based on measured variation data [10]. SSM is defined as:

$$Signal\ Sensing\ Margin\ (SSM) = < \Delta I_{sensing} > - \alpha \times (\sigma_{Read\ 0} + \sigma_{Read\ 1}) \quad (1)$$

where, $<\Delta I_{sensing}>$ is an average sensing margin (*i.e.* Read 1 – Read 0), and α is a factor equal to 4.5 for a 16 Mb array with 64 cell redundancies to yield (corresponding to SSM > 0). Under the assumptions that each dimensional parameter has a Gaussian distribution and its impact is independent of the other parameter values, the standard deviation in Read current due to all sources is calculated as follows [12]:

$$\sigma_{Read\ 0} \approx \sqrt{\begin{array}{c}(\sigma_{Read\ 0,RDF})^2 + (\sigma_{Read\ 0,T_{OX}})^2 + (\sigma_{Read\ 0,T_{Si}})^2 \\ +(\sigma_{Read\ 0,T_{BOX}})^2 + (\sigma_{Read\ 0,W_{Spacer}})^2\end{array}} \quad (2)$$

$$\sigma_{Read\ 1} \approx \sqrt{\begin{array}{c}\left(\sigma_{Read\ 1,RDF}\right)^2 + \left(\sigma_{Read\ 1,T_{OX}}\right)^2 + \left(\sigma_{Read\ 1,T_{Si}}\right)^2 \\ +\left(\sigma_{Read\ 1,T_{BOX}}\right)^2 + \left(\sigma_{Read\ 1,W_{Spacer}}\right)^2\end{array}} \quad (3)$$

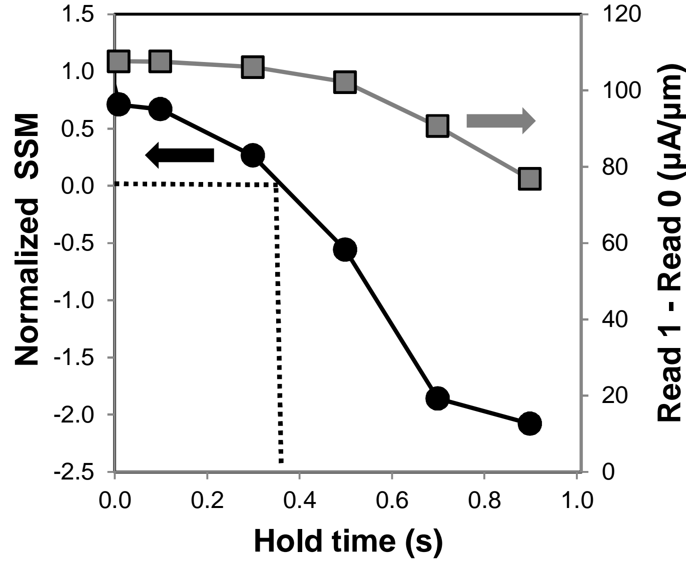


Figure 4.6. Signal sense margin (SSM) and median sensing current (Read 1 current – Read 0 current) as a function of data Hold time. Due to variations, the data retention time (corresponding to 0 SSM – ref. black dot lines) is reduced from 1.01 s to 0.364 s.

Fig. 4.6 shows how SSM decreases with increasing Hold time, falling below 0 at 0.364 s. Considering that the median sensing current falls below the minimum acceptable value of 60 μA/um (3 μA for 50 nm width [13, 14]), at 1.01 s, this result indicates that process-induced variations effectively reduce the retention time by approximately 63%, which is less dramatic than for a conventional DRAM cell design [15]. This can be attributed to the use of an undoped body, which results in reduced impact of RDF, and defect-free source/drain regions underlapped by the gate electrode. This results in very low gate-induced drain leakage current.

4.6 Summary

The read current of a back-gated thin-body capacitorless DRAM cell operated in the BJT mode shows the greatest sensitivity to variations in body thickness and BOX thickness. In consideration of these variations and those in front gate oxide thickness and spacer width, as well as random dopant fluctuation effects, the retention time of a 22 nm-node cell design is reduced by approximately 63 %, from 1.01 s to 0.364 s at room temperature.

4.7 References

[1] C. Shin, M.H. Cho, Y. Tsukamoto, B.-Y. Nguyen, B. Nikolić, and T.-J. King Liu, "SRAM Yield Enhancement with Thin-BOX FD-SOI," *Proc. IEEE Int'l SOI Conf.*, 2009, pp. 1-2.

[2] H. Furuhashi, T. Shino, T. Ohsawa, F. Matsuoka, T. Higashi, Y. Minami, H. Nakajima, K. Fujita, R. Fukuda, T. Hamamoto, and A. Nitayama, "Scaling Scenario of Floating Body Cell (FBC) Suppressing Vth Variation Due to Random Dopant Fluctuation," *Proc. IEEE Int'l SOI Conf.,* 2008, pp. 33-34.

[3] M.H. Cho, C. Shin, and T.-J. King Liu, "Optimization and Variation Studies of BJT-based Ultra Thin Body Capacitorless DRAM Cell," *Int'l Conf. on SSDM*, 2011, F-2-4.

[4] Sentaurus Process User Guide, Synopsys, Inc., Mountain View, CA, version E-2010.12, Dec. 2010.

[5] Sentaurus Device User Guide, Synopsys, Inc., Mountain View, CA, version D-2010.03, Mar. 2010.

[6] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, and E. Faraoni, "New Generation of Z-RAM," *IEDM Tech. Dig.,* 2007, pp. 925-928.

[7] International Technology Roadmap for Semiconductors, 2010. Available : http://www.itrs.net.

[8] O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X. Garros, M-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, and T. Ernst, "Planar Fully Depleted SOI Technology: a powerful architecture for the 20nm node and beyond," *IEDM Tech. Dig.,* 2010, pp. 3.2.1-3.2.4.

[9] W. Schwarzenbach, X. Cauchy, O. Bonnin, N. Daval, C. Aulnette, C. Girard, B.-Y. Nguyen, and C. Maleville, "Ultra-thin film SOI/BOX substrate development, its application and readiness," *Electrochemical Soc. Trans,* vol. 35, no. 5, pp. 239-245, May. 2011.

[10] F. Matsuoka, T. Ohsawa, I. Higashi, H. Furuhashi, K. Hatsuda, K. Fujita, R. Fukuda, N. Ikumi, T. Shino, Y. Minami, H. Nakajima, T. Hamamoto, A. Nitayama, and Y. Watanabe, "FBC's Potential of 6F2 Single Cell Operation in Multi-Gbit Memories Confirmed by a Newly Developed Method for Measuring Signal Sense Margin," *IEDM Tech. Dig.,* 2007, pp. 39-42.

[11] D.-I. Moon, S.-J. Choi, J.-W. Han, S. Kim, and Y.-K. Choi, "Fin-Width Dependence of BJT-Based 1T-DRAM Implemented on FinFET," *IEEE Electron Device Lett.,* vol. 31, no. 9, pp. 909-911, Sep. 2010.

[12] C. Shin, "Advanced MOSFET Designs and Implications for SRAM Scaling," Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., University of California, Berkeley, CA, 2011.

[13] H. Jeong, K.-W. Song, I.H. Park, T.-H. Kim, Y.S. Lee, S.-G. Kim, J. Seo, K. Cho, K. Lee, H. Shin, J.D. Lee, and B.-G. Park, "A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell), " *IEEE Trans. Nanotechnology,* vol. 6, no. 3, pp. 352-357, May, 2007.

[14] S. Kim, R. J. Tseng, W. Rachmady, B. Jin, U. Shah, I. Ban, U. E. Avci, and P. L..D. Chang, "Silicon on Replacement Insulator (SRI) Floating Body Cell (FBC) Memory," *VLSI Symp. Circuit Dig.*, Jun. 2010, pp. 165-166.

[15] K. Kim and J. Lee, "A New Investigation of Data Retention Time in Truly Nanoscaled DRAMs," *IEEE Electron Device Lett.,* vol. 30, no. 8, pp. 846-848, Aug. 2009.

Chapter 5

Variation-Aware Study with Scaling Limit

5.1 Introduction

Scaling is one of the most important issues for device technologies. As rapid development in transistor scaling continues, questions about minimum device dimensions related to performance limits become important. For several decades, higher speed and higher density memory devices with lower bit cost have been successfully achieved with scaled down semiconductor memory technologies [1]. For transistors having channel length shorter than 10 nm, experimental progress has already been reported [2-4]. With the progress of logic application transistor scaling, conventional DRAM (*i.e.* 1 access transistor and 1 storage capacitor: 1T1C) has successfully been scaled down [5]. However, 1T1C DRAM cell scaling has limitation due to the presence of a capacitor which is difficult to reduce in size. Capacitorless DRAM as a novel concept of the DRAM memory cell based on a single transistor was introduced in the early 1990s [6]. Capacitorless DRAM is expected to have simple processes and superior scalability compared to conventional DRAM [7-10]. However, there have been very few studies conducting about scaling for capacitorless DRAM [11, 12]. Sverdlov *et al.* and Butt *et al.* looked at scaling capacitorless DRAM based on the short channel effect (*i.e.* drain induced barrier lowering) or the quantum mechanical/atomistic level models. Though these models can suggest ultimate scaling limitations, they did not account for process induced variation factors. Additionally, because the MOSFET based operation mode (MOSFET mode) was used in their studies, the new operating mode (BJT mode [9]) should be investigated.

The short channel effect and variation factors are suppressed with thin body SOI structure because it has extremely high gate controllability [13-15]. Due to these advantages, the thin body SOI transistor with ultra-thin buried oxide (UTBOX) is one of the most promising candidates for scaled capacitorless DRAM. However, there have been

very a few investigations into capacitorless DRAM scaling with a thin body SOI structure [16]. In order to account for scaling-induced degradation, the process variation factors in fabrication should be considered. V_T variation is caused by many sources [17-19]. Dimensional variation sources include spacer width, body thickness, BOX thickness, and gate oxide thickness variations. In this study, random dopant fluctuations (RDF) are also considered. In the present study, the scaling of capacitorless DRAM with consideration of variation sources is investigated. **Fig. 5.1** shows the scaling investigation process flow. First, the body thickness limit is investigated and gate length is reduced. The scaling rule is to maintain a ***constant electric field*** in the body. The retention time and sensing margin of capacitorless DRAM are affected by electric field in the Hold state [20]. Additionally, in order to guarantee the oxide reliability, the constant electric field is the most reasonable scaling rule in capacitorless DRAM [21-22]. The optimized conditions are achieved based on constant field scaling. Finally the sensing margin is measured in terms of variation factors and each variation factor is also studied. The ultimate scaling limits will be proposed.

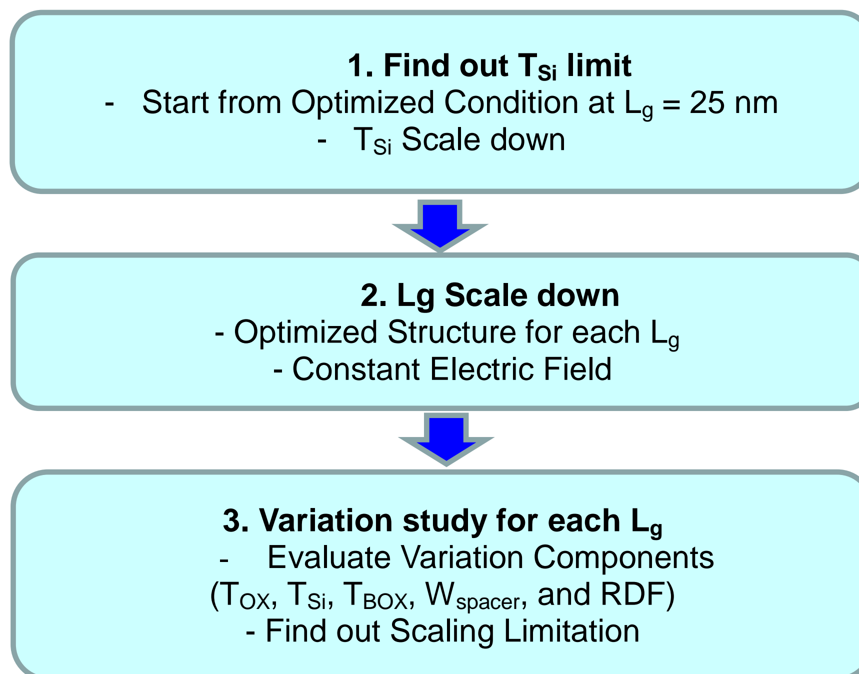


Figure 5.1. Process for determining scaling limit of the BJT mode capacitorless DRAM cell. This study follows the *constant electric field rule* because the electric field determines the retention time and sensing current in capacitorless DRAM operations.

5.2 Body Thickness Limitation

5.2.1 Reference Cell (25 nm Gate length) Design

The layout dimensions of the reference cell (with 25 nm gate length, L_g) were selected based on 22 nm SOI CMOS technology [15, 20, 23]. The BOX thickness (T_{BOX}) is set to be 10 nm because the fabrication process capability and ITRS are considered [24]. Due to reliability considerations, the gate oxide (SiO_2) thickness (T_{ox}) and gate-sidewall spacer width (W_{spacer}) cannot be scaled down with L_g and hence are fixed at 3 nm and 21 nm, respectively [20]. The body is also undoped, and the sub-BOX substrate underneath the body is doped P-type. Four operations are simulated herein for the capacitorless DRAM cell: Write 1, Write 0, Hold, and Read. Default cell operating voltages are summarized in **Table 5.1.** Sentaurus (version 2010) is used to simulate basic cell operations (Write, Hold, and Read) at room temperature [25, 26]. The durations of the Write and Read operations are each 20 ns.

	Write 1	Write 0	Hold	Read
Front Gate Voltage, V_{gs}	-1.0	0.0	-1.6	-1.0
Back Gate Voltage, V_{bg}	2.5	2.5	2.5	2.5
Drain Voltage, V_{ds}	1.7	-0.5	0.0	1.2
Source Voltage, V_s	0.0	0.0	0.0	0.0

Table 5.1. Capacitorless DRAM cell operating voltages (Volts).

5.2.2 Body Thickness Scaling

The thin body structure can reduce the V_T variation that results from various factors such as random dopant fluctuations (RDF). The thin body structure also suppresses drain-induced barrier lowering (DIBL), which is one of the main reasons that FDSOI is a good candidate for ultra-scaled technologies [13-16].

The retention characteristics with body thickness are shown in **Fig. 5.2**. The sensing currents become negligible below the 7 nm body thickness. Although a thinner body is beneficial for suppressing variations, retention time falls to zero if the body is too thin to adequately store charge. **Fig. 5.3** shows a cross sectional view for hole density in each body thickness transistor at Hold 1 state and 1 μs Hold duration time. All structure dimensions and operation conditions are the same except for the body thickness.

Butt *et al.* reported that double gated-capacitorless DRAM body thickness limitation is approximately 3 nm due to quantum confinement effects (QE) [12]. They utilized MOSFET mode and they did not measure sensing margin or retention time. They just focused on reduced hole density that results from the widening band gap. However, the quantum confinement effect is not dominant around 7 nm body thickness [12]. Therefore, QE is not the main reason to limit body thickness scaling.

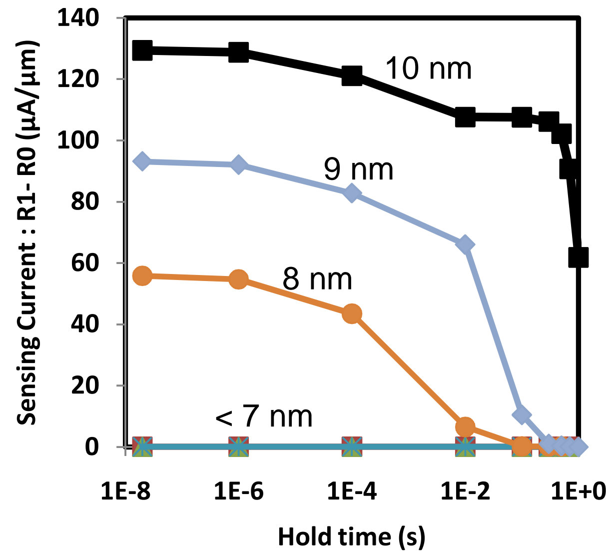


Figure 5.2. Retention characteristics for each body thickness. If body thickness is less than 7nm, the retention time cannot be measured due to negligible sensing current.

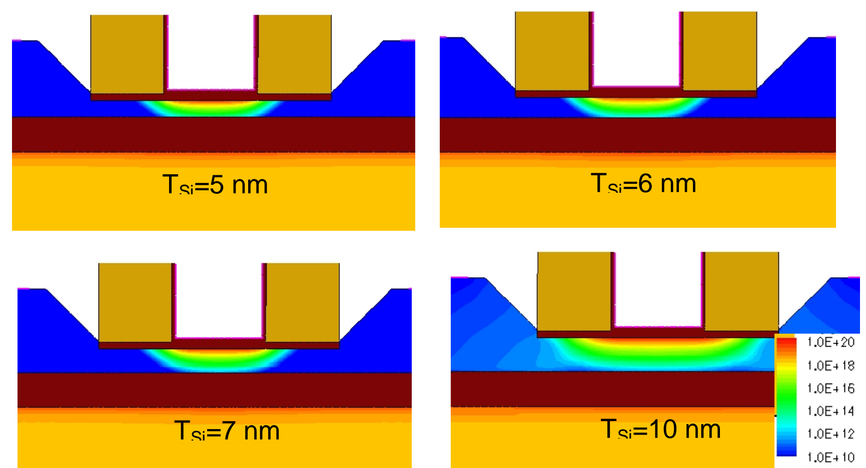


Figure 5.3. Cross sectional view of contour plots for hole density for various body thicknesses. All conditions except for body thickness are the same (Gate length (L_g) = 25 nm). When the body is thinner than 7 nm, the hole density is reduced.

5.3 Design Optimization of Scaled Cells

5.3.1 Scaling Constraints

Band-to-band tunneling (BTBT) limits retention time [20] so it is important to avoid increasing the peak electric field in the Hold state as L_g is scaled down. The cell operating voltages are adjusted together with L_g to maintain a ***constant peak electric field***, and to maximize the retention time. Though the thinner body is desirable for suppressing variations such as RDF [13-16], sensing margin (R1 – R0 current) is reduced with body thickness in capacitorless DRAM. Considering the marginal body thickness (8 nm) and variation ($6\sigma = 0.96$ nm), 9 nm is selected as the nominal body thickness. Due to reliability issues, the gate oxide and the spacer width chosen are kept fixed at 3 nm and 21 nm respectively [20, 22]. BOX thickness is selected to be 10 nm, based on fabrication capabilities [24].

5.3.2 Optimization of Cell Operating Voltages

The cell operating voltages are adjusted together with L_g to maintain a constant peak electric field, and to maximize the retention time. Three biases are selected to optimize the scaled devices: Hold gate voltage (V_{ghold}), back bias (V_{bg}), and Read drain voltages (V_{dr}), which affect the electric field in the body and determine capacitorless DRAM performance (retention time and sensing current) [20].

Figs. 5.4 ~ 5.9 show how the voltages affect performance. Results for the reference structure (L_g = 25 nm and body thickness (T_{Si}) = 9 nm) are shown in **Fig. 5.4**. **Fig. 5.4 (a)** illustrates the retention characteristics for Vghold optimization. Retention times are measured and plotted in **Fig. 5.4 (b)**. Retention time is defined as the Hold time to have 60 μA/μm sensing margin (Read 1 – Read 0) in this study [7, 8, 15, 23]. The retention time is maximized at V_{ghold} = -1.6 V. **Figs. 5.4 (c)** and **(d)** show the back gate bias effect on retention time. At V_{bg} = 2.5 V, the retention time has maximum value. As shown in **Figs. 5.4 (e)** and **(f)**, the retention time is maximized at V_{dr} = 1.4 V. The sensing margin is low due to small Vdr. In very high Vdr region, Read 1 and Read 0 currents increase simultaneously. Therefore, the sensing margin is reduced at an excessively high Vdr. Electric fields at Hold 1 and Hold 0 are measured (**Fig. 5.4 (g)**). These serve as the reference electric fields for the scaled devices (electric field at Hold 1 = 6.22×10^5 V/cm and electric field at Hold 0 = 9.75×10^5 V/cm). The optimized condition is selected at V_{ghold} = -1.6 V, V_{bg}=2.5 V, and V_{dr}=1.4 V. 0.542 s retention time is achieved. Scaled gate lengths (20 nm, 15 nm, 12 nm, 10 nm, and 9 nm) are tested in **Figs. 5.5, 5.6, 5.7, 5.8,** and **5.9** respectively. Optimized conditions are listed in **Table 5.2**. In **Fig. 5.10**, the electric fields of Hold state for each gate length are compared. The electric field of Hold 0 (0.975 MV/cm) and that of Hold 1 (0.622 MV/cm) should be maintained with scaling. In **Fig. 5.10 (b),** the percentages of electric field deviation are plotted. In this study, the electric field change kept with scaling is within 5%. Retention time for each gate length and electric field are summarized in **Table 5.3**. **Fig. 5.11** shows that the nominal retention time decreases with scaling, falling below 10 ms at 9 nm L_g.

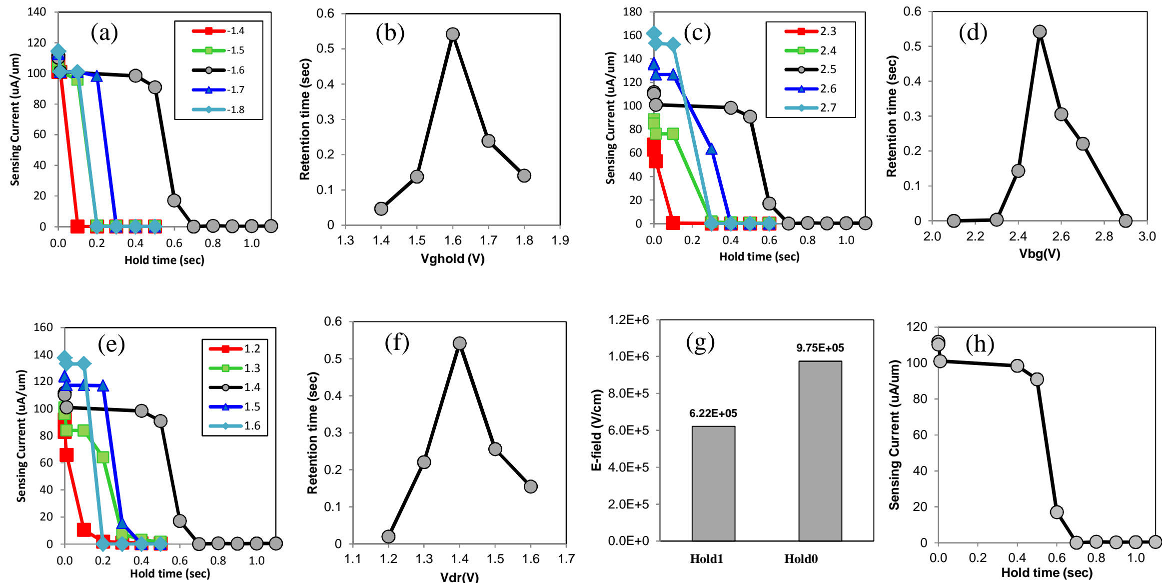


Figure 5.4. Optimization for L_g=25 nm. (a) Retention characteristics for various gate Hold voltage (V_{ghold}). (b) The retention time is maximized at V_{ghold}= -1.6 V from (a). (c) Retention characteristics for various back gate biases (V_{bg}). (d) The retention time is maximized at V_{bg}= 2.5 V. (e) Retention characteristics for various Read drain voltage (V_{dr}). (f) The retention time is maximized at V_{dr}= 1.4 V. (g) Electric field at Hold 1/Hold 0 state at optimized condition. (h) Optimized retention time is 0.542 s.

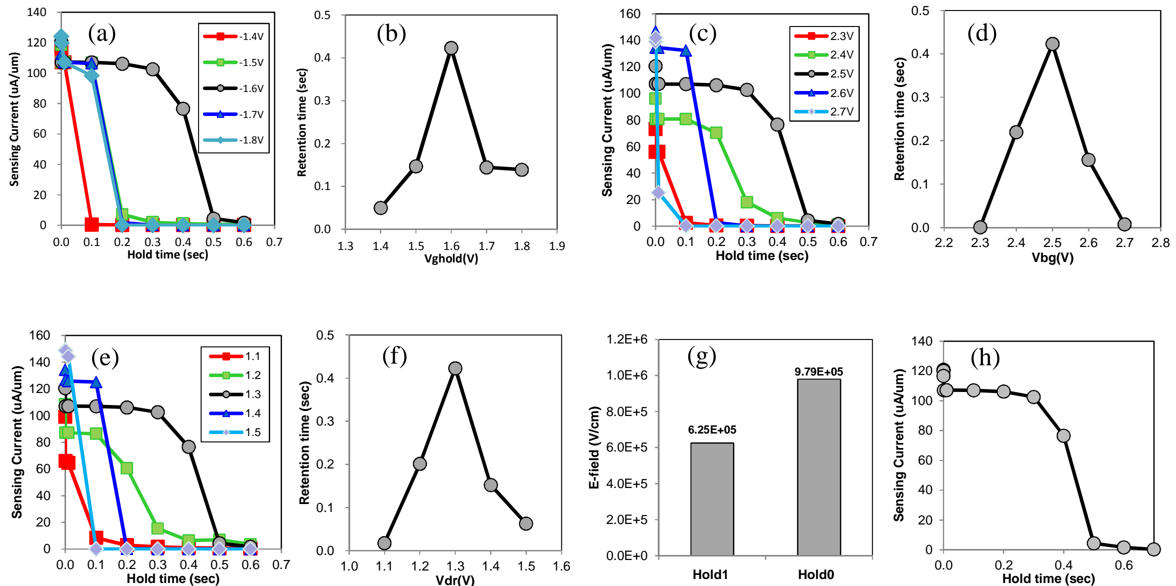


Figure 5.5. Optimization for L_g=20 nm. (a) Retention characteristics for various gate Hold voltage (V_{ghold}). (b) The retention time is maximized at V_{ghold}= -1.6 V from (a). (c) Retention characteristics for various back gate biases (V_{bg}). (d) The retention time is maximized at Vbg= 2.5 V. (e) Retention characteristics for various Read drain voltage (V_{dr}). (f) The retention time is maximized at V_{dr}= 1.3 V. (g) Electric field at Hold 1/Hold 0 state at optimized condition. (h) Optimized retention time is 0.423 s.

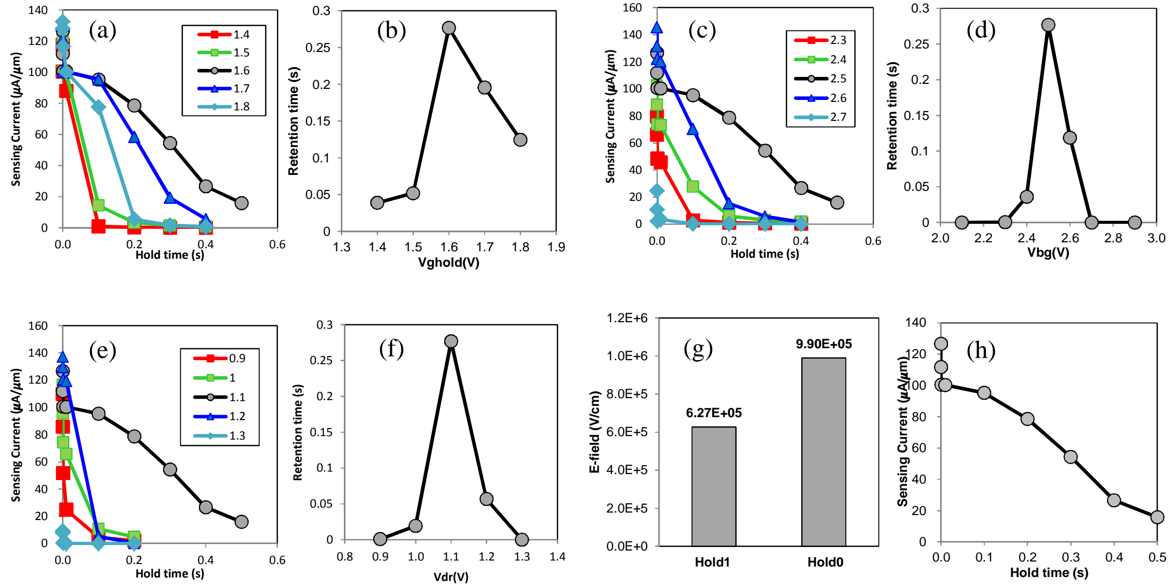


Figure 5.6. Optimization for L_g=15 nm. (a) Retention characteristics for various gate Hold voltage (V_{ghold}). (b) The retention time is maximized at V_{ghold}= -1.6 V from (a). (c) Retention characteristics for various back gate biases (V_{bg}). (d) The retention time is maximized at V_{bg}= 2.5 V. (e) Retention characteristics for various Read drain voltage (V_{dr}). (f) The retention time is maximized at V_{dr}= 1.1 V. (g) Electric field at Hold 1/Hold 0 state at optimized condition. (h) Optimized retention time is 0.277 s.

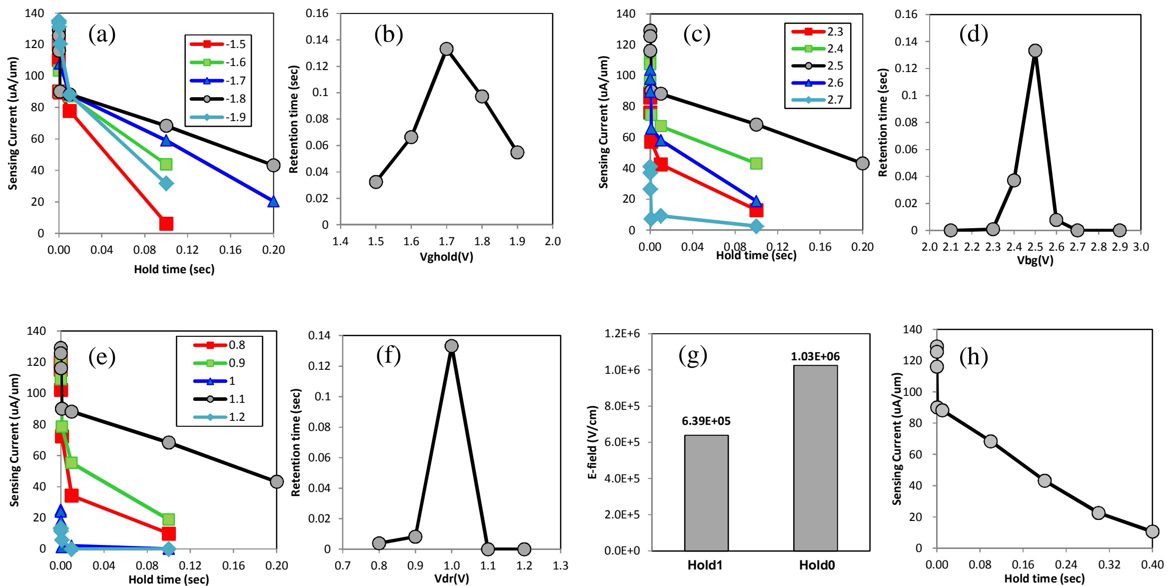


Figure 5.7. Optimization for L_g=12 nm. (a) Retention characteristics for various gate Hold voltage (V_{ghold}). (b) The retention time is maximized at V_{ghold}= -1.7 V from (a). (c) Retention characteristics for various back gate biases (V_{bg}). (d) The retention time is maximized at V_{bg}= 2.5 V. (e) Retention characteristics for various Read drain voltage (V_{dr}). (f) The retention time is maximized at V_{dr}= 1.0 V. (g) Electric field at Hold 1/Hold 0 state at optimized condition. (h) Optimized retention time is 0.133 s.

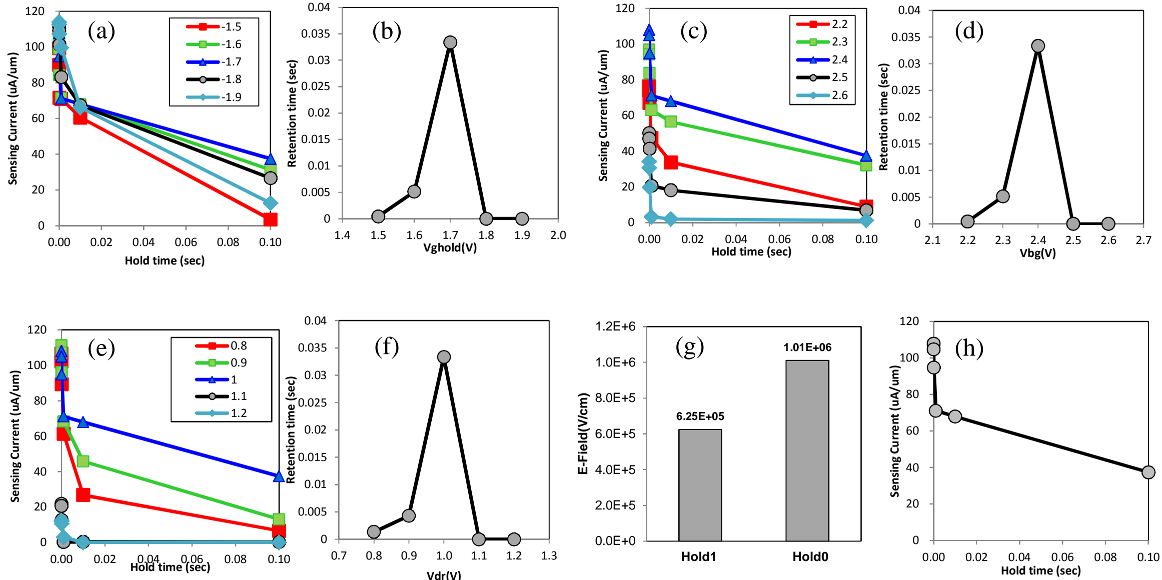


Figure 5.8. Optimization for L_g=10 nm. (a) Retention characteristics for various gate Hold voltage (V_{ghold}). (b) The retention time is maximized at V_{ghold}= -1.7 V from (a). (c) Retention characteristics for various back gate biases (V_{bg}). (d) The retention time is maximized at V_{bg}= 2.4 V. (e) Retention characteristics for various Read drain voltage (V_{dr}). (f) The retention time is maximized at V_{dr}= 1.0 V. (g) Electric field at Hold 1/Hold 0 state at optimized condition. (h) Optimized retention time is 0.033 s.

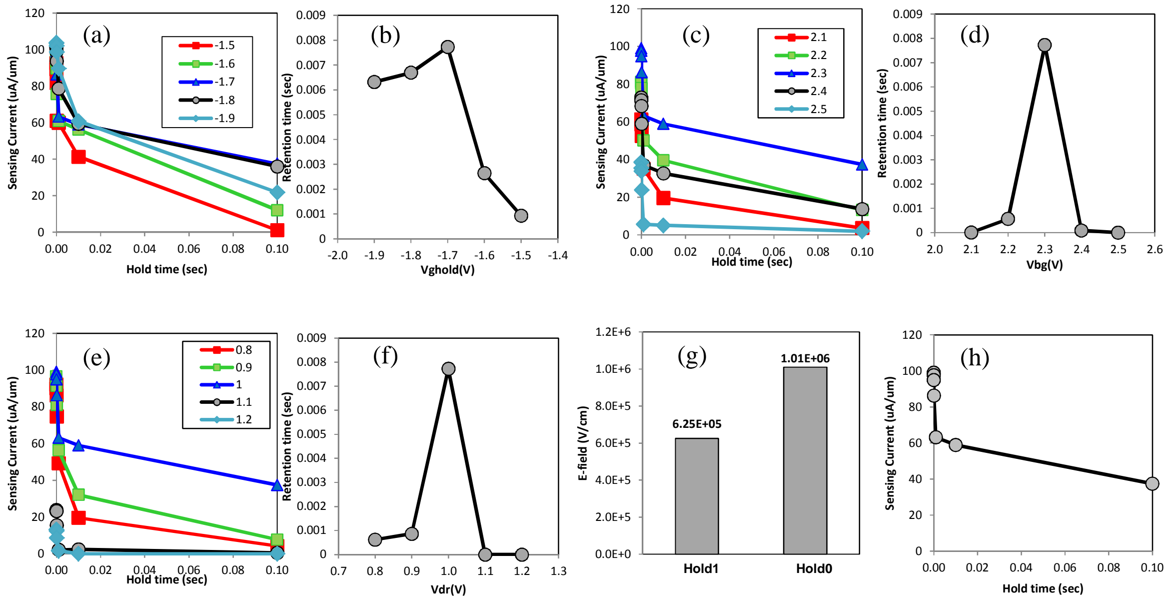


Figure 5.9. Optimization for L_g=9 nm. (a) Retention characteristics for various gate Hold voltage (V_{ghold}). (b) The retention time is maximized at V_{ghold}= -1.7 V from (a). (c) Retention characteristics for various back gate biases (V_{bg}). (d) The retention time is maximized at V_{bg}= 2.3 V. (e) Retention characteristics for various Read drain voltage (V_{dr}). (f) The retention time is maximized at V_{dr}= 1.0 V. (g) Electric field at Hold 1/Hold 0 state at optimized condition. (h) Optimized retention time is 0.0077 s.

L_g (nm)	T_{Si} (nm)	V_{bg} (V)	V_{ghold} (V)	V_{dr} (V)
9	9	2.3	-1.7	1
10	9	2.4	-1.7	1
12	9	2.5	-1.7	1
15	9	2.5	-1.6	1.1
20	9	2.5	-1.6	1.3
25	9	2.5	-1.6	1.4

Table 5.2. Optimized operating voltages for each gate length. V_{bg}, V_{ghold}, and V_{dr} affect performance and electric field in the body [20].

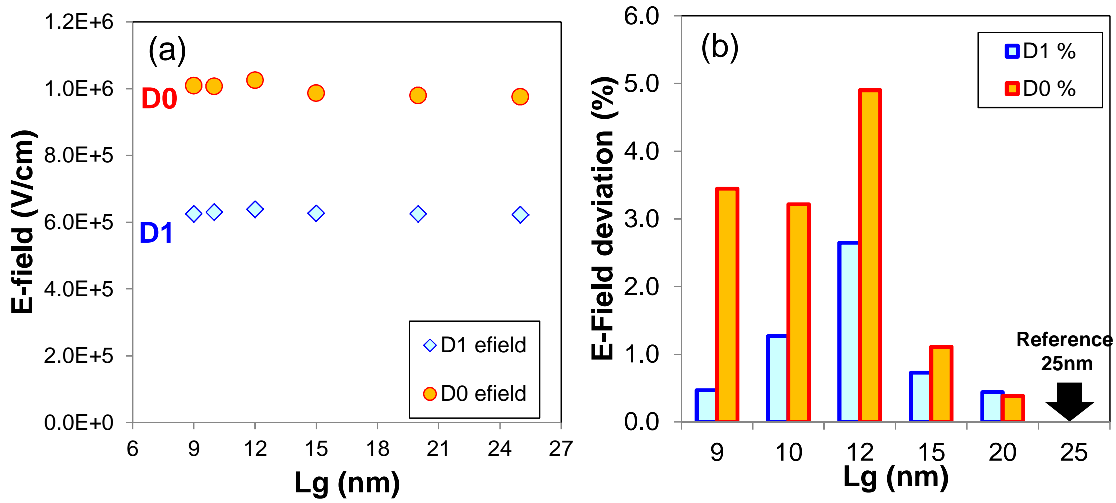


Figure 5.10. Electric field for optimized operating voltages for each gate length. (a) Hold 1 (D1) and Hold 0 (D0) state. (b) Electric field deviation (%) (reference structure is L_g=25 nm).

Gate length (nm)	Retention time (s)	D1 E-field (MV/cm)	D0 E-field (MV/cm)
9	0.008	0.63	1.01
10	0.033	0.63	1.01
12	0.133	0.64	1.02
15	0.277	0.63	0.99
20	0.423	0.62	0.98
25	0.542	0.62	0.98

Table 5.3. Retention time and electric field for each gate length. Retention time is reduced as gate length is lowed, and it drops to negligible level below 9 nm L_g.

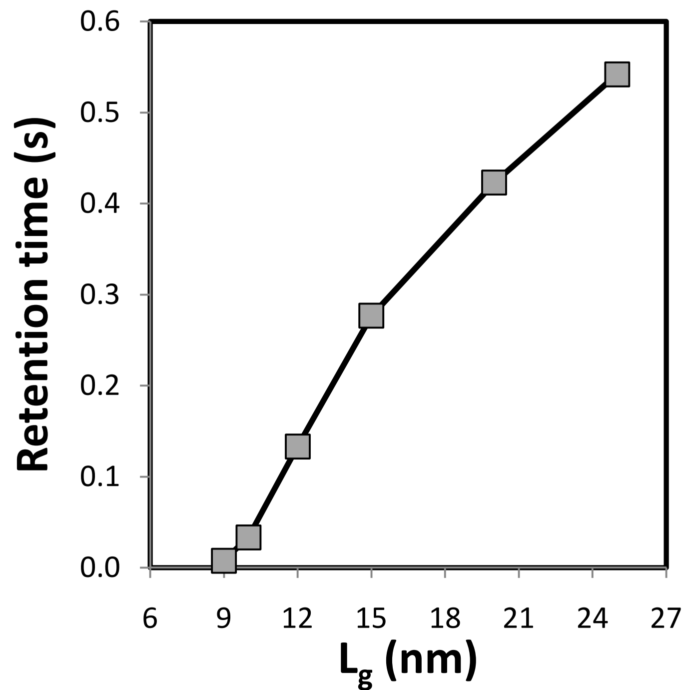


Figure 5.11. Median retention time with gate length. Each retention time is measured under a constant electric field in optimized condition.

5.4 Scaling Limitation in Terms of Variation Factors

5.4.1 Variation Factors

Systematic variations in T_{Si}, T_{BOX}, T_{ox}, and W_{spacer} are considered. Random dopant fluctuation (RDF) effects are investigated via Kinetic Monte Carlo (KMC) simulation (**Table 5.4**) [24, 27, 28]. The variation of each dimension is assumed to have a normal distribution, and the deviation of each factor induces a deviation in Read 1 and Read 0.

	T_{Si}	T_{BOX}	T_{OX}	W_{Spacer}
Median Value	9nm	10 nm	3 nm	21 nm
Standard Dev.	$1\sigma = 1.6$ Å	$1\sigma = 1.6$ Å	$1\sigma = 0.4$ Å	$1\sigma = 3.5$ Å
References	[24, 27]	[24, 28]	[24]	$3\sigma = 5\%$
LL (-4.5σ)	8.28 nm	9.28 nm	2.82 nm	19.43 nm
UL ($+4.5\sigma$)	9.72 nm	10.72 nm	3.18 nm	22.58 nm

Table 5.4. Variation factors used for device simulations

5.4.2 Dimension Variation Effects with Scaling

RDF is found to affect the local electric field and thereby the impact ionization rate and BTBT, hence the sensing current (**Fig. 5.12 (a)**) [16]. 100 cases in total are simulated with Sentaurus [25, 26].

To gauge the influence of each variation source, the concept of Sigma Sensitivity (SS) [23] is used: SS is defined to be the deviation (from the nominal value) in Read current that results from a standard-deviation change in the parameter of interest, keeping all other parameters fixed, and is plotted in **Figs. 5.12 (b)** and **(c)** for Read 1 and Read 0 currents, respectively.

Based on measured variation data, Matsuoka *et al*. introduced a signal sense margin (SSM) metric [29]. SSM is defined :

$$Signal\ Sensing\ Margin\ (SSM) = <\Delta I_{sensing}> - \alpha \times (\sigma_{Read\ 0} + \sigma_{Read\ 1}) \quad (1)$$

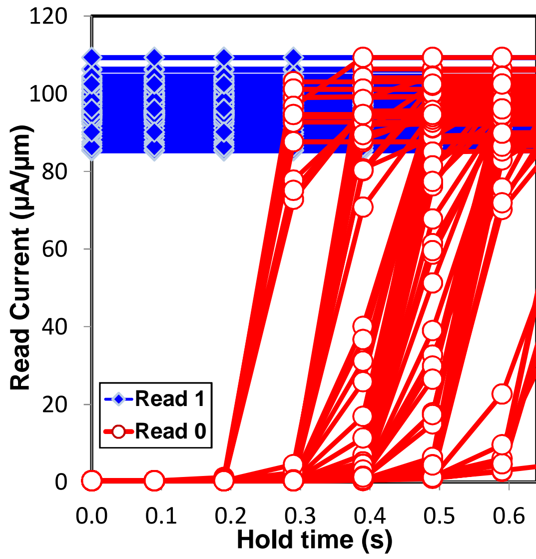
where $<\Delta I_{sensing}>$ is the average sensing margin (Read 1 – Read 0), and α is set to be 4.5 appropriate for 64 redundancies in 16M bit cells. When SSM drops below zero, the sensing margin can be negligible. Thus, SSM can be an indicator for variation immunity. Under the assumption that each variation dimension is statistically independent of other factors and all variations have normal distributions (Gaussian distributions), the total current variation is calculated as follows [17]:

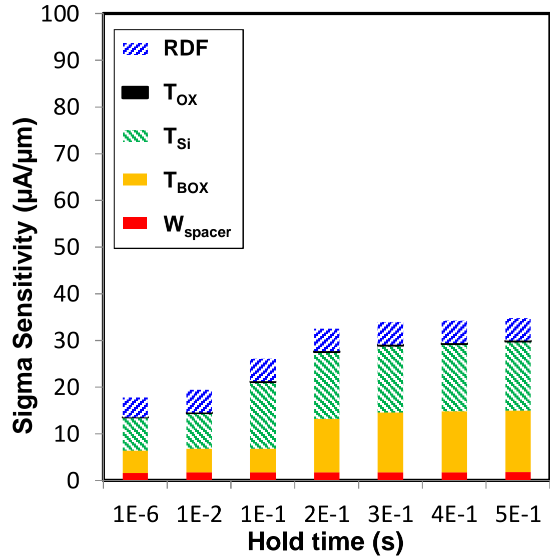
$$\sigma_{Read\ 0} \approx \sqrt{\begin{array}{c}(\sigma_{Read\ 0,RDF})^2 + (\sigma_{Read\ 0,T_{OX}})^2 + (\sigma_{Read\ 0,T_{Si}})^2 \\ +(\sigma_{Read\ 0,T_{BOX}})^2 + (\sigma_{Read\ 0,W_{spacer}})^2\end{array}} \quad (2)$$

$$\sigma_{Read\ 1} \approx \sqrt{\begin{array}{c}(\sigma_{Read\ 1,RDF})^2 + (\sigma_{Read\ 1,T_{OX}})^2 + (\sigma_{Read\ 1,T_{Si}})^2 \\ +(\sigma_{Read\ 1,T_{BOX}})^2 + (\sigma_{Read\ 1,W_{spacer}})^2\end{array}} \quad (3)$$

Fig. 5.12 (d) shows the way in which SSM and the nominal sensing current margin ($\Delta I_{sensing}$) each depend on the Hold time. Without accounting for variations, the retention time is overestimated to be 0.542 s (the Hold time at which $\Delta I_{sensing}$ falls below 60 µA/µm). Process-induced variations effectively reduce the retention time by ~62%, to 0.209 s (the Hold time at which SSM falls below 0).

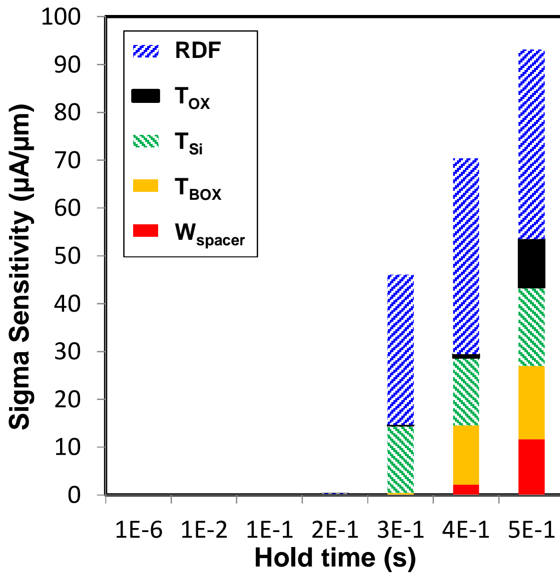
Variation simulations for 20 nm L_g are shown in **Fig. 5.13**. Retention time variation from RDF increases due to shorter gate length (**Fig. 5.13 (a)**), and variations also increase as shown in **Figs. 5.13 (b)** and **(c)**. **Fig. 5.13 (d)** shows sensing currents and SSMs with Hold time. Median retention time is 0.422 s and SSM falls to zero at 0.135 s. Still, there are large enough operation margins for a 20 nm gate length. **Fig. 5.14** shows results at 15 nm gate length. As is evident, shorter gate lengths degrade retention time variations. Even though median retention time is 0.27 s, SSM drops at 0.032 s (**Fig. 5.14 (d)**). Since the required retention time for stand-alone DRAM application is 0.064 s (JEDEC spec: [30]), 0.032 s may not be sufficient for this purpose. However, 15 nm gate length capacitorless DRAM is still competitive for embedded DRAM. Embedded DRAM allows a much more frequent refresh and retention time specifications as low as several hundred microseconds, depending on the application and design (Embedded DRAM does not follow JEDEC specifications) [31-33].

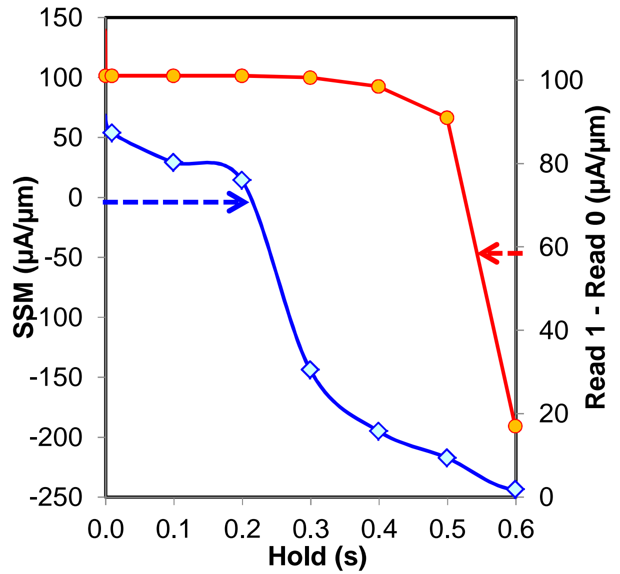




(a)

(b)

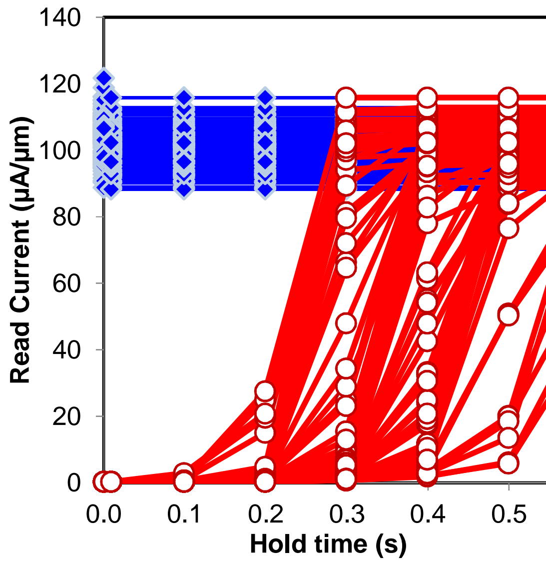




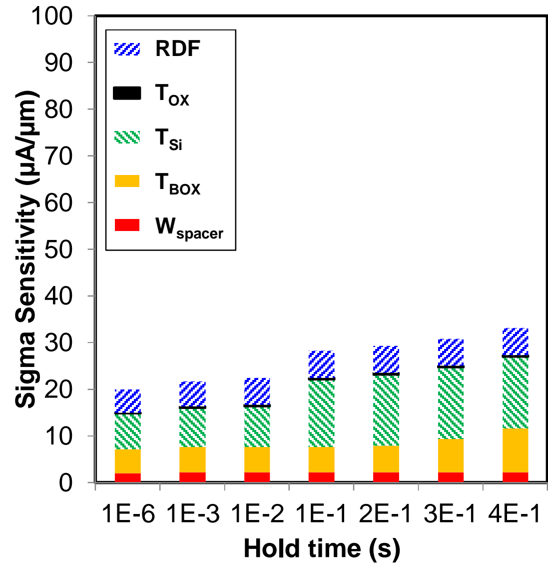
(c)

(d)

Figure 5.12. Gate length = 25 nm. (a) Simulated retention characteristics showing the impact of RDF. (100 cases are simulated using the KMC method. (b) Sigma sensitivity for capacitorless DRAM Read 1 current. The impact of 1-sigma variation is shown for each parameter, along with the impact of RDF, as a function of the data Hold time. (c) For Read 0. (d) Left axis is signal sense margin (SSM) and right axis is median sensing current (Read 1 current – Read 0 current) as a function of Hold time. Due to variations, the data retention time is reduced from 0.542 s to 0.209 s.



(a)



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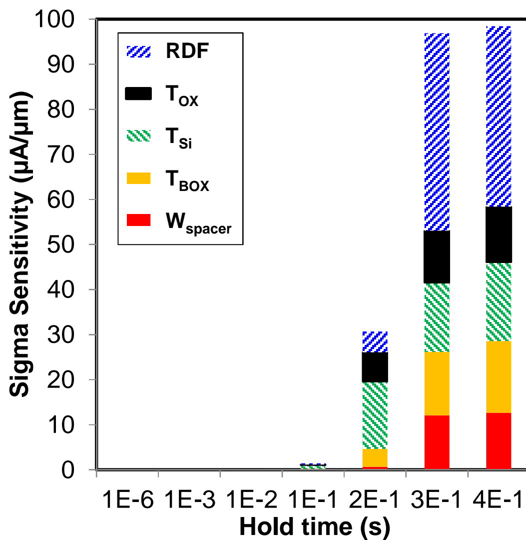

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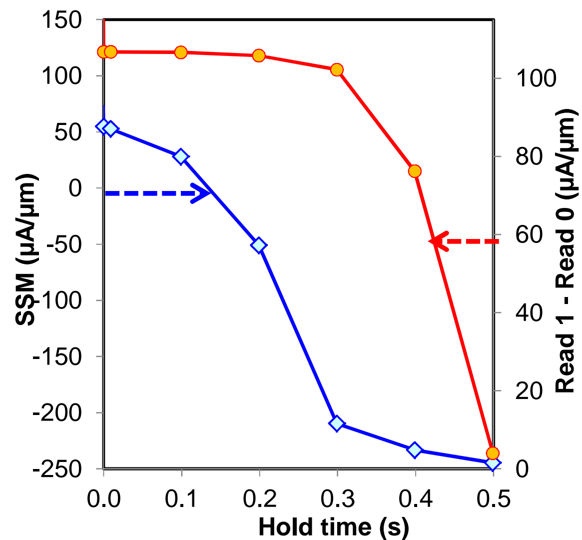
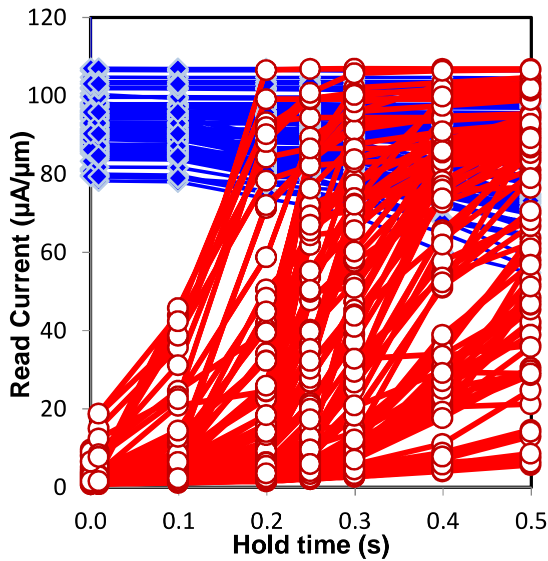
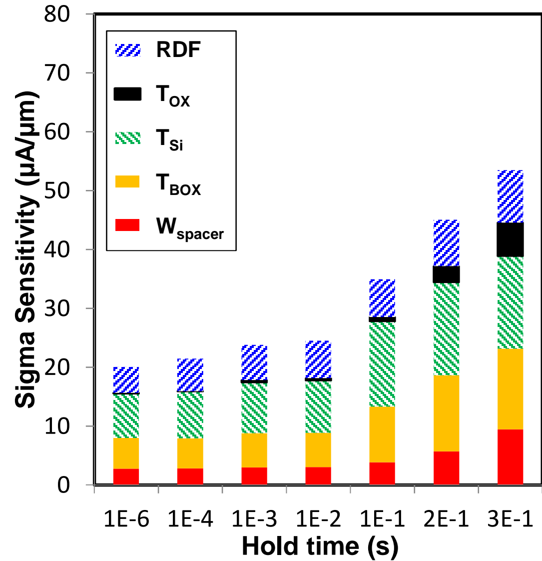


(d)

Figure 5.13. Gate length = 20 nm. (a) Simulated retention characteristics showing the impact of RDF. (100 cases are simulated using the KMC method. (b) Sigma sensitivity plots for capacitorless DRAM Read 1 current. The impact of 1-sigma variation is shown for each parameter, along with the impact of RDF, as a function of the data Hold time. (c) For Read 0. (d) Left axis is signal sense margin (SSM) and right axis is median sensing current (Read 1 current – Read 0 current) as a function of Hold time. Due to variations, the data retention time is reduced from 0.423 s to 0.135 s.



(a)



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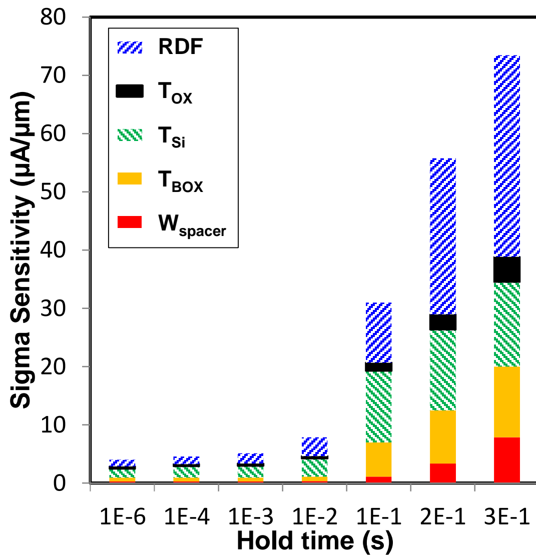
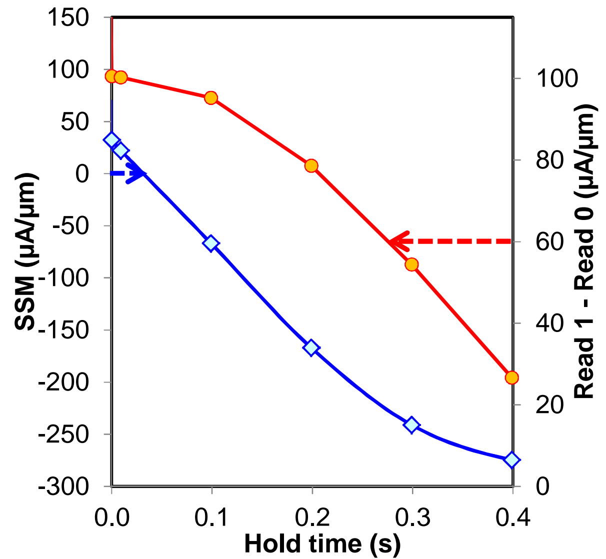
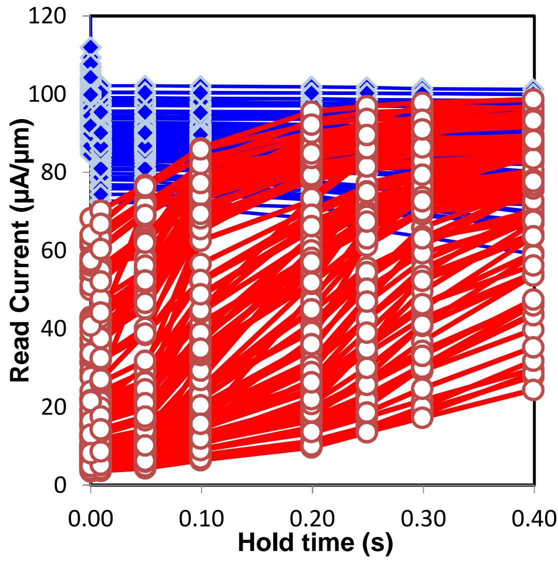


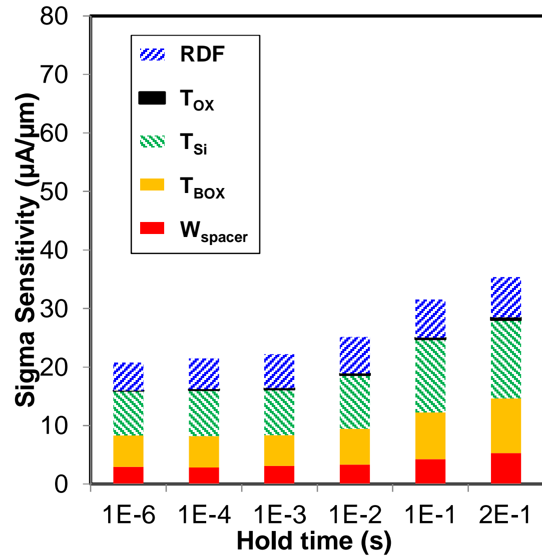
(c)



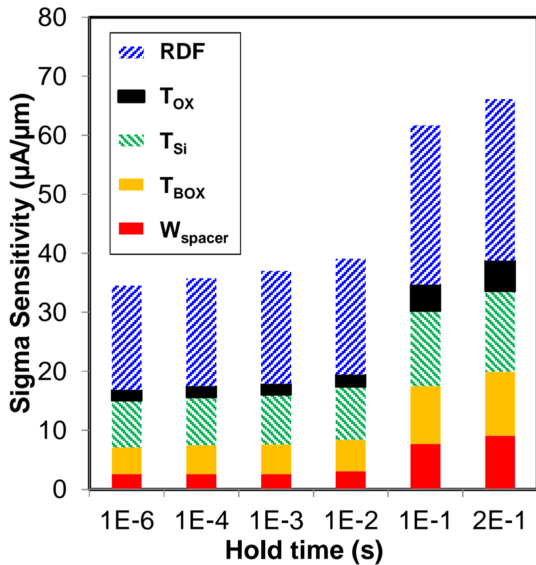
(d)

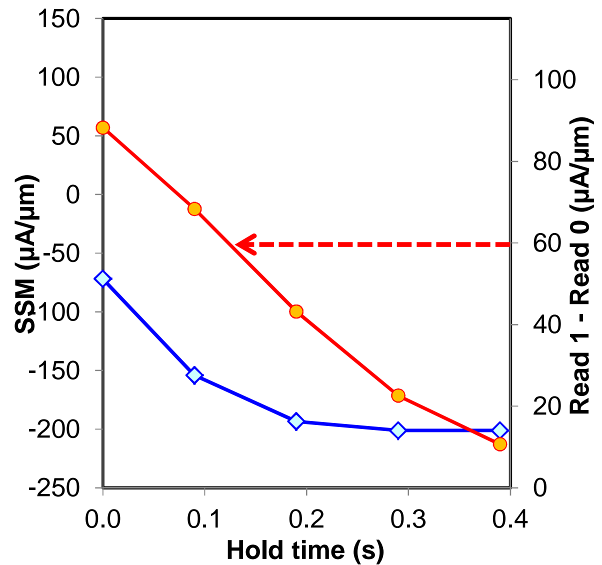
Figure 5.14. Gate length = 15 nm. (a) Simulated retention characteristics showing the impact of RDF. (100 cases are simulated using the KMC method. (b) Sigma sensitivity plots for capacitorless DRAM Read 1 current. The impact of 1-sigma variation is shown for each parameter, along with the impact of RDF, as a function of the data Hold time. (c) For Read 0. (d) Left axis is signal sense margin (SSM) and right axis is median sensing current (Read 1 current – Read 0 current) as a function of Hold time. Due to variations, the data retention time is reduced from 0.277 s to 0.032 s.





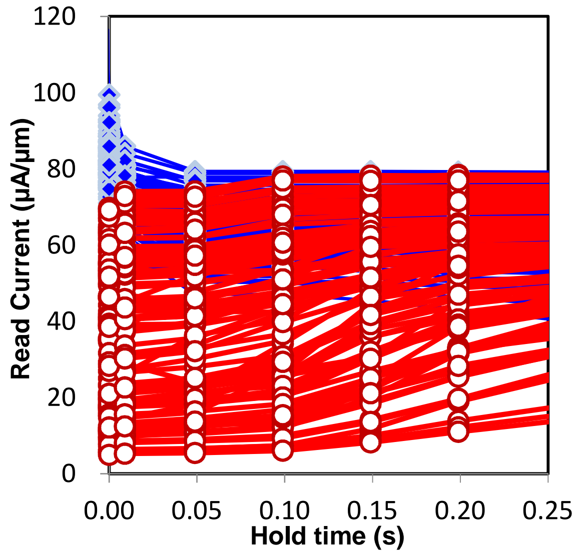
(a) (b)

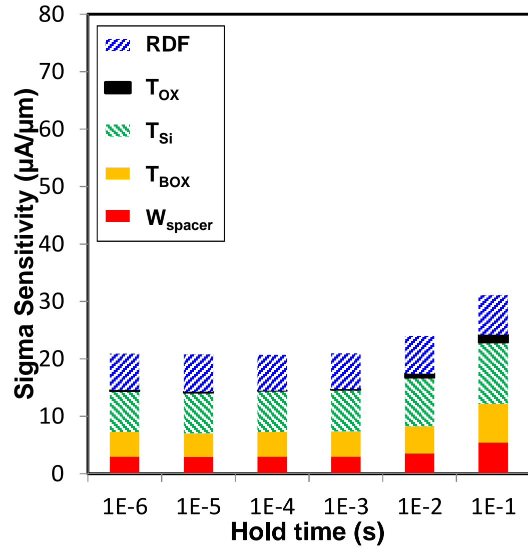




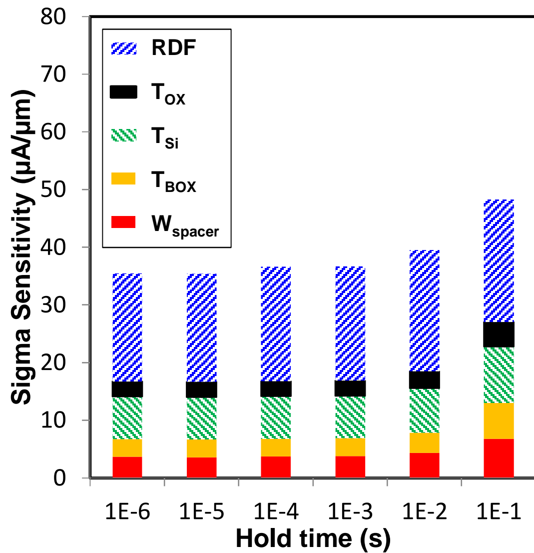
(c) (d)

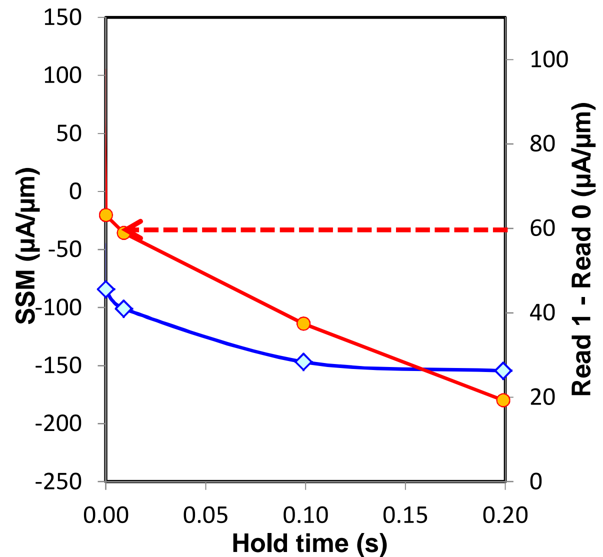
Figure 5.15. Gate length = 12 nm. (a) Simulated retention characteristics showing the impact of RDF. (100 cases are simulated using the KMC method. (b) Sigma sensitivity plots for capacitorless DRAM Read 1 current. The impact of 1-sigma variation is shown for each parameter, along with the impact of RDF, as a function of the data Hold time. (c) For Read 0. (d) Left axis is signal sense margin (SSM) and right axis is median sensing current (Read 1 current – Read 0 current) as a function of Hold time. The retention time 0.133 s but SSM is always negative in all whole range of Hold time due to variation.





(a) (b)





(c) (d)

Figure 5.16. Gate length = 9 nm. (a) Simulated retention characteristics showing the impact of RDF. (100 cases are simulated using the KMC method. (b) Sigma sensitivity plots for capacitorless DRAM Read 1 current. The impact of 1-sigma variation is shown for each parameter, along with the impact of RDF, as a function of the data Hold time. (c) For Read 0. (d) Left axis is signal sense margin (SSM) and right axis is median sensing current (Read 1 current – Read 0 current) as a function of Hold time. The retention time 0.077 s but SSM is always negative in all whole range of Hold time due to variation.

The corresponding results in **Fig. 5.15** for 12 nm L_g clearly show the increased impact of variations (in particular RDF) at shorter gate lengths, as SSM becomes negative even at 1 μs Hold time. This means that capacitorless DRAM devices that have gate length under 12 nm cannot guarantee production yields due to variation issues. **Fig. 5.16 (a)** shows retention characteristic variations that result from RDF (gate length is 9 nm). The impact of RDF is dominant with a range of Hold time as shown in **Figs. 5.16 (b)** and **(c).** With the 9 nm gate length transistor, capacitorless DRAM has very short median retention time (7.7 ms) and large variation sigma. Therefore, SSM is always negative below 1 μs and no yield is predicted. Even though SOI or 3-dimension transistors may provide solutions for scaling under 10 nm, the scaling of capacitorless DRAM is more sensitive to variation problems.

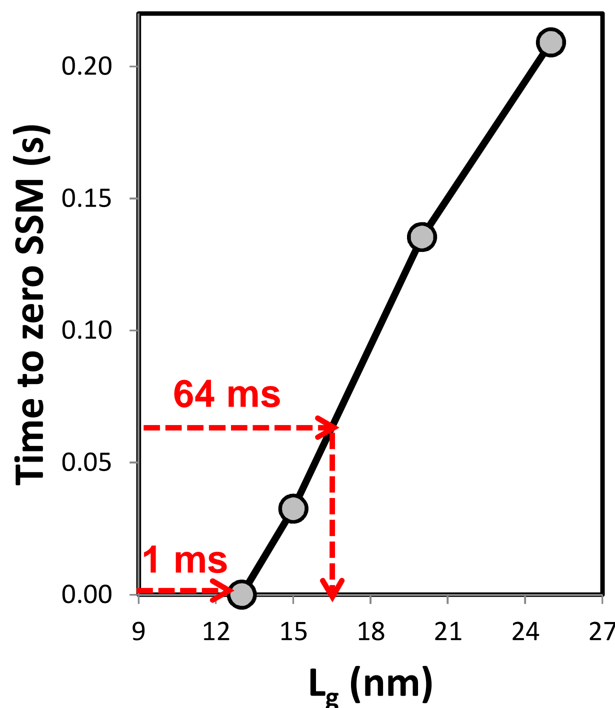


Figure 5.17. Time to Zero SSM (TZS) *vs.* gate length. TZSs are measured from **Fig. 5.13 (d), Fig. 5.14 (d),** and **Fig. 5.15 (d).** For stand-alone DRAM application, TZS=64 ms is selected and corresponding gate length is 16.5 nm. For e-DRAM application, TZS= 1 ms is assumed. Corresponding gate length is 13 nm that is ultimate scaling limit for thin body capacitorless DRAM.

From the graph of variation-aware retention time (Time to Zero SSM) *vs*. L_g in **Fig. 5.17**, it can be seen that the minimum L_g is approximately 16.5 nm for stand-alone DRAM applications (64 ms retention time [30]). For embedded DRAM (e-DRAM) applications (1 ms retention time [33]), the minimum L_g is around 13 nm. Capacitorless DRAM is more sensitive to variability compared to logic device applications because BTBT or impact ionization variations should be considered in addition to V_T variation.

5.5 Summary

In this study, the scaling limits of thin body SOI with UTBOX capacitorless DRAM is investigated through the analysis of dimension variations. This is the first study to explore this issue. For body thickness below 7 nm, the sensing current is negligible due to reduced hole density. Thus, in this study, body thickness is set as 9 nm, and then gate length is scaled down. The cell design and operating voltages are optimized at each gate length, following a constant electric field methodology. Systematic variations (normal distributions) in W_{spacer}, T_{Si}, T_{BOX}, and T_{OX} are considered and RDF effects are investigated through KMC simulation. As scaling down occurs, median retention time (at an optimized condition for each gate length) decreases and sigma variation increases. SSM is utilized to evaluate scaling limits that result from variations. Retention time decreases with gate length, so that the scaling limit is expected to be 16.5 nm or 13 nm, depending on the application.

5.6 References

[1] S.Y. Cha, "DRAM Technology - History & Challenges," *IEDM Technical Dig. short course lecture,* 2011.

[2] B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. A. Roy, O. Dokumaci, Z. Ren, F. Jamin, L. Shi, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H.-S. P. Wong, and W. Haensch, "Extreme scaling with ultra-thin Si channel MOSFETs," *IEDM Tech. Dig.,* Dec. 2002, pp. 267–270.

[3] H. Wakabayashi, T. Ezaki, T. Sakamoto, H. Kawaura, N. Ikarashi, N. Ikezawa, M. Narihiro, Y. Ochiai, T. Ikezawa, K. Takeuchi, T. Yamamoto, M. Hane, and T. Mogami, "Characteristics and Modeling of Sub-10-nm Planar Bulk CMOS Devices Fabricated by Lateral Source/Drain Junction Control," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 1961 - 1970, Sep. 2006.

[4] H. Kawaura, T. Sakamoto, and T. Baba, "Transport properties in Sub-10-nm-gate EJ-MOSFETs," in *Proc. Int. Conf. SSDM*, 1999, pp. 20–21

[5] S. Hong, "Memory Technology Trend and Future Challenges," *IEDM Tech. Dig.*, Dec. 2010, pp. 12.4.1 - 12.4.4.

[6] H.-J. Wann and C. Hu, "Capacitorless DRAM Cell on SO1 Substrate*", IEDM Technical Dig.*, Dec. 1993, pp. 635-638.

[7] S. Kim, R. J. Tseng, W. Rachmady, B. Jin, U. Shah, I. Ban, U. E. Avci, and P. L..D. Chang, "Silicon on Replacement Insulator (SRI) Floating Body Cell (FBC) Memory," *VLSI Symp. Circuit Dig.*, Jun. 2010, pp. 165-166.

[8] H. Jeong, K.-W. Song, I.H. Park, T.-H. Kim, Y.S. Lee, S.-G. Kim, J. Seo, K. Cho, K. Lee, H. Shin, J.D. Lee, and B.-G. Park, "A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell)," *IEEE Trans. Nanotechnology*, vol. 6, no. 3, pp. 352-357, May, 2007.

[9] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, E. Faraoni, "New Generation of Z-RAM", *IEDM Technical Dig.*, Dec. 2007, pp. 925-928.

[10] M.H. Cho, C. Shin, and T.-J. K. Liu, "Convex Channel Design for Improved CapacitorlessDRAM Retention Time Simulation of Semiconductor Processes and Devices", *IEEE International conference on simulation of semiconductor processes and devices (SISPAD)*, Sep. 2009, pp. 1-4.

[11] V. Sverdlov and S. Selberherr, "Scaling of Advanced Floating Body Z-RAM Storage Cells: A Modeling Approach," *VLSI-SoC. Int. Conf. on Digital Object Identifier*, 2009, pp. 85 -188.

[12] N. Z. Butt and M.A. Alam, "Scaling Limits of Double-Gate and Surround-GateZ-RAM Cells," *IEEE Trans. Electron Devices,* vol. 54, no. 9, pp. 2255 - 2262, Sep. 2007.

[13] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B.-Y. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[14] T. Ohtou, N. Sugii, and T. Hiramoto, "Impact of parameter variations and random dopant fluctuations on short-channel fully depleted SOI MOSFETs with extremely thin BOX," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 740–742, Aug. 2007.

[15] C. Shin, M. H. Cho, Y. Tsukamoto, B.-Y. Nguyen, B. Nikolić, and T.-J. K. Liu, "SRAM yield enhancement with thin-BOX FD-SOI," *Proc. IEEE Int. SOI Conf.*, Oct. 2009, pp. 1–2.

[16] H. Furuhashi, T. Shino, T. Ohsawa, F. Matsuoka, T. Higashi, Y. Minami, H. Nakajima, K. Fujita, R. Fukuda, T. Hamamoto, and A. Nitayama, "Scaling Scenario of Floating Body Cell (FBC) Suppressing Vth Variation Due to Random Dopant Fluctuation," *Proc. IEEE Int'l SOI Conf.,* 2008, pp. 33-34.

[17] C. Shin, "Advanced MOSFET Designs and Implications for SRAM Scaling," Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., University of California, Berkeley, CA, 2011.

[18] A. Asenov, "Simulation of statistical variability in nano MOSFETs," *VLSI Symp. Tech. Dig.*, Jun. 2007, pp. 86-87.

[19] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub 50 nm MOSFETs: a statistical 3D 'atomistic' simulation study," *IOP Semiconductor Science and Technology*, vol. 10, no. 2, pp. 153-158, Feb. 1999.

[20] M.H. Cho, C. Shin, and T.-J. K. Liu, "Optimization and Variation Studies of BJT-based Ultra Thin Body Capacitorless DRAM Cell," *Int'l Conf. on SSDM*, Sep. 2011. 971-972.

[21] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices. Cambridge, U.K.: Cambridge Univ. Press, 2006.

[22] E. Wu, W. Lai, M. Khare, J. Sune, L.-K. Han, J. McKenna, R. Bolam, D. Harmon, and A. Strong, "Polarity-dependent oxide BD of NFET devices for ultra-thin gate oxide," in *Proc. IEEE IRPS*, 2002, pp. 60–72.

[23] M.H. Cho and T.-J. K. Liu, "Variation Study and Implications for BJT-Based Thin-Body Capacitorless DRAM*,"* *IEEE Electron Device Lett.,* Vol. 33, no. 3, pp. 312-314, Mar. 2012.

[24] International Technology Roadmap for Semiconductors, 2010. Available : http://www.itrs.net.

[25] Sentaurus Process User Guide, Synopsys, Inc., Mountain View, CA, version E-2010.12, Dec. 2010.

[26] Sentaurus Device User Guide, Synopsys, Inc., Mountain View, CA, version D-2010.03, Mar. 2010.

[27] O. Faynot, F. Andrieu, O. Weber, C. Fenouillet-Béranger, P. Perreau, J. Mazurier, T. Benoist, O. Rozeau, T. Poiroux, M. Vinet, L. Grenouillet, J-P. Noel, N. Posseme, S. Barnola, F. Martin, C. Lapeyre, M. Cassé, X. Garros, M-A. Jaud, O. Thomas, G. Cibrario, L. Tosti, L. Brévard, C. Tabone, P. Gaud, S. Barraud, and T. Ernst , "Planar Fully Depleted SOI Technology: a powerful architecture for the 20nm node and beyond," *IEDM Tech. Dig.,* 2010, pp. 3.2.1 - 3.2.4.

[28] W. Schwarzenbach, X. Cauchy, O. Bonnin, N. Daval, C. Aulnette, C. Girard, B.-Y. Nguyen, and C. Maleville, "Ultra-thin film SOI/BOX substrate development, its

application and readiness," *Electrochemical Soc. Trans,* vol. 35, no. 5, pp. 239-245, May. 2011.

[29] F. Matsuoka, T. Ohsawa, I. Higashi, H. Furuhashi, K. Hatsuda, K. Fujita, R. Fukuda, N. Ikumi, T. Shino, Y. Minami, H. Nakajima, T. Hamamoto, A. Nitayama, and Y. Watanabe, "FBC's Potential of $6F^2$ Single Cell Operation in Multi-Gbit Memories Confirmed by a Newly Developed Method for Measuring Signal Sense Margin," *IEDM Tech. Dig.,* 2007, p. 39.

[30] JEDEC: Global Standards for the Microelectronics Industry [Online]. Avalable: http://www.jedec.org

[31] D. Somasekhar, Y. Yibin, P. Aseron, S.-L. Lu, M. M. Khellah, J. Howard, G. Ruhl, T. Karnik, S. Borkar, V. K. De, and A. Keshavarzi, "2 GHz 2 Mb 2T Gain Cell Memory Macro With 128 GBytes/sec Bandwidth in a 65 nm Logic Process Technology," *IEEE J. Solid-State Circuits*, Vol. 44, no. 1, pp. 174-185, Jan. 2009.

[32] K. C. Chun, P. Jain, C.H. Kim, "Logic-compatible embedded DRAM design for memory intensive low power systems," *Proc. IEEE ISCAS*, May 2010, pp. 277 - 280.

[33] C. S. Wang and E. C. K. Chen, "Embedded DRAM Technologies: Comparisons and Design Tradeoffs," Taiwan Semiconductor Manufacturing Company (TSMC) article for EDN, [Online]. Avalable: http://www.tsmc.com

Chapter 6

Positive Feedback SOI Transistor and Its Capacitorless DRAM Application

6.1 Introduction

Dimension scaling and severe short channel effects, such as drain-induced barrier lowering (DIBL), result in substantial increases in leakage current or power consumption. An important issue is power management in the further scaling of complementary metal–oxide–semiconductor (MOS) technology. For the past few decades, low power consumption, higher speed, and scalability of the devices are some of the major goals and concerns for the semiconductor device industry. An obstacle to further scaling of the power supply voltage in a conventional MOS field-effect transistor (MOSFET) is the fundamental limit of subthreshold slope (SS). SS is larger than 60 mV/dec at room temperature [1].

In the search for an alternative device with small SS, a positive feedback (PF) FET on silicon-on-insulator (SOI) is a promising lead in the search for a new transistor [2-4]. Bipolar junction transistor (BJT) operation and impact ionization are used in this device to overcome the subthreshold swing limitation of a conventional MOSFET. SS can be much lower than 60 mV/dec for a PF-FET according to both the theoretical and experimental results. Earlier devices, such as tunneling FET (TFET), Impact Ionization MOS (IMOS), or Feedback FET, have suffered from low values of on-current or asymmetric structures [5-10]. These devices are not compatible with standard CMOS applications.

In this chapter, a thin body SOI transistor with ultra-thin buried oxide (UTBOX) for positive feedback FET has been studied through device simulations with an analytical model. N-channel SOI transistor was fabricated and experimentally measured. It exhibits very steep SS due to positive feedback. This is also demonstrated with planar type SOI structure with silicon oxide gate dielectric, which has simpler processes, compared to other

steep SS devices. Due to the positive feedback operation, PF-FET may have hysteresis characteristics according to device conditions (operation voltage or device structure). Though this hysteresis behavior may be not suitable for logic devices, it is very promising for memory applications, and PF-FET has been researched for capacitorless DRAM [11]. In this study, new operating mode for capacitorless DRAM will be proposed, and longer retention time and larger sensing current are achieved without data collapse.

6.2 Principles

As shown in **Fig. 6.1**, this device structure is a basically planar type SOI transistor. The parasitic BJT can be activated with a back bias operation, which enables the positive feedback effect combined with impact ionization [11, 12].

$$I_D = \frac{M \times I_{ch}}{1 - \beta(M - 1)} \tag{1}$$

Where β is the parasitic BJT gain and M is the impact ionization multiplication factor, the latch occurrence condition is $\beta \times (M-1) \geq 1$ [1, 13]. In previous studies [14-16], the BJT-based capacitorless DRAM requires high operation voltages. However, the drain voltage of PF-FET can be reduced to less than 2 V with the help of impact ionization.

As shown in **Fig. 6.1**, the positive feedback phenomenon appears when both impact ionization in the sub-threshold region and BJT operation occur [11]. An increase of the body potential results from the hole current, which is generated by impact ionization at the drain. The positive body bias influences on the channel current by reducing threshold voltage [1]. More holes are created and injected into the body to further increase body potential. Generated holes also act as base current in parasitic BJT, which enhances the BJT on-current from the gain. The positive feedback loop gain is then larger than unity [2, 3, 12]. MOSFET will latch and the current increases abruptly. Fossum *et al.* reported that weak impact ionization is the dominant factor in triggering positive feedback [12].

In most logic applications, the positive feedback loop is normally restricted because the body factor is too small to result in positive feedback [11]. Though FDSOI has immunity for the body potential variation, back bias with UTBOX can effectively trigger positive feedback.

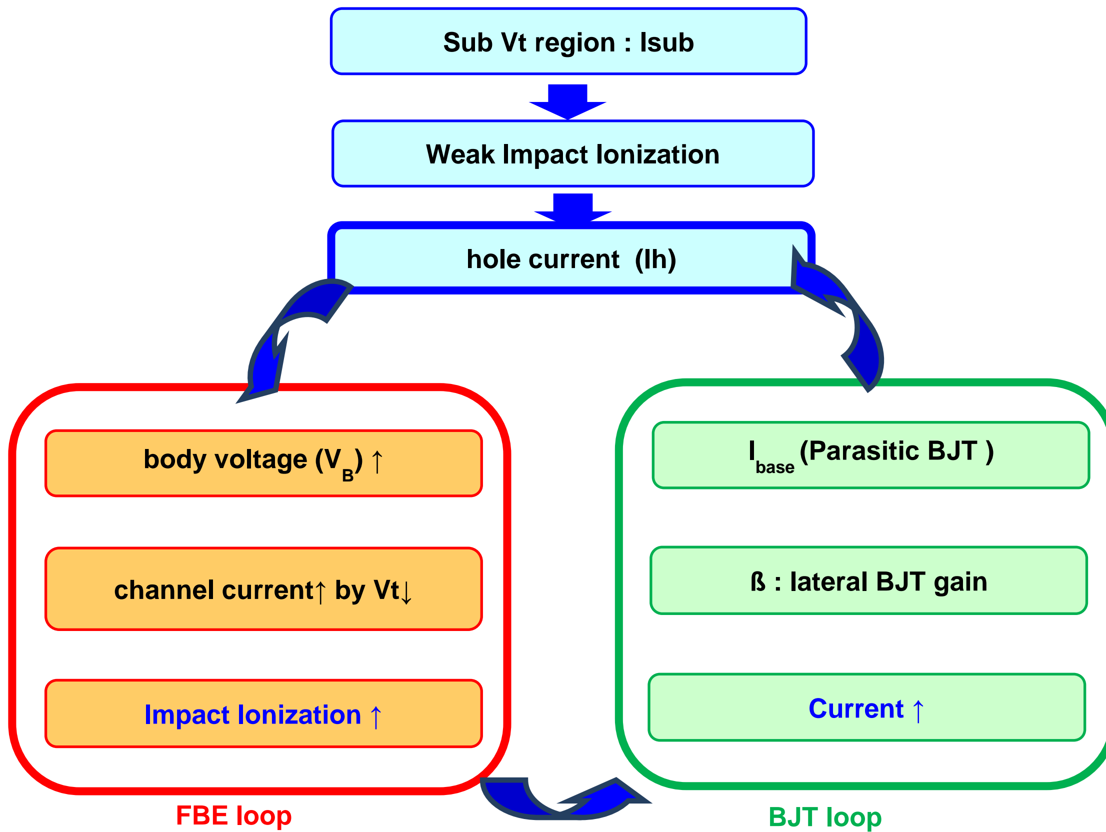


Figure 6.1. Positive feedback flow. Weak impact ionization occurs under the sub-threshold region and holes are generated. These holes are accumulated in the thin body and enhance the floating body effect and the parasitic BJT operation. The two loops give positive feedback to each other and the current abruptly increases.

6.3 Positive Feedback Modeling & Properties

6.3.1 Simulation Modeling

Each model and parameter is explained in chapter 1 in detail. In **Table 2.1**, some of selected parameters are summarized [17]. To account for transfer of energy and lattice heating, the hydrodynamic model is used. Quantum confinement effect and carrier mass are considered with ***Band*** models. Recombination models including impact ionization or band-to-band tunneling (BTBT) are essential to explain feedback effect with BJT and floating body effect. The Poisson equation is solved with other basic physics parameters.

Category	PF FET Models
Hydrodynamics	EnergyRelaxationTime
	EnergyFlux
	HeatFlux
Band	Bandgap Narrowing
	Intrinsic Density
	QW Strain
	e/hDOSMass
	QuantumPotentialParameters
Mobility Models	PhuMob
	StressMobility
Recombination model	Auger
	TrapAssistedTunneling
	Impact Ionization
	Band2BandTunneling
Boundary Conditions	SchottkyResistance
Gate Current Models	All included

Table 6.1. The summary of selected parameters for positive feedback simulation. Each parameter is explained in Sentaurus user guide [17].

6.3.2 Simulated Structure

In order to investigate positive feedback characteristics in transistors, various factors are simulated with Sentaurus [17]. **Table 6.2** and **Fig. 6.2** show the structure dimensions and a cross-section view, respectively. Constant doping concentration in source, drain, and body is used.

Parameter	Value
Gate length (Lg)	52 nm
Gate oxide thickness (T_{ox})	2.5 nm
Body thickness (T_{Si})	10 nm
BOX thickness (T_{BOX})	10 nm
Spacer width (W_{SPACER})	30 nm
Source/Drain dopant concentration	N-type :10^{20} cm^{-3}
Channel dopant concentration	N-type :10^{17} cm^{-3}
Substrate dopant concentration	N-type : 10^{18} cm^{-3}

Table 6.2. Positive feedback transistor (thin body with UTBOX structure) cell design parameters.

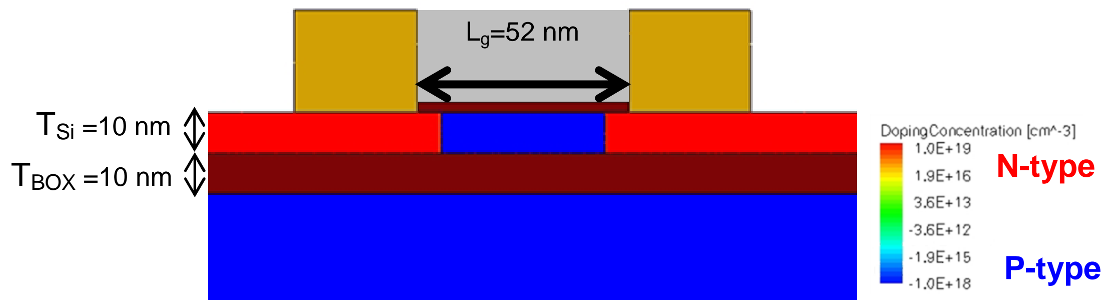


Figure 6.2. Cross-sectional doping contour map (2D).

I_{ds}-V_{gs} (drain current – gate voltage) curve is shown in **Fig. 6.3**. When gate voltage increases from -2 V to 0 V, the current increases abruptly at -0.85 V, which is defined as forward trigger voltage (V_{FT}). As gate voltage is reduced from 0 V to -2 V, the current is still high, even with below V_{TF}. This hysteresis is due to positive feedback. The feedback-loop still exists, and generated holes contribute to the BJT operation in the body. When gate voltage drops below backward trigger voltage (V_{BT}: -1.09 V) positive feedback disappears as a results of very weak impact ionization. The critical voltage induces hysteresis. The difference between V_{FT} and V_{BT} is defined as ***Window*** (hysteresis window).

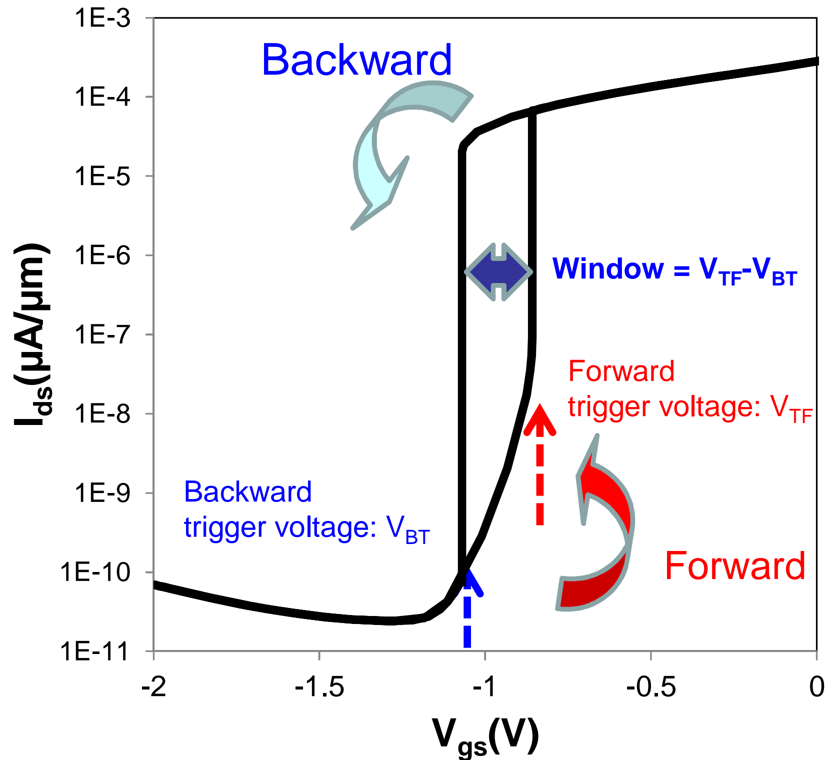


Figure 6.3. I_{ds}-V_{gs} curve with double sweep: hysteresis trend can be observed. **Window** is defined as the voltage difference between forward trigger voltage (V_{FT}) and backward trigger voltage (V_{BT}). V_{ds} =1.55 V, V_{bg} =3 V.

6.3.3 Positive Feedback Characteristics

Though hysteresis is undesirable in logic applications, it can be useful in memory applications. In order to understand positive feedback characteristics, each dimension parameter is investigated. Positive feedback effects are affected by various parameters (T_{OX}, T_{Si}, T_{BOX}, L_g, and V_{ds}) as shown in **Figs. 6.4 ~ 6.13.**

Gate oxide: As shown in **Figs. 6.4** and **6.5**, gate oxide thickness affects the trigger voltages and Windows intensively. The positive feedback effect for typical T_{OX} (gate oxide thickness) develops into the latch. As T_{OX} is increased, a significant Window appears as well as lower V_{FT} and V_{BT} (*i.e.* more negative V_{FT} and V_{BT}). The body effect should be considered when attempting to understand this phenomenon [1]. **Equation** (2) shows

$$r \propto -\frac{dV_T}{dV_{BS}} \propto \frac{C_D}{C_{OX}} \qquad (2)$$

where, C_D is the body depletion capacitance, V_T is threshold voltage, V_{bg} is back bias, and C_{OX} is gate dielectric capacitance. The Window results from impact-ionization charging of the body when the body effect factor is increased to a significant degree [11, 12]. One method of achieving this is by using a thick gate oxide. Thick gate oxide has small C_{OX}, which increases body effect (***r*** in **Equation** (2)). As shown in **Fig. 6.5 (a)**, the thicker gate oxide has lower V_{TF}, which means that it is much easier to activate positive feedback. The V_{TF} is reduced (lower voltage) with T_{OX}, as well (**Fig. 6.5 (b)**). This is desirable for ultra-scaled device technology.

Body thickness: The impact of body thickness is shown in **Figs. 6.6** and **6.7.** As silicon body is thinner, there is less chance to retain holes in thin body, and the positive feedback mechanism is disturbed. Thicker body transistors are advantageous for positive feedback as shown in **Fig. 6.7**.

BOX thickness: The effect of BOX thickness is shown in **Fig. 6.8**. The thin BOX induces higher electric field in the body, which lower the potential barrier from source and reduces V_T. Increased subthreshold current activates impact ionization at the lower gate voltage. As shown in **Fig. 6.9**, trigger voltages and Window increase with thinner BOX (*i.e.* higher electric field from the back gate).

Gate length: Fig. 6.10 shows the impact of gate channel length scaling. For the PF-FET design, gate length is related to BJT gain. The narrow base width (short L_g) has higher gain, which increases the BJT on-current. **Fig. 6.11** shows the scaling effect of the transistor. In scaling technologies, PF-FET is desirable because the short channel device has advantages for embodying PF-FET, as shown in **Fig. 6.11**.

Drain voltage: Figs. 6.12 and **6.13** show drain bias effect on PF-FET. Drain voltage changes the lateral electric field, which affects impact ionization. Because drain induced barrier lowering (DIBL) is effectively suppressed in the thin body SOI transistor, V_T changes slightly [18, 19]. However, increased impact ionization activates positive feedback in the subthreshold region, which lowers V_{TF} and increases the Window.

In **Fig. 6.14 (a)**, the relation between forward trigger voltages (V_{TF}) and Window as related to each dimension are shown. The lower V_{TF} has larger window due to the higher positive feedback effect. Its slope is around -1, which shows the linear relationship between the two parameters. In order to further investigate which parameter is dominant, each slope is compared in **Fig. 6.14 (b)**. Drain voltage has the strongest impact on the Window. In order to secure a wider Window, the drain voltage control is one of the most dominant factors. In other words, for memory application, adjusting the drain voltage is the most effective method.

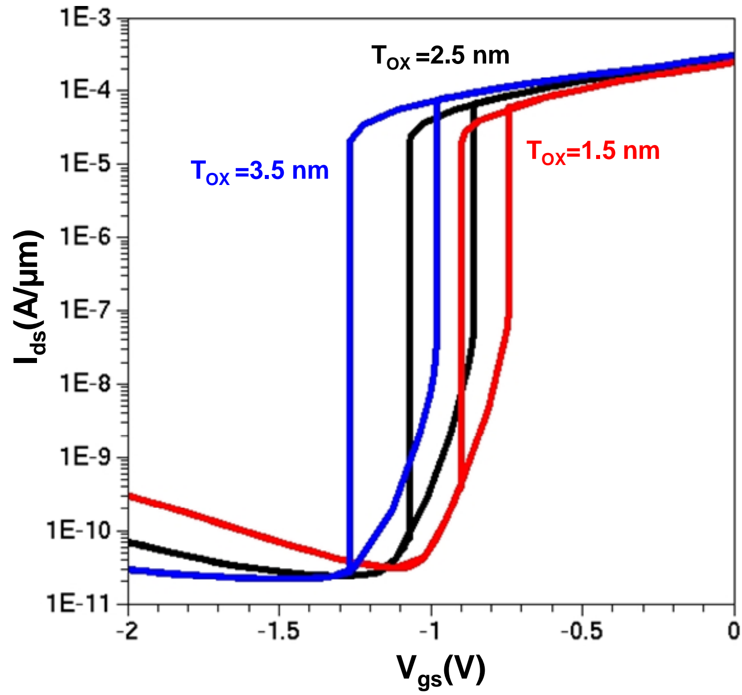


Figure 6.4. I_{ds}-V_{gs} curve with different gate oxide thicknesses (double sweep): hysteresis curves are measured and they have different trigger voltages and Windows.

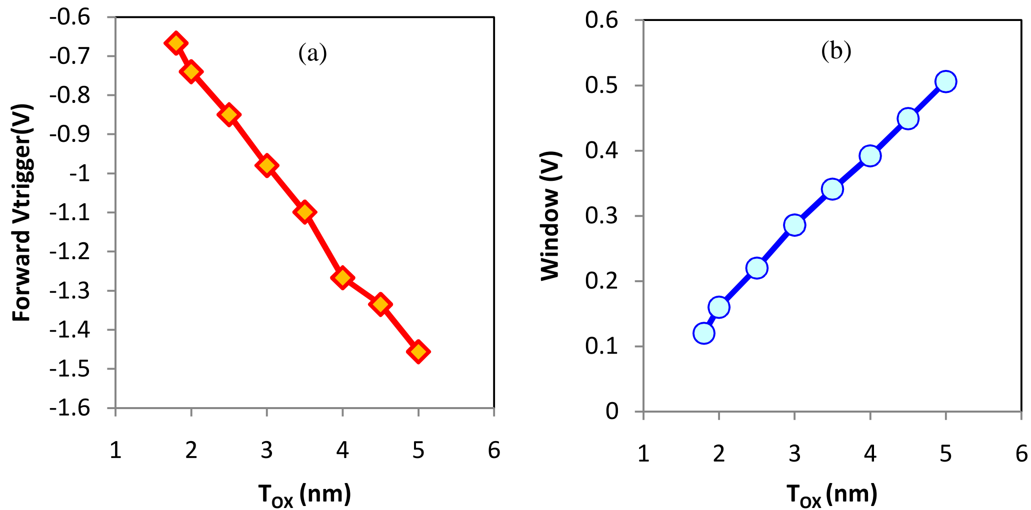


Figure 6.5. (a) Thicker gate oxide transistor has lower V_{TF}. (b) Trigger voltage difference (Window). Thicker gate oxide transistor induces wider Window due to enhanced positive feedback effect.

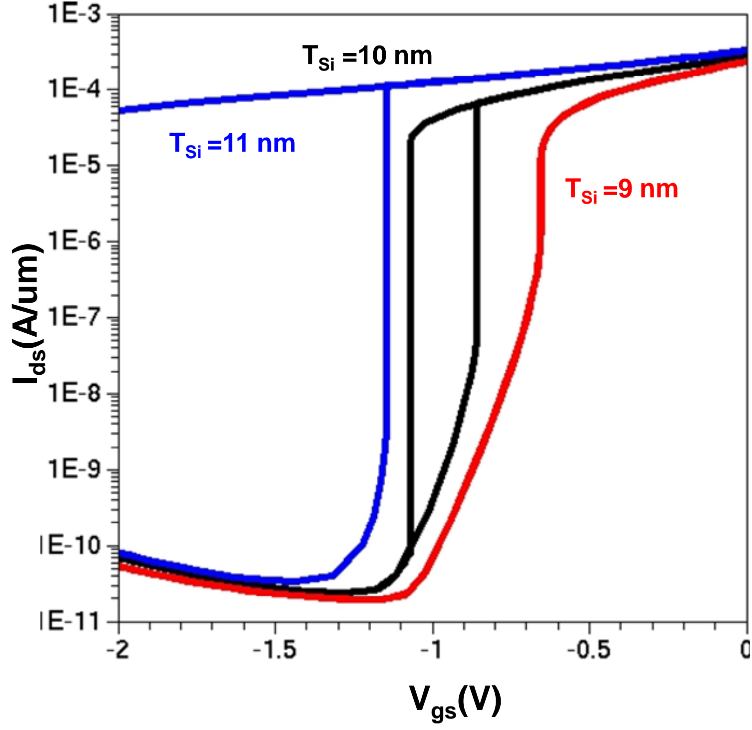


Figure 6.6. I_{ds}-V_{gs} curve with different body thicknesses (double sweep): hysteresis curves are measured and they have different trigger voltages and Windows.

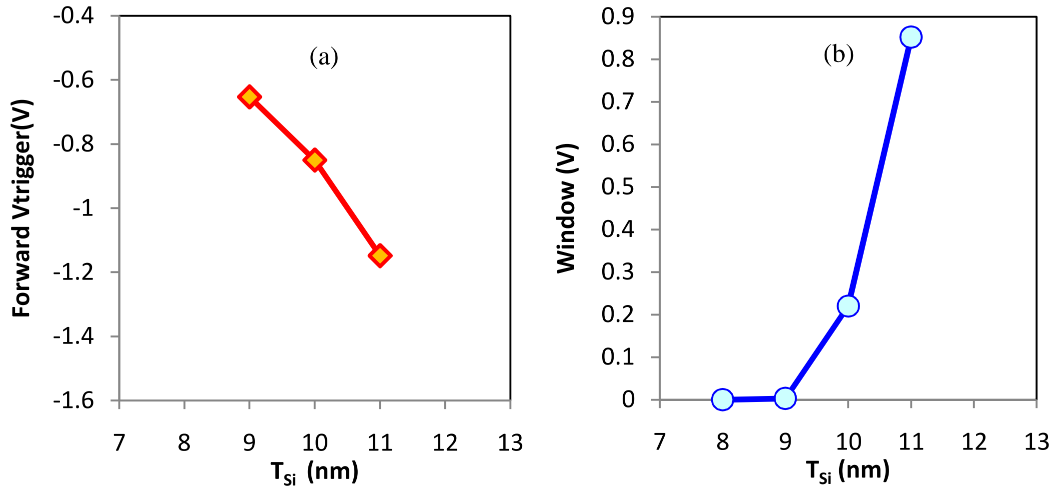


Figure 6.7. (a) Thicker body thickness transistor has lower V_{TF}. (b) Trigger voltage differences (Window). Thicker T_{Si} transistor induces wider window due to enhanced positive feedback effect.

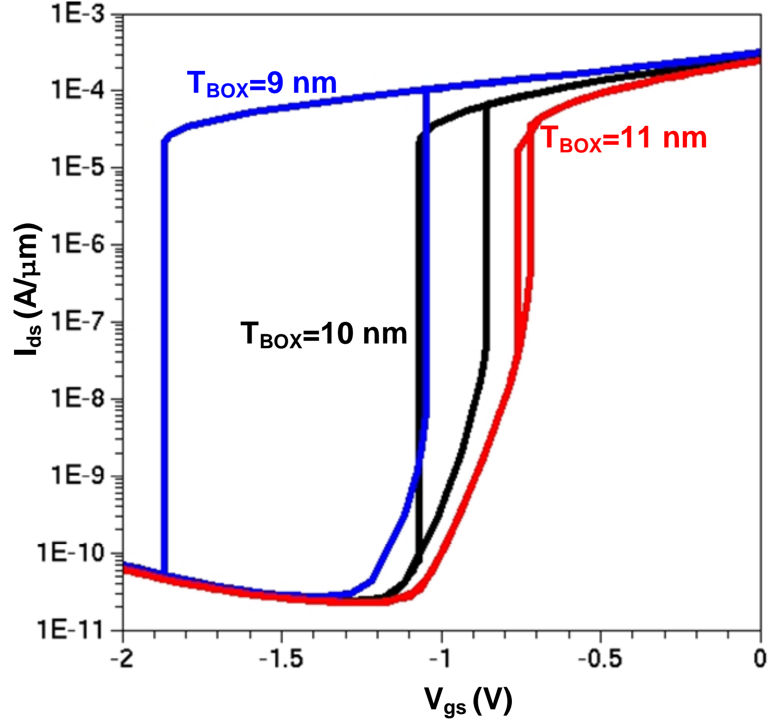


Figure 6.8. I_{ds}-V_{gs} curve with different BOX thicknesses (double sweep): hysteresis curves are measured and they have different trigger voltages and Windows. The thinner T_{BOX} increases window.

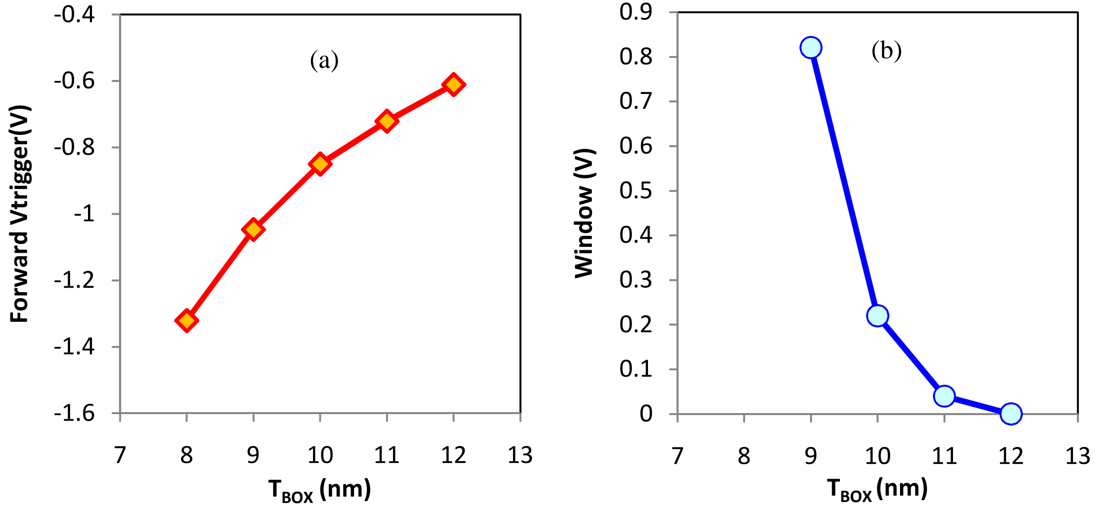


Figure 6.9. (a) Reduced BOX thickness transistor has lower V_{TF}. (b) Trigger voltage difference (Window). Thin BOX transistor induces wider window due to enhanced positive feedback effect.

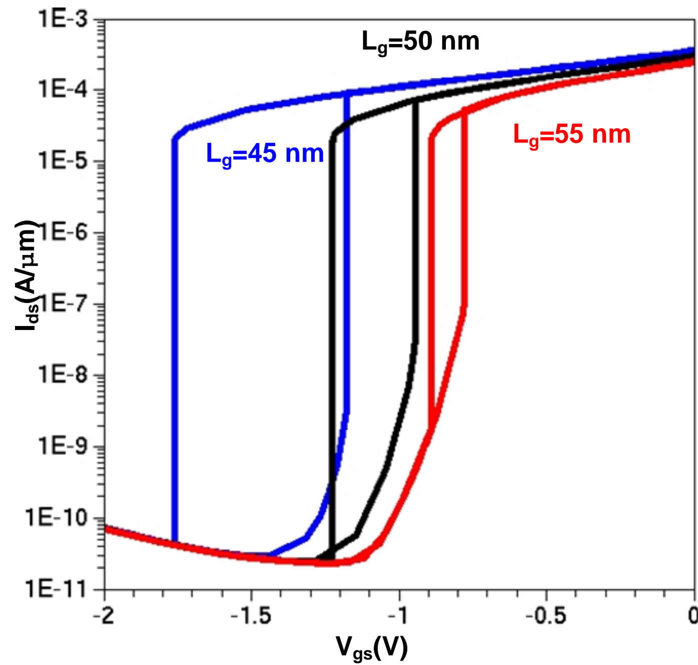


Figure 6.10. I_{ds}-V_{gs} curve with different gate lengths (double sweep): hysteresis curves are measured and they have different trigger voltages and Windows. Because shorter gate length transistor induces higher gain in BJT-based operation, positive feedback is activated easily.

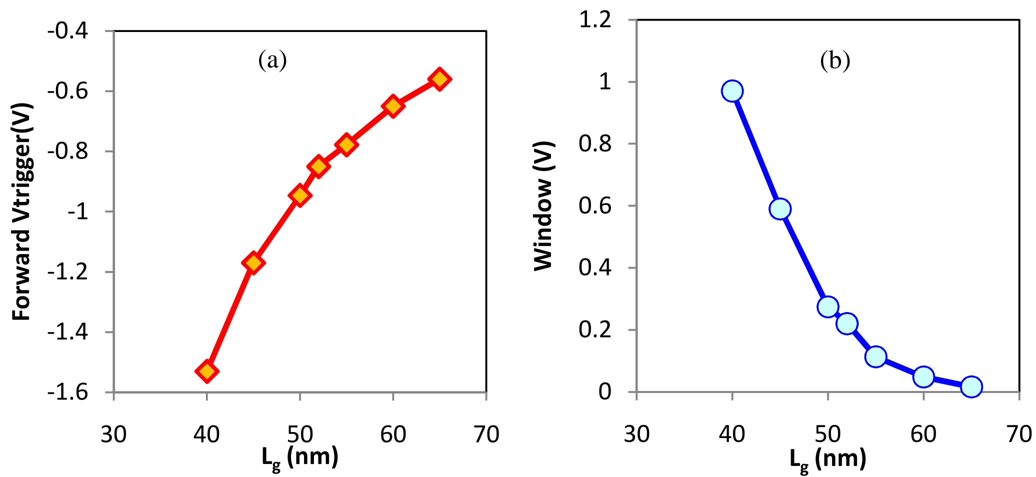


Figure 6.11. (a) Shorter gate length transistors have lower V_{TF} (more negative). (b) Window (trigger voltage difference). Short gate length transistor induces wider window due to the enhanced positive feedback effect.

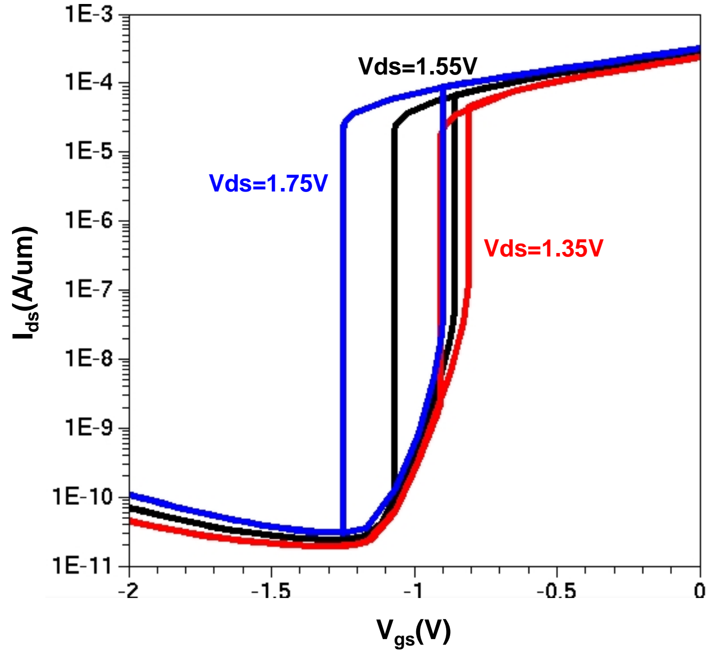


Figure 6.12. I_{ds}-V_{gs} curve with different drain voltages (double sweep): hysteresis curves are measured and they have different trigger voltages and Windows. Higher drain voltage increases electric field in lateral direction, which increases impact ionization and activates positive feedback.

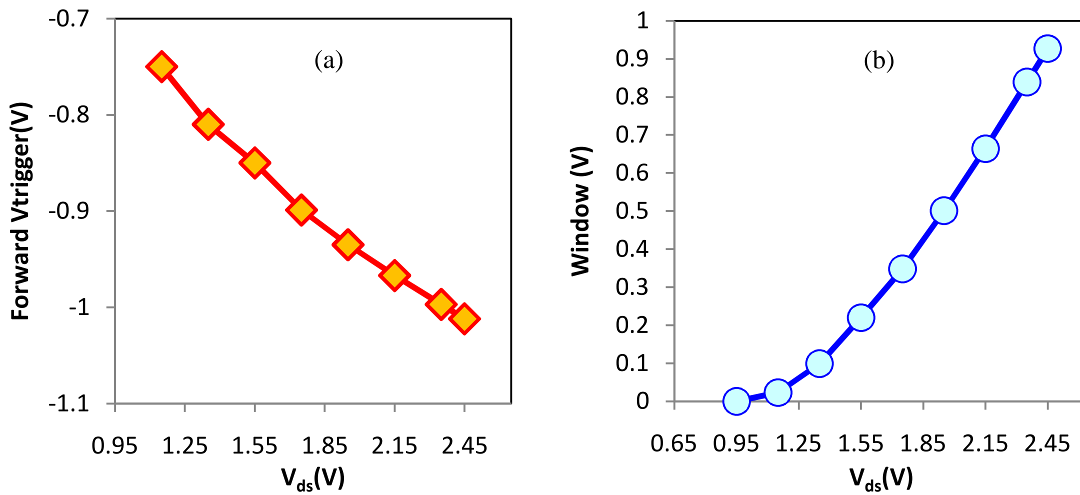


Figure 6.13. (a) Higher drain voltages have lower V_{TF} (more negative). (b) Window (trigger voltage difference). Increased lateral electric field induces wider Window due to the enhanced positive feedback effect.

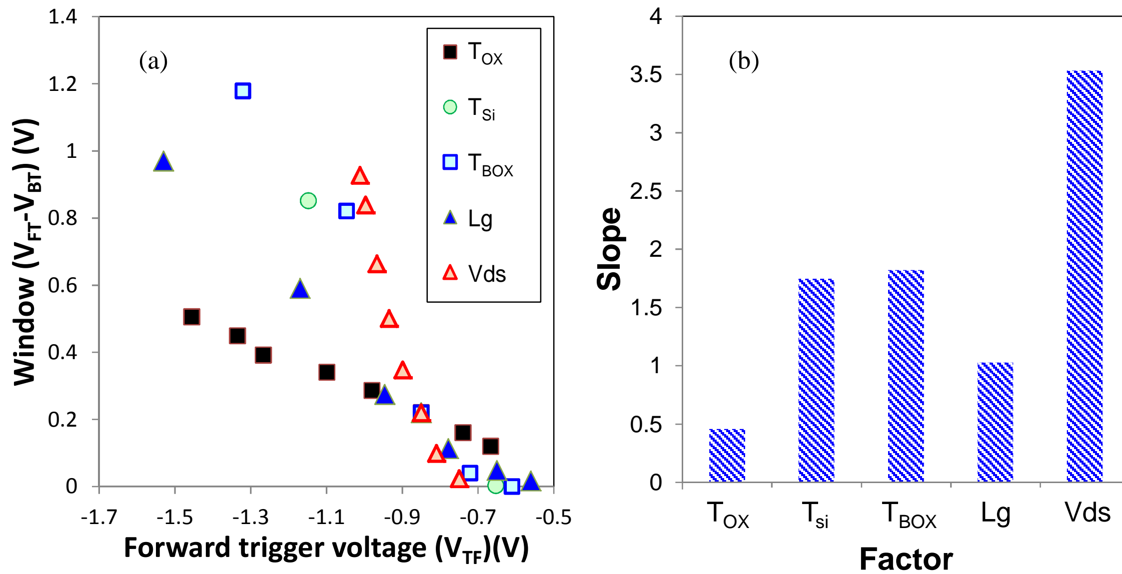


Figure 6.14. (a) The relation between V_{TF} and Window. PF-FETs with low V_{TF} have wider Window. (b) Slopes for each factor.

6.4 Device Structure and Fabrication

The N-channel PF-FETs were fabricated on thin body SOI wafer with a 10 nm buried oxide. In order to isolate the transistors, a modified Shallow Trench Isolation (STI) process was used. The ground plane doping implantation (GP) though 7 nm oxide has been done (Boron: 40 keV, 1×10^{13} dose/cm^2, Boron: 60 keV and 4×10^{13} dose/cm^2, and both with a tilt 7 deg). Post implant Anneal was 1000 ℃ and 30 s. The purpose of this doping was to place GP under the BOX, but the tail of the implant may be still in the channel. A gate stack with 2.5 nm SiO_xN_y and 5 nm TiN, capped with 100nm poly Si was used. Extensions were implanted with As 2 keV and 1×10^{15} dose/cm^2 (implanted through 5 nm SiO_2). There was no pocket doping process. After the extension implant, the gate sidewall nitride spacers were formed and selective epitaxial growth (raised source and drain) was formed to decrease the source/drain resistance. The source/drain implants implanted after selective epitaxial growth with Phosphorus: 8 keV and 2×10^{15} dose/cm^2, and it was annealed with a spike temperature profile (1050 ℃). After the junction annealing, $NiPt_x$ was used as a salicide. The physical gate length is 52 nm and **Fig. 6.15** shows the cross-section view in each dimension. The schematic presentation of the process flow is shown in **Fig. 6.16**.

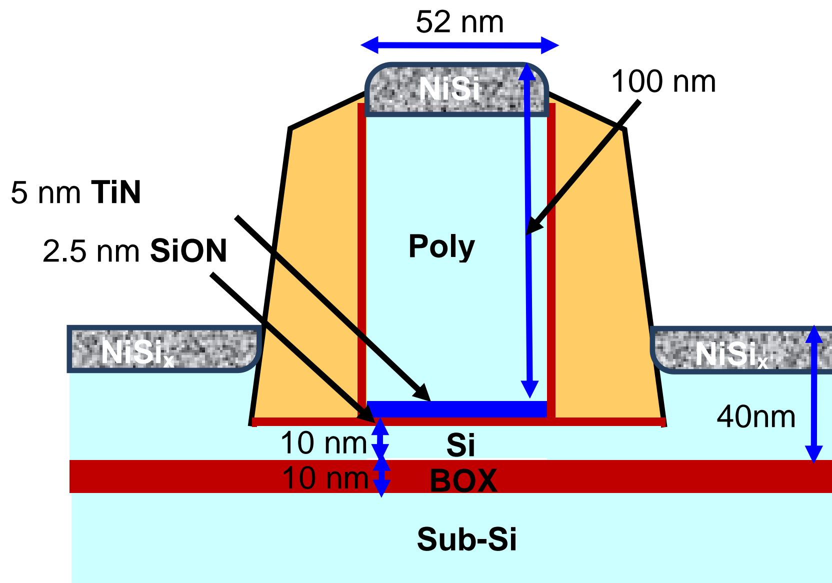


Figure 6.15. Cross-section view of a thin body SOI with UTBOX device; T_{BOX}=10 nm; T_{OX}=2.5 nm SiO_xN_y, 5 nm TiN, 10 nm Si film, and T_{Si} =10 nm devices are fabricated (courtesy of IMEC and SOITEC).

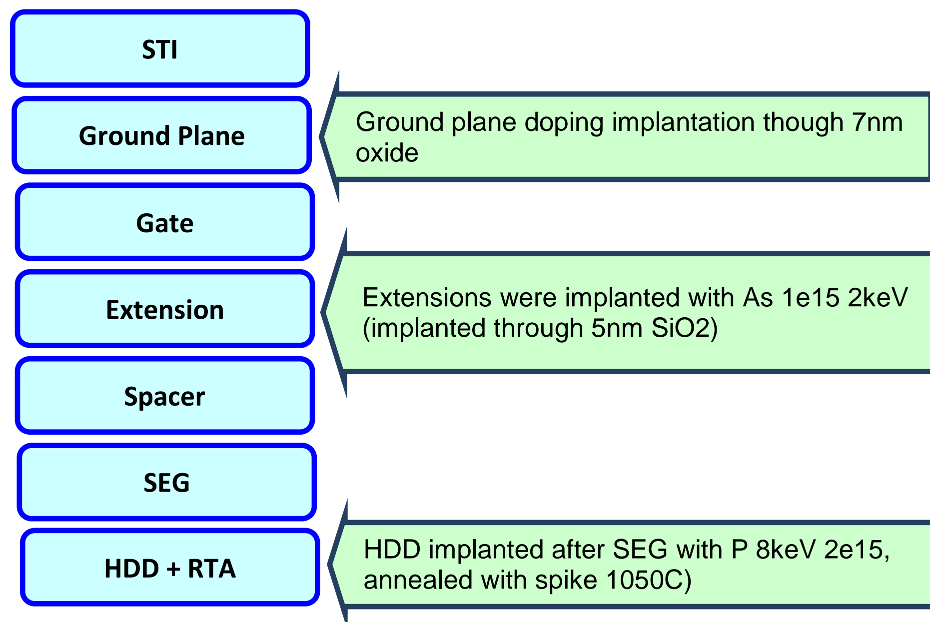


Figure 6.16. Process flow of device fabrication (courtesy of IMEC and SOITEC)

6.5 Measurement Configuration

The I-V (Drain current *vs.* Voltage) characteristics of the transistor are measured with a parameter analyzer (Agilent B1500A). The capacitorless DRAM needs AC transient measurement using pulse generator because the DC parameter analyzer is insufficient to measure small signal. The measurement setup consists of a pulse generator (Agilent), an oscilloscope (Tektronix DPO 2024), the parameter Analyzer (Agilent B1500A, HP 4145), a resistance decade box, and four-terminal probe station. In order to minimize issue of reflecting, 50 Ω resistors are attached at each equipment node. 50 Ω resistor is added to the source of transistor. The voltage drop is measured and converted into current [14, 23]. Finally, the transient characteristics of single capacitorless DRAM cell are evaluated using the test system shown in **Fig. 6.17**. It is measured at room temperature.

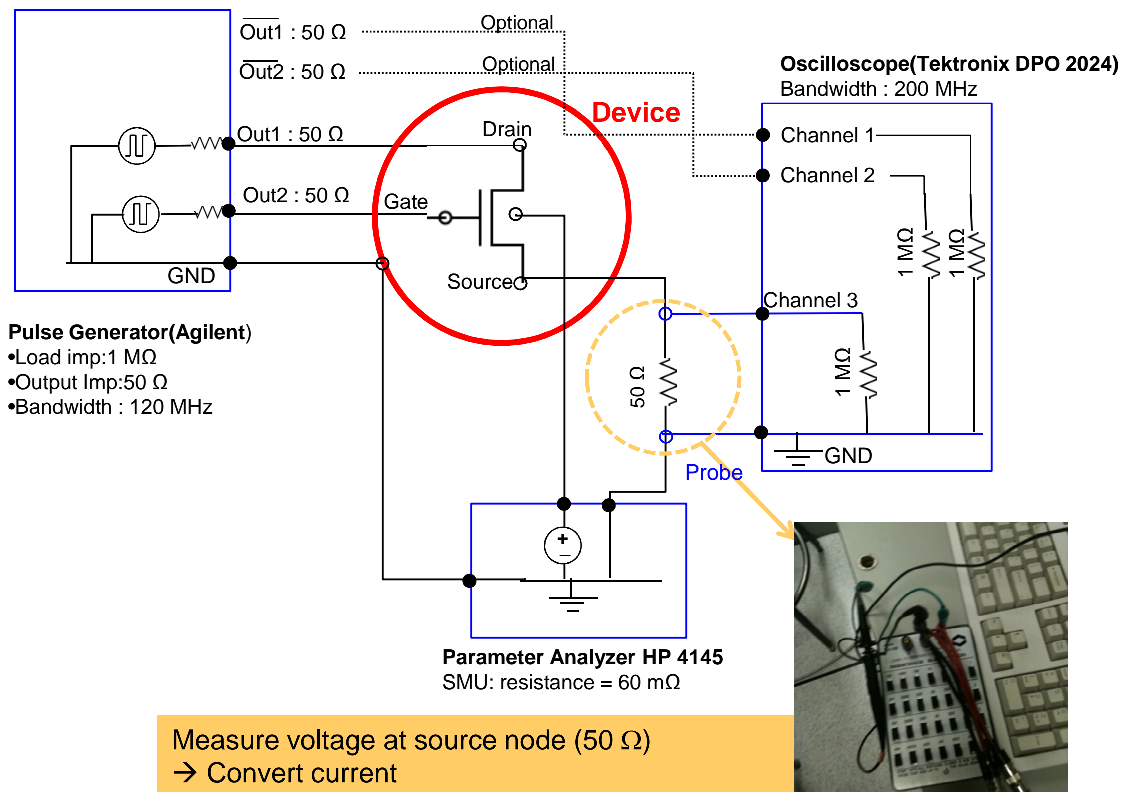


Figure 6.17. The measurement setup. Drain current can be extracted precisely by measuring the voltage drop at the resistor in source node.

6.6 Experimental I-V Characteristics

Fig. 6.18 shows the I_{ds}-V_{gs} curve of the PF-FET. Device and measurement conditions are: physical gate length= 52 nm, channel width= 1 µm, back bias (V_{bg}) = 3 V, and drain voltage (V_{ds}) = 1.55 V. The subthreshold slope (SS) is observed as 0.03 mV/dec, which is one of the smallest measured SS for modern steep transistors [2-13]. The forward trigger gate voltage is -0.85 V. As Fossum et al. reported, impact ionization plays a key role for triggering positive feedback [12]. In order to adjust gate trigger voltage to a reasonable range (around -1 V), the drain bias should be selected carefully. Trigger voltage is affected by drain voltage (V_{ds}), as shown in **Fig. 6.19**. At lower V_{ds} (< 1.2 V), there is no positive feedback because of very weak impact ionization. Over 1.4 V drain bias, the current increases abruptly. With higher V_{ds} (> 1.4 V) the positive feedback is more activated and the trigger voltage moves to further into negative numbers, which means that positive feedback is dominant even with low gate bias.

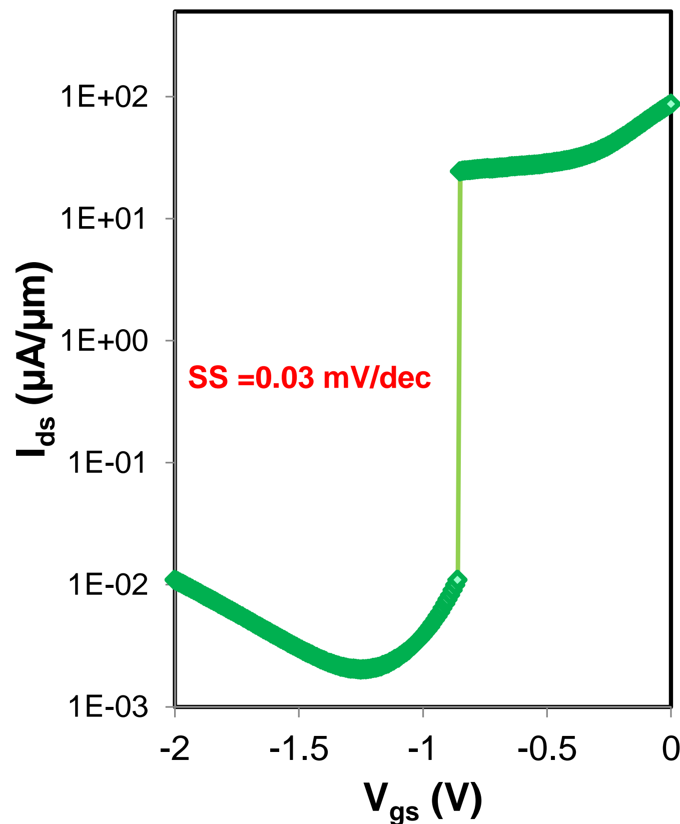


Figure 6.18. I_{ds}-V_{gs} curve. Very steep SS (0.03 mV/dec) is achieved. L_g=52 nm, Width=1 µm, V_{bg}=3 V, and V_{ds}=1.55 V.

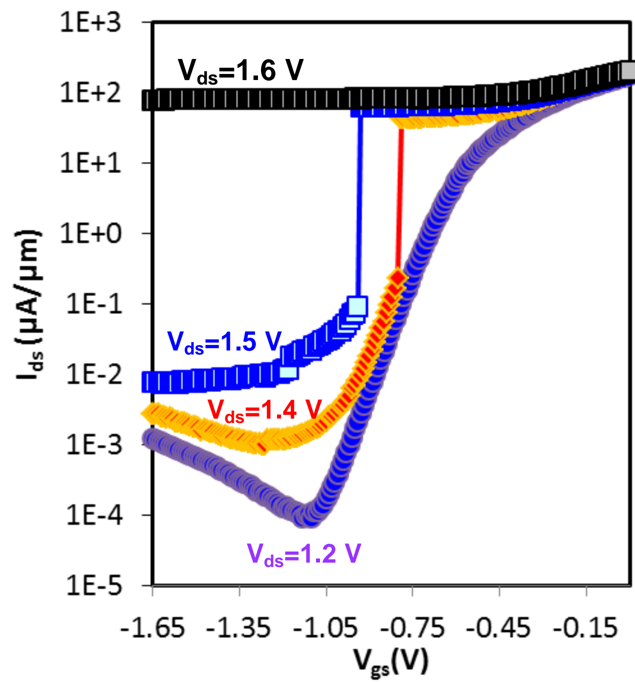


Figure 6.19. I_{ds}-V_{gs} curve with various V_{ds}. L_g= 52 nm, width= 1 µm, V_{bg}= 4 V

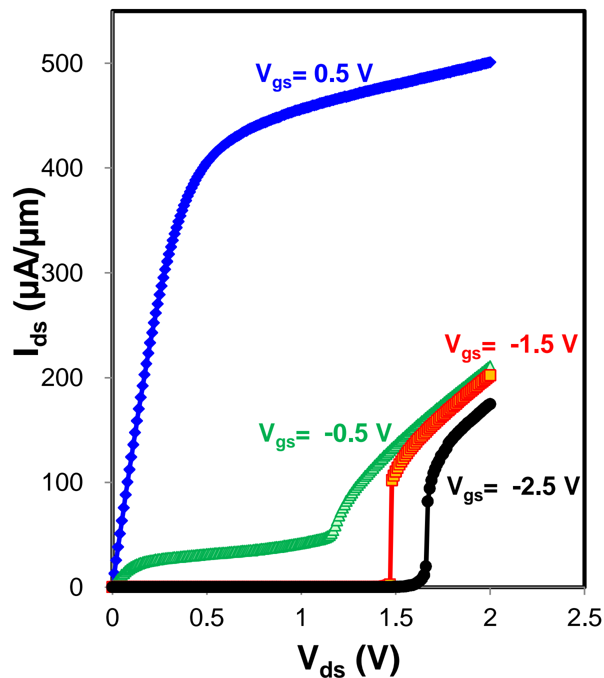


Figure 6.20. I_{ds}-V_{ds} curves at various V_{gs}. L_g= 52 nm, width= 1 µm, V_{bg}= 4 V.

Fig. 6.20 shows the family of I_{ds}-V_{ds} (drain current – drain voltage) for PF-FET as V_{gs} is varied. The I_{ds}-V_{ds} current behaves according to traditional I_{ds}-V_{ds} characteristics and the on-current is large under positive V_{gs}. When negative gate bias (< -1.5 V) is applied to the transistor, on-current is reduced. Transistor has a chance to occur positive feedback because positive feedback is triggered by the combination of ***BJT operation*** and ***weak impact ionization*** in the subthreshold region.

6.7 Capacitorless DRAM Application

Due to the Window (hysteresis window in I_{ds}-V_{gs}), PF-FET can be utilized to store data for capacitorless DRAM (memory applications). The wider Window is an essential factor for high sensing margin in DRAM. In this study, new operating conditions are proposed, as shown in **Fig. 6.21**. In order to erase data (Write 0), gate voltage is set as less than -1.1V. -1.5V is proper voltage to remove all stored data. If gate voltage is higher than -0.85, data is recorded and current is high enough to be on-current. The Read condition is placed inside the gate window voltages (between -1.1 and -0.85 V). When the transistor is in state of Data 1, positive feedback is running inside the body. Though gate voltage is lowered than V_{TF} (-0.85 V in **Fig. 6.21**), the current is still high (D1 state). Interestingly, the Read process has a self-refreshment property. The cell does not lose any data during the Read operation. The data, moreover, is refreshed, which means that the Read operation acts like Write operation.

The operation conditions are summarized in **Table 6.3**. In the operation, the drain current of Write 0 (erase) is very small as shown in **Fig. 6.21**. In conventional operating mode, forward bias is normally applied to drain (negative bias on drain) in order to remove holes in the body (erase operation; Write 0) [11, 23]. Although this is very effective in sweeping holes away, the forward current is so high (> half of Write 1 current). It induces unnecessary power consumption in capacitorless operation. In this study (**Fig. 6.21** and **Table 6.3**), holes are removed by turning off positive feedback operation in the body. Therefore, Write 0 current is negligible.

Fig. 6.22 shows the plots for sensing current *vs.* Hold time. The operating processes are Write 1 → Hold → Read 1→ Hold → Write 0 → Hold → Read 0→ Hold. Each step has the same duration time. It is measured at room temperature. As shown in **Figs. 6.22 (a)** and **(b)**, the Write 0 current is very small, as mentioned above. Both Write and Read currents do not collapse with Hold time, which is due to self-refreshment mechanism. The retention characteristics are shown in **Fig. 6.23**. The measured retention time is more than 4 s, which is one of longest retention times ever reported [2-14]. The sensing margin (the difference between Read 1 and Read 0) is 62 μA/μm.

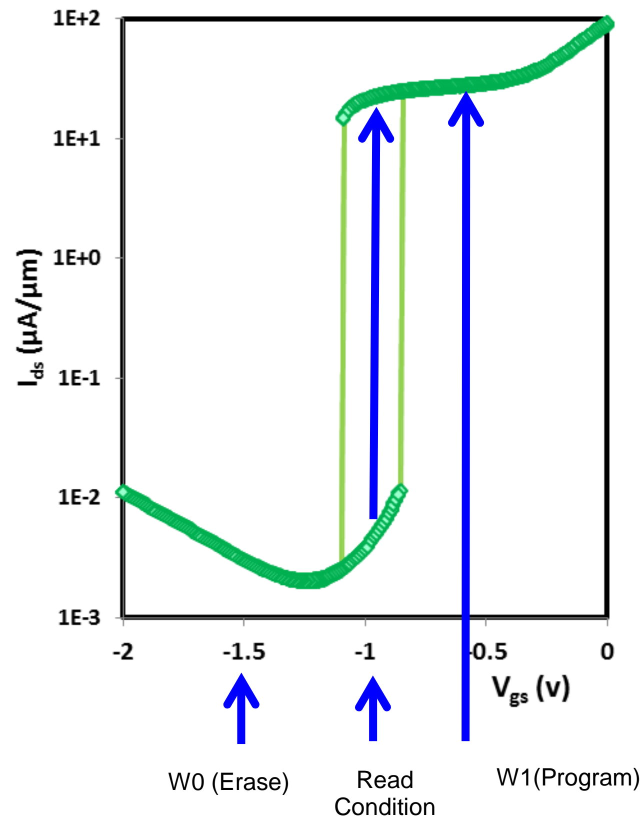


Figure 6.21. Capacitorless DRAM operating conditions are selected based on I-V hysteresis curve. V_{ds}= 1.55 V and V_{bg}= 3 V.

	Write 1 (program)	Write 0 (Erase)	Hold	Read
V_{gs} (V)	-0.65	-1.55	-1.55	-1.1
V_{bg} (V)	3	3	3	3
V_{ds} (V)	1.55	0	1.55	1.55
V_s (V)	0	0	0	0

Table 6.3. PF-FET capacitorless DRAM cell biasing conditions (Volts)

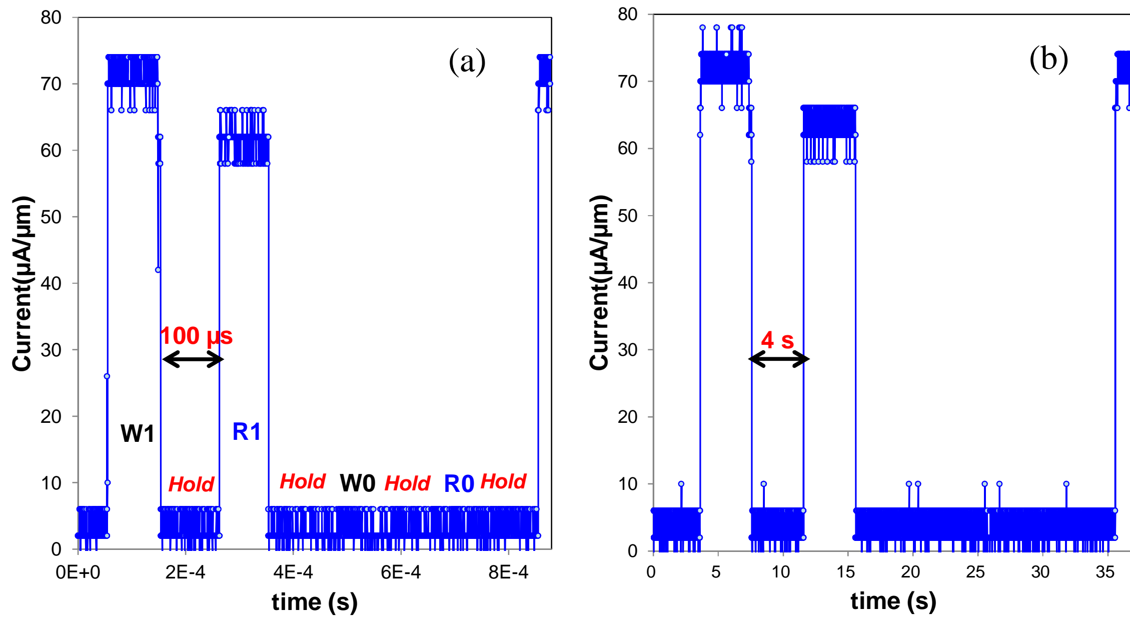


Figure 6.22. Sensing current *vs.* Hold time plots for capacitorless DRAM operation. (a) Retention time is 100 μs, and (b) retention time is 4 s. Write 0 current is negligible. Even with 4 s Hold time, the data does not degrade.

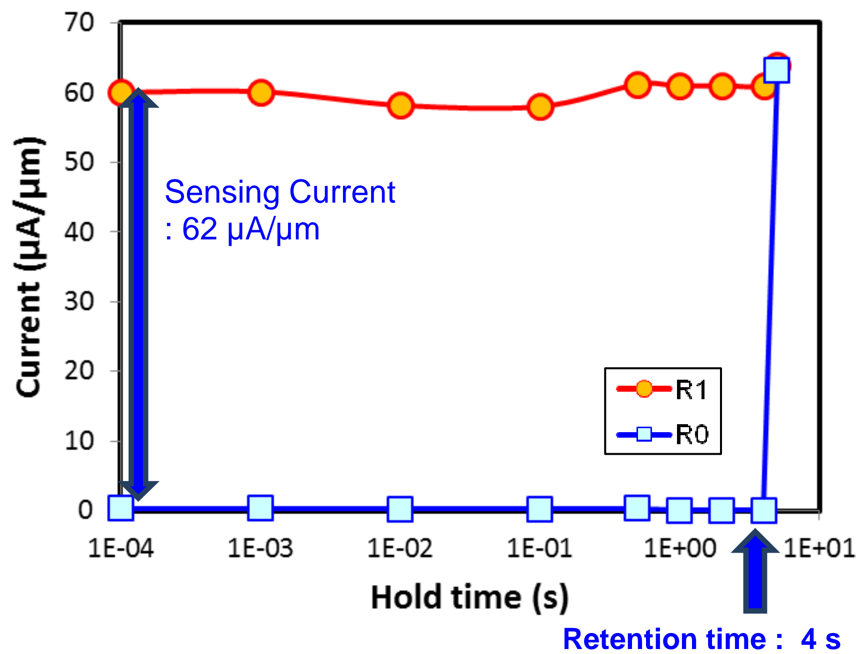


Figure 6.23. Retention characteristics of PF-FET capacitorless DRAM. Measured sensing current is 62 μA/μm and retention time is longer than 4 s.

6.8 Summary

Positive feedback occurs as a result of both BJT operation and floating body effect from weak impact ionization. In order to achieve steep sub-threshold slope, these operations should be under the sub-threshold region. Positive feedback properties are investigated with a simulation (Sentaurus). The proper models and physics are selected for matching simulation results with measured data. Various dimension factors are simulated, such as drain voltage, gate oxide, body thickness, BOX thickness, and gate length. Because the body factor and the BJT gain are determined by dimension factors, the *Window* (hysteresis window) and trigger voltages change. The control of drain voltage is one of the major factors that affect significantly positive feedback properties. The device was fabricated on thin body (10 nm) and thin BOX (10 nm) SOI structure. It exhibits very steep SS of 0.03mV/dec, which is one of the best results ever achieved. Positive feedback and wide Window are measured, which enables the PF-FET to be memory applications. The PF-FET capacitorless DRAM characteristics are measured experimentally. Due to self-refreshment in PF-FET, there is no data collapse during Read operation. The sensing margin is 62 μA/μm and retention time is greater than 4 s. These results suggest that PF-FET is very promising for capacitorless DRAM applications.

6.9 References

[1] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices. Cambridge, U.K.: Cambridge Univ. Press, 2006.

[2] J. G. Fossum, R. Sundaresan, and M. Matloubian, "Anomalous subthreshold current—Voltage characteristics of n-channel SOI MOSFET's," *IEEE Electron Device Lett.*, vol. 8, no. 11, pp. 544–546, Nov. 1986.

[3] J-Y. Choi and J. G. Fossum, "Analysis and Control of Floating-Body Bipolar Effects in Fully Depleted Submicrometer SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1384-1391, Jun. 1991.

[4] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, J. G. Fossum, L. Altimime, and M. Jurczak, "Realizing Super-Steep Subthreshold Slope with Conventional FDSOI CMOS at Low-Bias Voltages," *IEDM Tech. Dig.*, Dec. 2010, pp. 16.6.1-3.

[5] W.Y Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743-745, Aug. 2007.

[6] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 178-179.

[7] F. Mayer, C. L. Royer, G. L. Carval, L. Clavelier, and S. Deleonibus, "Static and Dynamic TCAD Analysis of IMOS Performance: From the Single Device to the Circuit," *IEEE Trans. Electron Devices*, vol. 53, no. 08, pp. 1852-1857, Aug. 2006

[8] C. Onal, R. Woo, H.-Y. S. Koh, P. B. Griffin, and J. D. Plummer, "A Novel Depletion-IMOS (DIMOS) Device With Improved Reliability and Reduced Operating Voltage," *IEEE Electron Device Lett.*, vol. 30, no. 1, pp. 64-67, Jan. 2009.

[9] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T.-J. K. Liu, "Feedback FET: A Novel Transistor Exhibiting Steep Switching Behavior at Low Bias Voltages," *IEDM Tech. Dig.*, Dec. 2008, pp. 1-4.

[10] C. W. Yeung, A. Padilla, T.-J. K. Liu, and C. Hu, "Programming characteristics of the steep turn-on/off feedback FET (FBFET)," *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 176-177.

[11] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, W. Schwarzenbach, O. Bonnin, K. K.Bourdelle, B.-Y. Nguyen, C. Mazure, L. Altimime, and M. Jurczak, "A Novel Low-Voltage Biasing Scheme for Double Gate FBC Achieving 5s Retention and 10^{16} Endurance at 85ºC," *IEDM Tech. Dig.*, Dec. 2010, pp. 12.3.1-4.

[12] J. G. Fossum and Z. Lu, "Anomalous Floating-Body Effects in SOI MOSFETs: Low-Voltage CMOS?," *IEEE International SOI Conference,* Oct. 2011, pp. 1-2.

[13] D.-I. Moon, S.-J. Choi, J. W. Han, S. Kim, and Y.-K. Choi, "Fin-Width Dependence of BJT-Based 1T-DRAM Implemented on FinFET," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 909–911, Sep. 2010.

[14] K.-W. Song, H. Jeong, J.-W. Lee, S. I. Hong, N.-K. Tak, Y.-T. Kim, Y. L. Choi, H. S. Joo, S. H. Kim, H. J. Song, Y. C. Oh, W.-S. Kim, Y.-T. Lee, K. Oh, and C. Kim, "55 nm Capacitor-less 1T DRAM Cell Transistor with Non-Overlap Structure," *IEDM Tech. Dig.*, Dec. 2008, pp. 1-4.
[15] M.H. Cho, C. Shin, and T.-J. K. Liu, "Convex Channel Design for Improved Capacitorless DRAM Retention Time," *IEEE International conference on simulation of semiconductor processes and devices (SISPAD)*, Sep. 2009, pp. 1-4.
[16] H. Jeong, K.-W. Song, I. H. Park, T.-H. Kim, Y. S. Lee, S.-G. Kim, J. Seo, K. Cho, K. Lee, H. Shin, J. D. Lee, and B.-G. Park, "A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell)," *IEEE Trans. Nanotechnology*, vol. 6, no. 3, pp. 352-357, May. 2007.
[17] Sentaurus Device User Guide, Synopsys, Inc., Mountain View, CA, Version D-2010.03, Mar. 2010.
[18] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B.-Y. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.
[19] C. Shin, M. H. Cho, Y. Tsukamoto, B.-Y. Nguyen, B. Nikolić, and T.-J. K. Liu, "SRAM yield enhancement with thin-BOX FD-SOI," *Proc. IEEE Int. SOI Conf.*, Oct. 2009, pp. 1–2.
[20] N. Xu, Ph.D. dissertation, Univ. California Berkeley, Berkeley, CA, May 2012.
[21] A. Cros, K. Romanjek, D. Fleury, S. Harrison, R. Cerutti, P. Coronel, B. Dumont, A. Pouydebasque, R. Wacquez, B. Duriez, R. Gwoziecki, F. Boeuf, H. Brut, G. Ghibaudo, T. Skotnicki, "Unexpected mobility degradation for very short devices : A new challenge for CMOS scaling," *IEDM Tech. Dig*., Dec. 2006, pp. 1-4.
[22] S. Severi, L. Pantisano, E. Augendre, E. S. Andrés, P. Eyben, and K. De Meyer, "A Reliable Metric for Mobility Extraction of Short-Channel MOSFETs," *IEEE Transactions on Electron Devices,* Vol. 54, no. 10, 2007, pp. 2690-2698.
[23] T.-S. Jang, J.-S. Kim, S.-M. Hwang, Y.-H. Oh, K.-M. Rho, S.-J. Chung, S.-O. Chung, J.-G. Oh, S. Bhardwaj, J. Kwon, D. Kim, M. Nagoga, Y.-T. Kim, S.-Y. Cha, S.-C. Moon, S.-W. Chung, S.-J. Hong, and S.-W. Park, "Highly scalable Z-RAM with remarkably long data retention for DRAM application," *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 234-235.

Chapter 7

Conclusion

7.1 Summary and Conclusion

In this dissertation, capacitorless DRAM cells with thin body and ultra-thin buried oxide (UTBOX) structure are investigated. Conventional DRAM cells generally suffer from scaling issues below 20 nm half pitch [1]. It is harder to build a capacitor with a small area having sufficient capacitance to provide high enough signal-to-noise ratio, as compared with transistor scaling. Capacitorless DRAM is a promising solution to issues of cell-area scalability and process complexity in conventional DRAM. As rapid development in transistor-scaling continues, thin-body silicon-on-insulator (SOI) transistor with UTBOX is one of the leading candidates for future devices. Short channel effects and V_T variation can be surmounted in a thin body and UTBOX structure [2]. This dissertation makes progress in proposing and answering the following questions: First, what is the failure mechanism in capacitorless DRAM? Second, how can capacitorless DRAM be improved based on failure mechanism studies? Third, what is the ultimate scaling limit considering variation factors? At the end of study, a novel operating concept of capacitorless DRAM using positive feedback FET (PF-FET) is proposed and investigated.

In chapter 2, the peak substrate doping concentration is investigated in order to optimize the tradeoff between increasing sensing margin and degraded retention time. Because the UTBOX structure is a back-gated fully depleted SOI transistor, the impact of substrate doping on capacitorless DRAM cell performance should be considered. A MOSFET-based operation (MOSFET mode [3]) is utilized in capacitorless DRAM cells. **10^{18} cm^{-3}** of substrate doping concentration is selected as the optimized condition in terms of performance (retention time/sensing current) and variation factors (random dopant fluctuation effect (RDF) of substrate). A novel concept - a **selective well structure** - is

proposed to reduce the peak electric field at the source/drain junctions. P-well underneath only the channel region structure improves retention time by ~9% for 25 nm gate length.

A capacitorless DRAM cell design with bipolar junction transistor (BJT)-based operation (BJT mode) is known to have larger sensing margins and longer retention times [4] and is widely researched [5-6]. In the BJT mode, a thick gate oxide of greater than 3 nm should be used in order to mitigate gate oxide reliability issues. Controlling band-to-band tunneling (BTBT) leakage related to the electric field plays a key role in limiting retention time. **D0 failure** limits the retention time in BJT-based capacitorless DRAM cells. Gate-sidewall spacer width and operating voltages are optimized to reduce BTBT leakage. With the underlap between the front gate and the source/drain regions, retention time as long as **1 second** (s) can be attainable for a cell with 25 nm gate length.

Variability in the capacitorless DRAM cell is investigated in chapter 4. Variations in body thickness (T_{Si}), front gate oxide thickness (T_{OX}), gate-sidewall spacer width (W_{spacer}), buried oxide thickness (T_{BOX}), and RDF are selected as the sources of variability. The **shielding effect** of holes alleviates front electric field fluctuations from the gate oxide variation. The BJT mode is most sensitive to variations in both body and buried oxide thicknesses. In order to qualify variability, the sigma sensitivity and signal sense margin metric are introduced. The retention time of a 25 nm gate length design is reduced by approximately **63 %**, from 1.01 s to 0.364 s at room temperature.

In chapter 5, the scaling limits of the thin-body SOI with UTBOX capacitorless DRAM are investigated through the analysis of dimension variables. Due to reduced hole density, the sensing current is negligible in body thickness below 7 nm. Optimized conditions are achieved for each scaled device under **constant electric field**. Scaling limitations due to variability are investigated based on analysis methods described in chapter 4. Design parameters (W_{spacer}, T_{Si}, T_{BOX}, and T_{OX}) and RDF are considered variation factors, as well. SSM analyses indicate that ultimate scaling limit is **13 nm** for e-DRAM applications (1 ms retention time assumed). Stand-alone DRAM applications need gate lengths longer than **16.5 nm**.

In chapter 6, PF-FET is investigated using simulations and experimental measurements. Positive feedback occurs as a result of both the BJT operation and the floating body effect that occurs as a result of weak impact ionization. The **Window** (hysteresis window) and trigger voltages are affected by physical dimension factors and voltages. The control of drain voltage is one of the most influential factors to significantly affect positive feedback properties. The device was fabricated on thin body (10 nm) and thin BOX (10 nm) SOI structure. It exhibits very steep subthreshold slope of **0.03 mV/dec**, which is one of the best results ever achieved in steep subthreshold slope devices [7-10]. Positive feedback and wide Window are measured, which enables the PF-FET to be used in capacitorless DRAM applications. Due to self-refreshment in PF-FET, there is no data collapse during the Read operation. The sensing margin is **62 µA/µm** and retention time is greater than **4 s**. These results suggest that PF-FET is viable for capacitorless DRAM applications.

7.2 Contributions of This Work

The impact of substrate doping concentration in back-gated FDSOI capacitorless DRAM cell performance is studied, which suggests ways in which to control substrate doping in SOI with UTBOX structure. The failure mechanism of the BJT mode is investigated for the first time. This can provide guidance in designing structure and its operating conditions, which will improve the performance of capacitorless DRAM. Based on variability investigation, the scaling limit is researched. Scaling limits are determined by variability. Therefore, in order to extend scaling limits, the variation should be reduced and new materials can be considered. From this dissertation, the future research directions can be predicted.

7.3 Suggested Future Works

7.3.1 Overcoming Scaling Limits with 3D Structures/ New materials

In this dissertation, the scaling limits of capacitorless DRAM are investigated in terms of variations. One solution for overcoming scaling limits is to minimize process variations. However, with current fabrication capability, it is actually quite hard to reduce variations of each dimension. Novel structures and the adoption of new materials are needed in order to overcome limitations.

1) Multi-Gate Structures

Over the past several decades, two very different solutions to scaling have emerged. One approach is the planar thin-body SOI that is explained in this dissertation (**Fig. 7.1 (a)**). The other schemes are multi-gate transistors (*e.g.* FinFET in **Figs. 7.1 (b) ~ (e)** [11]) which turn the channel on its side in order to create a 3-D device. Each approach comes with its own set of merits and manufacturing challenges. Recently, one of the leading technological companies (Intel®) announced that they plan to change the architecture of the transistor to FinFET [12]. If the multi-gate transistor is built on SOI wafer, it needs complex fabrication processes and high fabrication cost (due to SOI wafer). However, FinFET has advantages, such as high currents [13], which are expected to increase sensing margins and retention times. Because the failure mechanism or scaling limits from process-induced variations of multi gate FETs may be different from those of planar SOI FETs, further studies are needed.

2) Band Engineering/ New Materials

Band gap engineering using $SiGe_x$ or Si:C has the possibility to improve the performance of capacitorless DRAM [6, 14]. Hetero junction designs have advantages (longer retention time [6, 14]) and disadvantages (complex fabrication processes). These

technologies are necessary to overcome the scaling limits below 10 nm gate length. Vertical type transistor structure with band gap engineering will be one good candidate for future capacitorless DRAM cells (**Fig. 7.2**). The research for III-V materials with capacitorless DRAM is also very promising for improving performance.

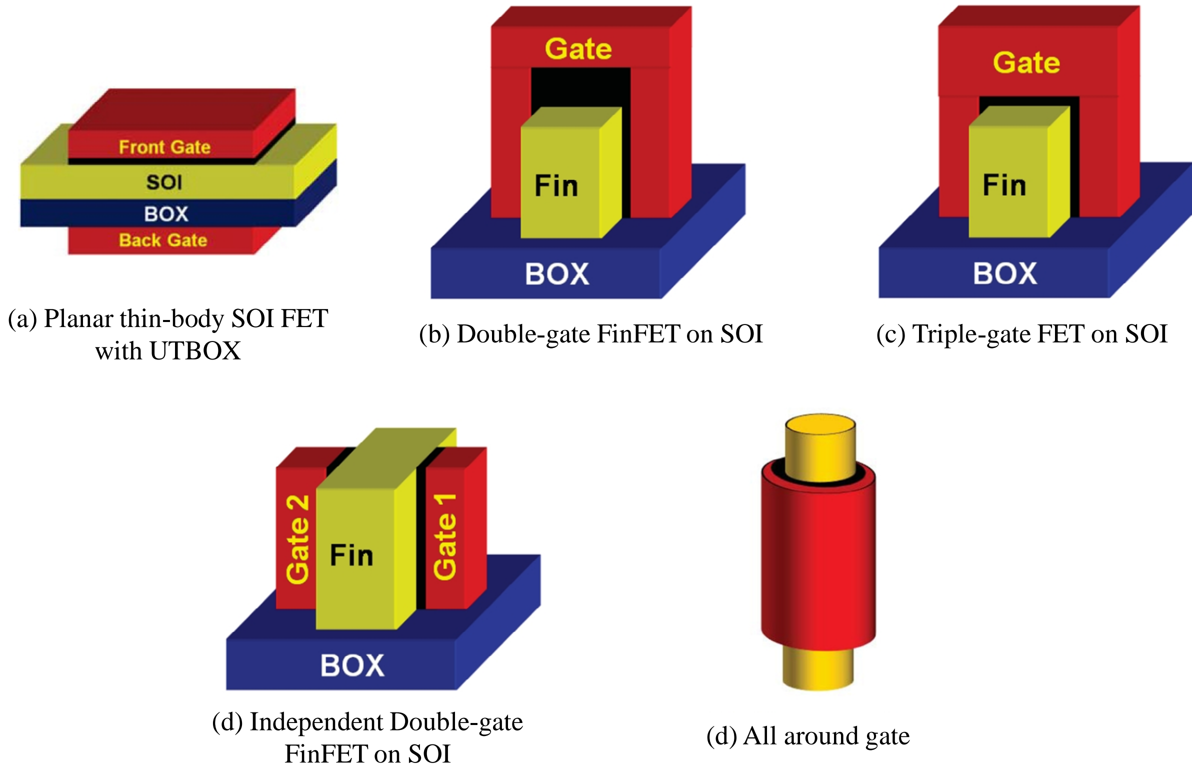


Figure 7.1. Illustration of multi-gate MOSFET structures (a) Planar thin-body SOI FET with UTBOX (basic test structure utilized in this study), (b) Double-gate FinFET on SOI, (c) Triple-gate FET on SOI, (d) Independent Double-gate FinFET on SOI, and (e) All around gate [11].

3) Miscellaneous

The reliability and disturbance issues should be also tested in terms of mass production. Though circuit architectures are outside the scope of this study, it can be another solution for sub 10 nm scaling technologies or improving reliability.

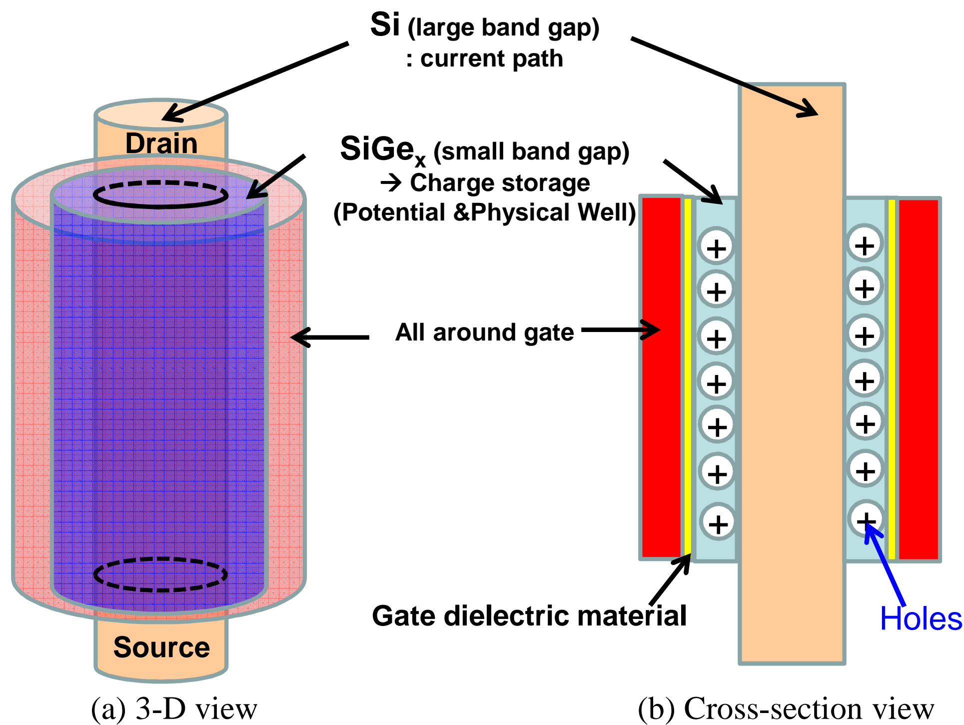


Figure 7.2. Vertical capacitorless DRAM structure using band gap engineering (with physical well and potential well). Large band gap material (*e.g.* silicon) is used as channel path and source/drain material. Small band gap material (*e.g.* silicon germanium ($SiGe_x$)) is used as charge storage node. $SiGe_x$ provides physical well and potential well, which can improve retention time [6]. (a) 3-dimensional view and (b) cross-section view.

7.3.2 Low Power Positive Feedback-FET

Low power integrated circuits are essential in mobile electronic systems. Power dissipation becomes an important constraint in device and design. The low power operation is also one of important issues in capacitorless DRAM cells. As explained in chapter 6, the operating voltages (gate bias or drain bias) in positive feedback are high. However, PF-FET is affected by dimensional factors and operating conditions. With the control of back bias and dimensional (body thickness or gate work function *etc.*) parameters, low operating voltages (< 0.5 V) can be achieved theoretically. Additionally, the scaling limit and failure mechanism of PF-FET should be studied in future.

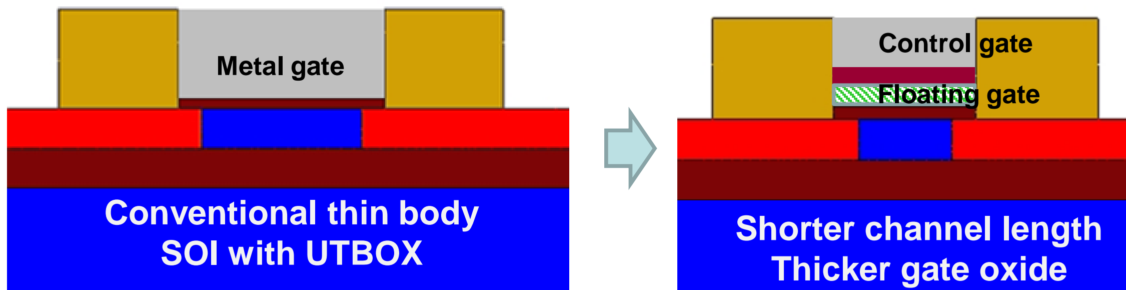


Figure 7.3. The tentative concept for NVM application using PF-FET.

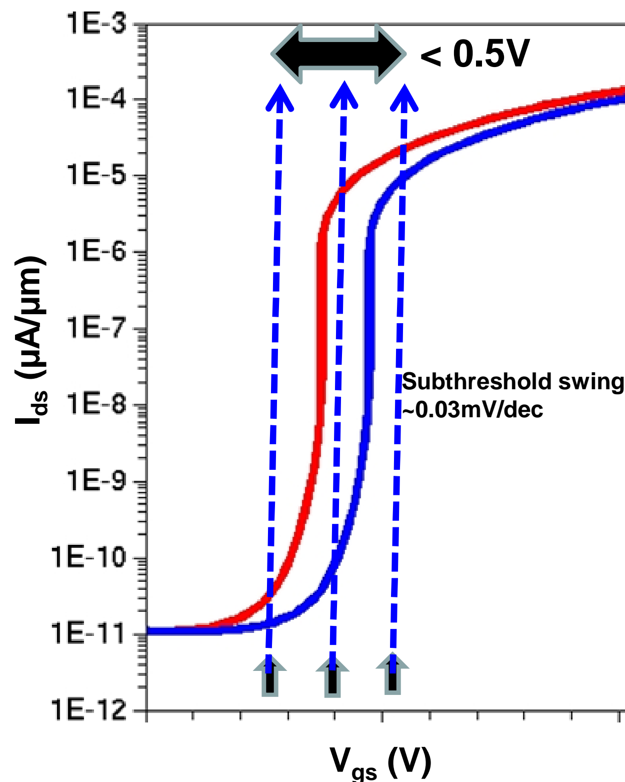


Figure 7.4. I_{ds}-V_{gs} curves for NVM using PF-FET. Due to steep subthreshold swing, data can be stored within small gate voltage range (< 0.5V). These curves are achieved in low drain voltage (V_{ds}= 0.5V).

7.3.3 Nonvolatile Memory Applications

There may be many applications of PF-FETs, including capacitorless DRAM. Steep sub-threshold slope can be utilized as non-volatile memories. Traditional nonvolatile memory (NVM) has floating gate structure. If the PF-FET is combined with NVM gate, a

novel concept of the NMV operation can be introduced. **Fig. 7.3** shows the new NVM structure. Though it is not yet optimized, very small gate voltage intervals can be taken using the PF-FET operation (**Fig. 7.4**). Traditional NMV needs thick gate oxide due to charge retention but it also suffers from short channel effect from low coupling of gate (low gate oxide capacitance). As explained in chapter 6, thicker gate oxide is desirable for PF-FET, and short channel length increases positive feedback. Additionally PF-FET can potentially be very promising in multi-bit NVM applications.

7.4 References

[1] International Technology Roadmap for Semiconductors (ITRS). [Online]. Available: http://public.itrs.net

[2] T. Ohtou, N. Sugii, and T. Hiramoto, "Impact of parameter variations and random dopant fluctuations on short-channel fully depleted SOI MOSFETs with extremely thin BOX," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 740–742, Aug. 2007

[3] H.-J. Wann and C. Hu, "Capacitorless DRAM Cell on SOI Substrate," *IEDM Tech. Dig.*, Dec. 1993, pp. 635 – 638.

[4] S. Okhonin, M. Nagoga, E. Carman, R. Beffa, and E. Faraoni, "New Generation of Z-RAM," *IEDM Tech. Dig.*, Dec. 2007, pp. 925-928.

[5] K.-W. Song, H. Jeong, J.-W. Lee, S. I. Hong, N.-K. Tak, Y.-T. Kim, Y. L. Choi, H. S. Joo, S. H. Kim, H. J. Song, Y. C. Oh, W.-S. Kim, Y.-T. Lee, K. Oh, and C. Kim, "55 nm Capacitor-less 1T DRAM Cell Transistor with Non-Overlap Structure," *IEDM Tech. Dig.*, Dec. 2008, pp. 1-4.

[6] M.H. Cho, C. Shin, and T.-J. K. Liu, "Convex Channel Design for Improved Capacitorless DRAM Retention Time," *IEEE International conference on simulation of semiconductor processes and devices (SISPAD)*, Sep. 2009, pp. 1-4.

[7] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T.-J. K. Liu, "Feedback FET: A Novel Transistor Exhibiting Steep Switching Behavior at Low Bias Voltages," *IEDM Tech. Dig.*, Dec. 2008, pp. 1-4.

[8] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 178-179.

[9] Z. Lu, N. Collaert, M. Aoulaiche, B. De Wachter, A. De Keersgieter, J. G. Fossum, L. Altimime, and M. Jurczak, "Realizing Super-Steep Subthreshold Slope with Conventional FDSOI CMOS at Low-Bias Voltages," *IEDM Tech. Dig.*, Dec. 2010, pp. 16.6.1-3.

[10] C. Onal, R. Woo, H.-Y. S. Koh, P. B. Griffin, and J. D. Plummer, "A Novel Depletion-IMOS (DIMOS) Device With Improved Reliability and Reduced Operating Voltage," *IEEE Electron Device Lett.*, vol. 30, no. 1, pp. 64-67, Jan. 2009.

[11] D. Lu, "Compact Models for Future Generation CMOS," Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., University of California, Berkeley, CA, 2011.

[12] K. Ahmed, K. Schuegraf, "transistor wars," *IEEE Spectrum*, vol. 48, no. 11, pp. 50-66, 2011.

[13] C.C. Wu, D.W. Lin, A. Keshavarzi, C.H. Huang, C.T. Chan, C.H. Tseng, C.L. Chen, C.Y. Hsieh, K.Y. Wong, M.L. Cheng, T.H. Li, Y.C. Lin, L.Y. Yang, C.P. Lin, C.S. Hou, H.C. Lin, J.L. Yang, K.F. Yu, M.J. Chen, T.H. Hsieh, Y.C. Peng, C.H. Chou, C.J. Lee, C.W. Huang, C.Y. Lu, F.K. Yang, H.K. Chen, L.W. Weng, P.C. Yen, S.H. Wang, S.W. Chang, S.W. Chuang, T.C. Gan, T.L. Wu, T.Y. Lee, W.S. Huang, Y.J. Huang, Y.W. Tseng, C.M. Wu, E. O. Yang, K.Y. Hsu, L.T. Lin, S.B. Wang, T.M. Kwok, C.C. Su, C.H. Tsai, M.J. Huang, H.M. Lin, A.S. Chang, S.H. Liao, L.S. Chen, J.H. Chen, P.S.

Lim, X.F. YU, S.Y. Ku, Y.B. Lee, P.C. Hsieh, P.W. Wang, Y.H. Chiu, S.S. Lin, H.J. Tao, M. Cao, and Y.J. Mii, "High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme," *IEDM Tech. Dig.*, Dec. 2010, pp. 27.1.1 - 27.1.4.

[14] S.-J. Choi, D.-I. Moon, Y. Ding, E. Y. J. Kong, Y.-C. Yeo, and Y.-K. Choi, "A Novel Floating Body Cell Memory with a Laterally Engineered Bandgap using a Si-Si:C Heterostructure," *IEDM Tech. Dig.*, Dec. 2010, pp. 22.4.1 - 22.4.4.