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Los Angeles

Study of Interfacial Reaction on Intermetallic Compound Formation  
in Sn/Cu Pillar Bump Affected by Scaling

A thesis submitted in partial satisfaction  
of the requirements for the degree Master of Science  
in Materials Science and Engineering

by

Ying-Ching Chu

2017

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2017

## ABSTRACT OF THE THESIS

### Study of Interfacial Reaction on Intermetallic Compound Formation in Sn/Cu Pillar Bump Affected by Scaling

by

Ying-Ching Chu

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2017

Professor King-Ning Tu, Chair

Sn/Cu pillar structure in diameter of 1, 5, 10, 20, and 30  $\mu\text{m}$  are fabricated by focused-ion-beam (FIB). After solid state reaction at  $175^{\circ}\text{C}$ ,  $185^{\circ}\text{C}$ , and  $195^{\circ}\text{C}$ , the growth of intermetallic compound (IMC) has been studied in this thesis. With the decrease of pillar diameter, especially below 20  $\mu\text{m}$ , the formation rate of IMC will increase. Through FIB slice-and-view study, several Kirkendall voids can be observed at the circumference area of the pillar. Based on the results, it is concluded that surface diffusion has more influence on small-sized pillar. Owing to different dominant diffusion path in small-sized pillar, the kinetic model used for lattice diffusion analysis has been modified by adding terms to represent

surface and grain boundary diffusion. For 1  $\mu\text{m}$  pillar case, with only single grain inside, a simple model has been built by ignoring lattice and grain boundary diffusion. Using this simple model, the surface diffusivity of Cu on  $\text{Cu}_6\text{Sn}_5$  is acquired, which is  $3.1 \times 10^{-7} \text{ cm}^2/\text{s}$  at  $185^\circ\text{C}$ .

The thesis of Ying-Ching Chu is approved.

Ya-Hong Xie

Jenn-Ming Yang

King-Ning Tu, Committee Chair

University of California, Los Angeles

2017

# Table of Contents

|   |           |
|---|-----------|
| <b>Chapter 1: Introduction</b>  | <b>1</b>  |
| 1.1 Motivation  | 1         |
| 1.2 IC packaging technology   | 3         |
| 1.3 Flip-chip technology  | 5         |
| 1.4 Sn/Cu binary system   | 8         |
| 1.5 Diffusion path in solids  | 12        |
| 1.6 Kirkendall effect   | 16        |
| <b>Chapter 2: Experimental</b>  | <b>18</b> |
| 2.1 Sn/Cu pillar sample preparation   | 18        |
| 2.2 Sn/Cu pillar reaction   | 20        |
| <b>Chapter 3: Results</b>   | <b>21</b> |
| 3.1 Results   | 21        |
| <b>Chapter 4: Discussion</b>  | <b>31</b> |
| 4.1 Cu/IMC interfacial reaction affected by scaling effect                      | 31        |
| 4.2 IMC uniformity affected by the poor quality of electroplating Sn film       | 34        |
| 4.3 The formation of Kirkendall voids around surface induced by inter-diffusion | 37        |
| 4.4 Kinetic model of IMC formation with surface diffusion involving             | 38        |
| 4.5 A simple model for IMC growth in pillars smaller than 1um                   | 41        |

|                              |           |
|------------------------------|-----------|
| <b>Chapter 5: Conclusion</b> | <b>46</b> |
| 5.1 <i>Conclusion</i>        | 46        |
| <b>References</b>            | <b>48</b> |



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# Chapter 1: Introduction

## 1.1 Motivation

In the era of big data and Internet of things, the mobile electronic devices have been forced to deal with much more data than before. Due to the increasing density of integrated circuits (IC), the input/output (I/O) bump pitch for packaging is becoming smaller and smaller. However, there are physical limitations for the fabrication process and materials, which slow down the size shrinking. As for the conventional solder bumps in 2D IC, the limitation is becoming more and more obvious. As a result, 3D IC packaging technology shows great potential in exceeding the physical limitation.

Microbump in 3D IC packaging is about 5 to 10 times smaller than regular solder bumps, which is around 10  $\mu\text{m}$  ~ 40  $\mu\text{m}$  in diameter. The volume of solder bumps decreases, but the Sn/ Cu reaction rate is still the same. As a result, the percentage of intermetallic compound (IMC) formation will dramatically increase and become a serious issue on reliability. Figure 1 shows the SEM image of two different size bumps with different portion of IMC formation [1]; the smaller one has more IMC than the bigger one under the same amount of annealing. Hence, in this thesis, we will focus on the relation between the size of microbump and the formation of IMC, and find out the possible cause from the kinetic point of view.

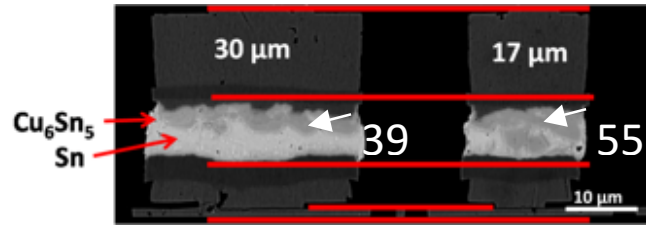


Figure 1. SEM image of Qualcomm sample in different size with different portion of IMC formation [1].

## 1.2 IC packaging technology

IC packaging technology is the electronic connection system which enables the operation of IC chips by a human, so that a combination of chip and its packaging form a useful electronic device. As a result, packaging technology is developed along the development of IC chips in order to meet the requirements of consumer electronic products, for example. In nowadays, portable devices and wearable devices are the mainstream in the semiconductor industry. Unlike traditional electronic devices, such as personal computer and television, the size of portable devices and wearable devices are much smaller. In order to achieve the same or higher performance of traditional electronic devices with larger size, every component in portable devices and wearable electronic devices has to be miniaturized. Owing to this trend, packaging technology has to keep improving in order to meet the requirement of the newest generation of ICs.

IC packaging technology can be categorized in 4 styles: through-hole (PTH), surface-mount (SMD or SMT), area array, and bare chip. In the 1970s, dual in-line package (DIP), the most common through-hole style package, is the mainstream in the industry. DIP is characteristic of two parallel rows of pins, ranging from 4 to 64 and the space between each pin is about 2.54 mm. In the 1980s, in order to reduce the size of package and increase component I/O densities, surface-mount style packages were invented. Small Out-Line Package (SOP) and Quad Flat Package (QFP) which are common SMT style package replaced DIP. However, PTH style and SMT style, based

on wire bonding interconnection, have limitation in shrinking size and increasing component I/O densities. In the early 1990s, area array style package was developed, which replace wires by solder balls which are arranged in a 2-dimensional grid. In this way, component I/O densities can be largely increased and the component volume can be further miniaturized. After 2000s, bare chip package, such as chip scale packages (CSP), fine ball grid array (FBGA), and wafer level packaging (WLP), largely diminished the area and weight of packaging. Especially, CSP flip-chip packaging has the smallest area, comparing to other packaging technologies. However, in nowadays, the density of IC is still increasing and bump pitch is becoming finer, even smaller than 150  $\mu\text{m}$ . As a result, 3D IC packaging has been developed. The key feature of 3D IC packaging is that chips are stacked up in the vertical direction, unlike the traditional packaging technology which places chips horizontally. Owing to this feature, the density of IC can be further increased. Thus, this stacking method seems to be the promising way to reach the tough requirement due to fast development of electronic devices [2][3].

### 1.3 Flip-chip technology

The flip-chip technique is one of the significant progress in the field of electronic packaging, which connects the chip and the substrate with a large number of I/O. In 1960's, IBM first introduced the Controlled-Collapse-Chip-Connection (C4) solder joint technology for the first-level interconnect in multi-chip module packages used in mainframe computers [4]. The main characteristic of the flip-chip technique is that the solder bump connections (C4 solder bumps) have been deposited on the bump-pads and distributed on the entire surface of the die. The connections are made under the entire die, not bonded on the sides of the die as in the traditional package. With the flip-chip technique, the active side on the chip is turned upside down towards the substrate. The process flow of flip-chip is shown in figure 2 [5].

By this method, the I/O density can be increased since the solder bumps can be distributed all over the surface, unlike the traditional wire bonding of tape automated bonding (TAB), in which bonds only occur on the edges of the die. In addition, higher device speed, better resolution and performance, and lower stress over active area can be achieved by the flip-chip technology.

Based on the concept of flip-chip technology, to reduce the stress requirement due to chip-packaging interaction, 2.5D and 3D packaging concepts have been developed. Unlike traditional packaging technology, the silicon dies are stacked up vertically with microbumps on the interposer using C4 joints and BGA to connect with the substrate and the PCB board. Figure 3 shows the structure of 2.5D IC packages and the size of

the solder balls. The size of microbump is from 10  $\mu\text{m}$  to 40  $\mu\text{m}$ , which is much smaller than C4 joint and BGA. Therefore, there are still many reliability issues, such as higher percentage of IMC formation, need to be studied [6].

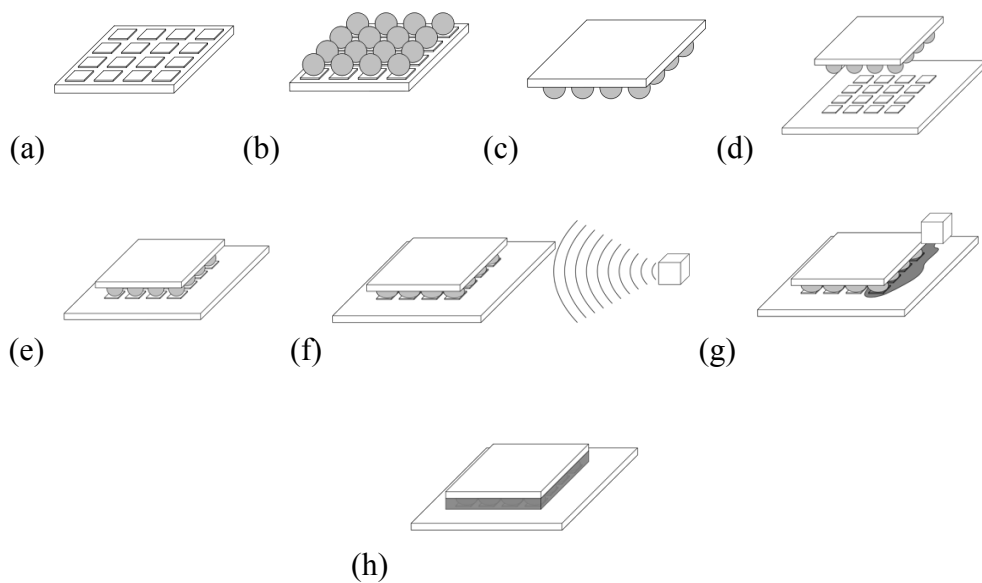


Figure 2. The process of flip-chip packaging, (a) process integrated circuits and pads on the wafer; (b) deposit the solder bumps on each of the pads; (c) Flip the chip; (d) solder bumps positioned and faced to the connectors; (e) connect the solder bumps with the external circuit; (f) reflow the solder bumps; (g) the chip is under-filled using an electrically-insulating adhesive [7].

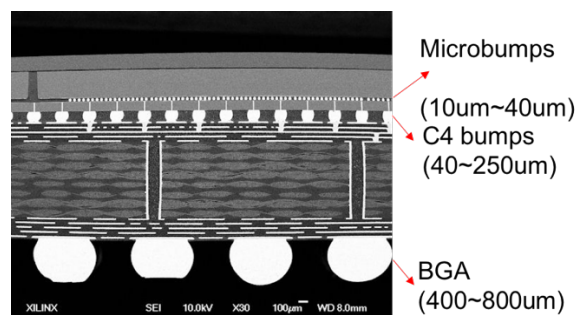


Figure 3. Cross-sectional microphotograph of 2.5D Xilinx Virtex 7 SSI device.

(Image courtesy of Xilinx)



## 1.4 Sn/Cu binary system

In solder joint technology, Sn and Cu are the most important elements. As a result, the intermetallic compound formation in Sn and Cu binary system has been studied thoroughly for many years. Figure 4 presents the Sn-Cu phase diagram. According to the phase diagram, we can see that different compound would be formed with different atomic ratio under different temperature. In our experiment, we only focus on compounds formed within the temperature range from 175°C to 195°C. Within this range, Sn/Cu binary system only forms two compounds:  $\text{Cu}_6\text{Sn}_5$  ( $\eta$ ) and  $\text{Cu}_3\text{Sn}$  ( $\epsilon$ ). In general,  $\text{Cu}_6\text{Sn}_5$  has two crystal structure: hexagonal ( $\eta$ ) and monoclinic ( $\eta'$ ). The phase transition temperature is about 186°C [8]. Referring to K. Nogita et al.'s work, it is difficult for  $\eta$  phase to transform to  $\eta'$  phase under 70°C, shown in figure 5. Hence, we are able to confirm that most of the crystal structure of  $\text{Cu}_6\text{Sn}_5$  is hexagonal ( $\eta$ ) in solder joint reaction [9].

For the Sn/Cu reaction, Tu et al. found out that when Sn react with Cu at room temperature, only the formation of  $\text{Cu}_6\text{Sn}_5$  compound can be observed even after one year. However, when Sn react with Cu at temperature above 100°C,  $\text{Cu}_3\text{Sn}$  will start to form a layer between Cu and  $\text{Cu}_6\text{Sn}_5$  with the consumption of  $\text{Cu}_6\text{Sn}_5$  [10] [11]. In 1981, to understand the kinetics of IMC formation, Tu and Thompson insert a layer of W markers between Sn and Cu thin film and react under room temperature. According to the shift of W markers, Tu and Thompson concluded that Cu is the dominant diffusion species during the Sn/Cu reaction under room temperature [12]. Figure 6

shows the schematic diagram of W marker motion between Sn and Cu thin film.

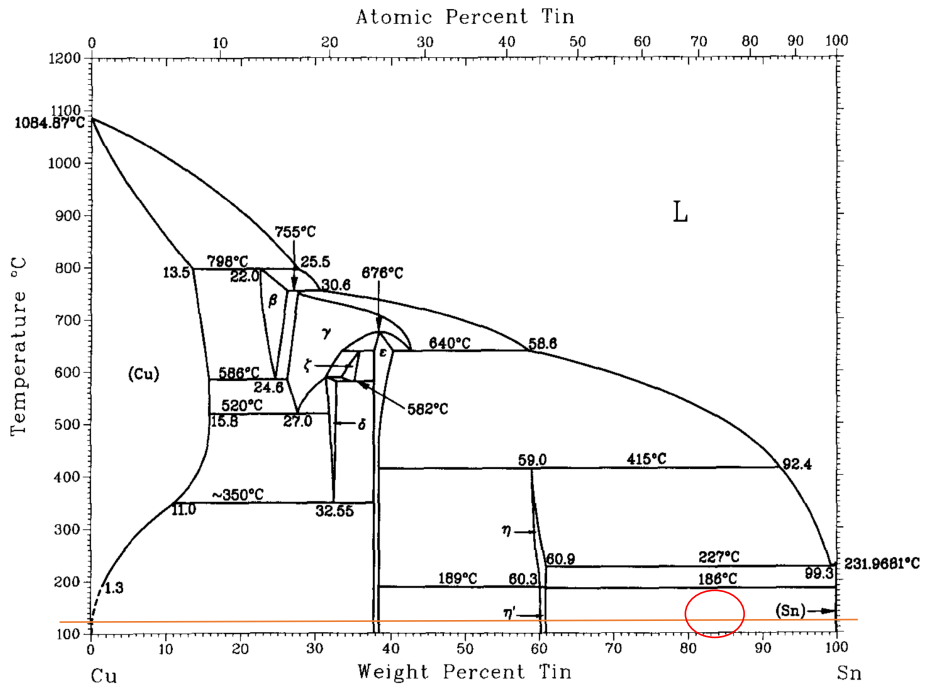


Figure 4. Cu-Sn equilibrium phase diagram [8].

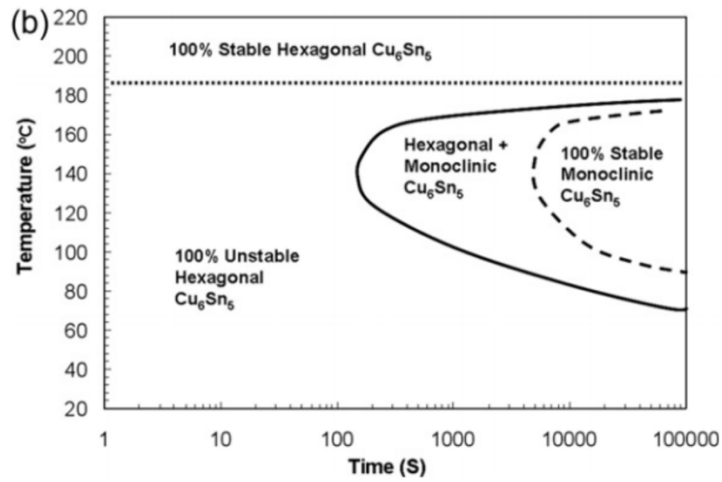


Figure 5. TTT diagram for  $\text{Cu}_6\text{Sn}_5$  [9].

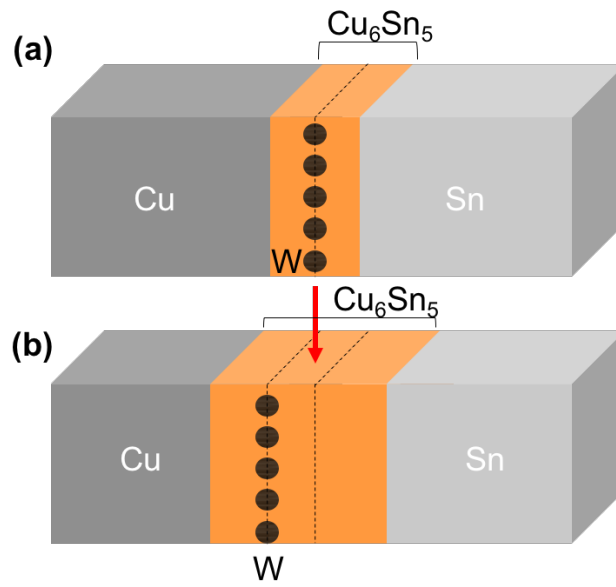


Figure 6. A schematic diagram of W markers motion in Sn/Cu diffusion couple. (a)

Before the reaction. (b) After the reaction.

## 1.5 Diffusion path in solids

Diffusion is an atomic process that an atom moves to another lattice site triggered by concentration gradient or temperature gradient. For an atom to diffuse in solids, there are several mechanisms: direct exchange, cyclic exchange, vacancy, and interstitial. Figure 7 shows the different atomic diffusion mechanisms in solids. In these diffusion mechanisms, vacancy is the most common one in face-centered cubic metals. If an atom wants to diffuse inside a metal, it has to diffuse by jumping to the neighboring vacancy site. However, when the atom attempts to jump to the neighboring site, it has to go over the saddle point with a certain activation energy [13] [14]. Figure 8 depicts the atom jump process. As a result, we know that atomic diffusion is a thermally activated process which is related to activation energy.

Vacancy is an equilibrium point defect. For metals, we can find most vacancy sites at the free surface, the grain boundary, and the dislocation. These sites are the high diffusivity path for atomic diffusion in metals [13]. Figure 9 presents a schematic diagram of different diffusion path in a pillar bump. In general, the activation energy of free surface diffusion is the lowest, followed by grain boundary diffusion and lattice diffusion. Lattice diffusion via a lattice vacancy, has the highest activation energy. As a result, the atomic jump rate would be the highest at free surface and would be lowest in the lattice [14]. In most cases in a bulk sample, the influence of surface diffusion is too small due to small surface/volume ratio. Hence, the contribution of surface diffusion can be neglected in most cases. However, in our

study, we find out that surface diffusion will become the dominant diffusion path in small-sized pillar bumps. Accordingly, we will discuss the contribution of diffusion path in small-sized bump in chapter 4.

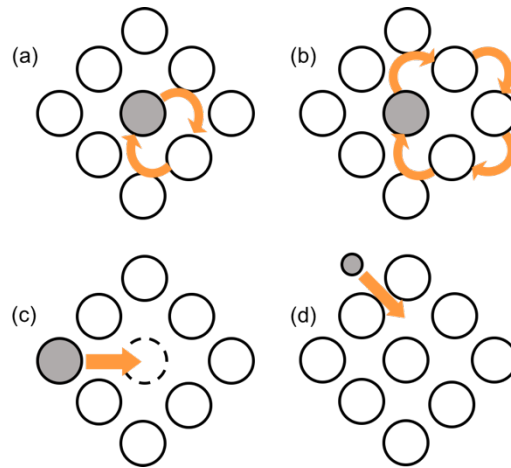


Figure 7. Atomic diffusion mechanisms in solids; (a) direct exchange, (b) cyclic exchange, (c) vacancy, and (d) interstitial.

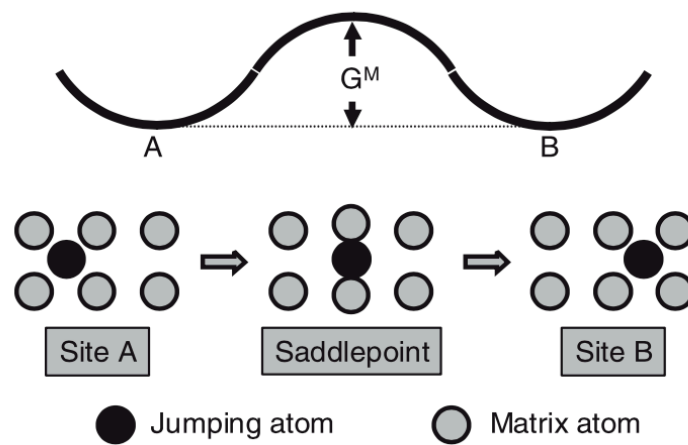


Figure 8. The process of the atom jump in vacancy diffusion [14].

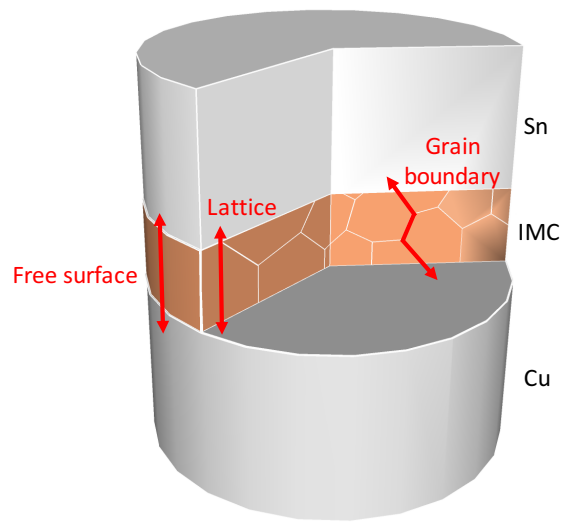


Figure 9. Different diffusion path in a pillar bump.



## 1.6 Kirkendall effect

In 1947, Smigelskas and Kirkendall inserted 10  $\mu\text{m}$  diameter Mo wires as markers in between the alpha-brass (70wt%Cu-30wt%Zn) and Cu diffusion couple. The schematic diagram of this experiment is shown in figure 10. They annealed the alpha-brass/Cu diffusion couple at 785°C. After annealing, they measure the distance between two lines of Mo markers and compared to the distance before annealing. They found out that the distance between two lines of Mo markers decreased. The result implied that Zn atoms which diffused out is more than Cu atoms which diffused in. It means that the fluxes of Zn and Cu in the opposite direction are uneven. By this experiment, the kinetic mechanism of atomic diffusion is also greatly modified.. If atoms diffuse by direct exchange or cyclic exchange, there would be no mark motion can be observed. On the other hand, if atoms diffused by vacancy jumping, a flux of vacancies will be needed to balance the uneven fluxes of Zn and Cu. As a result, marker motion can be observed in the latter case. This paper confirmed the kinetic process of atomic diffusion in face-centered cubic metal, which is vacancy jumping [15].

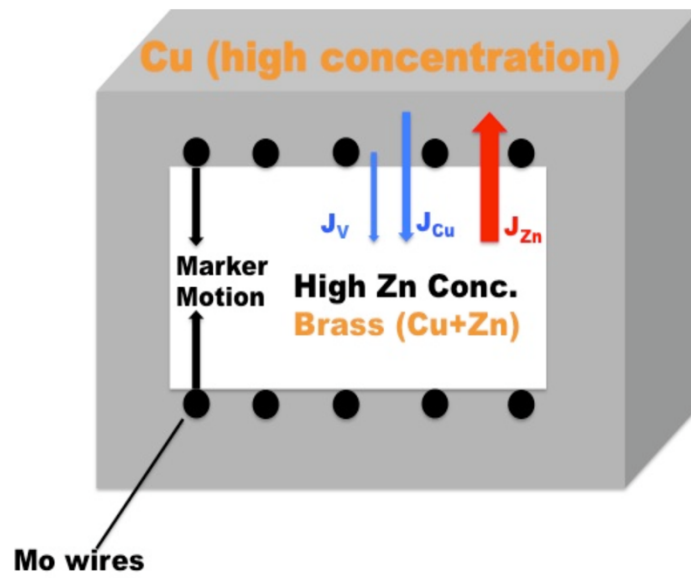


Figure 10. A schematic diagram represented the fluxes in the alpha-brass/Cu diffusion couple with Mo markers in between [16].

## Chapter 2: Experimental

### 2.1 Sn/Cu pillar sample preparation

For Sn/Cu pillar sample preparation, we used electroplating technique to deposit a very thin layer of Sn on a pure Cu substrate. After electroplating, focused-ion-beam (FIB) technique was applied for Sn/Cu pillar fabrication. The detail of sample preparation is as follows.

- (1). 1 cm by 1 cm polycrystalline Cu plates from MTI Cooperation were used for our experiment and were well-polished.
- (2). We put these Cu plates into 10% HNO<sub>3</sub> solution for 15 s for degreasing which is for oxidation layer and containment removal.
- (3). We placed these plates into Sn plating solution from Transene Company, Inc. and applied direct current to the solution at 0.05 A for 10 min. By these steps, a thin layer of Sn was formed on the polycrystalline Cu plates.
- (4). After electroplating process of Sn, we polished the layer of Sn and reduced the thickness of Sn layer down to 5 - 10 nm for focused-ion-beam patterning.

In order to obtain Sn/Cu pillar samples, we employed FIB, FEI Nova 600, to pattern the structure of pillars and removed the additional Sn through FIB induced Ga<sup>+</sup> ions. In our experiment, different diameter of Sn/Cu pillar samples which are 1, 5, 10, 20, and 30  $\mu\text{m}$  were produced. Figure 11 shows the experimental procedures from sample preparation to Sn/Cu reaction.

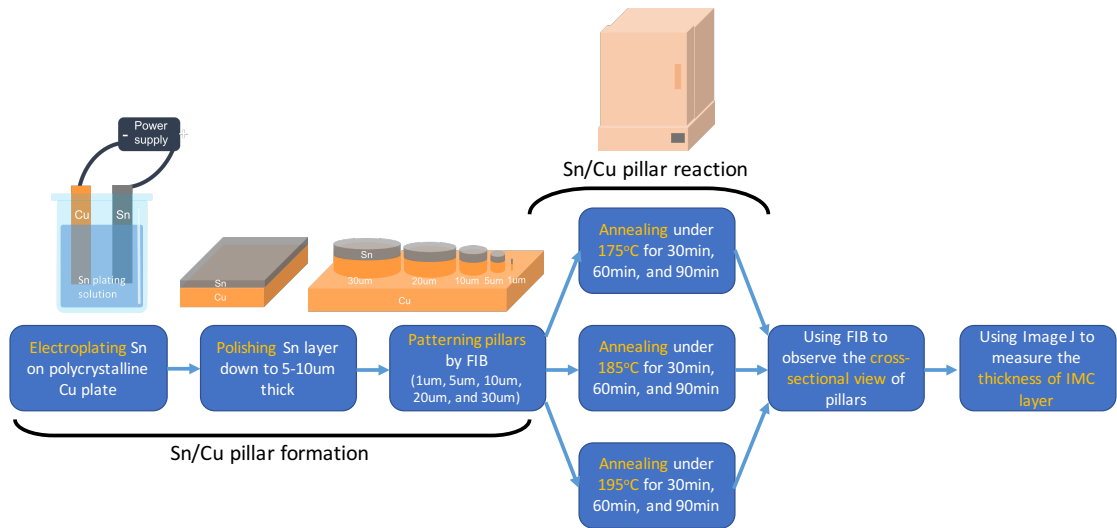


Figure 11. Experimental procedures from sample preparation to reaction.

## 2.2 Sn/Cu pillar reaction

To observe the growth of intermetallic compound, Sn/Cu pillar samples with different diameters were put into a vacuum oven with 28.6 In.Hg vacuum, about 33.4 torr, for annealing. These samples were annealed under 185 °C and 195 °C for 30 min, 60 min, and 90 min. For experimental observation of Sn/Cu reaction results, we used FIB to make cross-sectional view of 30 min-annealed samples and collected the results by SEM observation. After SEM observation, the 30 min-annealed samples were annealed for 30 min again at the same temperature to obtain the 60 min-annealed samples results. After collecting the 60 min-annealed samples results, we repeated the 30 min annealing process again to acquire the 90 min-annealed samples.

To define the composition of IMC, EDX analysis was applied on the samples which were cut cross-sectionally by FIB for SEM observation. Through the ratio of different elements shown by EDX, the layer of Cu, Sn, Cu<sub>3</sub>Sn and, Cu<sub>6</sub>Sn<sub>5</sub> can be confirmed at the cross-sectional image of our samples. However, we can detect the signal from Cu<sub>6</sub>Sn<sub>5</sub> in our sample by EDX, but not Cu<sub>3</sub>Sn. For IMC thickness measurement, we use software Image J to measure the area and length of IMC and we divided the area by length to acquire the IMC thickness.

## Chapter 3: Results

### 3.1 Results

Figure 12 shows the SEM cross-sectional image of Sn/Cu interface before annealing. At the interface of Sn/Cu, we can see a Sn electroplating film with a few tiny voids, which is suitable for our experiment. Figure 13 shows the 52-degree-tilt view of SEM image of FIB-patterned pillars with five different diameters: 1, 5, 10, 20, and 30  $\mu\text{m}$ , before annealing.

After annealing process, we can observe an obvious newly formed layer with light gray color between Sn and Cu layer, which is the  $\text{Cu}_6\text{Sn}_5$  layer, confirmed from SEM cross-sectional images, shown in Figure 14. The thickness of  $\text{Cu}_6\text{Sn}_5$  layer was measured by software Image J from SEM cross-sectional images. To reduce numerical error from our results, we measured the thickness of  $\text{Cu}_6\text{Sn}_5$  layer for 10 times and collected the average value as 1 datum point for 1 and 5  $\mu\text{m}$  samples. As for 10, 20, and 30  $\mu\text{m}$  samples, we measured the thickness of  $\text{Cu}_6\text{Sn}_5$  layer for 4 times and collected the average value as 1 datum point. Table 1 lists the calculated average thickness of  $\text{Cu}_6\text{Sn}_5$  layer from measured data under  $185^\circ\text{C}$  annealing process. Based on the data from Table 1, we plotted graphs with pillar diameter and IMC thickness, which is respectfully the x axis and the y axis, shown in Figure 15. According to Figure 13, samples after 30 min annealing showed a slight decreasing tendency of  $\text{Cu}_6\text{Sn}_5$  thickness when the pillar diameter increases. For samples after 60 min and 90

min annealing, the decreasing tendency become more obvious in 1 and 5  $\mu\text{m}$  pillars. However, in 30  $\mu\text{m}$  pillars, the decreasing tendency became opposite, which means that the thickness of  $\text{Cu}_6\text{Sn}_5$  increases. Especially, for 30  $\mu\text{m}$  pillars after 90 min annealing, the thickness of  $\text{Cu}_6\text{Sn}_5$  increases faster than after 60 min annealing. As a result, according to Figure 15, we found a non-monotonic behavior in IMC growth when the size of pillar is shrunk below 20 $\mu\text{m}$ . Hence, we will make an explanation of this kind of behavior in the discussion session.

Furthermore, we make a direct observation of morphology of our samples from SEM images for more details. Figure 16 shows the SEM image of 1 $\mu\text{m}$  diameter pillar after 195°C annealing process for 30, 60 and 90 min. We can observe from the surface of the pillar bump that the layer of IMC is getting thicker with the increase of annealing time. Few voids can be found at the interface of Cu/IMC after 60 min annealing, shown in figure 16. After 90 min annealing, the number of voids at the interface of Cu/IMC is increased and connected to each other, forming a bump crack. Figure 17 shows a SEM cross-sectional image of 1 and 5  $\mu\text{m}$  pillars after 30, 60, and 90 min annealing under 195°C. We can see that the IMC layer is getting thicker with the annealing time, both in 1 and 5  $\mu\text{m}$  pillars. At the interface of Cu/IMC, several voids which are pointed out by the red arrows can be found both in 1 and 5  $\mu\text{m}$  pillars. We consider these voids to be Kirkendall voids caused by Kirkendall effect. Not only the small voids at interface of Cu/IMC, but also several big voids can be found inside the IMC layer. This kind of big voids inside the IMC layer is caused by the poor

quality of Sn electroplating film.

Figure 18 presents SEM cross-sectional images of different diameter pillars after 60 min annealing under 185°C. We can see several big voids inside the IMC layer. The big-sized pillar is with more voids inside the IMC layer than the small-sized pillar. As a result, the uniformity of the big-sized pillar seems to be worse than the small-sized pillar. Table 2 lists the percentage of non-uniformity calculation results of the IMC layer in different diameter pillars after 60 min annealing under 185°C. The results show that the big-sized pillar tends to have higher percentage of non-uniformity, which is opposite to the small-sized pillar. The reason causing non-uniform IMC layer will be discussed in the later section.

To understand the distribution of interfacial voids between  $\text{Cu}_6\text{Sn}_5$  and Cu, we made several cross-sectional cuts sequentially through the sample by FIB, for slice-and-view study. Figure 19 show the results of slice-and-view study of 5  $\mu\text{m}$  pillar after 90 min annealing process, so that we can follow the sequence of slice-and-view study from the surface to the center of the pillar. Observing from the surface of the pillar, we can see many voids connected to each other, forming a bump crack, shown in Figure 19(a)(1). Next, by cutting into the pillar, the connected voids can be seen more obviously, indicating by the red arrow in Figure 19(a)(2). Afterwards, when slice-and-view study reached the center of the pillar, voids are rarely found at the interface, shown in Figure 19(a)(3). By this study, we can determine the distribution of interfacial voids, which located only along the



circumference area which is near the surface of the pillar. Figure 20 presents a schematic diagram of the distribution of interfacial voids of the 5 um pillar. Not only in 5 um pillars, we can also find this kind of interfacial voids distribution in almost all the samples. We will explain how this kind of interfacial voids formed in the next section.

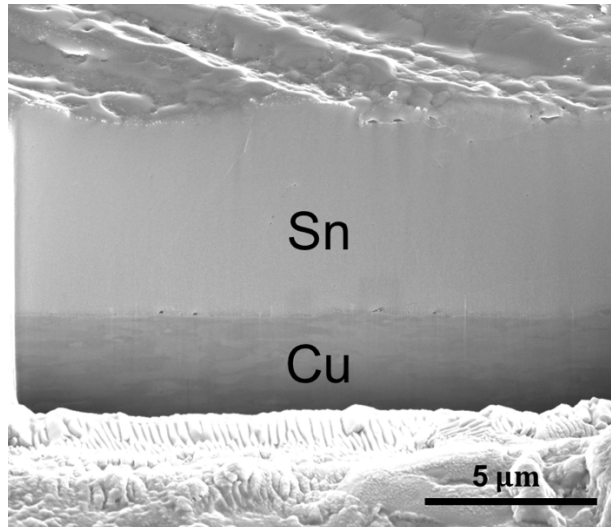


Figure 12. SEM cross-sectional image of Sn/Cu interface before annealing.

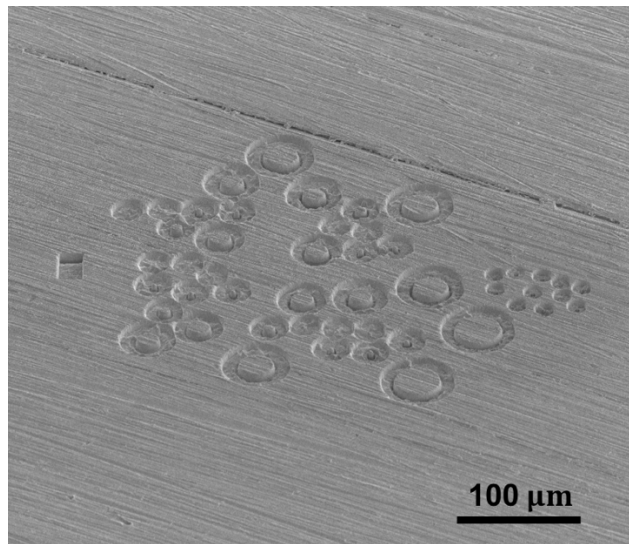


Figure 13. SEM image of FIB-patterned pillars with five different diameters: 1, 5, 10, 20, and 30um before annealing.

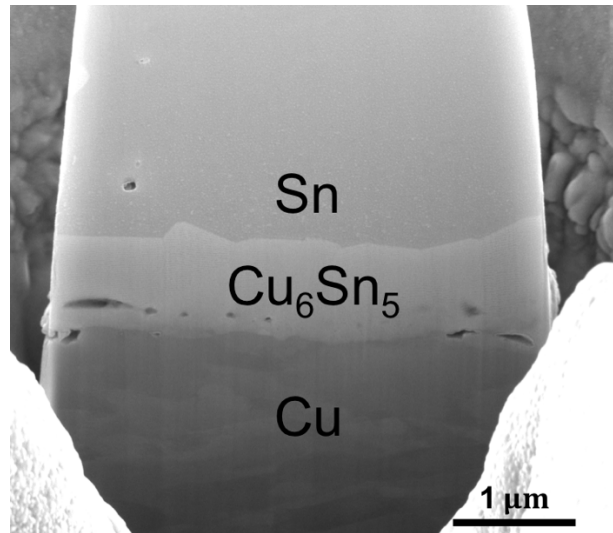


Figure 14. Cross-sectional SEM image of Sn/Cu pillar after 90min annealing under 185°C.

| Min | μm   |      |      |      |      |
|-----|------|------|------|------|------|
|     | 1    | 5    | 10   | 20   | 30   |
| 30  | 0.46 | 0.44 | 0.41 | 0.40 | 0.39 |
| 60  | 0.64 | 0.61 | 0.56 | 0.48 | 0.49 |
| 90  | 0.76 | 0.71 | 0.65 | 0.54 | 0.62 |

Table 1. Calculated average thickness of  $\text{Cu}_6\text{Sn}_5$  layer from measured data under 185°C after annealing process [1].

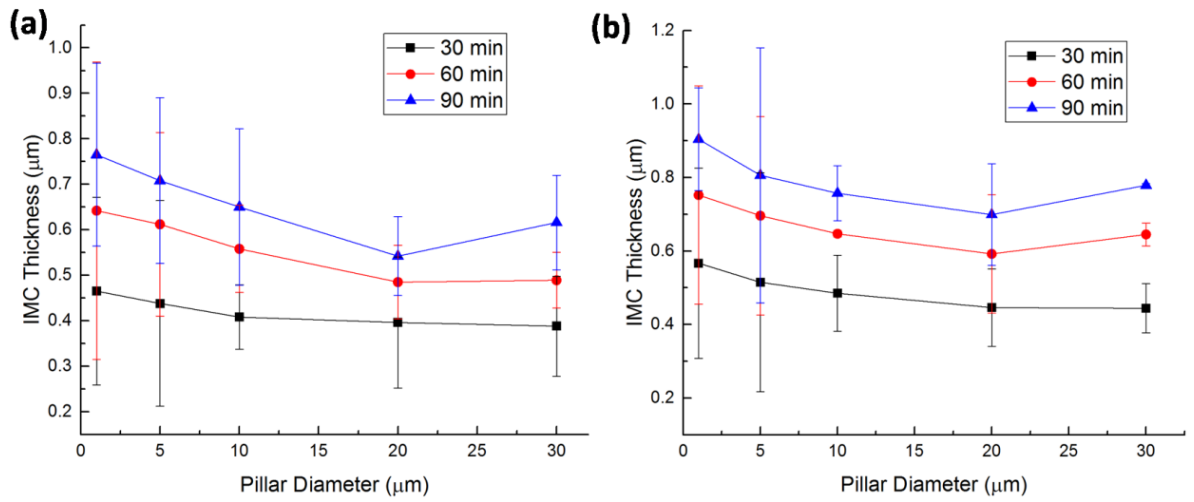


Figure 15. IMC thickness changing with different diameter after annealing process under (a) 185°C and (b) 195°C [1].

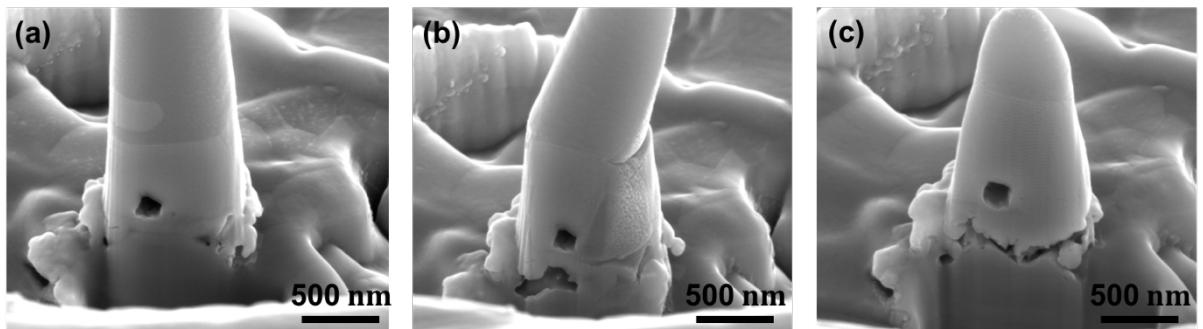


Figure 16. SEM image of 1 $\mu\text{m}$  diameter pillar after 195°C annealing process for (a) 30, (b) 60, and (c) 90 min.

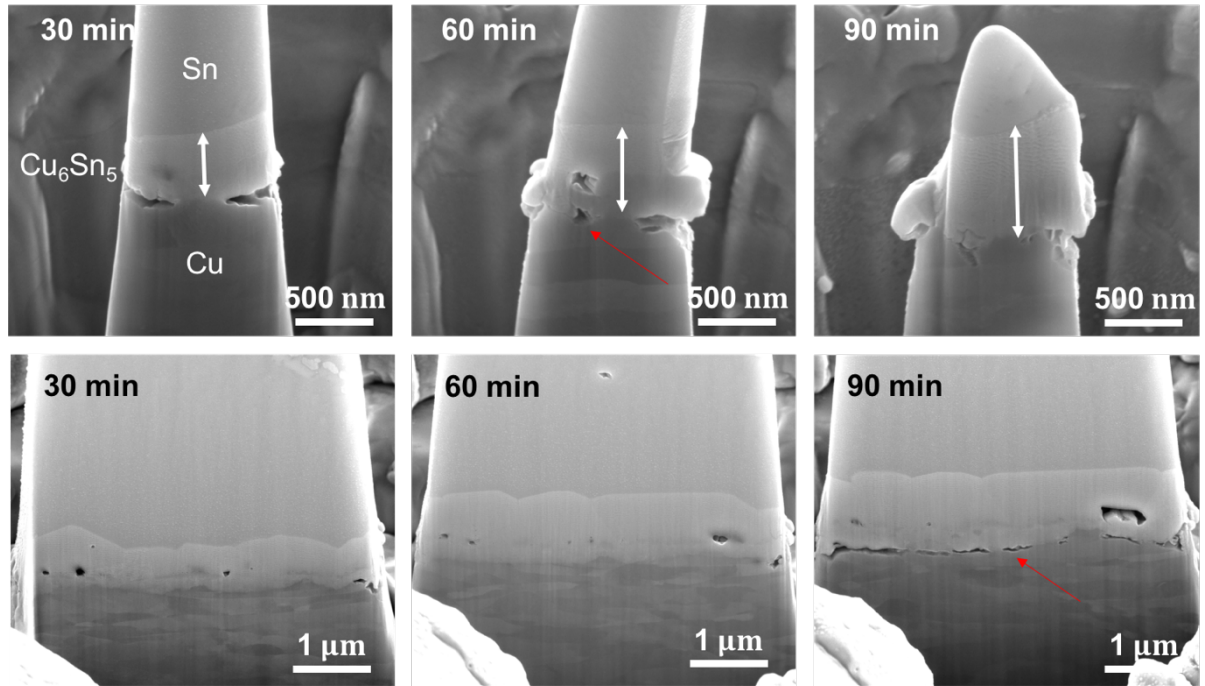


Figure 17. SEM cross-sectional images of 1 and 5 μm pillars after 30, 60, and 90 min annealing under 195°C.

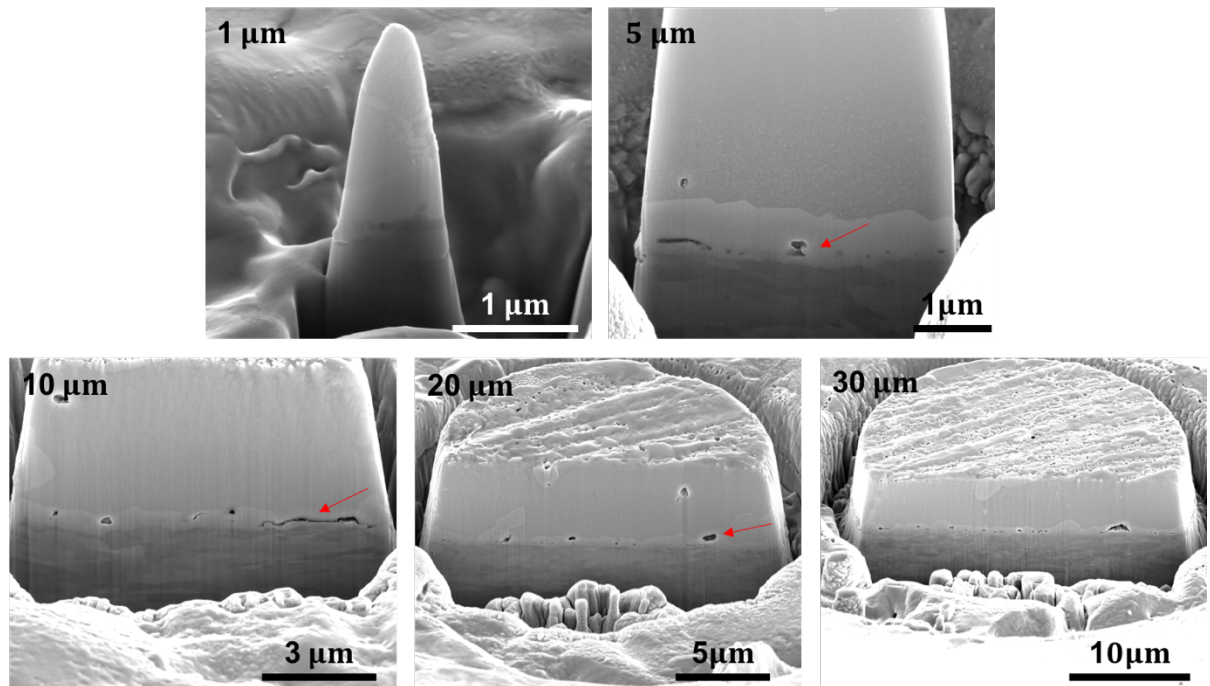


Figure 18. SEM cross-sectional images of different diameter pillars after 60 min annealing under 185°C.

| diameter | $t_{\max}$ | $t_{\min}$ | $t_{\max}-t_{\min}$ | $T_{\max}+t_{\min}$ | %Non-Uniformity |
|----------|------------|------------|---------------------|---------------------|-----------------|
| 1um      | 0.456      | 0.231      | 0.225               | 0.687               | 32.8            |
| 5um      | 0.83       | 0.5        | 0.33                | 1.33                | 24.8            |
| 10um     | 0.94       | 0.23       | 0.71                | 1.17                | 60.7            |
| 20um     | 1.86       | 0.275      | 1.585               | 2.135               | 74.2            |
| 30um     | 1.6        | 0.177      | 1.423               | 1.777               | 80.1            |

Table 2. % non-uniformity calculation results of the IMC layer in different diameter pillars after 60 min annealing under 185°C.

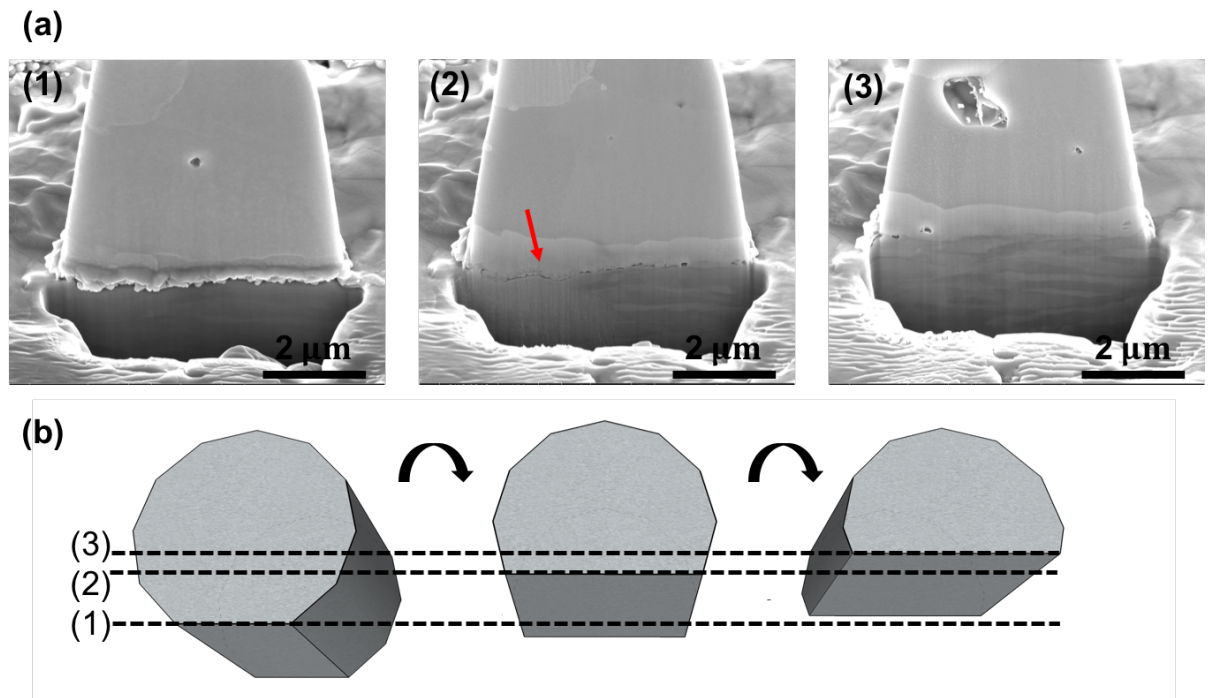


Figure 19. FIB slice-and-view study of the 5 μm pillar after 90 min annealing process.

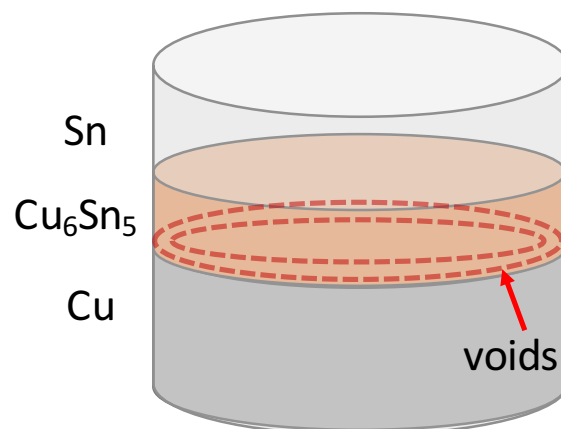


Figure 20. A schematic diagram of the distribution of interfacial voids of the 5 μm pillar.

## Chapter 4: Discussion

### 4.1 Cu/IMC interfacial reaction affected by scaling effect

Referring to the Sn/Cu phase diagram, Sn and Cu solid state reaction will form  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  at the interface between Sn and Cu. In our study, due to short annealing time, only  $\text{Cu}_6\text{Sn}_5$  can be observed. The formation of  $\text{Cu}_6\text{Sn}_5$  is caused by the diffusion of Cu atoms and Sn atoms. Referring to Tu and Thompson's work, Cu atoms are known to be the dominant diffusion species below the melting temperature of Sn. Cu atoms will diffuse to Sn rich side and react with Sn atoms [13]. If the concentration of Cu atoms which diffuse to Sn side is higher enough and reach enough supersaturation,  $\text{Cu}_6\text{Sn}_5$  will nucleate and form a layer. As a result, forming a layer of  $\text{Cu}_6\text{Sn}_5$  is controlled by Cu atoms diffusion.

For a Cu atom or a Sn atom to diffuse, it need a certain activation energy for it to jump to another site. There are several paths available for Cu atoms and Sn atoms to pass through, which are lattice, grain boundary, and free surface. Figure 8 shows a schematic illustration of high-diffusivity paths in a pillar. In general, free surface has the lowest activation energy and have the highest diffusivity. On the contrary, lattice has the highest activation energy and the lowest diffusivity [14]. The relation of activation energy and diffusivity can be presented as below.

$$D_l = D_{l0} \exp \frac{-Q_l}{RT}$$
$$D_{gb} = D_{gb0} \exp \frac{-Q_{gb}}{RT}$$



$$D_s = D_{s0} \exp \frac{-Q_s}{RT}$$

where  $D_l$ ,  $D_{gb}$ , and  $D_s$  are lattice, grain boundary, and free surface diffusivities, respectively.  $Q_l$ ,  $Q_{gb}$ , and  $Q_s$  present activation energy of lattice, grain boundary, and free surface, respectively.  $D_{l0}$ ,  $D_{gb0}$ , and  $D_{s0}$  are the pre-factors.

For BGA and C4 bumps which are large-sized bumps, due to the fact that the surface/volume ratio of these bumps is too small, free surface diffusion can be neglected. Accordingly, the grain boundary diffusion as well as the lattice diffusion would be the dominant diffusion path. However, for microbumps which size is down to a few microns, the surface/volume ratio of the pillar would be increased and the number of grain boundary in the IMC would be decreased, even it is possible that there is no grain boundary in the IMC. Since the grain size of  $\text{Cu}_6\text{Sn}_5$  is typically above 5  $\mu\text{m}$ , which has been measured in C4 bumps, we consider that there would be only one grain of  $\text{Cu}_6\text{Sn}_5$  in the microbump when the pillar diameter is below 5  $\mu\text{m}$ . In this case, free surface diffusion might involve and become the only diffusion path. As a result, the influence of surface diffusion would become greater and greater and the influence of grain boundary diffusion and lattice diffusion would become more and more limited, along the down scaling process of the microbumps.

In our experiment, we collected all the  $\text{Cu}_6\text{Sn}_5$  thickness data of different size pillars in different annealing time at 185°C and 195°C and plot graphs [1]. In Figure 13, we can see there is not much difference in the thickness of IMC after 30 min annealing. This is because the  $\text{Cu}_6\text{Sn}_5$  layer is still very thin and lattice diffusion

remains the dominant diffusion path at this time. Once  $\text{Cu}_6\text{Sn}_5$  layer grows thicker,  $\text{Cu}_6\text{Sn}_5$  layer will become a diffusion barrier for lattice diffusion. As a result, grain boundary diffusion will become the dominant diffusion path. However, we find out that the distribution tends to become a U shape after 60 min and 90 min annealing process. This indicates that when pillar diameter becomes bigger, the thickness of IMC would increase; when pillars become smaller, the thickness of IMC would also increase. As we know, when pillars become bigger, the number of grain boundary will increase resulting in the increase of the thickness of IMC. However, in general, when pillars become smaller, the number of grain boundary will decrease and the thickness of IMC should decrease. Hence, we believe that when the pillars are smaller than 20  $\mu\text{m}$ , surface diffusion has involved and becomes the dominant diffusion path instead of grain boundary diffusion, contributing to the increase of the thickness of IMC.

The process of  $\text{Cu}_6\text{Sn}_5$  formation is known to be diffusion controlled. Besides, we have collected the data of thickness and diffusion time under two different temperatures. As a result, activation energy is able to be calculated. The activation energies of 1  $\mu\text{m}$  and 30  $\mu\text{m}$  pillars are  $0.2 \pm 0.1$  eV/atom and  $0.7 \pm 0.1$  eV/atom, respectively [1]. Although we only have the data under two different temperatures, which might have a large uncertainty, we can still see the large difference in activation energy between 1  $\mu\text{m}$  and 30  $\mu\text{m}$  pillars. Therefore, this results support our conclusion that the dominant diffusion path in 1  $\mu\text{m}$  and 30  $\mu\text{m}$  pillars are different.

## 4.2 IMC uniformity affected by the poor quality of electroplating Sn film

When a Sn layer was electroplated on a Cu plate, several factors might affect the adhesion of electroplating film with substrate, including surface contamination, poor plating layers, and oxidized surface. Poor quality of electroplating film will cause poor adhesion at the interface between Sn layer and Cu layer. With poor interfacial adhesion, voids will remain at the Sn/Cu interface and the effective interface for diffusion will be reduced. According to the literature, Cu atoms are the dominant diffusing species, which diffuse into the Sn layer, examined by marker analysis (1). As a result, voids at the Sn/Cu interface will reduce the effective area of diffusion for Cu diffusion, which will retard IMC formation. Therefore, the uniformity of IMC layer would be worse and this might cause a large numerical error in measuring the average IMC thickness of sample.

To calculate the non-uniformity of IMC layer in different diameter samples, we use the simple non-uniformity formula,

$$\% \text{ non - uniformity} = \frac{(t_{max} - t_{min})}{(t_{max} + t_{min})} \times 100\%$$

, where  $t_{max}$  is the thickness of the thickest part and  $t_{min}$  is the thickness of the thinnest part. The results of non-uniformity are presented in Table 2.

According to Table 2, we can find out that the large-sized sample would have higher % of non-uniformity, which means that it would have worse uniformity, which is opposite to the small-sized sample. Comparing to Figure 16, we can find out that 10, 20, and 30  $\mu\text{m}$  pillars have more voids inside the IMC layer than 1 and 5  $\mu\text{m}$  pillars.

Especially, for 1  $\mu\text{m}$  pillars, we can barely see voids inside the IMC layer. Moreover, we can see that the IMC layer near the voids is rather thin, comparing to where no voids exist. As a result, we can conclude that voids inside the IMC layer did lead to higher percentage of non-uniformity.

Poor interfacial adhesion also leads to another problem on IMC growth. Figure 21 shows a SEM cross-sectional image of a 5  $\mu\text{m}$  pillar with a huge crack across the sample after 185°C annealing process. We can find out that some IMC appears at the center of the pillar. This indicates that the huge crack might serve as the free surface which is the fastest path for atoms diffusion. As a result, the interface between Sn/Cu in small-sized pillars is very unstable and easy to be influenced by the condition of interface. Hence, good quality of electroplating Sn film and more experimental data of IMC thickness are needed for more accurate results.

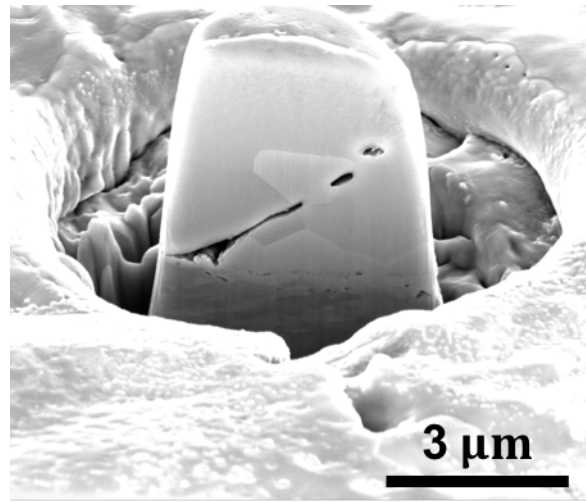


Figure 21. A SEM cross-sectional image of a 5  $\mu\text{m}$  pillar with a huge crack across the sample after 1850C annealing process.

### 4.3 The formation of Kirkendall voids around surface induced by inter-diffusion.

According to chapter 1.6, we know that Kirkendall effect is defined as the marker motion caused by uneven inter-diffusion fluxes. In Darken's analysis, he concluded that Kirkendall effect is caused by the lattice shift during uneven inter-diffusion process. No voids formation can be found in his analysis base on the assumption that vacancies are distributed at equilibrium everywhere in the sample. However, in the real case, vacancies are not distributed at equilibrium everywhere. Accordingly, vacancies would have chance to reach supersaturation and nucleate voids in the sample. These voids are so-called Kirkendall voids or Frenkel voids.

Through FIB slice-and-view study, shown in Figure 19 and 20, we can see that there are several voids formed at the interface between  $\text{Cu}_6\text{Sn}_5$  and Cu, which are considered as the Kirkendall voids. These voids are mainly located at the circumference area, shown in Figure 20, indicated that they are caused by uneven surface inter-diffusion. However, for solder joint technology, the formation of these voids is not favored due to the fact that the voids will decrease the mechanical strength of a solder bump. Hence, these voids formation would cause serious reliability issues and become a future concern in reliability.

#### 4.4 Kinetic model of IMC formation with surface diffusion involving

To present a kinetic model of IMC growth, we assume that the phase growth is diffusion-controlled and the compound is layered growth. And we only consider the diffusion of B (or Cu) atoms, which means that the diffusion is from B to A in Figure 19. The concentration of B atoms, which represented by  $C_B$ , in A can be neglected. The compound phase is represented by I and the concentration at the two interface are represented by  $C_R^{(i)}$  and  $C_L^{(i)}$ .  $C_R^{(i)}$  and  $C_L^{(i)}$  are constants and correspond to the concentration in equilibrium phase diagram due to diffusion-controlled growth. Figure 22 depicts the formation profile of IMC between A and B.

For i phase, we have

$$J_L^{(i)} = -\tilde{D}_L^{(i)} \frac{C_R^{(i)} - C_L^{(i)}}{x_R^{(i)} - x_L^{(i)}} \cong -\tilde{D}_L^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}}$$

$$J_G^{(i)} = -\tilde{D}_G^{(i)} \frac{C_R^{(i)} - C_L^{(i)}}{x_R^{(i)} - x_L^{(i)}} \cong -\tilde{D}_G^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}}$$

$$J_S^{(i)} = -\tilde{D}_S^{(i)} \frac{C_R^{(i)} - C_L^{(i)}}{x_R^{(i)} - x_L^{(i)}} \cong -\tilde{D}_S^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}}$$

For the traditional kinetic model, it only has the lattice diffusion (L) analysis. As a result, we add two equations of grain boundary diffusion (G) and surface diffusion (S) to modify it.

We can have the total flux passing through i phase. It would be

$$J^{(i)} = \frac{J_L^{(i)} \times A_L + J_G^{(i)} \times A_G + J_S^{(i)} \times A_S}{A_L + A_G + A_S}$$

where A represents area which flux passing through.

After replacing J by effective diffusivity, the equation can be simplified as

$$\tilde{D}^{(i)} = \frac{\tilde{D}_L^{(i)} \times A_L + \tilde{D}_G^{(i)} \times A_G + \tilde{D}_S^{(i)} \times A_S}{A_L + A_G + A_S}$$

And we can have the equation of total flux.

$$J^{(i)} = -\tilde{D}^{(i)} \frac{C_R^{(i)} - C_L^{(i)}}{x_R^{(i)} - x_L^{(i)}} \cong -\tilde{D}^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}}$$

We use these two equation to illustrate the growth of i phase at the left and right boundaries.

$$\begin{aligned} (C_L^{(i)} - 0) \frac{dx_{Ai}}{dt} &= -\tilde{D}^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}} - 0 \\ (C^B - C_R^{(i)}) \frac{dx_{iB}}{dt} &= 0 - \left( -\tilde{D}^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}} \right) \end{aligned}$$

After rearranging the equations above, we have

$$\frac{d(x_{iB} - x_{Ai})}{dt} = \left( \frac{1}{C^B - C_R^{(i)}} + \frac{1}{C_L^{(i)}} \right) \tilde{D}^{(i)} \frac{\Delta C^{(i)}}{\Delta x^{(i)}}$$

Although we can solve this equation by numerical analysis, we still cannot determine the concentration gradient in the stoichiometric compound,  $\Delta C^{(i)} \cong C_R^{(i)} - C_L^{(i)} \cong 0$ , which is unmeasurable. However, from another point of view, we knew that the formation energy of IMC across the thickness of IMC is where the driving force or the chemical potential gradient coming from. As a result, we can apply Wagner diffusivity analysis (by using chemical potential gradient) to overcome the unmeasurable  $\Delta C^{(i)}$  [1][17].



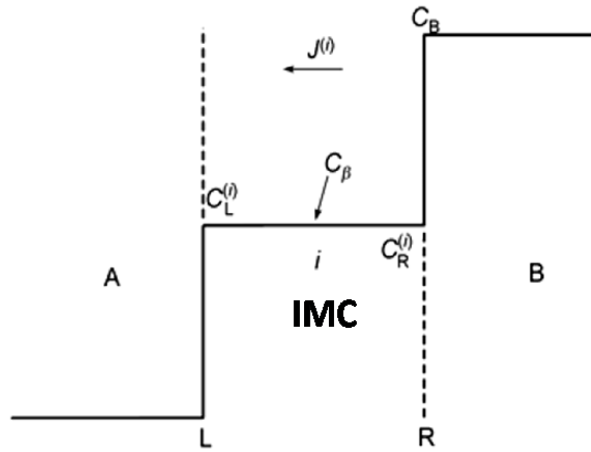


Figure 22. the formation profile of IMC between A and B [17].

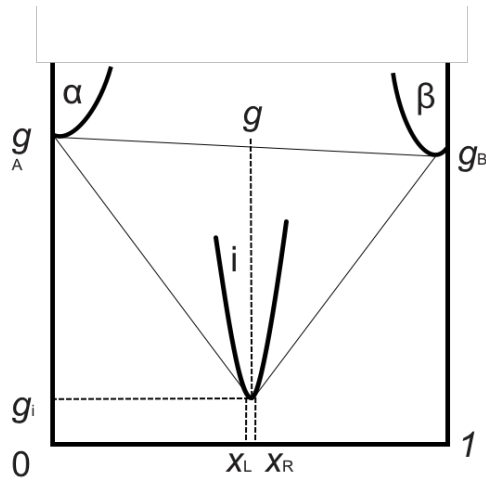


Figure 23. schematic diagram of free energy diagram of A( $\alpha$ -phase) and B( $\beta$ -phase) and an intermetallic compound (i-phase).

#### 4.5 A simple model for IMC growth in pillars smaller than 1um

Generally speaking, the diameter of one  $\text{Cu}_6\text{Sn}_5$  grain in C4 is about 5um. As a result, in 1 um pillar, we expect that there should be only a single grain of  $\text{Cu}_6\text{Sn}_5$  inside the pillar. Base on this assumption, we build a simple model for IMC growth without taking into account the lattice diffusion and grain boundary diffusion. Because we assume lattice diffusion is too small and there is no grain boundary existing inside 1 um pillar. According to literature, we know that Cu will diffuse interstitially in Sn. As a result, we can conclude that when Cu atoms diffuse through the surface of the IMC to the Sn side, these Cu atoms will diffuse interstitially into Sn and react to grow the internal  $\text{Cu}_6\text{Sn}_5$  layer, so that the  $\text{Cu}_6\text{Sn}_5$  can form a rather uniform layer in the pillar. We note that if there is only surface diffusion, we expect a coating layer of  $\text{Cu}_6\text{Sn}_5$  can form on the pillar surface of Sn. Figure 24 illustrate the mechanism of Cu diffusion inside a 1um pillar. Therefore, in this simple model, we only consider the contribution of surface diffusion and interstitially diffusion.

We assume that the atomic diameter is  $d$ , in a time  $t$  and the circumference of pillar is  $2\pi r$ . By these factors, we are able to have an equation from the definition of the flux in surface diffusion.

$$\#\text{Cu}_{\text{atom}} = J_s \times 2\pi r \times d \times t$$

We assume the  $\text{Cu}_6\text{Sn}_5$  growth rate is  $\frac{\Delta h}{\Delta t}$ , as shown in figure 24(b), and unit cell volume of one  $\text{Cu}_6\text{Sn}_5$  molecule is  $\Omega$ . By these assumption, we are able to calculate how many number of atoms in a layer of thickness of “h” of  $\text{Cu}_6\text{Sn}_5$ . And we can have

an equation as below.

$$\#Cu_{\text{atom}} = \pi r^2 h \frac{6}{\Omega}$$

By combining these two equations above, we can have

$$J_s \times A \times t = \#Cu_{\text{atom}} = \frac{V}{\Omega}$$

$$J_s = 3 \frac{r h 1}{d t \Omega}$$

According to Fick's first law, we can have an equation of the flux contributed by surface diffusion.

$$J_s = -D_s \frac{\Delta C}{\Delta x}$$

Although, in diffusion-controlled diffusion,  $\Delta C$  is an immeasurable term, we still can roughly assume that  $\Delta C$  is about 1% in the growth of  $Cu_6Sn_5$  owing to the  $Cu_6Sn_5$  composition range in the Sn-Cu equilibrium phase diagram, shown in figure 4.

Table 3 listed the measurement results of  $\Delta h$  and  $\Delta x$ , which are the thickness growth and the average value of  $\Delta h$ , respectively. By having the data of  $\Delta h$ ,  $\Delta x$ , and time, we are able to calculate the Cu surface diffusivity on  $Cu_6Sn_5$  [1]. We use the data at 60-90min, as an example, to calculate the Cu surface diffusivity in a 1  $\mu m$  pillar within this period. As we know, the radius  $r=0.5\mu m$ , the atomic diameter  $d=0.2556nm$ ,  $\Delta t=30min$ , and unit cell volume of  $Cu_6Sn_5$   $\Omega=0.0766 nm^3$ . According to the table 3, we can have  $\Delta h=0.12\mu m$  and  $\Delta x=0.7\mu m$ . By rearranging the equation above, we can have the equations as below,

$$D_s = 3 \frac{r h 1 \Delta x}{d t \Omega \Delta C}$$

By plugging all the terms, we can have

$$D_s = 3 \times \frac{5 \times 10^{-5}}{2.556 \times 10^{-8}} \times \frac{1.2 \times 10^{-5}}{1800} \times \frac{1}{7.66 \times 10^{-23}} \times \frac{7 \times 10^{-5}}{\Delta C}$$

Due to the fact that  $\Delta C$  is unmeasurable, we assume

$$\Delta C = \frac{0.01}{\Omega}$$

And we can calculate the  $D_s$  is equal to  $2.7 \times 10^{-7} \text{ cm}^2/\text{s}$  at  $185^\circ\text{C}$ .

However, measuring the thickness of IMC through SEM still have large uncertainty. If the thickness of IMC is below  $0.1 \mu\text{m}$ , the uncertainty caused by SEM would become a problem.

By this simple model, we can calculate not only the surface diffusivity of Cu on IMC, but also the surface diffusivity of other noble metals and near-noble metals which diffuse in group IV elements interstitially, shown in Table 4. Thus, we believe that this simple model could have a broader application [1].

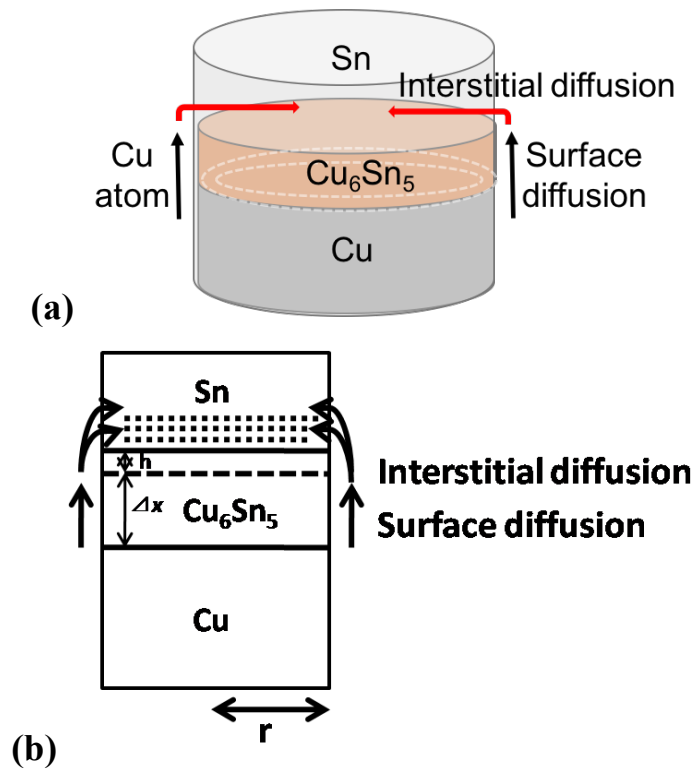


Figure 24. A schematic diagram to show the diffusion path for IMC growth in a 1  $\mu\text{m}$  pillar [1].

| $\Delta t$ (min) | $\Delta h$ ( $\mu\text{m}$ ) | $\Delta x$ ( $\mu\text{m}$ ) | $D_s$ ( $\times 10^{-7} \text{ cm}^2/\text{s}$ ) |
|------------------|------------------------------|------------------------------|--|
| 0–30             | 0.46                         | 0.23                         | 3.4  |
| 30–60            | 0.18                         | 0.55                         | 3.2  |
| 60–90            | 0.12                         | 0.70                         | 2.7  |

Table 3. The measurement results of  $\Delta h$  and  $\Delta x$  and calculate  $D_s$  in different period of time [1].

|            |                |                |
|------------|----------------|----------------|
| Conductor  | Contact        |                |
| Cu, Ag, Au | Ni, Pd, Pt     | Fast diffusion |
|            | Si, Ge, Sn, Pb | ↓              |
|            | Solder         |                |

Table 4. Metallic elements commonly found in a semi- conductor device [12].

## Chapter 5: Conclusion

### 5.1 Conclusion

In our study, we electroplate Sn on Cu plate and use FIB to fabricate the pillar structure in diameter of 1, 5, 10, 20, and 30 $\mu$ m. After 30, 60, and 90 min annealing under 175, 185, and 195 $^{\circ}$ C, Cu will react with Sn forming IMC which is  $\text{Cu}_6\text{Sn}_5$ . For the sample analysis, we applied FIB to take the cross-sectional SEM images of pillars and use software Image J to measure the thickness of IMC layer.

Base on the measurement and morphology observation, we find out that the thickness of IMC increases as the diameter of pillar decreases from 20  $\mu$ m to 1  $\mu$ m. This implies that when pillar size is smaller than 20  $\mu$ m, surface diffusion will have a significant contribution to the Sn/Cu reaction. Besides, we did the FIB slice-and-view study to observe the distribution of Kirkendall voids. Most of the Kirkendall voids locate at the peripheral area of pillar near the surface. This indicates that these Kirkendall voids are formed during the surface inter-diffusion. Not only Kirkendall voids, but there are also other large voids caused by poor quality of electroplating Sn film inside the IMC layer, which leads to poor uniformity of the IMC layer.

Base on the discussion that surface diffusion will involve in small size pillar, we modified the traditional kinetic model by adding the flux contribution from grain boundary diffusion and surface diffusion.

Finally, we discuss the diffusion mechanism of Cu atoms in a small pillar with no

grain boundary in the microstructure. To illustrate this mechanism, we make a simple model which only take surface and interstitial diffusion into account. By using this model, we are able to calculate the surface diffusivity of Cu atoms with the growth rate and the thickness of the IMC.



## References

- [1] Liu, Yingxia, Ying-Ching Chu, and K. N. Tu. "Scaling effect of interfacial reaction on intermetallic compound formation in Sn/Cu pillar down to 1  $\mu\text{m}$  diameter." *Acta Materialia* 117 (2016): 146-152.
- [2] Szendiuch, Ivan. "Development in electronic packaging—moving to 3D system configuration." *Radioengineering* 20.1 (2011): 214-220.
- [3] Anjoh, Ichiro, Asao Nishimura, and Shuji Eguchi. "Advanced IC packaging for the future applications." *IEEE Transactions on Electron Devices* 45.3 (1998): 743-752.
- [4] Kang, Sung K., Peter Gruber, and Da-Yuan Shih. "An overview of Pb-free, flip-chip wafer-bumping technologies." *JOM Journal of the Minerals, Metals and Materials Society* 60.6 (2008): 66-70.
- [5] Valentin, P. O. P. A. "FLIP-CHIP TECHNOLOGY—A STEP BEYOND IN SEMICONDUCTOR INDUSTRY."
- [6] Knickerbocker, John U., et al. "Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection." *IBM Journal of Research and Development* 49.4.5 (2005): 725-753.
- [7] "Flip chip." Wikipedia. Wikimedia Foundation. <[https://en.wikipedia.org/wiki/Flip\\_chip](https://en.wikipedia.org/wiki/Flip_chip)>.
- [8] Saunders, N., and A. P. Miodownik. "The Cu-Sn (copper-tin) system." *Journal of Phase Equilibria* 11.3 (1990): 278-287.

- [9] Nogita, K., et al. "Kinetics of the  $\eta$ - $\eta'$  transformation in Cu 6 Sn 5." *Scripta Materialia* 65.10 (2011): 922-925.
- [10] Tu, K. N. "Cu/Sn interfacial reactions: thin-film case versus bulk case." *Materials Chemistry and Physics* 46.2-3 (1996): 217-223.
- [11] Tu, K. N. "Interdiffusion and reaction in bimetallic Cu-Sn thin films." *Acta Metallurgica* 21.4 (1973): 347-354.
- [12] Tu, K. N., and R. D. Thompson. "Kinetics of interfacial reaction in bimetallic Cu-Sn thin films." *Acta Metallurgica* 30.5 (1982): 947-952.
- [13] Tu, King-Ning. *Electronic thin-film reliability*. Cambridge University Press, 2010.
- [14] Shewmon, Paul, ed. *Diffusion in solids*. Springer, 2016.
- [15] Kirkendall, E. O., and A. D. Smigelskas. "Zinc diffusion in alpha brass." *AIME TRANS* 171 (1947): 130-142.
- [16] "Kirkendall Effect." Wikipedia. Wikimedia Foundation. <[https://en.wikipedia.org/wiki/Kirkendall\\_effect](https://en.wikipedia.org/wiki/Kirkendall_effect)>.
- [17] Tu, King-Ning, and Andriy M. Gusak. *Kinetics in nanoscale materials*. John Wiley & Sons, 2014.