UNIVERSITY OF CALIFORNIA

Santa Barbara

N-Polar Deep Recess MISHEMTs for mm-Wave Applications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

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December 2018

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by

Steven M. Wienecke Jr.

Dedicated to my Mother, Father, Alex, and Eric

Thank you for all your support through all the years, if you'd even given me just 1/100th of the support you have in my life I'd still be forever grateful.

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- Wrote grant proposals and presented results to program manager.

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Engineering Technician: Electronic Materials and Devices June 2010 – Aug 2010

- Characterized the effects of partial strain relaxation on the optical properties in lattice mismatched semipolar InGaN films with polarization dependent photoluminescence measurements.
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PUBLICATIONS

Journal Publications

- **S. Wienecke**, B. Romancyzk, M. Guidry, H. Li, X. Zheng, E. Ahmadi, K. Hestroffer, S. Keller, and U. K. Mishra, "N-polar GaN cap MISHEMT with record power density exceeding 6.5 W/mm at 94 GHz," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 359-362, Jan 2017. DOI: 10.1109/LED.2017.2653192
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Conference

- **S. Wienecke**, B. Romanczyk, M. Guidry, H. Li, X. Zheng, E. Ahmadi, K. Hestroffer, S. Keller, and U. K. Mishra, "Effect of Sidewall Capacitance on N-Polar GaN Cap MISHEMT Performance," *2016 Lester Eastman Conference on High Performance Devices (LEC)*, Bethlehem, PA, August 2016. **(received Best Student Paper Award)**
- **S. Wienecke**, B. Romanczyk, M. Guidry, H. Li, X. Zheng, E. Ahmadi, K. Hestroffer, S. Keller, and U. K. Mishra, "N-Polar GaN Cap MISHEMT with Record 6.7 W/mm at 94 GHz," *74th Device Research Conference*, June 2016.
- **S. Wienecke**, B. Romanczyk, M. Guidry, H. Li, X. Zheng, E. Ahmadi, K. Hestroffer, S. Keller, and U. K. Mishra, "N-Polar Deep Recess HEMTs for W-Band Power Applications," *42nd International Symposium on Compound Semiconductors* (*ISCS*), Santa Barbara, CA, July 2015, pp. 197−198.
- **S. Wienecke**, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, and U. K. Mishra, "Optimization of Back-Barrier Doping in Graded AlGaN N-Face HEMTs," *2014 Lester Eastman Conference on High Performance Devices (LEC)*, Ithaca, NY, August 2014. **(received Best Student Poster Award)**
- B. Romanczyk, **S. Wienecke**, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, "W-band N-polar GaN MISHEMTs with high power and record 27.8% efficiency at 94 GHz," *Electon Devices Meeting (IEDM)*, Dec. 2016

HONORS AND AWARDS

University of California, Santa Barbara: Best student paper at the 2016 Lester Eastman Conference on High Performance Devices, Best student poster presentation at the 2014 Lester Eastman Conference on High Performance Devices.

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ABSTRACT

N-Polar GaN Deep Recess MISHEMTs for mm-Wave Applications

by

Steven M. Wienecke Jr.

GaN based high electron mobility transistors (HEMTs) have emerged as a leading technology for mm-wave (30-300 GHz) wireless applications. Specifically, great interest has been shown in GaN transistors for high power transmitter applications in the W-band portion of the frequency spectrum (75-110GHz) where atmospheric attenuation of RF signals experiences a local minimum. To date, reports on W-band GaN HEMTs and monolithic microwave integrated circuits (MMICs) have primarily featured devices fabricated in the Ga-Polar (0001) orientation. In this work, the advantages of N-Polar GaN are exploited to produce a metal-insulator-semiconductor (MIS-HEMT) exhibiting (at the time) record high power amplification performance at 94 GHz.

The key difference between Ga-Polar and N-Polar HEMTs is the orientation of the polarization fields. In N-Polar, the field orientation enables the fabrication of a novel recessed gate structure with the addition of an unintentionally doped (UID) GaN cap layer in the device access regions. This GaN cap serves a dual purpose. First, it effectively removes the DC-to-RF dispersion commonly seen in III-N transistors (dispersion in this sense refers to the phenomena where the device's large signal RF power performance is significantly

worse than that predicted from static DC measurements). The GaN cap removes this dispersion with a smaller capacitive penalty than traditional methods typically used in Ga-Polar transistors. Secondly, the GaN cap acts to reduce surface depletion, significantly reducing sheet resistance in the access regions. By reducing both the parasitic resistive and capacitive elements of the transistor, excellent large signal RF performance is achieved at very high frequencies.

In this work, the device concept is introduced and the fabrication procedure is detailed. Several aspects of the device structure are examined, optimized, and record (at the time) performance results are presented.

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Chapter 1

Introduction

Chapter 1.1 – Introduction to GaN:

The first reports on GaN dates all the way back to 1928 in Chicago Illinois by W. C. Johnson *et al* [1]. However, research in GaN devices did not occur until 1971 when Pankove began working on the first GaN light emitting diodes (LEDs). After Pankove's initial investigations [2], progress in GaN-based devices was sluggish for many years due to the poor material quality and inability to grow p-type doped material. Improvements in the growth techniques in the 1980's and early 1990's by Akasaki, Amano, and Nakamura dramatically improved the epitaxial quality of III-N epitaxy [3-4]. Further work from these researchers also led to the successful p-type doping of GaN [5-6]. After these advances, photonic device development for LEDs and laser diodes (LDs) exploded [7-11]. Prior to the successful growth of III-N based LEDs and LDs, there was not any semiconductor family with a direct bandgap which could emit in the blue or UV portions of the spectrum. With the successful fabrication of III-N base LEDs and LDs that can emit in this range, a huge commercial industry worth over $10 billion dollars has developed over the past 2 decades (Fig. 1.1) [12-13].

GaN and its alloys with InN and AlN posses a direct band gap ranging from 0.7 eV (InN) all the way to 6.2 eV (AlN) [14-15]. Theoretically this enables photonic devices which can emit photons anywhere from the IR to the UV portions of the electromagnetic spectrum all using only the III-N system of materials. With such qualities it makes sense that most of the early work in the III-Nitrides focused on developing the technology for use in photonic devices. However, GaN and its alloys with AlN and InN have many attractive properties for

electronic device applications as well. Table 1.1 compares some of the GaN material properties relevant to high power RF electronic devices with other semiconductors [16]. The high critical E-Field of GaN relative to

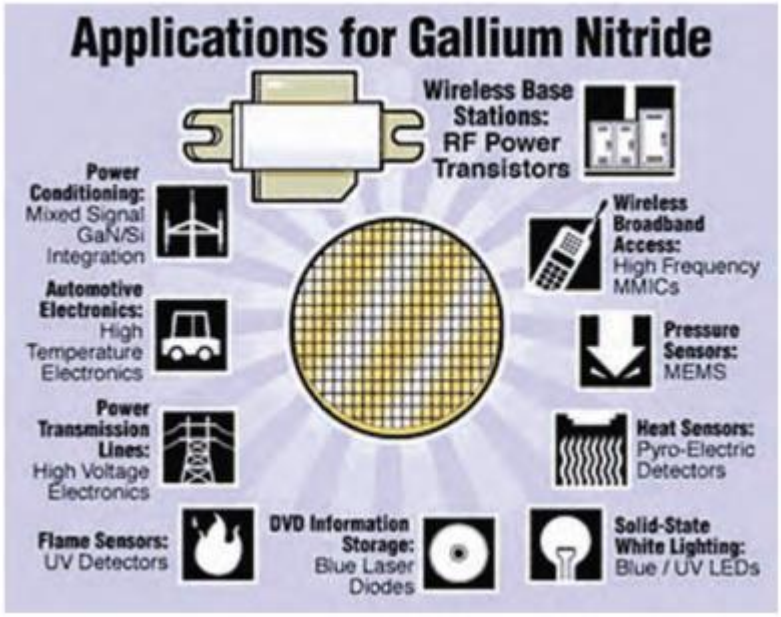

Fig. 1.1: Major current and/or projected markets for Nitride-based devices [12].

the other materials in this table enables large breakdown voltage transistors to be created with relatively small physical dimensions, reducing the parasitics of the device and allowing for better large signal gain at high frequencies. In addition, the III-N system has high values of spontaneous and piezoelectric polarization, leading to a large net polarization charge density at any heterointerface between GaN and one of its III-N alloys [17]. This enables very high two-dimensional electron gas (2DEG) densities over $1 \cdot 10^{13}$ cm^{-2} with reasonably high electron mobilities and saturation velocities to be induced at these heterointerfaces. The high 2DEG density and mobility leads to low extrinsic resistances and better large signal gain at high frequencies. The large 2DEG density and reasonably high saturation velocities lead to higher output current densities. Further, the wide range of accessible bandgaps along with the net

polarization charges at heterointerfaces in the III-N system offer multiple degrees of freedom in the electronic device design which simply do not exist in other semiconductor families. Together, these properties have historically made III-N high-electron-mobility-transistors (HEMTs) an attractive candidate for RF power amplification purposes [18].

Material	Bandgap (eV)	ε	E_c (MV/cm)	μ at 300K ($cm^{-2}V^{-1}s^{-1}$)	v_{sat} (v_{peak}) (cm/s)	2DEG density (cm^{-2})
Si	1.1	11.7	0.3	1500	1 (1)	$<5x10^{12}$
InP	1.35	12.5	0.5	5400	1 (2.3)	$< 5x10^{12}$
GaAs	1.43	13.1	0.4	8,500	1 (2.1)	$<5x10^{12}$
4H-SiC	3.3	9.7	3	700	2 (2)	NA
GaN	3.4	9.5	**3.3**	**2100* (2DEG)**	**1.3 (2.5)***	**~1-2e13**

Table 1.1: Comparison of material parameters relevant to RF electronic devices across several different semiconductors. (* the peak saturation velocity of GaN was predicted theoretically and has not been experimentally demonstrated) [16].

Chapter 1.2 – RF Amplifier Key Performance Metrics:

The goal of this thesis is to build the best possible semiconductor transistor for RF power amplification purposes in the W-Band (75-110 GHz) range of frequencies. In order to better understand the material in this dissertation, it is useful to review the most important aspects of RF power amplifier device fundamentals. Transistors for RF amplification purposes should be capable of producing high large signal gain, high efficiencies, and high output RF powers at the frequency range of interest. Equations for describing an RF transistor amplifier's efficiency and output RF power at a particular frequency are given below [19].

$$DE = \frac{P_{RF,out}}{P_{DC}} = \frac{P_{RF,out}}{V_{DC} \cdot I_{DC}} \tag{1.1}$$

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} = \frac{P_{RF,out}}{P_{DC}} \cdot \left(1 - \frac{1}{G}\right) = DE \cdot \left(1 - \frac{1}{G}\right) \tag{1.2}$$

$$P_{RF,out} = \frac{\left(V_{DSQ} - V_{knee}\right) \cdot I_{DSS}}{4} \tag{1.3}$$

In equation (1.1) DE = drain efficiency, P_{DC} is the mean dissipated DC power density, V_{DC} is the mean DC voltage, and I_{DC} is the mean DC current density. In equation (1.2) PAE = power-added efficiency, $P_{RF,out}$ = output RF power density, $P_{RF,\text{in}}$ = input RF power density, and G = power gain at the frequency of interest. In equation (4.3), V_{DSQ} = quiescent source-drain voltage bias, V_{knee} = knee voltage of the transistor's I-V curve, and I_{DSS} = saturation current density of the transistor.

The way in which a transistor amplifier is operated determines its Amplifier "Class". There are many different types of amplifier classes, but the three which will be talked about here are Class A, Class B, and Class AB. In Class A amplifiers, the device is biased normally-on, at about half the peak-peak output current and half the peak-peak output voltage (Fig. 1.3). The main advantage of Class A operation is that it offers the highest linearity of all Amplifier Classes. However, because the transistor is always on, the peak efficiency Class A operation can achieve is only ≈ 50%. This is Class A's biggest drawback.

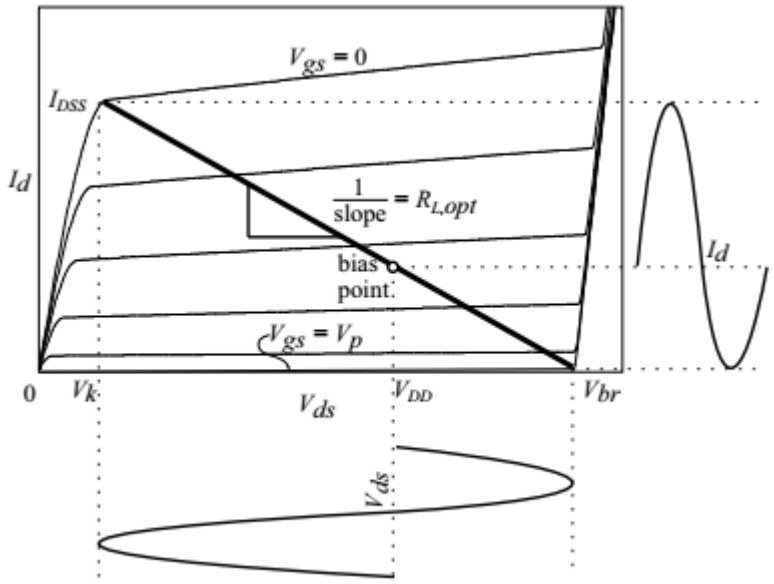

Fig. 1.3: Transistor operating in a Class A amplifier configuration with load line chosen for maximum power (Adapted from Mishra and Singh [20]).

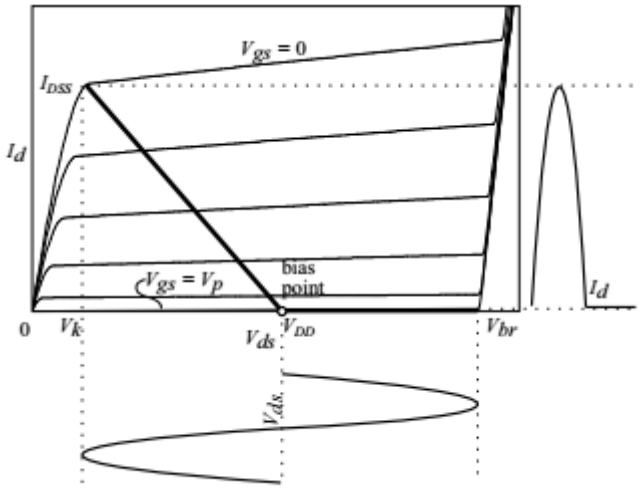

Fig. 1.4: Transistor operating in a Class B amplifier configuration (Adapted from Mishra and Singh [20]).

In Class B amplifiers, the device is biased at pinch-off (Fig. 1.4). The conduction angle (total number of degrees out of 360 at which the device is conducting) is 180° in this class of amplifier, meaning that the individual transistor device conducts ½ the time, and is in the cut-off regime the other ½ of the time. Because the device is only dissipating DC power

½ the time, less DC power is consumed. This enables amplifiers of this class to theoretically achieve efficiencies as high as π/4 (~78.6%). The drawback of Class B is that it is less linear than Class A. Further, it requires that the transistor has high RF transconductance at or near pinch-off, which is not always the case. Class AB amplifiers are a compromise between Class A and Class B. Here, the conduction angle is $180^o < \theta < 360^o$. It is a compromise between efficiency and linearity. Further, it relaxes the requirement of having high transconductance right at pinch-off.

To achieve the highest possible drain efficiency allowable within any of the aforementioned Amplifier Classes, the ratio between a transistor's breakdown voltage and RF knee voltage should be high. A load line which maximizes power delivered to the load typically will cross, or at least come close to, the knee of the transistor's I-V. Therefore, the DC power dissipated at voltages below the knee voltage do not contribute to $P_{RF,out}$, and thus should be minimized for high drain efficiencies. Moreover, having a higher breakdown voltage allows the device to be biased to higher quiescent source-drain voltages, increasing the total $P_{RF,out}$ and reducing the hit taken to *DE* from the power dissipated below the knee voltage. Further, the breakdown voltage sets the limit on the peak RF output power that can be expected from a given transistor device. For a Class A amplifier, $P_{RF,out,Max}$ is given by equation 1.4.

$$P_{RF,out,Max} = \frac{\left(V_{DS,Br} - V_{knee}\right) \cdot I_{DSS}}{8} \tag{1.4}$$

An inherent requirement for high *DE* in III-N transistors is the ability to control DC-to-RF dispersion. This dispersion is due to trap states in the device which cause the RF output power density to be less than what one would predict from the DC performance of the transistor in combination with equations 1.1 – 1.4 [21]. DC-to-RF dispersion plays a very large role in

III-N transistors and is explained in much greater detail in Chapter 3 of this thesis. The V_{knee} and I_{DSS} that matter in the above equations are the RF values at the application frequency. Drain-side dispersion will increase the RF V_{knee}, which will decrease both the maximum achievable RF output power as well as the drain efficiency of the device. Source-side dispersion will decrease the RF I_{DSS} and decrease the $P_{RF,out,Max}$. Therefore, controlling dispersion at the application frequency is critical for device performance. Successfully controlling dispersion while simultaneously achieving reasonable large signal gain at 94 GHz is an extremely important accomplishment of the work contained in this dissertation.

Power added efficiency (equation 1.2) takes into account not only the dissipated DC power, but also the input RF power required for a given output RF power. Because of this it gives a more accurate depiction of the transistor's actual overall efficiency within the circuit. As equation 1.2 shows, in order to achieve the highest possible *PAE* for a given Amplifier Class, the transistor amplifier must have both high drain efficiency and high power gain at the application frequency. *DE* is explained in the previous paragraph. Power gain *G* is related to how much an input RF signal will be amplified by the transistor amplifier at a particular frequency. During load pull measurements here at UCSB, the Maury Microwave software provides information on the transducer gain G_T of the transistor at each of the quiescent bias points. This transducer gain is related to the power gain of the transistor via equation 1.5.

$$G = 10^{\frac{G_T}{10}} \tag{1.5}$$

The transducer gain itself is related to (but not necessarily equal to) the unilateral gain of the transistor amplifier *U*. A good figure of merit for unilateral gain is the maximum frequency of oscillation, or f_{max} of the transistor (equation 1.6). This represents the frequency at which the unilateral gain becomes unity.

$$f_{max} = \frac{\frac{gm_{ext}}{2\pi * \left(C_{gs} + C_{gd}\right)}}{\sqrt{\frac{4}{R_{ds}} * \left(R_g + R_s + R_i\right) + 4\pi * f_T * C_{gd} * \left(2 * R_g + R_s + R_i\right)}} \tag{1.6}$$

As an amplifier is meant to provide gain/amplify an incoming signal, the f_{max} of the transistor amplifier signifies the upper limit at which the transistor can behave as an amplifier. For reasonable power gains, the transistor amplifier must operate well below its f_{max}. Another useful figure of merit is the short-circuit current cut-off frequency f_T.

$$f_T = \frac{gm_{ext}}{2\pi * \left(\left(C_{gs} + C_{gd}\right) * \left(1 + \frac{R_s + R_d}{R_{ds}} + C_{gd} * g_m * \left(R_s + R_d\right)\right)\right)} \tag{1.7}$$

Chapter 1.3 – Historical Development of GaN for RF Amplification

Purposes:

As mentioned in Section 1.1, the high critical electric fields, large 2DEG densities, and reasonably high electron saturation velocities and mobilities make III-N based HEMTs an attractive candidate for RF power amplification purposes. The first demonstration of a 2-dimensional electron gas at an AlGaN/GaN heterojunction was made by Khan in 1992 [22]. This was quickly followed by the first DC and small-signal RF measurements of an AlGaN/GaN HEMT in 1993 and 1994, respectively, by the same group [23-24].

In 1996, the first large signal RF power data from an AlGaN/GaN HEMT was reported by Wu *et al* [25]. In this work he demonstrated a peak RF output power density of 1.1 W/mm at 2 GHz. For the next few years, the output power density increased steadily due to improved

growth techniques, better epitaxial quality, and more advanced processing techniques (Fig. 1.6).

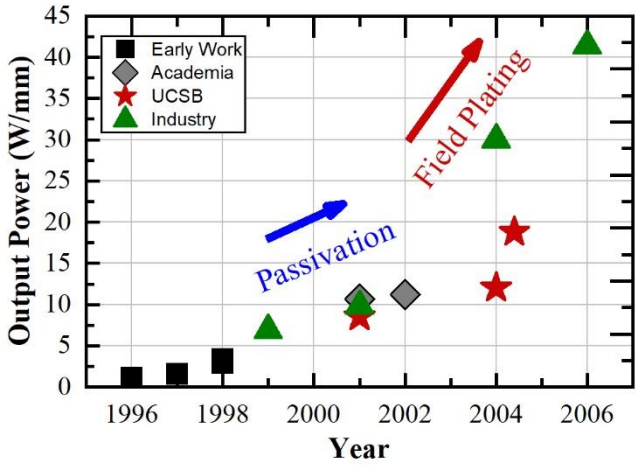

Fig. 1.6: Peak output power density versus year in III-N HEMTs. Can see large increases in power performance with introduction of techniques to reduce the DC-to-RF dispersion seen in the device [25-37].

However, the power density obtained over this period was still much lower than what one would predict if they inserted the DC values of breakdown voltage, knee voltage, and saturation current density into equation 1.4. This lower than expected RF output power density was due to DC-to-RF dispersion which can increase the RF knee voltage and/or decrease the RF current density of the transistor during large signal operation. Both of these potential effects reduce the $P_{RF,out}$, gain, and efficiency of the transistor amplifier. As mentioned in Section 1.2, DC-to-RF dispersion is caused by trap states locate in either the bulk semiconductor, at semiconductor heterointerfaces, or in the access regions at the surface of the III-N HEMT [38]. However, in many cases trap states in the access regions of the surface appear to be the dominant cause of this dispersion [21]. This was demonstrated in 2000 by [39] where application of an *ex situ* PECVD SiN dielectric passivation layer doubled the $P_{RF,out}$ of the authors' III-N HEMTs. Apparently this PECVD SiN passivation layer reduced the trap density at the surface of the III-N HEMT. By 2002, use of a PECVD SiN

passivation layer for reduced dispersion combined with fabrication of the AlGaN/GaN HEMT on a SiC substrate for reduced self-heating resulted in a $P_{RF,out}$ greater than 11 W/m [32]. The adoption of field plating in 2003 further decreased the DC-to-RF dispersion in the device [33-35]. Field plating also increased the transistor's breakdown voltage. By 2006, the PECVD SiN passivation in conjunction with field plating resulted in a huge increase in $P_{RF,out}$ with Wu *et al.* demonstrating over 40 W/mm at 4 GHz [36]. In summary, since the 1st demonstration of RF larges signal power performance in a GaN HEMT in 1996, reducing DC-to-RF dispersion has been instrumental in helping RF GaN HEMTs achieve their potential in RF transistor amplifier applications at frequencies of approximately 20 GHz or less.

Chapter 1.4 – Development of III-N HEMTs for W-Band Application:

Transistors for RF amplification purposes should be capable of producing high large signal gain, high efficiencies, and high output RF powers at the frequency range of interest. Achieving all three simultaneously at W-Band (75-110 GHz) has been a struggle in the III-N material system (Fig. 1.7). As a result, relatively low $P_{RF,out}$ has been achieved at W-Band. Further, $P_{RF,out}$ has remained approximately flat for over a decade with conventional $Al_xGa_{1-x}N$/GaN HEMTs (Fig. 1.8) (a recent result using $In_yAl_xGa_{1-x-y}N$/GaN HEMTs has improved $P_{RF,out}$ though). This is largely due to surface state related DC-to-RF dispersion. As explained in the previous section, historically, application of an *ex situ* dielectric passivation layer in conjunction with field plating has effectively removed this dispersion and enabled high power and efficiency performance in these devices [30-37], [39]. However, thick passivation layers and/or field plating is prohibitive at W-band due to the large parasitic capacitances they introduce. Thus, in order to get the sufficient small-signal RF gain (equations 1.6 and 1.7) at W-Band frequencies, most groups fabricating W-Band III-N

transistors do not use any field plating, and rely only on a relatively thin PECVD SiN passivation layers for controlling dispersion [42] (Fig. 1.9). As a result, they cannot push to higher drain voltages without experiencing large amounts of dispersion, ultimately limiting their large signal power performance at this frequency to roughly 2 W/mm in the AlGaN/GaN based HEMTs (3W/mm was recently demonstrated on an $In_yAl_xGa_{1-x-y}N$/GaN HEMT). Therefore, the reported RF output power densities at this frequency range has been much lower than what III-N HEMTs are theoretically capable of in absence of the DC-to-RF dispersion phenomenon.

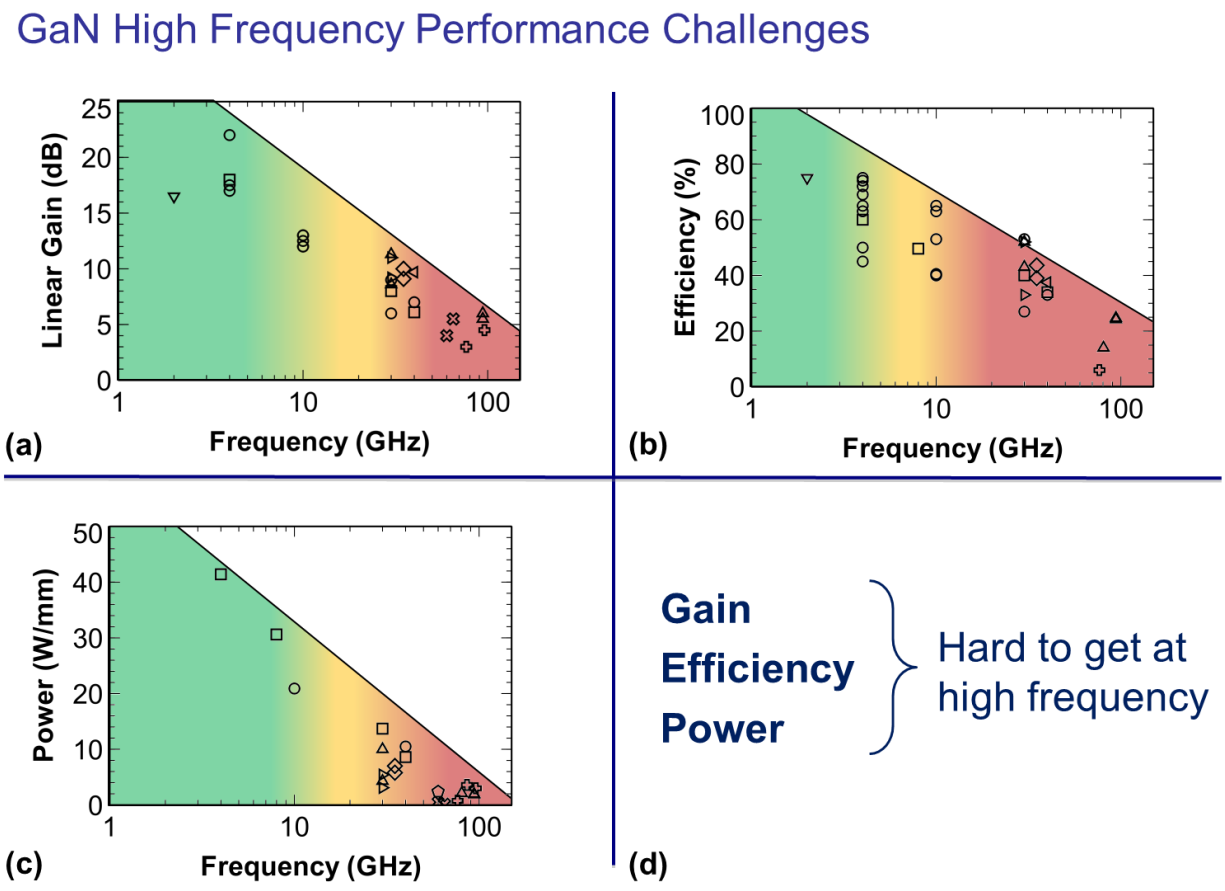

Fig 1.7: Large signal power performance for III-N HEMTs with respect to frequency. (a) Linear Gain (dB), (b) *PAE*, and (c) output RF power density versus frequency. Can clearly see that that the RF large signal power performance degrades with increasing frequency. (d) Summarizes the challenges facing III-N system at higher frequencies [40].

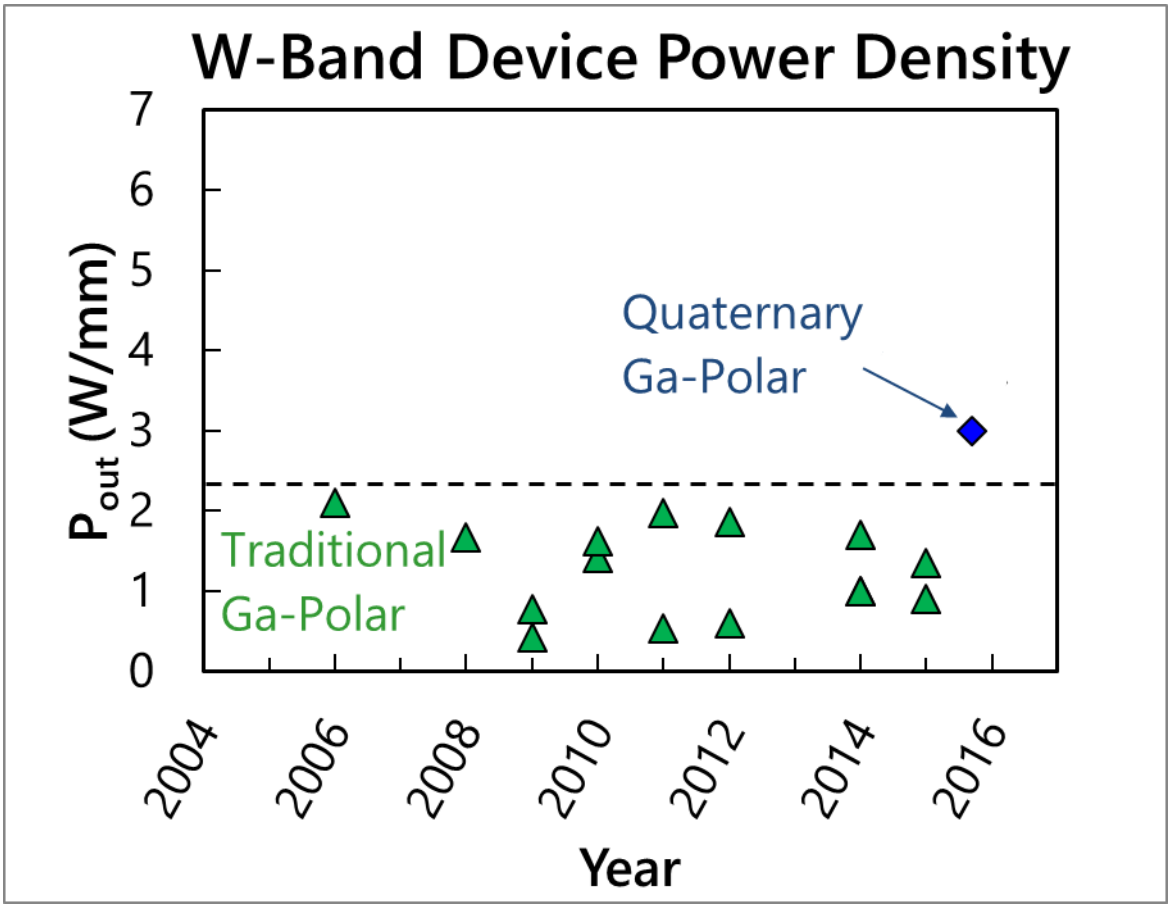

Fig. 1.8: Output RF power density at the W-Band range of frequencies for Ga-Polar III-N HEMTs. Can see that the power density has remained flat in conventional (AlGaN/GaN) Ga-Polar transistors at this frequency range for over a decade. Recently, an InAlGaN top-barrier HEMT has led to a higher output power density at 94 GHz, however [41].

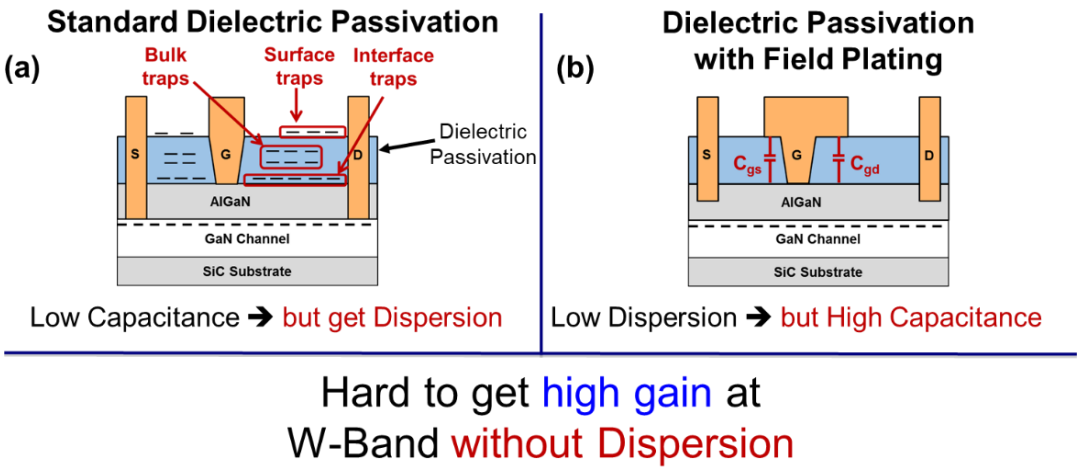

Fig. 1.9: (a) Dielectric passivation only, typical of many Ga-Polar transistor designed for W-Band operation [41]. Lack of field plating means higher E-Fields for a given V_{DS} bias, making electron injection into trap states more likely. (b) Field plated device. Reduced E-Fields resulting in reduced electron trapping, but higher capacitances will limit the gain at W-Band frequencies.

However, the N-Polar GaN metal-insulator HEMTs (MISHEMTs) reported in this work provide much higher power densities at 94 GHz (Fig. 1.10) [43-44]. The 6.7 W/mm power density reported towards the end of this dissertation is over 2x higher than the highest reported $P_{RF,out}$ at this frequency in the Ga-Polar transistors fabricated by virtually everyone else outside UCSB [44]. Details on the differences between Ga-Polar and N-Polar GaN transistors are given in the next section.

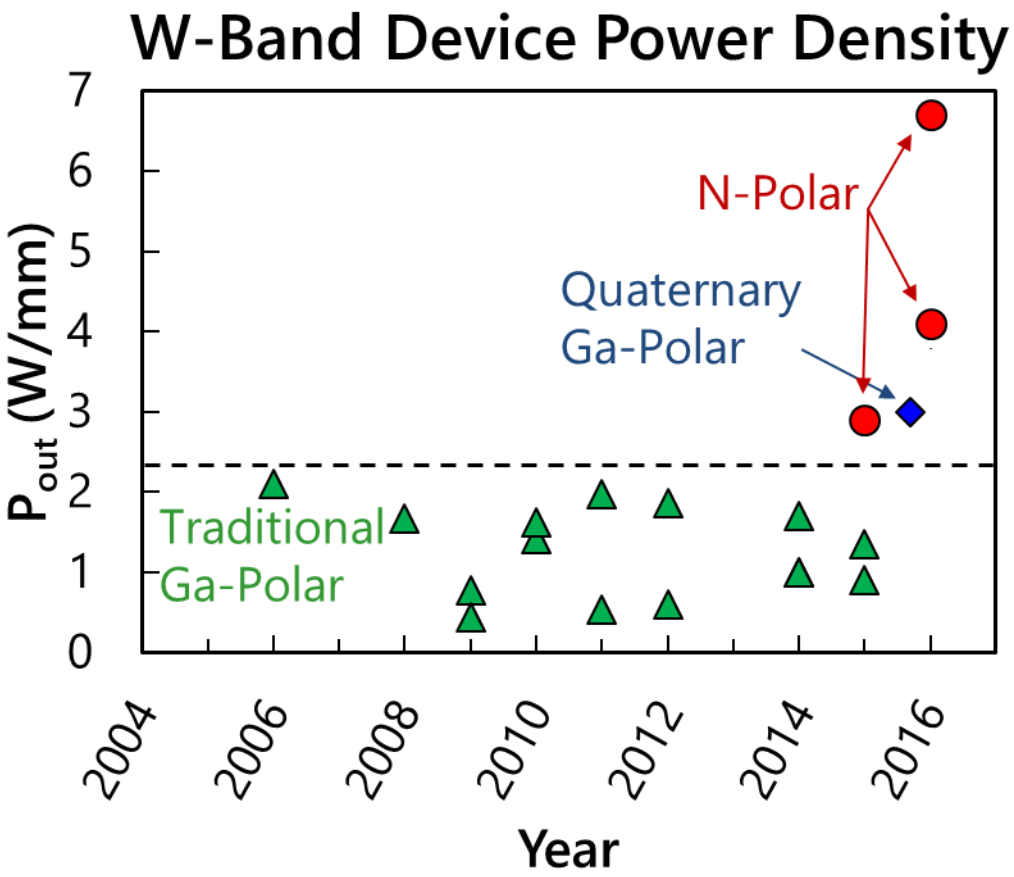

Fig. 1.10: Figure 1.9 with results from this thesis added to the chart. Can see that the N-Polar MISHEMTs developed in this dissertation more than doubled the highest Ga-Polar W-Band transistor power density [43-44] [41].

Chapter 1.5 – Advantages of the N-Polar Orientation in III-N Transistors:

GaN and its alloys are typically grown in the wurtzite crystallographic phase (Fig. 1.11). Wurtzite GaN (as well as InN and AlN) IS a polar material, containing high values of both spontaneous and piezoelectric polarization [46]. At heterojunctions between GaN and one of its alloys with AlN or InN, a polarization discontinuity results, creating a net polarization charge at the heterointerface. The directions of maximum polarity are the (0001) and $(000\bar{1})$, also known as the Ga-Polar and N-Polar faces, respectively. These faces can be interpreted as the top and bottom hexagons of Fig. 1.11. Fig. 1.12 shows the bond directions

for each of these crystallographic faces. Because of the reversed bond directions, the direction of the polarization dipole is also reversed between Ga-Polar and N-Polar. However, the magnitude of the polarization constants is the same.

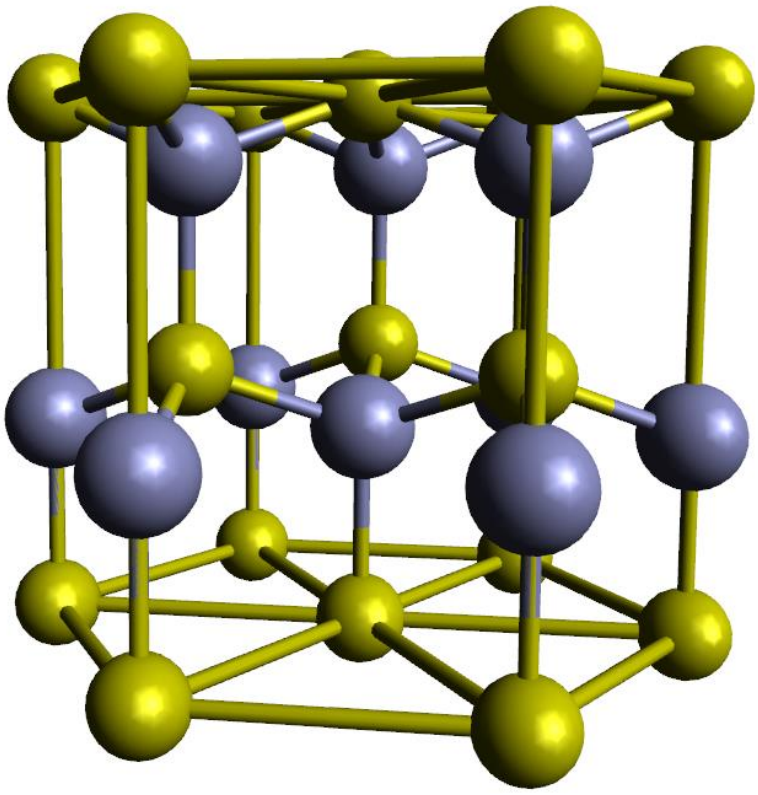

Fig. 1.11: One representation of the unit cell of a wurtzite crystal [45].

The opposite orientation of the polarization fields in Ga and N-Polar HEMTs is the key difference between the two, and leads to several inherent advantages for N-Polar HEMTs relative to their Ga-Polar counterparts.

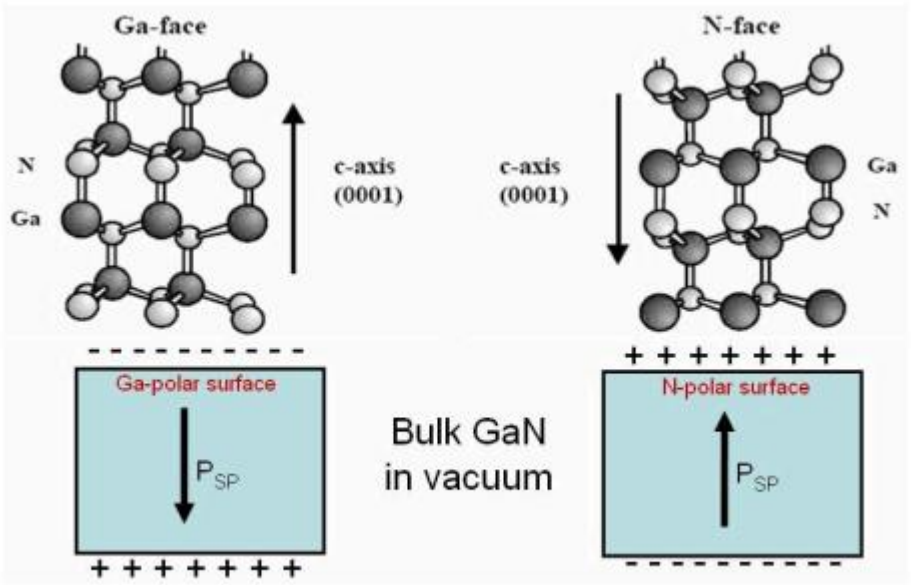

Fig. 1.12: Orientation of the bond structure and polarization dipole in both Ga-Polar and N-Polar GaN [47].

Chapter 1.5.1 – N-Polar's Natural Back-Barrier:

In N-Polar HEMTs, the fields are such that the charge inducing barrier is located at the back of the HEMT, not the top like in Ga-Polar (Fig. 1.13).

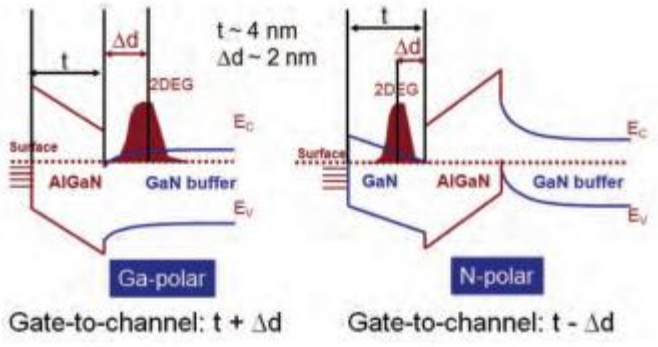

Fig. 1.13: Energy band diagram at equilibrium for simple Ga and N-Polar HEMT epitaxial structures [48].

This creates a natural back-barrier for the channel 2DEG in N-Polar HEMTs, improving the overall gate control of the channel charge and improving the output resistance of the device. Additionally, this back-barrier presents an additional barrier to electron transport from the channel into the bulk substrate, thus reducing the substrate leakage of the device without

the use of intentional deep level acceptor dopants. This property is potentially very useful in GaN high power electronics grown on Si substrates. In such devices, the buffer of the HEMT structure is grown very thick in order to improve the crystal quality of the GaN present in the active area of the device [49]. In order to reduce substrate leakage and increase the resistivity of the buffer the buffer is heavily doped with deep acceptors like C and/or Fe. Trap levels of 0.9 eV and 2.85 eV above the Valence Band have been identified for C and Fe dopants, respectively [50-51]. These acceptor dopants successfully reduce substrate leakage and increase buffer resistance, however their energy levels are so deep in the bandgap they essentially act as traps with very long time constants [52]. Thus, any substrate leakage that does occur can potentially lead to trapping and DC-to-RF dispersion in the device, as discussed previously. Having an additional barrier to electron injection to the substrate which does not have any deep acceptor dopants present can help reduce this problem. An investigation into N-Polar transistors for power electronic device applications is outside the scope of this thesis, but this potential benefit bears mentioning.

A Schrodinger-Poisson solver can be used to show that the presence of the AlGaN barrier which induces the 2DEG in either Ga or N-Polar displaces the centroid of the 2DEG away from that barrier by somewhere between 0.5 to 2 nm. By having the back-barrier induce the 2DEG charge, the centroid of the 2DEG is pushed towards the gate electrode, rather than away like in Ga-Polar (Fig. 1.13). This increases the effective aspect ratio of the N-Polar FET as well as the overall gate control of the channel charge.

It should be noted that it is possible to form a polarization induced barrier in Ga-Polar HEMTs. Although not an inherent/natural part of the Ga-Polar transistor structure, such barriers can also improve the gate control of the channel 2DEG, reduce substrate leakage, and

improve the output resistance of the transistor as well. However, certain problems can potentially arise from the use of such structures which are absent in the N-Polar implementation of a back-barrier.

In Ga-Polar, if one were to grow the entire buffer out of an $Al_xGa_{1-x}N$, grow a relatively thin (10-40 nm) GaN channel, and then grow a higher composition $Al_yGa_{1-y}N$ charge inducing barrier on top, such a back-barrier would be created [53]. In this case, it is not the ΔE_C of the $Al_xGa_{1-x}N$ buffer which creates the barrier to channel electrons, but rather the net negative polarization charge at the backside GaN/$Al_xGa_{1-x}N$ pulls the GaN channel at the back up in energy and this GaN layer acts as the barrier. The problem with this implementation is that the entire buffer must be made of an $Al_xGa_{1-x}N$ alloy, which will have a lower crystallographic quality than a binary GaN buffer would have. Further, the thermal conductivity of an $Al_xGa_{1-x}N$ alloy buffer is much worse than for a GaN buffer and a larger amount of self-heating would occur [54]. It is possible to only grow a layer of $Al_XGa_{1-x}N$ sandwiched between a GaN buffer and GaN channel for the same purpose. However, deep acceptor doping would have to be used at the bottom $Al_xGa_{1-x}N$/GaN interface, otherwise another 2DEG with a poor aspect ratio with respect to the gate electrode would form. Using deep acceptor doping this close to the channel could potentially cause trapping problems, as explained earlier. Additionally, an $In_xGa_{1-x}N$ back-barrier could be used like that in [55]. However, using a lower bandgap material in a region of the device which is exposed to high electric fields could potentially lead to a reduction in breakdown voltage of the device.

Chapter 1.5.2 – Better Ohmic Contacts:

Having the charge inducing layer underneath the channel is beneficial for regrown contacts as well, as the n+ to 2DEG contact can be made through the lower bandgap GaN,

rather than through AlGaN like in many Ga-Polar devices. It is possible to etch away the AlGaN layer in Ga-Polar HEMTs, but this can actually lead to an increase in the contact resistance, as the top AlGaN layer is what induces the 2DEG in Ga-Polar HEMTs in the first place.

Additionally, the orientation of the polarization fields in N-Polar HEMTs enables the engineer to grade the GaN channel to InN in the contact region of the device. Because the bandgap of InN is much smaller and the polarization and quasi-electric fields are such that the CB is flat when grading from GaN to InN in the N-Polar orientation, this regrowth scheme can eliminate barriers to electron transport between the semiconductor and metallic contact (Fig. 1.14 (b)). Dasgupta *et al*. has demonstrated an extremely low contact resistance of ~ 0.025 Ω·mm using such a regrowth design [57]. Such a scheme is not used in this dissertation, but very good contact resistances of around ~ 0.1 Ω·mm are obtained with plasma-assisted-molecular-beam-epitaxial grown n+ GaN contacts (Fig. 1.14 (a)) [58].

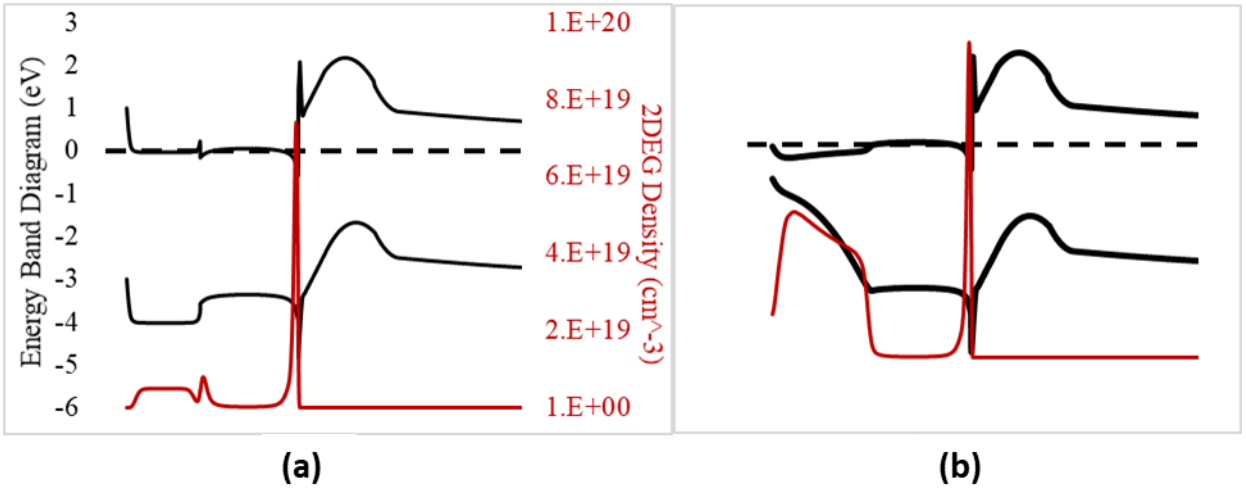

Fig. 1.14: Simulated energy band diagram in the ohmic region of the N-Polar transistor for the case of (a) a regrown n+ GaN cap and (b) a graded GaN to InN which is n+ doped during the entirety of the grade [58]. A graded AlGaN back-barrier was used in this simulation. More details regarding this type of N-Polar back-barrier will be given in Chapter 2.

Chapter 1.5.3 – N-Polar AlGaN Top Barrier:

In N-Polar HEMTs, when an AlGaN layer is placed on top of the GaN channel, the polarization fields oppose the electric fields produced in a reverse biased gate drain junction (Fig. 1.15). This is in contrast to Ga-Polar HEMTs where the polarization fields are in the same direction and an applied gate-drain reverse bias rapidly reduces the tunneling barrier for gate injected electrons. However, it should be noted that the schottky barrier in N-Polar HEMTs appears to be smaller than that in Ga-Polar transistors [59-60]. Thus, in terms of leakage in HEMTs with schottky gates, N-Polar may not actually be superior to Ga-Polar.

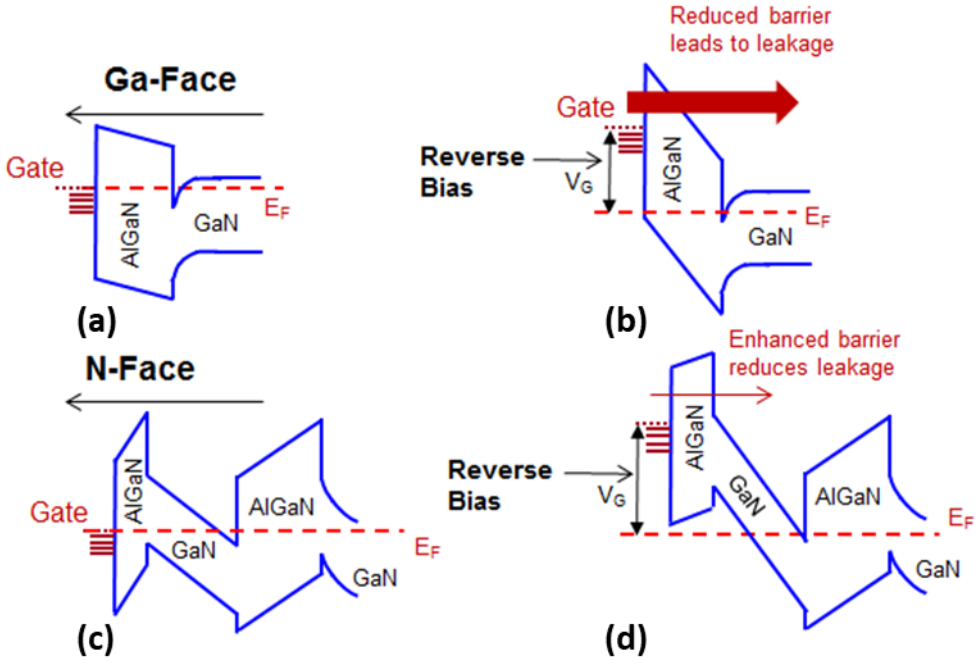

Fig. 1.15: A schematic of a Ga-Polar HEMT band diagram at (a) equilibrium and (b) with a reverse gate-drain voltage applied. (c) and (d) give the energy band diagram of a N-Polar HEMT with a thin AlGaN top-barrier at equilibrium and at a reverse gate-drain voltage bias, respectively [58].

Chapter 1.5.4 – GaN Cap in Access Region of N-Polar Transistor:

Finally, the direction of the polarization fields in N-Polar allows the device designer to add a UID GaN Cap in the access regions of the device for considerable performance

improvements (Fig. 1.16). This GaN Cap serves 2 purposes. First, the GaN Cap greatly enhances access region conductivity and lowers the On-Resistance of the transistor. This is because the fields in N-Polar are such that the UID GaN cap pushes the conduction band (CB) down relative to the Fermi level (E_F), resulting in an enhancement of the 2DEG charge in the access regions [43]. Further, the presence of the GaN cap relaxes the electric field seen by the channel 2DEG, pulling the centroid of the 2DEG away from the back GaN/AlGaN interface, reducing interfacial and alloy scattering [61]. This results in a large increase in 2DEG mobility. Together these benefits lowered the sheet resistance from 410 Ω/square in the recessed channel region to only 230 Ω/square in the GaN capped access regions for one of the devices reported on in later chapters of this dissertation (Fig. 1.17).

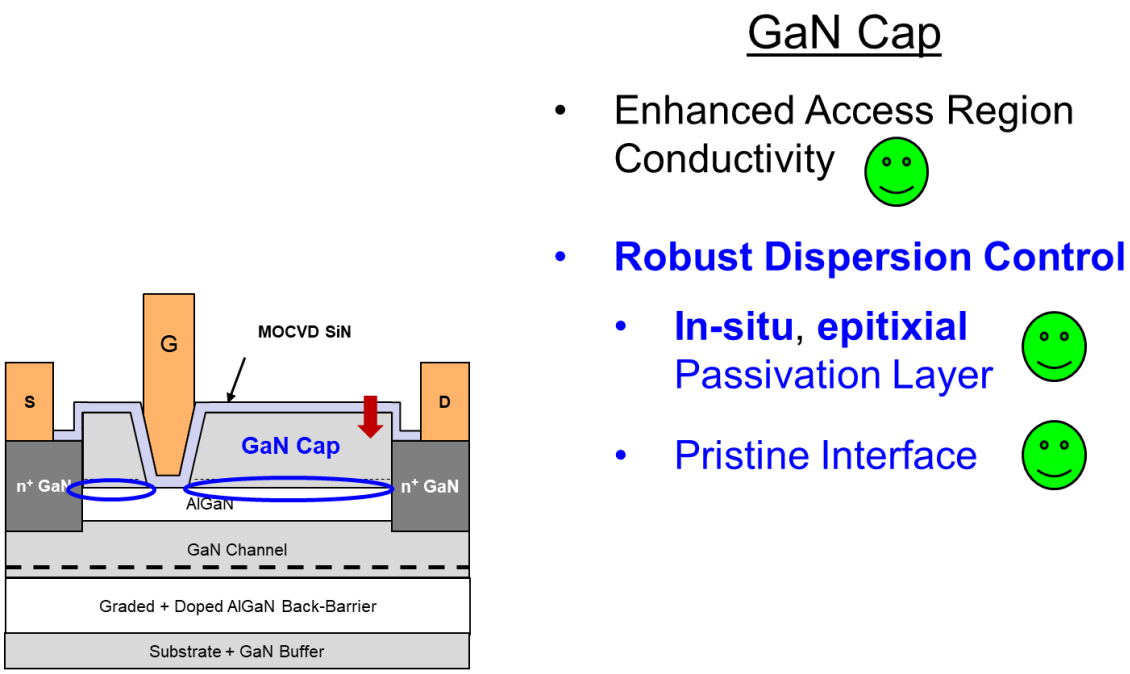

Fig. 1.16: Cross-section of the N-Polar GaN Cap MISHEMT device structure.

Second, and this is really the key to this entire transistor design, it replaces traditional ex-situ SiN passivation with a robust, in-situ epitaxial layer for dispersion control that has a pristine interface with the underlying HEMT structure allowing for consistent and reliable

control of dispersion. This ability to control dispersion at high frequencies, while actually reducing some of the extrinsic resistances which can limit high frequency performance is really the key to our transistor's excellent W-Band power performance

- Channel charge +30%
  - From polarization electric field
- Mobility +25%
  - Reduced interface scattering
- Resistance -44%

GTLM Results

Region	R_{sh}	n_s (e13)	μ
Gate	**410**	1.0	**1630**
Access (GaN Cap)	**230**	1.3	**2075**

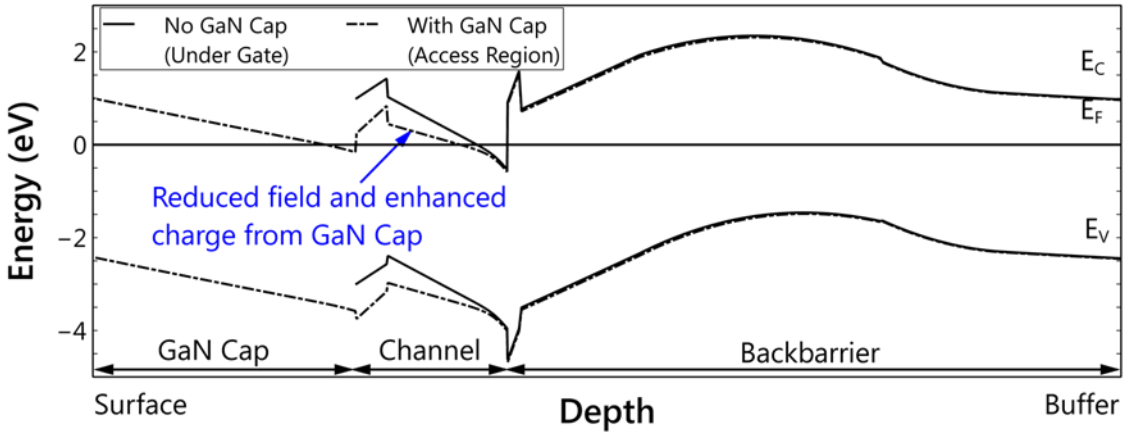

Fig. 1.18: Energy band diagram of a scaled N-Polar transistor both with and without a GaN Cap. Can see that the conduction band is pulled down by the presence of the GaN Cap. Can also see that the magnitude of the total field in proximity of the channel 2DEG has been reduced (total field is the derivative of the conduction band profile) [62-63].

This dissertation focuses on the development of a N-Polar MISHEMT with a UID GaN Cap in the access regions of the device for W-Band power amplification purposes. Such a structure is named a N-Polar Deep Recess MISHEMT after earlier Gallium and initial N-Polar incarnations [64-67]. An overview of each chapter contained in this dissertation is given in the next section of this chapter.

Chapter 1.6 – Synopsis of Thesis:

The goal of this dissertation is to make the best possible N-Polar MISHEMT device for large signal power performance at the W-Band range (75-110 GHz) portion of the electromagnetic spectrum. This goal has been achieved, as a N-Polar transistor with a peak RF output power density of more than 2x higher than any other device detailed in the literature at the time is reported in this thesis.

Chapter 2 begins with an experiment meant to find the best gate cap stack combination for use in high frequency N-Polar MISHEMT devices. Of the gate cap stack variations investigated, a clear winner is found that enables a significantly higher breakdown voltage than all other designs. A physics based explanation for why this gate cap stack performs the best is given. The next portion of the chapter goes over the relationship between channel 2DEG charge density and the overall device performance of the N-Polar MISHEMT, with a special focus on gate leakage and breakdown performance. Finally, an investigation into the ohmic contact design in N-Polar transistors is conducted.

Chapter 3 gives a thorough overview of DC-to-RF dispersion and introduces the concept of the N-Polar Deep Recess design for controlling dispersion. A fabrication procedure for the N-Polar Deep Recess MISHEMT is developed and explained in detail. Initial investigations into the ability of the GaN Cap to reduce both the access region resistance and DC-to-RF dispersion are conducted. Finally, a study to determine the maximum allowable gap between the gate metal and GaN Cap sidewall while still maintaining low dispersion in relatively unstressful large signal measurements is performed.

Chapter 4 reports on the initial T-Gate results for NPDR MISHEMTs fabricated on sapphire substrates. The ability of the GaN Cap in the source-gate access region to ameliorate

the source choke problem detailed by Palacios *et al*. [68] is detailed. Excellent large signal power performance of 4.5 W/mm with an associated *PAE* of 67% is demonstrated. An RF-IV measurement at 6 GHz shows the RF current density of the NPDR MISHEMT to be in excess of 2 A/mm at a V_{GS} = +2 V, confirming the excellent control of dispersion afforded by the GaN Cap design. Finally, a (then) record $P_{RF,out}$ of 2.9 W/mm at 94 GHz is achieved on an NPDR MISHEMT with a sapphire substrate.

The lateral device dimensions of the NPDR MISHEMT are optimized in Chapter 5. Specifically, investigations into the optimal source-drain spacing, gate metal overlap of the source-side GaN Cap, and the gate metal overlap of the drain-side GaN Cap are explored.

The optimized lateral device dimensions from Chapter 5 were then used to fabricate a N-Polar GaN Cap (NPDR) MISHEMT with record power performance at 94 GHz on a SiC substrate.

Finally, Chapter 7 summarizes the work contained in this thesis and presents ideas for future work/development of the NPDR MISHEMT design.

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Chapter 2

Planar N-Polar MISHEMT Optimization

As mentioned earlier, transistors for RF amplification purposes should have high *DE*, *PAE*, and produce high output RF power at the frequency of interest. Many components from both the intrinsic and extrinsic sections of the HEMT contribute to these metrics. In this section of the thesis, several experiments are carried out to optimize the planar portion of the NPDR device structure. These experiments were performed on planar N-Polar MIS-HEMTs with the aim of improving one or more of the performance metrics mentioned above. Knowledge gained from these experiments were then incorporated into the planar section of the NPDR HEMT at a later date.

Chapter 2.1 – MOCVD Growth and Basic Device Structure:

Samples were grown via MOCVD on c-plane sapphire substrates with a 4^{o} miscut towards the a-plane. Trimethylgallium (TMGa), trimethylaluminum (TMAl), ammonia (NH_3), disilane (Si_2H_6), and Ferrocene (Cp_2Fe) were used as precursors [1]. The N-Polar HEMT epitaxial structure used by Seshari Kolluri [2] served as a starting point for the device design of the HEMTs in this chapter and in subsequent chapters of this thesis. For devices in this chapter specifically, the basic epitaxial structure consisted of some gate cap stack comprised of a dielectric layer and possibly a wide band gap semiconductor layer, a 20 nm unintentionally doped (UID) GaN channel, a 0.7 nm AlN interlayer, a 10 nm UID $Al_{0.38}Ga_{0.62}N$ spacer layer, a 20 nm Si-doped graded AlGaN back-barrier, a 10 nm Si-doped

GaN layer, and a GaN buffer with a 150 nm UID GaN spacer layer followed by 1.35 µm of Fe-doped GaN. Either alloyed or n+ GaN layers were used to contact the channel 2DEG in the source/drain regions. A representative "generic" band diagram for this basic device design in the gated region is given in Fig. 2.1. Optimization experiments were run with regards to the gate cap stack, AlGaN back-barrier, and contact regions in this chapter of the thesis.

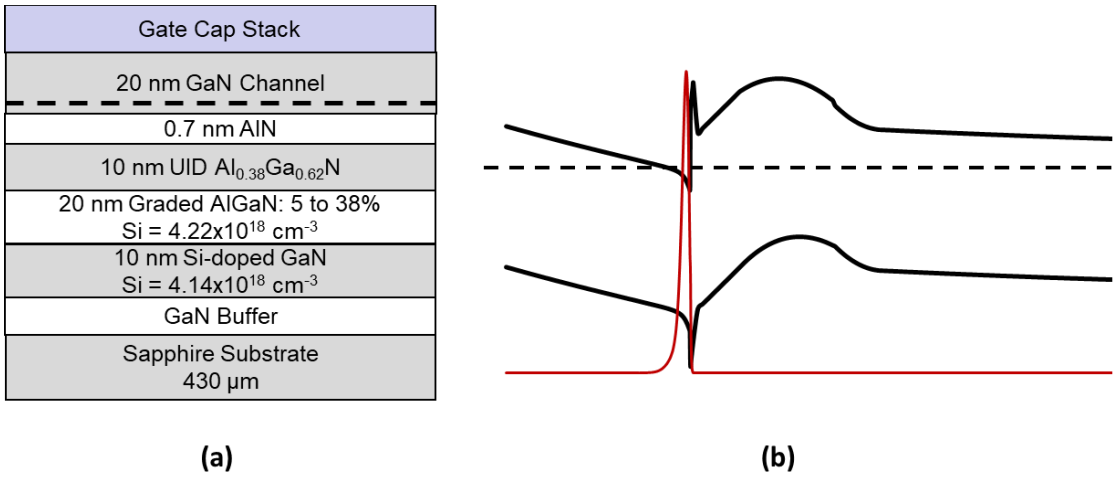


Fig. 2.1: Basic N-Polar HEMT structure for the N-Polar transistors discussed in this chapter of the thesis. The cross-section of the epitaxial structure is shown in (a). The energy band diagram is shown in (b). It should be noted that the gate cap stack was not included in the simulation of the band diagram [11].

Chapter 2.2 – Gate Cap Stack Experiments:

This section is devoted to experiments meant to map out the design space of the Gate Cap in our N-Polar transistor. The section begins by summarizing the historical work done in this area by prior Mishra students in N-Polar transistors. The next subsection(s) cover the experimental details, fabrication procedure, and basic static and small signal RF results. However, the main focus of the gate cap experiments is on their effect on leakage and breakdown performance. As such, a brief description of some of the various known breakdown mechanisms and measurement techniques for GaN based transistors is given. The

final subsections cover the leakage and breakdown performance of the devices and presents data on another transistor with the "best" gate cap stack.

Chapter 2.2.1 Introduction:

The early Schottky-gate N-Polar HEMTs fabricated by Siddarth Rajan [3] suffered from very high gate leakage, with two-terminal gate-leakage exceeding 4 mA/mm at voltages below 20 V. This is significantly worse than what is seen in Ga-Polar HEMTs with Schottky gates. A cross-section of Rajan's 2nd generation N-Polar GaN HEMT device structure is shown in Fig. 2.2 (a). The corresponding band diagram is given in Fig. 2.2 (b). Rajan gave several potential reasons for the high gate leakage/low breakdown voltage of this N-Polar device relative to a conventional Schottky-gate Ga-Polar HEMT. First, in conventional Ga-Polar HEMTs, the Schottky gate is typically placed on the wider bandgap charge inducing $Al_xGa_{1-x}N$ layer located at the surface of the as-grown epitaxial stack. In Rajan's device, the Schottky gate was placed directly on top of the UID GaN channel. This likely seemed natural, as the charge inducing wide bandgap layer in N-Polar oriented transistors is underneath the UID GaN channel, rather than on top like in Ga-Polar. As a result, the Schottky barrier height was probably lower for these N-Polar devices with respect to their conventional Ga-Polar counterparts [4-5]. Further, the peak E-Field at the drain-edge of the gate is now located in the UID GaN channel, rather than the wider bandgap $Al_xGa_{1-x}N$ layer. As the critical electric field is related to the bandgap of the material, it is reasonable to assume that the breakdown field for GaN is lower than that of $Al_xGa_{1-x}N$ [6]. Finally, Rajan's HEMT were grown via plasma-assisted molecular beam epitaxy (PAMBE), whereas conventional Ga-Polar HEMTs are traditionally grown via MOCVD. Although not explicitly stated, III-N epitaxial films

grown with PAMBE tend to be leakier and have lower breakdown voltages than devices grown with MOCVD [7].

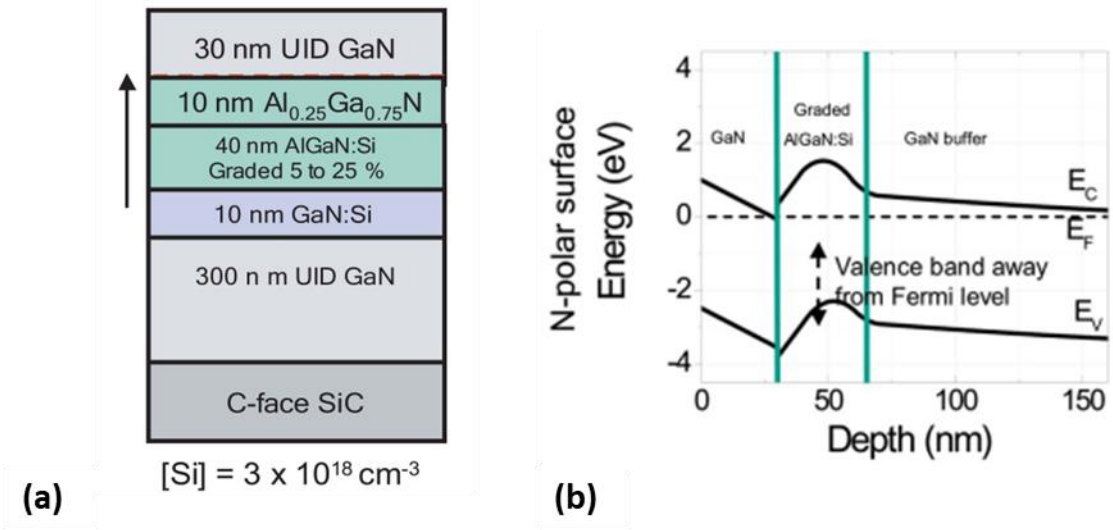


Fig. 2.2: 2nd generation N-Polar HEMT structure from [3]. The epitaxial structure and energy band diagram at equilibrium are given in (a) and (b), respectively.

To help mitigate these issues, Rajan thinned his GaN channel and grew a 25 nm $Al_{0.1}Ga_{0.90}N$ top-barrier on which he formed the device's Schottky gate contact (Fig. 2.3). This dramatically reduced the gate leakage in his devices and boosted the breakdown voltage over 3x. Man Hoi Wong later added a MOCVD SiN_X gate dielectric in combination with a thinner $Al_{0.10}Ga_{0.90}N$ top-barrier for further gate leakage reduction [8]. Subsequent N-Polar Mishra students [9-10] and [2] used some variation of this basic gate cap stack in combination with MOCVD grown N-Polar material.

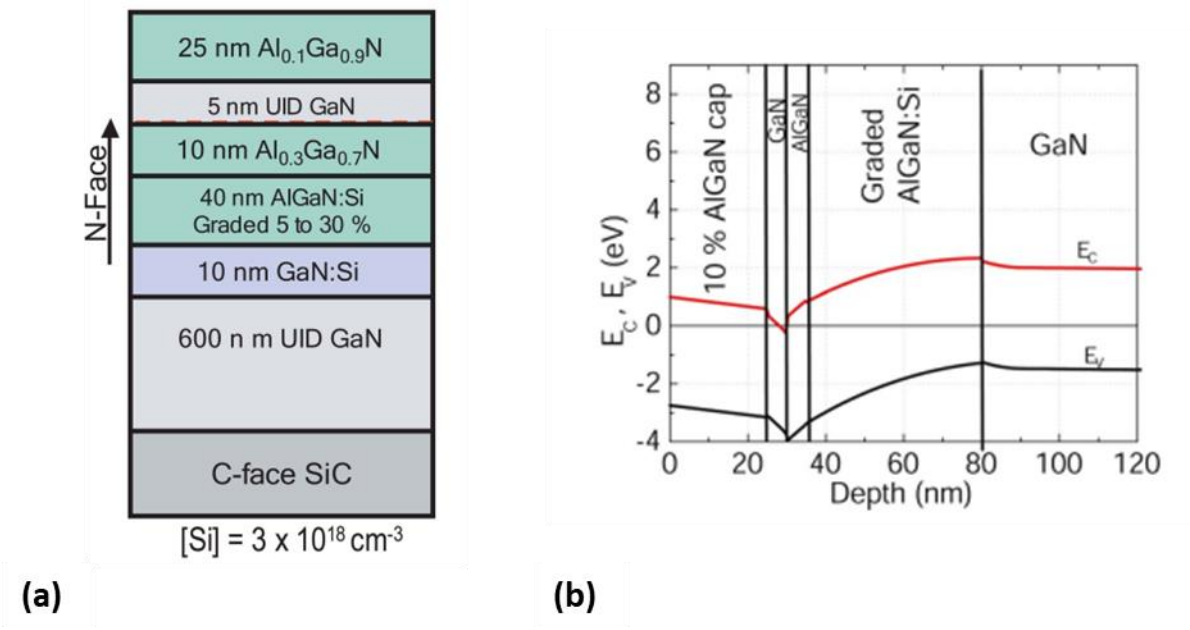


Fig. 1.3: 3rd generation N-Polar HEMT structure from [3] with an AlGaN top-barrier layer. The epitaxial structure and energy band diagram at equilibrium are given in (a) and (b), respectively.

Chapter 2.2.2 Experimental Details + Fabrication Procedure:

In this work, a more systematic study was performed to investigate the characteristics of the gate cap stack and how it affected overall device performance. In particular, the gate cap stack's impact on gate leakage and breakdown voltage were examined closely.

One N-Polar GaN HEMT sample was grown via MOCVD on a full 2" 4° miscut sapphire substrate. The epitaxial cross-section of the device is shown in Fig. 2.1 (a). The structure has Si-doping of $4.14 \cdot 10^{18}$ cm^{-3} in the doped GaN and $4.22 \cdot 10^{18}$ cm^{-3} Si-doping in the graded + doped AlGaN section of the HEMT. The **initial** gate cap consisted only of a 5 nm MOCVD SiN_x. However, this was merely to protect the N-Polar HEMT's surface during the fabrication process, as the N-Polar face is chemically reactive and gets roughened in the strong bases commonly used in photo-resist developers [12]. Later in the fabrication procedure, the SiN_x dielectric was wet etched off, the sample was cleaved into quarters, and

different Gate Cap stacks were regrown on top of the UID GaN channel for each quarter. The first 3 regrowths (samples A-C) were performed in the same Thomas Swan MOCVD reactor in which the original HEMT sample was grown. Sample D's regrowth, however, was performed in a custom in-house built MOCVD reactor.

On the 1st quarter (Sample A) a 9 nm MOCVD SiN_x dielectric was regrown. Sample B also had a 9 nm MOCVD SiN_x dielectric, but in this case the sample was annealed in an NH_3 ambient at 880C for 1 hour prior to regrowth. The thinking was that this anneal might help remove any remaining surface defects prior to the gate-dielectric deposition. On the 3rd quarter, 2.6 nm of $Al_{0.46}Ga_{0.64}N$ followed by 5 nm of MOCVD SiN_x was regrown (Sample C). It is important to note that this regrown $Al_{0.46}Ga_{0.64}N$ is crystallographic, whereas all the other regrown gate cap stacks consist of only amorphous dielectrics. Finally, a 20 nm MOCVD Al_2O_3 dielectric was regrown on the 4th quarter of the sample (Sample D). The samples and their designation (A, B, C, and D) are shown in Table 2.1. Fabrication details for these samples are given in the following paragraphs.

Gate Cap Stack	Sample Designation
9 nm of MOCVD SiN (No Anneal)	A
9 nm of MOCVD SiN (with Anneal)	B
2.6 nm of $Al_{0.46}Ga_{0.54}N$ + 5 nm of MOCVD SiN	C
20 nm of MOCVD Al_2O_3	D

Table 2.1: All 4 samples and their different gate cap stacks used in this section.

The fabrication process is essentially a combination of the fabrication procedures detailed in [2] and [10]. Only gate 1st MIS-HEMT devices (Fig. 2.5 (a)) will be discussed in

this section. Due to the anisotropic transport properties of N-Polar HEMTs grown on vicinal (miscut) substrates, all devices are designed such that source-drain conduction occurs in the high mobility direction parallel to the direction of substrate miscut [1]. Fabrication begins with the Alignment marks. Alignment marks are patterned via stepper lithography and transferred to the GaN epitaxial layers through reactive ion etching in a Cl_2 based chemistry. A regrowth mask consisting of (from bottom to top) the initial 5 nm MOCVD SiN dielectric, a thin ($\leq$ 15 nm) ALD Al_2O_3 etch-stop layer, a 500 nm PECVD SiO_2 layer, and a 10 nm hardmask of Cr on top is then deposited. Stepper lithography is used to pattern this regrowth mask and an inductively coupled-plasma (ICP) dry etch is used to transfer the pattern to the Cr hard mask and then the SiO_2 layers in a Cl_2 and CF_4/O_2 gas chemistry, respectively. The Cr hardmask is then removed in a blanket Cl_2 based dry etch. After the dry etches, the remaining Al_2O_3 etch-stop layer is selectively wet etched off in a timed Tetramethylammonium Hydroxide (TMAH) based photoresist developer wet etch (developer does not etch MOCVD SiN). The MOCVD SiN_x covering the GaN channel surface is then etched off with a low power CF_4/O_2 ICP dry etch. A short low powered BCl_3/Cl_2 based RIE etch is then used to remove any fluorine-based damage to the topmost nanometers of the exposed UID GaN channel. The samples are then put into a plasma assisted molecular beam epitaxy (PAMBE) system and 20 nm of UID GaN followed by 30 nm of highly Si-doped n+ GaN is regrown in the chamber. After this, the regrowth mask is removed in an ultrasonicated bath of HF/HNO_3. 20 nm of E-Beam SiO_2 is then deposited to protect the N-Polar epitaxial surface for the same reasons as mentioned earlier. Mesa isolation is subsequently performed through a combination of stepper lithography and reactive ion etching in Cl_2. The E-Beam SiO_2 is then removed in HF.

At this point the samples were cleaved into quarters. Each quarter underwent a regrowth cleaning procedure to remove residual Si contamination at the epi surface [13]. This was accomplished through an oxidation + wet etch procedure where the samples were exposed to 45' of UV ozone followed by an HF acid dip (two cycles of this), and then put into vacuum sealed bags prior to MOCVD regrowth. After this, one of the four previously mentioned Gate Cap stacks was regrown on each sample via MOCVD. This was followed by non-alloyed ohmic contact formation. Stepper lithography was used to define the ohmic regions. Windows in the gate dielectric were opened with a CF_4/O_2 ICP dry etch. Samples A – C used a low RF plasma power to minimize damage to the underlying n+ GaN. However, the Al_2O_3 dielectric required a higher RF power for its removal. A short low powered BCl_3/Cl_2 based RIE etch was then used to remove any fluorine-based damage to the topmost nanometers of the exposed n+ GaN. An additional 30" dip in dilute HCl removed a few more nanometers of n+ GaN and roughened the surface prior to metal deposition. The samples were then immediately placed in the E-Beam chamber where 20/250/25 nm of Ti/Au/Ni was deposited to form the ohmic contacts. Probe pads consisting of 20/500/30 nm of Ti/Au/Ni followed. Next, gates were defined and deposited via stepper lithography and E-Beam evaporation, respectively. The MIS-HEMT surface was then passivated with 3 nm of ALD Al_2O_3 followed by 120 nm of PECVD Si_xN_{1-x} (the ALD Al_2O_3 was only used for as an etch stop layer for trench gate devices not discussed here). Windows to the probe pad metals were formed in the passivation layer through a high power CF_4/O_2 RIE etch.

Chapter 2.2.3 DC and Small-Signal RF Results:

Table 2.2 contains DC results from a representative gate 1st device from each of the 4 samples. Fig. 2.7 (a) and (b) contain the I_{DS} vs. V_{DS} and transfer curve plots for each of the

samples, respectively. Device dimensions were L_G = 800 nm, L_{SD} = 3.2 μm, L_{GD} = 1.7 μm, and W_G = 2 x 75 μm. Samples A, B, and C all had similar performance, with A and B being nearly identical. All 3 samples had a drain-source current density ≈ 0.85 A/mm at a V_{GS} = 0 V. At this gate-source bias, samples A and B each had an Ron ≈ 1.37 Ω·mm. Ron of sample C was slightly lower at 1.22 Ω·mm, due to the lower Rsh in the device access region. The Rsh, Rc, and overall aspect ratio of these 3 samples are very similar, and it should not be surprising that the device performance is similar between them (Rsh, Rc, and aspect ratio are slightly better for Sample C, but apparently this difference was not larger than the variation across the epitaxial wafer). Sample D however was different. The lower charge, higher Rsh, higher Rc, and worse aspect ratio from the thicker gate dielectric all contributed to make current density and Ron at V_{GS} = 0 V significantly lower than the other samples. The "superior" forward bias characteristics [14], as well as the larger thickness of the Al_2O_3 layer did allow for a significantly larger positive gate bias to be applied to sample D (Fig. 2.8). Although the current density increased and Ron dropped, their values were still worse than the other samples, indicating that perhaps the GaN/Al_2O_3 interface introduces additional scattering mechanisms that do not exist in the other 3 samples. Ionized impurity scattering from the negative charges at the interface being the 1st mechanism that comes to mind.

Sample	I_{DS} (A/mm) (V_{GS} = 0 V)	R_{ON} (Ω·mm) (V_{GS} = 0 V)	Peak gm_{ext} (mS/mm)	Vth (V)	Pk I_G (nA/mm) (2 V below Vth)
MOCVD SiN (no anneal)	0.83	1.39	248	-3.86	3.86
Anneal + 9 nm MOCVD SiN	0.87	1.35	237	-3.82	12.8
AlGaN + 5 nm MOCVD SiN	0.88	1.22	277	-3.41	516
Al_2O_3 20 nm	0.52	2.48	128	-6.13	4.1

Table 2.2: DC performance of the 4 samples used in this experiment

Pulsed IV results on devices nominally equivalent to those given in Table 2 are shown in Fig. 2.9. Minimal dispersion is seen in samples B and C. Drain-side dispersion (knee walkout) occurs in both A and D, however. Sample A being dispersive is a bit of a mystery. Both the device structure and the fabrication/MOCVD SiN regrowth process are similar to other N-Polar HEMTs fabricated in the past which did not have any dispersion. The main difference is the UV ozone/HF acid treatment the sample was exposed too. Typically, the sample does not have an oxidation treatment prior to HF exposure, and it is possible that this procedure damaged the surface of the N-Polar GaN prior to dielectric regrowth. It is also conceivable that this oxidation/wet etch pre-treatment is responsible for the dispersion seen in sample D. However, the MOCVD regrowth of Al2O3 on N-Polar GaN is not as mature as SiN on N-Polar GaN, and increased interfacial trapping in sample D may simply be due to this lack of maturity (improving the quality of the MOCVD Al2O3 regrowth is outside the scope of this work and no further attempts were made here). The NH_3 anneal of sample B and the specific gas flows involved for the regrowth of the $Al_{0.46}Ga_{0.54}N$ layer in sample C may have recovered the surface of the GaN and prevented dispersion in the devices with little dispersion.

Bias-dependent S-parameter measurements up to 67 GHz were made with a Keysight N5227A PNA calibrated by the LRRM method at the probe tips using an impedance standard substrate [16]. Pad de-embedded current and power gain cutoff frequency values (f_T, f_{max}) for all 4 samples are shown in Table 3. An analytical equation for both these figures of merit (FOM) are shown in equations 2.1 and 2.2 respectively.

$$f_T = \frac{gm_{ext}}{2\pi * \left(\left(C_{gs} + C_{gd} \right) * \left(1 + \frac{R_s + R_d}{R_{ds}} + C_{gd} * g_m * (R_s + R_d) \right) \right)} \tag{2.1}$$

$$f_{max} = \frac{\frac{gm_{ext}}{2\pi * \left(C_{gs} + C_{gd} \right)}}{\sqrt{\frac{4}{R_{ds}} * \left(R_g + R_s + R_i \right) + 4\pi * f_T * C_{gd} * \left(2 * R_g + R_s + R_i \right)}} \tag{2.2}$$

The similarity in device geometry, Rsh, and Rc made the f_T and f_{max} values for samples A, B, and C nearly identical at ≈ 18 GHz and 60 GHz respectively. The small signal RF performance for the device on sample D was considerably worse. This is partially due to the fact that the source-drain spacing is 1 μm larger for the device on sample D relative to the devices on the other samples. However, the primary reason for the poorer small signal performance is due to the worse aspect

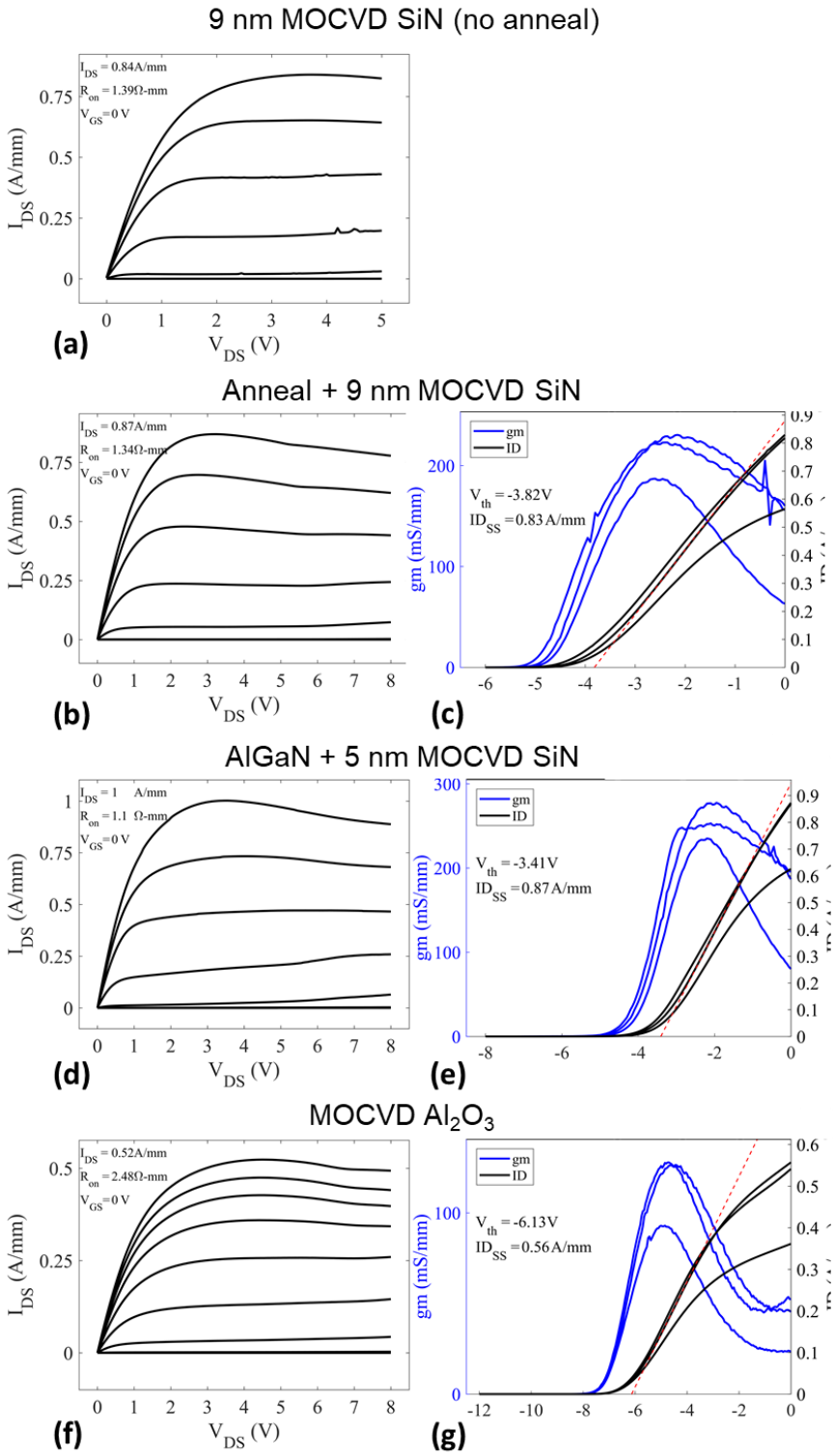


Fig. 2.7: I_{DS} vs. V_{DS} and transfer curves for each of the 4 samples discussed in this section. (a), (c), (e), and (f) are the I_{DS} vs. V_{DS} curves for each of the 4 samples discussed in this section. (b), (d), and (g) are the transfer curves for 3 of the 4 samples discussed in this section. The measurement for the MOCVD SiN gate dielectric sample (no anneal) was noisy, and was not included here. Its characteristics are detailed in Table 2.1.

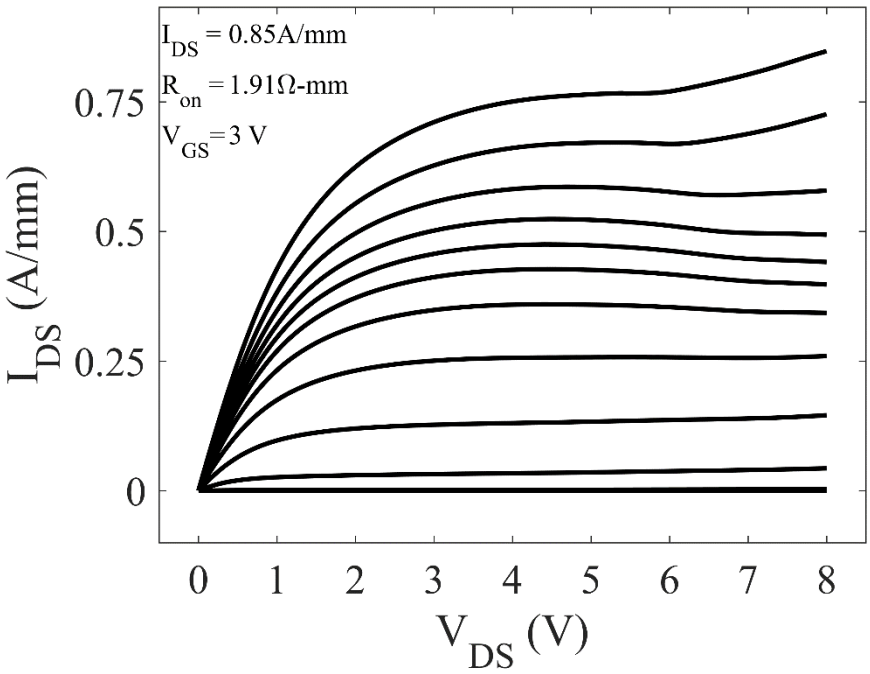


Fig. 2.8: I_{DS} vs. V_{DS} curve for the Al_2O_3 gate dielectric sample all the way up to a V_{GS} = +3 V. The kinks at higher V_{GS} are likely due to holes generated from impact ionization [15].

ratio (nominal Al2O3 thickness is over 2x thicker than other regrown caps) degrading the transconductance (gm) of the device, as well as the higher Rsh increasing the parasitic resistances (Rs) of the device. Together these effects dropped the f_T and f_{max} to 9.6 GHz and 31.25 GHz respectively in this device.

Chapter 2.2.4 – The Drain Current Injection Technique:

The main focus of this experiment is the gate cap stack's effect on off-state breakdown and leakage performance. Off-state breakdown was measured on these samples using del Alamo's *et al.* [17] Drain Current Injection (DCI) technique with a Keysight B1500A Semiconductor Device Parameter Analyzer. In the DCI method, a fixed predefined current is injected into the drain while the gate-source voltage is ramped down from on-state to below threshold (Fig. 2.9), during which V_{DS}, V_{DG}, and I_G are recorded on the parameter analyzer.

This technique traces the locus of V_{DS}, V_{DG}, and I_G versus V_{GS} at fixed I_D on the output I-V characteristics. The drain-source voltage at which off-state breakdown occurs ($V_{DS,BR}$) is unambiguously defined as the maximum V_{DS} attained, irrespective of V_{GS} (Fig. 2.10) . The measurement is usually carried out, however, until which $I_D = -I_G$ (all of the drain current is supplied by the gate). In some cases "channel" breakdown occurs prior to gate-drain breakdown and a change in the slope of V_{DS} vs. V_{GS} occurs before V_{DS} reaches its maximum value (Fig. 2.10 (b)). In extreme cases the channel breakdown is such that a short occurs between the source and drain. When this happens, gate cap breakdown will not occur until the V_{GS} is swept negative enough for the gate stack to breakdown between gate and source (assuming Lgd > Lgs). The concept of a "channel" breakdown will be further expounded upon later in this section of the thesis.

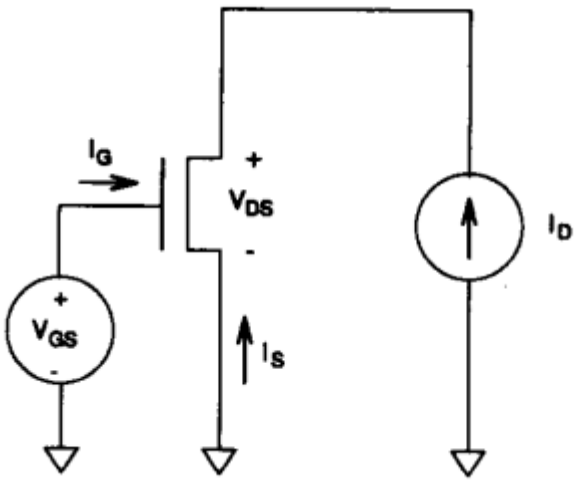


Fig. 2.9: Circuit schematic diagram depicting the biasing configuration for the DCI technique.

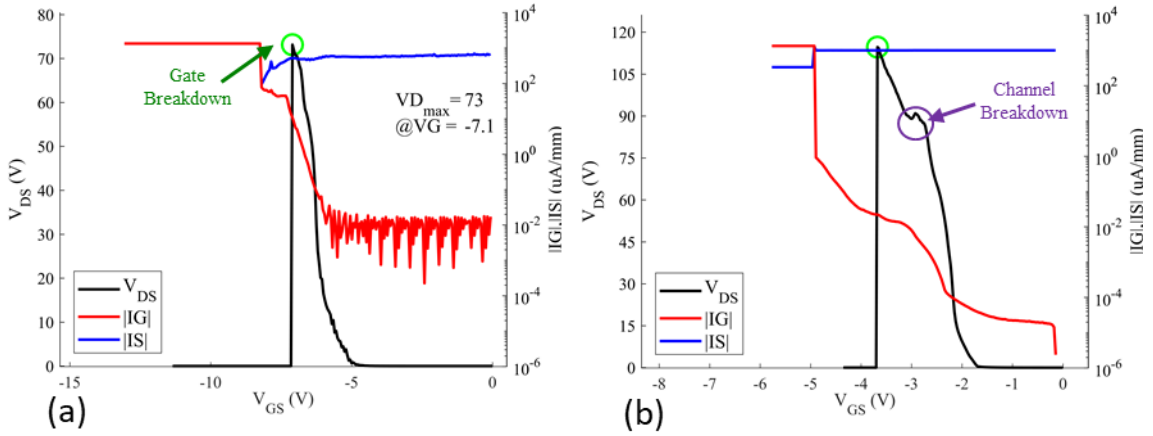


Fig. 2.10: An illustration of the DCI technique taken on N-Polar devices from this section. (a) shows an example where only "gate" breakdown occurs in the transistor. (b) Displays a particular instance where a "channel" breakdown occurs prior to gate breakdown.

Chapter 2.2.5 – Breakdown and Leakage and Performance:

A plot of $V_{DS,BR}$ vs. L_{GD} taken from a representative series of devices for each of the 4 samples is shown in Fig. 2.11. An Id criteria of 1 mA/mm was used for each of the DCI scans in this figure. All transistor devices had a nominal L_G = L_{GS} = 0.7 µm. The B1500A Semiconductor Parameter Analyzer is limited to 200 V outputs, so longer L_{GD}'s ($\geq$ 2.7 µm) could not be measured on some of the samples with higher breakdown voltages. The most significant takeaway from this plot is that sample D (2.7 nm $Al_{0.46}Ga_{0.54}N$ + 5 nm MOCVD SiN) has a significantly higher $V_{DS,BR}$ than all other samples. The two MOCVD SiN samples (A and B) have the second highest breakdown voltages, and the Al2O3 sample (C) has the lowest $V_{DS,BR}$ across all measured L_{GD}. This result is surprising for multiple reasons. First, the sample with the highest breakdown voltage (sample D) also has the highest 2DEG density of all samples at $1.19 \cdot 10^{13}$ cm^{-2}. The sample with the lowest $V_{DS,BR}$ (sample C) has the lowest

charge density at $0.536 \cdot 10^{13}$ cm^{-2}. From Poisson's equation (2.3) a higher charge density means higher channel E-Fields for a given set of V_{DS}, V_{GD}, and V_{GS} bias conditions.

$$\nabla \cdot \bar{E} = \frac{\rho}{\varepsilon} \tag{2.3}$$

$\bar{E}$ is electric field vector, ρ = free charge, and ε = permittivity of the semiconductor channel. Therefore, in the absence of electron trapping, sample D should actually have the highest channel E-Fields and sample C should have the lowest E-Fields of all samples measured for a given set of voltage biases. Still, as evidenced by the dispersion present in some PIV plots of Fig. 2.9, it is apparent that electron trapping does exist in at least some of our devices. Electrons which are dynamically trapped during the DCI scan could act to ameliorate the E-Fields of the device and alter the E-Field profile such that the highest electric fields may not occur in the sample with the highest 2DEG density as anticipated. However, virtually no dispersion is seen in the PIV scan of sample D, while a noticeable amount of knee walkout is seen in sample C. This result suggests a greater amount of electron trapping in sample C, and therefore, a larger degree of E-Field relaxation in sample C relative to D. Thus, for a given V_{DS}, V_{GD}, and V_{GS}, the channel E-Fields (both lateral and vertical) present in sample D should be higher than those present in sample C.

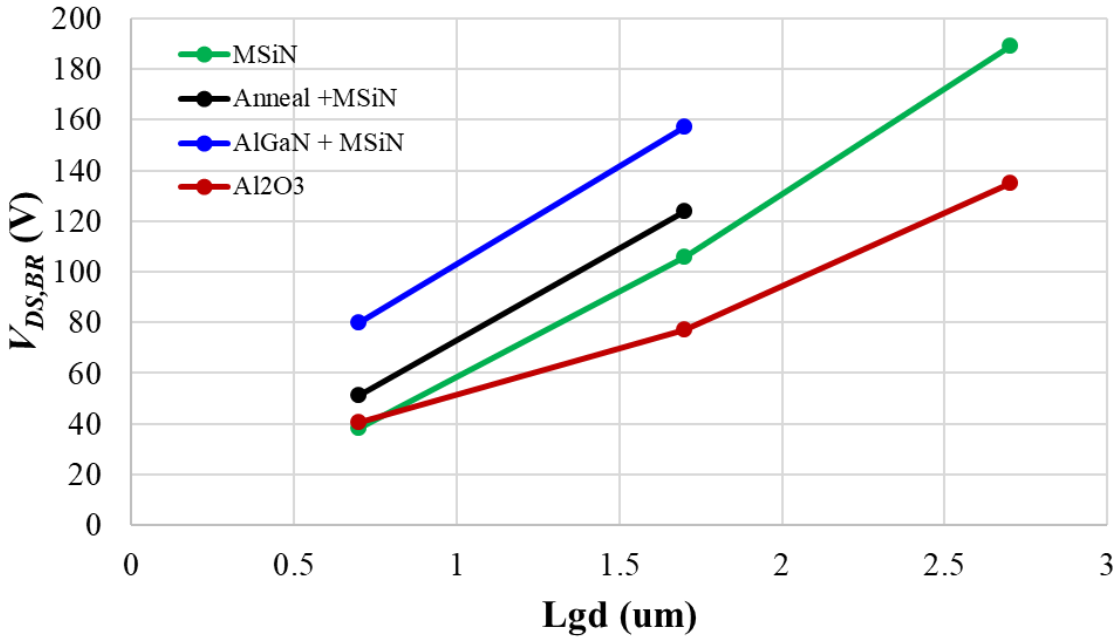


Fig. 2.11: $V_{DS,BR}$ vs. L_{GD} extracted from the DCI technique at a 1 mA/mm injection current density for all 4 samples discussed in this section of the thesis.

Moreover, the breakdown results of Fig. 2.11 are also surprising because sample D has significantly higher gate leakage than all other samples measured. Fig. 2.12 compares the 3-terminal gate leakage between the 4 samples with each device biased approximately 1 V below its respective threshold voltages. At these low voltages I_G for the dielectric only samples are roughly at the noise floor of the GSG probe station used to take these measurements. The gate leakage for sample D is roughly 2 orders of magnitude greater than this. This high gate leakage makes sense for several reasons. First, sample D has the thinnest gate cap stack of all 4 samples (7.6 nm in Sample D versus 9 nm or 20 nm in the other samples). Further, the regrown $Al_{0.46}Ga_{0.54}N$ portion of the gate stack has a smaller ΔE_c than either MOCVD SiN or Al2O3 (Table 2.2). Finally, as mentioned earlier, regrowth of a semiconductor (AlGaN) on top of another semiconductor (GaN) likely resulted in a huge Si doping spike at the regrown GaN/AlGaN interface. As Si is a shallow donor state in the III-N system, this means that the interface is heavily n-type doped. The fact that the 2DEG density

of sample D is over $2 \cdot 10^{12}$ cm^{-2} higher than all other samples (Table 2.1) strongly suggests this is what happened. Even if the Si doping is spread across the entire regrown $Al_{0.46}Ga_{0.54}N$ layer and we assume that all the Si donor dopants image in the channel 2DEG, a 2DEG increase of $2 \cdot 10^{12}$ cm^{-2} implies a Si dopant density of at least $7 \cdot 10^{20}$ cm^{-2}. Such a high Si doping could potentially degrade the quality of the $Al_{0.46}Ga_{0.54}N$ cap, reducing its ability to prevent the flow of gate injected electrons. Further, adding a high positive sheet charge in the $Al_{0.46}Ga_{0.54}N$ induces electric fields in the SiN gate dielectric which assist the tunneling of gate injected electrons through the gate cap stack. The fact that sample D has both the highest gate leakage and the highest breakdown voltage of all samples indicates that the mechanism which initiates the breakdown event does not come from gate injected electrons.

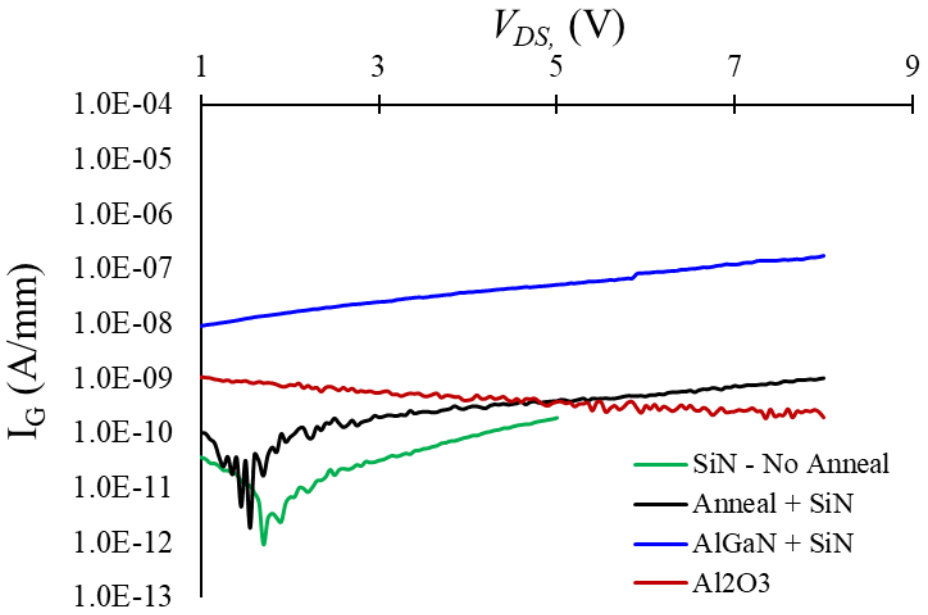


Fig. 2.12: Three-terminal gate leakage of all 4 samples with a V_{GS} bias ≈ 1 V below the threshold voltage of the transistor. The dielectric only samples are near the noise floor, while the AlGaN + SiN sample is roughly 2 orders of magnitude greater at these relatively low drain-source voltages.

ΔE_c with respect to GaN

Material	ΔE_c (eV)
MOCVD SiN	1.9
MOCVD Al_2O_3	2.1
$Al_{0.46}Ga_{0.54}N$	0.7

Table 2.3: Conduction band discontinuity between gate cap stack material and GaN [18-21].

DCI scans for transistors with nominally equivalent *lateral dimensions on samples A, C, and D (SiN only, $Al_{0.46}Ga_{0.54}N$ + SiN, and Al_2O_3, respectively) in Fig. 2.13 corroborate this assertion. The scan on sample C ($Al_{0.54}GaN$ + SiN, Fig. 2.13 (b)) reveals that the gate dielectric breaks down, the gate leakage shoots up, and the device catastrophically fails at a V_{GS} = -7.5 V. After breakdown, the gate dielectric is permanently degraded, and the gate leakage supplies both the 1 mA/mm of current to the drain contact as well as ~30 mA/mm to the source contact (source contact does not have a boundary condition placed on it, and is physically closer to the gate, reason for the higher current). Immediately prior to breakdown I_G = 291 μA/mm on the Sample D device. The scan on sample D (Al_2O_3, Fig. 2.13 (c)) show a different behavior. At a V_{GS} = -6.5 V the device catastrophically fails. After catastrophic breakdown, the bulk of the gate dielectric has not significantly degraded, and the gate leakage does not appreciably increase throughout the rest of the DCI sweep. Immediately prior to breakdown the gate leakage is less than 1 nA/mm, roughly 6 orders of magnitude less than the scan on sample D. The fact that the Al_2O_3 device's gate leakage is so much lower than sample D, yet its $V_{DS,BR}$ is also much lower than that of sample D (43 V vs. 84 V, respectively) further affirms the notion that gate injected electrons are not responsible for the breakdown of the

device. The relatively thick (20 nm) Al_2O_3 gate dielectric not substantially degrading after catastrophic failure is a further testament to this point. The scan on sample A (SiN only, Fig. 2.13 (a)) represents a situation between that of the $Al_{0.46}Ga_{0.54}N$ + SiN and Al_2O_3 samples. This device catastrophically fails at a V_{GS} = -4.8 V. At breakdown the gate dielectric does degrade and the gate leakage shoots up roughly 5 orders of magnitude. However, the gate dielectric degradation is not as severe nor as complete as that seen in the device on sample D. After catastrophic breakdown the gate only supplies roughly 1/3 of the total current to the drain contact, while the source contact continues to supply the remainder. This behavior is somewhere in between that of samples C and D. Immediately prior to breakdown the gate leakage is only 10 nA/mm, over 5 orders of magnitude less than sample D and approximately the same as on the Al_2O_3 sample. $V_{DS,BR}$ is significantly lower in sample A's device than on sample D (41 V versus 84 V) as well. Thus, this device on sample A serves as a mid-point between C and D, and again confirms that the event which initiates breakdown is almost certainly not coming from injected charge from the gate.

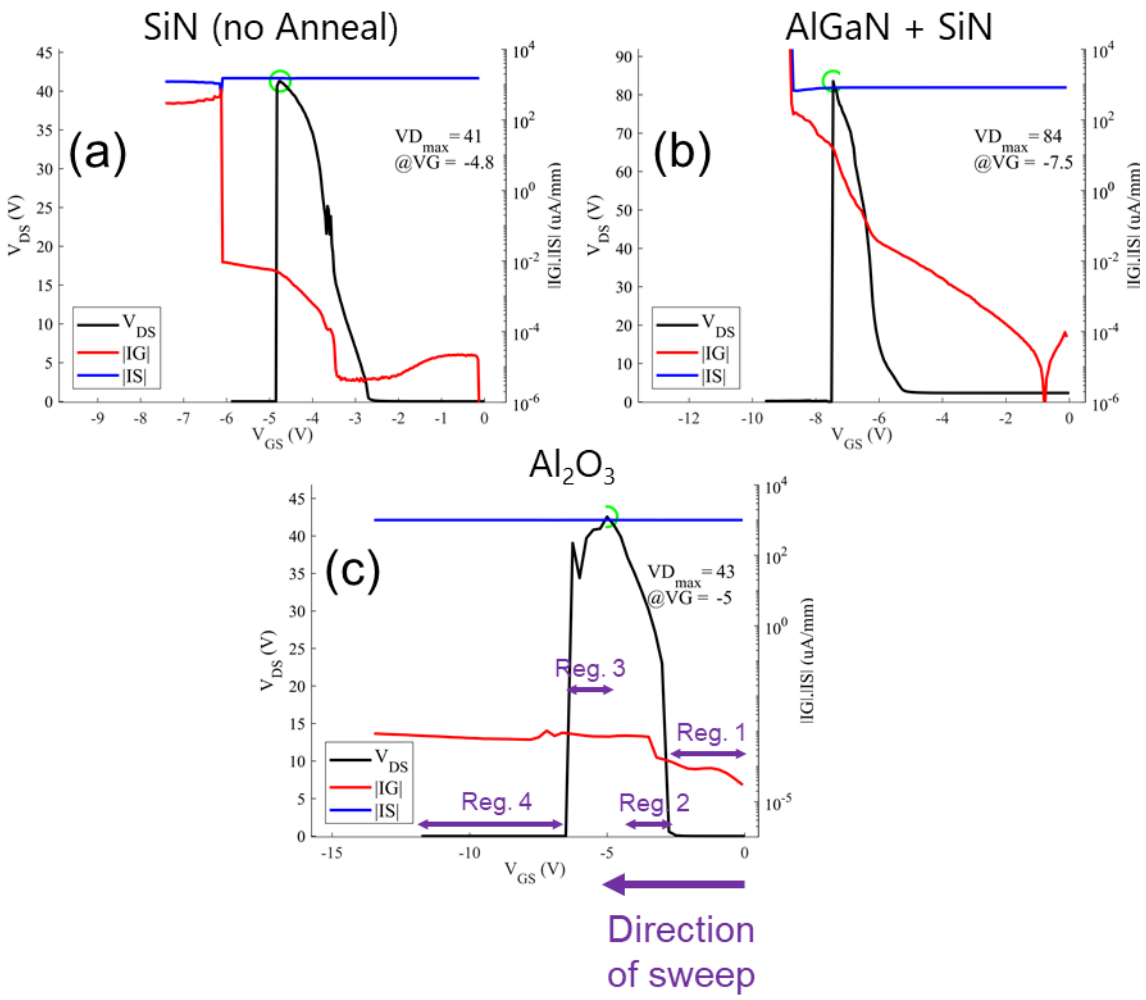


Fig. 2.13: DCI scans showing V_{DS}, I_S, and I_G taken with an injection current of 1 mA/mm for sample A, C, and D. Discussion of the characteristics of these traces is given in the text, although it should be noted that in some cases (not the one shown here), the Al_2O_3 gate dielectric did breakdown at the end of the DCI scan.

Chapter 2.2.7 – Breakdown Hypothesis:

The data presented in the previous section clearly demonstrate that $V_{DS,BR}$ is not initiated by the vertical degradation of the bulk gate dielectric in this set of samples. In other words, the initial breakdown event which leads to $V_{DS,BR}$ in this experiment is not caused by the vertical breakdown of the bulk gate dielectric. Still, all the devices in this experiment come from the same initial N-Polar 2" wafer. Thus, MISHEMTs from all 4 samples share the exact same 20 nm GaN channel. However, a clear difference in breakdown performance

between the samples is observed. The only plausible hypothesis that can explain the results is that the semiconductor/dielectric interface is the weak point and the source of the initial breakdown event which leads to the ultimate catastrophic failure of the device. To be clear, the hypothesis is that hot electrons from the channel cause a degradation of the semiconductor/dielectric interface and this is what initiates the chain of events which lead to device breakdown. This is the reason why the AlGaN + SiN gate cap stack had the highest $V_{DS,BR}$ of all the samples. The AlGaN layer introduces an additional ΔEc barrier to hot electrons transiting the channel. This additional barrier makes it more difficult for hot electrons from the channel to reach the semiconductor/dielectric interface (AlGaN/SiN in this case) and cause degradation and ultimately catastrophic failure of the device. Thus, in the AlGaN + SiN sample, higher voltages/channel electric fields relative to the other samples are required to enable channel electrons to gain sufficient energy to make it over the AlGaN barrier and rupture the bonds which exist between the semiconductor and the SiN.

Further, the AlGaN/SiN interface of sample D may be of higher quality than the other GaN/dielectric interfaces. It is possible that AlGaN intrinsically forms better/more stable interfaces with a MOCVD SiN dielectric. Additionally, the fact that this sample is the only regrowth to feature first a semiconductor growth then an *in situ* dielectric growth may actually be a better explanation (or at least an additional reason). Even though precautions were taken to clean the surface of the semiconductor and keep the sample in a vacuum sealed container prior to regrowth, the sample is, however briefly, still exposed to the outside environment for a small amount of time. This exposure could change the properties of the GaN surface prior to regrowth of the dielectric, most likely for the worse (could possibly form a poor quality oxide at the surface prior to growth of the desired gate dielectric). In the case of the AlGaN +

SiN sample, the AlGaN layer is first grown and the sample stays inside the MOCVD chamber as the growth conditions are changed prior to growth of the MOCD SiN. Thus, the surface of the semiconductor is never exposed to the outside atmosphere and the possibility of a higher quality semiconductor/dielectric interface is made more realistic. The GaN/AlGaN interface may be of lower quality than if the AlGaN was grown *in situ*, but it is not likely that this semiconductor/semiconductor interface is weaker than the semiconductor/dielectric one, so it is unlikely that the GaN/AlGaN interface is responsible for the breakdown event.

The Annealed + SiN sample had the 2nd highest $V_{DS,BR}$. Apparently, the NH_3 anneal did act to heal some of the surface damage caused after the oxidation + HF etch procedure. This likely improved the quality of the GaN/SiN interface. Aside from the fact that this sample had a higher breakdown than the other dielectric only regrowths, it was also the only sample (besides the AlGaN + SiN sample) to show little to no dispersion in PIV. The low dispersion suggests that the GaN/SiN interface is of at least reasonable quality and is likely superior to the other 2 dielectric only samples.

In comparison, the 2 samples which had the most dispersion in PIV also had the lowest $V_{DS,BR}$. Poor dispersion for these samples in PIV suggests traps in either the regrown bulk dielectric or at the interface between the dielectric and semiconductor. In the case of the MOCVD SiN sample, the quality of the bulk dielectric should be exactly the same as in the anneal + SiN sample, so trapping in that sample is most likely at the GaN/SiN interface. More traps at the GaN/dielectric interface suggests a weaker interface and is likely the reason why the non-annealed SiN only sample has a significantly lower $V_{DS,BR}$ than the sample with the NH_3 anneal + SiN regrowth. Aside from the annealing procedure to heal the GaN epitaxial surface prior to regrowth the 2 samples should be identical to one another.

Finally, the Al_2O_3 sample also had a significant amount of dispersion in PIV. This was also the first MOCVD Al_2O_3 dielectric regrowth performed on a N-Polar HEMT in our research group, so the growth procedure is likely not as well developed. Further, a TEM image taken of Al_2O_3 grown (Fig. 2.14) on the same reactor on a Ga-Polar GaN surface suggests that this interface is not perfectly abrupt, and therefore is likely to be both trappy and weak. No TEM was taken for this sample and the N-Polar/Al_2O_3 interface, so it is possible that this interface is of higher quality. Further, the significantly lower 2DEG density in this sample strongly suggests a large amount of negative charges exist either at the GaN/Al_2O_3 interface or in the bulk of the Al_2O_3 dielectric. All these pieces of data suggest, if not conclusively prove, that the interface between the GaN channel and the Al_2O_3 gate dielectric is of a poorer quality than of the other 3 samples, and this is the reason why the Al_2O_3 sample has the lowest $V_{DS,BR}$.

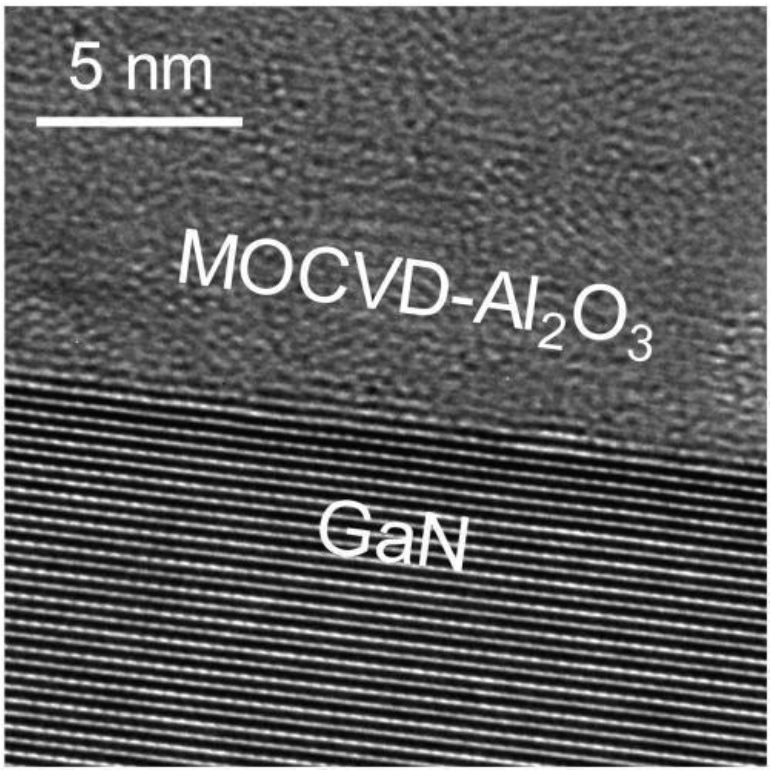


Fig. 2.14: Cross-sectional TEM image taken of a MOCVD Al_2O_3 growth on a Ga-Polar GaN sample in [22].

As a side note, the dispersion (electron trapping, or release of trapped holes) in the 2 samples with the lowest $V_{DS,BR}$ should actually ameliorate the E-Fields in the device, not increase them. This further supports the theory that the interface is the weak point because the E-Fields at a given voltage for the dispersive samples will actually be lower than that in the non-dispersive samples.

Chapter 2.2.7 – More Detailed Explanation of Breakdown Physics:

Knowing that the catastrophic failure of the device is initiated by the degradation of the semiconductor/dielectric interface enables us to explain the characteristics of each scan in Fig. 2.13. The description itself helps elucidate the deeper physics of breakdown taking place during the measurement.

Fig. 2.13 (c) shows the DCI scan for sample D, the Al_2O_3 dielectric sample with the lowest $V_{DS,BR}$ of all 4 samples. This scan can be subdivided into 4 regions of different V_{GS} values. The 1st region consists of $V_{GS} > V_{th}$ of the transistor device. As such, the channel is in the on-state, and very little V_{DS} is needed to satisfy the 1 mA/mm boundary condition placed on the drain contact. Region 2 occurs immediately after the channel is pinched off. Here, the V_{DS} rapidly rises with respect to increasing $|V_{GS}|$ to satisfy the boundary condition on the drain contact. Gate leakage also increases at the beginning of region 2, but remains extremely low at < 1 nA/mm. The device reaches its peak drain-source voltage ($V_{DS,BR}$) at the end of region 2. After reaching this peak voltage, the V_{DS} starts to decrease with increasing $|V_{GS}|$ (Region 3). Physically, this peak voltage represents the point at which the semiconductor/dielectric interface begins seriously degrading. Beyond this point, the semiconductor/dielectric interface begins to conduct a higher percentage of the injected drain current. The combination of the high voltage and the conduction current further degrades this

interface until the interface catastrophically fails and becomes highly conductive. In the Al_2O_3 sample, catastrophic failure of the semiconductor/dielectric interface occurs prior to any serious degradation of the Al_2O_3 gate dielectric, and very little increase in gate leakage is seen. The Al_2O_3 gate dielectric may momentarily be exposed to a high voltage (in the intermittent time as the B1500A electronics are responding to the device failure), but the Al_2O_3 was apparently thick enough/robust enough to handle the voltage spike without seriously degrading. Region 4 begins immediately after the catastrophic failure. The pathway between source and drain is essentially shorted now, and very little source-drain voltage is needed to satisfy the 1 mA/mm boundary condition on the drain contact. The gate leakage continues to very slowly increase. This is simply due to the increasing V_{GS} bias though.

The DCI scan of the MOCVD SiN only samples (Fig. 2.13 (b)) is very similar to the Al_2O_3 only sample. The main difference between the 2 stems from the fact that the SiN gate dielectric is less than ½ as thick as the Al_2O_3 dielectric. As a result, once catastrophic failure of the semiconductor/dielectric interface occurs, the voltage spike the SiN gate dielectric sees is enough to significantly degrade it and cause a rise in gate leakage roughly 5 orders of magnitude. The SiN dielectric is, however, thick enough to prevent it from catastrophically failing, and the gate leakage (though higher) only supplies roughly 1/3 of the total injected drain current.

Finally, the DCI scan of the $Al_{0.46}Ga_{0.54}N$ + SiN sample has 2 major differences relative to the other 2 samples shown in Fig. 2.13. First, because of the $Al_{0.46}Ga_{0.54}N$ layer and/or because of the higher quality semiconductor/dielectric interface, the $V_{DS,BR}$ is significantly higher in this sample as discussed earlier. Second, this sample has the thinnest and leakiest gate cap stack of all samples in this study. As a result, when the gate cap stack

sees the voltage spike at device failure, the gate dielectric degrades catastrophically and gate leakage shoots up to 30 mA/mm. After this point, the gate leakage supplies all 1 mA/mm to the drain contact, as well as ~29 mA/mm to the source contact.

Chapter 2.2.8 – Additional Semiconductor/Dielectric Quality Experiments:

One of the major takeaways from this regrown cap experiment is that the semiconductor/dielectric interface is the weak point in our N-Polar MISHEMT devices. Hot electrons generated during high voltage off-state stresses act to degrade this interface and it is this degradation that ultimately leads to the breakdown of the transistor device. From the standpoint of building the optimal N-Polar HEMT device, the major conclusion from this regrown cap experiment is that the $Al_{0.46}Ga_{0.54}N$ + SiN gate cap stack provides the highest breakdown voltage of all gate cap stacks investigated. This was despite the fact that it was the thinnest gate cap stack investigated (Table 2.1). Moreover, this is an important point, as the goal of this work is to build the optimal device for high frequency RF applications, and this requires both vertical and lateral scaling of the transistor. Two hypotheses were put forward to explain why this gate cap stack combination yielded the highest breakdown of all 4 samples investigated. The two theories are not mutually exclusive, and both may contribute to the higher breakdown seen in this sample. First, it is thought that the $Al_{0.46}Ga_{0.54}N$ layer introduces an additional ΔEc barrier to hot electrons transiting the channel. This additional barrier makes it more difficult for hot electrons from the channel to reach the semiconductor/dielectric interface and cause the degradation and ultimate failure of the device. Second, it is possible that the semiconductor/dielectric interface is of higher quality than the other semiconductor/dielectric interfaces investigated in this experiment. This may be because $Al_{0.46}Ga_{0.54}N$/SiN intrinsically forms a higher quality interface than the other

samples investigated in this experiment. It is also possible that the fact that this sample first had an $Al_{0.46}Ga_{0.54}N$ regrowth followed by the MOCVD SiN growth without ever breaking vacuum in the MOCVD chamber led to a higher quality interface than what was seen in the other samples.

In this section we try to investigate these hypotheses further. 2 new N-Polar MISHEMT samples nearly identical to the original 2" N-Polar wafer used in the previous regrowth experiment were grown here (Fig. 2.15). The major difference between the sample in the previous experiment and these 2 samples is the gate cap stack. In these 2 samples the 2.7 nm $Al_{0.46}Ga_{0.54}N$ portion of the gate cap stack was grown *in situ* during the initial growth of the wafer. The 2 samples underwent the same fabrication procedure as the samples used in the previous cap experiment. The one difference is that the cleaning procedure prior to regrowth of the gate dielectric consisted of only a 30" HF dip. After this dip, 5 nm of *ex situ* MOCVD SiN was regrown on top of the *in situ* $Al_{0.46}Ga_{0.54}N$ cap. Because the gate dielectric was grown *ex situ*, this will be referred to as the *ex situ* $Al_{0.46}Ga_{0.54}N$ + SiN samples. The rest of the sample fabrication process was identical to that of the regrown cap samples.

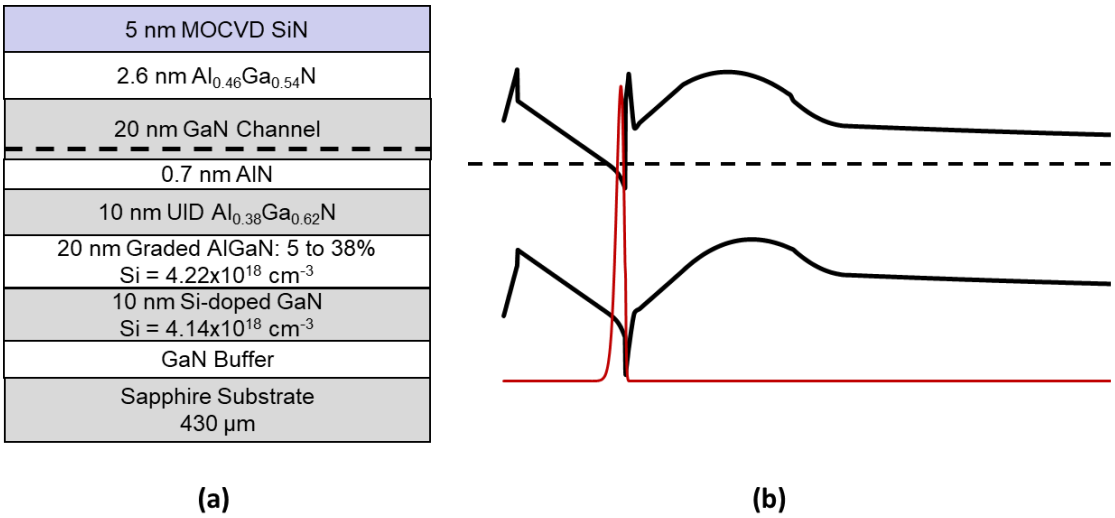


Fig. 2.15: N-Polar HEMT structure discussed in this section. Gate cap stack consists of a 2.6 nm $Al_{0.46}Ga_{0.54}N$ top-barrier grown at the end of the initial epitaxial MOCVD growth and a 5 nm MOCVD SiN gate dielectric regrown *ex situ* after some processing. The cross-section of the epitaxial structure is shown in (a). The energy band diagram is shown in (b). Simulations assume a Schottky gate structure with a pinning position of 1 eV to avoid making assumptions about the charge density located at the $Al_{0.46}Ga_{0.54}N$/SiN interface.

Structurally, the gate cap stack of these 2 samples is identical to that of sample D in the previous experiment. Unlike sample D, the regrowth does not begin with a semiconductor III-N growth, but starts directly with the MOCVD SiN dielectric growth. If beginning the regrowth with $Al_{0.54}Ga_{0.46}N$ leads to a better semiconductor/dielectric interface, than these 2 samples should have a lower $V_{DS,BR}$ than what was measured in sample D.

Breakdown measurements were made with the DCI method on several devices from both these samples. Statistical box plots of $V_{DS,BR}$ for all gate cap stacks investigated are plotted with respect to gate cap stack and L_{GD} in Fig. 2.16. $V_{DS,BR}$ data from these 2 samples are combined in this plot since they share the same gate cap stack. These 2 samples have higher $V_{DS,BR}$ than all the dielectric only samples, further confirming the breakdown benefits of the $Al_{0.46}Ga_{0.54}N$ cap. However, these 2 samples have lower breakdown voltage than sample D. This suggests that the initial growth of the $Al_{0.46}Ga_{0.54}N$ layer prior to MOCVD SiN growth does indeed lead to a stronger semiconductor/dielectric interface.

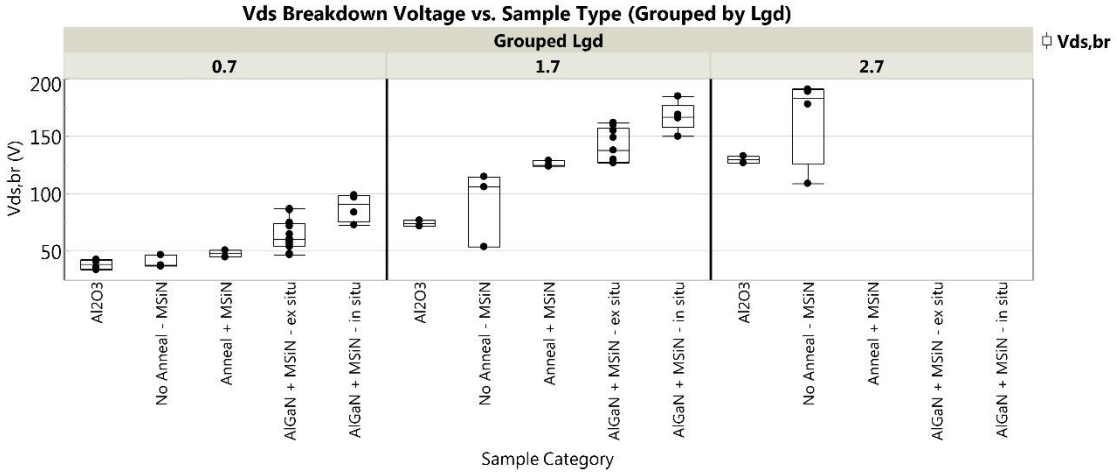


Fig. 2.16: Statistical box plots showing $V_{DS,BR}$ vs. L_{GD} for all sets of samples examined in this gate cap stack investigation.

Chapter 2.2.9 Gate Cap Stack Conclusion:

The gate cap stack of N-Polar MISHEMT devices was investigated in this section of the thesis. Specifically, the gate cap stack's effect on off-state breakdown performance was thoroughly examined. The semiconductor/dielectric interface was found to be the weak point during off-state breakdown, and was identified as the portion of the device which ultimately limits the breakdown performance of the MISHEMT. Adding a thin $Al_{0.46}Ga_{0.54}N$ epitaxial in addition to a MOCVD SiN gate dielectric was found to significantly enhance breakdown voltage with respect to all other gate cap stacks explored in this experiment. This was despite the fact that the total gate cap stack in the $Al_{0.46}Ga_{0.54}N$ + SiN sample was substantially thinner than all other gate cap stacks investigated. Moreover, this is an important point, as the goal of this work is to find the optimal gate cap stack for a N-Polar transistor in high frequency RF applications. To do this, requires both vertical and lateral scaling of the transistor.

Three hypotheses were put forward as to why the $Al_{0.46}Ga_{0.54}N$ + SiN gate cap stack has the highest breakdown performance of all gate cap stacks investigated. The theories are not mutually exclusive, and 2 of the 3 were strongly supported by the data generated from the

experiments. First, it is thought that the $Al_{0.46}Ga_{0.54}N$ layer introduces an additional ΔEc barrier to hot electrons transiting the channel. This additional barrier makes it more difficult for hot electrons from the channel to reach the semiconductor/dielectric interface and cause the degradation and ultimate failure of the device. The second and third hypotheses deal with the semiconductor/dielectric interface quality. There were multiple $Al_{0.46}Ga_{0.54}N$ + SiN samples with varying degrees of $Al_{0.46}Ga_{0.54}N$/SiN interface quality, and all of them had higher breakdown voltages than all other gate cap stacks investigated in this experiment. Because of this, the data seems to strongly support, though not conclusively confirm, the theory that the $Al_{0.46}Ga_{0.54}N$ layer helps improve breakdown by making it more difficult for hot channel electrons to reach, degrade, and ultimately cause catastrophic failure at the semiconductor/dielectric interface.

The second hypothesis posited was that when regrowth of the gate cap stack began with the growth of a semiconductor layer first followed by the gate dielectric without ever breaking vacuum in the MOCVD chamber, a higher quality semiconductor/dielectric interface was created. The fact that the sample with the regrown $Al_{0.46}Ga_{0.54}N$ + SiN had a higher breakdown voltage than the 2 samples with the exact same (structurally speaking) gate cap stack, but where the SiN was the 1st and only part of the gate cap stack, suggests that this also true.

The third hypothesis put forward is that the $Al_{0.46}Ga_{0.54}N$/SiN interface is intrinsically of higher quality than the other semiconductor/dielectric interfaces examined in this work. This theory was not directly tested, so it cannot be ruled out. Further, because this theory was not ruled out, it is still possible that electrons injected from the gate contribute to the degradation and ultimate catastrophic failure of the semiconductor/dielectric interface (first

hypothesis only relates to hot electrons injected laterally across the channel from the source contact). The gate leakage immediately prior to device failure is orders of magnitude higher in the regrown $Al_{0.46}Ga_{0.54}N$ + SiN device than in the dielectric only gate cap stack samples. Yet despite this, the regrown $Al_{0.46}Ga_{0.54}N$ + SiN device still has the highest breakdown of all samples investigated. Thus, the hypothesis that gate injected electrons contribute to device failure seems unlikely, but again, cannot be ruled out if it turns out that the $Al_{0.46}Ga_{0.54}N$/SiN interface quality is substantially better than all the other semiconductor/dielectric interfaces investigated in this study.

Finally, because the semiconductor/dielectric interface was identified as the portion of the device which limits breakdown in our MISHEMTs, one might conclude that we should remove the dielectric and just have a schottky gate. However, this would lead to even worse breakdown performance. As Rajan *et al.* showed in [3] a schottky junction formed on N-Polar GaN has a very low barrier height and is extremely leaky. The gate is so leaky that the device essentially experiences a premature breakdown event, and the $V_{DS,BR}$ is much lower than one might expect. Even when he formed a schottky gate to a N-Polar HEMT with an AlGaN cap, the device was still extremely leaky, and breakdown was lower than one would expect for a device with that 2DEG density. Further, schottky gates were formed directly on the *in situ* $Al_{0.46}Ga_{0.54}N$ + SiN on some die by etching through the MOCVD SiN gate dielectric in this experiment. These devices were also extremely leaky. Essentially, these schottky gate devices on N-Polar epi are extremely leaky and cause premature breakdown of the device in the off-state. Adding a dielectric helps reduce this leakage and actually increases the breakdown voltage of the device. The thicker the dielectric the higher the breakdown voltage, up until a certain thickness of gate dielectric is reached. Beyond this thickness, the breakdown

mechanism stops being vertical, starts becoming horizontal, and is limited by the degradation at the semiconductor/dielectric interface. Once the dielectric has reached this thickness, if the N-Polar MISHEMT designer wants to increase the breakdown voltage, the engineer must find a way to either protect this semiconductor/dielectric interface from seeing hot electrons, or find a way to improve the quality of this interface. More on this will be given in the next section.

Ch. 2.3 – Back-Barrier Doping + Channel 2DEG Density Optimization:

This section is devoted to finding the optimal back-barrier doping and channel 2DEG density for the back-barrier and gate cap stack investigated in the previous section (Fig. 2.17). The section begins by outlining the parameters around which the back-barrier doping is optimized around. The next subsections cover the experimental details, fabrication procedure, and the static and small signal RF results. The final sections look at the tradeoff between breakdown voltage, dispersion, doping density, and channel 2DEG density.

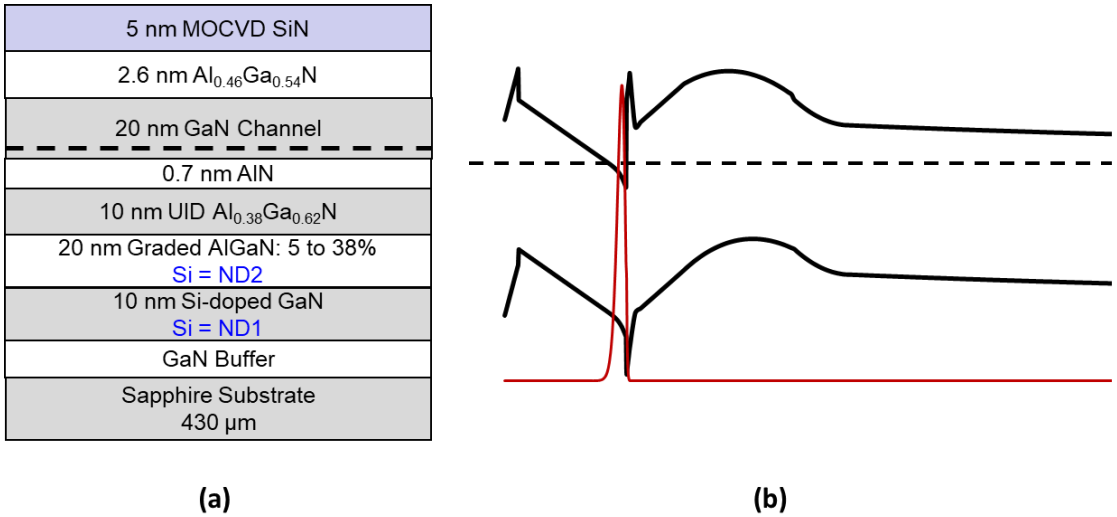


Fig. 2.17: Epitaxial cross-section (a) and band diagram (b) for the N-Polar transistors investigated in this section of the thesis. The energy band diagram is shown in (b). Simulations assume a Schottky gate structure with a pinning position of 1 eV to avoid making assumptions about the interfacial charge located at the $Al_{0.46}Ga_{0.54}N$/SiN interface. The Si doping in the Graded AlGaN and Si-doped GaN were varied as ND2 and ND1, respectively in this section of the thesis.

Chapter 2.3.1 – Introduction:

N-Polar engineers must contend with an additional design consideration that is absent in conventional schottky-gate Ga-Polar HEMTs. At negative polarization interfaces there exists a "hole trap" (deep donor) level located ~60-100meV above the VB [3], [23-26]. Such a negative polarization interface exists at the GaN buffer/AlGaN back-barrier interface in N-Polar HEMTs (Fig. 2.17), but is absent in conventional AlGaN/GaN schottky-gate Ga-Polar transistors (Fig. 2.18). Rajan *et al*. [3] found that when the electron Fermi-level is in proximity of this hole trap energy level at equilibrium, large signal dispersion is seen in PIV similar to that seen in Ga-Polar (and N-Polar) HEMTs from buffer/surface trap states. Nidhi *et al* and Denninghoff also made similar observations in N-Polar HEMTs [9-10]. An anomalous DC output conductance has also been attributed to the electron Fermi-level being in proximity of this trap [26]. To move the electron Fermi level away from the hole trap one can delta dope the negative polarization interface with Si [27]. Sufficiently high Si-doping concentrations can remove the dispersion associated with the hole trap.

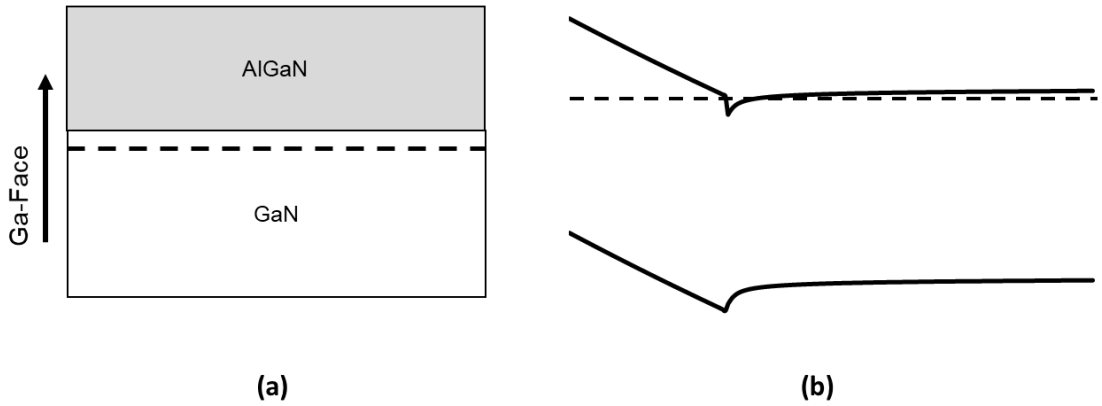


Fig. 2.18: Epitaxial cross-section (a) and band diagram (b) for a basic Ga-Polar HEMT structure. In such a Schottky gate structure, there is typically no III-N material grown on top of the AlGaN top-barrier. As such, surface reconstruction likely occurs and the same defect levels likely are not present.

Alternatively, Si-doping in conjunction with a graded $Al_xGa_{1-x}N$ back-barrier can be used for the same purpose. Such a scheme is implemented in this work. This structure expands the design window associated with the Si-doping of the back-barrier. A graded $Al_xGa_{1-x}N$ layer spreads the negative polarization charge and lowers the Si-doping density required to eliminate hole trap related dispersion. Lower doping densities allow subsequent epi-layers on top of the back-barrier to be grown at a high quality. Further, this back-barrier design increases the total amount of Si-doping that can be used in the negative polarization layers prior to the formation of a parasitic 2DEG at the back-side $Al_xGa_{1-x}N$/GaN interface (or within the $Al_xGa_{1-x}N$ back-barrier itself). Such a parasitic 2DEG causes output conductance and poor pinch-off issues in the transistor, making removal of it critical for high performance N-Polar HEMTs.

Implementation of this graded + Si-doped back-barrier is not novel to this work. Shen *et al*. was the 1st to use this design to move the electron Fermi level away from the hole trap at the top GaN/AlGaN interface that existed in his Ga-Polar Deep Recess structure [23]. Rajan *et al*. was the 1st to adopt this design to N-Polar transistors. Subsequent N-Polar students further optimized this back-barrier structure [9-10] and [28]. The back-barrier design utilized here is essentially identical to that used by Seshadri. However, since Seshadri's time improvements to the Thomas Swan MOCVD reactor used to grow the N-Polar samples has dramatically reduced the background O impurity concentration in the N-Polar epi-layers. Oxygen acts as a shallow donor in GaN, and therefore changes the position of the electron Fermi level relative to the hole trap in a similar fashion to Si-doping. As a result, the amount of Si-doping concentration used in the back-barrier had to be re-optimized. Additionally, the 2DEG density in the channel varies with the back-barrier doping density as (eq. 2.1).

$$ns = \left(\frac{\frac{\varepsilon}{q} \cdot (\Delta E_C - \varphi_B) - \sigma_{AlGaN_{top}} \cdot t_{AlGaN_{top}}}{t_{AlGaN,top} + t_{chan} - \Delta d1} \right) + \sigma_{Si} \quad (2.1)$$

In this equation, ns is the channel 2DEG density, ε is the dielectric constant of GaN, ΔE_C is the difference in conduction band height between the GaN and the AlGaN top barrier, φ_B is the assumed pinning position between the III-N semiconductor and the MOCVD SiN dielectric, q is the elementary unit of electron charge, $\sigma_{\pi,AlGaN,top}$ is the net polarization charge at the top AlGaN barrier/GaN channel interface, σ_{Si} is the total Si doping (in cm^{-2}) in the graded AlGaN back-barrier and Si-doped GaN layer, Δd1 is the distance between the AlN interlayer and the centroid of the channel 2DEG, $t_{AlGaN,top}$ is the thickness of the AlGaN top-barrier, and t_{chan} is the thickness of the UID GaN channel.

Since the back-barrier doping experiment had to be done anyway, a broader study exploring how the total 2DEG density in the channel effects device performance was conducted in parallel using the same samples.

Chapter 2.3.2 – Experimental Details + Fabrication Procedure:

In this work, a systematic study was performed to investigate the back-barrier doping and channel charge density's effect on overall device performance. Breakdown voltage was found to be the parameter which varied most strongly with doping/2DEG charge density for samples of this particular design. This aspect of device performance is explored in detail later in this section.

Experimental Details:

A series of samples with the same nominal structure (Fig. 2.17), but different doping densities in the Si-doped GaN and graded AlGaN regions were grown via MOCVD on a

sapphire substrate. From this point forward in this section of the thesis, the samples shall be identified by the total back-barrier doping used to grow them. Growth conditions are similar to that reported in [1]. In addition to the back-barrier, all samples contain a 20nm GaN channel, a 2.6nm $Al_{0.46}Ga_{0.54}N$ cap, a 5 nm high temperature MOCVD SiN gate dielectric, and a 120nm thick PECVD SiN passivation layer. In-dot Hall data for all samples is shown in Table 2.4. The mobility is approximately constant with respect to doping density, remaining within the measurement error across all doping densities explored. However, it should be noted that the mobility results extracted from this Hall measurement is a combination of the mobilities of the channel 2DEG in both the parallel and perpendicular directions relative to the substrate miscut according to Matthiessen's rule (eq. 2.2). Because the gates of all the devices are oriented in the high mobility (parallel to the substrate miscut) direction, this means that this mobility is an underestimate of the actual channel 2DEG mobility in the actual transistor devices.

$$\mu_{Hall} = \frac{1}{\frac{1}{\mu_{parallel}} + \frac{1}{\mu_{perpendicular}}} \tag{2.3.2}$$

	ND1 $x10^{18}cm^{-3}$	ND2 $x10^{18}cm^{-3}$	Total Doping $x10^{13}cm^{-2}$	2DEG $x10^{13}cm^{-2}$	Mobility $cm^2/(V\cdot s)$
A	2.17	2.18	0.65	0.95	1598
B	3.61	3.63	1.09	1.03	1460
C	4.14	4.22	1.26	1.09	1410
D	4.68	4.8	1.43	1.11	1480
E	6.51	6.56	1.96	1.19	1480
F	4.14	9.13	2.24	1.45	1490
G	9.05	9.13	2.73	1.56	1370

Table 2.4: Doping density and In dot hall results for the series of samples grown in this experiment.

Optical gate devices (no additional field plating) with PAMBE n+ regrown contacts were fabricated on the samples with a total back-barrier doping of 1.26, 1.43, 1.96, and $2.73 \cdot 10^{13}$ cm^{-2} from the table. The Fabrication process for these samples is nearly identical to what was done for the regrown cap devices in the previous section. The only difference is

that the wet treatment prior to the MOCVD SiN gate dielectric regrowth only consisted of a 30" HF (48% concentrated) dip. No UV ozone + wet etch process was utilized. The majority of the data in this section focuses on these devices. However, devices with a Slant Field Plate were also fabricated on these wafers (Fig. 2.19). Such devices have better control of the passivation layer and E-Fields which induce dispersion and were included in this experiment to facilitate a "cleaner" investigation of the role doping/2DEG density plays with regards to DC-to-RF dispersion. Further, devices with alloyed contacts were also fabricated on additional quarters from the 1.26, 1.43, and $2.73 \cdot 10^{13}$ cm^{-2} samples. Transistors with alloyed contacts were fabricated on the 0.65, 1.09, and $2.24 \cdot 10^{13}$ cm^{-2} as well. The device performance of these alloyed contact samples is the subject of section 2.4, but because these devices covered a wider range of doping/2DEG densities, their TLM results are included in the next sub-section of this section.

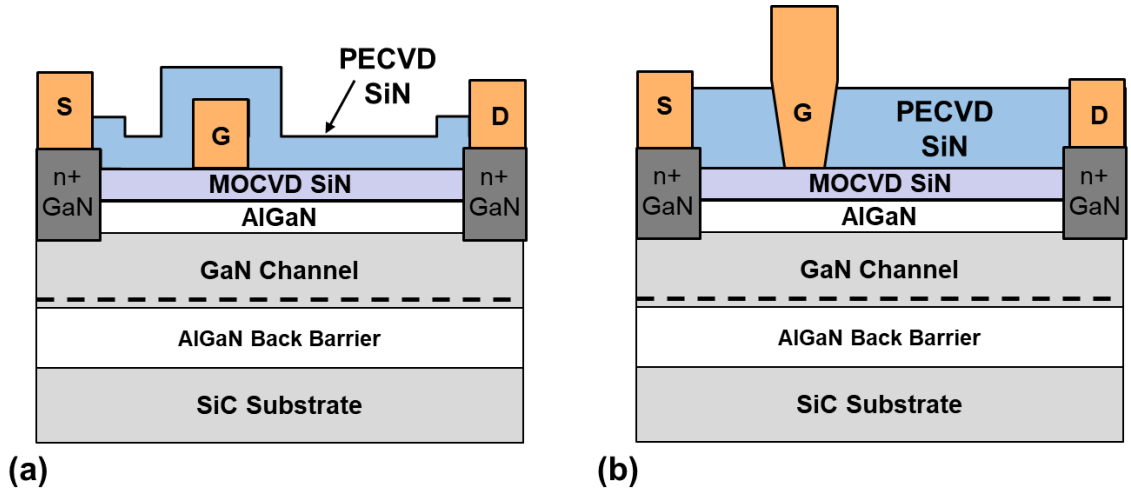


Fig. 2.19: The two types of N-Polar MISHEMT device structures fabricated in this section of the thesis. (a) Depicts a gate first device where the gate electrode metal is deposited prior to the deposition of the PECVD SiN passivation layer. (b) Shows a slant field plate device where the gate metal electrode is deposited after the deposition and subsequent gate recessing of the PECVD SiN.

TLM results from the alloyed contact samples are shown in Table 6. The TLM extracted sheet resistance (Rsh) is plotted vs. 2DEG density (ns) measured via In dot Hall in

Fig. 2.20 (a). A clear linear relationship between Rsh and ns is observed. Mobility extracted from the Rsh and ns data is plotted vs. ns in Fig. 2.20 (b). The fact that mobility is roughly constant with respect to 2DEG density is actually an extremely important finding. To the best of the authors' knowledge this is the 1st time mobility this high has been found to be constant with respect to such a wide range of 2DEG densities at or exceeding $0.95 \cdot 10^{13}$ cm^{-2} in MOCVD grown III-N HEMTs of N, Ga, or any other polarity. Typically, mobility will start to drop as 2DEG density increases much beyond $1 \cdot 10^{13}$ cm^{-2} in MOCVD grown III-N HEMTs [14]. The typical drop seen in mobility has been attributed to increased electron wavefunction penetration into the charge inducing $In_yAl_xGa_{1-x-y}N$ back-barrier. Both alloy scattering and interfacial dipole scattering [29] have been identified as the specific scattering mechanisms which causes the drop in electron mobility. A similar drop with respect to higher 2DEG density is not seen in these samples though. This is because of the pure binary AlN interlayer that exists at the interface between the GaN channel and the back-barrier in this set of N-Polar samples. The pure binary AlN interlayer in these N-Polar samples effectively cuts off the wavefunction penetration into the alloyed $Al_{0.38}Ga_{0.62}N$ back-barrier and pushes the centroid of the 2DEG further from the GaN/AlN interface, even for the highest charge densities investigated in this experiment. As a result, the scattering, be it alloy or interfacial, is greatly reduced in these samples, and very high 2DEG mobility is seen across a wide range of charge densities. Atom probe tomography has shown that MOCVD N-Polar HEMTs [30] can be grown with a pure binary AlN layer under an extremely wide range of growth parameters. This is not true of MOCVD grown Ga-Polar HEMTs [31-33]. Despite claims of AlN interlayers being grown in MOCVD Ga-Polar HEMTs, to the best of the author's knowledge, pure binary AlN has not actually been demonstrated to exist with Atom Probe

Tomography at any point in MOCVD grown Ga-Polar HEMTs. Thus, the Ga-Polar HEMTs suffer from higher raters of alloy and/or interfacial dipole scattering at higher 2DEG densities, resulting in lower overall 2DEG mobilities at higher charge densities. However, pure binary AlN has been demonstrated via Atom Probe Tomography in Ga-Polar PAMBE grown HEMTs [33]. As such, very high 2DEG mobilities have been demonstrated across a wide range of 2DEG densities in these PAMBE HEMTs. This is also true of PAMBE N-Polar HEMTs [34].

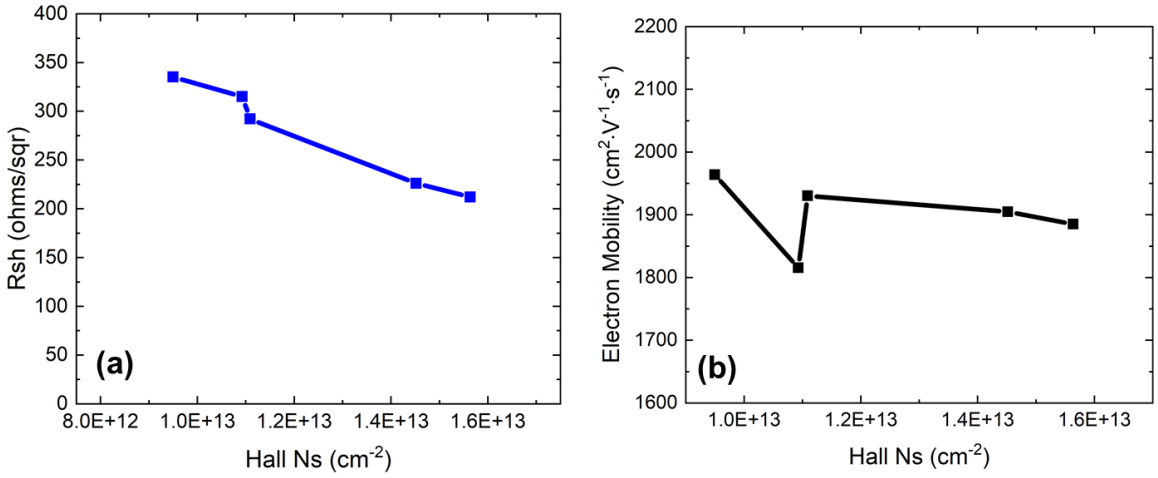


Fig. 2.20: The sheet resistance measured via TLM vs. the 2DEG distance measured from In dot Hall measurements is shown in (a). From these Rsh and Hall ns values, the electron mobility is calculated and plotted in (b).

Chapter 2.3.3 – DC and Small-Signal RF Results:

The differences in doping concentration for the first 1.26, 1.43, and $1.96 \cdot 10^{13}$ cm^{-2} samples did not appreciably change the 2DEG concentration measured in the channel despite large differences in back-barrier doping. As such, the DC performance of these 3 samples were nearly identical (Table 2.5). The much more highly doped sample ($2.73 \cdot 10^{13}$ cm^{-2}) did have a significant increase in ns. This resulted in a higher saturation current density and a slightly lower Ron than the other 3 samples. The discrepancy in charge density did not seem

to have an effect on transconductance or the small signal RF performance of the transistors, with all samples achieving roughly the same performance as one another.

DC						RF	
Doping Density (10^{13} cm^{-2})	In Dot Hall Ns (10^{13} cm^{-2})	I_{DS} (A/mm) (V_{GS} = 0 V)	R_{ON} (Ω·mm) (V_{GS} = 0 V)	Peak gm_{ext} (mS/mm)	Vth (V)	Peak f_T (GHz)	Peak f_{max} (GHz)
1.26	**1.09**	1.25	1.1	312	-2.8	15.1	52.8
1.43	**1.11**	1.25	1.2	315	-2.8	17	54.75
1.96	**1.19**	1.25	1.2	303	-3.5	NA	NA
2.73	**1.56**	1.48	1.0	318	-4.3	18	48.2

Table 2.5: DC and RF performance for the gate 1st N-Polar MISHEMTs discussed in this section. DC measurements were made on transistors with an L_G = 0.7 µm, L_{GS} = 0.7 µm, L_{GD} = 1.7 µm, and W_G = 2 x 75 µm. RF measurements were made on devices with the same dimensions, but with an L_G = 0.7 µm.

Chapter 2.3.4 – Breakdown Voltage:

Drain current injection (DCI) measurements [17] were then made on these 4 samples to see how the doping density, and increased 2DEG charge, affects the breakdown performance of the device. A 1 mA/mm injection current was used*. Breakdown results taken on non-field plated devices for each of the 4 samples is shown in Fig. 2.21.

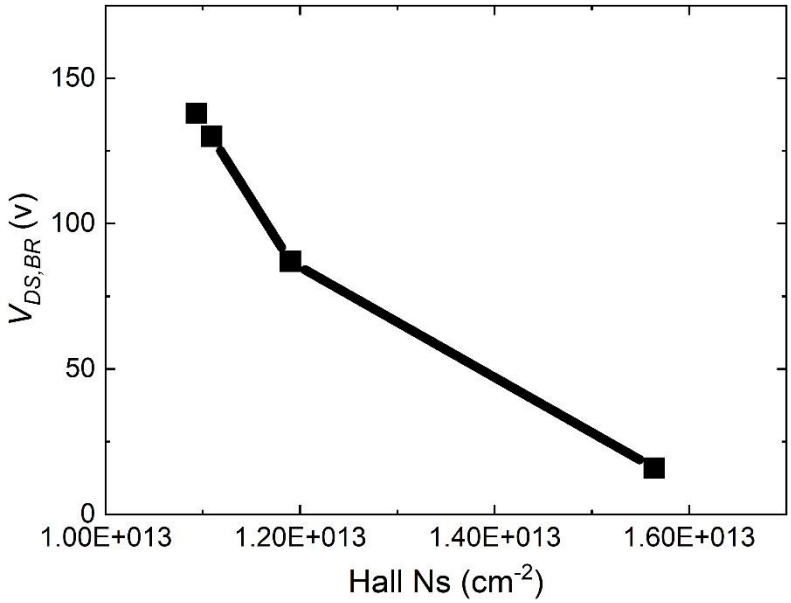


Fig. 2.21: Source-drain breakdown voltage with respect to the 2DEG density of the sample, as measured via In dot Hall. All devices had an L_G = 0.9 µm, L_{GS} = 0.7 µm, L_{GD} = 1.7 µm, and W_G = 2 x 75 µm.

A clear trend of decreasing off-state breakdown voltage with increasing doping concentration is observed. The fact that breakdown voltage shows this general trend is not surprising. Basic electrostatics implies that the samples with higher 2DEG charge densities should have higher channel E-Fields for a given set of bias conditions. This should lead to lower breakdown voltages in the samples with higher channel charge. However, the 5x difference in $V_{DS,BR}$ between the lowest and highest doped samples cannot be explained by basic electrostatics alone. Fig. 2.22 (a) compares the simulated lateral E-Fields for 2 HEMTs with different 2DEG densities at a V_{DS} = 30 V (the approximate $V_{DS,BR}$ of the highest doped sample). The magnitude of the peak lateral E-Field for higher doped simulation sample is 1.94 MV/cm. The peak lateral E-Field for the lower doped simulation sample is 1.63 MV/cm. At a V_{DS} = 45 V, the peak lateral E-Field of the lower doped simulation sample matches the peak of the higher doped sample at 30 V. If the breakdown of the lowest and highest doped real samples is initiated by the degradation of the semiconductor/dielectric interface as detailed in section 2.2, one would expect a similar discrepancy between the breakdown voltages of the

real highest and lowest doped samples (i.e. a discrepancy of around 50%). However, the discrepancy in $V_{DS,BR}$ is 5x. This suggests that the breakdown mechanism occurring in the highest and lowest doped samples differ.

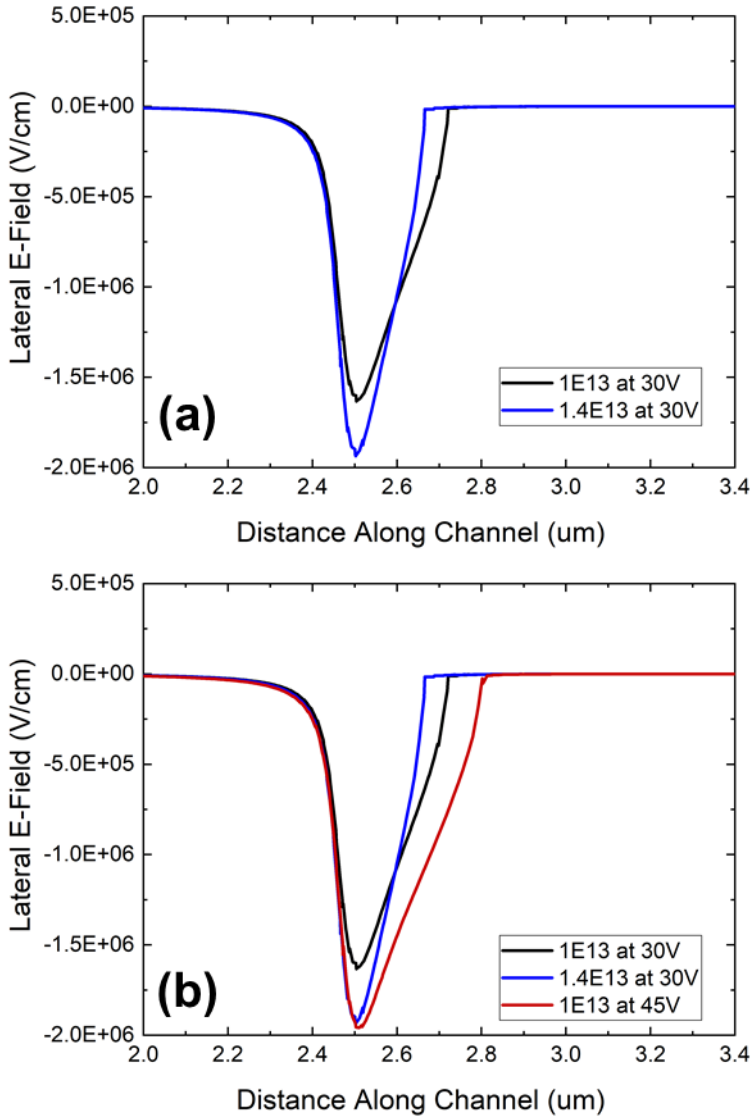


Fig. 2.22: Simulated lateral electric field along the 2DEG channel for a sample with a 2DEG density of $1 \cdot 10^{13}$ and $1.4 \cdot 10^{13}$ cm^{-2} at a V_{DS} = 30 V (a). In (b) it is shown that the peak lateral E-Field of the $1 \cdot 10^{13}$ cm^{-2} sample at a V_{DS} = 45 V is approximately equal to the peak lateral E-Field of the $1.4 \cdot 10^{13}$ cm^{-2} sample at 30 V.

Representative DCI scans for transistors from the 1.26, 1.96, and $2.73 \cdot 10^{13}$ cm^{-2} samples are given in Fig. 2.23. Analysis of these scans gives further insight into the

breakdown mechanisms at play. The lowest doped sample behaves in a similar fashion to the samples of section 2.2. Two breakdown events can be identified. At the lower V_{DS} value a "channel breakdown" occurs. The $\frac{V_{DS}}{V_{GS}}$ slope decreases after this channel breakdown until V_{DS} reaches its peak. At this point the gate dielectric breaks down and the device catastrophically fails. The behavior of the 2 highest doped samples is very different. In these samples, no channel breakdown is observed and only a single gate breakdown event occurs. Further, after V_{DS} reaches its peak value, the gate dielectric degrades, but does not catastrophically fail like in the lower doped samples.

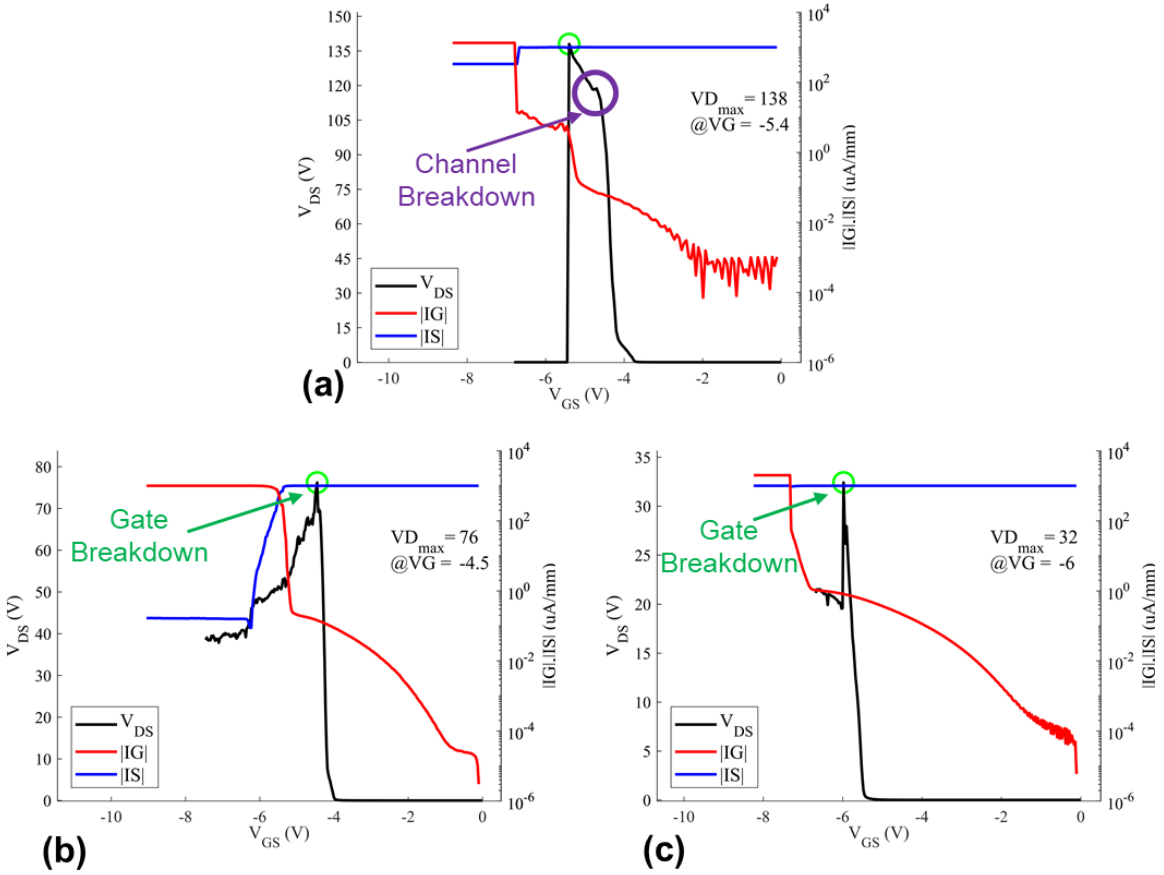


Fig. 2.23: DCI scans for the (a) $1.26 \cdot 10^{13}$, (b) $1.96 \cdot 10^{13}$, and (c) $2.73 \cdot 10^{13}$ cm^{-2} samples discussed in this section taken at a drain injection current density of 1 mA/mm.

The characteristics shown in the DCI scans of Fig. 2.23 generally held true for the rest of the devices measured on both the lower doping and higher doping set of samples. Fig. 2.24 (a) shows the percentage of Gate/Chanel failures that occur for each back-barrier doping investigated. Fig. 2.24 (b) illustrates the percentage of catastrophic vs non-catastrophic fails for the gate/channel breakdowns of each sample. In general, devices which have a channel breakdown fail catastrophically, while those which only experience a gate breakdown do not fail catastrophically.

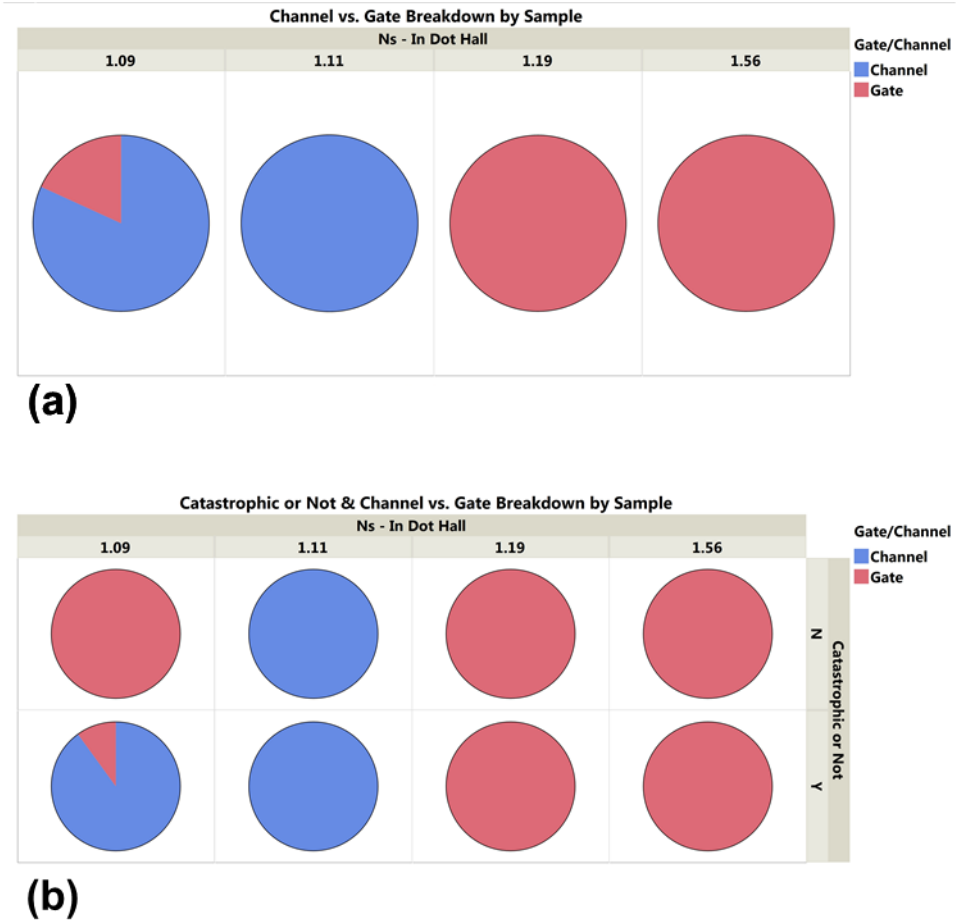


Fig. 2.24: Pie chart depicting the percentage of devices which breakdown in a particular fashion for each sample investigated in this section categorized by that sample's 2DEG density. (a) Shows the percentage of devices which experience a channel breakdown prior to the gate breakdown event. (b) Also depicts this, but it is split into sets of transistors whose gate breakdowns were catastrophic, and those devise whose gate breakdown event did not lead to catastrophic failure of the transistor.

Fig. 2.25 shows $V_{DS,BR}$ versus L_{GD} for all 4 samples. Like the regrown gate cap samples from the previous section, $V_{DS,BR}$ scales linearly with L_{GD} for the lower doped samples This behavior is not seen in the higher doped samples. In the 2 higher doped samples, $V_{DS,BR}$ remains approximately constant across a wide range of L_{GD} spacings.

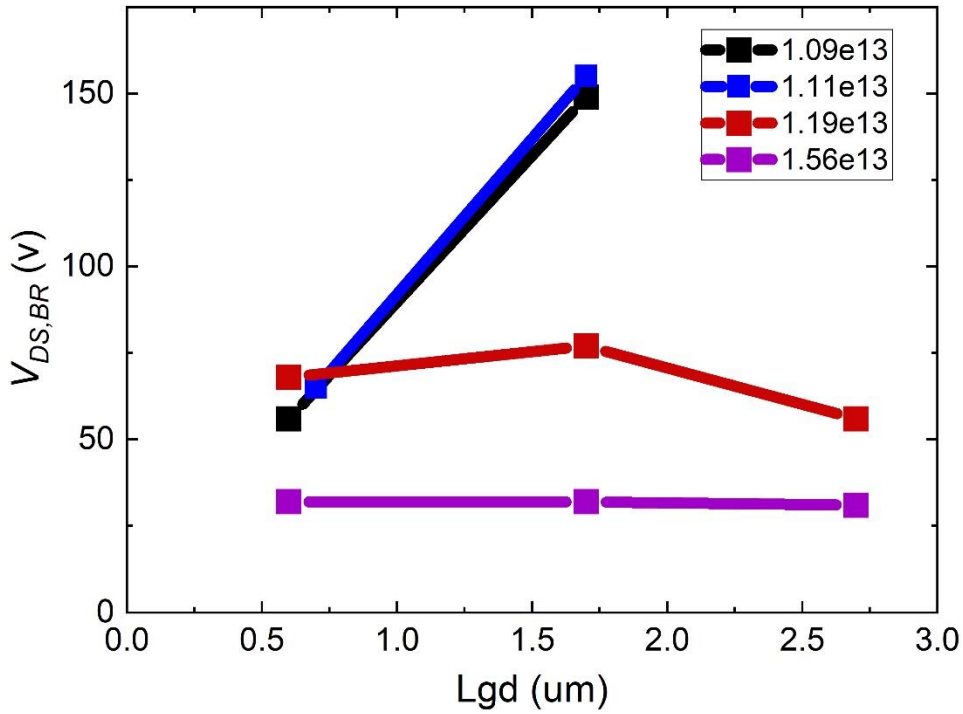


Fig. 2.25: Breakdown voltage with respect to gate-drain distance for each sample (categorized by 2DEG density).

All these sets of data indicate that different physical processes govern the off-state breakdown in the lower and higher doped samples. The lower doped samples behave in exactly the same fashion as the regrown gate cap samples of section 2.2. Thus, the physical mechanism causing breakdown is likely the same as the mechanism explained in that section. That is, degradation of the semiconductor/dielectric interface from hot electrons originating in the channel is what initiates the breakdown process. The point at which significant degradation of this interface takes place is most likely the voltage where "channel breakdown" occurs. After channel breakdown/significant degradation of this interface happens, the ability of the channel to hold increased V_{DS} with more negative V_{GS} is reduced. At some point the

semiconductor/dielectric interface catastrophically fails and conducts a significant fraction of the current. At that moment, the whole dielectric underneath the gate sees a relatively large voltage as the electronics of the B1500A respond to the device degradation and try to maintain the 1 mA/mm boundary condition on the drain contact. Because the gate dielectric used here (5 nm of MOCVD SiN) is significantly thinner than the 20 nm Al_2O_3 and 9 nm MOCVD SiN samples of the previous section, it cannot handle this voltage, and some weak point in the amorphous dielectric catastrophically fails. After this point, the gate conducts all of the current to satisfy the 1 mA/mm boundary condition at the drain.

A different physical mechanism controls the "soft" breakdown that occurs in the higher doped samples. In these samples, 100% of the breakdowns were of the "gate" breakdown variety. During the DCI scans of the higher doped samples (Fig. 2.23), once the device reaches pinch-off the gate leakage increases rapidly until the gate leakage alone completely satisfies the 1 mA/mm boundary condition on the drain contact. The combination of high voltage and relatively high conduction current across the gate dielectric does lead to gate dielectric degradation. However, for the vast majority of the highly doped transistors, this process does not cause catastrophic failure of the device or its gate dielectric (Fig. 2.24). Further DCI measurements can be made on the same device (Fig. 2.26), albeit with a lower $V_{DS,BR}$. This data suggests that the gate dielectric in the higher doped samples degrades faster than the semiconductor/dielectric interface during the breakdown measurement. Because of the more negative threshold voltage (Table 2.5) and higher 2DEG concentration, a higher vertical voltage drop (E-Field) exists across the gate cap stack in the highly doped samples. This leads to significantly higher gate leakages in the higher doped samples than in the lower doped ones. Fig. 2.27 is a representative plot of 3-terminal gate leakage versus V_{GS} at a V_{DS}

= 5 V for the 1.43 and $2.73 \cdot 10^{13}$ cm^{-2} doped samples. The gate leakage is much higher in the $2.73 \cdot 10^{13}$ cm^{-2} transistor than the lower doped HEMT. Further, the rate of increase in gate leakage with respect to V_{GS} is significantly higher in the highly doped sample as well. The combination of the higher vertical voltage drop and higher conduction current leads to a greater degree of gate dielectric degradation for the same V_{DS} relative to the lower doped samples. This degradation makes the gate dielectric leakier, and a positive feedback loop between the gate leakage and dielectric degradation occurs until the gate leakage is responsible for the entirety of the 1 mA/mm drain current boundary condition. This process happens before significant degradation of the semiconductor/dielectric interface occurs, preventing the device from catastrophically failing. Because the "softer" breakdown of the higher doped samples occurs at a V_{DS} less than where the semiconductor/dielectric interface fails at, it can be said that the $V_{DS,BR}$ of the higher doped samples is premature. Thickening the gate dielectric would act to reduce the gate leakage and increase the breakdown voltage in these higher doped samples. Once the gate dielectric reaches a thickness such that the breakdown mechanism stops being vertical and starts becoming horizontal, the breakdown will be limited by the degradation at the semiconductor/dielectric interface just like in the lower doped samples. The lateral E-Field in the higher doped samples is larger due to the higher 2DEG density, so the $V_{DS,BR}$ of transistors with higher doping would still be lower than that seen in the lower doped transistor. However, the discrepancy in $V_{DS,BR}$ will be much smaller, closer to the 1.5x difference suggested by Fig. 2.22, rather than the 5x change that actually happened in the samples.

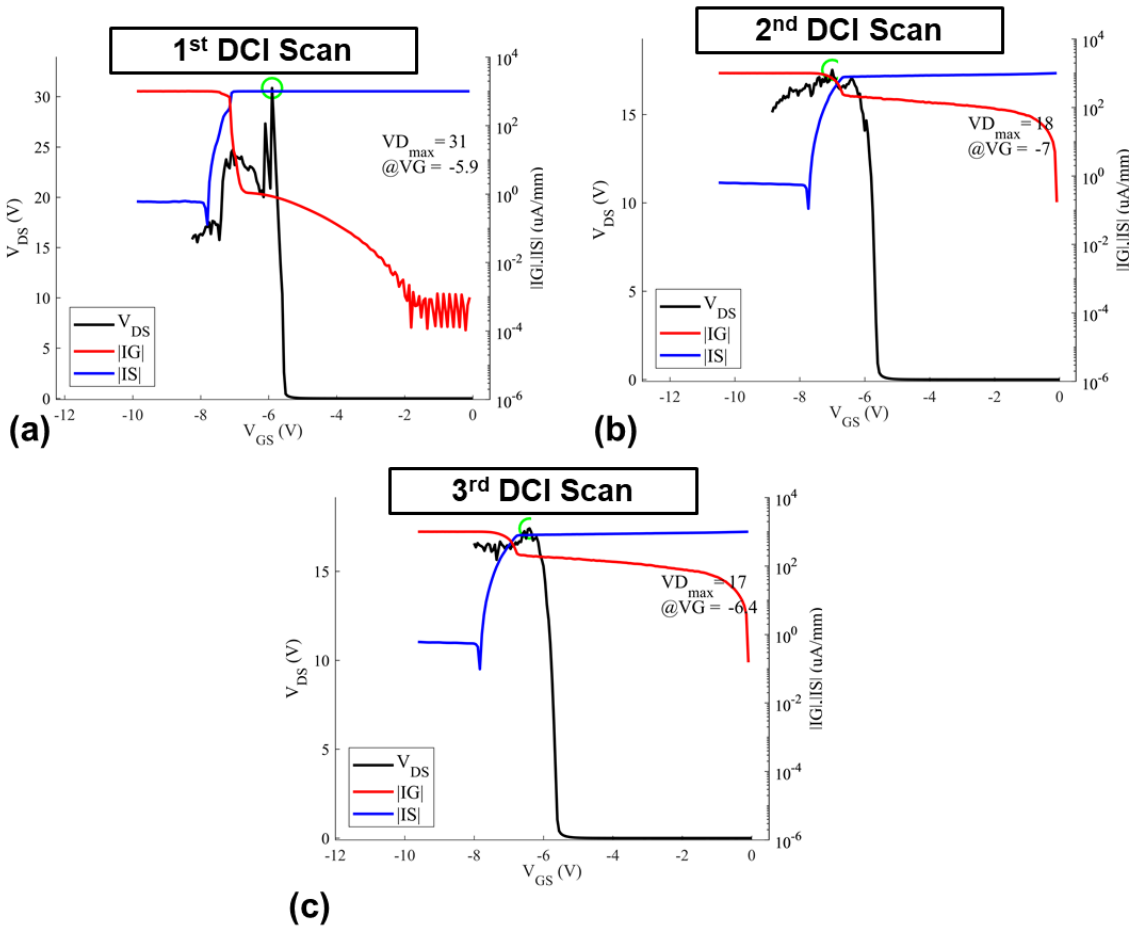


Fig. 2.26: DCI scans taken multiple times on the same transistor on the highest doped sample (2DEG density equal to $1.56 \cdot 10^{13}$ cm^{-2}). Device dimensions are L_G = 0.7 µm, L_{GS} = 0.7 µm, L_{GD} = 2.7 µm, and a W_G = 2 x 75 µm.

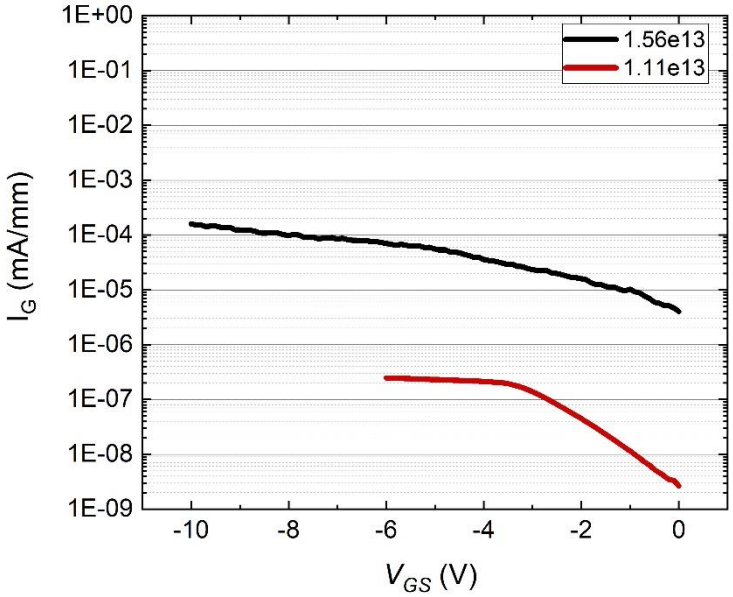


Fig. 2.27: Three-terminal gate leakage vs. V_{GS} at a V_{DS} = 5 V for the 1.11 and 1.56·10^{13} cm^{-2} samples.

Chapter 2.3.5 – Dispersion:

To investigate DC-to-RF dispersion, devices with slant field plates and regrown contacts were also fabricated on these 4 samples (Fig. 2.19 (b)). The fabrication procedure is similar to that for the devices with no field plates, but includes additional steps at the latter end of the process. Prior to gate/field plate metal deposition, a thin ALD Al_2O_3 etch stop layer is deposited, followed by the 120 nm PECVD SiN passivation layer. A double-layer photoresist (PR) layer is spun on, baked, lithographically exposed, and then developed. After development, the TOP photoresist has a significant overhang inside the PR gap relative to the bottom PR layer [35] (Fig. 2.28). This double layer resist combination is used as an etch mask for the subsequent CF4/O2 etch of the PECVD SiN. The ALD Al_2O_3 acts as an etch stop. The overhang profile of the resist makes it such that the etch rate in the central gap is significantly higher than underneath the overhang. However, with a high enough chamber pressure (20 mTorr used here [35]), the PECVD SiN underneath the top PR overhang will

also etch as well. This double-layer resist + etch combination results in a trench with a very shallow (~22 degrees from the horizontal) sloped sidewall. The procedure was adopted from Yuvaraj *et al* [35]. After the etch, the remaining ALD Al_2O_3 is removed in a TMAH-based developer wet etch. The gate + FP lithography comes next, followed by the gate + slant field plate + 200nm lateral field plate metal deposition. At this point, probe pads have already been deposited, and a probe pad lithography + etch is used to remove the PECVD SiN covering the probe pad metal. This concludes the fabrication process.

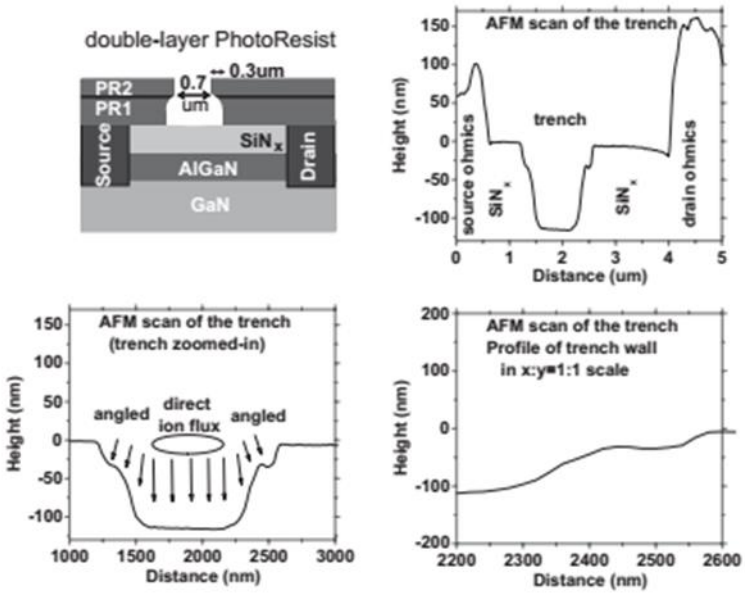


Fig. 2.28: Double layer photoresist used and an AFM scan of the etched trench in the PECVD SiN taken from Yuvaraj Dora's dissertation [35].

This slant field plate process helps reduce surface state induced dispersion in two ways. First, by putting the passivation layer down prior to the gate metal, one ensures that the SiN in the channel/access regions of the device is deposited on a planar surface. This ensures a better and more stable coverage of the HEMT surface than if the gate was deposited first. That is, the passivation quality/coverage at the corners of the gate might be poor when the gate is deposited prior to the passivation like in all the devices discussed in the previous sections of this chapter (Fig. 2.29). Further, the slant field plate reduces the electric field peak

at the corner of the gate, and helps ameliorate any very high electric fields that may result from a very sharp gate corner. Both of these characteristics act to reduce surface state related DC-to-RF dispersion. The drawback of this gate-connected slant field plate structure is the higher C_{gd} and C_{gs} it introduces. As shown in equations (2.1) and (2.2), these higher capacitances can significantly degrade the high frequency performance of the device. This degradation in small-signal RF performance is illustrated in Table 2.6 which compares the small signal RF performance for devices with nominally equivalent dimensions with and without the slant field plate fabricated on the same sample.

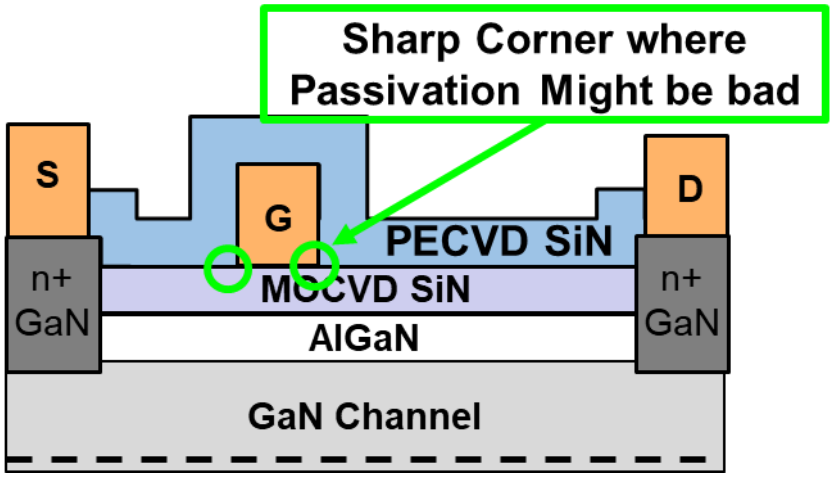


Fig. 2.29: Cross-sectional diagram of the gate 1st N-Polar MISHEMT structure used in section 2.2 and here in section 2.3. Because we use a metal lift-off process for the gate, sharp edges are left at the gate metal/MOCVD SiN corner which may be difficult for the PECVD SiN to fully cover.

Sample		Gate 1st		Slant Field Plate	
Doping Density (10^{13} cm^{-2})	In Dot Hall Ns (10^{13} cm^{-2})	Peak f_T (GHz)	Peak f_{max} (GHz)	Peak f_T (GHz)	Peak f_{max} (GHz)
1.26	**1.09**	15.1	52.8	13.5	34.7
1.43	**1.11**	17	54.75	14	38.5
1.96	**1.19**	NA	NA	13.7	36.8
2.73	**1.56**	18	48.2	14	35

Table 2.6: RF small-signal performance for transistors fabricated with a gate 1st process and those with a gate-last (slant field plate) process on the same sample. Both device styles contain a L_G = 0.7 µm, L_{GS} = 0.7 µm, L_{GD} = 1.7 µm, and a W_G = 2 x 75 µm. The gate length of the slant field plate is defined at the base of the recessed trench.

A dual pulsed IV system from Teledyne Scientific was used as the primary measurement tool to characterize the dispersion in these devices. A simplified circuit schematic and cartoon depiction of how the tool works is given in Fig. 2.30. Because this tool contains 2 pulse generators, the transistor's quiescent gate-source (V_{DSQ}) and drain-source (V_{DSQ}) biases can be held constant while pulsing to all other locations on the IV plane. Thus, the HEMT's I_{DS} vs. V_{DS} characteristics can be traced out for virtually any V_{GSQ} and V_{DSQ} combination. Dispersion can be calculated relative to the IV characteristics exhibited by the device when pulsed from a (V_{GSQ}, V_{DSQ}) = (0, 0) quiescent bias. This is better than most PIV systems where the pulsed IV data is compared to the DC IV data. Because the currents and voltages in the III-N systems are higher than most other semiconductor families, significant self-heating is seen from DC I_{DS} vs. V_{DS} traces, and this can mask the DC-to-RF dispersion. Further, the tool can be used to monitor knee walkout and/or current collapse with respect to increasing V_{DSQ}, V_{GSQ}, or both.

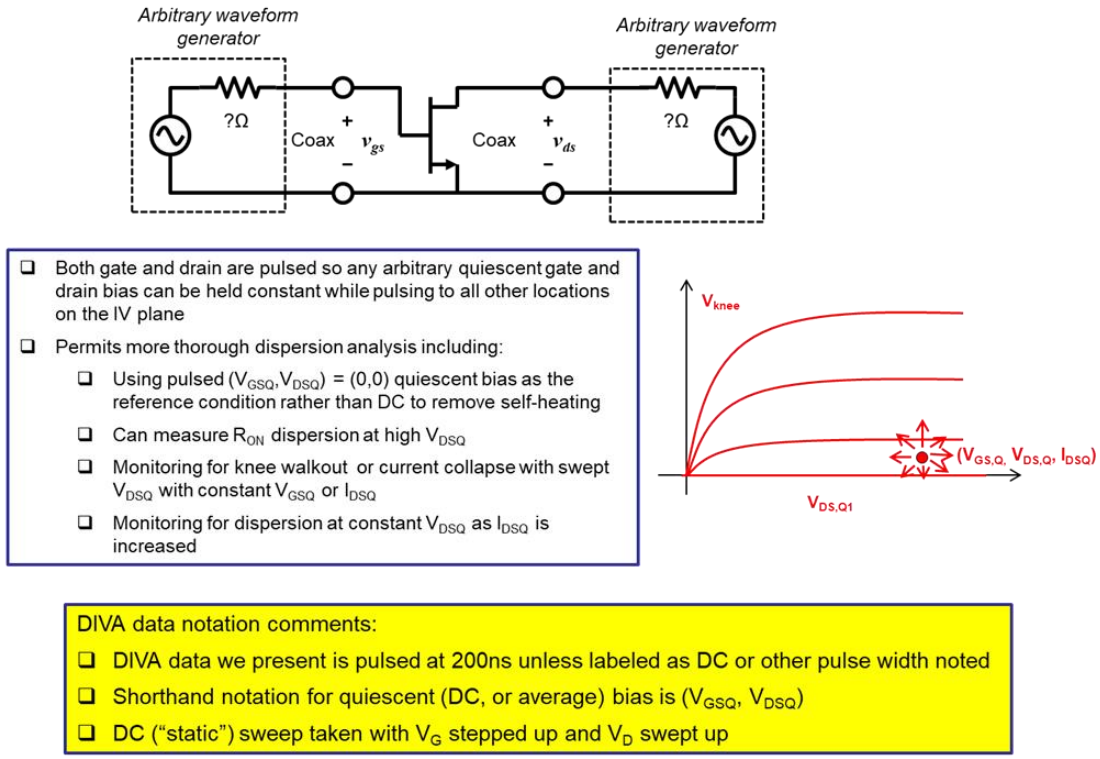


Fig. 2.30: Circuit schematic and description of the Diva dual PIV system used in this section [36].

Using this system, PIV measurements were made on the SLFP samples for the 1.43 and $2.76 \cdot 10^{13}$ cm^{-2} samples. Fig. 2.31 shows the results. At similar quiescent biases, the $2.76 \cdot 10^{13}$ cm^{-2} sample exhibited less dispersion than the $1.43 \cdot 10^{13}$ cm^{-2} sample. As both devices are passivated and field plated, dispersion due to surface states should be minimal. Therefore, this discrepancy may be due to the electron quasi-Fermi level being closer to the hole trap in the lower doped sample. At higher quiescent drain biases, the electron quasi-Fermi level may interact with the hole trap and lead to a larger amount of DC-to-RF dispersion in the lower doped transistor. Alternatively, the mere fact that the lower doped sample has lower 2DEG density may be the reason for the higher dispersion relative to the highest doped sample. For instance, if the electron traps at the surface or in the buffer trap a total of $0.3 \cdot 10^{13}$ electrons in the channel before becoming filled, this would lead to an approximate drop of $\approx 0.3 \cdot 10^{13}$ electrons in the conducting 2DEG channel for both samples.

As discussed earlier in this section, the 2DEG mobility has been shown to be high and approximately constant for a 2DEG density from 0.95 to $1.56 \cdot 10^{13}$ cm^{-2}. If $0.3 \cdot 10^{13}$ electrons are removed from the channel 2DEG in the highest doped sample, its 2DEG concentration still falls within this range. However, if $0.3 \cdot 10^{13}$ cm^{-2} are subtracted from the lower doped sample, its 2DEG concentration will fall outside this range. At lower 2DEG concentrations, columbic scattering from interfacial dipoles can increase significantly [29]. Therefore, even if the traps remove the same number of electrons from both the lower and highest doped samples, the dispersion seen in the lower doped sample may be higher, as the 2DEG mobility may also be adversely impacted by this process.

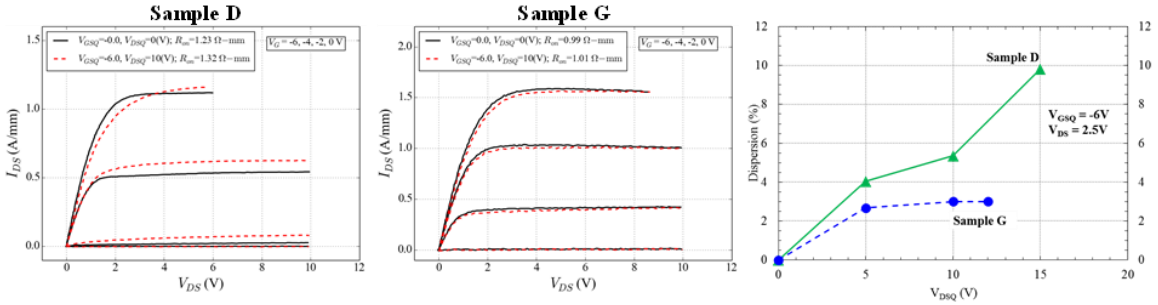


Fig. 2.31: (a) and (b) PIV data from a slant field plate device on the samples with a 2DEG density of 1.11 and $1.56 \cdot 10^{13}$ cm^{-2}, respectively. Measurements taken at a similar epitaxial location with a pulse width of 200 ns and a period of 0.5 ms. (c) Comparison of dispersion performance between these two samples, taken at V_{GS} = 0 V, V_{DS} = 2.5 V. Device dimensions are L_G = 0.7 µm, L_{GS} = 0.7 µm, L_{GD} = 1.7 µm, and W_G = 2 x 75 µm. The gate length of the slant field plate device is defined at the base of the recessed trench.

It should be stated that whatever the physical mechanism responsible for the lower DC-to-RF dispersion seen in the highest doped sample, the dispersion in both samples is relatively low.

Chapter 2.3.6 – Doping Series Conclusion:

To summarize, higher back-barrier doping leads to higher channel 2DEG density without a significant drop in electron mobility (at least for the range explored in this work). This leads to higher saturation current density and (slightly) lower Ron as shown in Table 2.5.

Virtually no effect on small signal RF performance was seen in this doping range. However, the higher back-barrier doping/2DEG density leads to a very significant drop in breakdown voltage for the gate cap stack used in this experiment (5x between the lowest and highest doped samples explored here). The breakdown voltage can be improved by thickening the gate dielectric. This will lead to a worse aspect ratio (gate length divided by gate-2DEG separation), which will decrease C_{gs} relative to the other capacitances in the transistor and lead to a decrease in the high frequency performance of the MISHEMT. Further, the higher doping/2DEG density reduces DC-to-RF dispersion somewhat relative to the lower doped samples. The difference is not very significant though. The N-Polar HEMT designer must take into account all these factors when choosing what back-barrier doping to user in their transistor. For this specific graded + Si doped AlGaN back-barrier in conjunction with the 20 nm GaN channel thickness and AlGaN/MSiN gate cap stack, the $1.43 \cdot 10^{13}$ cm^{-2} doping appears to be optimal. No drop in $V_{DS,BR}$ is seen in this sample relative to the lowest doped sample, however, the electron quasi-Fermi level is slightly further away from the "hole trap", so the dispersion performance should be better than or equal to the dispersion performance seen in the lowest doped sample.

Ch. 2.4 – Alloyed vs. Regrown Contacts

In this section a series of samples whose transistors feature either alloyed or regrown n+ GaN contacts is explored. The device performance between devices with these types of contacts is compared. It is found that N-Polar MISHEMTs with regrown n+ GaN contacts outperform the alloyed contact transistors by an amount greater than the discrepancy in contact resistance suggests. The section begins by covering the experimental details and

fabrication procedure of the alloyed and regrown contact samples. The next subsection provides a general overview of the differences between devices featuring alloyed contacts and those with regrown contacts. The final subsections look specifically at the static, small-signal RF, and dynamic performance of one sample where one quarter of the wafer is all alloyed contact devices and the other quarter is all regrown contact devices.

Chapter 2.4.1 – Experimental Details + Fabrication Procedure:

The same set of samples grown for the doping series experiments of section 2.3 are used in the experiments of this section. Each sample was grown on 2" full thickness miscut sapphire wafers and then cleaved into quarters before fabrication of either the regrown or alloyed contact transistors. Table 2.4 lists every sample grown in this back-barrier doping series as well as which samples had transistors with regrown n+ GaN and/or alloyed contacts fabricated on them.

The fabrication procedure for samples with regrown n+ GaN contacts for transistors with both slant field plate and no slant field plate is detailed in sections 2.2 and 2.3. The process for fabricating the alloyed contacts is similar, but with a few key differences. First, there is no regrowth of any kind in the alloyed contact samples. As a result, the initial *in situ* $Al_{0.46}Ga_{0.54}N$ + MOCVD SiN gate cap stack that exists at the beginning of the process is the gate cap stack used in the final device. Secondly, a Ti/Al/Ni/Au (20/100/10/50 nm) ohmic metal stack is deposited directly on top of the MOCVD SiN dielectric. A 820^{o} C anneal is used to alloy contacts through the 5 nm MOCVD SiN dielectric, the top 2.6 nm $Al_{0.46}Ga_{0.54}N$ barrier, and the 20 nm UID GaN channel. The annealing process in combination with the metals used likely consume much of the MOCVD SiN, AlGaN cap, and UID GaN channel, in a similar fashion to what was shown in the cross-sectional TEM image of [37] (Fig. 2.32).

Other Mishra students have found that if the MOCVD SiN dielectric is significantly thicker, the metal does not alloy all the way through, and the contacts end up being non-ohmic [38]. This was not the case for these samples. A plan view optical microscope image of the annealed ohmic contacts from one of the alloyed contact samples in this work is shown in Fig. 2.33. The rest of the process follows in a similar fashion to the fabrication procedure of the regrown contact samples.

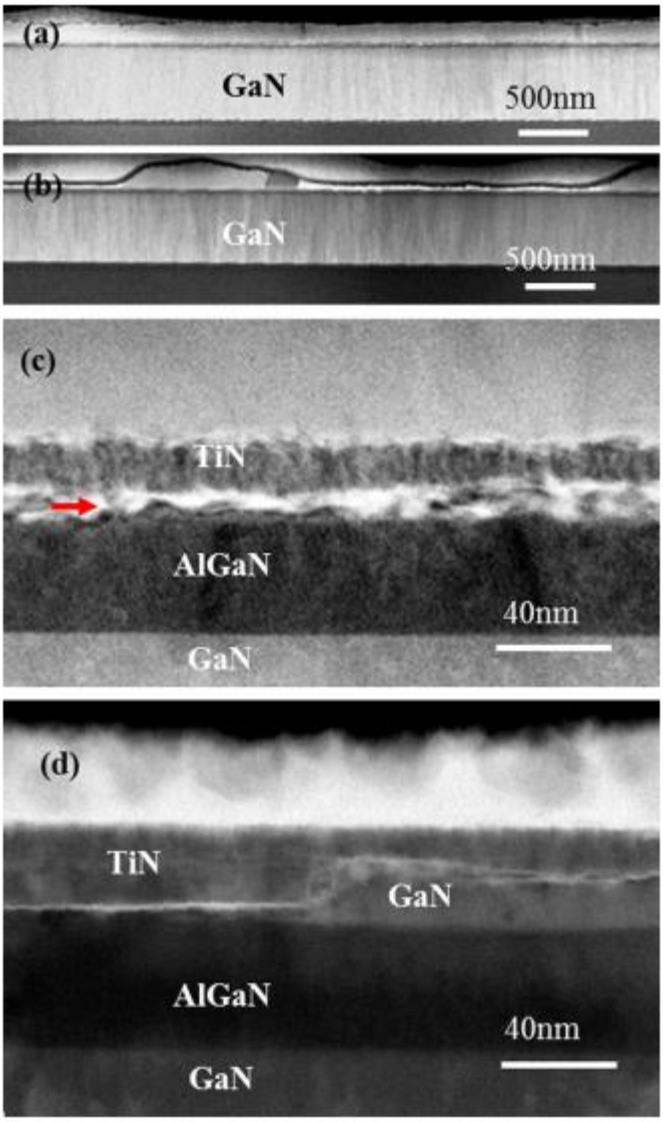


Fig. 2.32: A high-angle annular-dark-field scanning transmission electron microscope image of a Ti/Al/Ni/Au metal stack annealed at 850^{o} C on a N-Polar HEMT sample taken from [37].

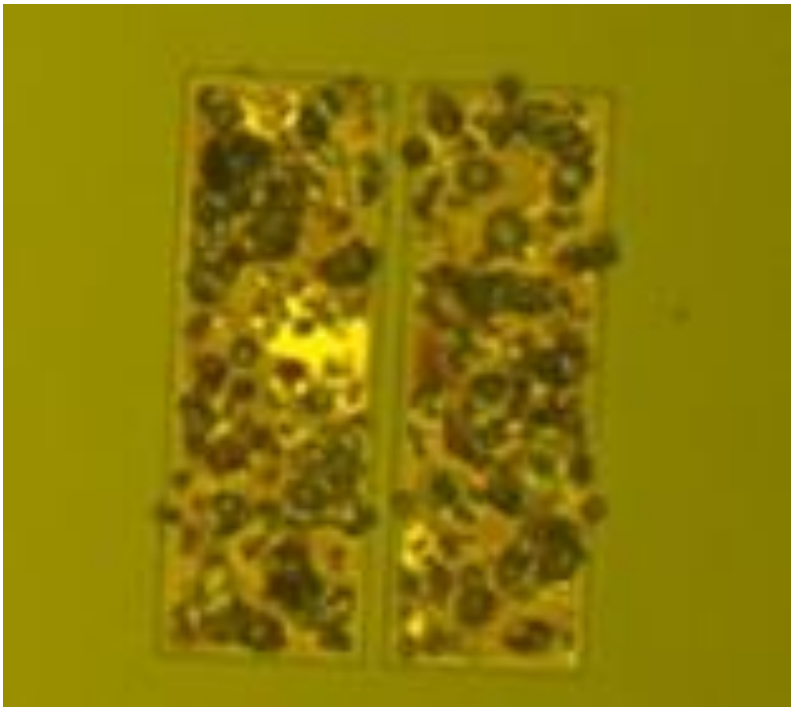


Fig. 3.33: Optical microscope image of a N-Polar MISHEMT annealed ohmic contact.

Chapter 2.4.2 – Alloyed vs. Regrown Contacts – Overview:

Large area gate capacitors (100 μm radius) were used to make capacitance voltage (CV) measurements on both the alloyed and regrown contact samples. The measured ns and V_{th} vs. total back-barrier doping density is shown in Fig. 2.33. In all alloyed contact samples fabricated, the 2DEG concentration measured via CV was significantly lower than that seen in samples with regrown contacts. Further, the threshold voltage of the alloyed contact samples was less negative than in the transistors with regrown contacts as well. This was the general trend across many of the measurements made on these sets of samples. For some reason, devices with annealed contacts behave as if the 2DEG concentration in them was suppressed relative to the ns expected (and measured via In dot Hall) after growth.

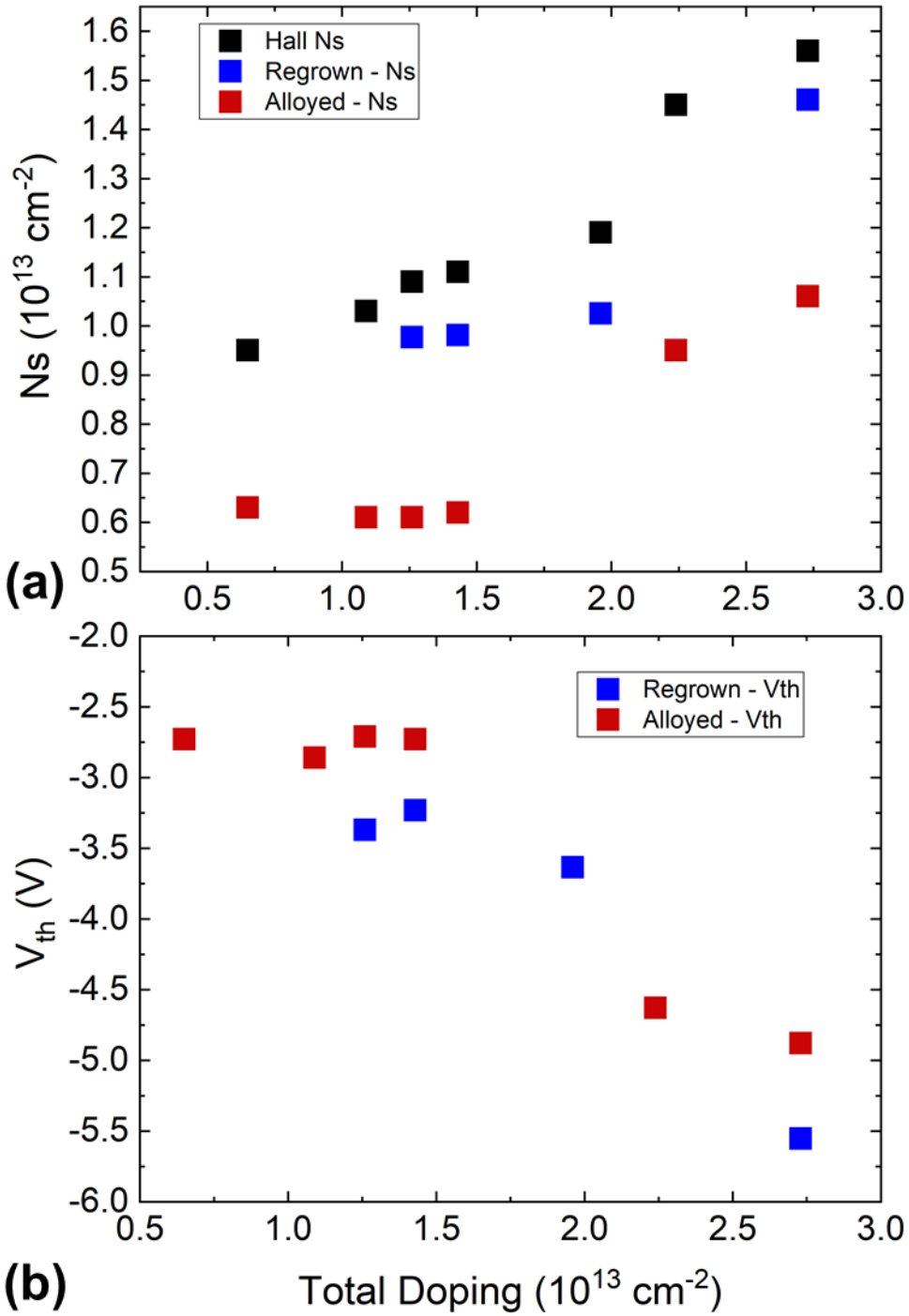


Fig. 2.33: (a) Measured 2DEG density from In dot Hall, CV on devices with alloyed contacts, and CV taken on devices with PAMBE n+ GaN regrown ohmic contacts versus the total Si doping in the HEMT epitaxy. (b) Threshold voltage measured via CV on transistors with both annealed and regrown ohmic contacts versus the total Si-doping.

This “charge suppression” phenomena is also seen in the breakdown performance of the alloyed contacts transistors. DCI measurements were taken on each set of samples with a 1 mA/mm injection current. The breakdown results for the doping series samples with regrown contacts is explained in detail in section 2.3. The highlights of that study are summarized in Table 2.7. In general, the two lowest doped samples featured a channel breakdown event and the breakdowns resulted in catastrophic failure of the devices. The two highest doped samples mostly did not have a channel breakdown event and the breakdowns were not catastrophic in nature. $V_{DS,BR}$ was significantly lower in the higher doped samples than in the lower doped ones. Further, the breakdown voltages of the lower doped samples scaled linearly with increasing L_{GD}, whereas $V_{DS,BR}$ did not in the transistors with higher doping. Section 2.3 explains that the difference in breakdown behavior between the lower and higher doped samples is due to a difference in the physical mechanisms of breakdown. In the lower doped samples, hot electrons from the channel degrade the semiconductor/dielectric interface until catastrophic failure of this interface (and therefore the transistor device) occurs. For the higher doped samples, the more negative V_{th} and higher channel 2DEG creates a significantly higher vertical E-Field across the gate cap stack. For the same voltage biases a much higher gate leakage is seen in these devices relative to the lower doped samples. At a high enough V_{DS} the gate leakage is enough to completely satisfy the 1 mA/mm boundary condition on the drain contact. This occurs before significant degradation of the semiconductor/dielectric interface. The combination of the relatively high conduction current and V_{GD} is enough to degrade the gate dielectric, but not enough to cause catastrophic failure, and multiple measurements can be made on the same device.

Doping Series Breakdown Analysis Summary For Devices with Regrown PAMBE n+ GaN Ohmic Contacts

Sample		Common Occurrences > 50%		
Doping Density (10^{13} cm^{-2})	In Dot Hall Ns (10^{13} cm^{-2})	Channel $V_{DS,BR}$ (Y/N)	Catastrophic Failure (Y/N)	Does $V_{DS,BR}$ scale with L_{GD}
1.26	1.09	Y	Y	Y
1.43	1.11	Y	Y	Y
1.96	1.19	N	N	N
2.73	1.56	N	N	N

Table 2.7: Summary of breakdown analysis performed on devices from this doping series which had regrown ohmic contacts on them from section 2.3

All of the alloyed contact samples, including the highest doped sample (which has a regrown contact analogue) behave in the same fashion to the lower doped samples with regrown contacts. That is, they have a higher breakdown voltage, feature a channel breakdown event, and the devices fail catastrophically after gate breakdown. Fig. 2.35 compares the DCI scans for the highest doped sample with regrown (a) and alloyed (b) contacts separately. The sample with alloyed contacts has a $V_{DS,BR}$ over 3x that of the sample with regrown contacts. Additionally, the transistor with alloyed contacts features a channel breakdown event and fails catastrophically after gate breakdown. 14 different devices from the 2 highest doped samples with alloyed contacts (2.24 and 2.73·10^{13} cm^{-2}) had DCI scans taken on them. All 14 devices featured a channel breakdown and failed catastrophically. Breakdown voltage vs. L_{GD} for the highest doping sample is presented in Fig. 2.35. With alloyed contacts, $V_{DS,BR}$ scales with gate-drain spacing in the same fashion as in the lower doped samples. All of these breakdown characteristics suggest that the physical breakdown is initiated at the semiconductor/dielectric interface, just like in the lower doped samples with

regrown contacts. Further, it illustrates that within the range of back-barrier doping densities explored, breakdown voltage scales with the actual 2DEG density in the channel, not doping.

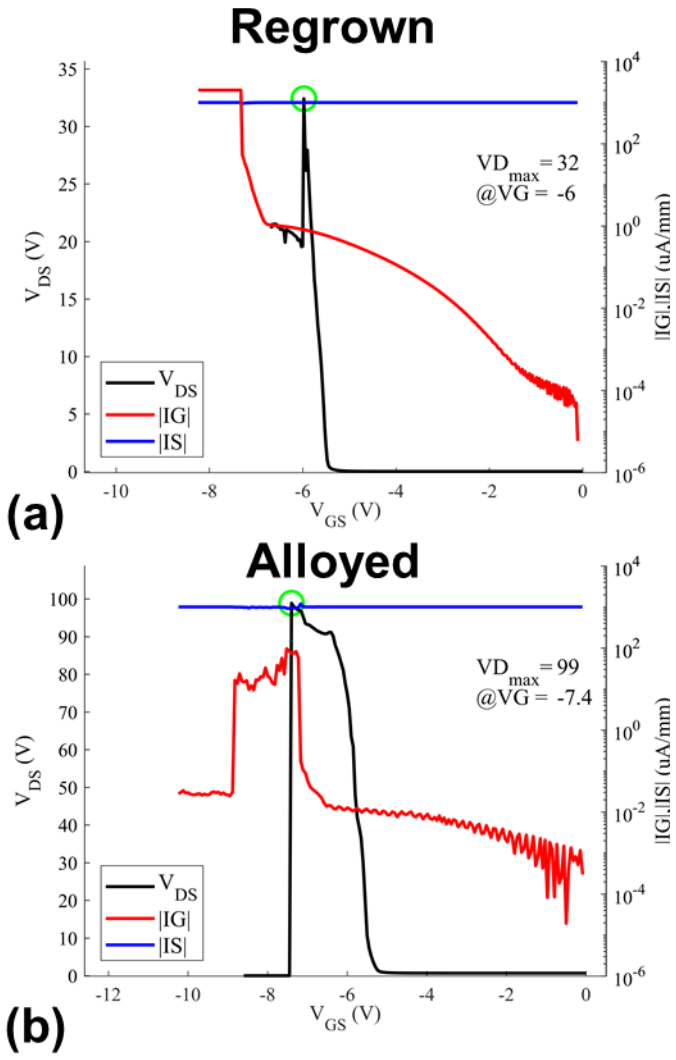


Fig. 2.34: DCI scans for the highest doped sample (total doping of $2.73 \cdot 10^{13}$ cm^{-2}) for devices with PAMBE regrown n+ GaN contacts (a) and alloyed contacts in (b).

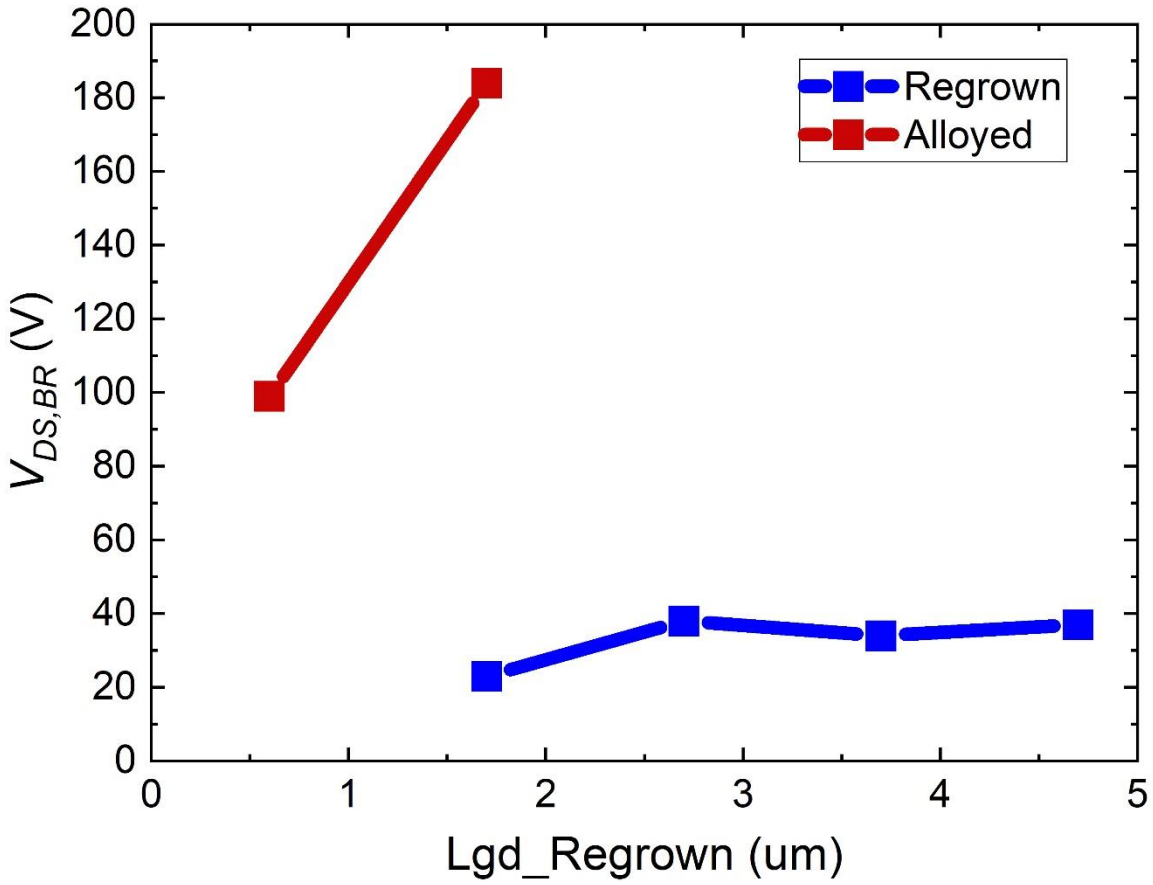


Fig. 2.35: $V_{DS,BR}$ versus L_{GD} for the sample with the highest total doping with both Alloyed and Regrown contacts.

Chapter 2.4.3 – Alloyed vs. Regrown Contacts Comparison of $1.43 \cdot 10^{13}$ cm^{-2}

Sample:

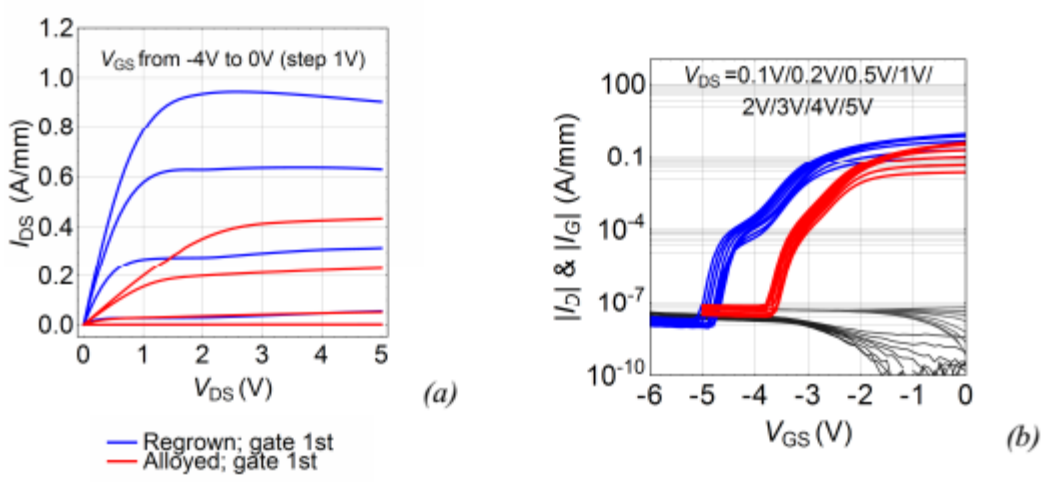
Static Characterization:

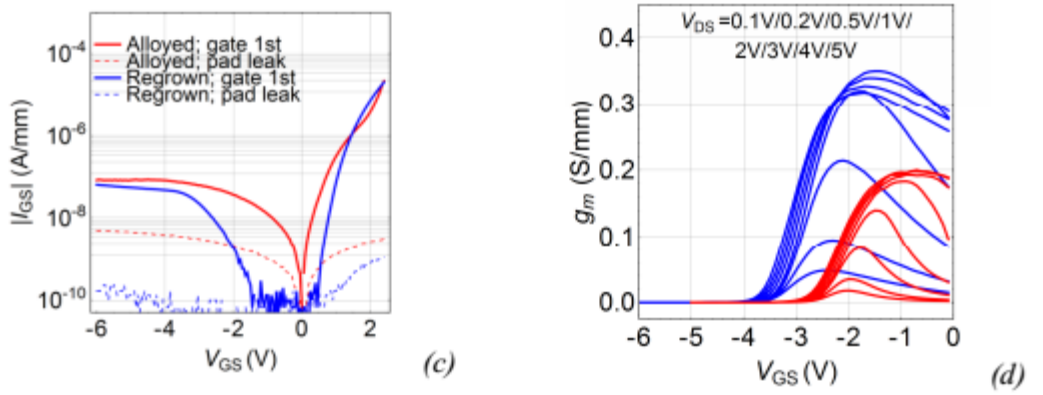
Both the alloyed and regrown contact versions of the $1.43 \cdot 10^{13}$ cm^{-2} samples were sent to the University of Padova for additional characterization. Fig. 2.36 depicts the current-voltage DC characterization of a representative device with alloyed and regrown contacts. Nominal lateral dimensions for this device consisted of an L_G, L_{SD}, and L_{GD} of 0.6, 2.0, and 1 μm, respectively. The samples with regrown contacts had significantly higher saturation current density (0.94 A/mm vs. 0.43 A/mm), improved transconductance peak

(350 S/mm vs. 200 S/mm), lower on-resistance (0.93 Ω·mm vs. 4.82 Ω·mm), and more negative threshold voltage (-3.4 V vs. -2.5 V). TLM's were also measured on both the alloyed and regrown contact $1.43 \cdot 10^{13}$ cm^{-2} samples at UCSB. A sheet resistance of 290 Ω/sqr along with a contact resistance of 0.83 Ω·mm were extracted from the sample with alloyed contacts. A sheet resistances of 250 Ω/sqr and a contact resistance of 0.175 Ω·mm were extracted from the regrown contact sample. The discrepancy in contact resistance and ungated sheet resistance between the two samples is not nearly large enough to account for the differences in static performance. A simple back-of-the-envelope calculation can be made to calculate the approximate Ron for each sample (eq. 2.4.1).

$$R_{on} = 2 \cdot R_C + L_{SD} \cdot R_{SH} \tag{2.4.1}$$

Plugging in the R_C and R_{SH} values for the transistor with regrown contacts in Fig. 2.36 yields an R_{on} = 0.85 Ω·mm. This is almost exactly equal to the actual 0.93 Ω·mm measured on that sample. Using the R_C and R_{SH} values for the alloyed contact sample of Fig. 2.36 gives an Ron = 2.235 Ω·mm. This is less than ½ the value of the 4.82 Ω·mm actually measured on the alloyed contact transistor. Gated TLM was also measured on this alloyed contact sample. An Rsh of 505 Ω/sqr was measured underneath the gate. This is significantly higher than the sheet resistance extracted for the ungated TLM measurements, but this R_{SH} is also too low to explain the discrepancy in performance. An R_{SH} of 1,585 Ω/sqr is required to make up the difference if the R_C and R_{SH} in the access regions are the same as that measured via TLMs.





Alloyed

I_{DSS} @ V_G=0V	433.1	mA/mm
R_{ON} @ V_G=0V	4.821	Ω·mm
$g_{m,max}$	200.	mS/mm
V_{TH} @ 0.1V;1mA/mm	-2.538	V
SS @ 0.1V;1μA/mm	123.1	mV/dec
DIBL (0.1V/5V)	72.55	mV/V
$I_{G,leak}$ @ -5V;5V	-5.5×10^{-8}	A/mm
$I_{D,leak}$ @ -5V;5V	7.1×10^{-8}	A/mm

Regrown

I_{DSS} @ V_G=0V	944.6	mA/mm
R_{ON} @ V_G=0V	0.9304	Ω·mm
$g_{m,max}$	350.	mS/mm
V_{TH} @ 0.1V;1mA/mm	-3.423	V
SS @ 0.1V;1μA/mm	113.6	mV/dec
DIBL (0.1V/5V)	79.86	mV/V
$I_{G,leak}$ @ -6V;5V	-3.7×10^{-8}	A/mm
$I_{D,leak}$ @ -6V;5V	2.3×10^{-8}	A/mm

Fig. 2.36: I_{DS} vs. V_{DS}, I_{DS} vs. V_{GS}, I_{GS} vs. V_{GS}, and gm_{ext} vs. V_{GS} of the sample with a total Si doping of $1.43\cdot10^{13}$ cm^{-2} are given in (a), (b), (c), and (d), respectively. Blue lines are data taken on regrown contact devices while the red line come from transistors with Alloyed Contacts.

Fig. 2.36 (c) also compares 3-termianl gate leakage current between the two samples. Leakage was less than 100 nA/mm at a (V_{GS}, V_{DS}) = (- 5 V, 5V) in both samples. However, higher leakages were seen in devices with alloyed contacts, especially in the low voltage

regime ($V_{GS} > V_{th}$). This may suggest that the quality of the *ex situ* gate dielectric of the regrown samples is superior to the *in situ* gate dielectric of the alloyed contact samples. The *in situ* dielectric is exposed to a 820 C anneal in a N_2 ambient that the regrown MOCVD SiN does not see. The growth temperature of MOCVD SiN is significantly higher than this (~ 1050C), but that is performed in an NH_3 environment.

Extrinsic gate-source pad leakage was also measured by on buffer insulation test structures, and compared with the intrinsic gate-source current. Alloyed-contact devices show higher pad leakages than the regrown contact devices.

Chapter 2.4.4 – Double Pulsed I-V Characterization:

Large signal Dynamic performance of the two samples was investigated with a double-pulsed I-V system at the University of Padova as well. General information about dual PIV systems is given in section 2.3 of this thesis. Information regarding the particular system in the University of Padova is given in [39]. Transistor from both the alloyed and regrown contact samples were subjected to gate-lag and drain-lag measurements.

Fig. 2.37 shows gate-lag I_{DS}-V_{DS}, I_{DS}-V_{GS}, and gm-V_G characteristics of representative devices with alloyed and regrown contacts. The quiescent-bias began at a (V_{GSQ}, V_{DSQ}) = (0 V, 0 V), and was stepped down in 1 V increments until the V_{GSQ} was roughly 2.5 V below the threshold voltage of the device. Pulse width and pulse period are 1 μs and 1 ms in these measurements, respectively.

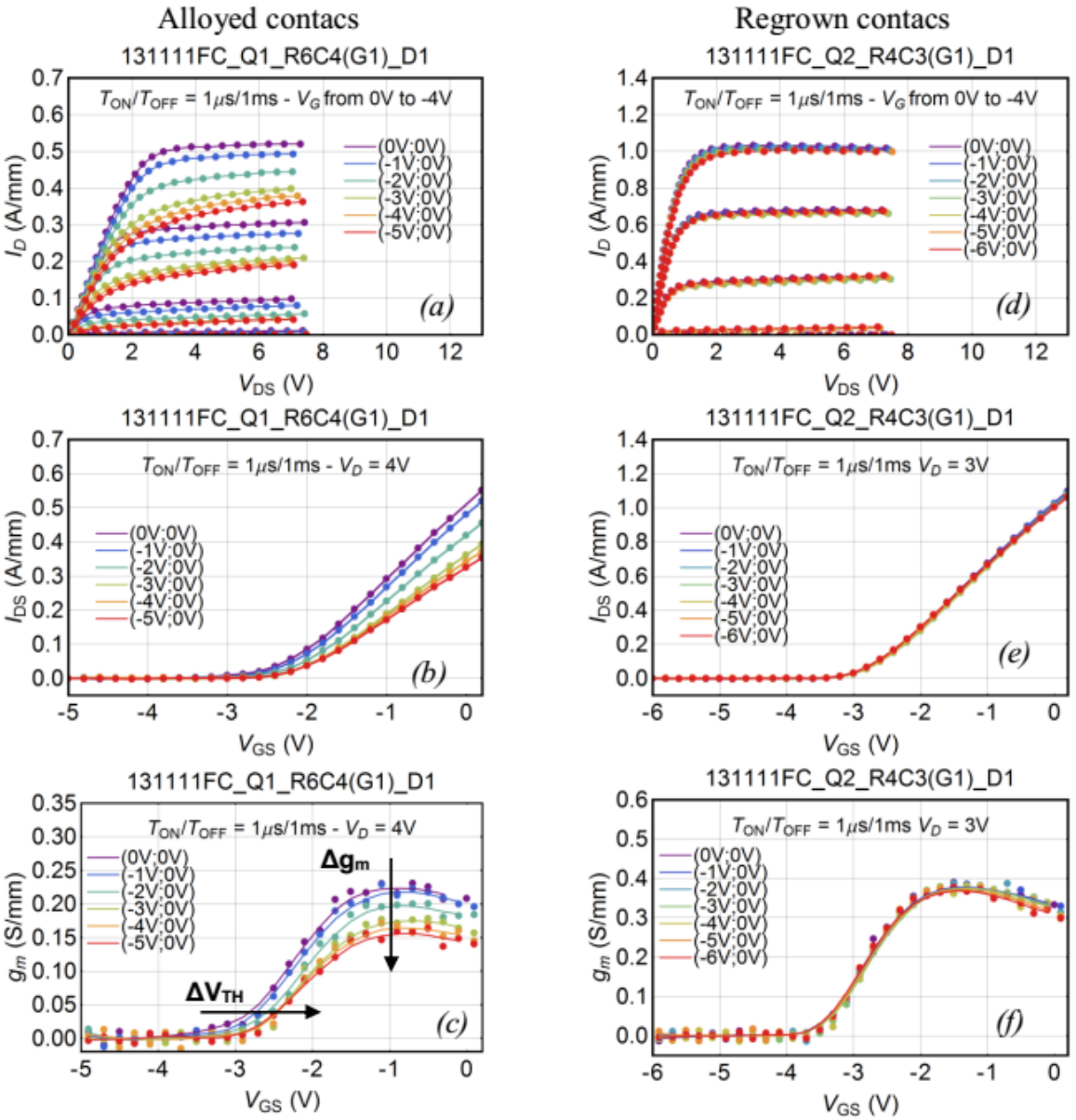


Fig. 2.37: Dual PIV measurements taken on the sample with a total Si doping of $1.43 \cdot 10^{13}$ cm^{-2} where the device is exposed to a reverse gate quiescent bias (but a 0 V drain quiescent bias). Plots on the left-hand side depict measurements taken on transistors with Regrown PAMBE contacts, while plots on the right show data from the devices with alloyed contacts. (a) and (d) show the dual PIV I_{DS} vs. V_{DS} trace, (b) and (e) show the dual PIV I_{DS} vs. V_{GS} trace, and (c) and (f) show the extrinsic *gm* vs. V_{GS} trace.

A very large degradation in saturation current (32% at (V_{GSQ}, V_{DSQ}) = (-5 V, 0 V), Fig. 2.37 (a). Double-pulsed I_{DS}-V_{GS} measurements reveal that this degradation is caused by the combination of a positive V_{th} shift (250 mV at (V_{GSQ}, V_{DSQ}) = (-5 V, 0 V)) and a degradation of the transconductance (27% at (V_{GSQ}, V_{DSQ}) = (-5 V, 0 V)).

Transistor with regrown contacts, showed negligible collapse of dynamic performance under the same set of conditions. At a (V_{GSQ}, V_{DSQ}) = (-6 V, 0 V), there was only a 2.5% reduction in saturation current, 10 mV of V_{th} shift, and a 6% degradation in transconductance.

Double pulsed IV measurements were also carried out from an off-state quiescent bias point to investigate the influence of the drain voltage on dynamic performance (Fig. 2.38). V_{GSQ} was set to 2.5 V below the threshold voltage of the individual device, and V_{DSQ} was varied from 0 V all the way up to 20 V in 5 V increments. At the highest V_{DSQ}, competition between 2 distinct mechanisms is observed. On one hand, the transconductance of the device drops, but on the other hand, the V_{th} shifts to more negative values. In transistors with regrown contacts, the combination of these two effects lead to current dispersion in the knee region, where the transconductance and on-resistance of the device dominates performance. Current anti-dispersion occurs in the saturation region though, where the device performance is dominated by the threshold voltage. A potential hypothesis to explain this current "anti-dispersion" phenomena is depicted in Fig. 2.4.13, and explained in this body of text. When the device is biased in the off-state, the electron quasi Fermi level drops below the "hole trap" (deep donor) located at the top GaN/$Al_{0.46}Ga_{0.54}N$ interface. Energetically, this hole trap is approximately 60 meV above the valence band [40]. This acts to ionize the deep donor levels to a positively charged state. When the device is pulsed to the on-state, the deep donors do not have sufficient time to capture electrons, and stay positively charged. This pushes the V_{th} of the device more negative during the pulse, and a higher saturation current than expected results.

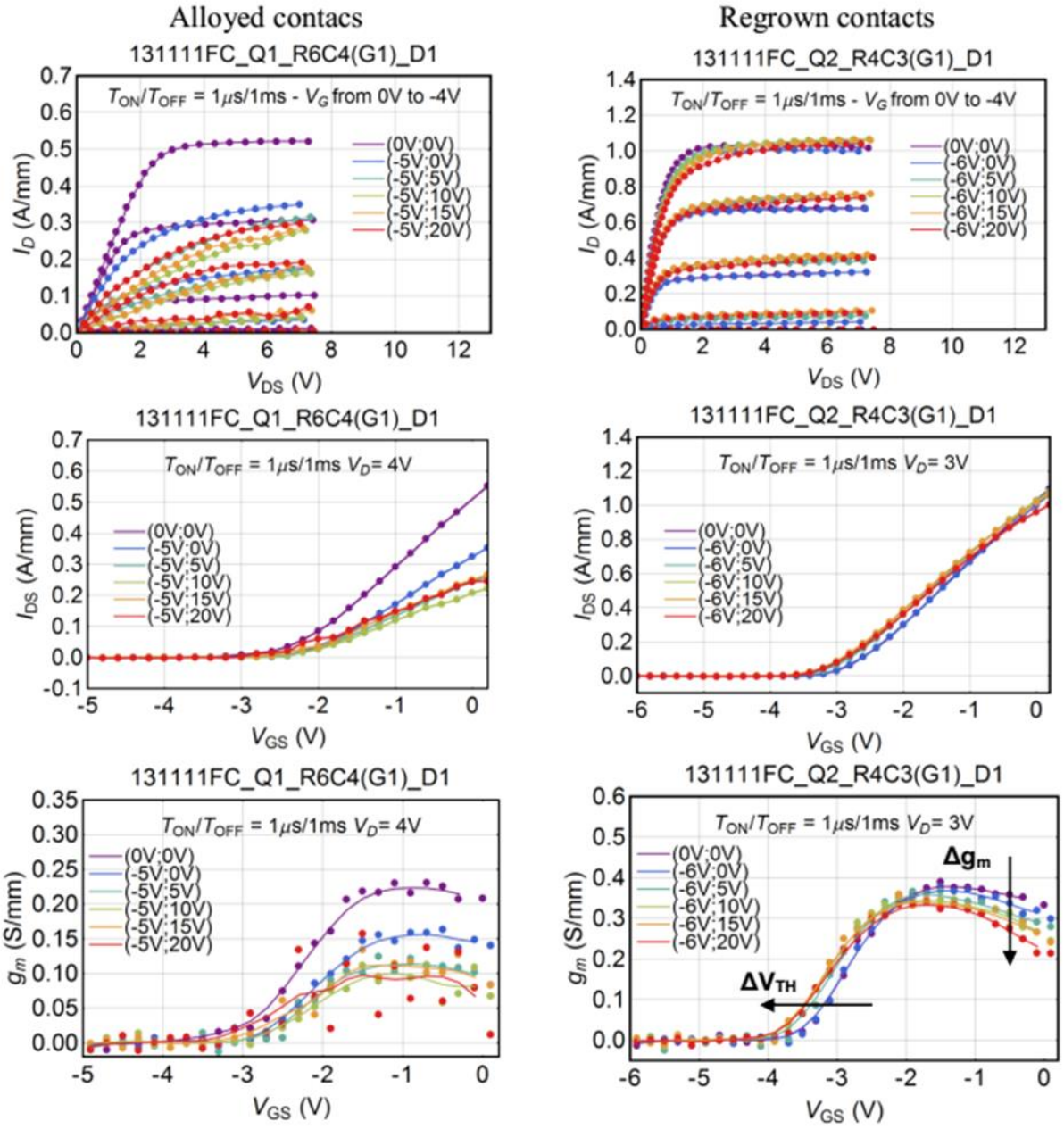


Fig. 2.38: Dual PIV measurements taken on the sample with a total Si doping of $1.43 \cdot 10^{13}$ cm^{-2} where the device is exposed to an off-state quiescent bias (both a nonzero gate and drain quiescent bias voltage). Plots on the left-hand side depict measurements taken on transistors with Regrown PAMBE contacts, while plots on the right show data from the devices with alloyed contacts. (a) and (d) show the dual PIV I_{DS} vs. V_{DS} trace, (b) and (e) show the dual PIV I_{DS} vs. V_{GS} trace, and (c) and (f) show the extrinsic *gm* vs. V_{GS} trace.

It is quite likely that similar competing mechanisms exist in the sample with alloyed contacts. However, the much more dispersive nature of the transistors on that sample likely masks this.

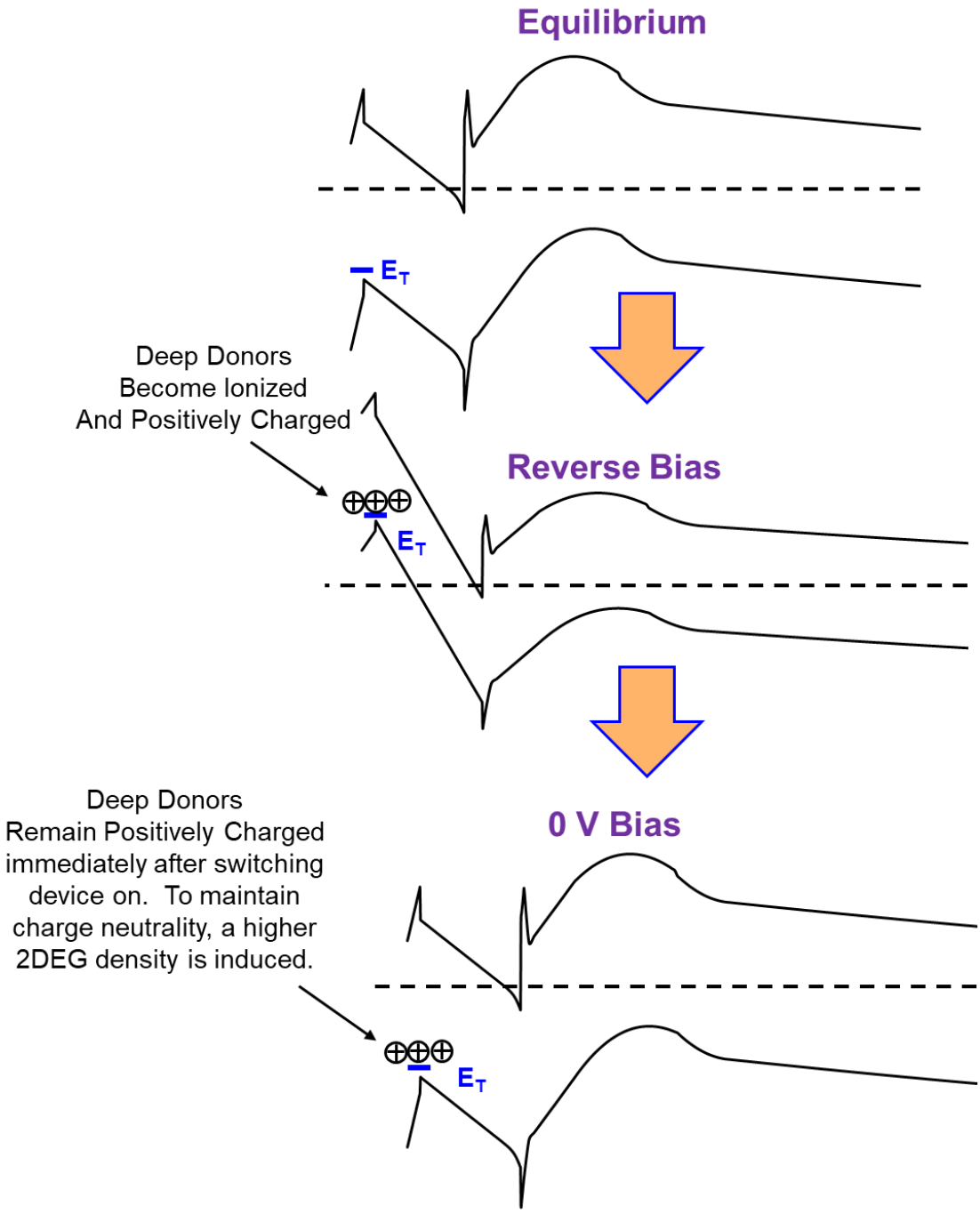


Fig 2.39: Band diagram as the N-Polar transistor is switched from a V_{GS} = 0 V, to a reverse bias, and back to 0 V.

A summary of the double pulsed IV results on both samples is depicted in Fig. 2.40.

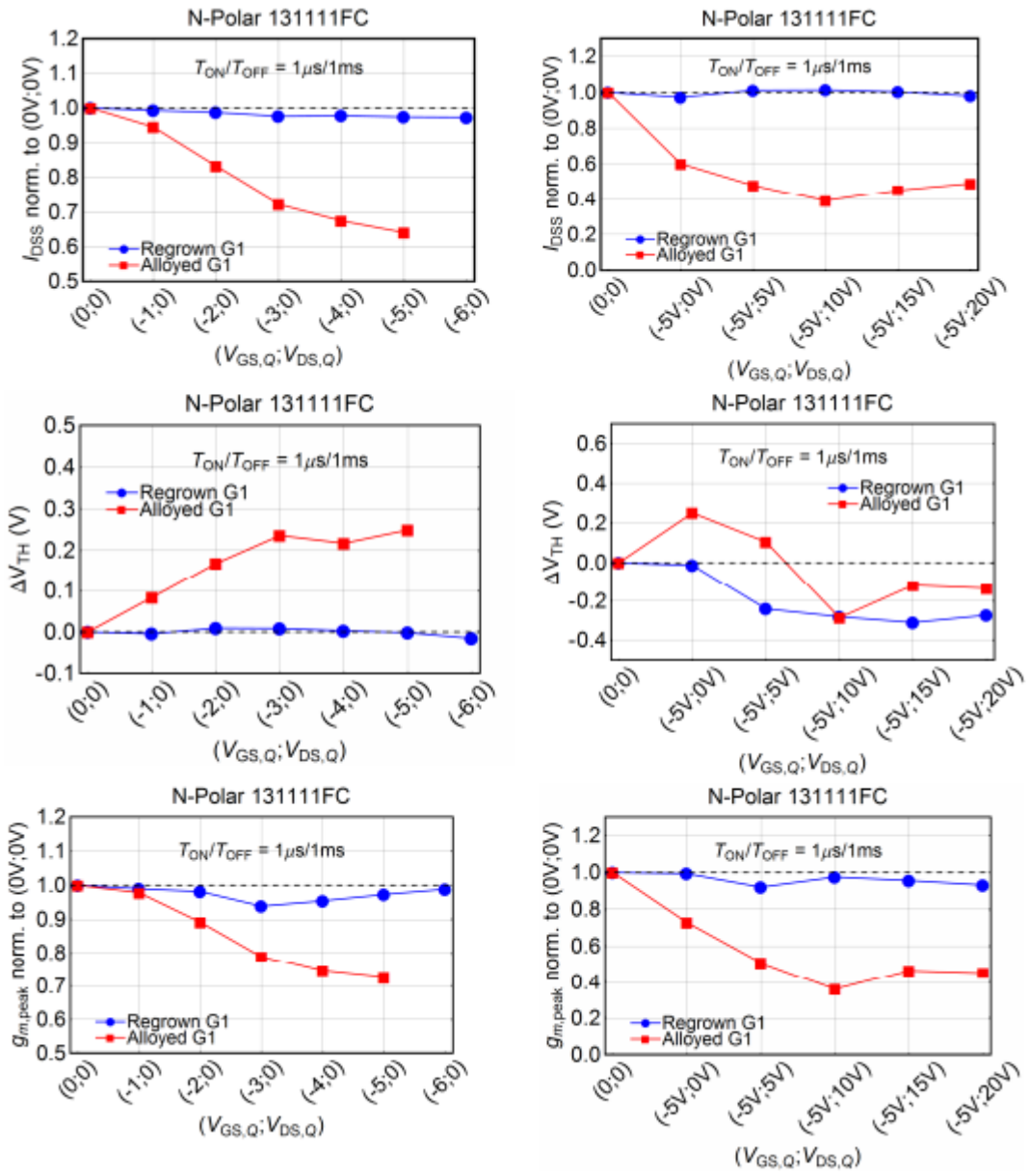


Fig. 2.40: Change in saturation current density, threshold voltage, and extrinsic transconductance with respect to quiescent bias in the double pulsed *IV* setup. Left-hand side depicts these parameters with respect to a non-zero gate quiescent bias. Right-hand side depicts these parameters with respect to both a non-zero gate and drain quiescent bias voltage.

Chapter 2.4.5 – Small Signal RF:

Bias-dependent S-parameter measurements up to 67 GHz were made with a Keysight N5227A PNA calibrated by the LRRM method at the probe tips using an impedance standard substrate [17]. Small-signal characteristics (after pad de-embedding) for transistors from each

sample biased for peak f_{max} is given in Fig. 2.41 (a) and (b). Performance is actually quite similar between the 2 samples in this case. A peak de-embedded f_{max} of 50.0 GHz vs. 54.8 GHz is recorded for the alloyed and regrown contact devices, respectively. Plots with devices biased for peak f_T are given in Fig. 2.41 (c) and (d). Here, a peak de-embedded f_T of 15.5 GHz vs. 15.2 GHz is measured in the alloyed and regrown contact transistors, respectively. This is somewhat similar to the sheet resistance extracted from TLM measurements in the alloyed and regrown contact samples. Although there was a difference between the two (alloyed = 290 Ω/sqr, regrown = 250 Ω/sqr), the discrepancy was much smaller than in all other measurements made on the two samples. Un-gated TLM's are somewhat similar to the small-signal RF measurements made here in that they feature relatively low voltage biases, and therefore, relatively low E-Fields. It is possible that that the "charge suppression" phenomena seen throughout the static measurements in earlier sections is related to the higher E-Fields that occur in those measurements. This will be discussed in a little more detail in the conclusion.

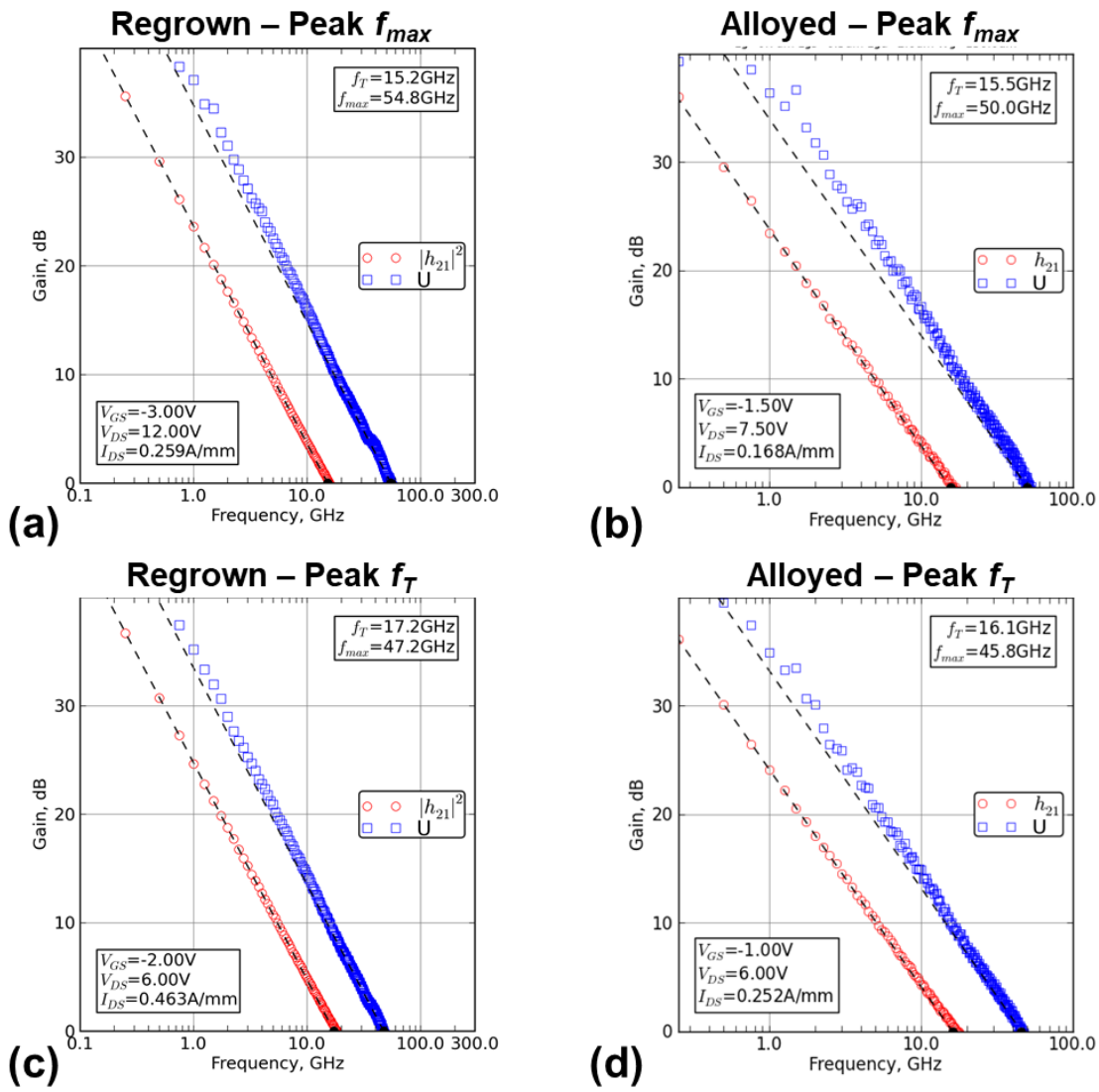


Fig. 2.41: Small-signal RF performance for the Regrown Contact samples (left-hand side) and Alloyed Contact samples (Right-hand side). The transistor devices measured here each had a L_G = 0.7 µm, L_{GS} = 0.7 µm, L_{GD} = 1.7 µm, and a W_G = 2 x 75 µm.

Chapter 2.4.6 – Conclusion:

In this section, the static, small-signal RF, and large signal dynamic performance of samples with both alloyed and PAMBE regrown n+ GaN contacts were investigated. The major takeaway from this study is that N-Polar MISHEMTs employing alloyed contacts with this particular metal stack and annealing conditions are unsuitable for high performance RF

transistor devices. These findings have also been reproduced by other students in the Mishra group. The lower contact resistances provided by the PAMBE n+ GaN regrown contacts implies that if the N-Polar transistor designer desires the highest possible performance, they should go with a similar PAMBE regrown contact configuration. However, a much steeper drop in performance than what contact resistance alone would predict is seen in the alloyed contact samples. As such, the N-Polar designer would have to sacrifice a great deal in terms of performance for the efficiency and cost savings enabled by utilizing annealed contacts.

The greater large signal dispersion seen in the alloyed contact sample could possibly be due to the differences in gate dielectric between the alloyed and regrown contact sample. In the regrown contact sample, the initial gate dielectric is stripped from the sample using HF/HNO_3, and a new MOCVD SiN gate dielectric is deposited *ex situ* in the MOCVD reactor. In the alloyed contact sample, the gate dielectric is deposited *in situ* during the initial growth. This gate dielectric is used throughout all fabrication steps of the transistor, including the 820^{O} C anneal in a N_2 ambient. It is possible that this anneal degrades the quality of the MOCVD SiN, and that this is what leads to greater large signal dispersion in the sample.

It is unlikely that the "charge suppression" phenomena seen in the alloyed contact samples could be due to the fact that the *in situ* gate dielectric is exposed to a 820^{o} C anneal. A third quarter from one of lower doped samples was also processed by a Mishra group colleague (Onur Koksaldi). In this sample, a low power CF_4/O_2 etch followed by a low power Cl_2 etch was used to remove the MOCVD SiN gate dielectric and $Al_{0.46}Ga_{0.54}N$ cap, respectively. Ti/Au contacts were then deposited on top of the UID GaN channel without use of any anneal. The rest of the fabrication process was identical to earlier. The contacts were not ohmic, however, they were not so resistive as to prevent CV measurements from being

made. Fig. 2.42 shows CV characteristics of the sample with both annealed and non-annealed contacts. The characteristics are nearly identical. This suggests that the charge suppression phenomena is related more to the inability of the contacts to supply charge to the 2DEG at higher E-Fields. Further studies will look to specifically identify the root cause for this phenomena. However, the focus of this thesis is to achieve the highest performance N-Polar MISHEMT at W-Band frequencies. As such, further exploration of the alloyed contacts lies outside the scope of this work.

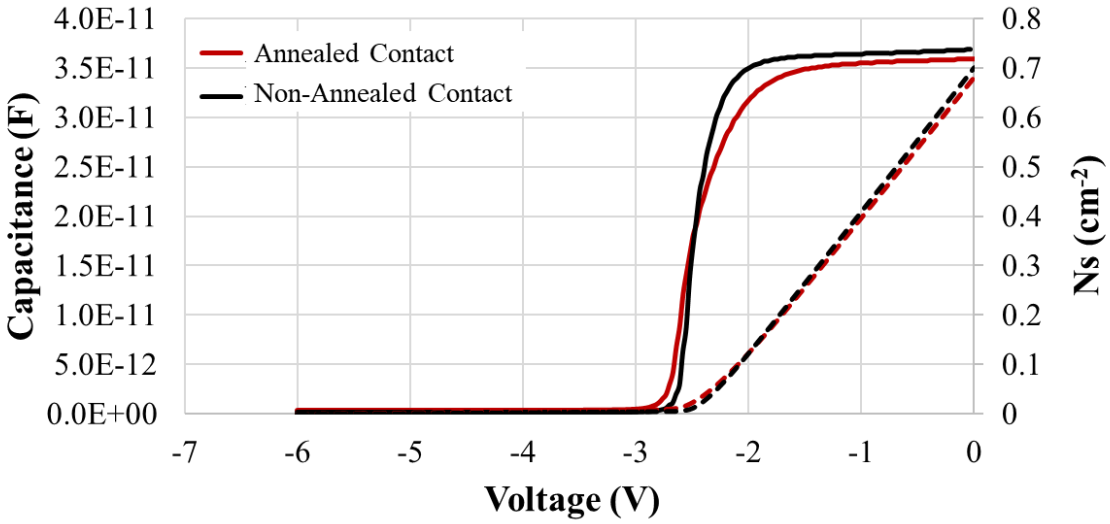


Fig. 2.42: CV trace for a sample with annealed contacts and with non-annealed contacts.

Ch. 2.5 – Planar N-Polar MISHEMT Optimization Summary:

In this chapter of the thesis, several experiments have been carried out to map out the design space for the planar portion of the NPDR device structure. The gate cap stack of the N-Polar MISHEMT was first investigated. It is found that high gate leakage can cause premature breakdown if the gate dielectric is too thin for the given channel 2DEG density. Making the gate dielectric thicker improves breakdown voltage until the point at which the breakdown is limited by degradation of the semiconductor/dielectric interface from hot

electrons in the channel. Placing a thin AlGaN cap on top of the UID GaN channel can help prevent hot electrons from degrading the top semiconductor/dielectric interface, and therefore improve the ultimate breakdown of the device. Finally, it is found that using highly Si-doped III-N regrown contacts is imperative for optimal high frequency large signal performance.

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Chapter 3 – Intro to the N-Polar Deep Recess (NPDR) MISHEMT

Chapter 3.1 – Introduction + Dispersion Explanation and Traditional Solutions:

Transistors for RF amplification purposes should be capable of producing high large signal gain, high efficiencies, and high output RF powers at the frequency range of interest. Achieving all three simultaneously at W-Band (75-110 GHz) has been a struggle in the III-N material system. This is largely due to surface state related DC-to-RF dispersion. DC-to-RF dispersion is the phenomena where the device's large signal RF power performance is significantly worse than that predicted from DC and small-signal RF measurements. This phenomenon is illustrated in Fig. 3.1. In a conventional planar unpassivated HEMT, surface states in the access regions form a "virtual gate" in series with the actual gate electrode [1]. When the gate electrode is held at pinch-off the 2DEG underneath the metallic gate is depleted entirely. When this occurs, the surface states charge up negatively and the virtual gate takes on the same potential relative to the channel as the metal gate electrode. Because the pinch-off voltage underneath the gate electrode and in the access regions are the same, the 2DEG in the access region is also pinched off at this point. When a positive ΔV_{GS} ($-\Delta V_{GD}$) is applied to turn the device on, the 2DEG underneath the gate responds immediately. However, at higher frequencies, the slow-moving surface states cannot respond fast enough, and the 2DEG in the access region remains depleted, causing large additional extrinsic resistances to appear. On the source-side, this additional **extrinsic** source resistance increases the extrinsic voltage drop across the source, in turn reducing the intrinsic gate-source voltage bias. This reduces the high frequency extrinsic transconductance of the device and results in a lower RF current

density for a given V_{GS} voltage bias (Fig. 3.2). This is often referred to as "current collapse" or source-side dispersion. On the drain-side, the additional extrinsic resistance increases the extrinsic voltage drop across the drain and reduces the intrinsic drain-source voltage bias. This results in an increase of the RF knee voltage (Fig. 3.3) and is commonly referred to as "knee-walkout" or drain-side dispersion. Both the lower RF current and higher RF knee-voltage act to diminish the RF large signal power below what one would expect from the DC performance of the transistor (eq. 3.1).

$$P_{RF_{out}} = \frac{(2 \cdot V_{DD} - V_{knee}) * I_{D_{SS}}}{8} \tag{3.1}$$

Historically, application of an *ex situ* dielectric passivation layer in conjunction with field plating has effectively reduced dispersion to tolerable levels and enabled high power performance in conventional Ga-Polar transistors [2].

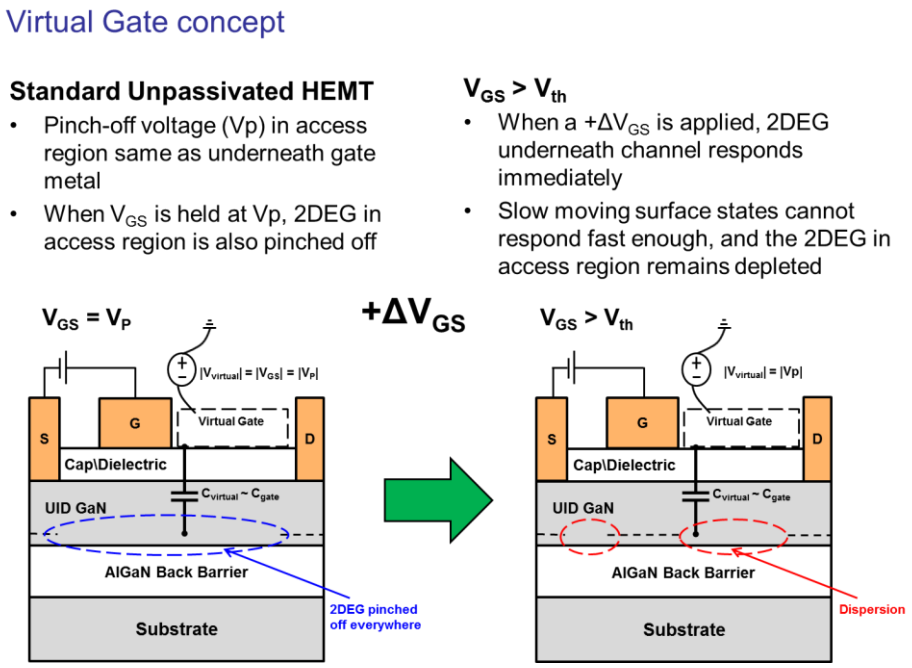

Fig. 3.1: Pictorial representation of surface-state induced dispersion in an unpassivated N-Polar GaN HEMT.

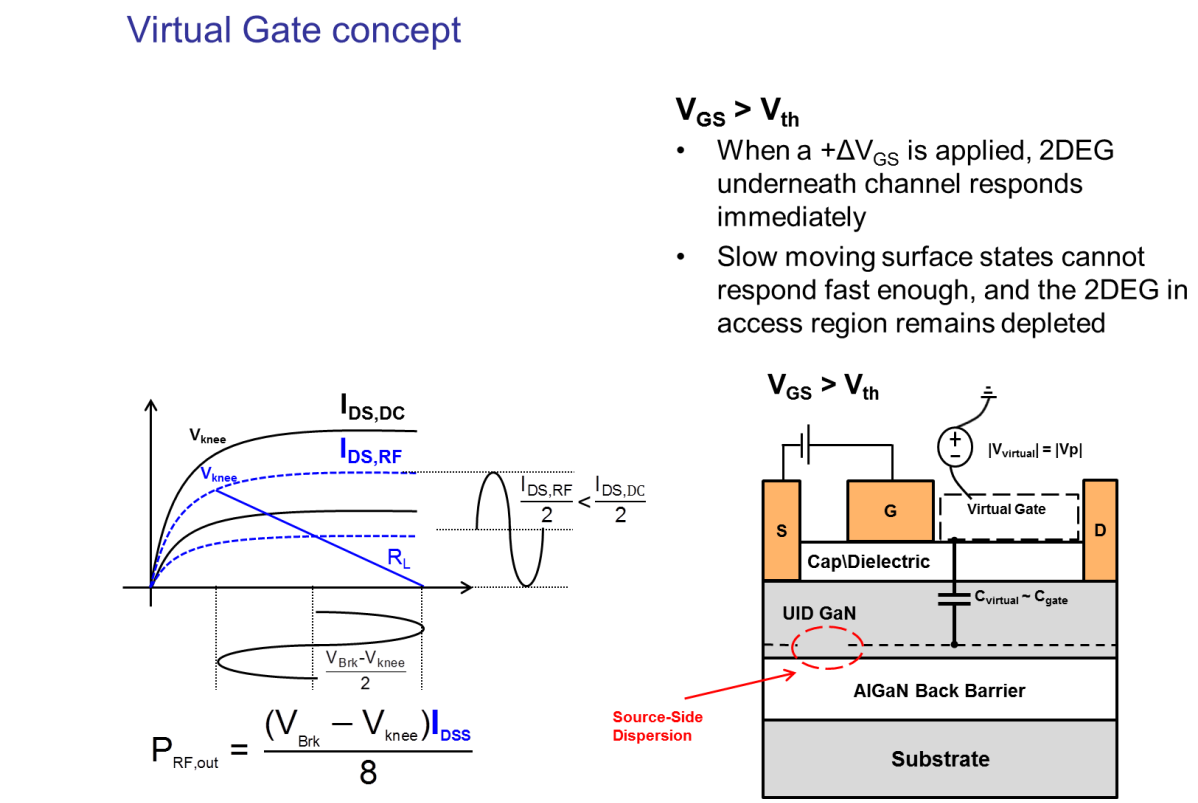

Fig. 3.2: Graphical depiction and explanation of source-side dispersion in a N-Polar GaN HEMT.

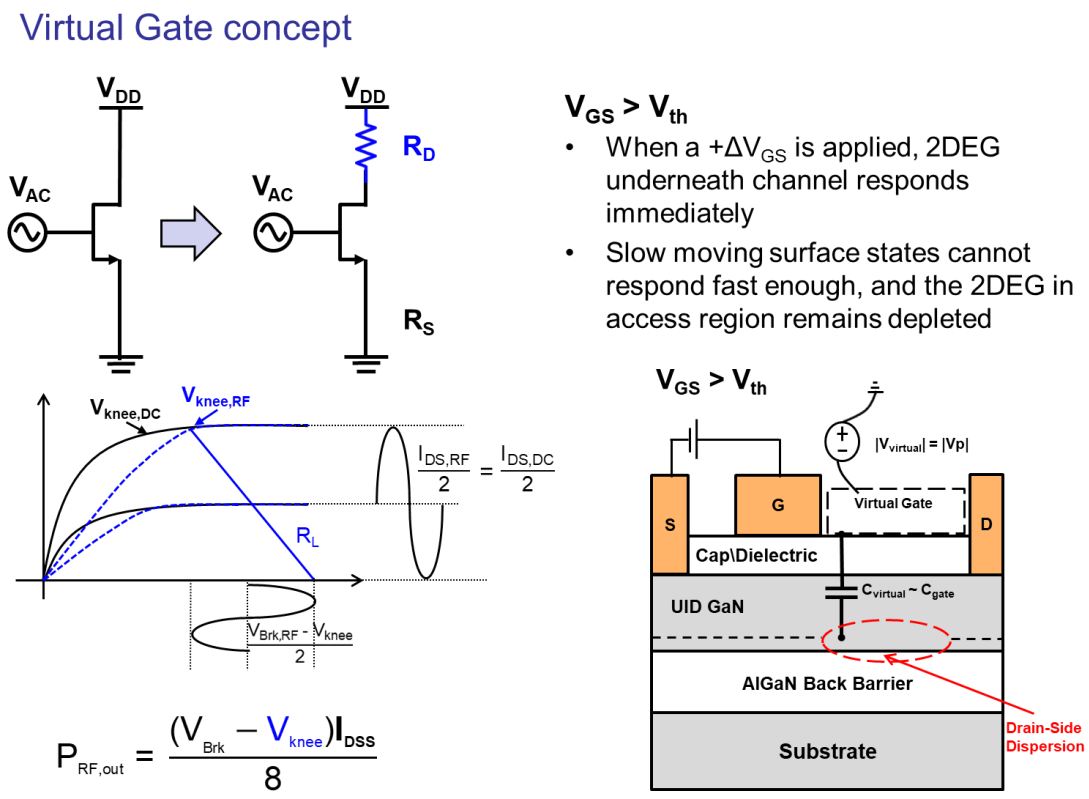

Fig. 3.3: Graphical illustration of drain-side dispersion in a N-Polar GaN HEMT.

Use of an *ex situ* dielectric passivation layer (typically PECVD SiN) decreases dispersion by reducing the number of traps which can actively capture electrons at the III-N/dielectric passivation interface [3]. This interface does not charge up as negatively as in the unpassivated case, and the 2DEG in the access region does not become as depleted under off-state operation. There are trap states at the surface of the dielectric passivation layer which may also create a "virtual gate" in the HEMT as well though. However, the addition of the *ex situ* dielectric layer increases the magnitude of the pinch-off voltage in the access region. Thus, even if the virtual gate at the top of the PECVD SiN takes a very negative potential relative to the access region 2DEG, the surface's ability to deplete the access region 2DEG has significantly weakened. A traditional Ga-Polar HEMT with only a SiN dielectric

passivation layer is shown in Fig. 3.4 (a) and (b). Eastman *et al* [4] were the first to publicly demonstrate the large signal RF power performance improvement through the use of an *ex situ* PECVD SiN dielectric. The addition of a dielectric passivation layer significantly improved the RF power performance in their III-N HEMTs relative to earlier times when no passivation layer was used. However, there was still a large difference between the power performance attained with a dielectric passivation layer only and that predicted based upon the DC values of the transistor. This discrepancy is mainly attributed to hot electron injection into trap states at the III-N/dielectric interface [5]. At high drain voltages, large E-Fields exist in proximity of the drain-edge of the gate electrode (Fig. 3.5). The high E-Field at the gate electrode can inject hot electrons from the gate into trap states at the III-N/dielectric interface. Additionally, large drain-source voltages also accelerate electrons transiting the channel from source to drain near the drain-side edge of the gate. At sufficiently high drain voltages, these hot electrons may have enough energy to be excited to the III-N/dielectric interface trap states as well [6] (Fig. 3.6). All these processes act to increase the drain-side dispersion of the device and degrade RF power performance relative to that which would be predicted from DC measurements from the same device.

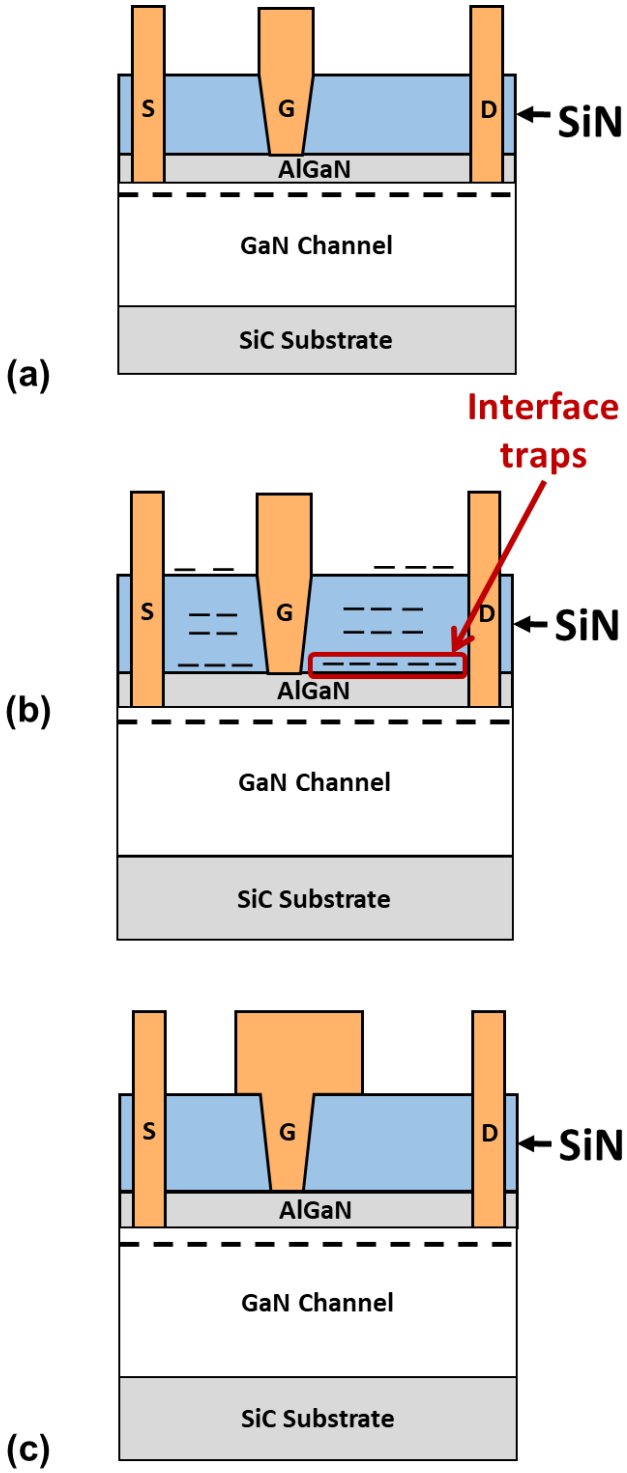

Fig. 3.4: Traditional Ga-Polar schottky gate HEMTs with different passivation schemes. (a) Shows a Ga-Polar HEMT with an *ex situ* PECVD SiN passivation. (b) Points out the location of trap states in this HEMT, specifically the traps that exist at the semiconductor/PECVD SiN interface which are thought to be responsible for the dispersion seen in devices with such a passivation scheme. (c) Depicts a Ga-Polar HEMT with both an *ex situ* PECVD SiN passivation and an additional field plate to help control large signal DC-to-RF dispersion in the device.

A conventional III-N HEMT employing both an *ex situ* dielectric passivation as well as field plating is shown in Fig. 3.4 (c). Properly designed field plating can dramatically reduce the peak E-Field near the drain-edge of the gate (Fig. 3.5, black line). The lower E-Field decreases the number of high energy electrons which can be injected into trap states at both the III-N/dielectric interface as well as the dielectric surface. Further, the lower E-fields may also reduce the ionization rate of trap states, lowering the total number of trap states which can actively capture electrons. The application of field plates in conjunction with a dielectric passivation layer greatly reduces surface state dispersion present in III-N devices, and enables high power and efficiency performance in GaN HEMTs. An RF output power density exceeding 40 W/mm was achieved by Yifeng Wu in 2004 at 4 GHz [2].

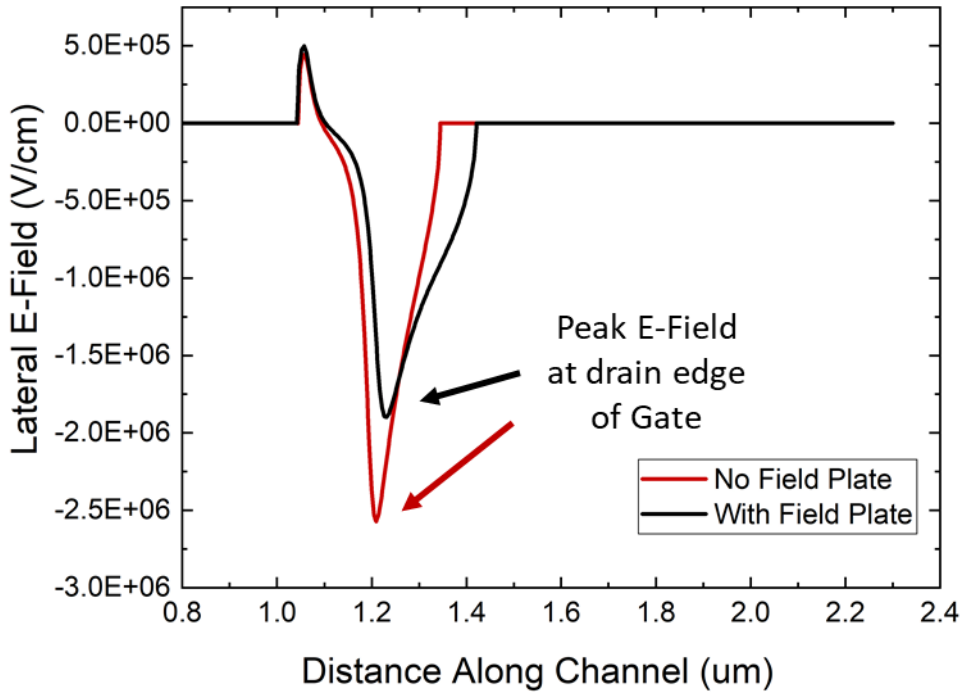

Fig. 3.5: Simulated lateral E-Field at the UID GaN/AlN interface in the channel of a N-Polar HEMT both with no field plate (red line) and with a combination slant + lateral overhang field plate (black line).

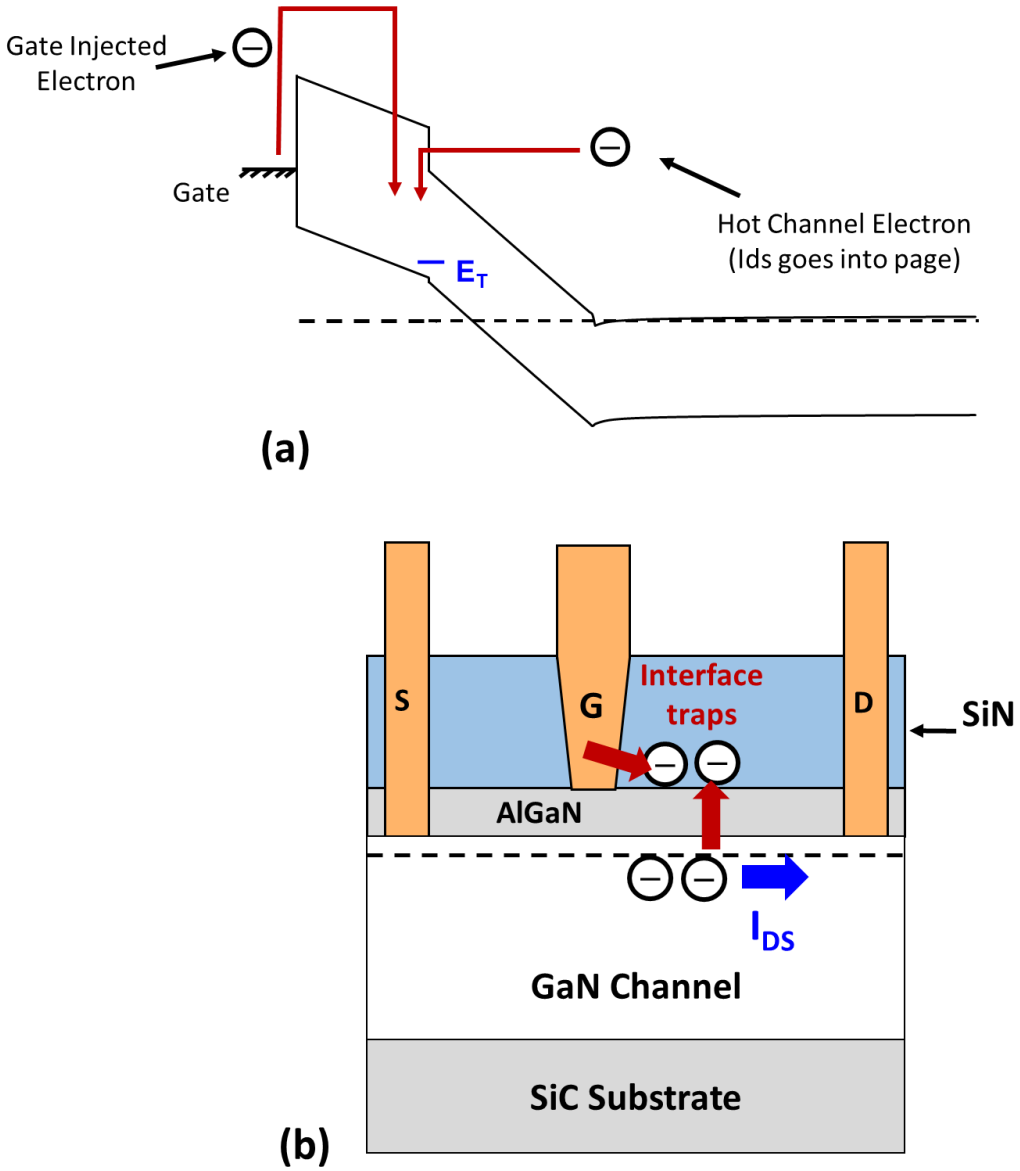

Fig. 3.6: Depiction of hot electrons injected into trap states at the semiconductor/dielectric interface originating from either the gate electrode or from channel. (a) Gives a 1-D band diagram depicting how at a reverse gate-drain bias hot electrons can be injected into the semiconductor/dielectric interface either from the gate or the channel. (b) Cartoon 2-D representation of the same phenomena.

However, the additional extrinsic capacitances these methods introduce severely limit the large signal gain of the device and make it very difficult for the transistor to attain high efficiencies and/or useful gain at W-Band frequencies. Therefore, in order to get acceptable gain at W-Band, most groups do not use any field plating, and rely only on a thin *ex situ* dielectric passivation layer to control dispersion. As a result, they cannot push to higher drain

voltages without experiencing large amounts of dispersion, ultimately limiting their total power performance.

Chapter 3.2 – Deep Recess Solution to Dispersion:

An alternative *in situ* epitaxial method to dispersion control was introduced in 2003 Fig. 3.7 [7]. In this method, an undoped GaN cap is used in place of the traditional *ex situ* passivating dielectric. The whole structure is grown in one shot in the MOCVD reactor, and a gate recess is used in order to obtain reasonable transconductance in the resultant transistor. Shen *et al* also used a recess in the ohmic regions to reduce the spiking distance required for his annealed ohmics and enable lower contact resistances. The way in which dispersion behaves in this GaN "Deep Recess" structure is no different than in any other III-N HEMT without an *ex situ* passivating dielectric. The trap states at the surface of the access region GaN cap form a virtual gate in series with the actual gate. During off-state operation, these surface states become negatively charged and take on the same potential as the metallic gate electrode with respect to the drain access region. However, in a properly designed Deep Recess structure, the relatively thick GaN cap increases the magnitude of the pinch-off voltage in the access region ($V_{P,access}$) with respect to the pinch-off voltage in the gate recessed region ($V_{P,gate}$) (Fig. 3.8). Thus, even if the virtual gate at the top of the UID GaN cap takes a very negative potential relative to the access region 2DEG, the surface's ability to deplete the access region 2DEG has significantly weakened. If $|V_{P,access}| >>$ applied gate-drain bias, very little depletion of the access region 2DEG will occur, and surface state dispersion should be minimal. Equation 3.2 and 3.3 describe $V_{P,gate}$ and $V_{P,access}$ for the Ga-Polar design displayed in Fig. 3.7.

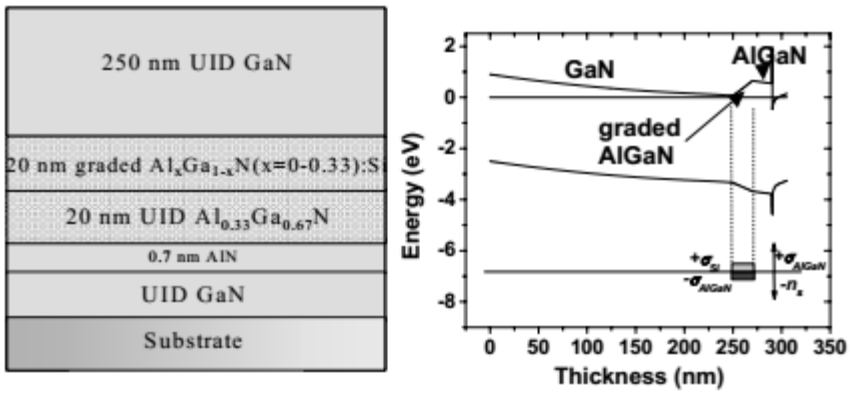

Fig. 3.7: Epitaxial structure and band diagram of the Ga-Polar Deep Recess structure introduced by Shen in [8].

$$V_{P,gate} = \varphi_B - \Delta E_C - \frac{q \cdot \sigma_{AlGaN}}{\varepsilon \cdot \varepsilon_0} \cdot t_{AlGaN} \tag{3.2}$$

$$V_{P,access} = \varphi_B - \frac{q}{\varepsilon \cdot \varepsilon_0} \cdot \left[\sigma_{Si} \cdot \left(t_{cap} + \frac{t_{grade}}{2}\right) - \sigma_{AlGaN} \cdot \left(\frac{t_{grade}}{2} + t_{AlGaN}\right) + \sigma_{AlN} \cdot t_{AlN}\right] \tag{3.3}$$

In equation 3.2, q is the fundamental charge of an electron, ε is the relative permittivity of GaN (assumes AlGaN has ≈ same permittivity as GaN), φ_B is the assumed surface barrier height between the gate metal electrode and the AlGaN top-barrier, ΔE_C is the value of the conduction band discontinuity between the AlGaN top-barrier and the GaN channel, σ_{AlGaN} is the net polarization discontinuity between the AlGaN top-barrier and the GaN channel, t_{AlGaN} is the thickness of the AlGaN top-barrier. In equation 3.3, t_{cap} is the thickness of the UID GaN cap, t_{grade} is the thickness of the graded AlGaN layer, t_{AlGaN} is the thickness of the ungraded portion of the AlGaN layer, t_{AlN} is the thickness of the AlN layer, σ_{Si} is the total Si-doping at the GaN Cap – AlGaN top-barrier interface, φ_B is the assumed surface barrier height of the UID GaN cap, and the rest of the parameters are the same as in equation 3.2.

The description of how the UID GaN Cap controls dispersion is essentially the same as that for an *ex situ* amorphous PECVD SiN dielectric passivation layer. However, the UID GaN cap is grown *in situ* in the MOCVD reactor, with no lattice mismatch relative to the GaN buffer. This results in a pristine interface between the epitaxial passivent and the underlying HEMT structure, with no appreciable amount of interface trap states. Moreover, there should not be any more bulk trap states in the UID GaN cap than what exist in the UID GaN channel of the HEMT either. Because the total number of trap states near the 2DEG is significantly smaller, the access region GaN Cap provides a consistent and robust control of dispersion that more closely approximates what is ideally expected from the electrostatics outlined in this section than what an *ex situ* PECVD SiN passivation does. As mentioned earlier, a significant amount of traps exist at the III-N/PECVD SiN interface [3] in conventional HEMTs. These traps can capture hot electrons when the E-Fields are high, and this leads to a deviation between the expected and realized dispersion performance for HEMTs employing a PECVD SiN passivation alone. This Ga-Polar Deep Recess structure demonstrated impressive large signal power performance at L, S, and X-Band [9-11].

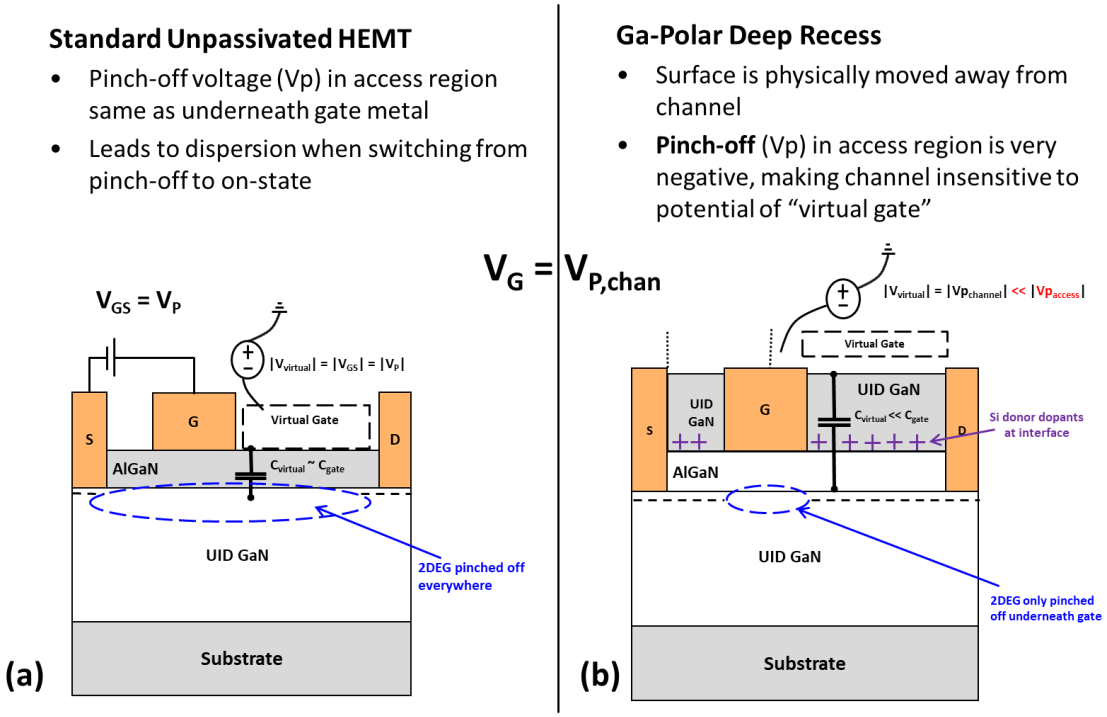

Fig. 3.8: Depiction of how the Ga-Polar Deep Recess structure introduced in [7] is able to mitigate dispersion without the use of any *ex situ* dielectrics or additional field plating. (a) Shows a conventional unpassivated Ga-Polar AlGaN/GaN HEMT which will likely suffer from DC-to-RF dispersion. (b) Shows the Ga-Polar Deep Recess structure introduced in [7] by Shen *et al*.

Chapter 3.2.1 – Potential Limitations to the Ga-Polar Deep Recess Structure:

As mentioned earlier, impressive large signal power performance was demonstrated by Ga-Polar Deep Recess structures at L, S, and X-Band. However, Deep Recess devices made in the Ga-Polar orientation contain significant design tradeoffs that could limit their applicability to higher frequencies. This is due to the orientation of the polarization fields in Ga-Polar HEMTs. If a UID GaN cap is grown directly on top of a standard **un**doped AlGaN/GaN HEMT structure, the electrostatics are such that a progressively thicker GaN caps will deplete the access region 2DEG and the electron density will decrease as shown in equation 4.3 [8].

$$ns = \frac{\sigma_{AlGaN} \cdot t_{AlGaN} - \frac{\varepsilon\varepsilon_0}{q} \cdot \varphi_B}{t_{cap} + t_{AlGaN} + \Delta d} \tag{3.4}$$

Here σ_{AlGaN} is the net polarization charge density at the GaN cap/AlGaN barrier interface, t_{cap} is the thickness of the GaN cap layer, t_{AlGaN} is the thickness of the AlGaN barrier, φ_B is the surface potential at equilibrium, and Δd is the distance between the centroid of the 2DEG and the AlGaN barrier. As the GaN cap is made progressively thicker, at some point the Fermi level will touch either the valence band or the "hole trap" (deep donor) discussed in the previous chapter (Fig. 3.9). At this point, the 2DEG density stops decreasing and reaches the value shown in eq. 3.5, where $\Delta E_{G,AlGaN}$ is the difference in bandgap energy between GaN and the AlGaN top barrier and the rest of the variables are the same as in eq. 3.4.

$$ns_0 = \frac{\sigma_{AlGaN} \cdot t_{AlGaN} - \frac{\varepsilon\varepsilon_0}{q} \cdot \Delta E_{G,AlGaN}}{t_{cap} + t_{AlGaN} + \Delta d} \tag{3.5}$$

In order to maintain charge neutrality, positive charges are induced at the GaN Cap/AlGaN barrier interface. If there is no "hole trap", or if the "hole trap" density is low, the majority of these positive charges will be mobile holes. In this case, charge control analysis reveals that $|V_{P,access}|$ will not be any larger than $|V_{P,gate}|$ (eq. 3.6), and the ability of the Ga-Polar Deep Recess structure to control dispersion is severely degraded. This is because there is no vertical barrier to mobile holes at pinch-off, as they can float upwards towards the gate electrode under reverse gate-drain bias. If the "hole trap" (deep donor) density is large, then the induced positive charges will be ionized donor states. In this case, $|V_{P,access}|$ will be larger than $|V_{P,gate}|$. However, as discussed in the previous section, if the surface states are slow to respond the large signal response of the device may deviate from that predicted from DC measurements. As a result, the dispersion performance may again be compromised.

$$V_{P,Access} \approx V_{P,gate} = \frac{q \cdot \sigma_{AlGaN}}{\varepsilon \cdot \varepsilon_0} \cdot t_{AlGaN} \tag{3.6}$$

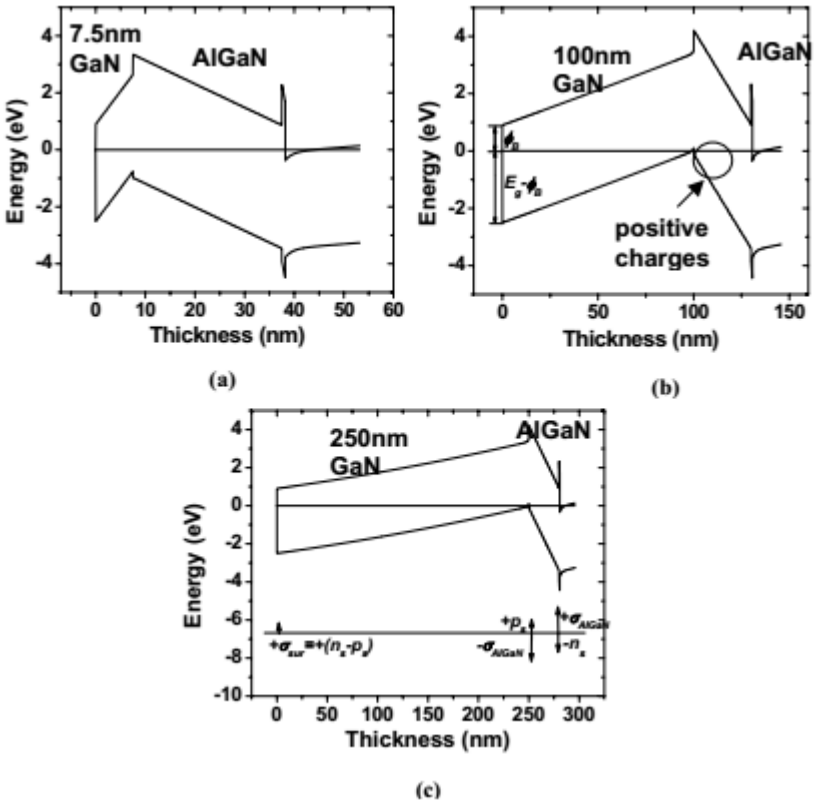

Fig. 3.9: Band diagram for a Ga-Polar Deep Recess structure with no grading or Si-doping of the AlGaN layer. As the GaN Cap is made progressively thicker from 7.5 nm (a) to 100 nm (b) to 250 nm (c), the net negative polarization discontinuity at the GaN Cap – AlGaN top-barrier interface pulls the bands up. (Figures taken from [8]).

To control the electrostatics such that $|V_{P,access}| >> |V_{P,gate}|$, Shen *et al* [8] delta doped the GaN Cap/AlGaN barrier interface with Si. This did result in an increase in $|V_{P,access}|$ and lower DC-to-RF dispersion, but the doping density window was tight. Too much doping substantially increased the leakage current and degraded breakdown voltage [8]. Too little Si-doping did not enhance $|V_{P,access}|$ by the desired amount and dispersion was seen in large signal measurements. Shen *et al*. was able to widen this doping window through use of a graded + Si-doped AlGaN layer. In fact, this is where the idea for the graded + Si-doped AlGaN back-barrier in the N-Polar HEMTs of this thesis came from. However, this design is not ideal for W-Band applications. At W-Band frequencies, the III-N transistor must be scaled significantly in both the lateral and vertical directions. To achieve vertical scaling with a

consistent and repeatable transconductance in the Ga-Polar Deep Recess structure would likely require a selective gate recess etch. A selective etch of AlN with respect to GaN was developed by Bhuttari *et al* [12]. However, a Ga-Polar Deep Recess HEMT with a graded AlGaN top-barrier would necessitate, selectively etching lower composition AlGaN at the top of the barrier with respect to higher composition AlGaN near the 2DEG channel. The selectivity of this etch will be much lower than that between AlGaN and binary GaN, and this could cause fabrication and repeatability issues.

Chapter 3.2.2 – N-Polar Deep Recess Intro:

In this work, optimization of a Deep Recess structure on N-Polar oriented wafers is explored. Fabrication of N-Polar Deep Recess structures (NPDR) was first demonstrated by Kolluri *et al* [13]. The key difference between Gallium and N-Polar Deep Recess HEMTs is the orientation of the polarization fields (Fig. 3.10). In N-Polar Deep Recess HEMTs, the direction of the fields are such that the UID GaN cap pushes the conduction band down relative to the Fermi level (E_F), resulting in an enhancement of the 2DEG charge in the access regions (Fig. 3.11). This is in contrast to Ga-Polar HEMTs, where a UID GaN cap pulls the conduction band up and depletes the 2DEG charge. Further, the presence of the GaN Cap in the N-Polar orientation relaxes the E-Field seen by the channel 2DEG, pulling the centroid of the 2DEG away from the back GaN/Al(Ga)N interface, reducing interfacial and alloy scattering. A large increase in electron mobility for vertically scaled channels results, as this interfacial scattering is one of the dominant scattering mechanisms in scaled N-Polar transistors [14]. Together these benefits greatly lowered the sheet resistance from

410 Ω/square in the gate recessed region, to only 230 Ω/square in the access regions of the device presented in the following sections.

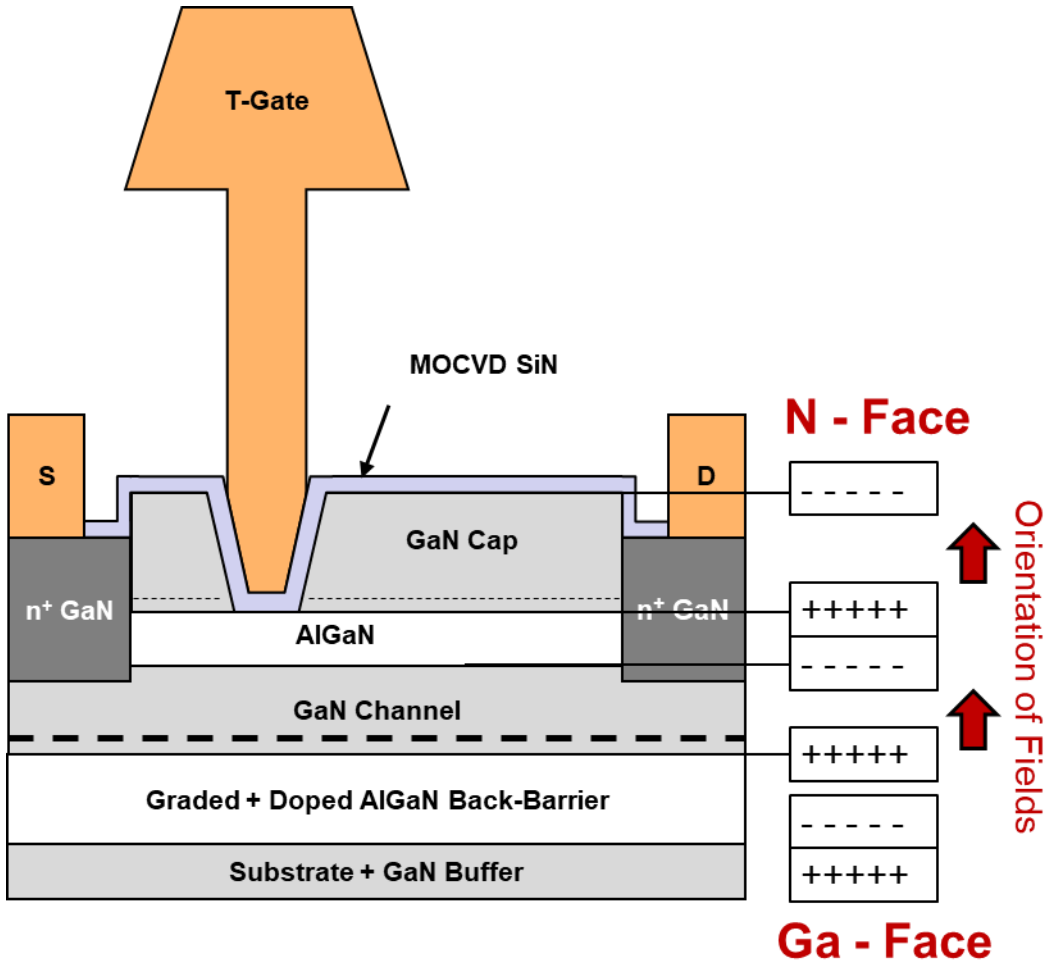

Fig. 3.10: Cross-section of the N-Polar Deep Recess MISHEMT device structure and epitaxial configuration.

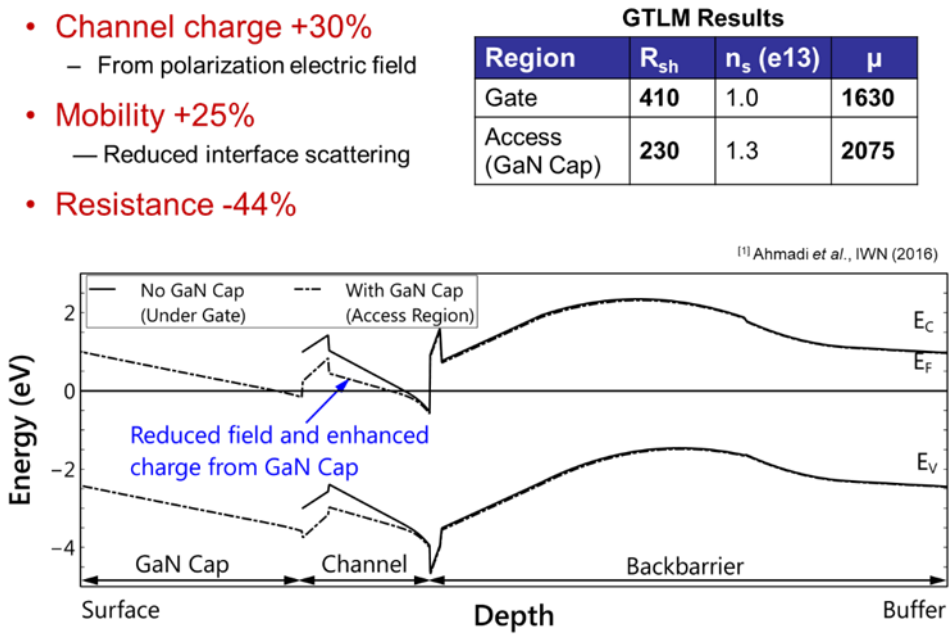

Fig. 3.11: Overlaid band diagrams of the gate recessed and GaN Cap access regions. Can see the conduction band is pulsed down and the electric field of the channel is reduced in the access region of the device.

Moreover, the orientation of the polarization fields in N-Polar HEMTs is such that the addition of the UID GaN cap will enhance $|V_{P,access}|$ regardless of the Si-doping or even if a "hole trap" (deep donor) truly exists at negative polarization interfaces. This is because in N-Polar HEMTs the AlGaN back-barrier presents a barrier to hole leakage to the gate, and the mobile holes stay should stay roughly located at the negative polarization interface under reverse gate-drain bias, unlike in the Ga-Polar Deep Recess HEMT. To precisely control $|V_{P,access}|$, the N-Polar designer will still want to dope the back-barrier, however, this layer is located underneath the 2DEG in N-Face HEMTs, as opposed to on top of the 2DEG like in Ga-Polar HEMTs. As a result, the graded + Si-doped AlGaN layer can be designed more or less independently of the gate metal to 2DEG centroid distance, and high vertical scaling can still be achieved even with a graded + Si-doped design. As mentioned earlier, the graded + Si-doped AlGaN design expands the range of feasible doping densities applicable to the NPDR structure. This enables higher total Si-doping densities, which allows for thinner GaN

caps to achieve the same $V_{p,access}$ relative to the Ga-Polar structures. Thinner GaN caps reduce the amount of extrinsic capacitances and allow for higher frequency operation. With this design, the device designer can precisely control $|V_{P,access}|$ to achieve excellent dispersion control, even at W-Band frequencies. Equation 3.7 and 3.8 describes $|V_{P,gate}|$ and $|V_{P,access,primary}|$ for the NPDR MISHEMT. Equations 3.9, 3.10, and 3.11 describe ns in the gate recessed region, ns in the primary channel in the access region, and the secondary ns induced in the GaN Cap of the NPDR design.

$$V_{P,recess} = \frac{C_{semicon,recess}}{C_{recess_{tot}}} \cdot \{\varphi_B - \Delta E_C + \frac{q}{\varepsilon} \cdot \left[\sigma_{\pi,AlGaN,top} \cdot t_{AlGaN,top} - \sigma_{Si} \cdot \left(t_{AlGaN,top} + t_{chan} - \Delta d1\right)\right] \quad (3.7)$$

$$V_{P,access} = \frac{C_{total,semicon}}{C_{total}} \cdot \left\{\varphi_B + \frac{q}{\varepsilon} \cdot \begin{bmatrix} \sigma_{\pi,AlGaN,top} \cdot t_{AlGaN,top} \\ -\sigma_{Si} \cdot \left(t_{cap} + t_{AlGaN,top} + t_{chan} - \Delta d2\right) \end{bmatrix}\right\} \quad (3.8)$$

$$ns_{recess} = \left(\frac{\frac{\varepsilon}{q} \cdot (\Delta E_C - \varphi_B) - \sigma_{AlGaN_{top}} \cdot t_{AlGaN_{top}}}{t_{AlGaN,top} + t_{chan} - \Delta d1}\right) + \sigma_{Si} \quad (3.9)$$

$$ns_{primary} = \sigma_{Si} - \frac{\sigma_{\pi,AlGaN,top} \cdot t_{AlGaN,top}}{t_{cap} + t_{AlGaN,top} + t_{chan} + \Delta d2 - \Delta d1} \quad (3.10)$$

$$ns_{cap} = \sigma_{Si} - \frac{\frac{\varepsilon}{q} \cdot \varphi_B}{t_{cap} - \Delta d2} - ns_{primary} \quad (3.11)$$

Further, the pinch-off voltage of the secondary 2DEG located in the GaN cap can be calculate from equation 3.12.

$$V_{P,cap} = \frac{C_{semicon_{cap}}}{C_{cap,tot}} \cdot \left[\varphi_B + \frac{q}{\varepsilon} \cdot \left[ns_{primary} - \sigma_{Si}\right] \cdot \left(t_{cap} - \Delta d2\right)\right] \quad (3.12)$$

In these equations, $C_{semicon,recess}$ is the capacitance between the channel 2DEG and the surface of the AlGaN top barrier, $C_{recess,tot}$ is the total capacitance between the channel 2DEG and the top of the MOCVD SiN gate dielectric, $C_{total,semicon}$ is the capacitance between the access region primary 2DEG and the surface of the UID GaN cap, C_{total} is the total capacitance between the access region 2DEG and the top of the MOCVD SiN dielectric sitting on top of the UID GaN cap, $C_{semicon,cap}$ is the capacitance between the secondary 2DEG in the GaN cap and the top of the GaN cap surface, $C_{cap,tot}$ is the capacitance between the secondary 2DEG in the GaN cap and the top of the MOCVD SiN dielectric sitting on top of the UID GaN cap, φ_B is the assumed pinning position between the III-N semiconductor and the MOCVD SiN dielectric, q is the elementary unit of electron charge, ΔEc is the difference in conduction band height between the GaN and the AlGaN top barrier, $\sigma_{\pi,AlGaN,top}$ is the net polarization charge at the top AlGaN barrier/GaN channel interface, σ_{Si} is the total Si doping (in cm^{-2}) in the graded AlGaN back-barrier and Si-doped GaN layer, $\Delta d1$ is the distance between the AlN interlayer and the centroid of the primary 2DEG in both the recessed and access regions (values may be slightly different in these regions), $\Delta d2$ is the distance between the centroid of the secondary GaN cap 2DEG and the AlGaN top barrier, t_{cap} is the thickness of the UID GaN cap, $t_{AlGaN,top}$ is the thickness of the top AlGaN barrier, and t_{chan} is the thickness of the UID GaN channel. It should be noted that these equations assume complete ionization of the back-barrier Si-dopants and that the Si-doping is high enough such that Fermi Level is above the valence band and the "hole trap". This is tantamount to saying that this assumes that the Fermi Level is located somewhere between the "hole trap" level and the Si donor state level.

Finally, the vertical distance between the gate electrode and gate recessed 2DEG can be precisely controlled in this structure by using the AlGaN top-barrier as a selective etch stop

for the UID GaN cap. Thus, this AlGaN top barrier serves 2 purposes, one is to enhance the breakdown voltage of the device as described in Chapter 2, and second as an etch stop for the NPDR gate and ohmic recesses.

Chapter 3.3 – Epi-Structure of the NPDR MIS-HEMT:

As mentioned earlier, transistors for RF amplification purposes should be capable of producing high large signal gain, high efficiencies, and high output RF powers at the frequency range of interest. In this work, the frequency range of interest is the W-Band portion of the electromagnetic spectrum (75 – 110 GHz). In this section, a generalized description of the epitaxial structure for the NPDR MISHEMT is given. The thought behind the specific design choices made for each layer, as well as how these choices affect large signal power performance at W-Band is described in detail. A generic NPDR epi-structure is shown in Fig. 3.11. Band diagrams for the gate recessed region and GaN cap access regions are shown in Fig. 3.11 (b) and (c) respectively [15].

Chapter 3.3.1 – Graded + Si-Doped AlGaN Back-Barrier:

Achieving high gain at W-Band frequencies in the III-N system requires low extrinsic resistances (eq. 3.13). Low resistances can be obtained when the 2DEG charge in both the gate recessed and access regions is high (so long as the electron mobility is high as well). A high 2DEG is generally desirable, though there are tradeoffs between the charge density and breakdown voltage, as described in chapter 2.3. Regardless, equation 3.9 and 3.10 reveal that the 2DEG density in the gate and access regions is limited by the total cm^{-2} Si doping density in the back-barrier. As mentioned earlier, the assumption that went into equations 3.9 and

3.10 is that the Fermi Level is below the Si-doping density, i.e. that all of the Si dopants are completely ionized. When this is no longer true, the channel 2DEG begins to saturate. At some point, a parasitic 2DEG may form at the AlGaN back-barrier/Si-doped interface or within the graded AlGaN layer. The assumption of complete ionization is true so long as the graded polarization charge of the AlGaN back-barrier ($\sigma_{AlGaN,grade}$) is greater than the Si doping density. Thus, the actual limit placed on the 2DEG density is how high of an Al composition the graded AlGaN back-barrier grades to. This was optimized by the MOCVD growers prior to this work, and for this specific back-barrier design, 38% was found to roughly be the limit when the N-Polar HEMT is grown on a sapphire substrate. An Al composition higher than this will likely lead to cracking in the AlGaN back-barrier. At 38%, minimal cracking is typically not seen, and this is usually only near the edges of the wafer. A back-barrier using InAlN could be used to achieve higher channel charge. However, previous N-Polar HEMTs grown on InAlN back-barriers resulted in DC-to-RF dispersion, likely related to the Fermi Level interacting with the hole trap in the back. More growth/design optimization was deemed necessary if such a back-barrier were to be used, and the graded AlGaN back-barrier used in the previous chapter was chosen.

Chapter 2.3 thoroughly details the tradeoffs between higher 2DEG density and the breakdown performance of a N-Polar transistor. The HEMT in that case was planar (no GaN cap in access region) and had a slightly different gate cap stack. However, the results are still mostly applicable to the NPDR MISHEMT explored here, so long as the total charge density (including the 2DEG in the GaN cap) is included. For the first sets of NPDR HEMTs described in this chapter, a Si doping density of ND1 = ND2 = $5.5 \cdot 10^{13}$ cm^{-2} was used. This gives a total Si doping density of $\sigma_{Si} = 1.65 \cdot 10^{13}$ cm^{-2}.

$$f_{max} = \frac{\frac{gm_{ext}}{2\pi * \left(C_{gs} + C_{gd}\right)}}{\sqrt{\frac{4}{R_{ds}} * \left(R_g + R_s + R_i\right) + 8\pi * f_T * C_{gd} * \left(2 * R_g + R_s + R_i\right)}} \quad (3.13)$$

Chapter 3.3.2 – UID GaN Channel:

Achieving appreciable gain at W-Band frequencies in the III-N system requires low extrinsic and intrinsic capacitances (i.e. short gate lengths, eq. 3.13). In order to maintain adequate control of the channel charge the intrinsic gate-source capacitance should be large relative to the extrinsic capacitances of the device. This necessitates a small 2DEG to gate electrode distance. Because the centroid of the channel 2DEG is located at the bottom of the UID GaN channel/AlGaN interface in N-Polar HEMTs, the thickness of the UID GaN channel is the primary variable determining the gate to 2DEG distance. Thus, a relatively thin UID GaN channel is desired for N-Polar transistors designed for W-Band applications. As equation 3.9 shows, the thinner the channel, the larger the effect of the φ_B term is at depleting the channel 2DEG. This places a limit on how thin a UID GaN channel can be while still maintaining adequately high 2DEG channel charge. Prior to the growth of the initial set of NPDR wafers, the MOCVD growth team had recently (at the time) demonstrated N-Polar HEMTs with a 46% AlGaN cap and a 12 nm UID GaN channel with reasonable 2DEG densities and electron mobility. Thus, a channel thickness of 12 nm was chosen for the initial set of NPDR MISHEMTs.

Chapter 3.3.3 – Gate Cap Stack:

There is a tradeoff in performance metrics involved when choosing the appropriate gate cap stack for a N-Polar MISHEMT. If the gate dielectric is too thin, the breakdown voltage will be limited by gate leakage and a lower breakdown voltage will result. Thickening the gate dielectric will lower this gate leakage until the breakdown is no longer limited by gate leakage, but by breakdown of the semiconductor/dielectric interface (see Chapter 2.2). However, a thicker gate dielectric increases the distance between the 2DEG and gate electrode, reducing C_{gs} and reducing the control the gate has on the channel charge. This can lead to short channel effects which can reduce the large signal gain, efficiency, and RF output power of the transistor. At lower frequencies, larger gate lengths can be used, and the MOCVD SiN gate dielectric can be made very thick without compromising performance. However, at W-Band a compromise between gate leakage, breakdown voltage, and aspect ratio must be made. More details regarding the MOCVD SiN thickness chosen are given in later sections of this chapter.

Of the different gate cap stacks investigated in Chapter 2.2 the AlGaN + MOCVD SiN stack was found to be the best from a breakdown voltage perspective. The tradeoffs in the thickness of the AlGaN top-barrier are similar to those of the MOCVD SiN gate dielectric. A thicker AlGaN top-barrier will likely reduce the gate leakage and increase the breakdown voltage. At a certain thickness the benefits in terms of breakdown performance enhancement likely saturates and a thicker AlGaN top-barrier probably won't increase breakdown voltage further. The drawback of a thicker AlGaN top-barrier is the reduction in aspect ratio, similar to what was stated for a thicker MOCVD SiN gate dielectric. A thickness of 2.6 nm was chosen for the AlGaN top-barrier (same as in Chapter 2).

The design tradeoffs for the Al composition of the top-barrier are similar to what was stated before. A higher Al composition will likely lower the leakage and increase the breakdown voltage. For a given AlGaN top-barrier thickness, the Al composition at which the breakdown enhancement saturates at might be different. Higher Al compositions also can degrade the aspect ratio indirectly. Although changing the Al composition of the top-barrier does not change the total distance between the center of the 2DEG and the gate electrode, equation 3.9 and 3.10 reveal that a higher Al composition will deplete the channel 2DEG density for a given channel thickness. Thus, the Al composition places a limit on how thin a channel can be used for a given N-Polar W-Band transistor. An Al composition of 27% was chosen as a compromise between the gate leakage/breakdown performance of the transistor and the aspect ratio considerations.

There is an additional tradeoff for thicker and/or higher composition AlGaN top-barriers that was not explored in the planar N-Polar MISHEMT of Chapter 2.2. In a N-Polar Deep Recess structure, when a UID GaN layer is added on top of the AlGaN top-barrier, the orientation of the polarization fields are such that a 2DEG is induced in the GaN cap. As equations 3.10 and 3.11 illustrate, the total 2DEG density in the access region is not affected by the AlGaN cap. For cap thicknesses >> the channel thickness, the 2DEG density in the access region is basically set only by the Si doping and the GaN Cap thickness. However, the AlGaN cap acts to reduce the amount of useful 2DEG that exists in the primary channel and repartitions this portion of the 2DEG to the 2DEG that exists in the GaN Cap. A barrier (the AlGaN top-barrier) exists between the 2DEG in the GaN Cap and the primary 2DEG in the channel. Because of this barrier, the 2DEG in the GaN Cap should have a negligible contribution to actual conduction current in the HEMT. The 2DEG in the GaN Cap

will become depleted under off-state operation though. Thus, the 2DEG in the GaN Cap will contribute to lowering the breakdown voltage of the transistor (see Chapter 2.3). Thus, the higher the 2DEG in the GaN Cap for a given total access region 2DEG density, the lower the breakdown voltage is for a particular On-Resistance (i.e. the breakdown vs. Ron product decreases due to the 2DEG in the GaN Cap). The thicker the AlGaN top-barrier or the higher the Al composition the higher the percentage of the overall access region 2DEG is located in the GaN Cap.

Finally, the selectivity of the selective gate and ohmic recess etches detailed in the next section depends on the Al composition of the top-barrier. Moreover, to ensure one does not etch through the AlGaN top-barrier, a thicker AlGaN top-barrier can be used as well. Shen *et al* [16] did a selectivity study on Ga-Polar (Fig. 3.12). For a 27% AlGaN top-barrier, we obtained similar results to those which he found on a Ga-Polar HEMT with a 27% AlGaN top-barrier. As a compromise between the leakage/breakdown performance, the aspect ratio of the transistor, and the etch selectivity, an AlGaN top-barrier thickness of 2.6 nm (same as Chapter 2) and an Al composition of 27% was chosen for the NPDR MISHEMTs in this work.

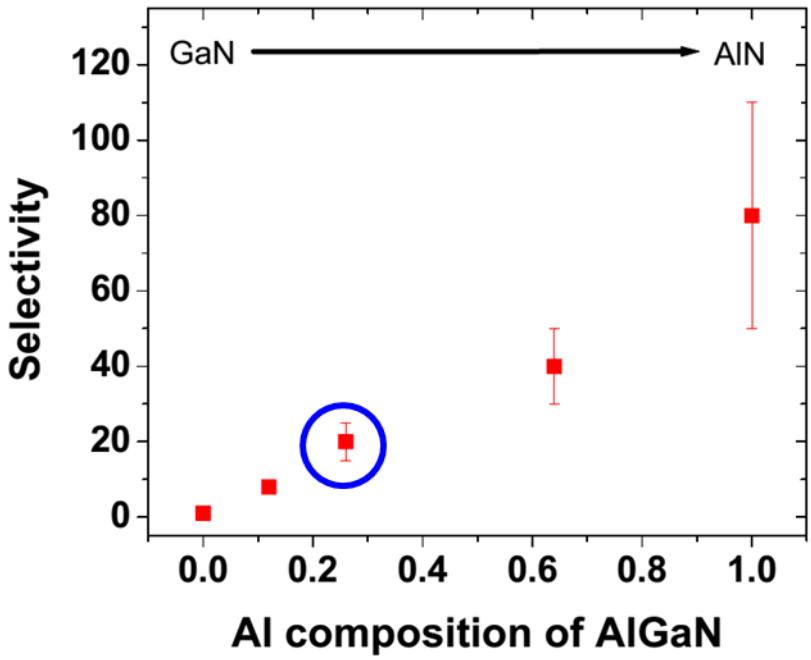

Fig. 3.12: Etch selectivity of $Al_xGa_{1-x}N$ with respect to GaN from [16]

Chapter 3.3.4 – GaN Cap Thickness:

The analytical equation for the pinch-off voltage in the GaN Cap Access region for the NPDR MISHEMT is given in eq. 3.8. When the GaN cap is significantly thicker than both the GaN channel and the MOCVD SiN dielectric thickness ($t_{cap} >> t_{chan}$ and $t_{cap} >> t_{SiN}$), then $|V_{P,access}| \approx \sigma_{Si} \cdot t_{cap}$. The total Si doping was chosen to be $\sigma_{Si} = 1.65 \cdot 10^{13}$ cm^{-2} taking into consideration the findings from the planar N-Polar MISHEMT studies of Chapter 2. Thus, the thickness of the UID GaN cap is the primary knob controlling $|V_{P,access}|$ and therefore dispersion in our NPDR MISHEMT. Ideally, the pinch-off voltage in the access region should be made such that minimal dispersion is seen during large signal operation of the device for all gate-drain biases the NPDR MISHEMT device will see during operation. However, the NPDR designer wants the thinnest possible GaN Cap which can satisfy this requirement, as

thicker GaN Caps may present manufacturability/repeatability issues with respect to the selective gate and ohmic recesses stopping on the AlGaN top-barrier. Further, thicker GaN Caps have higher extrinsic capacitance values which can limit the large signal RF gain of the device. For these reasons, the thinnest possible GaN Cap which can be used to ameliorate dispersion for all gate-drain voltages during device operation is optimal.

Chapter 3.4 – GaN Cap Thickness Series + Fabrication Details:

A series of 4 NPDR MISHEMTs with different GaN Cap thicknesses and the same everything else were grown. Because all these samples had the same total Si doping, this GaN Cap thickness series can also be though of as an access region pinch-off voltage series. The goal of this experiment is to find the minimum GaN Cap thickness/pinch-off voltage necessary to eliminate dispersion at all gate-drain bias voltages of interest. Table 3.1 contains the GaN Cap thicknesses, predicted (via. Eq. 3.8) pinch-off voltages, and measured pinch-off voltage for each of the 4 samples. The exact reason for the discrepancy between the theoretical and measured pinch-off voltages is unknown. It may be that the actual active Si donor dopant density is less than the intended dopant density. If the Si donor dopant density in the graded AlGaN and Si-doped GaN layers is $3.5 \cdot 10^{18}$ cm^{-3}, the access region pinch-off values predicted by theory match quite well with the measured values of pinch-off.

t_{cap}	$V_{P,access}$ (eq. 3.8)	$V_{P,access}$ (Simulated via BANDENG)	$V_{P,access}$ (Measured via CV)	$V_{P,access}$ (Measured via Hg CV)
45 nm	-20 V	-21 V	-14 V	
75 nm	-30 V	-32 V		-21 V
110 nm	-41 V	-44 V		-29 V
140 nm	-51 V	-56 V		NA

Table 3.1: GaN Cap (pinch-off voltage) series description.

Chapter 3.4.1 – Growth Procedure:

Samples were grown via MOCVD on c-plane sapphire substrates with a 4^{o} miscut towards the a-plane. Trimethylgallium (TMGa), trimethylaluminum (TMAl), ammonia (NH_3), disilane (Si_2H_6), and Ferrocene (Cp_2Fe) were used as precursors. The cross-section of the device structure is shown in Fig. 3.12. From substrate on up, the samples contain an initial high-temperature GaN nucleation layer, an Fe-doped GaN buffer layer, a 150 nm UID GaN spacer layer, a 10 nm of Si-doped GaN, a 20 nm graded and Si-doped AlGaN back-barrier, a 10 nm UID $Al_{0.38}Ga_{0.62}N$ spacer layer, a 0.7 nm AlN interlayer, a 12 nm UID GaN channel, a 2.6 nm $Al_{0.27}Ga_{0.73}N$ top-barrier, and one of the 4 UID GaN caps listed in Table 3.1. Band diagrams of the GaN Capped access regions for each of the 4 cap thicknesses is given in Fig. 3.13. Two quarters of each sample were used. On one quarter, a 5 nm MOCVD SiN gate dielectric was deposited (as was done in Chapter 2). In the 2nd quarter a 9 nm MOCVD SiN dielectric was used. This thicker MOCVD SiN dielectric was chosen so that capacitance-voltage (CV) measurements could be made on top of the GaN cap access regions without excessive gate leakage messing up the measurement (pinch-off voltages of these thick GaN Cap access regions are very negative). The 9 nm of MOCVD SiN was apparently not thick enough to enable CV measurement of the thickest (140 nm) GaN Cap device apparently though (Table 3.1). Additionally, the set of samples with the 9 nm MOCVD SiN had a piranha etch (H2SO4:H2O2) performed on them after the selective gate recess prior to MOCVD SiN deposition. The piranha solution did not attack the GaN capped regions, however, in the gate recessed regions the $Al_{0.27}Ga_{0.73}N$ top-barrier was etched in a non-uniform fashion. This appears to be an issue specific to Al containing N-Polar films and has not been witnessed on Ga-Polar HEMT devices. This caused a very large positive shift in threshold voltage in the

gate recessed regions (closer to being an enhancement mode device), reduced the 2DEG density in this region and greatly increased the resistance of the channel in the gate recessed region greatly. Interestingly, it did not seem to introduce any dispersion in the devices. Some of the observations made on the 9 nm MOCVD SiN gate dielectric samples which do not seem to be directly affected by this piranha exposure are included in the following sections.

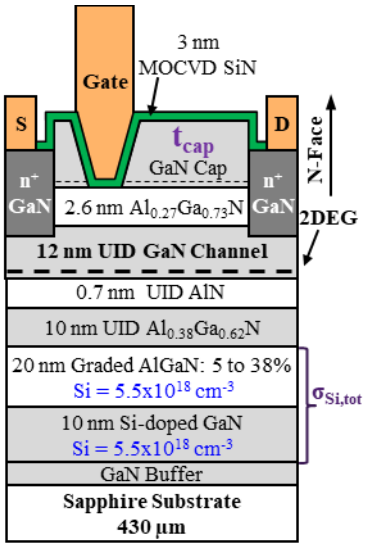

Fig. 3.12: Cross-section of the N-Polar Deep Recess MISHEMT device structure (not to scale).

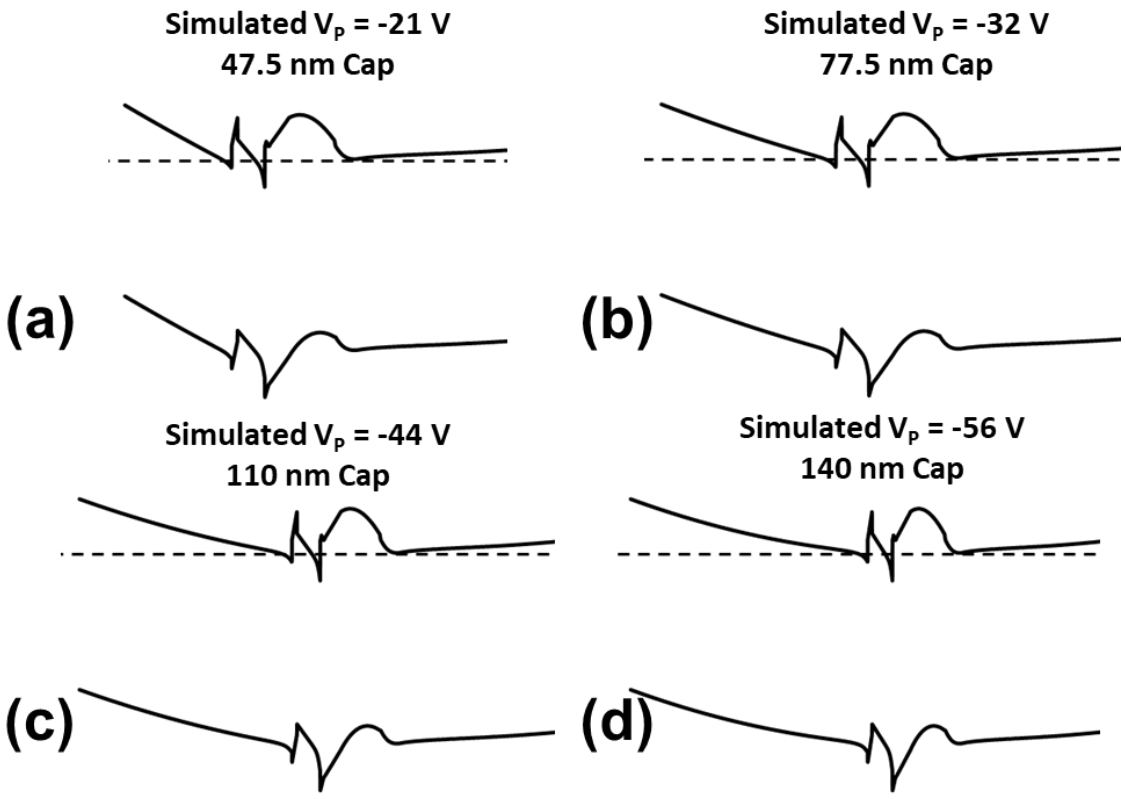

Fig. 3.13: Simulated GaN Cap access regions for the (a) 47.5 nm GaN Cap, (b) 77.5 nm GaN Cap, (c) 110 nm GaN Cap, and (d) 140 nm GaN Cap [15].

Chapter 3.4.2 – Fabrication Procedure:

Due to the anisotropic transport properties of N-polar HEMTs grown on vicinal substrates, all devices are designed such that source-drain conduction occurs in the high mobility direction parallel to the direction of substrate miscut [17]. The subsequent fabrication procedure is similar to that reported in [18] with alterations due to the presence of the UID GaN cap (process is also very similar to that shown in Chapter 2). A pictorial representation of the fabrication procedure is given in Fig. 3.14. Fabrication begins with the Alignment marks. Alignment marks are patterned via stepper lithography and transferred to the GaN epitaxial layers through reactive ion etching in a Cl_2 based chemistry. A regrowth mask

consisting of (from bottom to top) the initial 5 nm MOCVD SiN dielectric, a thin ($\leq$ 15 nm) ALD Al_2O_3 etch-stop layer, a 500 nm PECVD SiO_2 layer, and a 10 nm hardmask of Cr on top is then deposited. Stepper lithography is used to pattern this regrowth mask and an inductively coupled-plasma (ICP) dry etch is used to transfer the pattern to the Cr hard mask and then the SiO_2 layers in a Cl_2 and CF_4/O_2 gas chemistry, respectively. The Cr hardmask is then removed in a blanket Cl_2 based dry etch. After the dry etches, the remaining Al_2O_3 etch-stop layer is selectively wet etched off in a timed TMAH based photoresist developer wet etch (developer does not etch MOCVD SiN). The MOCVD SiN_x covering the GaN channel surface is then etched off with a low power CF_4/O_2 ICP dry etch. Prior to the n^+ GaN regrowth, a BCl_3/SF_6 inductively coupled plasma (ICP) dry etch with a selectivity of between 11 and 22 to 1 is implemented to remove the UID GaN cap with respect to the $Al_{0.27}Ga_{0.73}N$ top barrier [12]. An additional unselective BCl_3/Cl_2 etch is then performed to remove the $Al_{0.27}Ga_{0.73}N$ top barrier prior to n^+ GaN regrowth. The n^+ GaN and high temperature MOCVD SiN_x dielectric regrowth steps follow from [18]. After dielectric regrowth, electron-beam-lithography (EBL) is used to define the gate recessed region of the transistor. In this case, a low pressure, unselective BCl_3/Cl_2 etch was used to remove the 1st 60% of the trench. The purpose of this unselective etch was to try and establish a 60^o sidewall slope, which is slightly steeper than what is achievable with the selective recess alone (later it was found to not make much of a difference, and this unselective recess was dropped from the process). This was followed by another selective BCl_3/SF_6 etch to finish off the recessed trench and stop on the $Al_{0.27}Ga_{0.73}N$ top-barrier. Fig. 3.15 (a) shows a cross-sectional SEM image of the trench profile after completion of the etch. Fig 3.15 (b) illustrates that the etch results in a smooth surface, with a surface roughness roughly equivalent to the starting surface roughness. The sample is then

put back in the MOCVD reactor for high temperature SiN_x gate dielectric regrowth followed by a BCl_3/Cl_2 reactive ion etch for mesa isolation. Realignment to the recessed trench is performed in the EBL system to write the gates. Unless stated otherwise, in this study, I-Gates whose metal completely covered the floor of the gate recess + ½ of the GaN Cap sidewall were used. This was an attempt to make sure that any dispersion seen was due to an insufficient thickness/pinch-off voltage of the access region, not due to unpassivated gaps between the metal and GaN Cap sidewalls. Ohmic contact and pad formation follow. The samples with 9 nm MOCVD SiN did not receive any PECVD passivation. The samples with 5 nm MOCVD SiN had a thin 18 nm SiN_x passivation layer deposited via plasma-enhanced chemical vapor deposition to remove any residual dispersion caused by gate misalignment inside the trench.

Chapter 3.4.3 – CV and Gated TLM:

CV and gated TLM was performed on the gate recessed section of one the GaN Cap samples with 5 nm of MOCVD SiN gate dielectric. CV and gated TLM were also performed on the 47.5 nm GaN Cap sample access region with 9 nm of MOCVD SiN (needed this thickness to measure CV until pinch-off). The extracted electron density, mobility, and sheet resistances for both regions is shown in Fig. 3.16. As predicted earlier, the access region GaN Cap minimizes the surface depletion term in equations 3.9, 3.10, and 3.11. This results in an increase of the total charge density from $0.95 \cdot 10^{13}$ cm^{-2} in the gate recessed region to $1.32 \cdot 10^{13}$ cm^{-2} in the GaN cap access region of the device at a gate bias of 0 V. However, this $1.32 \cdot 10^{13}$ cm^{-2} actually consists of both the primary channel 2DEG and the GaN Cap 2DEG. The GaN Cap 2DEG likely does not appreciably contribute to the conduction current due to

the barrier the electrons see from the $Al_{0.27}Ga_{0.73}N$ top-barrier. Looking at Fig. 3.16 (b), we can see that the GaN Cap 2DEG pinches off at ≈ -2 V. At this voltage bias, very little depletion of the primary channel 2DEG has occurred, and we can see that the GaN Cap has increased the primary channel 2DEG to ~$1.15 \cdot 10^{-13}$ cm^{-2}. Further, the 2DEG mobility was also increased by the GaN Cap.

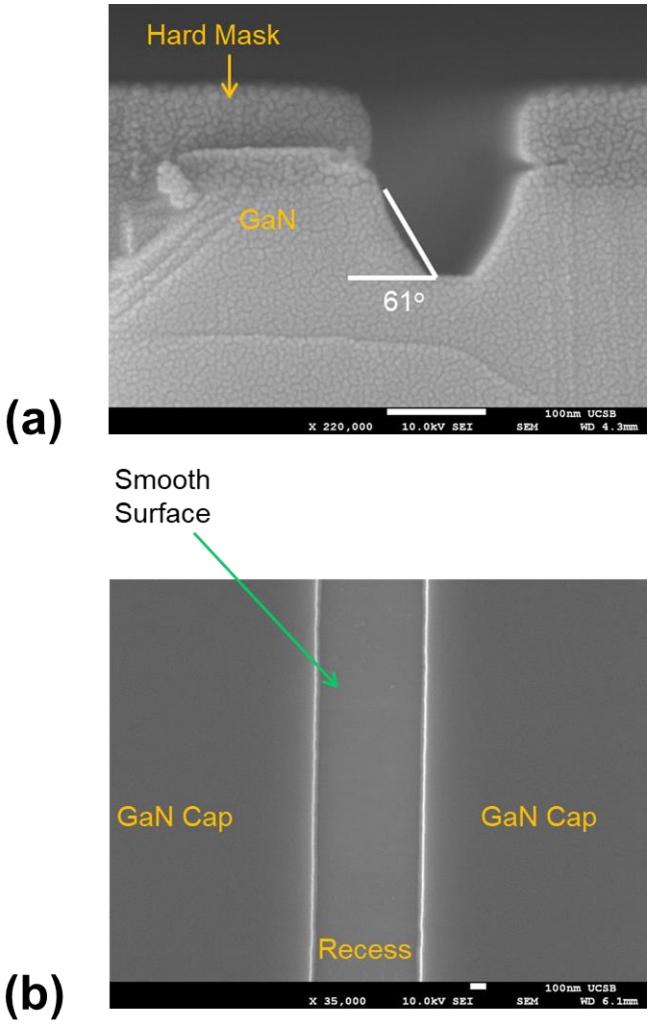

Fig. 3.15: SEM photos of the (a) cross-section of the gate recessed trench and (b) planar image of the gate recessed region after the selective etch has been performed.

Peak mobility was increased from ~1,600 $V \cdot cm^{-2} \cdot s^{-1}$ to ~2,100 $V \cdot cm^{-2} \cdot s^{-1}$. As stated earlier, the higher 2DEG mobility is because the presence of the GaN cap relaxes the vertical

E-Field in the channel. This pulls the centroid of the 2DEG away from the GaN/AlN interface, significantly reducing the interfacial charge scattering that occurs there. Fig. 3.17 shows the conduction bands of the gate recessed and GaN Capped access regions respectively. Can see that the distance between the AlN interlayer and the centroid of the 2DEG has proportionally been increased significantly with the addition of the GaN Cap. Although the absolute distance value is very small in both cases, the interfacial charge scattering's effect drops off with $\left(\frac{1}{distance}\right)^2$, so a substantial difference should be expected. Together, the increase in primary 2DEG density and electron

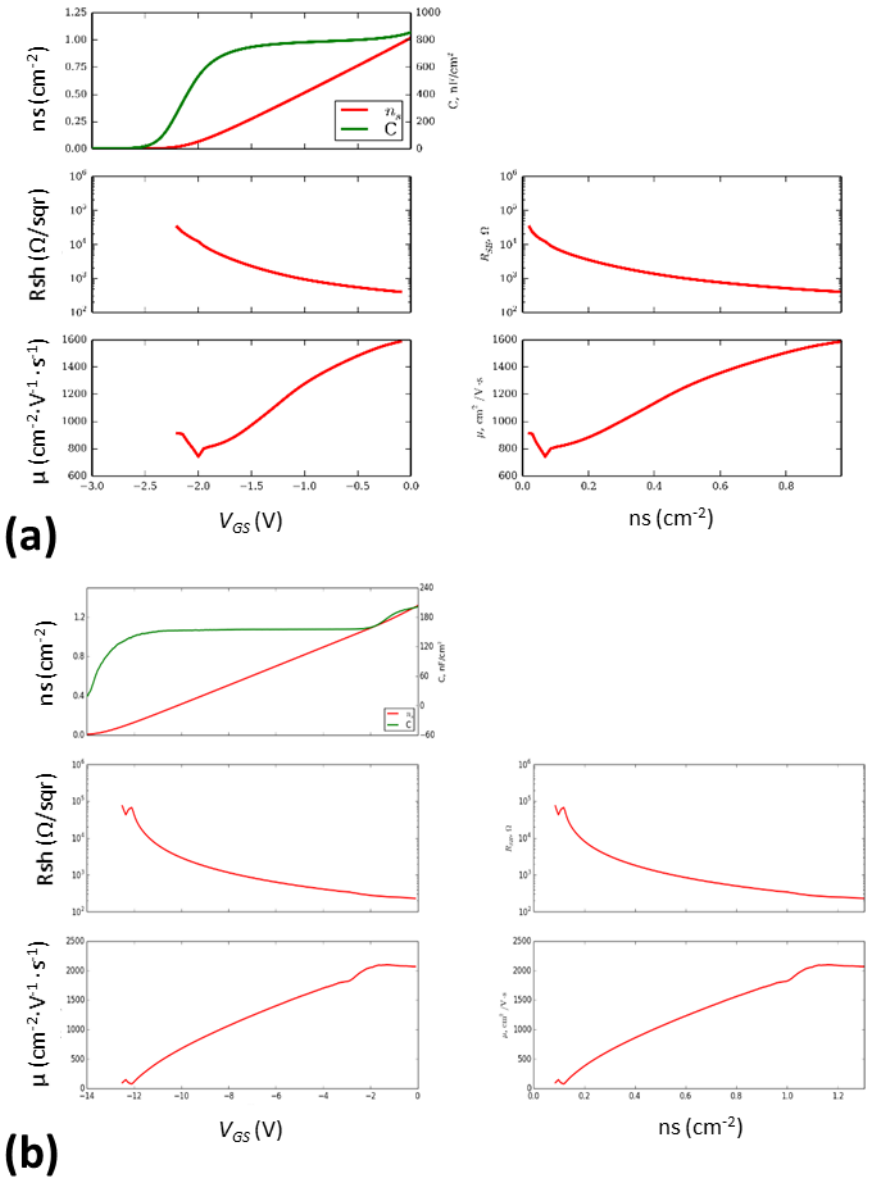

Fig. 3.16: Electron mobility, sheet resistance, and 2DEG density extracted from Gated TLM measurements from the (a) gate recessed and (b) GaN Cap access regions, respectively.

mobility reduced the sheet resistance from 410 Ω/sqr in the gate recessed region to ≈255 Ω/sqr in the access region at a gate bias of 0 V. According to the data, the Rsh of the access region is actually ≈225 Ω/sqr at 0 V. However, this is partially due to the contribution of the GaN Cap 2DEG, which does not actually appreciably contribute to current in the actual transistor device. As a side note, in the gate recessed region, the peak 2DEG mobility occurs at a

gate bias of 0 V. At more negative gate biases the centroid of the 2DEG is pushed further into the back-barrier, increasing the interfacial and alloy scattering, in turn reducing electron mobility. Interestingly, in the access region the peak mobility occurs at ~ -2 V. This is also the voltage at which the GaN Cap 2DEG pinches off. Unlike in actual transistor IV measurements, both the primary and GaN Cap 2DEG are being measured in these gated TLM measurements. The GaN Cap 2DEG's mobility is likely lower than that of the primary channel because it lacks the AlN interlayer of the primary channel 2DEG. As a result, the overall mobility is dragged down by the GaN Cap 2DEG until it is fully pinched off.

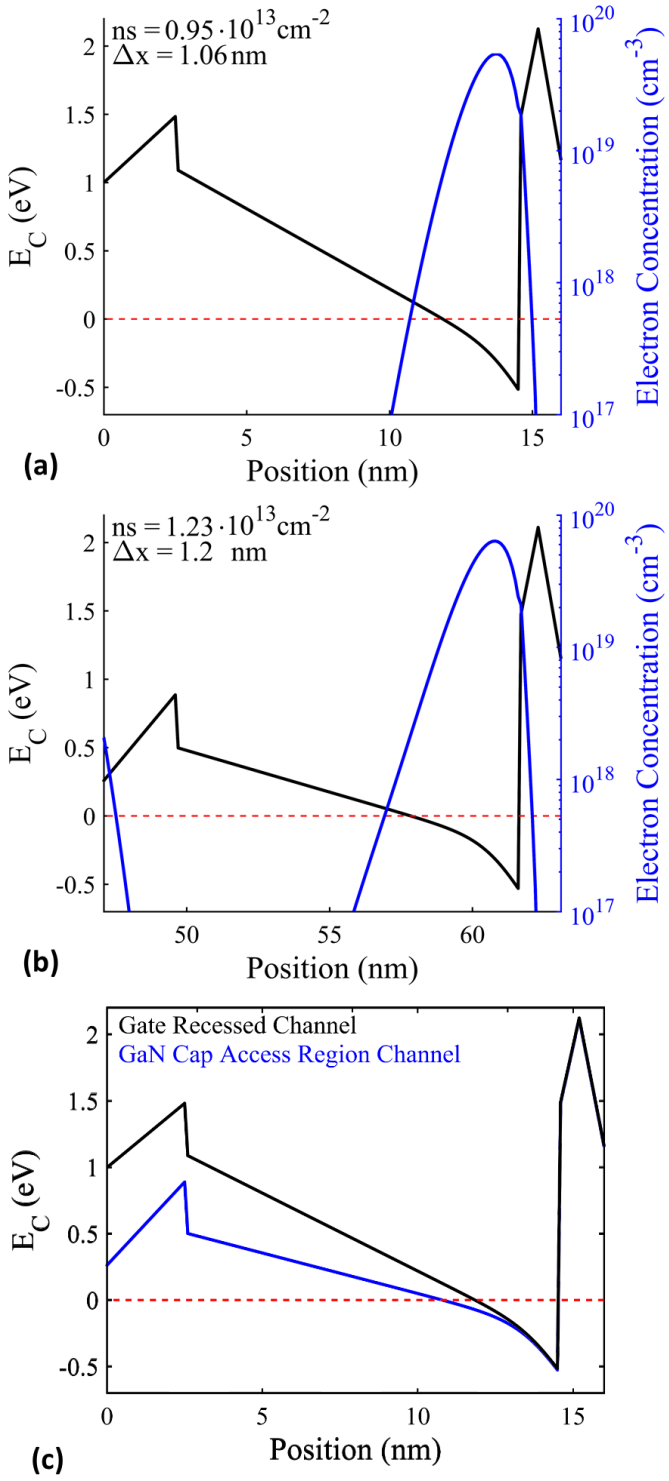

Fig. 3.17: Comparison of the conduction band profile and 2DEG profile in the channel region of the NPDR MISHEMT in (a) the gate recessed and (b) the GaN Cap Access Region of the device. The Δx value in (a) and (b) is the distance between the centroid of the 2DEG and the AlN interlayer. The addition of the GaN cap increases this distance by about 13%, leading to the large increase in 2DEG mobility described earlier [14]. In (c) the channel conduction band profiles of the Gate Recessed (black line) and GaN Capped Access region (blue line) are overlaid with one another to emphasize the reduction in the vertical E-Field present in the channel with the addition of the GaN Cap in the Access Region.

Chapter 3.4.4 – PIV Results:

Fig. 3.18 shows dual PIV data taken at Teledyne Scientific for the thinnest/lowest $|V_{P,access}|$ GaN Cap sample (47.5 nm GaN Cap) with a 9 nm MOCVD SiN gate dielectric, and nominally 15 nm of gate metal coverage over the source and drain sidewalls (roughly ½ the GaN Cap sidewall). Although dispersion is non-zero, it is still very low within the source-drain bias voltages explored in Fig. 3.18 (up to a V_{DSQ} = 20 V). Moreover, due to the finite drive power and matching capabilities of the W-Band load pull system in the Mishra lab, it is unlikely that we would bias our NPDR MISHEMT much beyond 20 V for large signal power measurements anyway. Further, the relatively low breakdown voltage of the NPDR MISHEMT relative to the planar N-Polar MISHEMTs of Chapter 2 (see next section), also make it unlikely a drain quiescent bias much

greater than 20 V would be applied to the device, even if the Mishra W-Band load pull system could provide the necessary input power and matching conditions. Thus, the thinnest GaN Cap device (47.5 nm GaN Cap) appears to provide excellent control of dispersion in the entire range of source-drain quiescent bias voltages of interest at W-Band (target frequency range of this work). As stated earlier, to maximize both the large signal gain and efficiency of our NPDR MISHEMT at W-Band frequencies we need to minimize capacitance. The 47.5 nm GaN Cap introduces the smallest amount of additional capacitance relative to all the other aN Cap thicknesses investigated in this study due to it being the thinnest GaN Cap. Because of this, a 47.5 nm GaN Cap thickness is deemed to be the best GaN Cap thickness choice of all GaN Cap thicknesses investigated in this thesis.

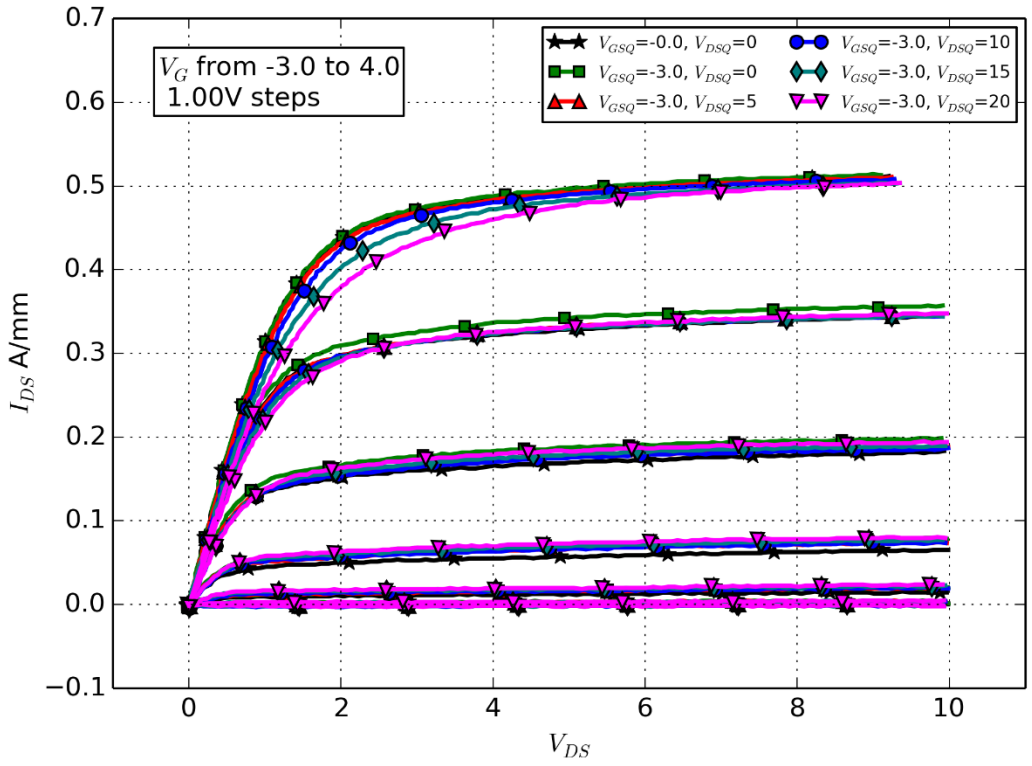

Fig. 3.18: Dual pulsed IV taken on the 47.5 nm GaN Cap device at a V_{GSQ} = -3 V and a V_{DSQ} from 0 to 20 V in 5 V steps.

Chapter 3.4.5 – Breakdown Voltage:

Drain Current Injection (DCI) measurements were taken on the 47.5 nm GaN cap sample with the 5 nm MOCVD SiN gate dielectric thickness [19]. A 1 mA/mm injection current was used. A thorough explanation of this technique and how to properly analyze the DCI scans is given in Chapter 2.2 and 2.3. Representative DCI scans for the 47.5 nm GaN Cap sample with a 5 nm MOCVD SiN gate dielectric is shown in Fig. 3.19 (a). For this sample with the thinner (5 nm) MOCVD SiN gate dielectric, channel breakdown was not witnessed, and almost all breakdowns were non-catastrophic (Fig. 3.19 (a)). Further, the breakdown voltages (and gate leakages) were much lower (higher) than what was measured

on the planar (i.e. no GaN Cap in access region) N-Polar samples of Chapter 2.3 with similar doping levels.

Multiple reasons likely contributed to this breakdown voltage and gate leakage discrepancy. For one thing, the 2DEG density in the access region is much higher in the NPDR MISHEMT than in the planar N-Polar transistors of Chapter 2. The presence of the 47.5 nm GaN Cap significantly reduces the effect of the surface barrier height and AlGaN top-barrier terms in equations 3.9, 3.10, and 3.11. Moreover, an additional 2DEG is also induced in the GaN Cap as well. Together, these effects increased the total charge density in the GaN Cap access region of the NPDR MISHEMT to $\approx 1.32 \cdot 10^{13}$ cm^{-2} despite being only $\approx 0.95 \cdot 10^{13}$ cm^{-2} in the gate recessed region (2DEG density in gate recessed region is equal to what it would be in an equivalent planar N-Polar MISHEMT). In a FET, the majority of the source-drain voltage is held in the gate-drain access region (Fig. 3.5). As a result, the total charge density in the access region of the HEMT plays a large role in determining the peak E-Fields in the transistor. When the NPDR MISHEMT is held in the off-state, both the primary and the GaN Cap 2DEGs will become depleted and contribute to the E-Field. This causes the NPDR MISHEMT to have higher overall E-Fields than

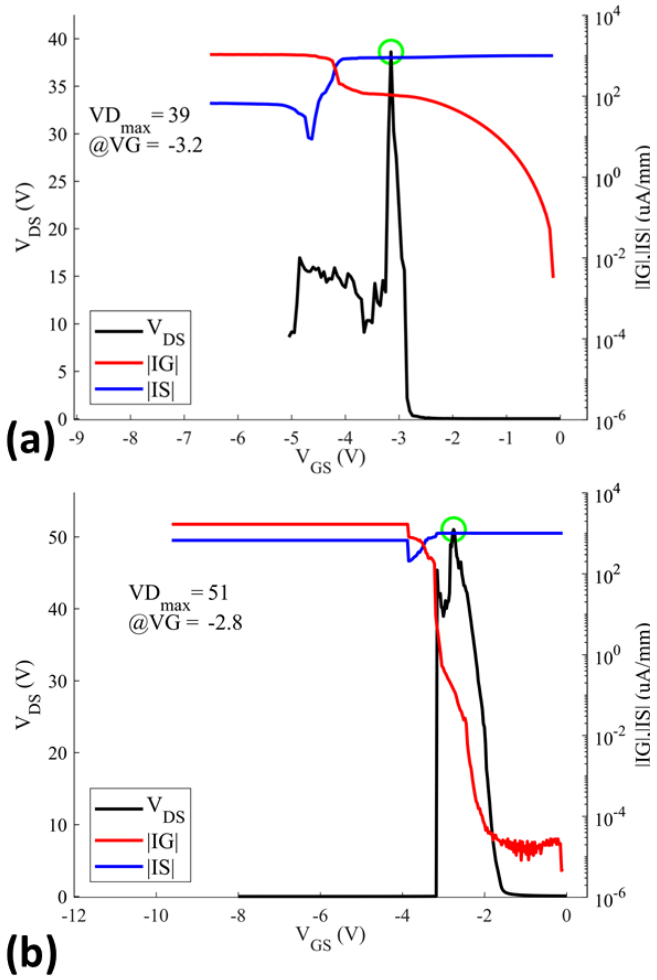

Fig. 3.19: DCI scans from the 47.5 nm GaN Cap sample with (a) 5 nm of MOCVD SiN and (b) 9 nm of MOCVD SiN.

an equivalent planar N-Polar MISHEMT. Additionally, the peak E-Field in the NPDR MISHEMTs of this section occurs at the corner of the gate recess/GaN Cap intersection (Fig. 3.20 (b)). The sidewall of the GaN Cap has a nominally thinner gate cap stack due to the absence of an AlGaN top-barrier between the GaN Cap and the MOCVD SiN gate dielectric. Further, we do not currently know if the thickness and quality of the MOCVD SiN dielectric grown on the GaN Cap sidewall is the same as that grown on a planar surface. It is possible that the sidewall MOCVD SiN is thinner and/or of poorer quality than that grown in the gate recessed trench. Finally, as will be clearly demonstrated throughout the later sections

of this thesis, the NPDR transistor design enables exceptional control of surface-state induced dispersion. This actually acts to lower the breakdown voltage measured via the DCI technique. In dispersive devices, electrons are captured at the surface/interface trap states at high gate-drain voltage biases. As a result, many of the positively charged Si donor states in the back-barrier can now image on these negatively charged trap states in the access region, instead of all imaging at the drain-edge of the gate electrode. This expands the lateral distance over which the gate-drain voltage is dropped, reducing the peak E-Field of the device and enhancing the device's breakdown voltage. This is similar to what field plating does for transistors biased at high gate-drain voltages. However, unlike metal field plates, these trap states are likely too slow to respond at higher frequencies like the microwave and mm-wave ranges that III-N transistors are typically employed at. Thus, the interface/surface state induced dispersion can capture electrons and increase the breakdown voltage at the relatively low frequencies used during the DCI scan, but the breakdown voltage at higher frequencies is likely to be less than what is observed in the DCI scans. In the NPDR MISHEMT, the total number of trap states in the NPDR MISHEMT in areas of high E-Field is significantly reduced relative to a planar N-Polar MISHEMT (see Fig. 3.21). As a result, fewer electrons are likely trapped, and the NPDR transistor does not have its breakdown voltage enhanced like what occurs in planar transistors.

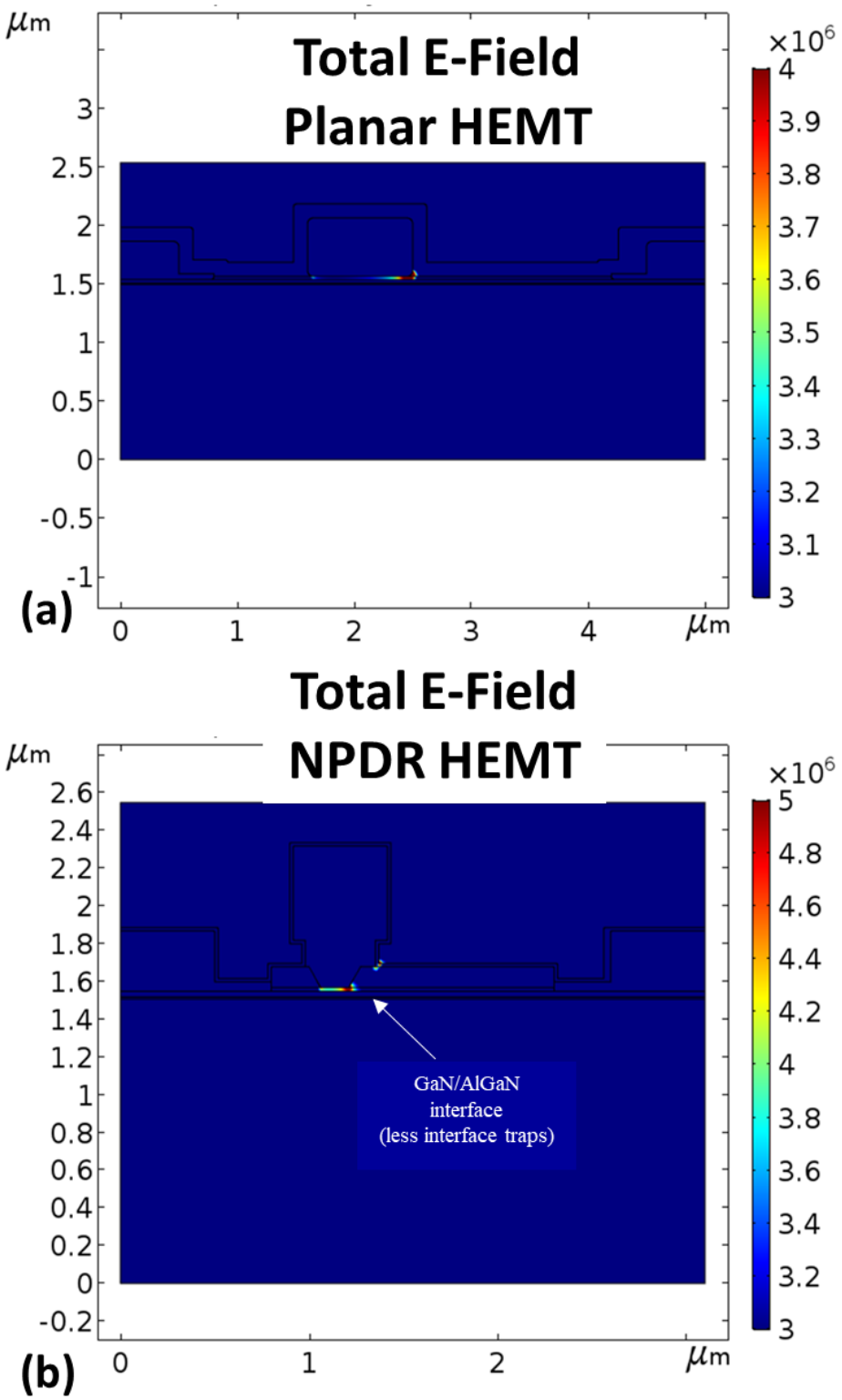

Fig. 3.20: Absolute value of E-Field from a 2-dimensional cross-section of a (a) planar N-Polar MISHEMT (no GaN Cap in access region) and (b) of a NPDR MISHEMT.

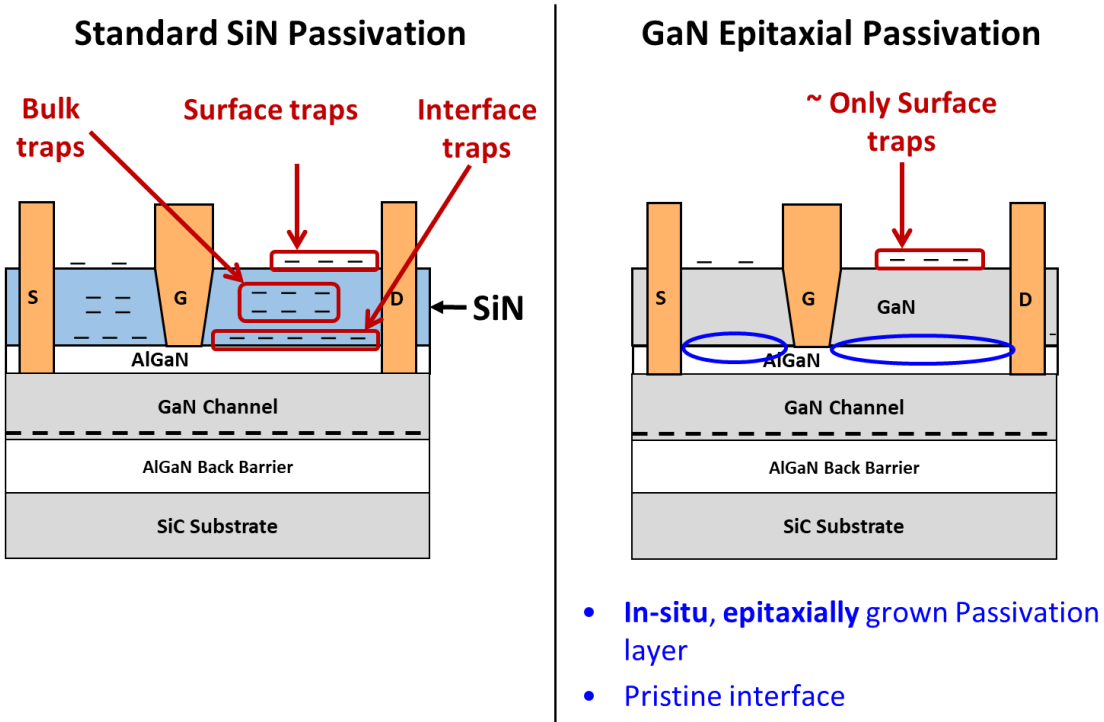

Fig. 3.21: Cartoon representation comparing a conventional *ex situ* PECVD SiN passivation with an *in situ* GaN Cap being used in the access regions for passivation. Because the GaN Cap is made of the same material as the GaN buffer and channel, no additional buffer traps are introduced. Further, because it is grown *in situ* and with no crystal lattice mismatch with the underlying N-Polar HEMT, there are significantly less interfacial defects as well.

All of the factors stated above contribute to the higher gate leakages and lower breakdown voltages seen in the NPDR MISHEMT relative to an equivalent planar N-Polar MISHEMT. During the DCI scans of the NPDR MISHEMT device, once the device reaches pinch-off the gate leakage increases rapidly until the gate leakage alone completely satisfies the 1 mA/mm boundary condition on the drain contact. This occurs prior to serious degradation of the semiconductor/gate dielectric interface, avoiding the onset of channel breakdown in the device and preventing the transistors from catastrophically failing. The relatively high voltages and conduction current through gate cap stack of the NPDR transistor do degrade the gate dielectric. However, they do not cause catastrophic failure and multiple DCI scans can be made on 1 device at an injection current of 1 mA/mm (the subsequent scans

do have lower breakdown voltages though). Because the breakdown event occurs at a V_{DS} less than where the semiconductor/gate dielectric interface fails at, it can be said that the device essentially breaks down prematurely.

Based on the findings of Chapter 2, it appears that a thicker MOCVD SiN gate dielectric would act to reduce the gate leakage and increase the breakdown voltage of the NPDR MISHEMT. To test this theory, DCI measurements with a 1 mA/mm injection current were also made on the 47.5 nm GaN Cap sample with the 9 nm MOCVD SiN gate dielectric thickness. A representative DCI scan for 47.5 nm GaN Cap sample with the thicker 9 nm MOCVD SiN gate dielectric is shown in Fig. 3.19 (b). The breakdown characteristics of the sample with 9 nm of MOCVD SiN is a little bit different than the sample with a thinner gate dielectric (Fig. 3.19 (a)). First, the breakdown voltages are higher overall than equivalent devices fabricated on the sample with a thinner gate dielectric. Additionally, the three terminal gate leakage at low V_{DS} ($\leq$ 5 V) is at the noise floor for the 9 nm MOCVD SiN sample whereas it is in the single μA/mm range for the relative to the 5 nm MOCVD SiN sample (Fig. 3.22). Moreover, roughly ¼ of all devices measured on the sample with a thicker gate dielectric experienced a channel breakdown event prior to gate breakdown. Although this is not a majority of devices, it is significantly higher than what was seen in the 5 nm MOCVD SiN sample which did not have a single device which demonstrated a channel breakdown prior to the gate breakdown event. Further, slightly over ½ of all NPDR MISHEMTs with the thicker gate dielectric failed catastrophically during the DCI scan, as opposed to 0 devices failing catastrophically in the 5 nm MOCVD SiN sample. All these characteristics indicates that the thicker gate dielectric helped increase the breakdown voltage and lower the gate leakage current relative to the NPDR MISHEMT with a thinner gate dielectric as predicted.

The processing issue mentioned earlier reduced the 2DEG density in the gate recessed region for the 9 nm MOCVD SiN sample, which could potentially contribute to the enhancement of breakdown voltage and lowering of the gate leakage. However, as stated earlier, the majority of the voltage drop occurs in the gate-drain access region, as does the peak in the E-Field. The piranha exposure did not affect the charge density in the GaN Cap access region. Thus, although the lower 2DEG density in the gate recess region may have contributed somewhat to the higher breakdown/lower gate leakage, it is very likely that the role played by the thicker MOCVD SiN gate dielectric is significantly more important. Moreover, the fact that only ¼ of the NPDR MISHEMTs with 9 nm of MOCVD SiN experienced a channel breakdown event suggests that there is perhaps a little more room to expand the breakdown voltage of the transistor through further thickening of the gate dielectric. How much more this would increase breakdown voltage is not certain, but as Chapter 2 illustrated, breakdown in these N-Polar MISHEMT designs likely is not at its peak until 100% of the devices experience a channel breakdown prior to gate breakdown when using a 1 mA/mm injection current density. At this point, it is the semiconductor/dielectric interface that limits the breakdown voltage, not the gate dielectric.

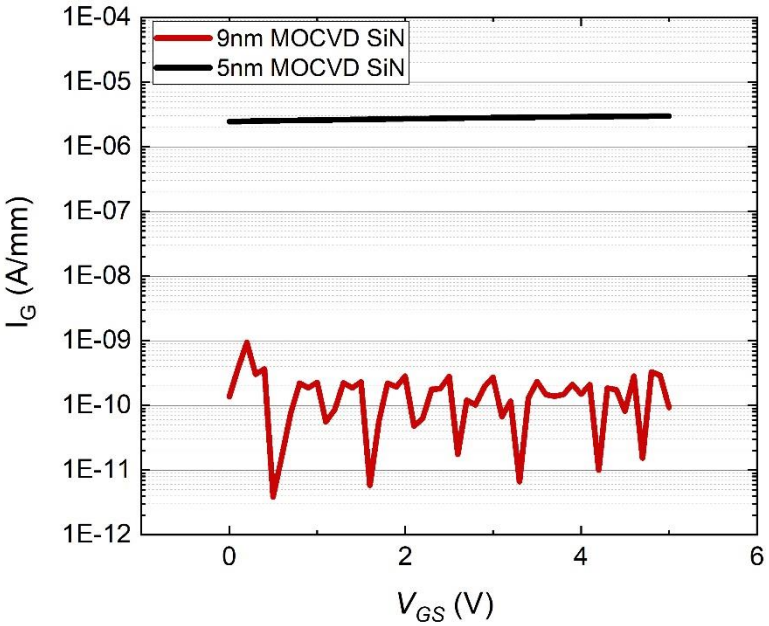

Fig. 3.22: Comparison of gate leakage at 2 V below the threshold voltage of the device for the two NPDR MISHEMTs with a 47.5 nm GaN Cap in the access regions and a 5 nm (black line) and a 9 nm (red line) MOCVD SiN gate dielectric.

Chapter 3.5 – Lateral Metal Coverage of GaN Cap Sidewall vs. Dispersion:

The PIV results from earlier clearly demonstrate that a 47.5 nm UID GaN Cap in conjunction with a σ_S *- = $1.65 \cdot 10^{13}$ cm^{-2} is enough to control dispersion very well when nominally ½ the GaN Cap sidewall is covered in gate metal. In this section of the thesis we examine how the placement of the gate metal relative to the GaN Cap sidewall affects the overall current dispersion of the device. The amount of metal coverage (or distance between the gate metal and GaN Cap sidewall) was determined via plan-view SEM (Fig. 3.23). DC-to-RF dispersion performance was investigated via PIV. All transistors were held at a relatively low stress quiescent bias equal to (V_{GSQ}, V_{DSQ}) = (-4 V, 7 V) and 200 ns gate pulses were applied along a 25 Ω load line in +1 V steps until a maximum V_{GS} of 0 V was reached. The pulsed current density at the knee was compared to the current density at the knee in a DC sweep to calculate dispersion percentage. Fig. 3.24 shows the percentage of current

dispersion at the knee for varying amounts of gate metal coverage (gap) on the drain-side GaN Cap. The amount of gate metal coverage (gap) is measured with respect to the base of the GaN Cap sidewall, not the top. Further, the GaN Cap sidewall in this sample is ~26 nm long on each side. In this device series, gate metal covers the entire GaN Cap sidewall on the source-side + an additional 50 nm of overlap on top of the source-side GaN Cap. This is to ensure that any dispersion seen in the device is strictly due to drain-side dispersion. When the gate recessed area and GaN Cap sidewalls are fully covered by gate metal, negligible dispersion is seen in the device (Fig. 3.24 (a)). With a ~ 5 nm average gap (gate metal and GaN Cap sidewall not perfectly sharp), a very small amount of drain-side dispersion is seen, but at these relatively low quiescent biases, the overall effect on current density at the knee voltage is still very small (Fig. 3.24 (b)). When the gap between gate metal and drain-side GaN Cap is $\geq$ 50 nm, very large dispersion is seen in the device (Fig. 3.24 (c)).

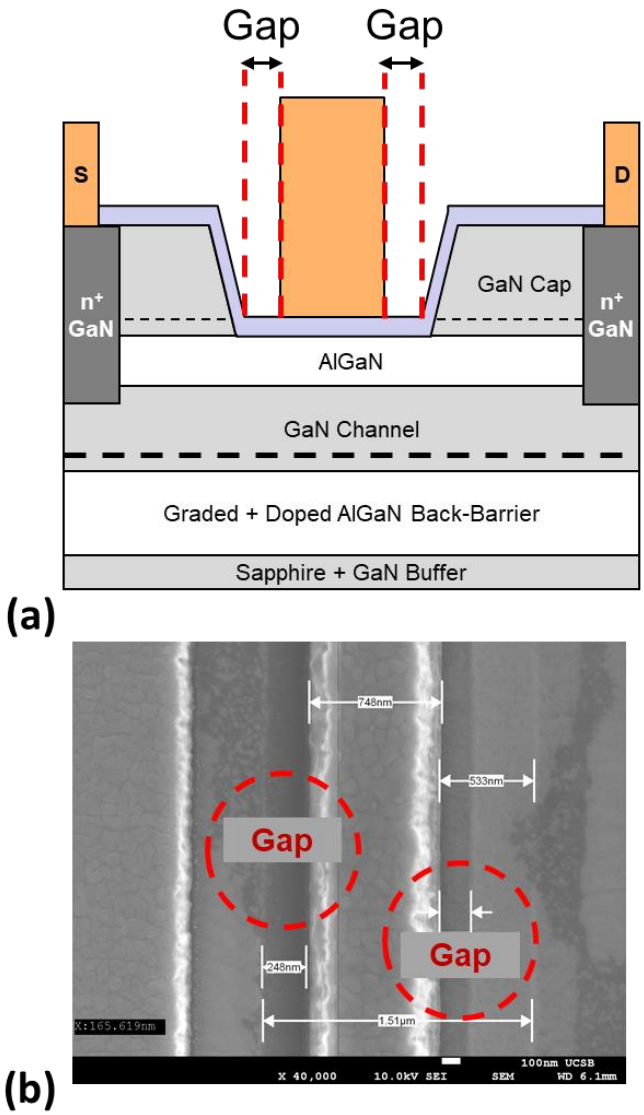

Fig. 3.23: (a) Gives a cartoon depiction of an NPDR MISHEMT which features gaps between the gate metal and the GaN Cap sidewalls. (b) Shows a plan-view SEM image of the actual device, illustrating how the actual gap between gate metal and GaN Cap sidewall is determined in this experiment.

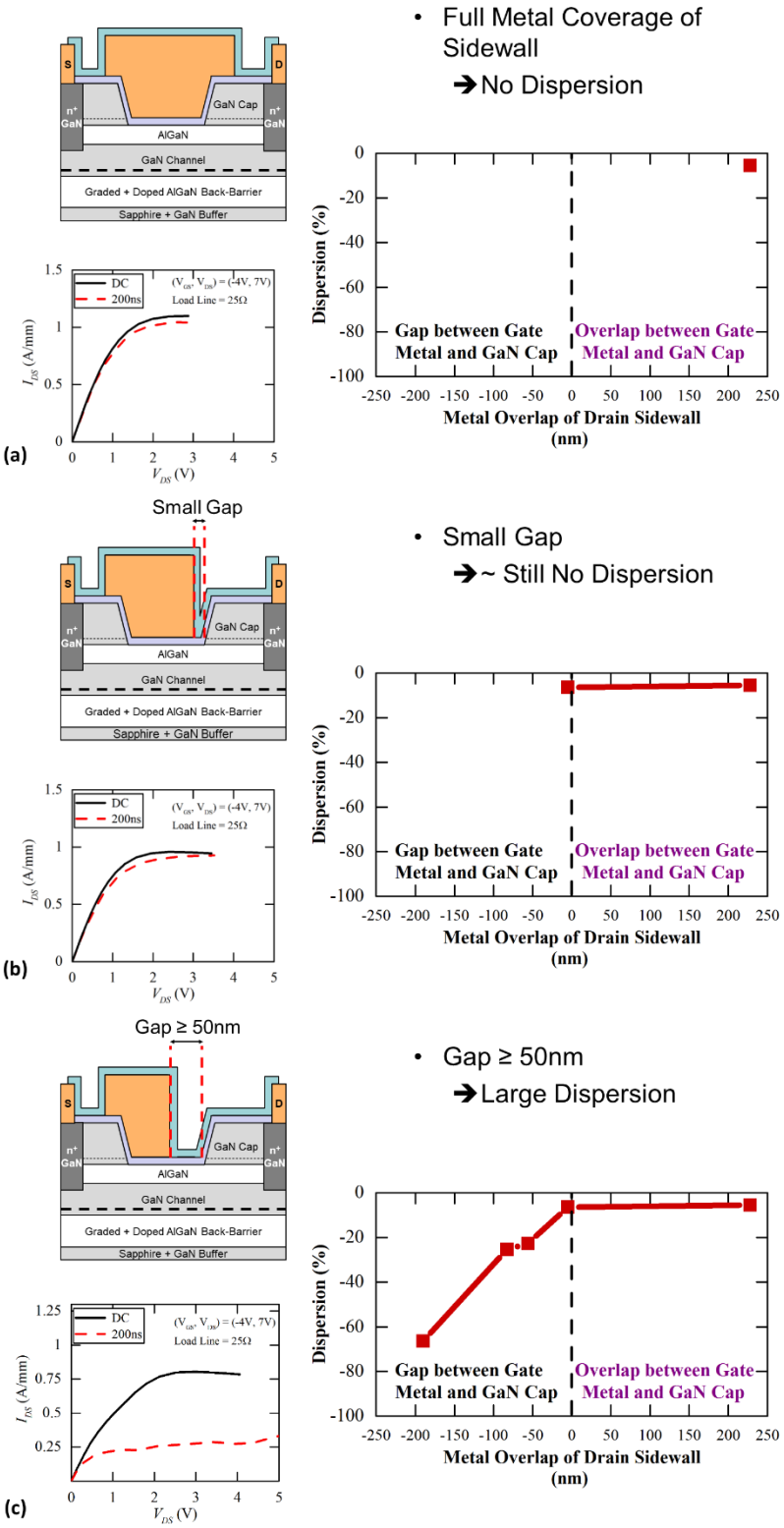

Fig. 3.24: Plots of dispersion vs. gate metal coverage (gap) between the drain-side GaN Cap sidewall and gate metal. V_{GS} was held at 2 V below the -2 V threshold voltage of the device (V_{th} = -2 V) and 200 ns gate pulses were applied along a 25 Ω load line in +1 V steps until a maximum V_{GS} of 0 V was reached. This was compared to the DC current to get the % dispersion.

Fig. 3.25 shows the percentage of current dispersion at the knee for varying amounts of gate metal coverage (gap) on the source-side GaN Cap. In this device series, gate metal covers the entire GaN Cap sidewall on the drain-side + an additional 50 nm of overlap on top of the drain-side GaN Cap. This is to ensure that any dispersion seen in the device is strictly due to source-side dispersion. Very similar results to what was seen for the drain-side experiment is observed. This is likely due to the relatively low stress quiescent biases used here. At higher source-drain quiescent biases, it is expected that the drain-side dispersion would increase, but the source-side dispersion would stay relatively constant.

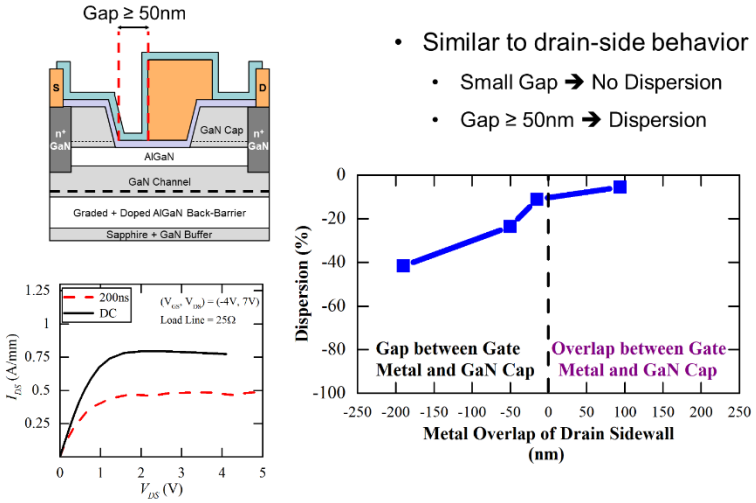

Fig. 3.25: Plots of dispersion vs. gate metal coverage (gap) between the source-side GaN Cap sidewall and gate metal. V_{GS} was held at 2 V below the -2 V threshold voltage of the device (V_{th} = -2 V) and 200 ns gate pulses were applied along a 25 Ω load line in +1 V steps until a maximum V_{GS} of 0 V was reached. This was compared to the DC current to get the % dispersion.

Fig. 3.24 and 3.25 indicate that surface-state induced DC-to-RF dispersion can be well controlled when the gate metal covers the entirety of the gate recessed region. Any gap at all seems to introduce some dispersion. An extremely small gap (~ 5 nm average) on the source-side may be tolerable, but a small increase in dispersion was witnessed in this case even with the relatively low stress quiescent bias voltages used in this experiment. This may be okay on the source-side where the E-Field should not change much with respect to the

source-drain quiescent bias voltage. A similar amount of dispersion was seen when a very small gap (~ 5 nm average) between the gate metal and drain-side GaN Cap sidewall was introduced. However, dispersion may increase with increasing source-drain bias voltage in this case, as the E-Field in the gate-drain access region will increase with increasing source-drain voltage. The PIV setup used in this study was unable to provide much more stringent quiescent bias voltages than what was explored here. Further study of what type of gate metal to drain-side GaN Cap sidewall gap is tolerable from a dispersion point of view is given in Chapter 5 though. Moreover, gaps $\geq$ 50 nm between the gate metal and GaN Cap sidewall on both the source and drain side are prohibitive and cause huge increases in DC-to-RF dispersion.

It should be noted that for some reason dispersion was seen even for low V_{DSQ} biases for all devices investigated on the 2 samples processed in this fabrication round (47.5 nm GaN Cap in this section, Chapter 4 and 110 nm GaN Cap discussed in Chapter 5). To correct for this, a thin 18 nm *ex situ* PECVD SiN passivation layer was added to the transistor which essentially fixed this problem. It is unclear why this *ex situ* PECVD SiN passivation had to be added for good dispersion control, as this was not necessary in any of the other samples investigated in this thesis, including samples that came from the same initial NPDR MOCVD growth. Regardless, the results have repeatably been reproduced in later sections of this thesis on NPDR MISHEMTs without any additional *ex situ* passivation layers. However, those sections did not involve as thorough an experimental series as that presented here, so this is what is presented.

Chapter 3.6 – Intro to the N-Polar Deep Recess (NPDR) MISHEMT

Summary:

In this chapter of the thesis a thorough description of the DC-to-RF dispersion phenomena in III-N transistors is given. Traditional solutions to this problem like application of an *ex situ* dielectric passivation layer in conjunction with field plating is detailed. An alternative epitaxial approach to dispersion reduction through the addition of an *in situ* UID GaN Cap in the access region is introduced. Past large signal results from Ga-Polar devices using this approach is covered. An explanation of the key device design advantages provided by the orientation of the polarization fields in N-Polar HEMTs for such a GaN Cap structure is discussed. Data confirming these advantages from capacitance voltage, gated TLM, and initial transistor devices fabricated on such a GaN Cap structure is discussed. A series of NPDR MISHEMT samples with different GaN Cap thicknesses is investigated to find the best GaN Cap thickness for use in a W-Band device. It is found that a 47.5 nm GaN Cap thickness is best amongst all the GaN Cap thicknesses explored in this chapter. Finally, the breakdown characteristics of the NPDR are compared to those measured on the planar N-Polar MISHEMTs of chapter 2. The reason for the lower breakdown voltages in the NPDR MISHEMTs is identified, and is found to be partially ameliorated by using a thicker gate dielectric.

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Chapter 4: Initial T-Gate Results on NPDR MISHEMTs

Chapter 4.1 – Performance Metrics for RF Power Amplifier Devices:

Transistors for RF amplification purposes should be capable of producing high large signal gain, high efficiencies, and high output RF powers at the frequency range of interest. A discussion regarding RF amplifier performance metrics is detailed in Chapter 1.2. That section is essentially repeated here for convenience.

Equations for describing an RF transistor amplifier's efficiency and output RF power at a particular frequency are given below

$$DE = \frac{P_{RF,out}}{P_{DC}} = \frac{P_{RF,out}}{V_{DC} \cdot I_{DC}} \tag{4.1}$$

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} = \frac{P_{RF,out}}{P_{DC}} \cdot \left(1 - \frac{1}{G}\right) = DE \cdot \left(1 - \frac{1}{G}\right) \tag{4.2}$$

$$P_{RF,out} = \frac{\left(V_{DSQ} - V_{knee}\right) \cdot I_{DSS}}{4} \tag{4.3}$$

In equation (4.1) DE = drain efficiency, P_{DC} is the mean dissipated DC power density, V_{DC} is the mean DC voltage, and I_{DC} is the mean DC current density. In equation (4.2) PAE = power-added efficiency, $P_{RF,out}$ = output RF power density, $P_{RF,\text{in}}$ = input RF power density, and G = power gain at the frequency of interest. In equation (4.3), V_{DSQ} = quiescent source-drain voltage bias, V_{knee} = knee voltage of the transistor's I-V curve, and I_{DSS} = saturation current density of the transistor.

The way in which a transistor amplifier is operated determines its Amplifier "Class". There are many different types of amplifier classes, but the three which will be talked about here are Class A, Class B, and Class AB. In Class A amplifiers, the device is biased

normally-on, at about half the peak-peak output current and half the peak-peak output voltage (Fig. 4.1). The main advantage of Class A operation is that it offers the highest linearity of all Amplifier Classes. However, because the transistor is always on, the peak efficiency Class A operation can achieve is only ≈ 50%. This is Class A's biggest drawback.

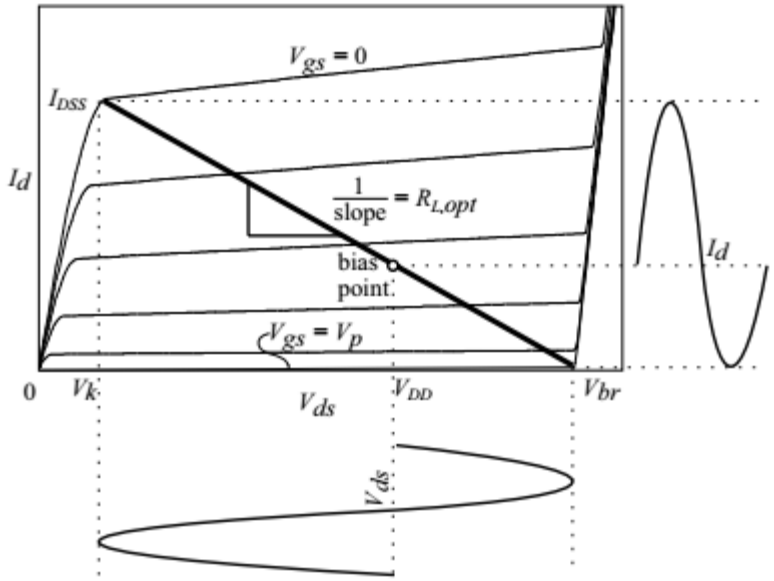

Fig. 4.1: Transistor operating in a Class A amplifier configuration with load line chosen for maximum power (Adapted from Mishra and Singh [1]).

In Class B amplifiers, the device is biased at pinch-off (Fig. 4.2). The conduction angle (total number of degrees out of 360 at which the device is conducting) is 180° in this class of amplifier, meaning that the individual transistor device conducts ½ the time, and is in the cut-off regime the other ½ of the time. Because the device is only dissipating DC power ½ the time, less DC power is consumed. This enables amplifiers of this class to theoretically achieve efficiencies as high as π/4 (~78.6%). The drawback of Class B is that it is less linear than Class A. Further, it requires that the transistor has high RF transconductance at or near pinch-off, which is not always the case. Class AB amplifiers are a compromise between Class A and Class B. Here, the conduction angle is $180^o < \theta < 360^o$. It is a compromise between

efficiency and linearity. Further, it relaxes the requirement of having high transconductance right at pinch-off.

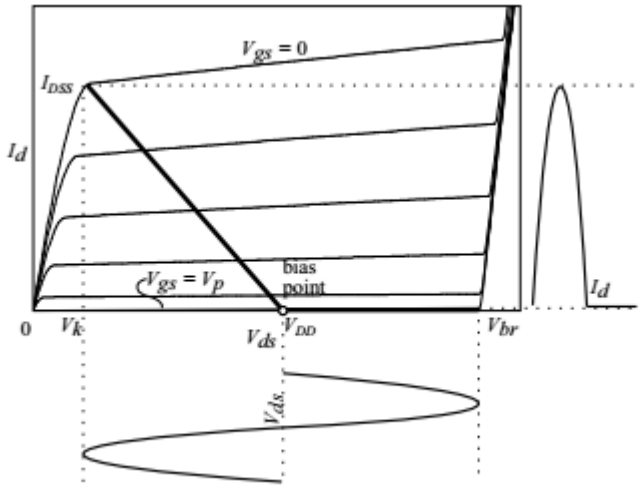

Fig. 4.2: Transistor operating in a Class B amplifier configuration (Adapted from Mishra and Singh [1]).

To achieve the highest possible drain efficiency allowable within any of the aforementioned Amplifier Classes, the ratio between a transistor's breakdown voltage and RF knee voltage should be high. A load line which maximizes power delivered to the load typically will cross, or at least come close to, the knee of the transistor's I-V. Therefore, the DC power dissipated at voltages below the knee voltage do not contribute to $P_{RF,out}$, and thus should be minimized for high drain efficiencies. Moreover, having a higher breakdown voltage allows the device to be biased to higher quiescent source-drain voltages, increasing the total $P_{RF,out}$ and reducing the hit taken to *DE* from the power dissipated below the knee voltage. Further, the breakdown voltage sets the limit on the peak RF output power that can be expected from a given transistor device. For a Class A amplifier, $P_{RF,out,Max}$ is given by equation 4.4.

$$P_{RF,out,Max} = \frac{\left(V_{DS,Br} - V_{knee}\right) \cdot I_{DSS}}{8} \tag{4.4}$$

An inherent requirement for high *DE* in III-N transistors is the ability to control DC-to-RF dispersion. The V_{knee} and I_{DSS} that matter in the above equations are the RF values at the application frequency. Drain-side dispersion will increase the RF V_{knee}, which will decrease both the maximum achievable RF output power as well as the drain efficiency of the device. Source-side dispersion will decrease the RF I_{DSS} and decrease the $P_{RF,out,Max}$. Therefore, controlling dispersion at the application frequency is critical for device performance.

Power added efficiency (equation 4.2) takes into account not only the dissipated DC power, but also the input RF power required for a given output RF power. Because of this it gives a more accurate depiction of the transistor's actual overall efficiency within the circuit. As equation 4.2 shows, in order to achieve the highest possible *PAE* for a given Amplifier Class, the transistor amplifier must have both high drain efficiency and high power gain at the application frequency. *DE* is explained in the previous paragraph. Power gain *G* is related to how much an input RF signal will be amplified by the transistor amplifier at a particular frequency. During load pull measurements here at UCSB, the Maury Microwave software provides information on the transducer gain G_T of the transistor at each of the quiescent bias points. This transducer gain is related to the power gain of the transistor via equation 4.5.

$$G = 10^{\frac{G_T}{10}} \tag{4.5}$$

The transducer gain itself is related to (but not necessarily equal to) the unilateral gain of the transistor amplifier *U*. A good figure of merit for unilateral gain is the maximum frequency of oscillation, or f_{max} of the transistor (equation 4.6). This represents the frequency at which the unilateral gain becomes unity.

$$f_{max} = \frac{\frac{gm_{ext}}{2\pi * \left(C_{gs} + C_{gd}\right)}}{\sqrt{\frac{4}{R_{ds}} * \left(R_g + R_s + R_i\right) + 8\pi * f_T * C_{gd} * \left(2 * R_g + R_s + R_i\right)}} \tag{4.6}$$

As an amplifier is meant to provide gain/amplify an incoming signal, the f_{max} of the transistor amplifier signifies the upper limit at which the transistor can behave as an amplifier. For reasonable power gains, the transistor amplifier must operate well below its f_{max}. Another useful figure of merit is the short-circuit current cut-off frequency f_T.

$$f_T = \frac{gm_{ext}}{2\pi * \left(\left(C_{gs} + C_{gd} \right) * \left(1 + \frac{R_s + R_d}{R_{ds}} + C_{gd} * g_m * (R_s + R_d) \right) \right)} \tag{4.7}$$

Chapter 4.2 – Introduction to T-Gate Device Design:

In this work, the goal is to build a N-Polar transistor which can simultaneously achieve high large signal gain, high efficiencies, and high RF output power at the W-Band range of frequencies (77-110 GHz). Achieving high gain at these frequencies is a struggle in the III-N system. Although the electrons which comprise the 2DEG in GaN can achieve relatively high room temperature mobilities of ~2,100 $V \cdot s^{-1} \cdot cm^{-2}$, this is still much lower than that which can be achieved by InP and (In)GaAs HEMTs (Table 4.1) [2]. As such, the fabricated transistor design must be optimized to get as a high an f_{max} as possible in order to achieve reasonable gain at W-Band. An important parameter which must be minimized to obtain a high f_{max} is the gate resistance term R_G in equation 4.6. DC R_G is given by equation 4.8

$$R_{G,DC} = \rho \cdot \frac{W_G}{Gate\ Area} \tag{4.8}$$

The relationship between DC and RF gate resistance is given by:

$$R_{G,AC} = \frac{R_{G,DC}}{3} = \rho \cdot \frac{1}{3} \cdot \frac{W_G}{Gate\ Area} \tag{4.9}$$

$R_{G,AC}$ is 1/3 the DC gate resistance due to the distributed nature of charges along the gate when the device is biased [3].

Material	Bandgap (eV)	ε	E_c (MV/cm)	μ at 300K ($cm^{-2}V^{-1}s^{-1}$)	v_{sat} (v_{peak}) (cm/s)	2DEG density (cm^{-2})
Si	1.1	11.7	0.3	1500	1 (1)	$<5x10^{12}$
InP	1.35	12.5	0.5	5400	1 (2.3)	$< 5x10^{12}$
GaAs	1.43	13.1	0.4	8,500	1 (2.1)	$<5x10^{12}$
4H-SiC	3.3	9.7	3	700	2 (2)	NA
GaN	3.4	9.5	**3.3**	**2100* (2DEG)**	**1.3 (2.5)***	**~1-2e13**

Table 4.1: Comparison of material parameters relevant to RF electronic devices across several different semiconductors. (* the peak saturation velocity of GaN was predicted theoretically and has not been experimentally demonstrated) [2].

As equation 4.9 suggests, one way to reduce $R_{G,AC}$ is to make transistor devices with smaller gate widths (W_G) [4]. This will minimize the distance over which the RF gate signal must travel to reach the ends of the gate fingers, thus reducing overall gate resistance. Another way to minimize gate resistance is to maximize the area of the gate. This can be difficult to do without increasing the gate length L_G of the transistor when using a rectangular i-gate design (Fig. 4.3 (a)). However, a T-Gate design such as that shown in Fig. 4.3 (b) makes this much more feasible. A T-Gate essentially consists of two sections, a "foot" gate and a "top" gate. The foot gate defines the electrical gate length (L_G) of the transistor. It can be kept short in order to minimize the gate length and therefore the intrinsic capacitance C_{gs} of the transistor. The equations for f_T and f_{max} reveal that this intrinsic capacitance must be kept low in order to

get the highest possible gain out of the transistor. (However, C_{gs} cannot be made too low, otherwise the gate will lose electrical control of the channel, causing a drop in R_{ds} and a subsequent drop in gain). The top gate can be made to have a large cross-sectional area to minimize AC R_G. Together, the foot and top gates allow for "the best of both worlds" and enable much higher power gain than what would be possible with a rectangular i-gate with dimensions of either the foot or top portions of the T-Gate. One drawback of the T-Gate design is that the large top gate will capacitively couple to other portions of the transistor (Fig. 4.4). Increasing the top-gate length will only increase this capacitance. Further, the skin effect must be taken into consideration at high frequencies. That is, the AC current density in a conductor is concentrated near the surface of the conductor and decays exponentially towards the center of the conductor. The skin depth δ is the distance from the conductor surface to the point where the AC current density decreases to 1/e of its value at the surface. Here e is the base of the natural logarithm. The simplified expression for skin depth is given in equation 4.10 [5].

$$\delta = \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu}} \tag{4.10}$$

ρ is the gate metal resistivity, f is the signal frequency, and μ is the metal permeability. Gold is the primary metal used to construct the T-Gates in this work. The resistivity of Au is $\approx 2.24 \cdot 10^{-8}$ [6]. At 94 GHz, the skin depth of Au is approximately 245 nm. Thus, any top gate length > 500 nm is essentially just increasing the total capacitance of the device without actually decreasing the AC gate resistance.

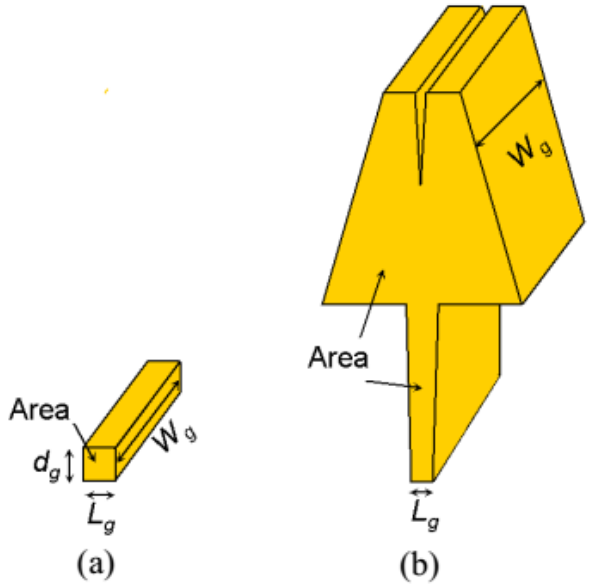

Fig. 4.3: (a) A rectangular I-gate structure whose relatively small cross-sectional area leads to higher gate resistances. (b) A T-Gate structure with the same gate length as the I-gate, but a much larger cross-sectional area, leading to a much lower gate resistance (adopted from [4]).

Making a taller foot gate height can minimize this capacitance however. Matthew Guidry simulated the capacitance between the top gate and access region 2DEG with respect to foot gate height in COMSOL. He found that this capacitance begins to saturate at roughly 200 nm above the access region (Fig. 4.5). This was the target foot gate height for all T-Gate devices discussed in this thesis.

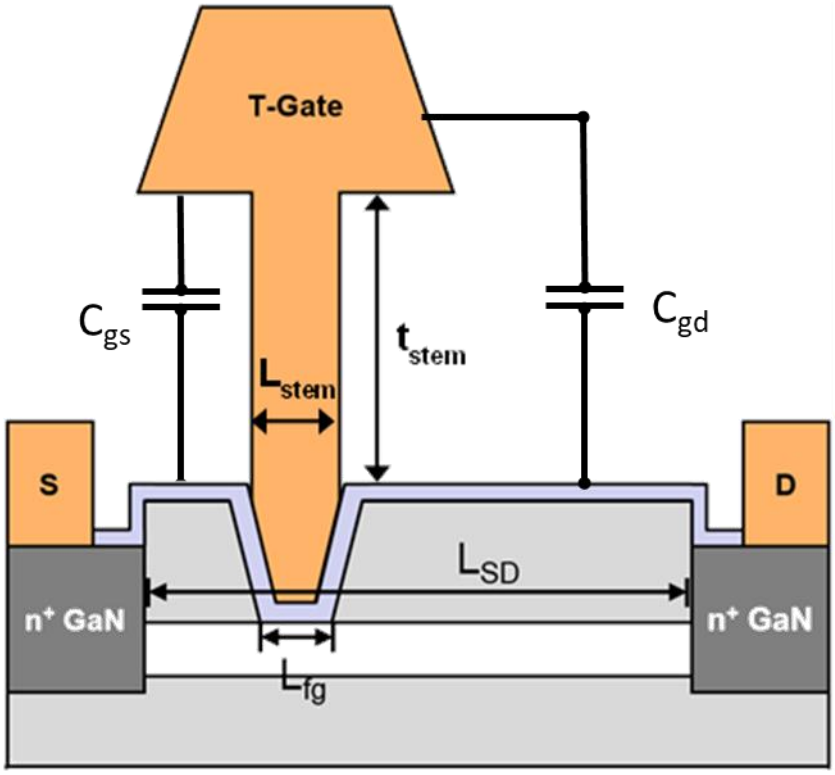

Fig. 4.4: NPDR MISHEMT T-gate structure depicting some of the additional capacitances the T-gate structure introduces.

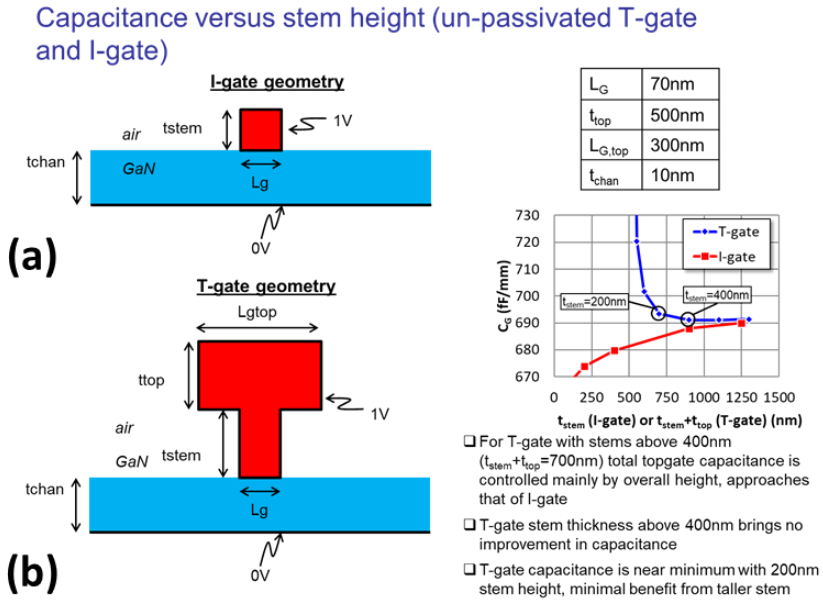

Fig. 4.5: Comparison of the simulated gate to channel 2DEG capacitance for a N-Polar transistor with a mechanical gate length of 70 nm in (a) an i-gate structure (red line) and (b) a T-gate structure with respect to the stem height of the gate metal. The gate to 2DEG capacitance drops rapidly with increasing stem height until a stem height of around 200 nm. At around 400 nm, the gate metal to 2DEG capacitance is roughly equivalent between an i-gate and T-gate structure.

Chapter 4.3 – T-Gate Fabrication Procedure + Initial T-Gate Results:

T-Gates were fabricated on all 4 GaN Cap thickness samples from Chapter 3.3. However, unless otherwise stated, only T-Gates fabricated on the 47.5 nm GaN Cap will be discussed here.

Growth Procedure:

Samples were grown via MOCVD on miscut sapphire substrates [7]. Growth conditions are similar to that reported in [7]. The epitaxial structure is shown in Fig. 4.6 (a). Devices contain a 5 nm MOCVD SiN_x gate dielectric, a 47.5 nm UID GaN cap (access regions only), a 2.6 nm $Al_{0.27}Ga_{0.73}N$ top barrier, a 12 nm UID GaN channel, a 0.7 nm AlN interlayer, a 10 nm UID $Al_{0.38}Ga_{0.62}N$ spacer layer, and a Si-doped graded AlGaN back-barrier. Band diagrams generated with a one-dimensional self-consistent Schrödinger-Poisson solver [8] for the gate recess and GaN cap regions are shown in Fig. 4.6 (b) and (c) respectively.

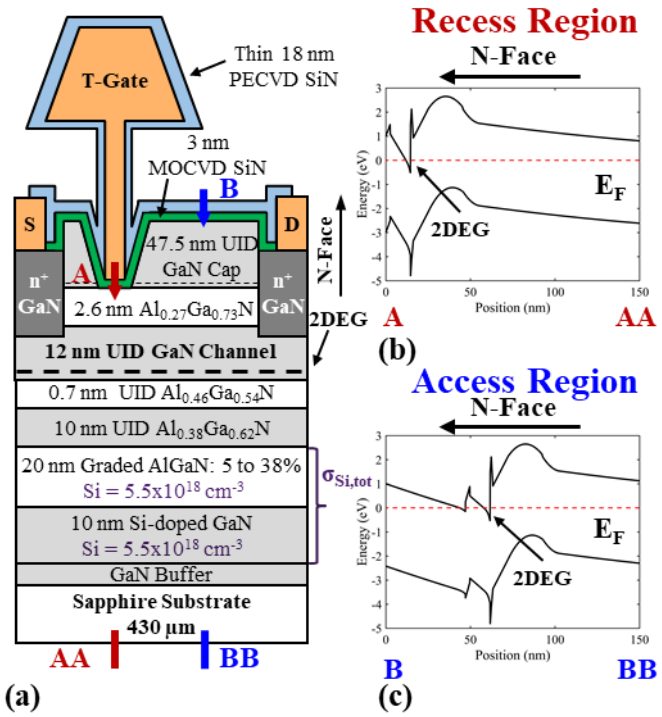

Fig. 4.6: Fig. 1. (a) Cross-section of nominal NPDR MISHEMT device structure (not to scale). Energy band diagram at equilibrium in the (b) gate recessed region and (c) the access region. Simulations assume a Schottky gate structure with a pinning position of 1 eV [8] to eliminate the complexities associated with the MIS interface.

Fabrication Procedure:

The fabrication procedure is nearly identical to the process detailed in Chapter 3.3 for i-Gates. The only difference is that a 2-step electron beam lithography (EBL) is used to write the T-Gates, as opposed to the 1-step EBL for i-Gates. Nonetheless, the fabrication procedure is provided here for convenience (Fig. 4.7).

Due to the anisotropic transport properties of N-polar HEMTs grown on vicinal substrates, all devices are designed such that source-drain conduction occurs in the high mobility direction parallel to the direction of substrate miscut [7]. The subsequent T-gate device fabrication procedure is similar to that reported in [9] with alterations due to the presence of the UID GaN cap. Prior to the n^+ GaN regrowth, a BCl_3/SF_6 inductively coupled plasma (ICP) dry etch with a selectivity of 17 to 1 is implemented to remove the UID GaN

cap with respect to the $Al_{0.27}Ga_{0.73}N$ top barrier [10]. An additional unselective BCl_3/Cl_2 etch is then performed to remove the $Al_{0.27}Ga_{0.73}N$ top barrier prior to n^+ GaN regrowth. The n^+ GaN and high temperature MOCVD SiN_x dielectric regrowth steps follow from [9]. After dielectric regrowth, electron-beam-lithography (EBL) is used to define the gate recessed region of the transistor, followed by another selective BCl_3/SF_6 etch to form the recessed trench. The sample is then put back in the MOCVD reactor for high temperature SiN_x gate dielectric regrowth followed by a BCl_3/Cl_2 reactive ion etch for mesa isolation. Realignment to the recessed trench is performed in the EBL system and a 2-step EBL process is used to write T-gates into the recessed trench. T-gates with a 200 nm stem height are then formed following a 30/500 nm Ti/Au electron-beam evaporation and lift-off procedure. Ohmic contact and pad formation follow. Finally, for some reason, samples from this fabrication run were somewhat dispersive even at low V_{DSQ} biases for all investigated MISHEMTs (same fabrication run as Chapter 3.4). To correct for this, a thin 18 nm PECVD SiN passivation layer was added which essentially fixed this problem.

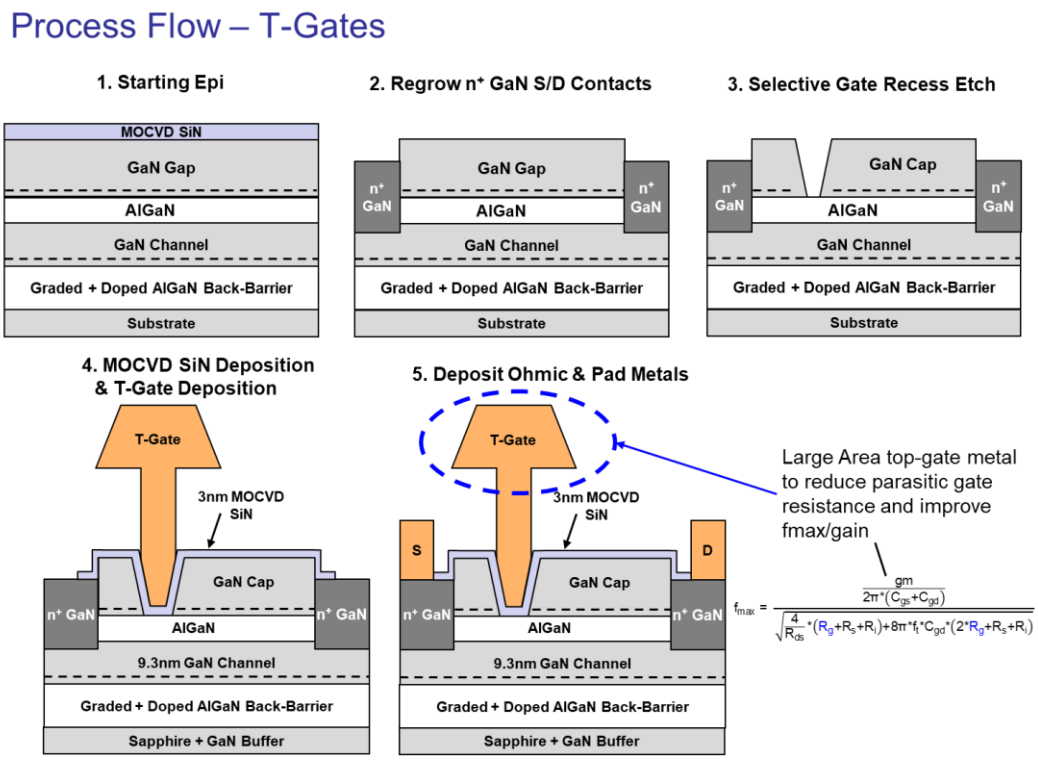

Fig. 4.7: Process flow for NPDR T-gate MISHEMT structure.

Comment on Reported Dimensions of this Chapter:

It should be noted that the nominal gate lengths reported for the transistors of this chapter do not match with their actual real physical dimensions. Table 4.2 shows both the nominal and actual gate recess dimensions measured via plan-view SEM for the 47.5 nm GaN cap sample for multiple devices. Clearly, a large discrepancy is seen. However, analogous SEM measurements were not made for each device reported on in this chapter. As such, only the targeted/nominal gate recess dimensions are mentioned in this chapter, but it should be kept in mind that the actual foot gate lengths are shorter than the nominal dimensions.

Nominal Gate Recess (nm)	Real Gate Recess (nm)
50	16
75	38
100	62
125	99
150	138
150	130

Table 4.2: Comparison between the target gate recess dimensions and the actual gate recess dimensions (as measured from plan-view SEM).

NPDR vs. Planar T-Gate MISHEMTs – Elimination of Source Choke:

Initial T-Gate results on the NPDR samples show a very large increase in DC extrinsic transconductance relative to planar N-Polar MISHEMTs which featured similar overall epitaxial and device dimensions (Fig. 4.8). This is most likely due to the enhanced conductivity in the access regions due to the presence of the GaN Cap in the NPDR design, as discussed in Chapter 3. This lowers the extrinsic R_s term in the equation for extrinsic transconductance (eq. 4.11), making the measured extrinsic transconductance closer to the intrinsic transconductance of the transistor.

$$gm_{ext} = \frac{gm_{int}}{1 + R_S \cdot gm_{int}} \tag{4.11}$$

Moreover, in planar III-N HEMTs it has been shown that the dynamic source resistance increases substantially at higher current densities [11]. This leads to a reduction in extrinsic transconductance at higher current densities. Fig. 4.8 shows that the addition of the GaN Cap in the access regions helps to reduce the dynamic source resistance at high current densities

and leads to a higher transconductance across a larger range of current densities relative to a planar N-Polar MISHEMT of similar epitaxial and device dimensions. From equation 4.7 and 4.8, this should lead to a higher f_T and f_{max} across a broader range of current densities relative to a planar N-Polar MISHEMT as well (see next chapter for data). Further, as a first approximation, the large signal linearity of the transistor is proportional to the square root of f_T. Thus, the broader transconductance provided by the NPDR MISHEMT should also lead to a higher degree of large signal linearity as well.

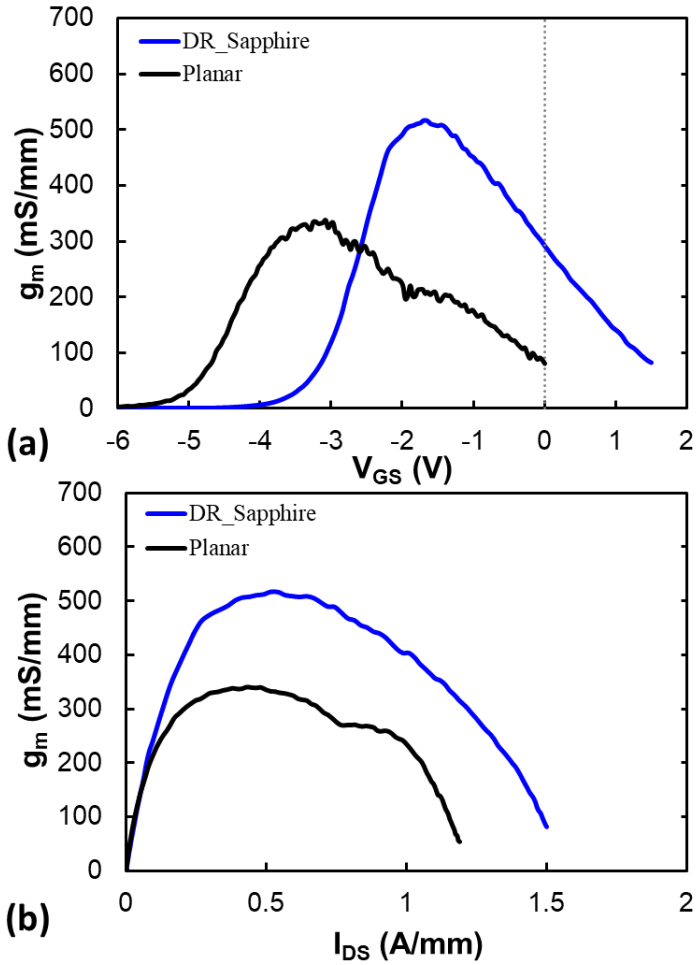

Fig. 4.8: (a) DC extrinsic transconductance vs. V_{GS} comparison between a planar N-Polar MISHEMT and a N-Polar Deep Recess MISHEMT. (b) DC extrinsic transconductance vs. current density in a planar N-Polar MISHEMT and a NPDR MISHEMT.

Chapter 4.4 – Full Gate Metal Coverage of Sidewall vs. No Gate Metal on Sidewall:

Multiple T-Gate device designs were fabricated on these set of samples. The i-gate study of Chapter 3.5 indicated that even relatively small gaps between the gate metal and GaN Cap sidewall ($\geq$ 50 nm) led to large amounts of DC-to-RF dispersion in pulsed IV (PIV) measurements even when a thin $\approx$ 18 nm PECVD SiN was added to the transistor. As a result, initial investigations of NPDR MISHEMTs with T-Gates focused on two main device designs. The "Flush" design is constructed such that the foot gate metal is nominally flush with the bottom edge of the UID GaN cap sidewall on each side. In the "Full" design the foot gate metal nominally covers the entirety of both the source and drain GaN cap sidewalls (26 nm of lateral metal overlap).

DC and Pulsed IV Results:

DC and pulsed IV characteristics were nearly identical for the two device designs (Fig. 4.9). A small amount of source-side dispersion was seen in both sets of devices. However, this dispersion was relatively small and did not increase dramatically with increasing drain bias. This demonstrates the effectiveness of the GaN cap in controlling dispersion with or without full metal coverage of the GaN cap sidewall, so long as the gate recessed region is covered in gate metal.

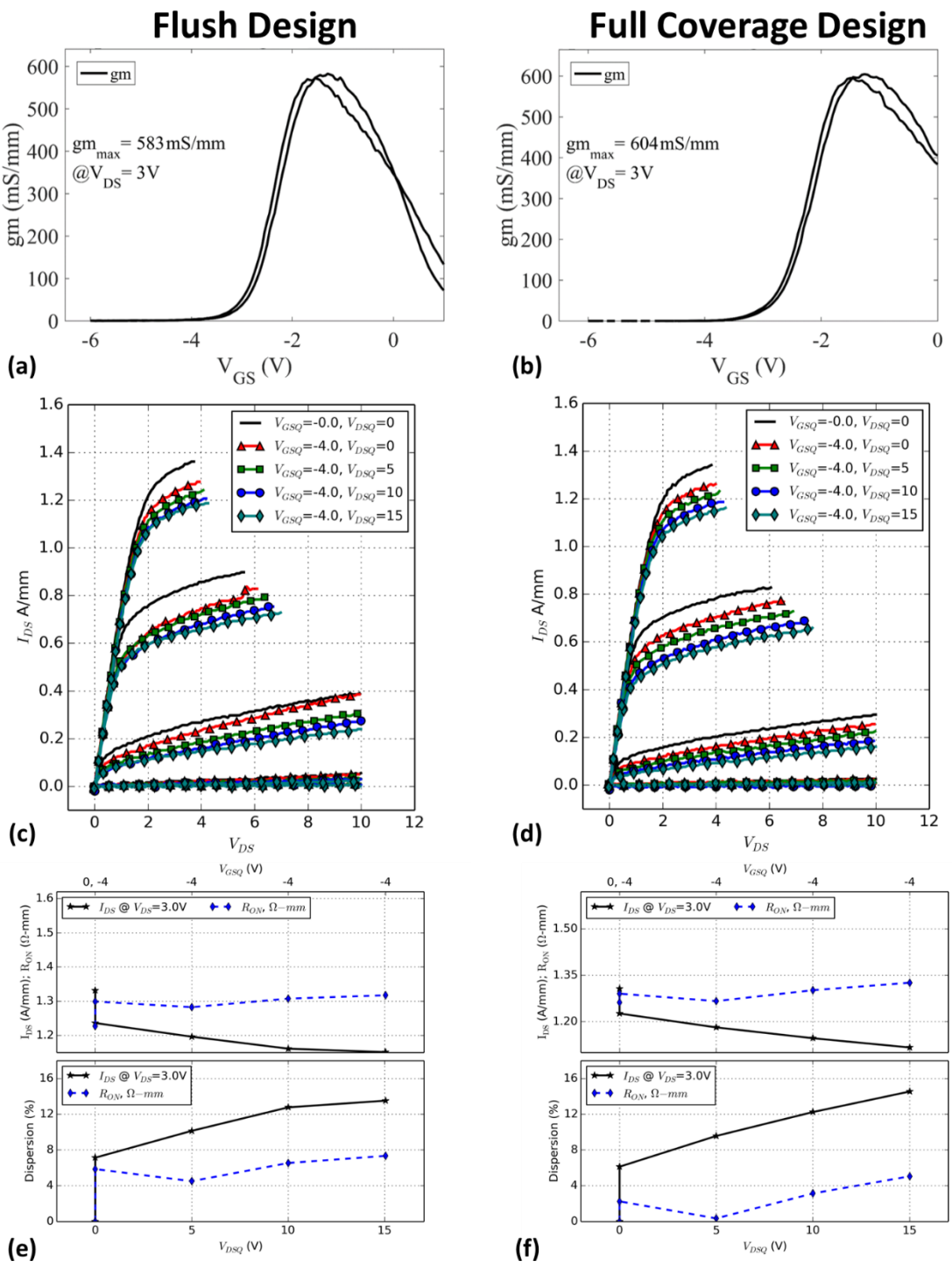

Fig. 4.9: Comparison of the DC and PIV performance for two NPDR MISHEMTs. The data on the left-hand side comes from an NPDR MISHEMT where the gate metal nominally fills the floor of the gate recessed trench but does not overlap either the source or drain GaN Cap sidewalls ("Flush" design). The plots on the right-hand side come from an NPDR MISHEMT where the gate metal nominally fills the entire recessed trench (both the floor and the sidewalls of the GaN Cap on the source and drain sides), but contains nominally no additional field plating over the tops of the GaN Cap access regions. Both devices have a nominal L_{GS} = 226 nm, L_G = 125 nm, L_{GD} = 1.149 μm, and a W_G = 2 x 75 μm.

RF Small and Large Signal Comparison:

The main tradeoff between these two device designs is the amount of additional capacitance introduced by the foot gate metal coverage of the GaN cap sidewall in the Full metal coverage with respect to the Flush design. COMSOL capacitance simulations indicate that this additional metal coverage nearly doubles the fringing capacitance of the Full metal coverage transistors compared to the Flush devices at a V_{DS} = 0 V (Fig. 4.10). This capacitive penalty leads to HEMTs with Full gate metal coverage to have an effective foot gate length (L_{FG}) which is 25 nm greater than a Flush transistor with the same mechanical L_{FG}. This is reflected in the small signal RF performance of the two device designs (Fig. 4.11), where the f_T of the Full metal coverage transistors is consistently 13-15 GHz lower than the corresponding Flush transistor with the same L_{FG}. The f_{max} of the Full metal coverage device was also lower than the corresponding Flush transistor for devices with the same L_{FG} [12].

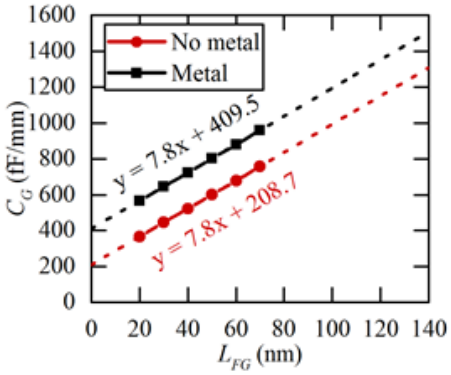

Fig. 4.10: COMSOL capacitance simulations (performed by Matthew Guidry) for the two NPDR MISHEMTs discussed in this section. The "Flush" device simulations is in black, whereas, the "Full" Metal Coverage device is in red [13].

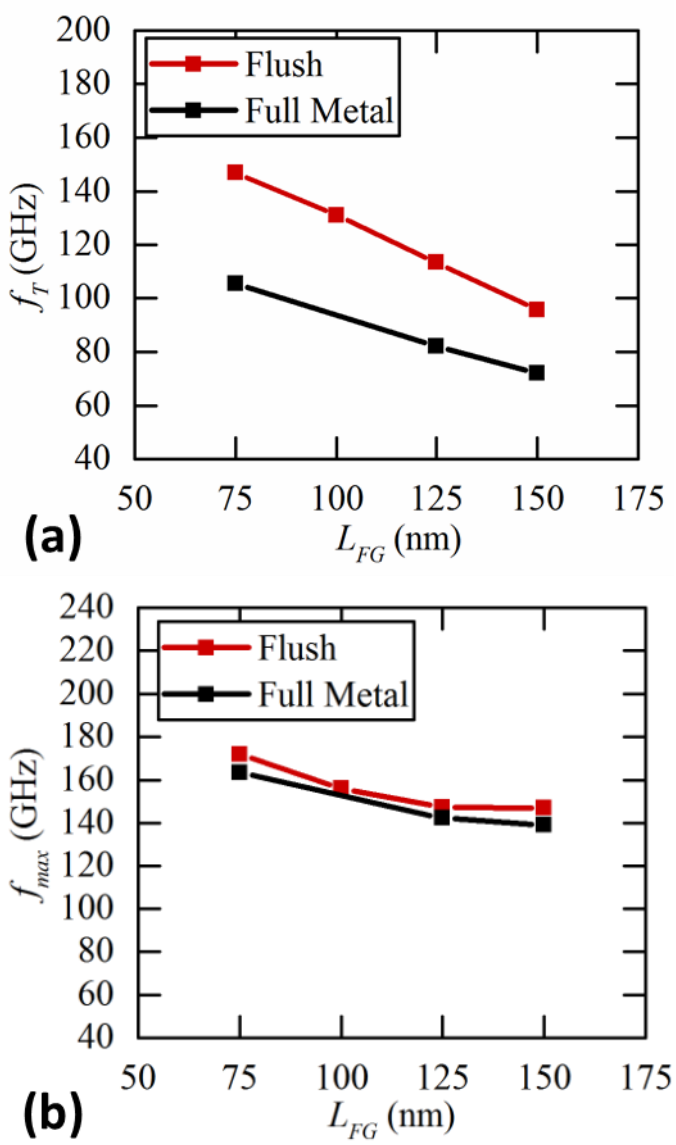

Fig. 4.11: (a) Peak de-embedded f_T vs. foot gate-length for the Flush device (red line) and Full Metal Coverage device (black line). (b) Peak de-embedded f_{max} vs. foot gate-length for both devices as well. All devices had an L_{GS} = 226 nm, L_{SD} = 1.5 µm, and a W_G = 2 x 75 µm.

The benefit of the sidewall capacitance/metal coverage is, however, that it relaxes the electric field at the drain edge of the gate. This advantage was evident during large signal measurements. Uncooled continuous wave power performance at 10 GHz was determined using a Maury Microwave tuner-based load pull system. Transistors were biased at class AB with an $I_{DS,Q}$ of 100 mA/mm in each case. Power sweep data for two comparable Flush and

Full metal coverage MISHEMTs are shown in Fig. 4.12. Power density scaled well with drain bias for both sets of transistors (Fig 4.12 (a)). An estimate of the RF current swing in the devices can be made by taking the derivative of equation 4.3 with respect to the quiescent source-drain bias voltage. The resultant equation for RF current density is shown here for convenience.

$$I_{RF} = 4 \cdot \frac{\partial P_{RF,out}}{\partial V_{DSQ}} \tag{4.12}$$

Using equation 4.12, both designs yield an estimated RF current swing of over 1.5 A/mm for each design. However, Flush transistors had consistently higher gate leakage and failed at lower drain biases than did transistors with Full metal coverage (Fig. 4.12 (b)). The ability to apply higher drain biases to Full metal coverage devices allowed them to achieve significantly higher power densities at X-Band than Flush MISHEMTs with similar dimensions (Fig. 4.13).

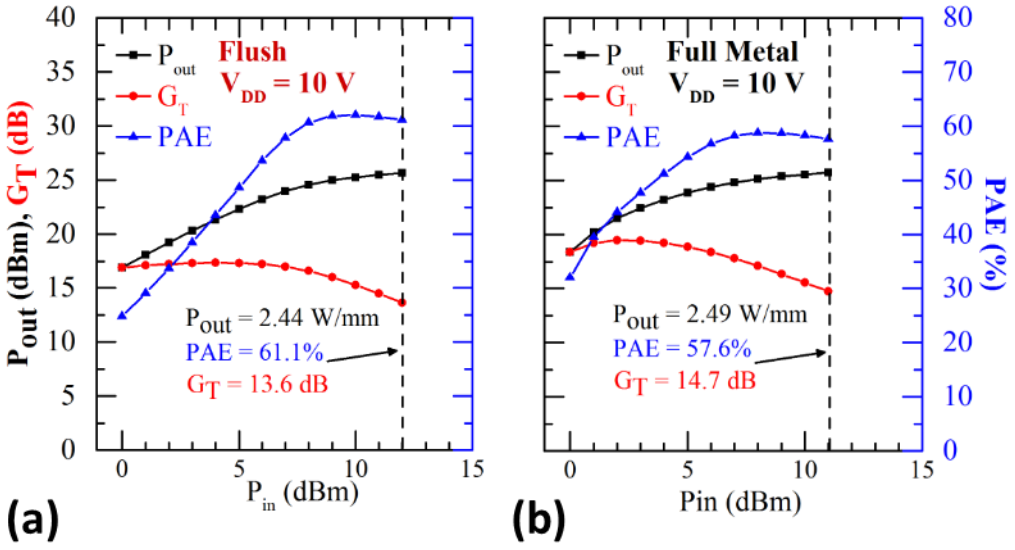

Fig. 4.12: 10 GHz load pull power sweeps at an I_{DSQ} = 100 mA/mm on MISHEMTs with (a) no sidewall metal, and with sidewall metal (b). Device dimensions are W_G = 2 x 75 µm, L_G = 125 nm, and L_{SD} = 1.5 µm for both transistors.

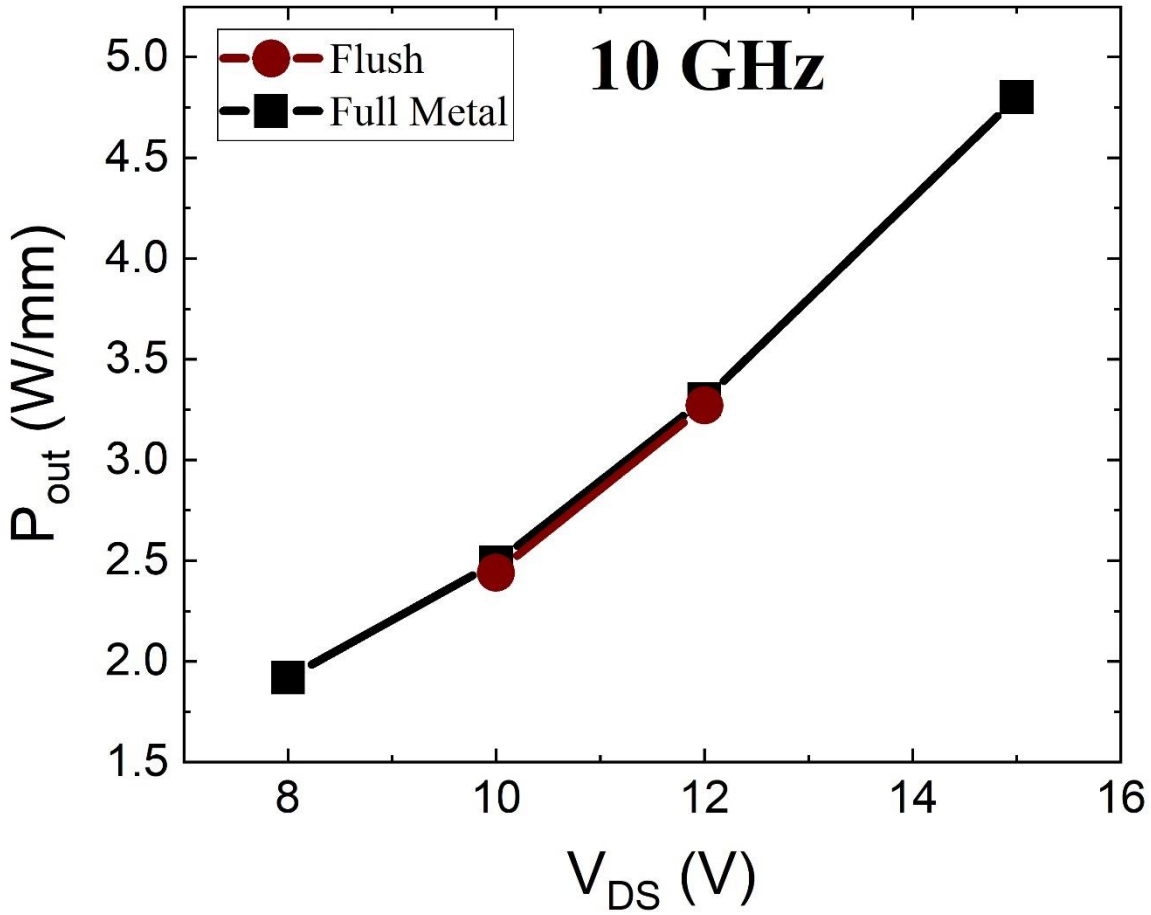

Fig. 4.13: Maximum RF output power density vs. V_{DS} bias for both the Flush and Full Metal Coverage designs. Both transistors have an L_{SD} = 226 nm, L_G = 125 nm, L_{GD} = 1.149 µm, and a W_G = 2 x 75 µm.

Uncooled continuous wave (CW) power performance at 94 GHz was then measured on a Full metal coverage transistor with a 2 x 25 µm gate width (W_G), nominal 100 nm foot gate length (defined as the physical length at the base of the GaN Cap recess), 450 nm top gate length, 226 nm source-gate spacing (L_{GS}), and 1.5 µm source-drain spacing (L_{SD}). Measurements were made on another Maury Microwave tuner-based load pull system [13]. The Full metal coverage device was biased at class AB with an $I_{DS,Q}$ of 350 mA/mm (Fig. 4.13). At a V_{DSQ} = 8 V, a peak power density of 1.52 W/mm was measured at a gain compression of 1.82 dB, with a maximum *PAE* of 12.35% (Fig. 4.13 (a)). A peak power

density of 1.92 W/mm with an associated power added efficiency (*PAE*) of 13.6% was measured at a quiescent drain bias of 10 V (Fig. 4.13 (b)). At a V_{DS} = 16 V, a very high power density of 3.0 W/mm was measured with an associated *PAE* = 7.3% (Fig. 4.13 (c)). At the time, this was the highest reported power density of any semiconductor transistor at a frequency of 94 GHz or higher.

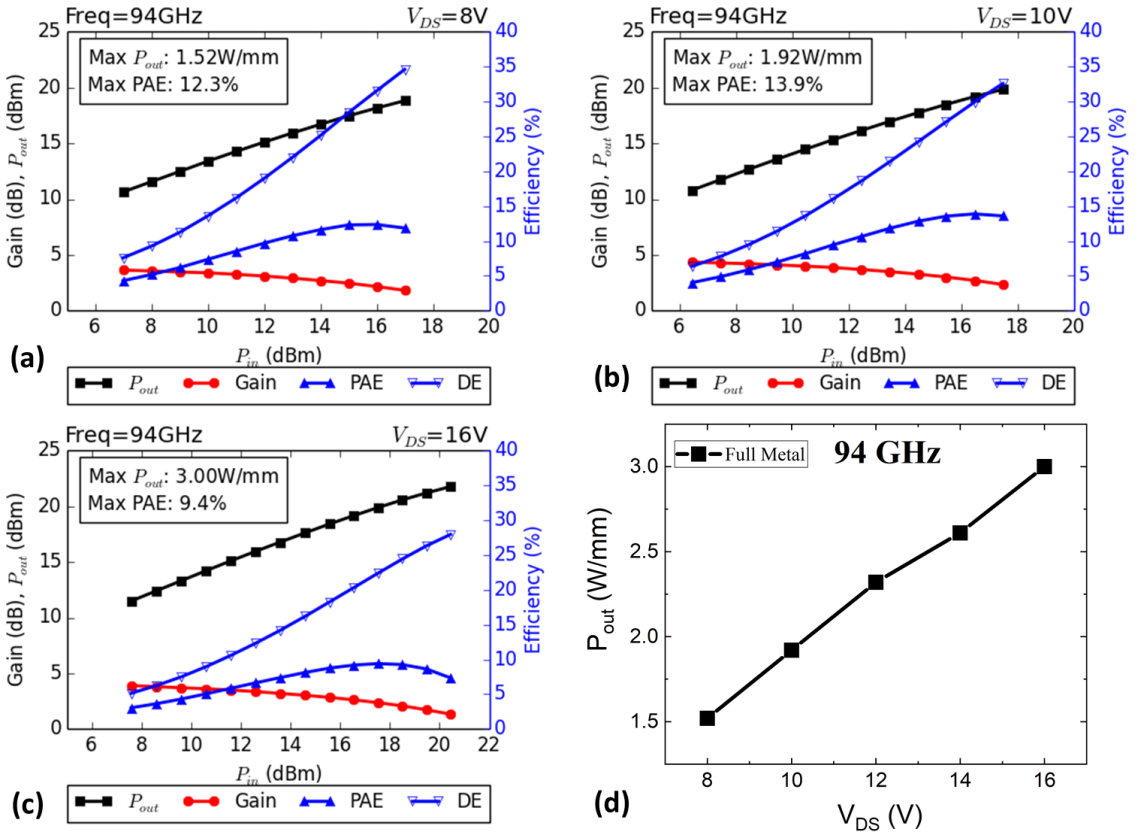

Fig. 4.14: Power sweep data taken on the Full Metal Coverage device at 94 GHz with a drain-source voltage of (a) 8 V, (b) 10 V, and (c) 16 V. (d) Shows how the peak RF output power density scales with respect to V_{DS}. The linear scaling indicates that this NPDR design controls DC-to-RF dispersion quite well. However, the power densities are lower at 94 GHz than at 10 GHz. This is due to self-heating. The efficiency of the device at 94 GHz is much less than at 10 GHz due to the limited gain at such a high frequency. To increase the gain, the device is biased closer to class A. However, this also increases the dissipated DC power of the device, which will can also increase self-heating. A more thermally conductive substrate like SiC could help alleviate this problem. Nominal device dimensions are L_{GS} = 226 nm, L_G = 100 nm, L_{GD} = 1.174 µm, and a W_G = 2 x 25 µm.

94 GHz power performance was also measured on the Flush transistor with a 2 x 12.5 µm W_G, nominal 100 nm foot gate length, 300 nm top gate length, 226 nm L_{GS}, and a 1.5 µm L_{SD}. At a V_{DSQ} = 8 V, a peak power density of 1.92 W/mm was measured at a gain

compression of 3.6 dB. A maximum *PAE* of 12.08% was also recorded in this device (Fig. 4.17). Thus, the Flush transistor achieved a higher power density at the same V_{DSQ} with respect to the MISHEMT with full metal coverage of the GaN Cap sidewalls. This is partially due to the fact that the Flush transistor had a higher linear transducer gain than the Full metal coverage device. The linear G_T of the Flush device is measured to be 4.37 dB, while it is only 3.64 dB in the Full metal coverage MISHEMT. Because of this higher G_T, the Flush transistor could be biased further into compression without *PAE* dropping too precipitously (equation 4.2), and a higher power at a more reasonable *PAE* could be achieved in the Flush device at this bias. Large signal measurements beyond 8 V were not made on the Flush device.

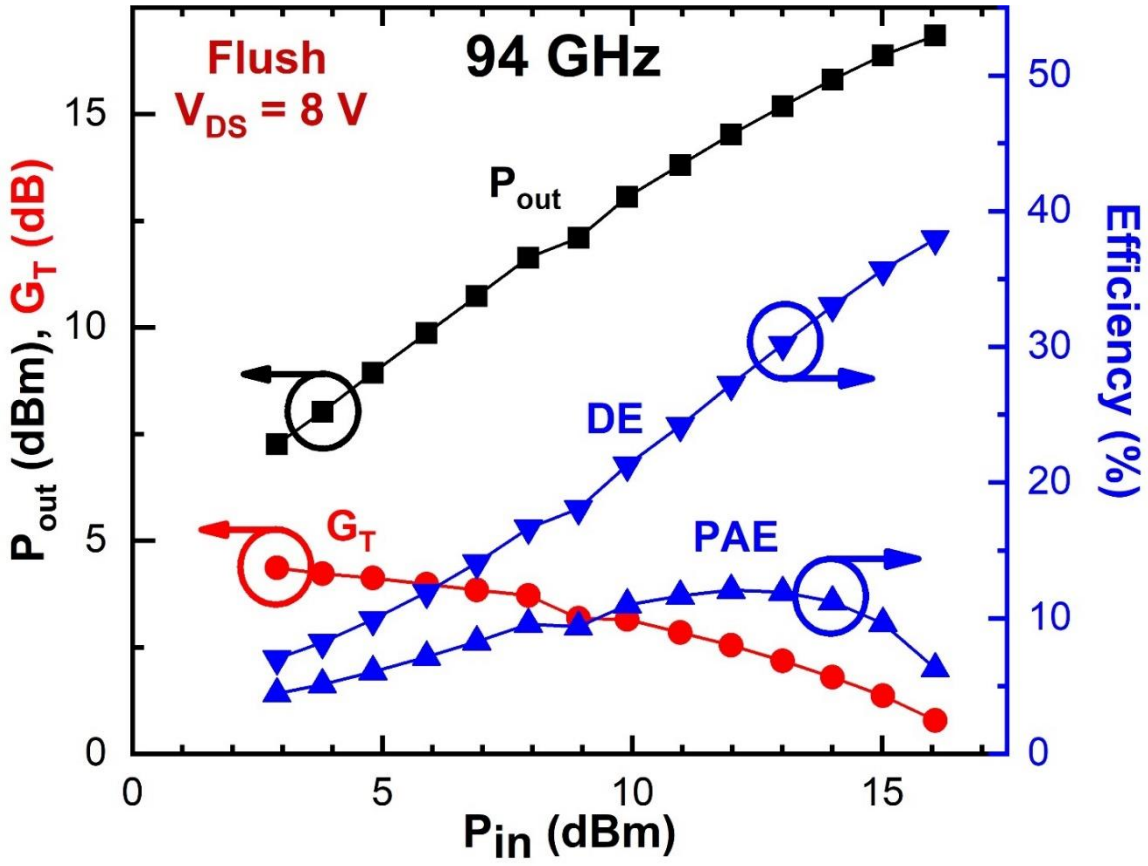

Fig. 4.17: Power sweep data at 94 GHz on the Flush device at a V_{DS} = 8 V.

Comments regarding Large Signal Power Performance at 94 GHz:

Although the power density achieved by these transistors were record setting, the efficiencies were not. There are several reasons for this. First, these two devices have a relatively large source-drain spacing of 1.5 μm. This introduces unnecessarily high parasitic extrinsic resistances R_s and R_d. Future devices should likely have a smaller L_{sd} to minimize such resistances and allow for higher small and large signal gain. Chapter 5 investigates this.

Secondly, the device is fabricated on a full thickness sapphire substrate. Given that the efficiency is already low in the device, a large amount of power is dissipated as heat. The thermal conductivity of sapphire substrate is quite poor, and is somewhere between 0.231 to 0.252 $W \cdot cm^{-1} \cdot K^{-1}$, depending on the direction which thermal energy propagates [14]. This exacerbates the self-heating of the device, raising the temperature in the channel, creating more phonons, lowering the electron velocity and mobility in the channel/access regions, increasing the knee voltage, decreasing the current density, and increasing the parasitic extrinsic resistances R_s and R_d. This feedback loop all leads to further decreases in the *PAE* (as well as the output RF power) of the device.

The third reason is actually something intrinsic to the NPDR MISHEMT design. Both the small and large signal gain of the transistor occurs at a much higher I_{DSQ} than what is typically found in Ga-Polar high frequency HEMTs. At more negative V_{GSQ} (lower I_{DSQ}), the electron 2DEG is pushed further into the AlGaN back-barrier of the HEMT (Fig. 4.18). This increases the amount of charged impurity and alloy scattering in the 2DEG [15] and leads to a reduction in electron mobility. GTLM data demonstrating this is shown in Fig. 4.19 (same data as in Chapter 3). Peak de-embedded f_{max} for a full metal coverage device is shown in Fig. 4.20. Large signal G_T at 94 GHz is shown for another NPDR sample in Fig. 4.21. Thus, to have higher gain, a high quiescent-current density must be used. However, *DE* is higher at

lower source-drain quiescent current densities. The 350 mA/mm used here was chosen as a compromise between power gain and *DE* in order to maximize *PAE*. A higher *PAE* would be obtainable if the peak transconductance occurred at lower I_{DSQ}.

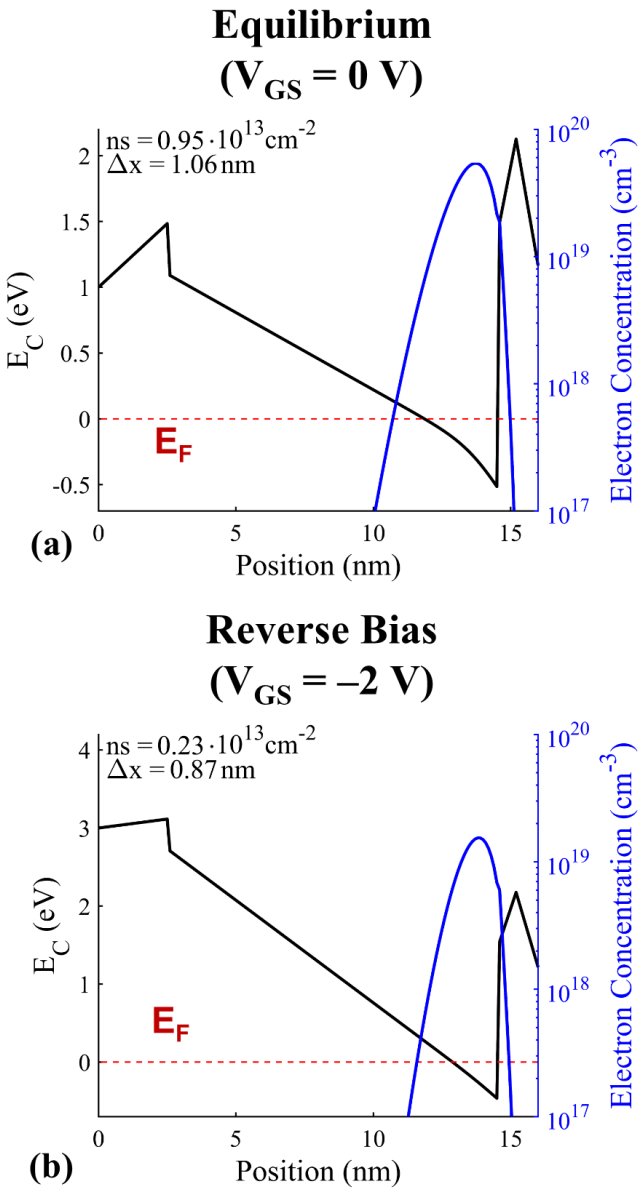

Fig. 4.18: Comparison of the conduction band profile and 2DEG profile in the channel region of the NPDR MISHEMT at (a) equilibrium (V_{GS} = 0 V) and (b) at reverse bias (V_{GS} = –2 V). The distance between the centroid of the 2DEG and the AlN interlayer is given by the Δx value in the figure. Can see that a –2 V reverse bias reduces Δx by about 18% relative to the value at equilibrium. From the findings in [15], this helps explain why the large signal gain is lower when the NPDR MISHEMT is biased closer to class B than to class A.

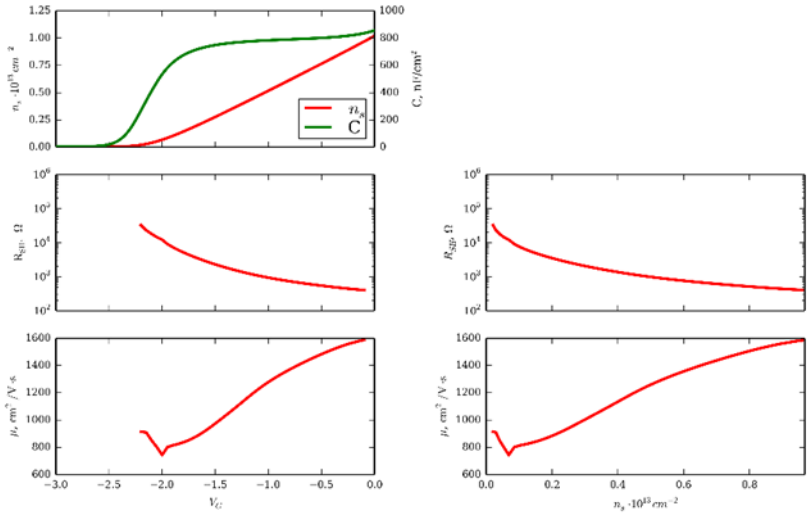

Fig. 4.19: Electron mobility, sheet resistance, and 2DEG density extracted from Gated TLM measurements within the gate recessed region of the NPDR MISHEMT device.

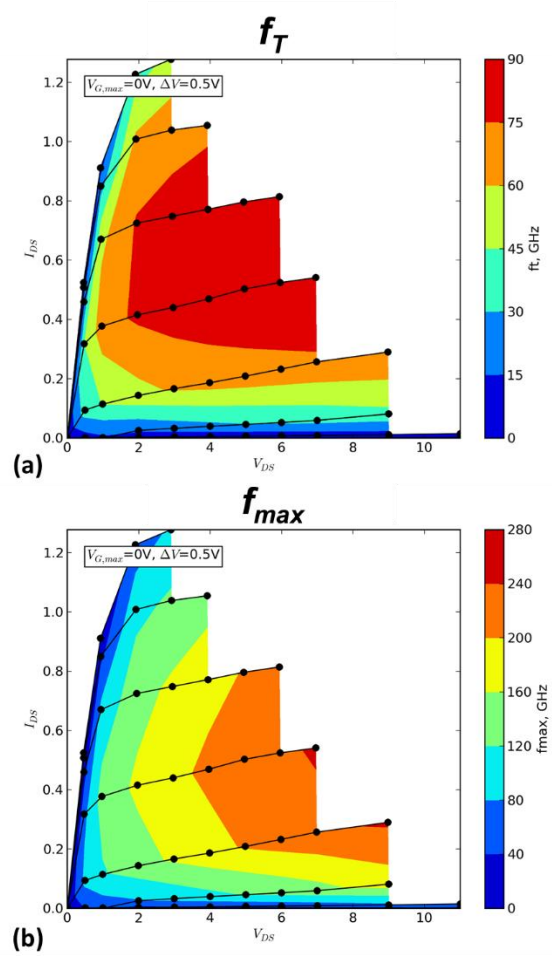

Fig. 4.20: De-embedded contour plot of (a) f_T and (b) f_{max} taken on a Full Metal Coverage NPDR device with a nominal L_{GS} = 125 nm, L_G = 100 nm, L_{GD} = 1.174 µm, and a W_G = 2 x 25 µm.

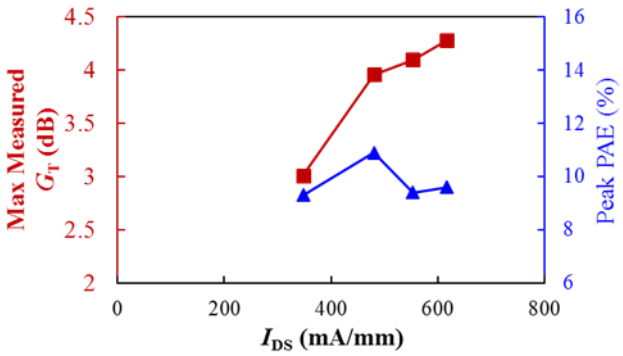

Fig. 4.21: G_T scales with higher I_{DSQ} as would be expected from the de-embedded peak f_{max} plot of Fig. 4.18. It should be noted that this data was taken on another NPDR MISHEMT sample which was fabricated on a SiC substrate. SiC has much higher thermal conductivity than sapphire, so there should be less self-heating in this sample, and this may allow G_T to continue increasing at higher current densities. Nonetheless, the overall trend of increasing G_T with increasing current quiescent source-drain current density should be the same for the NPDR devices fabricated on sapphire substrates.

Moreover, the device's probe pad layout is not optimal and introduces an undesirably high source inductance (Fig. 4.22). Further, the finite tuning range on the signal source side prevents the input from being fully conjugate matched. Finally, gain is reduced by the presence of substrate modes which exist due to our use of an ungrounded coplanar waveguide on a full thickness (425 μm) Al_2O_3 substrate. Addition details regarding how the extrinsic part of the device and the W-Band load pull setup limit the measured *PAE* of this device are discussed at length in reference [16].

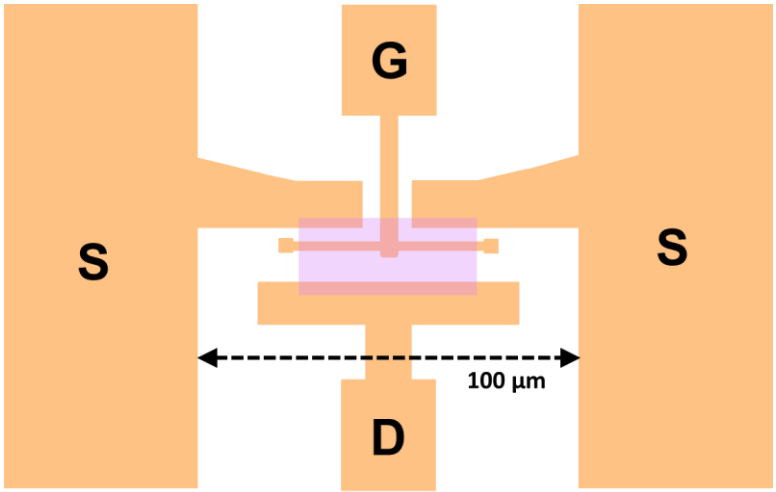

Fig. 4.22: Schematic of the T-feed probe pad layout for the NPDR MISHEMTs used in this work.

Small Signal RF gain with and without 18 nm PECVD SiN Passivation:

As mentioned before, the NPDR MISHEMTs examined in this chapter had a thin 18 nm PECVD SiN external passivation layer applied to them. Many other NPDR MISHEMT samples processed for this thesis did not require this passivation layer to obtain good control of dispersion. Prior to passivating this sample, small signal RF measurements were made on an L_{FG} series of devices with a $W_G = 150$ μm on the 110 nm GaN Cap sample. After deposition of the 18 nm of PECVD SiN, small signal RF measurements were made on nominally equivalent devices on another portion of the wafer. Peak de-embedded f_T and f_{max} data is shown in Fig. 4.23 (a) and (b), respectively. The higher capacitance from the *ex situ* PECVD SiN passivation led to a roughly ~6% decrease in the peak de-embedded f_T values for these set of devices. The drop in f_{max} was smaller at around ~2.3%.

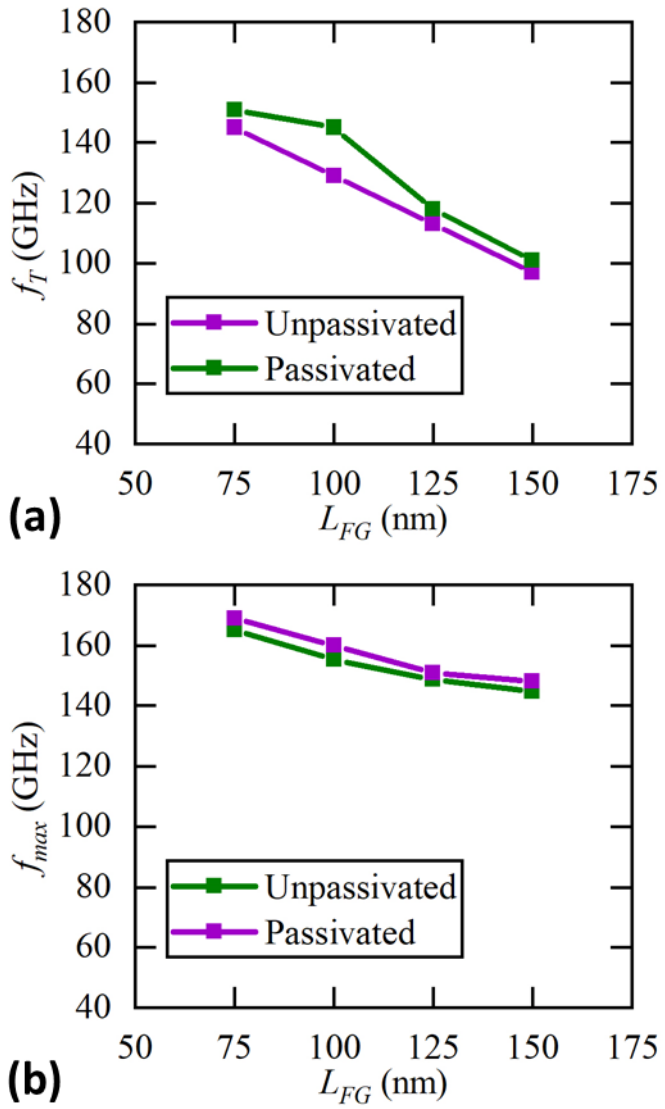

Fig. 4.23: Comparison of peak de-embedded (a) f_T and (b) f_{max} for Full Metal coverage devices on a NPDR MISHEMT sample with 110 nm GaN Cap in the access regions.

10 GHz Load Pull Data taken at Maury Microwave:

Large signal power performance was also taken at 10 GHz on a full metal coverage device at Maury Microwave with their MT2000 Mixed Signal Active Harmonic Load Pull system. This is a complete turnkey load pull system measuring transistors under varying impedances at fundamental and harmonic frequencies. The system is broadband, capable of measuring up to 40 GHz, which allows control of the fundamental, 2nd, and 3rd harmonic load

and source gamma in a completley arbitrary way and allows for very fast measurements. In this measurement, an optmized 2nd harmonic match was used, however, only very small improvements were seen compared with using a 50 Ω impedance.

Fig. 4.24 (a) shows power sweep data taken at V_{DSQ} = 14 V and an I_{DSQ} = 100 mA/mm. A maximum output power density of 4.5 W/mm with an associated *PAE* = 67.7% is recorded. Fig. 4.24 (b) shows the peak $P_{RF,out}$ and associated *PAE* vs. V_{DSQ} for this particular transistor. $P_{RF,out}$ scales very well with drain voltage, suggesting an RF current swing of approximately 1.6 A/mm from equation 4.12.

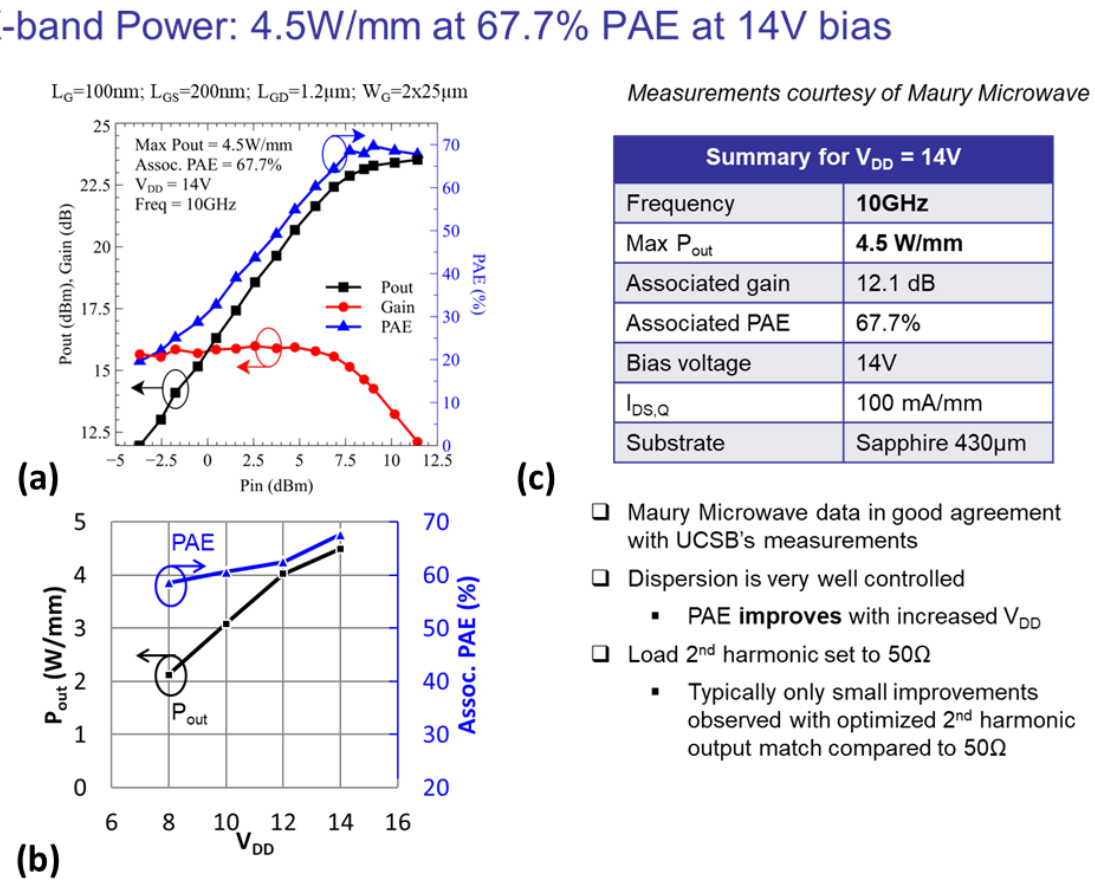

Fig. 4.24: (a) Power sweep data taken on a Full Metal coverage device at a V_{DSQ} = 14 V. (b) Peak RF output power density and associated *PAE* VS. V_{DSQ}. (c) Table summarizing the NPDR MISHEMT device performance at a V_{DSQ} = 14 V.

RF IV data taken at 6 GHz at Maury Microwave with their MT2000 system is shown in Fig. 4.25. Fig. 4.25 (a) shows the device at a V_{DSQ} = 8 V, and a V_{GSQ} = 0, +1, and +2 V. Very high RF current densiteis are measured, exceeding 2 A/mm for a V_{GSQ} = +2 V. This is actually higher than the DC current denstiy measured on a nominally equivalent NPDR MISHEMT (measurement is pulsed and results in less self-heating), confirming the excellent control of dispersion provided by the NPDR MISHEMMT design. Fig. 4.25 (b) displays the RF IV trace at a V_{GSQ} = +2 V, at a V_{DSQ} of 8, 10, and 12 V. Two things can be deduced from this plot. First, there is some knee walkout (drain-side dispersion) seen in the transistor when the transistor is biased at higher drain-source voltages. However, the peak current density also increases with increasing drain-source bias as well. This is likely due to the threshold voltage of the transistor moving more negative at higher drain-source bias voltages, as explained in Chapter 2.4.

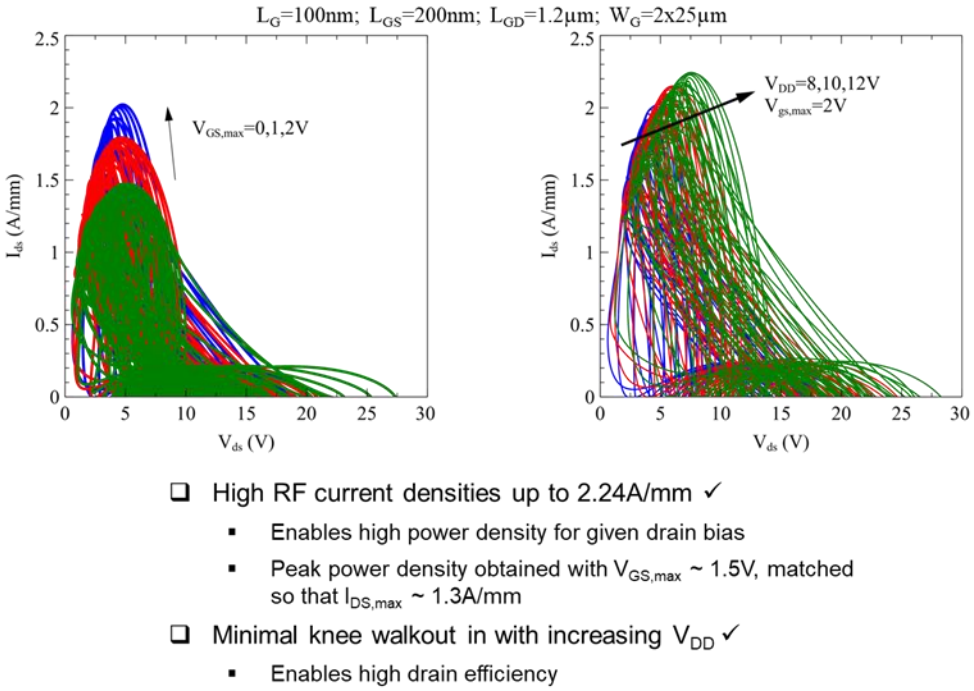

Fig. 4.25: RF IV measurements taken at 6 GHz at Maury Microwave [17]. (a) Shows how the RF-IV varies with respect to a changing V_{GSQ}. (b) Shows how the RF-IV varies with respect to a changing V_{DSQ}.

Flush Device with Scaled Source-Drain Spacing:

Data was also taken on a Flush device with a 110 nm GaN Cap, a shorter L_{sd}, along with the 18 nm PECVD SiN passivation layer. This NPDR MISHEMT has a foot gate length of 75 nm (L_{fg}), top gate length of 300 nm (L_{tg}), L_{gs} = 160 nm, L_{gd} = 365 nm, and W_g = 2 x 25 µm is presented. The device is constructed such that the foot gate metal is flush with the bottom edge of the UID GaN cap sidewall. There is nominally no gate metal overlap onto that sidewall.

DC and pulsed IV characteristics of the transistor are displayed in Fig. 4.26. At V_{GS} = 0 V the DC on-resistance (R_{on}) and maximum drain-source current density are measured to be 0.58 Ω·mm and 1.5 A/mm, respectively (Fig. 4.26 (a)). Transfer characteristics at V_{DS} = 5

V give a peak extrinsic transconductance (g_m) of 620 mS/mm and a drain-induced barrier lowering (*DIBL*) of 63.5 mV/V (Fig. 4.26 (b)).

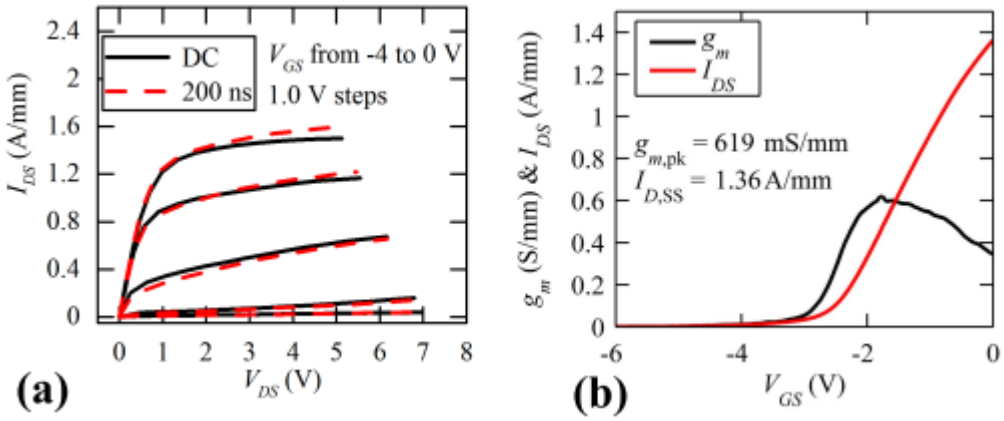

Fig. 4.26: (a) DC vs 200 ns Pulsed IV plot. V_{GS} was held at 1.5 V below the -2.5 V threshold voltage of the device (V_{GS} = -4 V) and 200 ns gate pulses were applied along a 25 Ω load line in +1 V steps until a maximum V_{GS} of 0 V was reached. (b) Transfer characteristics of the NPDR MISHEMT at a V_{DS} = 5 V.

Pulsed IV measurements were taken as a check of the transistor's dispersion performance. 200 ns gate pulses from 1.5 V below the -2.5 V threshold voltage of the device were applied along a 25 Ω load line (Fig. 4.26 (a)). Very little DC-to-RF dispersion is seen, demonstrating the effectiveness of the NPDR design. The small-signal characteristics (after pad de-embedding) [18] of another device with the same nominal dimensions as that reported throughout this letter is displayed in Fig. 4.27. At a quiescent bias of V_{GS} = -2.0 V, V_{DS} = 8 V, and I_{DS} = 0.6 A/mm a simultaneous f_{max}/f_t combination of 276/149 GHz is achieved, illustrating the excellent high frequency capabilities of the NPDR MISHEMT.

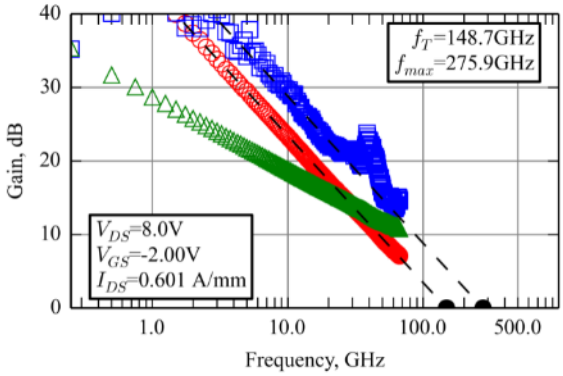

Fig. 4.27: Small signal RF performance at a quiescent bias of V_{GS} = -2.0 V, V_{DS} = 8 V, and I_{DS} = 0.6 A/mm after pad de-embedding [18].

Uncooled continuous wave (*CW*) power performance at 94 GHz was measured using a passive Maury Microwave load pull system. The transistor was biased at class AB with a source-drain quiescent current density of 345 mA/mm. Fig. 4.28 (a) shows the power sweep data at a drain bias of V_{DS} = 8 V. A peak *PAE* of 20% with an associated output power density (P_{out}) of 1.73 W/mm is achieved at this bias. At a higher input power, a maximum P_{out} = 2.4 W/mm with an associated *PAE* = 13.7% and drain efficiency *DE* = 47.4% is measured. Load pull measurements were also made at V_{DS} = 10 V and an I_{DS} = 345 mA/mm (Fig. 4 (b)). Peak P_{out} = 2.9 W/mm with an associated *PAE* = 15.5% and a drain efficiency of 43.4%. The factors limiting gain and *PAE* from the earlier section in Chapter 4.4 also are true for the W-Band load pull measurements taken here.

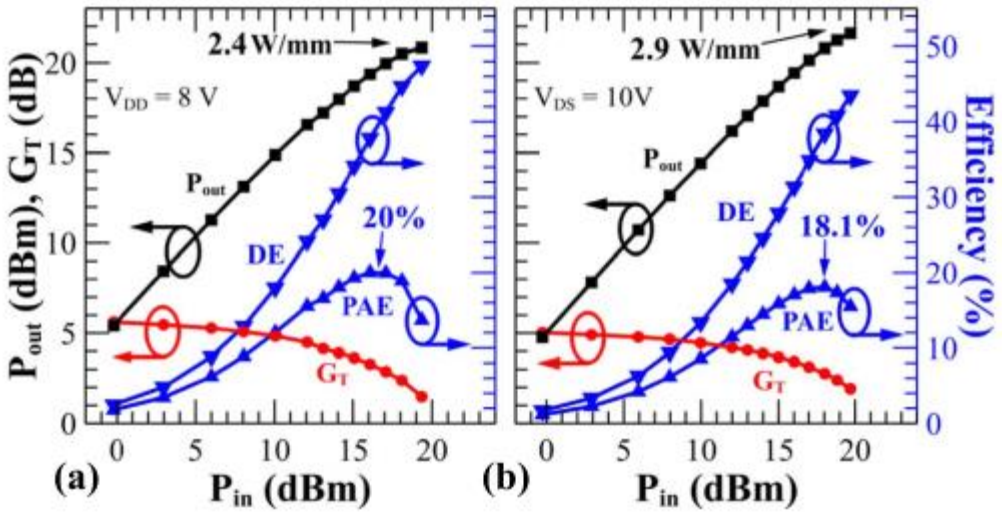

Fig. 4.28: Large-signal power performance of the NPDR MISHEMT at 94 GHz with a quiescent current density of I_{DS} = 345 mA/mm. (a) At a V_{DS} = 8 V, (b) At a V_{DS} = 10 V. Device dimensions are L_G = 75 nm, L_{GS} = 160 nm, L_{GD} = 365 nm, and W_G = 2 x 25 μm.

Chapter 4.5 – Summary:

Initial results on NPDR MISHEMTs with T-Gates are reported in this chapter. The devices demonstrated record power performance (at the time of measurement). The factors limiting performance, especially gain and efficiency, were outlined, and will be explored in greater detail in Chapter 5.

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Chapter 5: Lateral Device Dimension Optimization

Initial NPDR MISHEMT T-Gate results were shown in the previous chapter. Record large signal RF power performance was achieved despite the low thermal conductivity of the sapphire substrate the NPDR T-Gate devices were fabricated on. In this chapter, a more systematic study of the lateral device dimensions and their effect on overall device performance at 94 *GHz* is investigated.

Chapter 5.1 – Growth + Fabrication Details:

Unless otherwise stated, devices in this section were grown via MOCVD on miscut sapphire substrates [1]. Growth conditions are similar to that reported in [1]. The epitaxial structure is shown in Fig. 5.1 (a). Devices contain a 5 nm MOCVD SiN_x gate dielectric, a 110 nm UID GaN cap (access regions only), a 2.6 nm $Al_{0.27}Ga_{0.73}N$ top barrier, a 12 nm UID GaN channel, a 0.7 nm AlN interlayer, a 10 nm UID $Al_{0.38}Ga_{0.62}N$ spacer layer, and a Si-doped graded AlGaN back-barrier. Band diagrams generated with a one-dimensional self-consistent Schrödinger-Poisson solver [2] for the gate recess and GaN cap regions are shown in Fig. 5.1 (b) and (c) respectively.

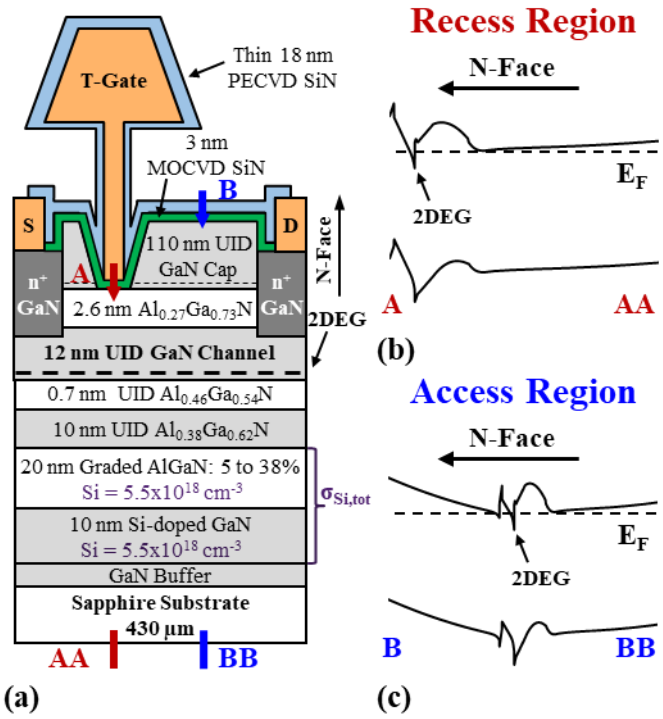

Fig. 5.1: (a) Cross-section of nominal NPDR MISHEMT device structure (not to scale). Energy band diagram at equilibrium in the (b) gate recessed region and (c) the access region. Simulations assume a Schottky gate structure with a pinning position of 1 eV [2] to eliminate the complexities associated with the MIS interface.

The fabrication process is identical to that detailed in Chapter 4, including the addition of the 18 nm PECVD SiN *ex situ* passivation layer (same fabrication run as samples from previous chapter). The gate recessed GaN Cap sidewall had a slope of approximately 61°, meaning the length of the recessed GaN Cap sidewall is ~ 61 nm.

Chapter 5.2 – Source-Drain (Gate-Drain) Spacing Series:

Chapter 4.4 showed data suggesting that a shorter source-drain spacing was beneficial to device performance at 94 GHz. However, those results did not constitute a clean study as the gate lengths were different for the 2 transistors. In this section a more thorough

investigation of the source-drain spacing's (L_{SD}) effect on overall device performance is conducted.

All devices had a foot gate length (L_{FG}) of 150 nm, a top-gate length (L_{TG}) of 450 nm, a stem height of ~ 200 nm, a n+ regrowth to base of recess length of 300 nm (L_{gs}), and a gate width (W_G) of 2x75 μm patterned in a T-feed configuration. The drain-side GaN Cap sidewall was nominally covered in its entirety with gate metal (61 nm of gate metal coverage). The source-side GaN Cap sidewall has full metal coverage + 50 nm of lateral field plating over top of it. A pictorial representation of the device is shown in Fig. 5.2. This series of devices consisted of three transistors, with an L_{SD} of 1, 2.5, and 3.5 μm.

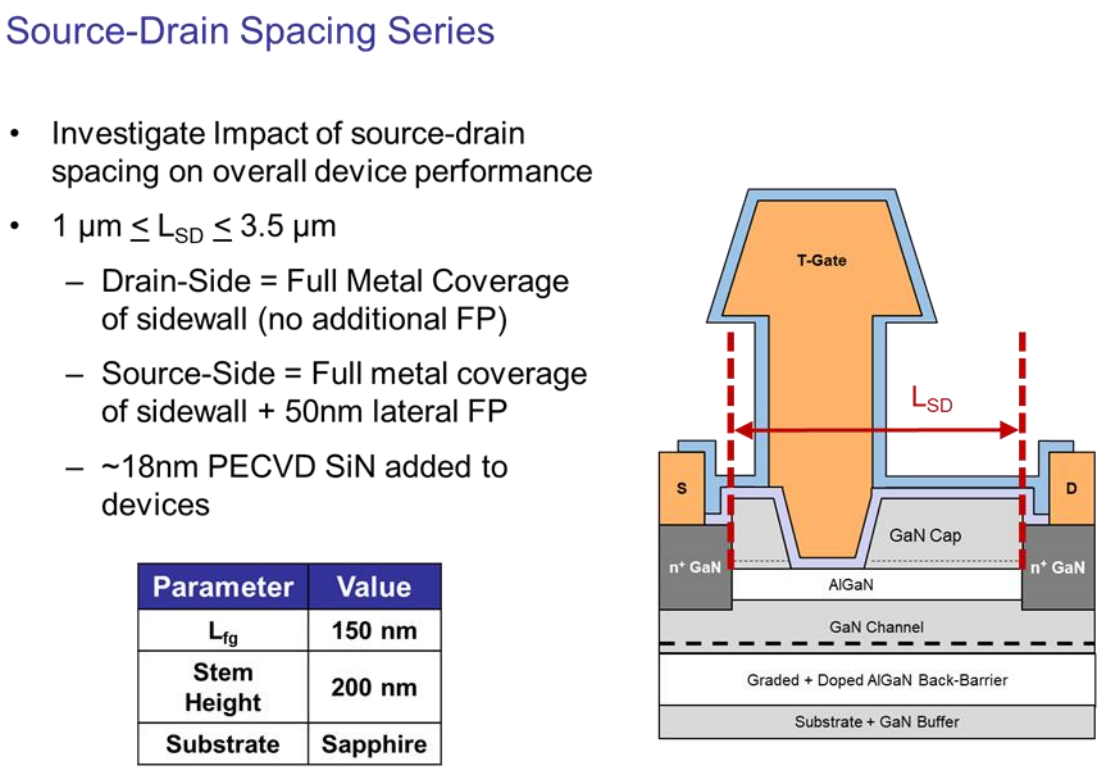

Fig. 5.2: Cartoon representation of the NPDR MISHEMT devices investigated in this source-drain spacing series.

All three MISHEMTs had a similar extrinsic transconductance and saturation current density. The peak extrinsic transconductance is ~ 580 mS/mm and at V_{GS} = 0 V the saturation

current density in all three NPDR transistors is ~ 1.2 A/mm. However, the on-resistance (R_{ON}) of the device decreased significantly with decreasing source-drain spacing. Fig. 5.3 shows that the R_{ON} decreased from a value of 1.3 Ω·mm to 0.65 Ω·mm when L_{SD} was shrunk from 3.5 to 1 µm.

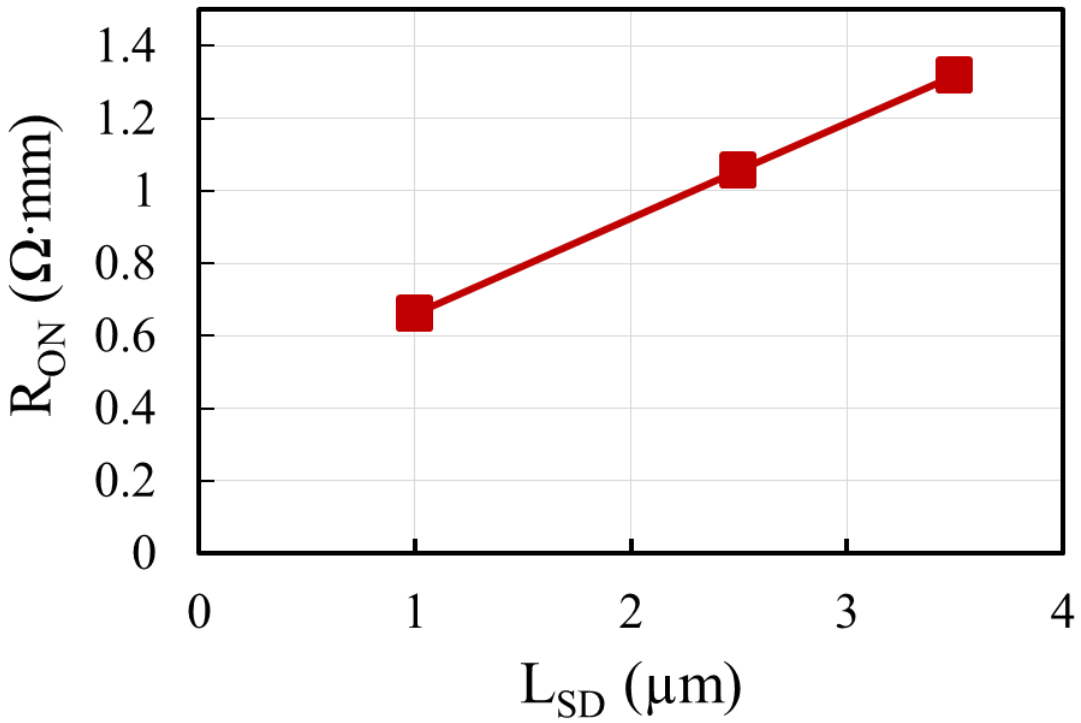

Fig. 5.3: Variation of DC on-resistance at a V_{GS} = 0 V with respect to the total source-drain spacing.

This drop in extrinsic resistance with decreasing L_{SD} also led to an increase in peak de-embedded power gain cutoff frequency (f_{max}) (equation 5.1) as shown in Fig. 5.4. It should be noted that the 2 x 75 µm W_G is too large for a true W-Band device, and as such the reported f_{max} values are all lower than one would expect for a device operating at 94 GHz. However, the trends displayed should still hold true when the gate width is shrunk to a more appropriate size for a transistor amplifier meant to operate in the W-Band range of frequencies.

$$f_{max} = \frac{\frac{gm_{ext}}{2\pi * (C_{gs} + C_{gd})}}{\sqrt{\frac{4}{R_{ds}} * (R_g + R_s + R_i) + 8\pi * f_T * C_{gd} * (2 * R_g + R_s + R_i)}} \quad (5.1)$$

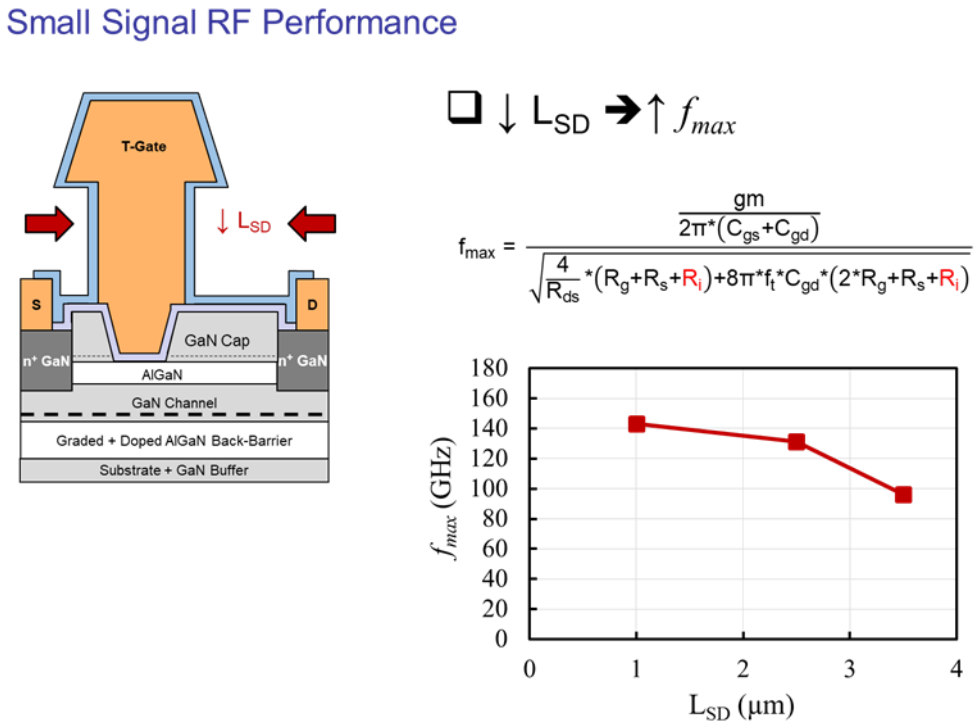

Fig. 5.4: Variation of peak de-embedded f_{max} vs. L_{SD} of the NPDR MISHEMT devices.

Breakdown measurements were measured via the Drain Current Injection (DCI) technique on the three devices adjacent to one another on the wafer [3]. A 1 mA/mm injection current was used. Fig. 5.5 shows the breakdown scans for all 3 devices. Like the NPDR i-Gate MISHEMTs of Chapter 3.3, all devices in this series had a "soft" breakdown which was non-catastrophic and where channel breakdown was not witnessed in any of the measurements. Fig. 5.6 reveals that breakdown voltage did not scale with L_{SD}. Based on the discussions of "soft" breakdown given in Chapter 2.3, 2.4, and 3.3, this was to be expected. The apparent anti-correlation of breakdown voltage is with L_{SD} is likely due to random

variations in the epi from device to device. Additional data (not part of this relatively "clean" series), does not suggest that breakdown gets lower with increasing L_{SD}.

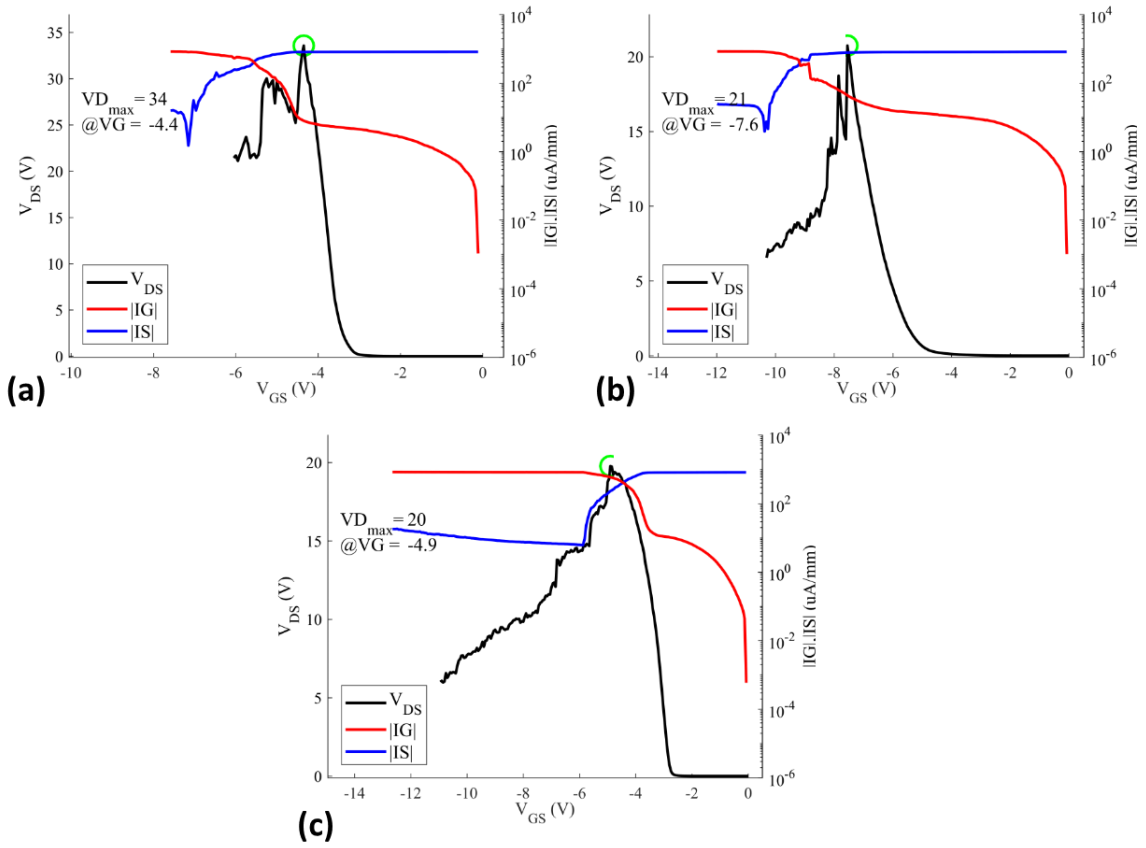

Fig. 5.5: DCI scans for an NPDR MISHEMT with a source-drain spacing of (a) 1 μm, (b) 2.5 μm, and (c) 3.5 μm.

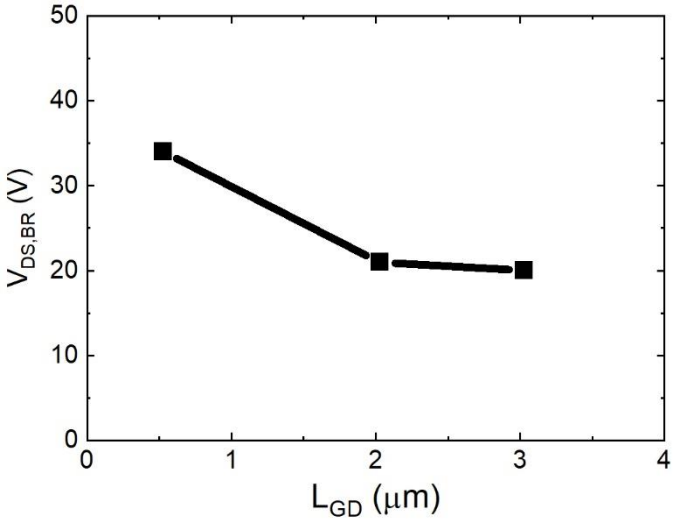

Fig. 5.6: Breakdown voltage vs. L_{GD} in this series. Can see that $V_{DS,BR}$ does not increase with increasing L_{GD}.

Large signal power performance was measured at 10 GHz using a Maury Microwave tuner-based load pull system. Transistors were biased at class AB with an I_{DSQ} of 100 mA/mm in each case. Fig. 5.7 shows how the RF output power density ($P_{RF,out}$) and gate leakage (I_G) scale with the V_{DSQ} of the transistor. $P_{RF,out}$ scales well with V_{DSQ} for the L_{SD} = 3.5 μm device and I_G remains relatively low up until V_{DSQ} = 17 V. At L_{SD} = 2.5 μm, the $P_{RF,out}$ has increased, but so too has the gate leakage. For the L_{SD} = 1 μm device $P_{RF,out}$ is significantly higher, but the I_G has increased appreciably as well. The increasing I_G seems to suggest that even if the absolute breakdown voltage measured via the DCI technique is similar between several devices, their ability to handle constant applied voltage may not be the same, as was seen for the shorter L_{SD} devices in this series.

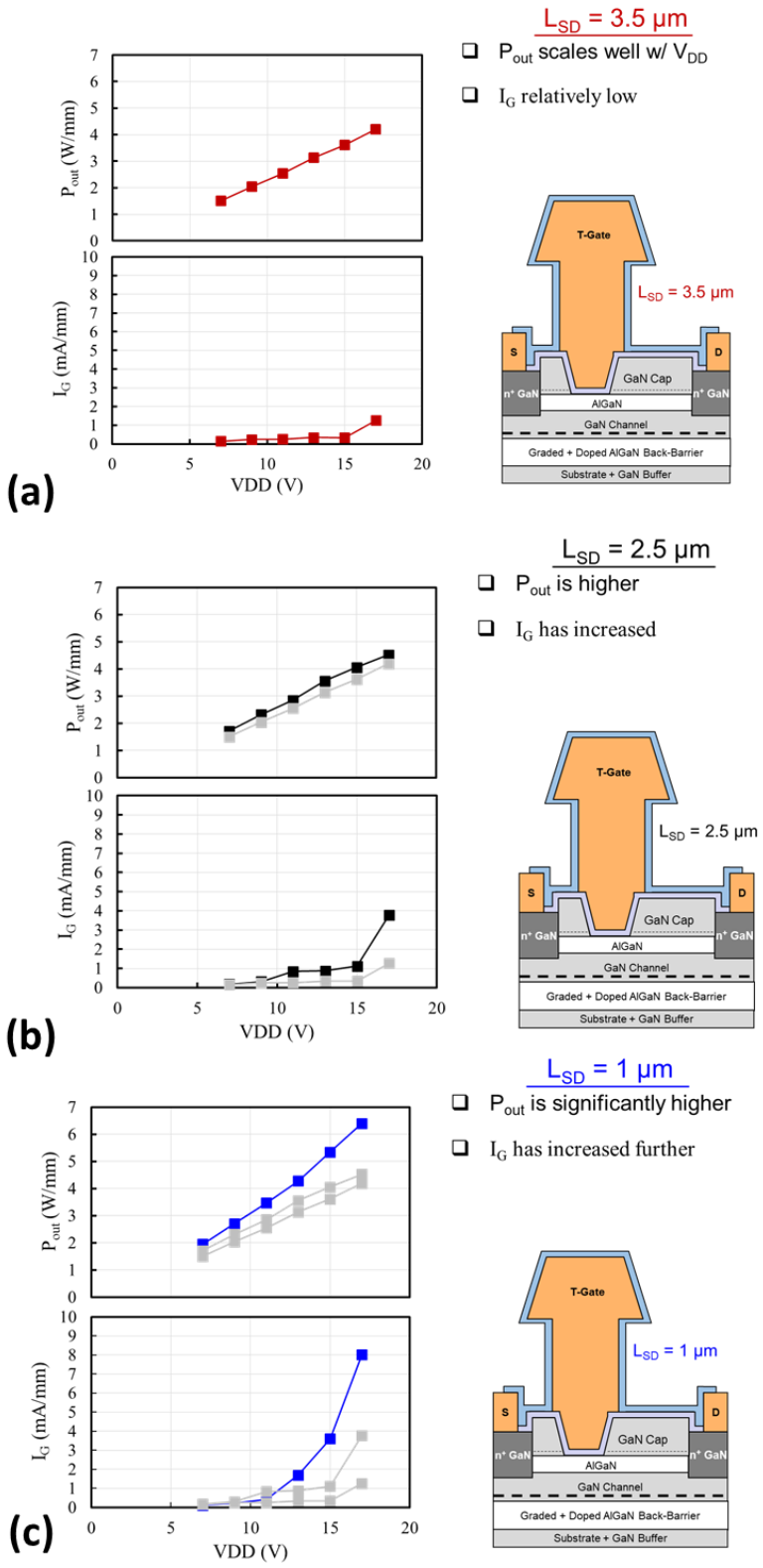

Fig. 5.7: Variation of gate RF output power density and gate leakage with respect to source-drain (gate-drain) spacing. All devices contain a nominal L_{GS} = 300 nm, L_G = 150 nm, and a W_G = 2 x 75 µm.

Taking all these factors into account the device with the minimum L_{SD} (1 μm) of the series appears to be the best choice for a W-Band transistor amplifier. This device had the lowest R_{ON} (lower knee voltage), highest f_{max}, and had the highest large signal RF output power density of all devices in this L_{SD} series. This device did have higher I_G, but because gain and efficiency are very hard to achieve at 94 GHz in the III-N system, this is considered a reasonable tradeoff. Moreover, additional data suggests that the benefits of shrinking L_{SD} continues down to at least an L_{SD} = 500 nm (which is near the limit of what the i-line stepper can repeatably achieve in the UCSB nanofab) without serious degradation of leakage and breakdown performance.

Chapter 5.3 – Drain Side Metal Coverage Study on T-Gates:

Chapter 3.4 investigated how the placement of the gate metal relative to the GaN Cap sidewall affects the overall current dispersion of the device. It was found that any gap between the gate metal and GaN Cap sidewall $\geq$ 50 nm resulted in very large amounts of DC-to-RF dispersion. This section explores the impact of gate metal coverage (gap) on the drain-side GaN Cap with respect to overall NPDR device performance.

All devices had an L_{FG} = 150 nm, L_{TG} = 500 nm, L_{SD} = 1.5 μm, W_G = 2x75 μm, and a stem height of ~ 200 nm. The source-side GaN Cap sidewall has full metal coverage + 50 nm of lateral field plating over top of it, while the placement of the gate metal relative to the drain-side GaN Cap sidewall varied from a gap of ~15 nm to having full gate metal coverage of the GaN Cap sidewall + 50 nm of lateral field plating over the top of the GaN Cap (see Table 5.1). A pictorial representation of this series of NPDR devices is given Fig. 5.8.

Device	Gate Metal Coverage of Drain-side GaN Cap Sidewall
1	Full Metal Coverage (61 nm) + 50 nm of Field Plating
2	Full Metal Coverage (61 nm)
3	~ ½ Sidewall Metal Coverage (~ 30 nm)
4	No Metal Coverage & No Gap
5	~ 15 nm Gap between Gate Metal and Base of Sidewall

Table 5.1: Description of each NPDR device investigated in this section of the thesis.

Parameter	Value
L_{fg}	150 nm
L_{SD}	1.5 µm
W_G	2 x 75 µm
Stem Height	200 nm
Substrate	Sapphire

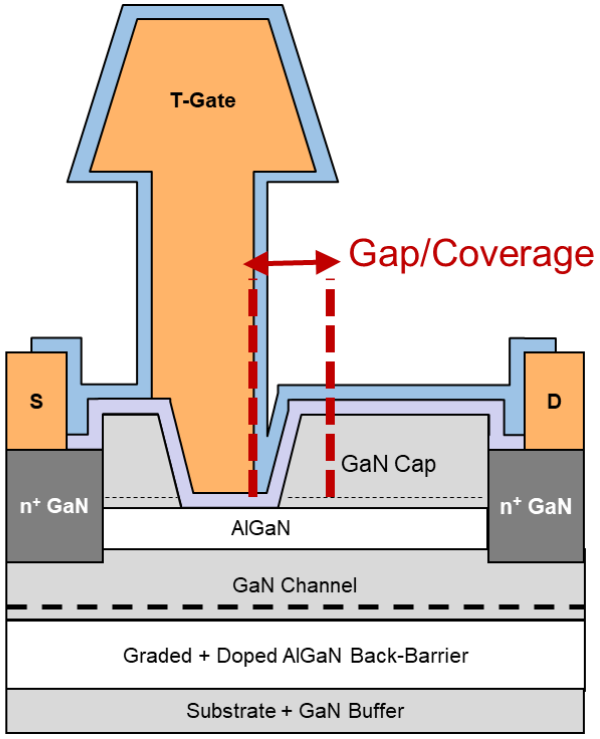

Fig. 5.8: Cross-section of the N-Polar GaN Cap MISHEMT device series investigated in this section of the thesis.

DC and PIV performance was comparable for all NPDR MISHEMTs in this series (Fig. 5.9). However, it should be noted that the PIV conditions used here were not very harsh, and that a more stringent test of dispersion performance is provided by the large signal power performance of the transistor (to be shown soon). Bias-dependent S-parameter measurements up to 67 GHz were also made on this series of devices with a Keysight N5227A PNA calibrated by the LRRM method at the probe tips using an impedance standard substrate [4].

Fig. 5.11 shows the peak de-embedded f_{max} with respect to the amount of gate metal coverage (gap) over the GaN Cap sidewall. A small increase is seen with decreasing gate metal coverage, however, the biggest jump in f_{max} (i.e. largest drop in C_{gd} in equation 5.1) occurs when an actual gap is introduced between the gate metal and GaN Cap sidewall. This is supported by COMSOL simulations performed by Matt Guidry showing that a small decrease in capacitance occurs when the gate metal coverage of the sidewall is reduced, but a much larger decrease is seen when an actual gap is introduced between the gate metal and sidewall.

Parameter	Value
g_m	580 mS/mm
R_{on}	0.9 Ω·mm
I_{DS}	1.2 A/mm
Dispersion	~0%

(a)

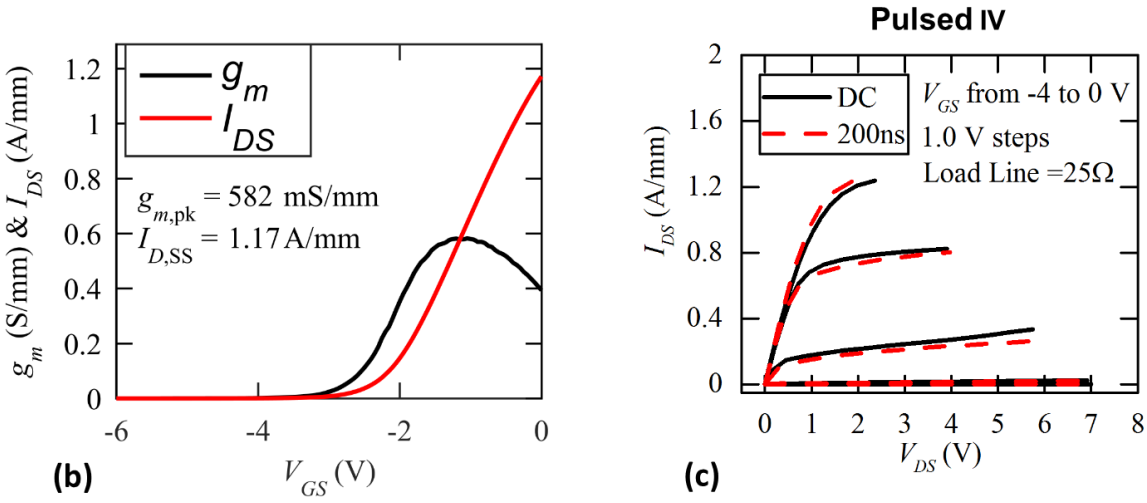

Fig. 5.9: (a) Table highlighting the typical DC and PIV performance of the devices in this series. (b) I_{DS} and extrinsic g_m vs. V_{GS}. (c) PIV performance for one of the devices in this gate metal coverage of drain GaN Cap sidewall series.

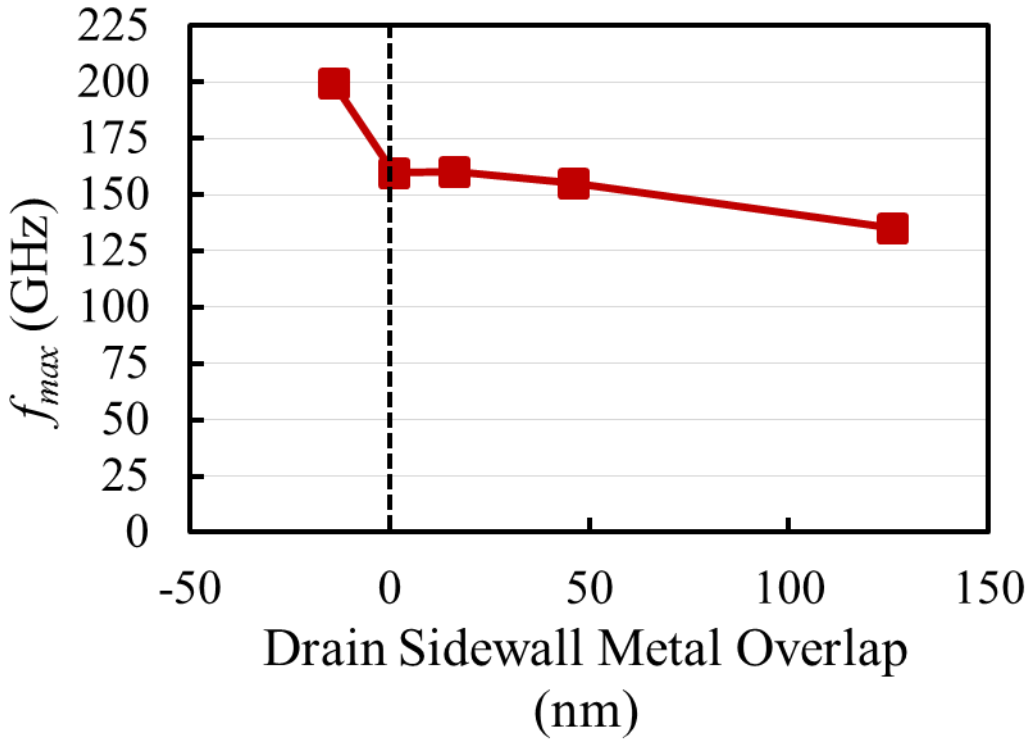

Fig. 5.11: Variation of f_{max} with gate metal coverage of the drain-side GaN Cap sidewall. A large increase in f_{max} once a gap is introduced between the metal and sidewall.

Uncooled continuous wave (*CW*) large signal power performance was measured at 10 GHz using a Maury Microwave tuner-based load pull system. Transistors were biased at class AB with an I_{DSQ} of 100 mA/mm in each case. Fig. 5.12 shows how the $P_{RF,out}$ and I_G scale with the V_{DSQ} for each of the transistors in this series. It can be seen that $P_{RF,out}$ scales well with drain bias and I_G remains low up until a V_{DSQ} = 17 V for the device with Full metal coverage + 50 nm of field plating (Fig. 5.12 (a)). The device with full metal coverage performed in a similar fashion, but had higher $P_{RF,out}$ and slightly higher I_G (Fig. 5.12 (b)). The device where only ½ the drain-side GaN Cap sidewall is covered in gate metal has a similar $P_{RF,out}$ and I_G up until a V_{DSQ} = 13 V (Fig. 5.12 (c)). After this point, the gate leakage shoots up, and the power density no longer scales with drain voltage. A similar trend is seen in the device where the gate metal is flush with the bottom edge of the sidewall. However, in this case the Flush device begins degrading at a V_{DSQ} = 11 V (Fig. 5.12 (d)). Finally, a

different set of scaling behavior is seen with respect to V_{DSQ} in the NPDR transistor with a 15 nm gap between gate metal and GaN Cap sidewall (Fig. 5.12 (e)). In this device, the $P_{RF,out}$ is lower for all investigated V_{DSQ} biases relative to the other devices in this series. Further, the I_G is actually lower than that of both the Flush device and even the transistor where ½ the GaN Cap sidewall is covered in gate metal.

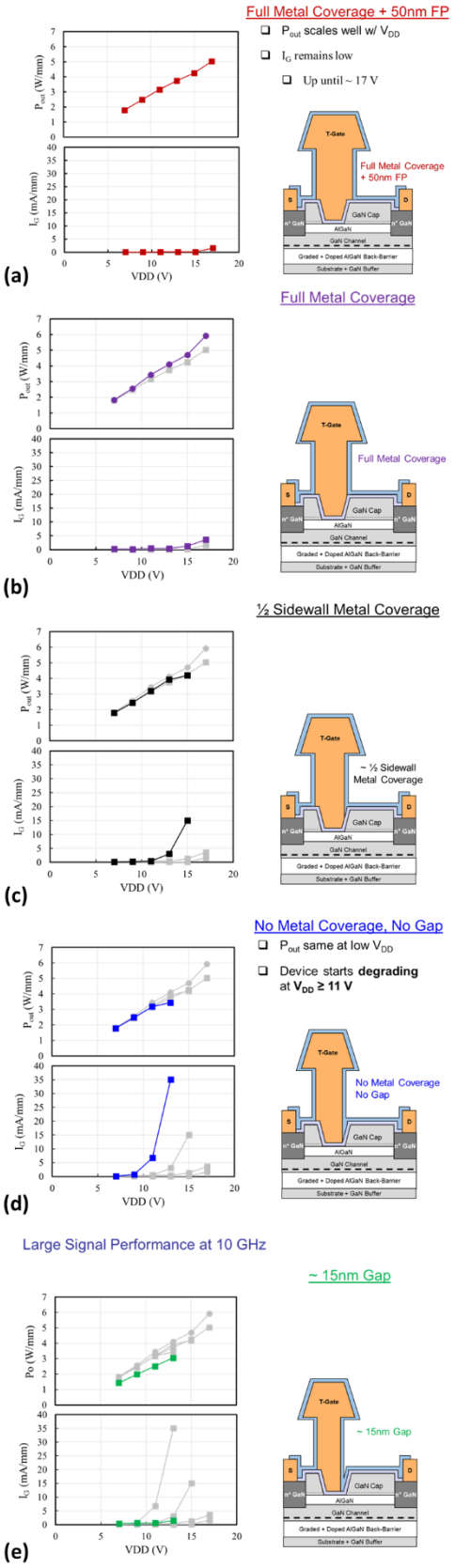

Fig. 5.12: Variation of P_{out} and I_G vs. V_{DS} in this gate metal coverage of drain-sidewall series.

Fig. 5.13 compares the simulated lateral E-Field in the channel of the device with Full Metal coverage + 50 nm Field Plating, the device where ½ the sidewall is covered in gate metal, and this device which has a ~ 15 nm gap between gate metal and sidewall. This simulation assumes no dispersion/trapping occurs in the device. If all three simulated devices were free of trapping, the lateral E-Field should be approximately 20% higher in the device with a gap relative to the device where ½ the sidewall is covered in gate metal. However, the gate leakage is actually lower in the device with a gap relative to the ½ sidewall coverage device. The lower absolute power density, worse scaling of $P_{RF,out}$ with respect to drain voltage, and the lower gate leakage all seem to indicate that the device with a 15 nm gap between gate metal and sidewall is suffering from DC-to-RF dispersion. As mentioned earlier, this device did not show significant dispersion in the PIV measurements, but the large signal load pull data offers a more stringent test of dispersion.

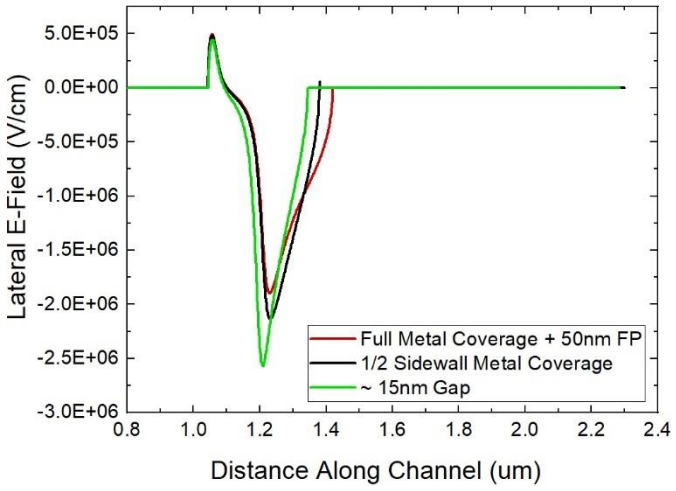

Fig. 5.13: Simulated lateral E-Field at the GaN channel/AlN interface for the NPDR device with Full metal coverage + 50 nm of lateral field plating (red line), the device with ½ the drain-side GaN Cap sidewall covered in metal (black line), and the device with a 15 nm gap between the gate metal and drain-side GaN Cap sidewall. The simulation assumes no dispersion/trapping anywhere in the device. Further, the simulation assumed a 47.5 nm GaN cap, not a 110 nm cap. The overall trend should be the same regardless.

Considering all the data presented in this section, it seems like the device with full metal coverage of the slanted drain-side GaN Cap sidewall, but no additional field plating, is

the optimal choice. It had the highest $P_{RF,out}$ of all devices investigated, had roughly the lowest gate leakage (slightly higher than additional field plating device), and had a slightly higher f_{max} than the device with additional 50 nm of field plating as well.

Chapter 5.4 – Source Side Metal Coverage Study on T-Gates:

Chapter 3.4 investigated how the placement of the gate metal relative to the GaN Cap sidewall affects the overall current dispersion of the device. It was found that any gap between the gate metal and GaN Cap sidewall $\geq$ 50 nm resulted in very large amounts of DC-to-RF dispersion. This section explores the impact of gate metal coverage (gap) on the source-side GaN Cap sidewall with respect to overall NPDR transistor performance. A different sample than that used in the previous sections of this chapter was used for this particular study. Details of the growth procedure and epitaxial layers of the sample are given in the following paragraph.

The sample was grown via metal organic chemical vapor deposition (MOCVD) on a miscut SiC substrate [1]. The epitaxial structure is shown in Fig. 5.15 (a). Devices contain a 3 nm MOCVD SiN_x gate dielectric, a 47.5 nm UID GaN cap layer (access regions only), a 2.6 nm $Al_{0.27}Ga_{0.73}N$ top-barrier, a 9.3 nm UID GaN channel, a 0.7 nm AlN interlayer, a 10 nm UID $Al_{0.38}Ga_{0.62}N$ spacer layer, and a Si-doped graded AlGaN back barrier. An n+ GaN layer regrown by plasma assisted molecular beam epitaxy (PAMBE) takes the place of the GaN cap and $Al_{0.27}Ga_{0.73}N$ top-barrier in the source/drain contact regions. The fabrication procedure is essentially the same as that for the other samples in this Chapter. However, no PECVD SiN_x passivation layer was added to the device presented here, as the 47.5 nm GaN cap and 3 nm MOCVD SiN_x dielectric were sufficient to eliminate any DC-to-RF dispersion in the device.

(Also, the gate and ohmic recesses consisted of only the selective BCl_3/SF6 etch in this case, and they resulted in a sidewall angle of 57° with respect to the horizontal and a 30 nm lateral length of the GaN Cap sidewall).

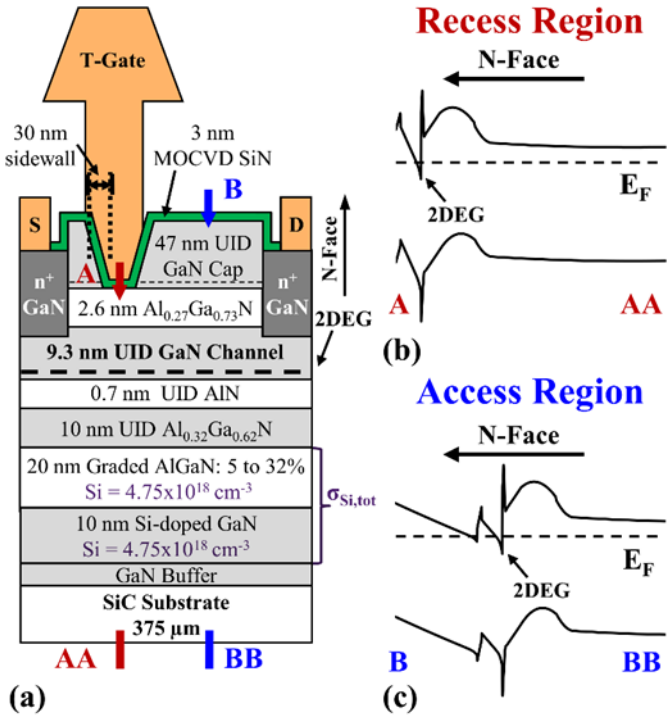

Fig. 5.14: a) Cross-section of the N-Polar GaN cap MISHEMT device structure (not to scale). Energy band diagram at equilibrium in the (b) gate recessed region and (c) the access region. Simulations assume a Schottky gate structure with a pinning position of 1 eV [15] to eliminate the complexities associated with the MIS interface.

This series consisted of three NPDR MISHEMTs. All devices had an L_{FG} = 75 nm, L_{SD} = 1.5 µm, W_G = 2x75 µm, and a stem height of ~ 200 nm. The drain-side GaN Cap sidewall has full metal coverage + 50 nm of lateral field plating over top of it for all devices as well. One device has a ~ 35 nm gap between gate metal and source-side GaN Cap sidewall. One device has ½ of the GaN Cap sidewall covered in metal (~ 15 nm), and the final device in the series has full metal coverage + 35 nm of field plating over top of the sidewall. The location of the gate metal placement relative to the source-side GaN Cap sidewall is also given in Table 5.2. A pictorial representation of this series of NPDR devices is shown in Fig. 5.15.

Device	Gate Metal Coverage of Source-side GaN Cap Sidewall
1	35 nm Gap
2	½ Sidewall Metal Coverage (30 nm)
3	Full Metal Coverage + 35 nm of Field Plating

Table 5.2: Description of each NPDR device investigated in this section of the thesis.

Parameter	Value
L_{fg}	75 nm
L_{SD}	1.5 µm
W_G	2x75 µm
Stem Height	200 nm
Substrate	SiC

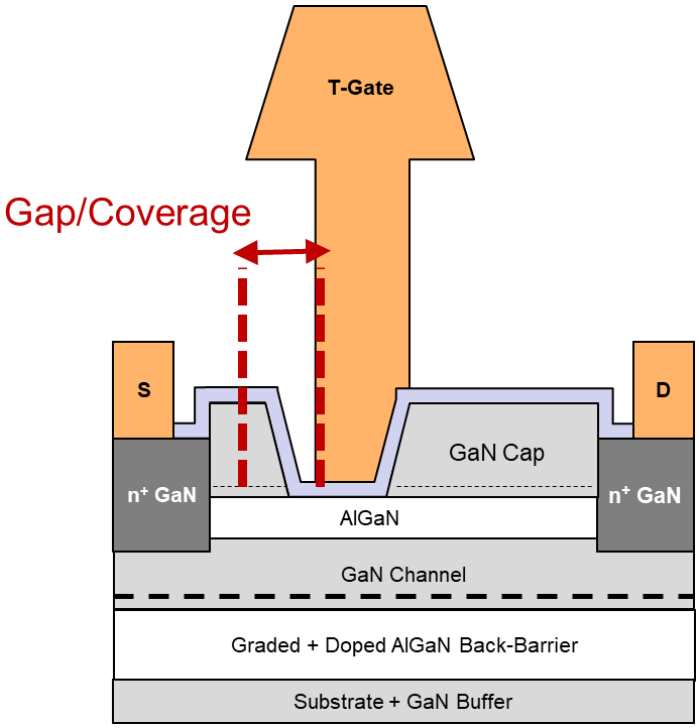

Fig. 5.15: Cross-section of the N-Polar GaN Cap MISHEMT device series investigated in this section of the thesis.

DC measurements were conducted on this series of transistors (Fig. 5.16). A similar extrinsic transconductance and saturation current density were found in the 2 samples where the gate metal overlapped the source-side sidewall. However, both the gm_{ext} and I_{DSS} drop when a gap is introduced between the gate metal and GaN Cap sidewall. Bias-dependent S-parameter measurements up to 67 GHz were then made on this series of devices with a Keysight N5227A PNA calibrated by the LRRM method at the probe tips using an impedance standard substrate [4]. Fig. 5.17 shows the peak de-embedded f_{max} with respect to the amount of gate metal coverage (gap) over the GaN Cap sidewall. Although the C_{gs} decreases when

a gap is introduced between the GaN Cap sidewall and gate metal, so too does the extrinsic transconductance. As a result, only a very small increase in f_{max} is seen when a gap is introduced between the gate metal and sidewall.

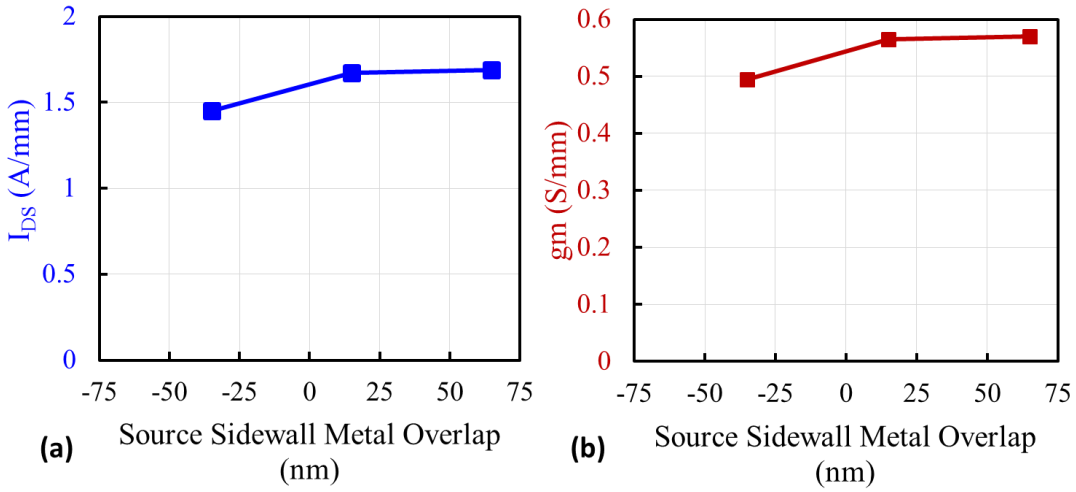

Fig. 5.16: Variation of the (a) saturation current density (V_{GS} = 0 V) and (b) extrinsic transconductance of the device with respect to the gate metal coverage (gap) of the source-side GaN Cap sidewall.

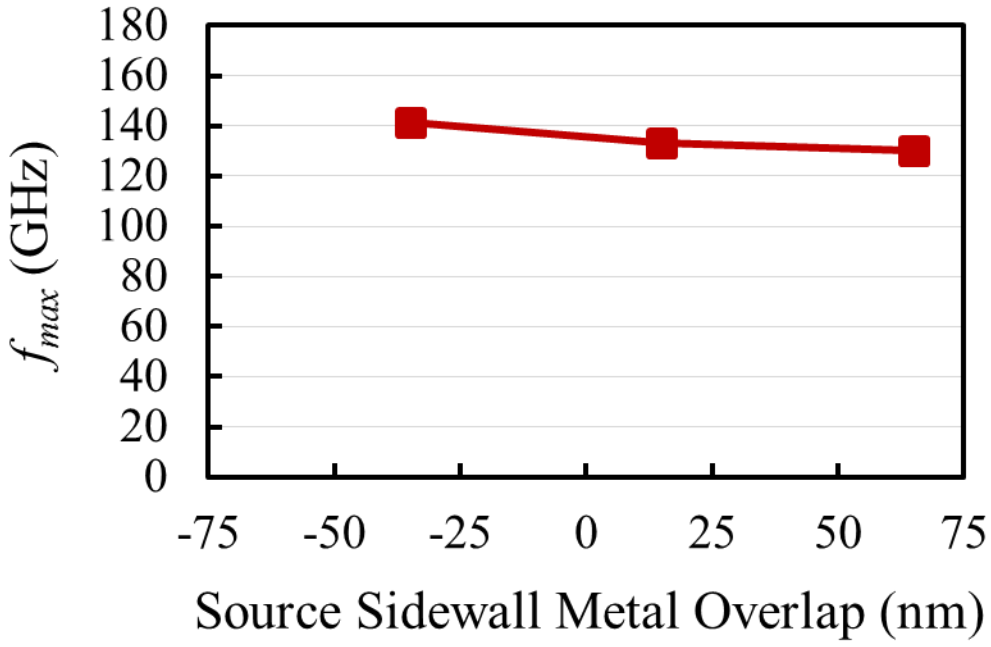

Fig. 5.17: Variation of f_{max} with gate metal coverage of the source-side GaN Cap sidewall. A gap between the gate metal and source-sidewall does not increase f_{max} as much as it did on the drain-side in the previous section. This is likely due to the drop in extrinsic gm as demonstrated in Fig. 5.16.

Taking all the data presented in this section into account, it seems as if a device with full metal coverage of the source-side GaN Cap sidewall is best. Any gap between the gate metal and sidewall decreases the current and transconductance of the device. The decrease in C_{gs} for a device with a gap between gate and sidewall does not lead to an appreciable increase in RF gain either. Further, having no gap between the gate metal and source-side GaN Cap sidewall allows the device to be fabricated without the use of any additional *ex situ* PECVD SiN passivation.

Chapter 5.5 – Summary:

In this chapter a systematic study of the lateral device dimensions and their effect on the overall NPDR T-Gate MISHEMT performance is investigated. From the L_{SD} series, it is determined that a source-drain spacing close to the minimum resolution of the i-line stepper in the UCSB cleanroom delivers the best tradeoff between breakdown/leakage performance and large signal power, gain, and efficiency performance. From the drain-side metal coverage and source-side metal coverage series it is determined that full metal coverage (with no additional field plating) on both GaN Cap sidewalls provides the best tradeoff between breakdown performance, large signal power performance, and efficiency. Fig. 5.18 shows the difference in lateral E-Field within the channel for a device with full metal coverage vs. one where the gate metal is flush with the bottom edge of the drain-side GaN Cap sidewall. Trapping is assumed to be negligible in both devices. It is seen that the peak lateral E-Field is reduced by ~ 22% with the introduction of the gate metal coverage. This helps make such a device more robust when operated at higher voltages/power densities.

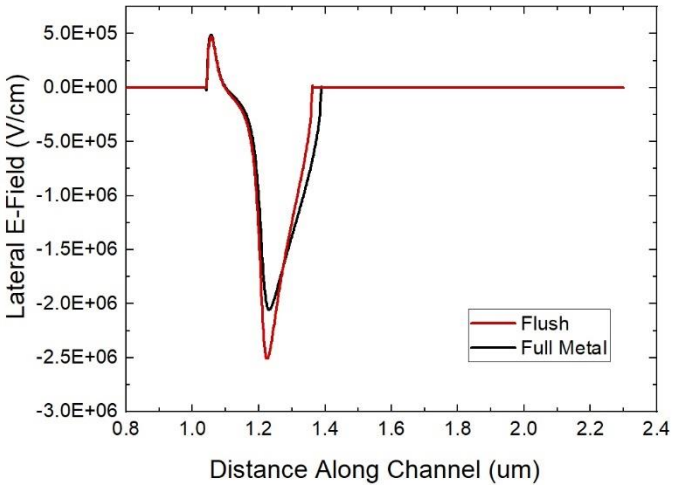

Fig. 5.18: Comparison of simulated lateral E-Field at the GaN channel/AlN interface for the NPDR device where the gate metal is flush with the bottom edge of the GaN Cap sidewall (red line) and the NPDR transistor with Full metal coverage of the slanted sidewall (but no additional lateral field plating – black line). The simulation assumes no dispersion/trapping anywhere in the device. Further, the simulation assumed a 47.5 nm GaN cap, not a 110 nm cap like what is discussed in this section of the thesis. The overall trend should be the same regardless.

However, it is possible that higher gain and efficiency at low drain voltage biases is possible when the gate metal is exactly flush with the bottom edge of the GaN Cap sidewall on both sides. With the current fabrication process, this is very difficult to repeatably achieve, as there is always some misalignment between the gate recess and the foot gate metal of the T-Gate. Our electron beam lithography system has an alignment tolerance of ~ 15 nm. As the gate recess and foot gate Lithographies are done separately, and each are aligned with respect to the initial alignment marks, this means as much of 30 nm of misalignment is possible with this fabrication process. Chapter 3 found that a 47.5 nm GaN Cap seemed best for the NPDR MISHEMT design amongst the 4 GaN Cap thicknesses investigated. An NPDR MISHEMT with a 47.5 nm GaN Cap means that the recessed slanted sidewall will be ~ 30 nm long on both the source and drain sides. A design which nominally has full metal coverage of both sidewalls ensures that no gap will ever occur between the gate metal and any one of

the sidewalls so long as the alignment tolerance of the electron beam is within the tolerance of the system.

References

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[4] M.C.A.M. Koolen, *et al.*, "AN IMPROVED DEEMBEDDING TECHNIQUE FOR ON-WAFER HIGH-FREQUENCY CHARACTERIZATION," *Proc. 1991 Bipolar Circuits Tech. Meeting*, Minneapolis, MN, Sept. 1991, pp. 188−191

Chapter 6 – N-Polar GaN Cap MISHEMT with Record 6.7 W/mm at 94 GHz

Chapter 6.1 – Introduction:

Chapter 4.4 reported on a N-Polar Deep Recess (NPDR) MISHEMT which demonstrated a then record 2.9 W/mm output power density ($P_{RF,out}$) at 94 GHz on a sapphire substrate. The device results reported in this chapter build upon that work in several ways. First, the GaN Cap was reduced from 110 nm to 47.5 nm in order to reduce overall device capacitance and increase the RF gain of the transistor. Second, the findings of Chapter 5 were used to construct an NPDR device with more optimal lateral device dimensions. Finally, the NPDR epitaxial growth was transitions from a sapphire to a SiC substrate to reduce self-heating. Combined, these changes have resulted in over a 2x increase in power density at 94 GHz compared to that which was reported in Chapter 4.4.

Chapter 6.2 – Growth + Fabrication Details:

The sample used in this chapter was grown via metal organic chemical vapor deposition (MOCVD) on a miscut SiC substrate [1]. The epitaxial structure is shown in Fig. 6.1 (a). Devices contain a 3 nm MOCVD SiN_x gate dielectric, a 47.5 nm UID GaN cap layer (access regions only), a 2.6 nm $Al_{0.27}Ga_{0.73}N$ top-barrier, a 9.3 nm UID GaN channel, a 0.7 nm AlN interlayer, a 10 nm UID $Al_{0.38}Ga_{0.62}N$ spacer layer, and a Si-doped graded AlGaN back barrier. An n+ GaN layer regrown by plasma assisted molecular beam epitaxy (PAMBE) takes the place of the GaN cap and $Al_{0.27}Ga_{0.73}N$ top-barrier in the source/drain contact regions. The

fabrication procedure is essentially the same as that for the other samples in this Chapter. However, no PECVD SiN_x passivation layer was added to the device presented here, as the 47.5 nm GaN cap and 3 nm MOCVD SiN_x dielectric were sufficient to eliminate any DC-to-RF dispersion in the device. (Also, the gate and ohmic recesses consisted of only the selective BCl_3/SF6 etch in this case).

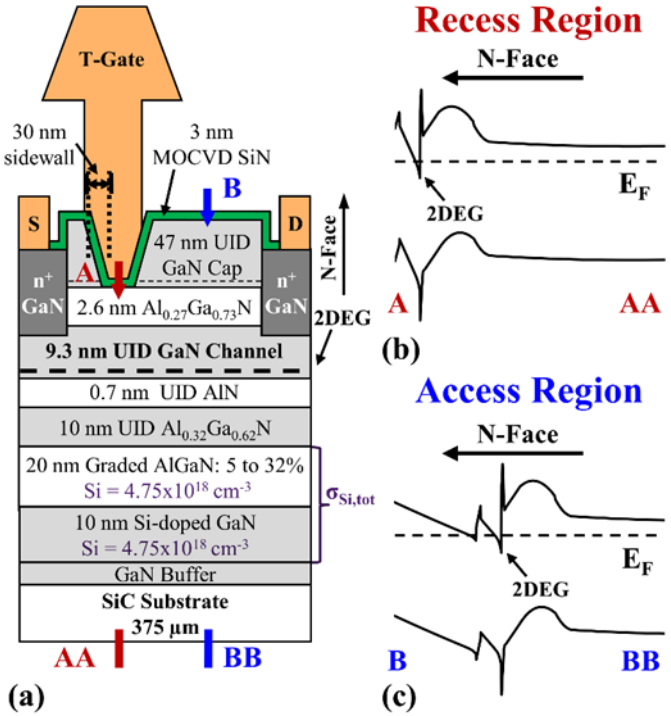

Fig. 6.1: (a) Cross-section of the N-Polar GaN cap MISHEMT device structure (not to scale). Energy band diagram at equilibrium in the (b) gate recessed region and (c) the access region. Simulations assume a Schottky gate structure with a pinning position of 1 eV [2] to eliminate the complexities associated with the MIS interface.

Chapter 6.3 – Device Results and Discussion:

Transfer-length measurements (TLMs) made in the direction parallel to the substrate miscut [1] reveal that the sheet resistance was lowered from 385 Ω/square in the gate recessed region to only 220 Ω/square in the GaN cap access regions.

Device data on a N-polar GaN cap MISHEMT with a 2 x 25 µm gate width (W_G), 45 nm foot gate length (L_{FG}, defined as the physical length at the base of the GaN cap recess),

450 nm top gate length, 125 nm L_{GS}, and 600 nm L_{SD} is presented throughout this section. The sidewall angle in the recessed region is 57^{o} with respect to the horizontal, resulting in a GaN cap sidewall which extends 30 nm laterally and 47.5 nm vertically. The device is constructed such that the foot gate metal nominally covers both the source and drain recess sidewalls (30 nm of lateral metal coverage on each side). However, a small amount of misalignment during the foot gate lithography step caused the T-gate to be shifted slightly (~10-15 nm) towards the source side of the trench. All measurements were made on wafer with a full thickness SiC substrate.

DC and pulsed *IV* (single pulse) characteristics of the transistor are shown in Fig. 6.2. Transfer characteristics at a 5 V V_{DS} reveal a peak extrinsic transconductance of 650 mS/mm (Fig. 2 (a)). At V_{GS} = 0 V, the DC on-resistance and maximum drain-source current density are measured to be 0.61 Ω·mm and 1.9 A/mm, respectively. No current collapse is seen in this PIV measurement, however, the quiescent-bias voltages used in this particular measurement shown in Fig. 6.2 (b) do not constitute a truly rigorous evaluation of trap induced dispersion. A nominally equivalent device on this sample was taken to Teledyne Scientific in order to measure dual PIV under more stringent quiescent bias voltage conditions. The results are shown in Fig. 6.3. Very little DC-to-RF dispersion is seen, demonstrating the effectiveness of the N-Polar GaN Cap MISHEMT design in controlling dispersion.

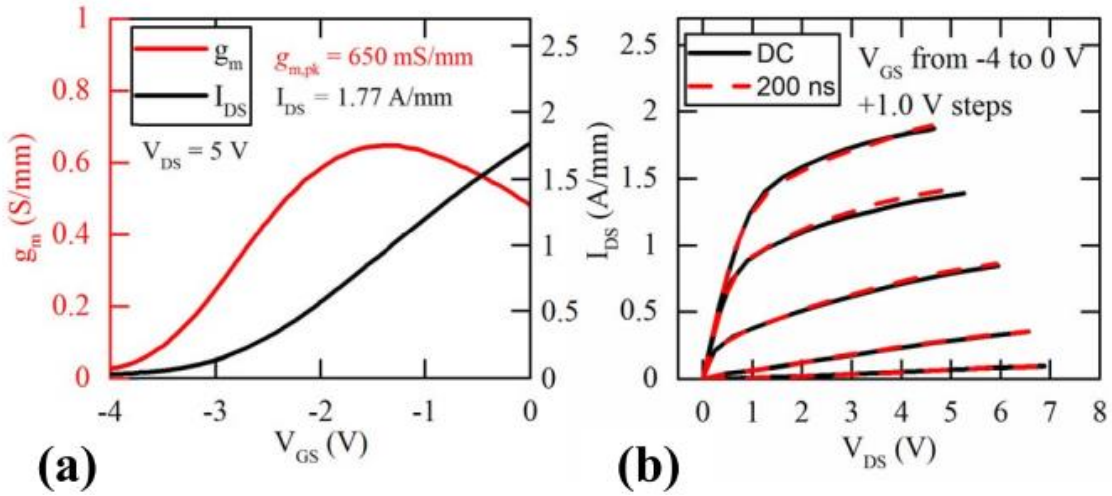

Fig. 6.2: (a) Transfer characteristics of the N-Polar MISHEMT at a V_{DS} = 5 V. (b) DC vs 200 ns Pulsed IV plot. V_{GS} was held at 1.5 V below the -2.5 V threshold voltage of the device (V_{GS} = -4 V) and 200 ns gate pulses with a 10% duty cycle were applied along a 25 Ω load line in +1 V steps until a maximum V_{GS} of 0 V was reached.

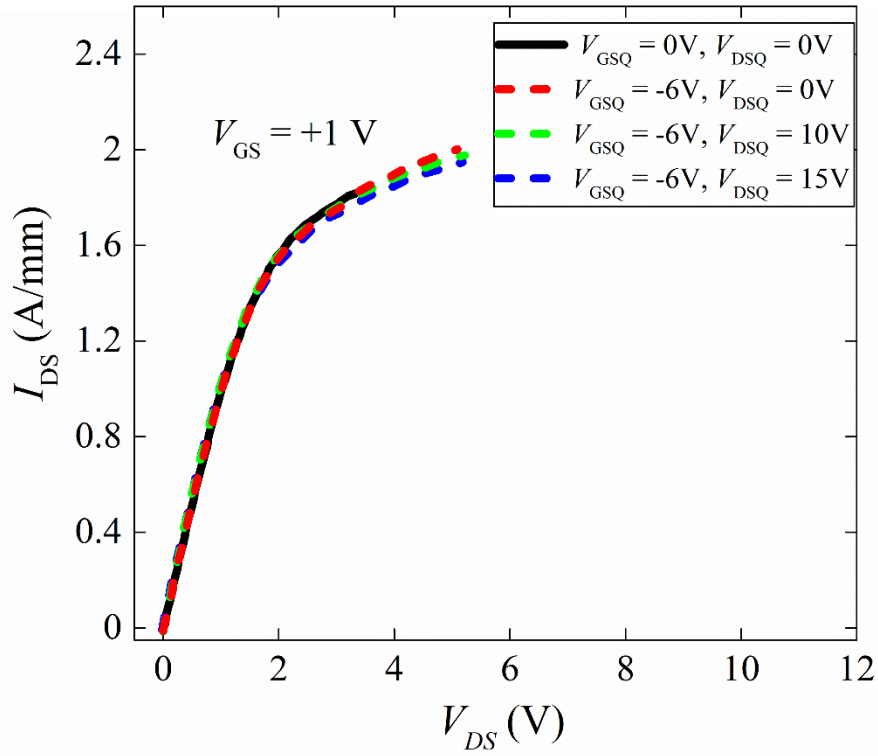

Fig. 6.3: Pulsed IV measurements of the transistor with a 200 ns pulse width. Compares the I_{DS} of the transistor when pulsed to a V_{GS} = +1 V from pinch-off (V_{GSQ} = -6 V, $V_{DSQ} \geq 0$ V) relative to the I_{DS} of the transistor when pulsed from an unstressed state (V_{GSQ} = 0V, V_{DSQ} = 0V). Very little DC-to-RF dispersion is seen, demonstrating the effectiveness of the N-Polar GaN cap MISHEMT design in controlling dispersion.

Bias-dependent S-parameter measurements up to 67 GHz were made with a Keysight N5227A PNA calibrated by the LRRM method at the probe tips using an impedance standard substrate [17]. Pad de-embedded current and power gain cutoff frequency (f_T, f_{max}) values of 112 GHz and 323 GHz, respectively, were simultaneously extracted at a quiescent bias of V_{GS} = −1.75 V, V_{DS} = 13 V, and I_{DS} = 1.03 A/mm (Fig. 6.4 (a)). Fig. 6.4 (b) shows the peak f_T and f_{max} values with respect to quiescent drain voltage bias from 2 to 13 V.

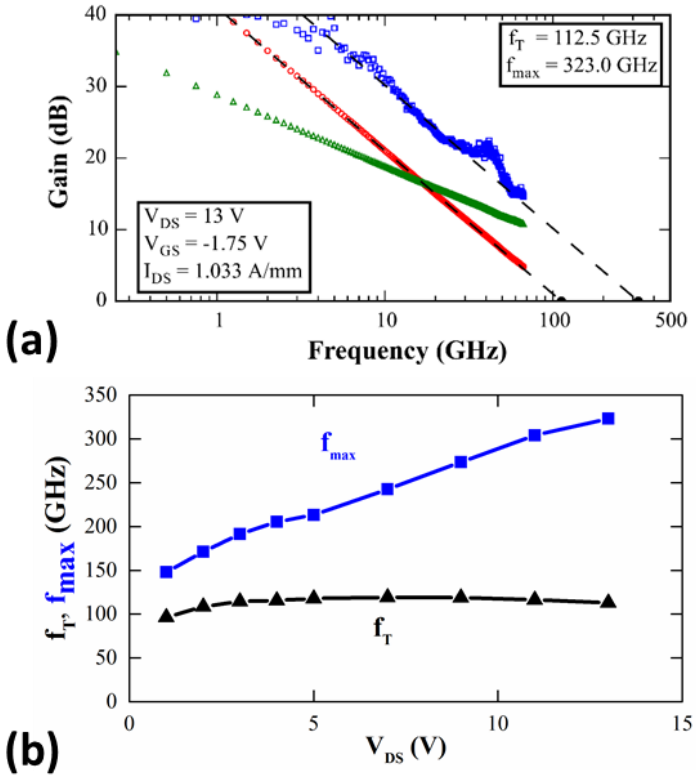

Fig. 6.4: (a) Measured pad de-embedded RF gain at a quiescent bias of V_{GS} = −1.75 V, V_{DS} = 13 V, and I_{DS} = 1.03 A/mm. (b) Peak de-embedded f_T and f_{max} values with respect to drain bias. The reduced self-heating provided by the SiC substrate (compared to Sapphire [2]) allows device gain to scale better with increased drain bias than would be possible with sapphire.

Uncooled continuous wave (*CW*) power performance at 94 GHz was measured using a Maury Microwave passive tuner-based load pull system, described in [3]. The transistor was biased under Class-AB conditions with a nominal quiescent drain-source current density (I_{DS}) of 500 mA/mm. This I_{DS} was chosen to maximize power-added efficiency (*PAE*), as the

peak gain of our device occurs at a relatively high I_{DS} (Fig. 3 (a)), while drain-efficiency (*DE*) is higher at lower I_{DS}. Power sweep data is shown in Fig. 6.5. At a V_{DS} = 16 V and an I_{DS} = 444 mA/m a maximum total output power of 25.26 dBm (336 mW) was measured on the device with an associated *PAE* of 14.4% (Fig. 4 (b)). This corresponds to a very high power density of 6.7 W/mm which, at the time, represents the highest output power density ever recorded for a GaN device measured at W-band. Fig. 6.6 (a) shows P_{out} vs. V_{DS} for this N-Polar MISHEMT in comparison to other W-band III-N HEMT data reported in the literature at the time these device results were published. The output power density of this N-Polar MISHEMT exceeds that of any reported Ga-Polar device by a significant margin and scales extremely well with drain bias, suggesting an RF current swing close to 2 A/mm. Similar RF current densities were also observed from RF-IV during C-band active load pull in Chapter 4. Further, P_{out} continues to scale well with drain bias even at higher V_{DS}, and does not saturate like in our previous work [2] due to a reduction in self-heating from the SiC substrate. Fig. 6.6 (b) illustrates that associated *PAE* stays relatively flat with respect to P_{out} in our transistor. Both sets of scaling behaviors confirm the N-Polar GaN Cap's successful removal of surface-state induced dispersion without the use of an *ex situ* PECVD SiN passivation.

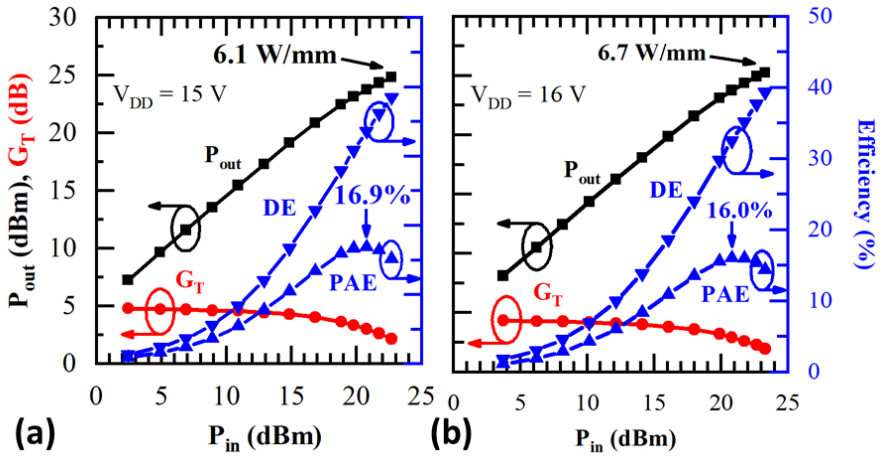

Fig. 6.5: 94 GHz load pull power sweeps at (a) an I_{DS} of 500 mA/mm and a V_{DS} of 15 V and (b) an I_{DS} = 444 mA/mm and a V_{DS} = 16 V. Device dimensions are W_G = 2 x 25 µm, L_{FG} = 45 nm, and L_{SD} = 600 nm.

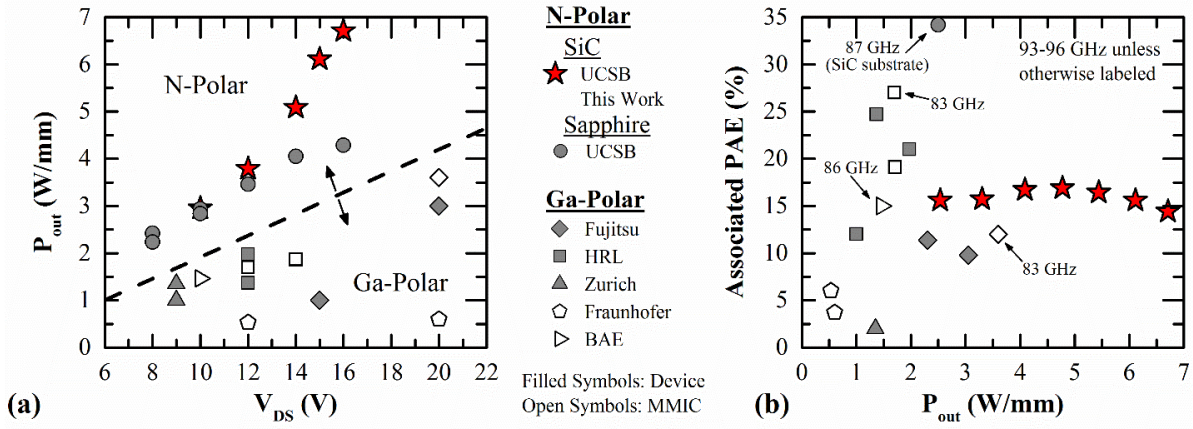

Fig. 6.6: Comparison of W-Band GaN HEMT technologies at frequencies above 83 GHz. (a) N-Polar GaN demonstrates much higher power densities at lower drain-source voltages than competing technologies. Further, P_{out} scales exceedingly well with V_{DS} for this work, and does not saturate at higher V_{DS} like in our previous report [2] due to a reduction in self-heating from the SiC substrate. (b) Plot of Associated *PAE* vs. P_{out} across different W-Band GaN HEMT technologies. The relatively flat *PAE* vs. P_{out} in this work demonstrates the N-Polar GaN Cap's successful mitigation of dispersion. For both plots, open symbols correspond to data taken on MMICs [5-6], [7-11]. Filled symbols correspond to data taken on single device cells wither with or without on-wafer pre-matching [12-17].

A maximum *PAE* of 16.9% with an associated 4.8 W/mm P_{out} was measured at a V_{DS} = 15 V and an I_{DS} = 500 mA/mm (Fig. 6.4 (a)). The *PAE* in this transistor is mostly limited by the transistor's 4.8 dB of linear transducer gain (G_T) at 94 GHz. As mentioned in chapter 4.4, small-signal modeling of this device [4] indicates that the G_T is itself primarily constrained by three factors external to the intrinsic device. First, the device's probe pad layout is not optimal and introduces an undesirably high source inductance. Second, the finite

tuning range on the signal source side prevents the input from being fully conjugate matched. Third, gain is reduced by the presence of substrate modes which exist due to our use of an ungrounded coplanar waveguide on a full thickness (375 μm) SiC substrate. By addressing these external factors, linear G_T can be improved by over 2 dB. Assuming the same gain compression behavior, this improvement in G_T is expected to increase *PAE* to over 22% with no reduction in output power density. A more thorough analysis of the factors impacting G_T in this device, including factors intrinsic to the transistor, is given in [4].

Chapter 6.4 – Summary:

A record output power density of 6.7 W/mm at 94 GHz has been demonstrated with a N-Polar GaN Cap MISHEMT on a full thickness SiC substrate (375 μm) [18]. The output power density scales exceptionally well with drain bias confirming the excellent control over DC-to-RF dispersion provided by this N-Polar GaN Cap transistor design. A clear pathway towards improved gain and efficiency in load pull exists through optimization of the existing probe pad layout and a thinning of the SiC substrate. Additional performance enhancements in gain, efficiency, and power density are expected with further vertical and lateral scaling of the device dimensions. With continued development, the high power density provided by this N-Polar GaN technology should enable greater levels of integration in high-power solid-state transmitter applications with fewer power combining stages required at both the chip and system level.

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Chapter 7 – Conclusion + Summary and Future Work

Chapter 7.1 – Conclusion + Summary:

1) Planar N-Polar MISHEMTs

- Gate Cap Stack Experiment
    - Data suggests that when the gate cap stack is thick enough to prevent premature failure of the dielectric, the semiconductor/dielectric interface is the weak point for breakdown/device failure.
    - Found that AlGaN + MSiN gate cap stack improved breakdown by presenting an additional ΔEc barrier to hot electrons from the channel making it to the semiconductor/dielectric interface and causing breakdown. May also be that AlGaN/MSiN interface is of higher quality than GaN/MSiN or GaN/Al_2O_3 interface. Experiment could not distinguish between these 2 possible causes for why AlGaN/MSiN has highest breakdown voltage
- Back-Barrier Doping + Channel 2DEG Density Series
    - Breakdown voltage scales with the actual channel 2DEG density, not the doping of the semiconductor. When the 2DEG is depleted, the exposed positive charges which induced the 2DEG (either ionized donor states or the net polarization charge at the AlGaN/GaN interface) image primarily on the drain-edge of the gate electrode, increasing the E-Field in the channel.
    - Higher 2DEG charge for the same gate to 2DEG distance increases the $|V_P|$. This increases the vertical E-Field between 2DEG and gate during off-state operation. This is in addition to the higher E-Fields that would be present from

the simple fact that there is a higher density of unscreened positive charges in the depletion region of a HEMT, operated in the off-state, with higher 2DEG density relative to a HEMT with lower 2DEG density. A higher E-Field across the gate dielectric results for a HEMT with a higher $|V_P|$ and higher 2DEG density. If the criteria for breakdown is based on a particular leakage current when the HEMT is in the off-state, this higher $|V_P|$ and 2DEG density may lead to a premature breakdown event where the gate dielectric degrades and leaks enough to satisfy this leakage criteria prior to failure of the semiconductor/dielectric interface. If the gate dielectric is made thicker to reduce this gate leakage, it is possible to increase the breakdown voltage up until the point where the device is limited by the breakdown of the semiconductor/dielectric interface again.

- Alloyed vs. Regrown n+ GaN Ohmic Contacts
    - Achieving high efficiencies and large signal gain at 94 GHz is difficult to achieve in the III-N system. As such, an ohmic contact scheme which provides the lowest possible contact resistance is most desirable. The significantly lower contact resistances attainable through regrown n+ GaN ohmic contacts relative to annealed alloyed contacts would make them the preferred choice in most circumstances at 94 GHz. However, until the many issues detailed in the text concerning alloyed contacts on N-Polar material are solved they are currently unusable for 94 GHz N-Polar transistors.

2) N-Polar GaN Cap MISHEMTs

- N-Polar Deep Recess (NPDR) solution to dispersion

- Use of a UID GaN cap in the access region of the N-Polar HEMT is put forward as the best method for overcoming surface state induced DC-to-RF dispersion at 94 GHz within the framework of the virtual gate model. Further, the orientation of the polarization fields in N-Polar are such that adding this UID GaN Cap greatly enhances the conductivity in the access regions of the transistor. This GaN Cap reduced the sheet resistance in the access regions of the device from 410 Ω/square in the gate recessed region to only 230 Ω/square in the access regions of the N-Polar device.
- Moreover, a fabrication process was developed for producing T-Gate MISHEMTs capable of achieving excellent large signal power performance at 94 GHz. This process borrowed many elements from the fabrication procedures developed by previous Mishra students [1-4].
- With a total Si-doping of $1.65 \cdot 10^{13}$ cm^{-13} in the graded AlGaN back-barrier of the HEMT, a GaN Cap thickness series was performed to find the minimum GaN Cap thickness/pinch-off voltage necessary to eliminate dispersion at all gate-drain bias voltages of interest. With such a back-barrier doping density, the thinnest GaN Cap thickness investigated (t_{cap} = 47.5 nm) was found to provide excellent control of DC-to-RF dispersion within the quiescent voltage bias range of interest. That is, very low dispersion was seen in the device at least until ½ the breakdown voltage of the NPDR MISHEMT, which is approximately the limit one can bias the transistor during large signal operation (as the device will swing as high as 2x the quiescent bias of the device).

- It is possible that an even thinner GaN Cap may provide adequate control of dispersion within the desired range of bias voltages. Further, it is possible that if one desires to decrease the capacitances of the device they could go to an even smaller GaN Cap thickness and limit the transistor to a smaller range of bias voltages. This may allow for slightly higher gain/efficiency at the lower range of bias voltages. However, a GaN Cap thickness below 47.5 nm was not explored in this work.

- With a 47.5 nm GaN Cap thickness, excellent large signal power performance was achieved at X-Band. An RF output power density ($P_{RF,out+}$) of 4.5 W/mm and an associated power-added efficiency (*PAE*) of 67% were achieved on a sapphire substrate at 10 GHz.
    - At 6 Ghz, a similar device demonstrated an RF current swing of over 2 A/mm in RF-IV measurements, demonstrating the excellent control of dispersion afforded by the N-Polar Deep Recess MISHEMT design.
- At 94 GHz, a then record $P_{RF,out}$ of 2.9 W/mm with an associated *PAE* of 15.5% was achieved. A peak *PAE* = 20% with an associated $P_{RF,out}$ = 1.74 W/mm was also achieved on the same sample.
- Lateral device dimensions for the NPDR MISHEMT were then optimized to achieve better large signal power performance at 94 GHz. A smaller source-drain spacing down near the resolution limit which can be repeatably achieved on the i-line stepper at UCSB was found to provide an overall beneficial tradeoff between gate leakage and large signal gain, power, and

efficiency for high frequency power performance. Gaps of ≥ 50 nm between the gate metal and either the source and or drain GaN Cap sidewall were found to cause large amounts of DC-to-RF dispersion, even during relatively unstressful large signal measurements. Further, it was found that even a small gap (~ 15 nm) between the gate metal and drain-side GaN Cap sidewall could cause dispersion during large signal power measurements. The device results from these experiments were taken into consideration when developing the device design for the final fabricated N-Polar GaN Cap MISHEMT of this thesis. An additional consideration was given to the desire to eliminate any gaps from appearing between the gate metal and either GaN Cap sidewall due to misalignment in the electron beam lithography (EBL) system. The fabrication process used to produce T-Gate NPDR MISHEMTs in this thesis has a maximum amount of misalignment equal to 30 nm, so long as the JEOL EBL system at UCSB is within spec.

- Taking all these considerations into account, a final NPDR MISHEMT structure which (nominally) has full gate metal coverage of both sidewalls for a 47.5 nm GaN Cap MISHEMT sample was fabricated on a SiC substrate for reduced self-heating. A record output power density of 6.7 W/mm at 94 GHz with an associated *PAE* of 14.4% was achieved on this sample. At the time, this power density was over 2x higher than the next highest power density for a III-N HEMT at 94 GHz reported in the literature. The particular sample used in this sample had a slightly lower Al composition in the AlGaN back-barrier, as well as slightly higher Si-doping. This caused a secondary 2DEG to form

at the Si-doped GaN/graded + doped AlGaN back-barrier (Fig. 7.1). With the higher Al composition and lower Si-doping used in the NPDR MISHEMTs on sapphire used throughout this thesis, even better large signal power performance at 94 GHz can be achieved with this device design.

Chapter 7.2 – Future Work:

Fabrication Process:

Misalignment of the gate electrode with respect to the gate recess caused some problems for the devices fabricated in this thesis. The true device design was never exactly what was intended due to misalignment in the EBL system. Brian Romanczyk has modified the process in this thesis to create a self-aligned NPDR MISHEMT transistor [5]. In that process, full gate metal coverage of the GaN Cap sidewalls (with no additional lateral field plating) can be consistently achieved. The drawback is that if one wants to have less gate metal coverage in order to reduce the capacitance/increase the gain and efficiency of the transistor at lower voltage biases, they cannot with this fabrication process. Excellent large signal power performance at 94 GHz has been achieved with this self-aligned NPDR MISHEMT design.

Further optimization of the pad layout is necessary to increase the gain and efficiency measured on the NPDR MISHEMT devices. This work has been begun by Matt Guidry and Brian Romanczyk, and a reduction in the inductance of the source pad has been done [6].

If a gate metal flush design is desired, it is possible that an etch stop layer in combination with a sidewall spacer could be implemented with the current process detailed in this thesis. The engineer can deposit an ALD Al_2O_3 etch stop within the gate recess followed

by an ALD SiO_2 deposition. A low power fluorine based etch could be used to etch the SiO2 at the floor of the gate recess down until the Al_2O_3, while not etching all the way through the SiO_2 deposited on the sidewall of the GaN Cap. The Al_2O_3 in the floor of the gate recess can be wet etched away selectively in a TMAH based developer. The T-Gate can be deposited in the recessed area. Afterwards, a dilute BHF dip can be used to remove the ALD Al_2O_3 and SiO_2 on the sidewall, in turn creating an air gap between the gate metal and GaN Cap, which can increase gain and efficiency at lower biases. However, not having any gate metal on the drain-side GaN Cap sidewall will reduce the maximum source-drain voltage bias which can be applied to the device. If increasing large signal gain and efficiency are more important than increasing the output RF power density of the current NPDR MISHEMT at 94 GHz, this may be a worthwhile tradeoff.

Moreover, a Si-doping series for the n+ GaN regrown contacts should be performed to find the minimum possible contact and sheet resistance that can be obtained. As the source-drain length has been shrunk appreciably to 600 nm in the final device structure, much of the source and drain resistances come from the contacts, and diminishing returns will occur for further shrinking of the source-drain distance without reducing the contact resistances.

A number of methods can be used to improve the breakdown and gate leakage performance of the NPDR MISHEMT reported in this thesis. After the selective gate recess, several cycles of UV ozone + HF dips could be used to remove the remainder of the AlGaN top-barrier in the HEMT. When the device is put back into the MOCVD reactor, a higher AlGaN top-barrier can be regrown prior to the deposition of the MOCVD SiN gate dielectric. Such a scheme may reduce the gate leakage and possibly lead to a higher breakdown voltage in our device.

Moreover, the MOCVD SiN on the sidewall of the GaN Cap can be made thicker without hurting the aspect ratio of the gated 2DEG at the floor of the gate recess. After the selective gate recess, a thicker MOCVD SiN could easily be deposited on the sample during the regrowth of the gate dielectric. In this case, an additional electron beam step is introduced to lithographically pattern only the base of the gate recess. Multiple UV ozone + BHF dip cycles could be performed to get the desired aspect ratio at the base of the gate recess. The electron beam resist would, however, protect the MOCVD SiN on the sidewalls of the GaN Cap. This would allow the MOCVD SiN to remain thick on the sidewalls, and potentially reduce gate leakage and increase breakdown voltage of the transistor if the sidewall contribution to these parameters is significant. A small variation to this idea could leave a small gap at the edges of floor of the recess, so that the corners of the to-be-deposited foot gate electrode are positioned over top of a thicker gate dielectric than in the rest of the gate recess. As the peak electric field in the device occurs at the drain-edge (corner) of the foot gate electrode, having a thicker gate dielectric specifically in that location should reduce gate leakage and potentially increase breakdown voltage as well. The biggest challenge for this idea is dealing with the misalignment of the EBL system during the EBL lithographies.

Further, multiple AlGaN insertion layers could be grown in the GaN Cap to raise the conduction band in the access region. If designed correctly, these AlGaN insertion layers can increase the Conduction Band enough such that no 2DEG is induced in the GaN Cap, while having little effect on the 2DEG in the primary channel of the device. This is important because the GaN Cap 2DEG will deplete while the device is in the off-state, thus increasing the E-Field and lowering the breakdown voltage of the device. However, the AlGaN top-barrier which induces the GaN Cap 2DEG limits the contribution to source-drain

conduction current from this 2DEG. Thus, the GaN Cap 2DEG hurts the off-state performance of the NPDR MISHEMT without actually helping the on-state performance. Eliminating this 2DEG should help off-state device performance while simultaneously having a minimal impact on the on-state performance.

The proposed ideas for increasing breakdown voltage and reducing gate leakage are not mutually exclusive and can be used in concert with one another to achieve the goal.

Finally, more vertical/lateral scaling of the transistor to improve the gain of the NPDR transistor should also be pursued. This is problematic with the current GaN channel design used throughout this thesis. This is because as the GaN channel is shrunk, the 2DEG wave function is pushed further into the AlN/AlGaN back-barrier of the N-Polar HEMT [7]. This decreases the mobility and velocity of the channel 2DEG. However, this can be at least partially alleviated if an $In_xGa_{1-x}N$ layer replaces at the portion of the channel nearest the gate electrode. Because of the very large coefficients of spontaneous polarization for InN [8], a very large percentage of the total voltage drop between top of the MOCVD SiN gate dielectric and the channel 2DEG will occur across the $In_xGa_{1-x}N$ layer. This relaxes the electric field in the GaN portion of the channel and increases the distance between the AlN interlayer and the centroid of the 2DEG. This has already been demonstrated to increase the electron mobility in Hall measurements [9].

Chapter 7.3 – Conclusion:

Finally, excellent large signal power performance at 94 GHz has been achieved with this N-Polar GaN Cap MISHEMT device structure. An output RF power density of 6.7 W/mm, more than 2x higher than anything reported in the literature at the time of

publication [10-14], is demonstrated. Implementation of some of the ideas in this section should lead to even better performance. With continued development the future of the NPDR MISHEMT for power amplification purposes at W-Band and possibly other frequencies looks very bright.

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