UNIVERSITY of CALIFORNIA
Santa Barbara

Growth, Fabrication, and Characterization of Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers

A dissertation submitted in partial satisfaction of the
requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

SeungGeun Lee

Committee in charge:

Professor Steven P. DenBaars, Chair
Professor Shuji Nakamura
Professor Jonathan Klamkin
Professor James S. Speck

December 2018

The dissertation of SeungGeun Lee is approved:

_____

Shuji Nakamura

_____

Jonathan Klamkin

_____

James. S. Speck

_____

Steven P. DenBaars, Committee Chair

December 2018

Growth, Fabrication, and Characterization of
Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers

by

SeungGeun Lee

Acknowledgements

My past five years at UCSB have been a time of struggling and learning from many unsuccessful results, which led me to the final success in the end. I am grateful to get a good result in this project which was considered to be difficult. It would not be possible without the support of many individuals.

At first, I would like to thanks to my advisor Prof. DenBaars for supporting my Ph.D study with many encouragements from the beginning to the end. His support on many ideas helped me to experience in all the time of research. It has been a pleasure to be a member of his group.

I would also thanks to my co-advisor Prof. Nakamura. His continuing interest in the VCSEL project has led this project continued and gave me a chance to work on this. By working on this project, I have gained knowledge from the fundamental of materials to the device characteristics.

Besides my advisors, I would like to thank the rest of my thesis committee: Prof. Speck and Prof. Klamkin, for their insightful comments and question which incented me to widen my research perspectives.

I am also grateful to all staff scientists, especially Dr. Dan Cohen. He is one of the most knowledgeable people in our research group in the field of lasers. All discussions, advices, and encouragements guided me until the end of my research. Dr. Stacia keller gave me an idea and analysis for tunnel junction growth and epitaxial analysis. Additionally, I would thank Dr. Tal Margalith for

managing group meetings and encouraging graduate students with his work experience.

I would also like to acknowledge the past and present graduate students who worked on the VCSEL project together. Especially, Dr. John T. Leonard spent his precious time teaching me all basics including growth, fabrication, characterization, and simulation. He is one who proposed BTJ VCSEL at the first time, which now became the topic of my dissertation. I am also thankful to research with Dr. Charles A. Forman who was my research and office mate. It was always grateful to discuss the project and to share ideas on daily basis. I would not be able to gain all my result without his suggestions and analysis. Jared Kearns and Joonho Back brought ideas I have never thought about. I hope that they achieve better result than what I got.

My thanks also go to researchers who worked on TJ project. Dr. Erin Young spent her time to grow MBE TJ contact for VCSEL projects. Dr. David Hwang shared his result for MOCVD-grown TJ contacts from which I have started. Dr. Abdullah Alhassan also shared his idea and discussed about it.

I would like to thank Dr. Changmin Lee for talking about all matters including research and life. He is the second person with whom I discussed the most for the project. Dr. Sang Ho Oh was one who also thought me about LEDs from basics to packaging. Haojun Zhang started to study together for graduated

classes and the screening exam in UCSB. We struggled together from the very beginning of our graduate years.

Lastly, I would also like to thank my friends and family, Mom, Dad, and brother in the USA and Korea for their continual support. This truly would not have been possible without them.

Curriculum Vitae
SeungGeun Lee
December 2018

Education

University of California, Santa Barbara (UCSB)

- Doctor of Philosophy, Electrical and Computer Engineering
  June 16 – present
- Master of Science, Electrical and Computer Engineering Sep 13 – June 16
- PhD Advisor: Prof. Steve Denbaars
- PhD Co-advisor: Prof. Shuji Nakamura
- PhD Committee: Prof. Steven P. DenBaars, Prof. Shuji Nakamura, Prof. James S. Speck, Prof. Jonathan Klamkin
- Dissertation Topic: Growth, Fabrication, and Characterization of Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers

Illinois Institute of technology

- Bachelor of Science, Electrical Engineering Jan 09 – Dec 10

Inha University, South Korea

- Bachelor of Science, Electronic Engineering Feb 04 – Dec 08

Work Experience

- Graduate Student Researcher Sep 14 – present
  Solid State Lighting and Energy Center (SSLEC)
  Electrical and Computer Engineering, UCSB
  Developed processes for the growth and fabrication of m-plane III-N VCSELs.
- Application Engineer July 13 – Feb 11
  Samsung Electronics Co., Ltd, Korea
  Worked as a verification and support engineer for Samsung's SoC processors.

Teaching Experience

- Teaching Assitant Sep 10 – Dec 10
  Illinois Institute of technology
  Taught undergraduate embedded system course.

Publications

- **S. Lee***, et al. (2018); GaN-based vertical-cavity surface-emitting lasers with tunnel junction contacts grown by metal-organic chemical vapor deposition, Applied Physics Express, 11: 062703.
- **S. Lee***, et al. (2017); Smooth and Selective Photoelectrochemical Etching of Heavily Doped GaN:Si Using a Mode Locked 355 nm Microchip Laser, Applied Physics Express, 10: 011001.
- C. A. Forman, **S. Lee***, et al. (2018); Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers, SPIE, 83.
- C. A. Forman, **S. Lee***, et al. (2018); Continuous-Wave Operation of m-Plane GaN-based Vertical-Cavity Surface-Emitting Lasers with a Tunnel Junction Intracavity Contact, Applied Physics Letter. 112: 111106.
- C. Lee, C. Zhang, D. L. Becerra, **S. Lee***, et al. (2016); Dynamic characteristics of 410 nm semipolar ($20\bar{2}\bar{1}$) III-nitride laser diodes with a modulation bandwidth of over 5 GHz, Applied Physics Letter. 109: 101104.
- J. T. Leonard, B. P. Yonkee, D. A. Cohen, L. Megalini, **S. Lee***, et al. (2016); Nonpolar III-nitride vertical-cavity surface-emitting laser with a photoelectrochemically etched air-gap aperture, Applied Physics Letter. 108: 031111.
- J. T. Leonard, D. A. Cohen, B. P. Yonkee, R. M. Farrell, T. Margalith, **S. Lee***, et al. (2015); Nonpolar III-nitride vertical-cavity surface-emitting lasers incorporating an ion implanted aperture, Applied Physics Letter. 107: 011102.

Conference Presentations

- **S. Lee***, et al. (2018); A violet III-nitride vertical-cavity surface-emitting laser with a MOCVD-grown tunnel junction contact. CLEO: Science and Innovations
- **S. Lee***, et al. (2018); MOCVD tunnel junction with in-situ activated buried p-GaN. ICMOVPE
- C. A. Forman, **S. Lee***, et al. (2018); Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers. SPIE Photonics West
- C. A. Forman, **S. Lee***, et al. (2017); Nonpolar GaN-based vertical-cavity surface-emitting lasers, Photonics Conference (IPC)
- C. Lee, C. Zhang, D. Becerra, **S. Lee***, et al. (2016); High speed performance of III-nitride laser diode grown on (2021) semipolar plane for visible light communication, Photonics Conference (IPC)

- C. Lee, C. Zhang, D. Becerra, **S. Lee***, et al. (2016); High-speed performance of III-nitride 410 nm ridge laser diode on (20$\bar{2}$1) plane for visible light communication. In Compound Semiconductor Week (CSW)

Patents

- **S. Lee***, et al. "MOCVD Tunnel Junction with As-Grown Activated Buried p-GaN," Docket 30794.672-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- C. Forman, **S. Lee***, et al. "III-Nitride Surface-Emitting Laser and Method of Fabrication," Docket 30794.662-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- C. Forman, J. Leonard, **S. Lee***, et al. "Buried Tunnel Junction Aperture for III-Nitride Surface Emitting Lasers," Docket 30794.629-US-P1, Prepared by Gates & Cooper LLP, Sept. 2016 (provisional patent).

Academic Honors and Awards

- Outstanding Graduate Student Research Achievement Award — Nov 18
  UCSB Solid State Lighting and Energy Center (SSLEC)
- Doctoral Student Travel Grant, UCSB — 2018
- Outstanding Graduate Student Research Achievement Award — Nov 17
  UCSB Solid State Lighting and Energy Center (SSLEC)
- Special Promotion, Samsung Electronics Co., Ltd — 2013
- Innovation prize, Samsung Electronics Co., Ltd — 2012
- Dean's List Honors: All semesters for two years, IIT — 2009 – 2010

Abstract

Growth, Fabrication, and Characterization of

Nonpolar III-Nitride Vertical-Cavity Surface-Emitting Lasers

by

SeungGeun Lee

III-N vertical-cavity surface-emitting lasers (VCSELs) can be used for various applications including data communications, displays, optical sensors, and atomic clocks. However, III-N VCSELs have never been commercialized because of difficulties in fabrication, reliability, and high power lasing. From past few years, we have intensively developed VCSEL performance as well as reliability. We started to get milliwatt-class VCSELs under pulsed operation along with the maximum output power of 2.8 mW. This advancement could be achieved by applying new aperture design and developing overall processing steps. We also investigated thermal characteristics of VCSELs. Then, a VCSEL with a metalorganic chemical vapor deposition (MOCVD)-grown tunnel junction (TJ) contact and a buried tunnel junction (BTJ) VCSEL were demonstrated for the first

time. Finally, the maximum output power of 726 μW under CW operation was achieved.

In the first chapter of this dissertation, motivations and applications of III-N VCSELs are presented along with introduction of VCSEL designs. In the second chapter, trials to optimize the VCSEL structure are demonstrated. Especially, the GaN TJ contact is intensely studied to replace a hybrid MOCVD/ molecular beam epitaxy (MBE) growth technique. Lastly, break down voltage of lightly doped p/n-GaN junction is verified for BTJ current aperture design. In the third chapter, processing steps are described for BTJ VCSELs and ion implant aperture (IIA) VCSELs. In the fourth chapter, optical and electrical characteristics of processed AII VCSELs and BTJ VCSELs are demonstrated and analyzed. Then, thermal analysis and effects were separately discussed. In the final chapter, conclusion and future works are mentioned.

Contents

1. Introduction of III-N VCSELs

III-N vertical-cavity surface-emitting lasers (VCSELs) have received high interest due to their possible emission spectral regimes for attractive applications, such as displays, optical sensors, communications, and atomic clocks [1]–[6]. As shown in figure 1.1, band gaps of GaN-based crystals can be engineered by growing them with aluminum and indium to create a light spectrum from UV to visible range [1], [7], [8]. However, III-N VCSELs have not been commercialized because of the difficulties in processing and poor device characteristics; low optical output power and high threshold current density. Firstly, these problems come from material properties, such as a high number of defects, wide band gap, and low injection efficiency [1], [8]. Moreover, high lattice mismatches among GaN, AlN, and InN, make it challenging to grow high quality of epitaxial distributed Bragg reflectors (DBRs) [8]–[11]. Despite these difficulties, the performance of III-N VCSEL with various designs has been improved since the first demonstration of electrically pumped lasing in 2008 [9]. Sony first demonstrated a VCSEL with over one milliwatt (mW) output power in 2016 [12], then Meijo university continuously reported 6 mW and 15.7 mW output powers in 2018 [13], [14]. These continuing improvements in III-N VCSELs will make it promising for use in various applications.

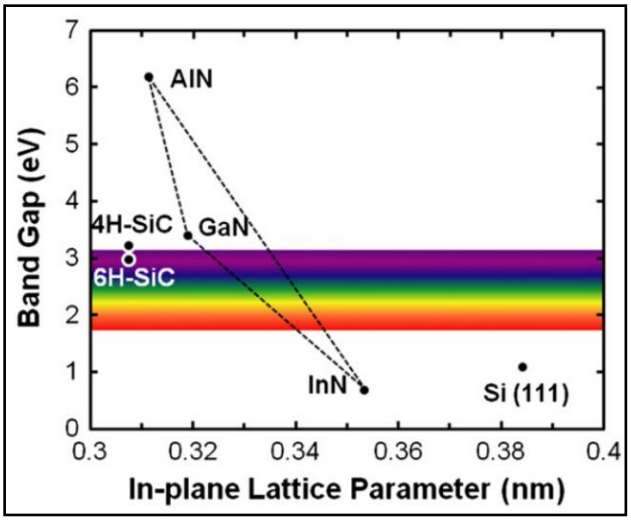


Figure 1.1 Band gaps versus lattice constants of c-plane GaN and its related alloys. [7]

In this chapter, possible applications will be discussed, which motivate developing III-N VCSELs. Then, various designs will be described focusing on the choice of DBRs, current apertures, and current spreading layers.

1.1. Applications

Fiber-optic communication is the first field where GaAs-based VCSELs were commercialized as multimode transceivers using their fast frequency response and narrow full width half maximum (FWHM) [8], [15]. Since the first production, VCSEL transceivers have been one of the main applications in VCSEL markets [8], [15]. Well-developed III-N VCSELs will also have the same device characteristics due to their small device and thin cavity. However, the technology of III-N VCSELs is still immature compared to GaAs- and InP-based

VCSELs [8], [13], so possible future applications should be where these unique characteristics are advantageous. For example, blue LEDs have been studied for underwater communication due to the high penetration depth of blue light as illustrated in figure 1.2 (a) [16]–[18]. Well-developed blue VCSELs will have even more advantages for fast rate communication in underwater systems. Figure 1.2 (b) illustrates the possible purposes of different device types and wave types in the underwater environment [2], [3], [18]. In addition, plastic optical fiber (POF) has low attenuation from blue to green light as shown in figure 1.3. POF's main advantage over the glass product is its robustness under bending and stretching which can be used in digital home appliances, home networks, industrial networks, and car networks [8]. GaN-based materials are the most promising candidates for blue and green light VCSELs.

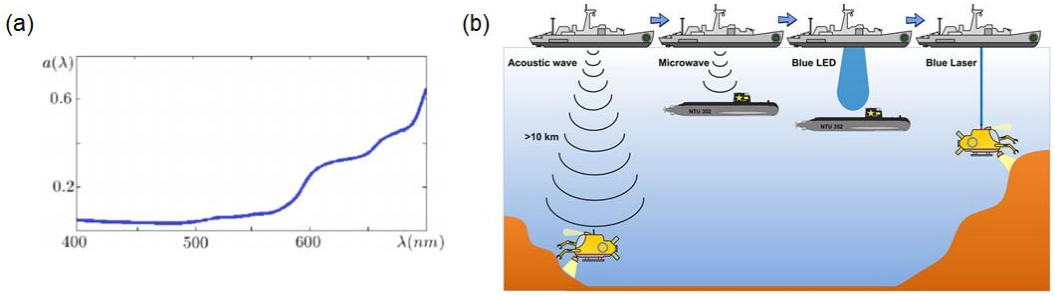


Figure 1.2 (a) Absorption spectrum of open ocean and (b) Schematic of acoustic wave-, microwave-, blue LED-, and blue LD-based [17], [18].

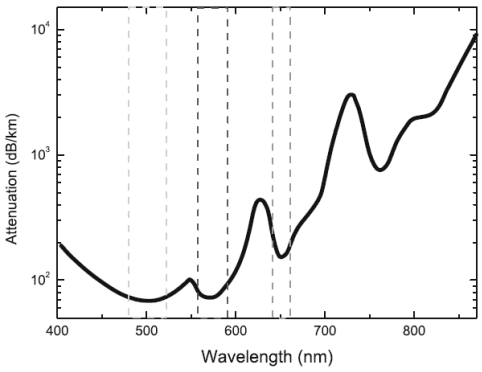


Figure 1.3 Attenuation of standard step-index plastic optical fiber in various wavelengths [8]. The dashed lines indicate the regions of attenuation minima in the visible spectral range.

VCSELs are compact, efficient, and low-cost sources for optically pumped atomic clocks, when the emission wavelengths of single-mode VCSELs are designed to interact with atomic transitions [8], [19]. In particular, III-N VCSELs lasing at 369.5 nm are possible to use for compact Yb^+ atomic clocks as shown in figure 1.4 [20], [21]. This allows the construction of chip-scale atomic clocks, with volumes of below 1 cm^3. For such applications, single-mode VCSELs with stable polarization should be achieved.

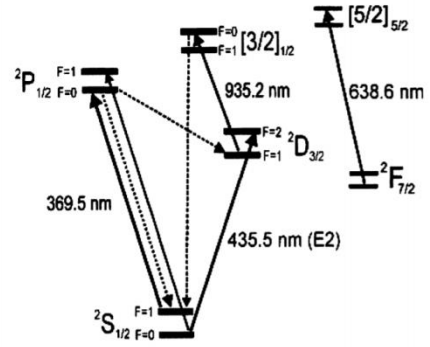


Figure 1.4 energy level scheme of the 171 Yb 435.5 nm electric-quadrupole clock. The transition at 369.5 nm is used for cooling the ion and the electric quadrupole transition at 435.5 nm is the clock transition [21].

Gas and bio sensing and analysis through absorption spectroscopy using tunable diode lasers are of industrial importance in various fields including research and medicine [22], [23]. Detection techniques are based on wavelength modulation spectroscopy, and sweeping emission wavelength through specific absorption lines. The use of tunable VCSELs is more advantageous than other types of diode lasers due to tuning range, response time, power consumption, and beam quality. In addition, ultraviolet lasers for fluorescence of biological material can also be used for detecting pathogens such as aerosolized bacterial spores and viruses [22], [24].

Currently, numerous companies are focusing on developing displays using uLEDs, which are expected to have advantages over organic LED (OLED) displays in terms of energy efficiency, lifetime, resolution, response time, color reproduction, and brightness. These benefits have a very high demand for portable devices such as smart glasses, watches, and phones as well as televisions. III-N is the only semiconductor material possible to be used as blue and green light sources. For future displays, III-N VCSELs can be used to improve even more the resolution, response time, and color reproduction, while using a similar platform because they also emit lights from the surface as uLEDs. Another approach for displays is projecting images on glasses away from projectors. Intel demonstrated smart glasses using VCSELs as illumination sources and lenses as holographic reflectors. However, only monochromatic texts could be demonstrated, probably

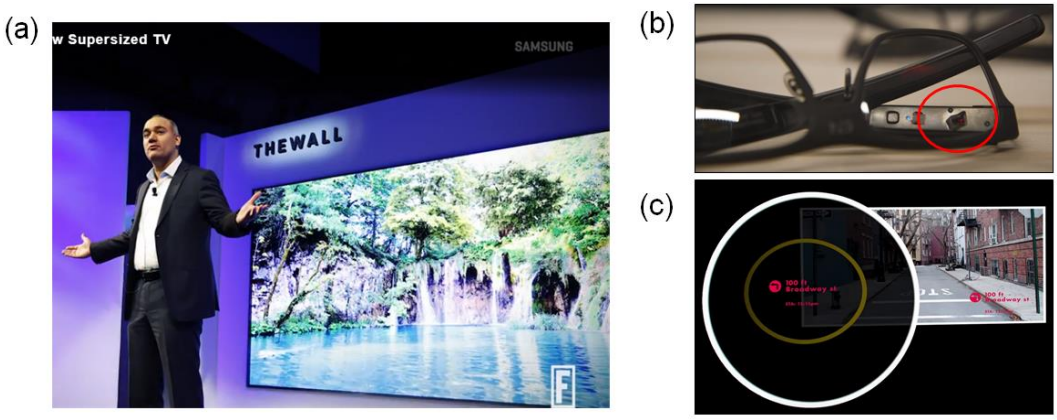


Figure 1.5 (a) 146 in modular TV demonstrated in CES 2018, (b) smart glasses using red VCSELs, and (c) an illustration showing image from users [25], [26].

because GaAs-based VCSELs emitting red light are only commercially available in the visible range. Development of III-N VCSELs for blue and green light will enable all visible color ranges.

In addition to the applications discussed above, there are numerous other possible applications for III-N VCSELs in the area of sensing, communication, illuminations, and displays [1], [8]. Further development of III-VCSELs, in terms of growth, fabrication, and analysis, will enable these applications.

1.2. Design

Figure 1.6 illustrates a diagram of a flip-chip III-N VCSEL. The VCSEL requires highly reflective mirrors, commonly comprised of DBRs, on the top and at the bottom to trap most of the lights inside a cavity [8], [15]. Because these mirrors are usually resistive, current spreading layers are required on each side of

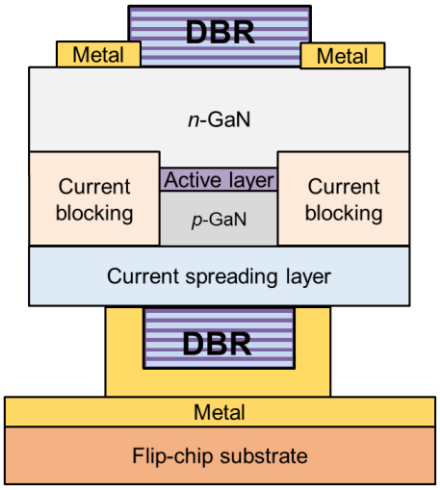


Figure 1.6 Diagram of a III-N flip-chip VCSEL

an active layer. Then, the current blocking area is also needed to confine the current inside the cavity to prevent current flowing out of the mirrors. Although other types are present, main components composing VCSELs are not very different. In this chapter, the characteristics of various mirror designs, current spreading layers, and current blocking methods for III-N VCSELs will be discussed.

1.2.1. Distributed Bragg Reflectors

Compared with edge-emitting lasers, VCSELs require highly reflective mirrors with a reflectance of over 99% due to the small confinement factor. Most of the VCSELs use distributed Bragg reflectors (DBRs) to achieve such high reflectance, which is comprised of multiple layers with varying refractive or

effective refractive indexes. When the thickness of each layer is a quarter of the optical thickness of vacuum wavelength, the reflections combine with constructive interference, so the total reflection acts as a high reflector. Typical DBR designs are categorized as dielectric and epitaxial DBR. Both designs have pros and cons as follows.

In general, reported VCSELs used dielectric DBRs SiO_2/Ta_2O_5, SiO_2/Si_3N_4, or Nb_2O_5 for violet and blue VCSELs [5], [10], [12], [27], [28]. Because of high refractive index differences between two dielectric materials, dielectric DBRs have wider stopband than epitaxial DBRs as shown in figure 1.7, which will be more tolerant of processing errors. Dielectric DBR also requires just 10~16 periods to get reflectance > 99%, while epitaxial DBR requires > 40 periods. However, dielectric DBRs also have several disadvantages. Because dielectric materials are mostly not conductive, intracavity contacts are necessary which require current spreading layers. Current density will gradually decrease from the out to the center of the apertures, which makes large sized devices disadvantageous. Dielectric materials also have low thermal conductivities which will trap heat inside the cavity. For fabrication matters, dielectric DBRs cannot be easily placed on the backside of cavities, n-side, while they can be easily deposited on another side. Nevertheless, several methods have been proposed for bottom dielectric-DBRs, such as mechanical polishing, epitaxial lateral overgrowth (ELO), and photoelectrochemical (PEC) etching [29]–[31]. Bottom

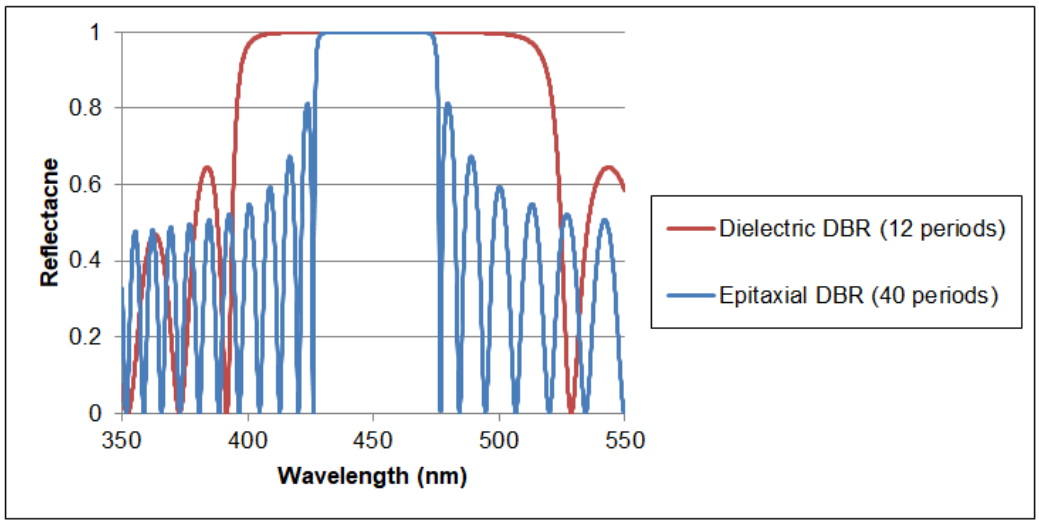


Figure 1.7 Reflectance of 12 periods of SiO_2/Ta_2O_5 DBR and 40 periods of AlN/GaN DBR simulated using Vertical. Index dispersion and optical loss were ignored.

DBR can be deposited after removing the sapphire or GaN substrate using mechanical polishing and photoelectrochemical (PEC) etching. Unlike mechanical polishing, selective PEC etching is a proper method to precisely define cavity thickness. However, PEC etching is still difficult to use for epitaxial structures grown on c-plane because the etchant solution reacts with the nitrogen face of GaN, -c-plane, causing rough surface morphology. Without removing the original substrate, epitaxial structures can be over grown on existing dielectric DBRs using ELO techniques.

In contrast, using epitaxial DBRs overcomes several issues of dielectric DBR structures. For example, the main cavity structure can be directly grown on the epitaxial DBR which does not require flip-chip process. And also using doped

layers, epitaxial DBRs can be made to be conductive, which overcomes the current spreading issue though doping might increase the optical loss inside the DBRs [13]. However, it is still challenging to grow because of the small refractive index difference and the big lattice mismatch between GaN, AlN, and InN. Over 40 periods of GaN/AlInN stacks have been slowly grown to overcome the issues [32]. Hybrid dielectric/epitaxial DBR VCSELs have been reported. They also reported that output power through epitaxial DBR is higher than through dielectric DBR, which implies that reflectance of the dielectric DBR is still higher than the epitaxial DBR. Despite these difficulties, they have been reported as the highest output power using the hybrid DBR structure [33].

Though epitaxial and dielectric DBRs are only types which have been used for electrically pumped III-N VCSELs, there are also other possible candidates. For example, using electrochemical (EC) etching, highly doped layers

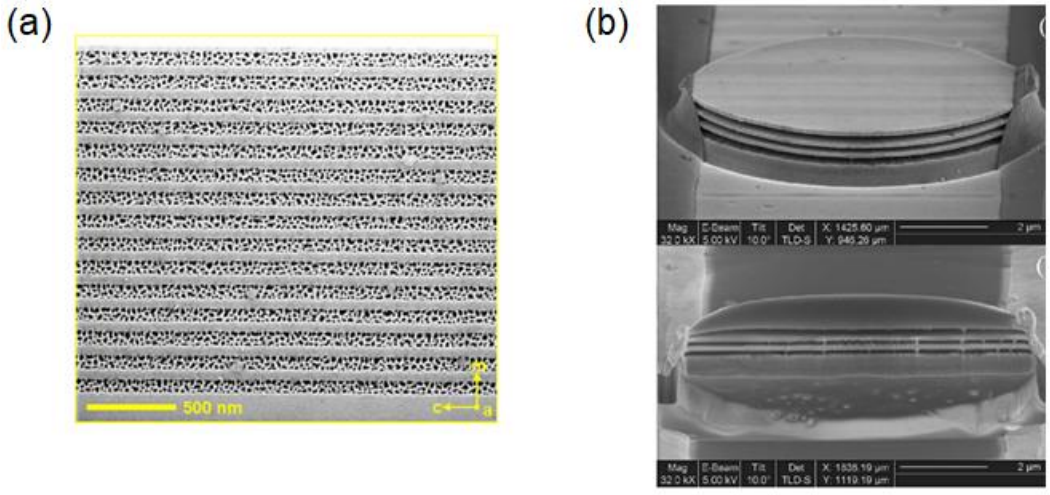


Figure 1.8 SEM images of (a) nanoporous and (b) air-gap DBRs [34], [35].

can be etched as in figure 1.8, which changes effective refractive indexes [36]. Using the nanoporous structure on stacks of different n-type GaN layers, DBR can be constructed which shows reflectance of ~98 % [34], [37], [38]. Using nanoporous DBRs optically pumped VCSELs were also demonstrated [39]. Another example is using the PEC selective etching to fabricate air-gap DBRs. However, a reported air-gap DBR shows a maximum reflectance right above 50 % which is not enough to use for VCSELs [35]. One reason why the reported air-gap DBR does not show high reflectance could be because the epitaxial structure was grown on a c-plane substrate. Because the bottom of the structure is a nitrogen face, it is reactive in an HCl solution without a light source which roughens the surface morphology. Higher reflectance will be achieved using an epitaxial structure grown on an m-plane substrate.

1.2.2. Current Apertures

DBR and aperture design are one of the main structural points deciding the performance of VCSELs. GaAs-based VCSELs have shown drastically improved output power since the oxide current aperture was used, though the aperture design is difficult for the employment in III-N VCSELs [8]. The most common approaches are using the dielectric aperture including SiO_2 and Si_3N_4 or ion

implantation apertures, including aluminum and boron ions for III-N VCSELs [5], [12], [31], [40].

Dielectric films have been commonly used as current blocking layers in many semiconductor devices. Therefore, deposition of dielectric materials is well developed to use for VCSELs. Moreover, many dielectric films, including SiO_2 and Si_3N_4, are almost optically lossless in the visible wavelength range and have lower refractive indexes than GaN, which can enhance lateral optical confinement. However, dielectric films out of aperture generate step-like structures which may cause optical anti-guiding in VCSEL cavities [33]. Furthermore, low thermal conductivities of dielectric materials increase the overall thermal impedance of VCSELs, and these low thermal conductivities can limit VCSEL performances under CW operation. In addition, III-N tunnel junction (TJ) structures are difficult to apply due to the limitation of continuing crystal growth on dielectric materials.

The next common method to block current flow is using ion implantation. III-N materials implanted with certain ions, such as Al and Br, become electrically resistive because of implantations damages [6], [12], [40]–[42]. Unlike dielectric film, ion implantation allows continuous epitaxial growth on current blocking layers, which is necessary for III-N TJ structures. The surface also remains flat after implantation. However, additional internal loss is added from increased material absorption caused by the ion implantation damage [40]. So the proper VCSEL design with ion implantation aperture will be where optical

overlap with the implanted area is minimal. For example in GaAs-based VCSELs, ion implanted apertures are usually used for large-sized VCSELs without intracavity contacts, because optical overlap with the implanted area is relatively small in large-size apertures and the current spreading issue is rare without intracavity contacts. In contrast, III-N VCSELs have been generally used in intracavity contact design which is inappropriate for large-sized apertures due to current spreading issues. Therefore, ion implantation aperture may not be the best option for most current III-N VCSEL designs.

Another reported approach is using air-gap current aperture defined by etching an active layer using the PEC technique [43]. This design is very similar to GaO current aperture of GaAs-based VCSELs which has become the standard aperture design due to many benefits, such as lateral confinement, low optical loss, and possible regrowth. Air-gap apertures also improve lateral optical confinement and almost perfectly block current flow. However, the void area makes the structure physically fragile and increases thermal impedance.

Buried TJ (BTJ) current aperture is another concept used in GaAs- and InP-based VCSELs because this aperture has many benefits, such as lateral optical confinement, low thermal impedance, low internal optical loss, and possible epitaxial overgrowth [8], [15], [44]. However, BTJ has not been demonstrated for III-N VCSELs because of difficulties to form effective III-N TJ contacts until our first demonstration. The BTJ VCSEL design is the main topic of

my dissertation and details will be covered in the following chapters from processing to characteristics.

1.2.3. Current Spreading Layers

In n-side, n-GaN is used as current spreading for most of the reported III-N VCSELs because n-GaN has high conductivity and low optical loss as well as being convenient to use. In contrast, p-GaN is too resistive to use for current spreading, which requires other current spreading layers for VCSELs as well as other III-N devices.

Indium tin oxide (ITO) as a current spreading layer on p-GaN layer has been commonly used for III-N VCSELs as well as LEDs [1], [6], [13], [31], [32], [45]. Well-developed ITO will have high conductivity, smooth surface morphology, and low contact resistance with optimized p^{++}-GaN. One critical downside is its optical absorption causing high internal loss for VCSELs. This effect has been minimized by depositing only a thin ITO film and placing the null of an optical mode at ITO in III-N VCSELs. ITO has been the most common material used for III-N LEDs for a long time and there are not many alternatives, so most of the III-N VCSELs have been using ITO except several VCSEL reports from UCSB.

III-N TJs with n-type layers are a promising alternative to replace ITO for contacts and current spreading on p-GaN layers. When the heavily doped p-n junction layer is reversely biased, electrons can tunnel from the valence band to the conduction band. In addition to the highly doped n^{++}-GaN in the TJ, a thicker n-GaN layer can be grown to reduce electrical and thermal impedance while having lower optical loss than ITO and p-GaN [5], [28], [46], [47]. Moreover, TJs offer more flexibility to design various structures, such as buried TJ current apertures and dual epitaxial DBRs as demonstrated previously in GaAs- and InP-based VCSELs. Despite these benefits, only a few III-N TJ VCSELs have been reported because of difficulties in achieving effective TJ contact. Fortunately, efficient TJ contacts have been achieved at UCSB and applied for III-N VCSELs for the past few years. More details will be covered in chapter 2.2.

Other transparent conductive oxides (TCOs) will also be possible candidates. For example, lower optical loss of ZnO than ITO has been reported, which allows depositing thicker layer for better heatsink while having lower optical absorption than ITO [48]. However, possible usability should be carefully contemplated because ZnO has a lower conductivity than ITO.

2. Optimization for VCSEL structure

The performance of a VCSEL is a result of several factors, and each factor can be separately analyzed and improved. When these improved factors properly apply to new devices, the final device will show better performance. VCSELs have complicated structure, so it is impossible for few researchers to perfectly investigate all components in their time. Before the actual VCSEL processing, we also checked some area, which we believed was critical for performance and yield. Among these trials, we got a good result in TJ contacts, so their possible future use for VCSELs was investigated.

In this chapter, some epitaxial calibration processes were investigated. Then, characteristics of PEC etching were observed. Lastly, efforts to achieve MOCVD-grown TJ contacts and BTJ structures will be discussed.

2.1. Epitaxial Optimization

VCSELs processed with quality epitaxial structures will have a higher chance to show good performance. But personally, optimizing epitaxial structure was one of the most difficult works because of variations of each growth as well as its complexity. Sometimes, I got different quicktest output powers and wavelengths grown by the same recipe. In this chapter, therefore, I will mention

more general information based on experimental data, which I believe is repeatable.

2.1.1. Surface Morphology

For VCSEL structures, smooth surface morphology is necessary to reduce scattering loss. We want to have epitaxial structures with RMS surface roughness below 1 nm. There will be many factors that determine the surface morphology for MOCVD growth, such as temperature, carrier gas flows, and reactor design. In this chapter, I will first discuss Si doping concentration of the n-GaN layer influencing the surface morphology. Then, the surface morphologies on the actual VCSEL sample before and after MOCVD regrowth will be investigated.

Choosing the right thickness and doping concentration of n-GaN layers is somewhat complicated. A thick cavity design will be beneficial for current spreading and heat dissipation but is disadvantageous for single-mode lasing and total internal optical loss [41], [49]. Moreover, a high Si doping concentration for

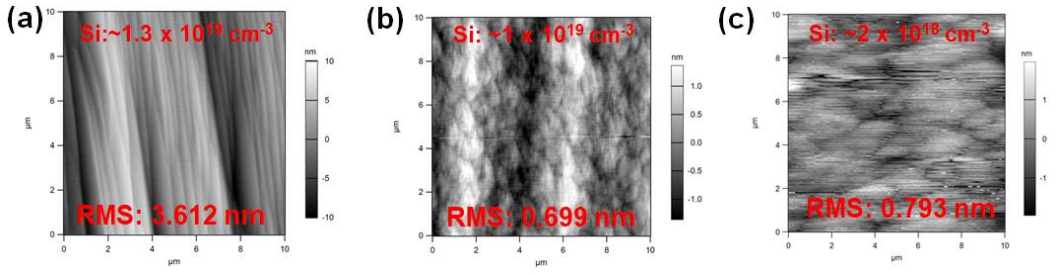


Figure 2.1 Surface morphologies measured by AFM on (a) ~1.5 µm, (b) ~1.5 µm, and (c) 2.8 µm n-GaN on a template grown with TMG.

n-GaN layers will improve conductivity but increase free carrier absorption which will increase internal loss [50], [51]. Furthermore, surface morphology will come out rough when Si doping concentration is higher than criteria in a certain growth condition [52]. Figure 2.1 shows surface morphologies of the Si-doped n-GaN layers grown with three different SiH_4 flow rate; (a) 10 sccm, (b) 8 sccm, and (c) 1.5 sccm. The doping concentrations in the AFM images were calculated based on secondary ion mass spectrometry (SIMS) data of n-GaN layers grown with SiH_4 flow rates of 1.88 sccm and 6 sccm, assuming that the doping concentration was linearly proportional to SiH_4 flow rate. While figure 2.1 (b) and (c) shows similar surface morphology, the n-GaN (Si: 1.3 x 10^{19} cm^{-3}) sample showed rough surface, which had a little higher doping concentration than the n-GaN (Si: 1 x 10^{19} cm^{-3}). The criteria point of Si doping concentration causing rough surface morphology seemed in somewhere between 1x10^{19} cm^{-3} and 1.3x10^{19} cm^{-3}. Because of this reason, I have avoided growing n-GaN with Si doping concentration above 1 x 10^{19} cm^{-3} except for contacts.

Next, surface morphologies were also measured during actual IIA VCSEL processing. The information of the epitaxial structure is described in table 4.1 (chapter 4.1.1). As shown in figure 2.2, the surface roughness became worse after regrowth probably due to the highly doped 40 nm n^{++}-GaN layer and residues left before regrowth. Nevertheless, the regrown sample showed RMS roughness

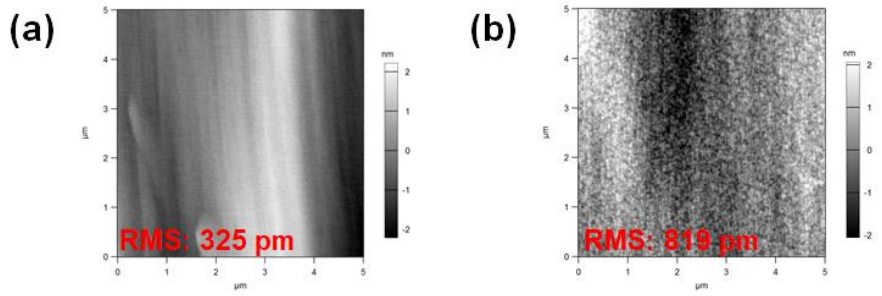


Figure 2.2 Surface morphologies measured by AFM during IIA VCSEL processing (a) before and (b) after TJ regrowth.

below 1 nm which was much better than MBE regrown TJ structures[41]. One of the benefits of growing full structure only by MOCVD rather than by hybrid MOCVD/MBE is smooth surface morphology on m-plan with -1° miscut to c-direction because favorable miscut for MBE growth on m-plane is +1° miscut to c-direction [41]. The result also means that thicker n-GaN layer can be regrown by MOCVD without sacrificing surface morphology, which will improve current spreading and heatsink. The regrowth with a smooth surface will be also necessary for dual epitaxial DBR designs.

2.1.2. X-ray Diffraction (XRD) measurement

Knowing accurate thickness and composition will be critical for VCSEL cavity designs. For instance, a VCSEL designed to place mode peak at an active layer and mode null at a p^{++}-GaN layer might unintentionally have mode null at the active layer and mode peak at the p^{++}-GaN layer, which will cause low

confinement factor and high optical loss (chapter 2.1.2.2). I frequently used XRD to measure thickness and composition on test structures. In this chapter, several experimental aspects, concerning about calibrating growth rate and composition, will be dealt based on XRD data.

Proper epitaxial structures might be different depends on their purposes such as indium composition and plane. Table 2.1 describes typical XRD structures I used to calibrate each layer for violet VCSELs, which gave thickness fringes clear enough to be fitted. If a thickness of a GaN layer is too thin or thick, its fringes will be too wide or small to be fitted. Compared with other layers, the thickness of p^{++}-GaN in table 2.1 (a) was a bit thinner. It is because thick p^{++}-GaN sometimes makes the intensity of peaks weaker. It might be due to Mg clustering and rough surface morphology [53], [54]. The InGaN XRD structure in table 2.1 (c) might be controversial because the top of the InGaN layer could be etched

Table 2.1 Epitaxial structures grown for XRD calibration.

(a)

Layer	Thickness (nm)	Composition (%)
p^{++}-GaN	~ 50	
p-AlGaN	20 ~ 25	15 ~ 25
Template		

(b)

Layer	Thickness (nm)	Composition (%)
n-, n^{++}-, UID, and *p*-GaN	~ 100	
n or p-AlGaN	20 ~ 30	15 ~ 25
Template		

(c)

Layer	Thickness (nm)	Composition (%)
InGaN	~ 24	~ 9
Template		

during the cool down step at the end of MOCVD growth. To investigate how much InGaN will be etched away during the cool down, experiments were performed.

2.1.2.1 InGaN layer

Figure 4.19 illustrates test samples for InGaN calibrations. Sample 2 had an UID GaN cap layer to protect InGaN from being etched during the MOCVD cooldown. Sample 3 had a superlattice structure to reduce any relaxation effects. Table 2.2 shows XRD fit results. For the fitting, the thickness of UID GaN was separately measured. As described in table 2.2, sample 1 showed only 3% of the growth rate difference compared to other structures. Therefore, it is hard to be concluded if InGaN was etched during cool down step because sample 1 showed even thicker InGaN than sample 2. In PL measurement, sample 1 showed longer

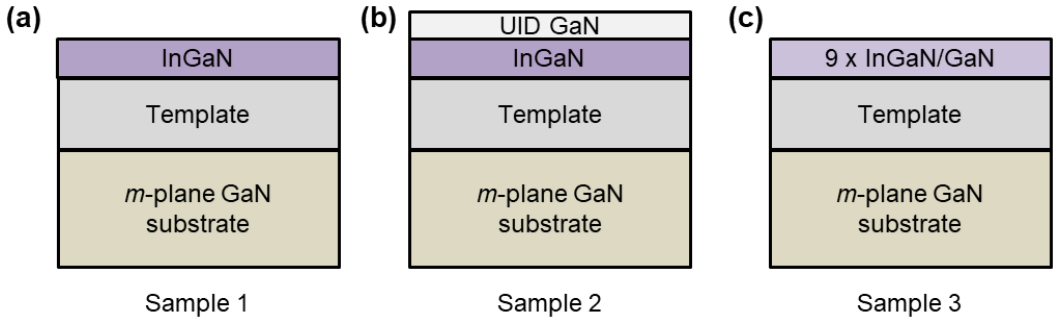


Figure 2.3 Epitaxial structures grown for InGaN XRD calibration (a) without a cap layer and with (b) an UID GaN cap layer and (b) a superlattice structure.

Table 2.2 XRD measurement results fitted using Global fit and PL wavelength peaks.

	Thickness (nm)	Indium Composition (%)	Growth rate (nm/min)	PL peak (nm)
Sample 1	28	8	6.47	396.5
Sample 2	27.2	8.52	6.29	400.0
Sample 3	9 x 3.3/2 (InGaN/GaN)	8.4	6.67	

wavelength than sample 2, which explains composition difference in XRD data. These differences will be due to a variation of the growth rather than structural matter. Sample 3 does not show a huge difference with other structures as well. It will be just because 28 nm InGaN with 8% indium composition was not thick enough to be relaxed, which can be different for longer wavelength QWs. The InGaN layer of sample 1 might be etched during cool down. However, the etched thickness seems smaller than growth variations. Because all structures showed similar results, I choose to sample 1 for my XRD calibrations because it is simplest and is not affected by variations of the GaN growth condition.

Two software is commonly used in our group for XRD fitting; Global fit and X`Pert. However, Dr. Christopher Pynn pointed out that the parameters of X`Pert may not be accurate for semipolar. Thus, it was briefly checked for m-plane as well. Using X`Pert, I could get similar thickness but higher composition for sample 1 as shown in figure 2.4. Just for rough calculation using equation (2.1) where b is 4.4 eV and x is InGaN composition [55].

$$E_g(x) = 3.50(1-x) + 1.95x - bx(1-x). \quad (2.1)$$

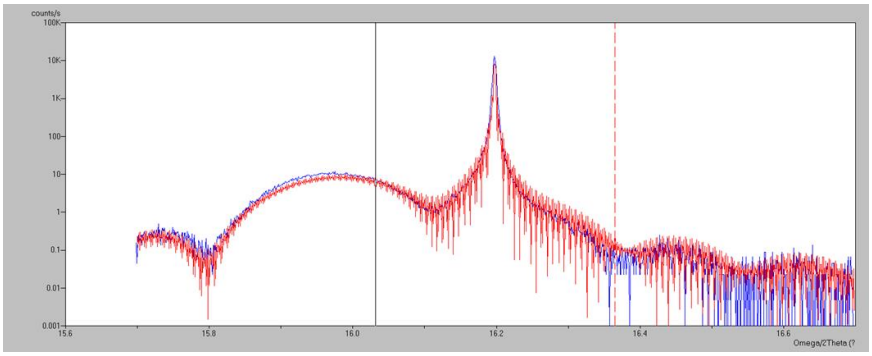


Figure 2.4 (blue) XRD measurement of sample 1 and (red) fitting by X`Pert. The simulation matches with a thickness of 27.5 nm and an indium composition of 10.7% for InGaN.

8% (Global fit) and 10.7% (X`Pert) indium compositions for InGaN correspond to the wavelength of 406.27 nm and 425.94 nm, respectively. Considering its PL peak at 396.5 nm, Global fit seems better for m-plane than X`Pert. The difference between 406.27 nm (calculation) and 396.5 nm (PL) may be due to the equation (2.1) referencing for a bulk c-plan GaN.

2.1.2.2 Growth Variation

VCSEL structures are designed based on refractive index and cavity thickness. We place an active layer at the peak of optical mode to maximize enhancement factor and lossy layers at the null to minimize internal loss. Then, the epitaxial structures are grown following a simulated design. Thus, it is important to know accurate growth rates for each layer before the growth. However, I have experienced a variation of growth rates time to time.

Several XRD measurement results for n-GaN layers grown in similar conditions are plotted as shown in figure 2.5. When the growth condition was exactly the same, 1~5 % difference in the growth rates were found. These variations may come from changes of the MOCVD chamber caused by maintenance and residues from previous growth. Furthermore, errors may also come from the XRD fitting. For instance, thickness fringes of 99~101 nm n-GaN layer from XRD measurement do not show a significant difference, which means that we may have errors of ±1% only from the fitting. The errors might be even bigger for thinner layers in XRD samples, such as p^{++}-GaN and AlGaN. Even for a sample grown right after an XRD measurement, it will be proper to assume that the thickness of each layer may have < 5% error. It means that, when an active

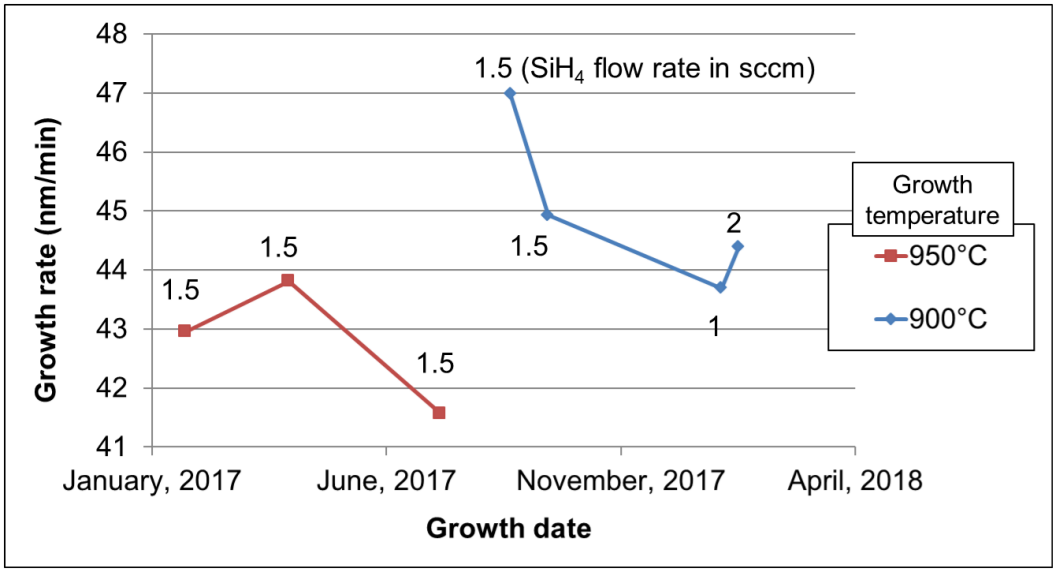


Figure 2.5 Growth rates of ~100 nm n-GaN layer measured by XRD grown in different days. SiH_4 flow rates were labeled above each point. Beside growth temperature and SiH_4 flow, other growth conditions were designed the same.

layer is designed to be placed 5-λ away from a peak of optical intensity, it may be at the null instead of the peak due to the 5% error. In our flip-chip design, the mode peak usually begins from the end of p-DBR when no spacer is used on the p-side. Thus, it may be risky to have thick layers on p-side in this perspective.

2.2. III-N Tunnel Junction Contacts

In this dissertation, the TJ means a junction composed of highly doped p- and n-type semiconductors for electrons to tunnel through from the valence band to the conduction band when a high voltage is applied on n-type; reverse bias in a diode [1], [50]. So, the GaN TJ contact means a contact between p^{++}-GaN and n^{++}-GaN. Despite it usually has higher contact resistance than metal contact, TJ contacts have been generally used for GaAs- and InP- VCSELs because an n-type current spreading layer can be regrown right above the TJ contacts [8], [15]. Lower optical absorption and high conductivity of n-GaN make it attractive for VCSEL current spreading. Furthermore, epitaxial regrowth is necessary for the top DBR of dual dielectric DBR VCSEL design.

However, growing GaN TJ contacts using MOCVD poses several physical and technical challenges. One of the issues for MOCVD-grown GaN TJs is Mg activation for a p-GaN layer covered by n-GaN layers. The n-GaN capping layer prevents activation by performing as a strong barrier to hydrogen diffusion [56].

p-GaN activation by sidewalls has been reported [57], [58]; however, this method limits the freedom of device design and size because of the limitation of diffusion length of hydrogen. Furthermore, hydrogen diffusion could also be constrained by ion implantation, which has been widely used to form current confinements of III-N VCSELs [4]–[6], [59]. Thus, growing TJ structure with activated p-GaN offers more flexibility in device design.

In this chapter, trials to optimize the GaN TJ contact will be demonstrated based on experimental results including doping concentration, surface treatment, and in-situ activation. Then, the optimized TJ contact will be analyzed with SIMS data.

2.2.1. Processing for TJ Test Samples

To optimize the GaN TJ contacts, many LED test samples were grown with variations of several factors including p-type doping, n-type doping, and surface treatment. Following is processing steps for a representative test sample.

At first, the main epitaxial structure was grown by MOCVD on a bulk m-plane GaN substrate with an -1˚ miscut in the c-direction. The main structure was composed of an n-GaN template (~1 μm), 5 QWs (3 nm/ 2 nm InGaN/GaN), p-GaN (100 nm), and a p^{++}-GaN contact layer (10 nm). The sample was then taken out of the chamber and treated in BHF for 5 min to reduce Mg on the surface of

p^{++}-GaN [53], [57]. The Mg may diffuse into the regrown n^{++}-GaN layer, which might compensate n-type doping. To activate the p-GaN, the chamber temperature was held at 750℃ for 5 min, during the temperature ramp up to 900℃ for n^{++}-GaN regrowth as shown in figure 2.6 (b). The TJ structure was composed of 40 nm n^{++}-GaN (Si: ~1 × 10^{20} cm^{-3}), 100 nm n-GaN (Si: ~1.8 × 10^{18} cm^{-3}), and 5 nm n^{+}-GaN (Si: ~1 × 10^{19} cm^{-3}). Then, Ti/Au was deposited by electron-beam (e-beam) evaporation for p-side contacts. To define circular mesa, ~200 nm was etched by reactive ion etching (RIE) using Ar/Cl_2 plasma. This etching step should be processed carefully because over etching might cause sidewall leakage. Lastly, the back side of the substrate was soldered with indium for n-side contacts. Final structure is illustrated in figure 2.6 (a).

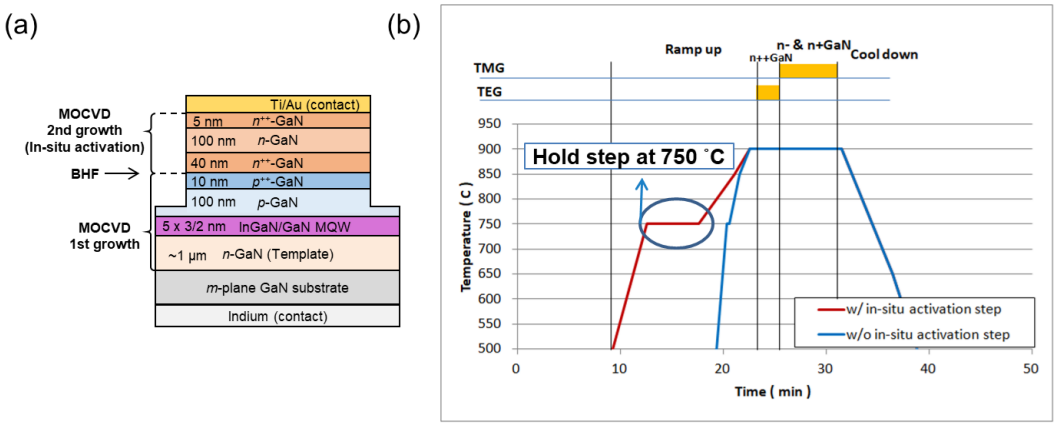


Figure 2.6 a) An illustration of a TJ test structure and b) regrowth temperature setting with and without in-situ activation step. The temperature setting is different from real growth condition because of temperature waiting steps at 750℃, 850℃, and 900℃ during the ramp up.

Even after I-V measurement, it is uncertain whether the current is flowing through the TJ contact or other paths, such as sidewall leakage and defects. Moreover, we might end up activating from the sidewall during the process. The simplest method to verify if the TJ contacts are properly working is observing light from the top as shown in figure 2.7 (a). If somehow the sample was activated from the sidewall, we should see gradual degradation from out to the center. However, we have observed uniform light extraction from the top on the entire surface which means that it was activated as grown. To verify the sidewall leakage, the light from the backside was also measured as shown in figure 2.7 (b). If the mesa etch passes through the active layer, it will cause a leakage path through the sidewall. As a result, almost no light was observed at low current until it is actually turned on (blue). Comparatively, the light output power from the properly etched sample (red) shows linear increment. This will be difficult to be

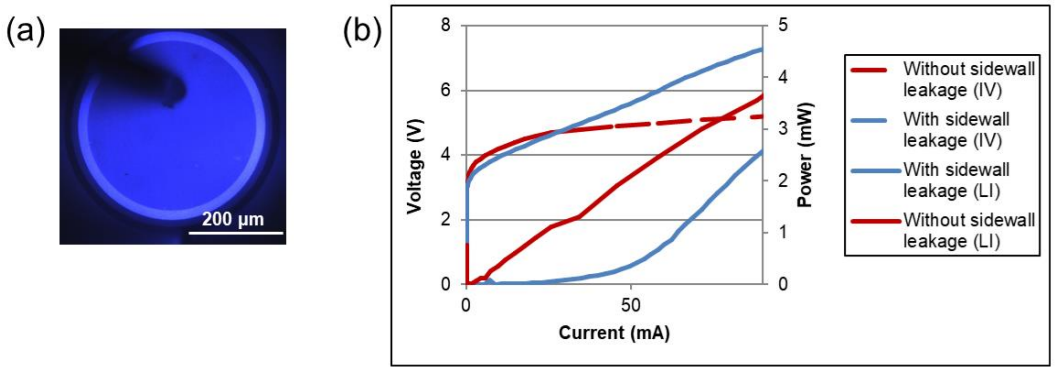


Figure 2.7 (a) Microscope image during EL measurement for a test sample with 200 µm radius of aperture and (b) L-I-V curve of test sample with and without sidewall leakage. (a) To observe light illumination through the top, thin metal (5/5 nm, Ti/Au) was used for top contact. (b, blue) Mesa etch passed active layer which caused sidewall leakage.

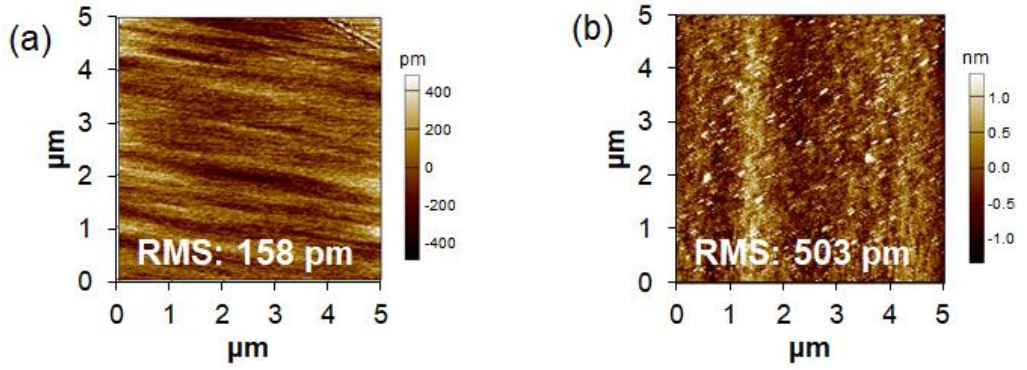


Figure 2.8 Surface morphology of the LED TJ test samples measured by AFM (a) before and (b) after MOCVD 2nd regrowth. The RMS roughness of (a) 158 pm and (b) 503 pm was obtained. (AFM measurement by Charles Forman, UCSB)

noticed only by observing the I-V curve.

During this process, surface morphologies were investigated by atomic force microscopy (AFM) after the first and the second growth as shown in figure. 2.8. As expected, the smooth surface morphology (< 1 nm) was obtained after TJ growth, which is necessary to reduce scattering loss for VCSELs [2].

2.2.2. Doping Concentration

A highly doped layer is commonly used for TJ contacts as well as for metal contacts because it forms an abrupt junction. However, increased doping concentration may increase material absorption. To investigate proper doping concentration, TJ structures were grown with different SiH_4 flow rate, 8 sccm (Si: ~10^{20} cm^{-3}), 6 sccm (Si: ~7.6 x 10^{19} cm^{-3}), and 2 sccm (Si: ~1.9 x 10^{19} cm^{-3}), for n^{++}-GaN layer. After processing, the current density-voltage (J-V) characteristics

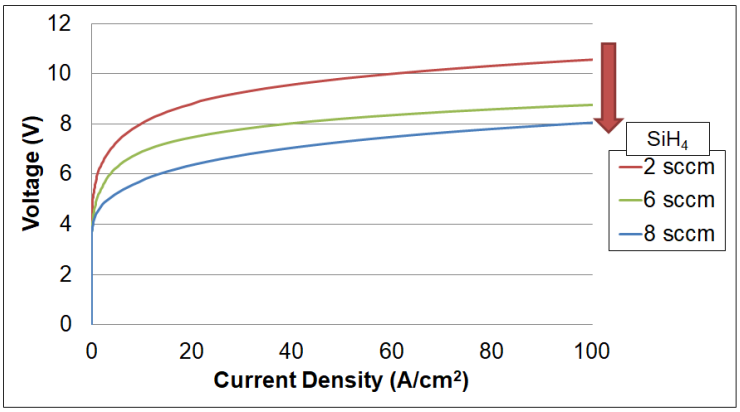


Figure 2.9 J-V characteristics of TJ test samples with n^{++}-GaN layer grown with various SiH_4 flow rates.

in continuous wave (CW) were measured up to a current density of 1 kA/cm^2 as shown in figure 2.9 , which shows improvement of the TJ contacts as increasing the Si doping concentration. 10 sccm of SiH_4 flow rate was also compared with 8 sccm in a different condition; however, it shows similar J-V characteristics. Considering growth variation, 10 sccm of SiH_4 was used for most of my VCSELs

Figure 2.10 also shows the improvement of TJ contacts as increasing Cp_2Mg flow for the p^{++}-GaN layer at the GaN TJ. Based on other experimental data, Mg doping concentration seems to be saturated at around 120 sccm. Unlike Si doping, the result is not obvious because high Mg concentration will increase Mg diffusion into n^{++}-GaN layers which may compensate n-type doping. Furthermore, a higher flow rate of Cp_2Mg than certain point might decrease p-type carrier concentration due to Mg clustering. However, the result does not show degradation with high Mg doping concentration. It may be because

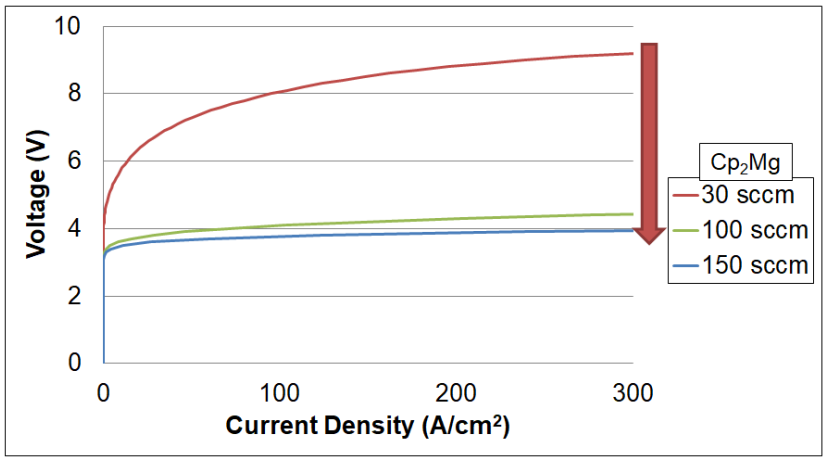


Figure 2.10 J-V characteristics of TJ test samples with p^{++}-GaN layer grown with various Cp_2Mg flow rates.

saturated doping concentration was still not high enough to be degraded or BHF surface treatment reduced those side effects.

2.2.3. BHF Surface Treatment

The role of BHF surface treatment on the p^{++}-GaN surface has been demonstrated in several papers [53], [57]. It is expected that the BHF treatment before n^{++}-GaN regrowth reduces Mg diffusion into the n^{++}-GaN layer, which may compensate for electron carriers. To verify its effect on GaN TJ, samples were grown with and without BHF surface treatments before n^{++}-GaN regrowth. Figure 2.11 shows J-V characteristics of the test samples. The sample regrown after BHF treatment showed a reduction of 0.5 V at 1 kA/cm^2, which supports previously reported results.

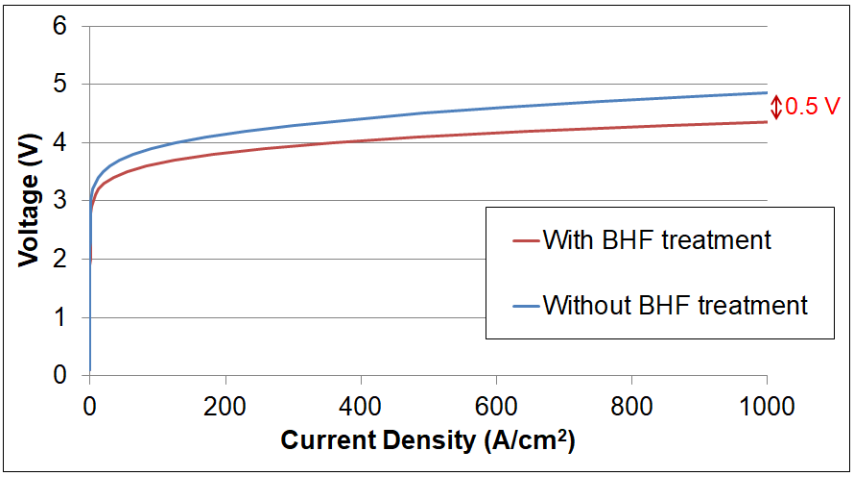


Figure 2.11 J-V characteristics of TJ test samples with (red) and without (blue) BHF surface treatment on p^{++}-GaN surface before regrowth.

2.2.4. In-situ Activation

The in-situ activation step was performed for most of TJ test samples as described in chapter 2.2.1 and figure 2.6 (b). In fact, in-situ activation step would not be needed if its effect is the same as out-situ activation. Activating in a furnace at 600℃ for 15 min could be better because it has been commonly used for a long time. A sample should be taken out of the MOCVD chamber for the BHF surface treatment anyway. Moreover, if p-GaN is deactivated during n-GaN growth, it would not be a matter whether p-GaN is activated out or in the chamber. Nevertheless, confirming the in-situ activation step is still necessary to verify many factors. For example, if a p^{++}/n^{++}-GaN TJ grown in 1-step does not work, it will not be uncertain whether it is because in-situ activation does not effectively activate or the p^{++}-GaN is deactivated after the activation. Moreover, proper in-

situ activation may enable to grow entire TJ structure at once without taking it out of the chamber, which will be desirable to minimize contamination. It was also used for SIMS analysis (chapter 2.2.6).

To verify if the in-situ activation is helping GaN TJ contacts, three samples were grown and measured as shown in figure 2.12. The sample without the activation was grown as the blue curve in figure 2.6 (b). The result showed that in-situ activation reduced ~1.1 V at a current density of 1kA/cm^2. However, the sample grown without the activation would also be partially activated during the temperature ramp up step. Based on the result, extra holding step seems to help to activate the p-GaN, which was not completely deactivated during n^{++}-GaN regrowth. Another sample was also in-situ activated after activating in a furnace as shown in figure 2.12 (green curve). Both samples with (red) and without (green)

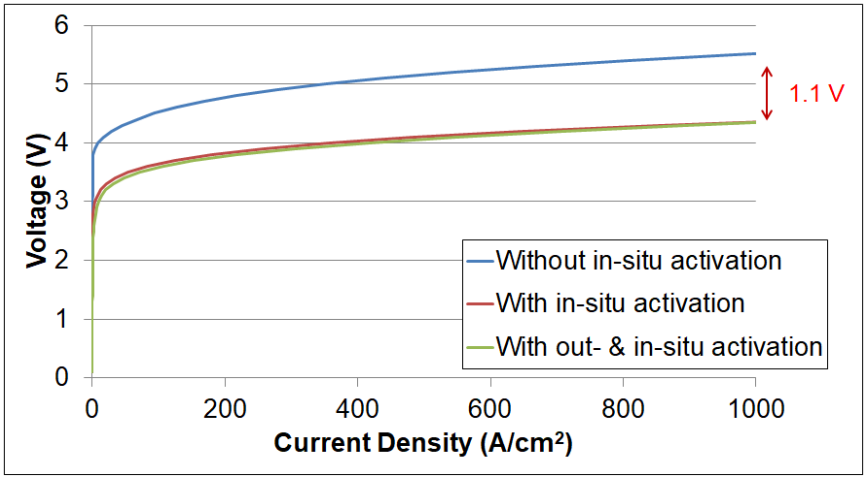


Figure 2.12 J-V characteristics of TJ test samples (red) with and (blue) without in-situ activation step (figure 2.6 b) and (green) with out- and in-situ activation steps. The out-situ activation was performed in a furnace at 600 ℃ for 15 min.

activation in the furnace show almost identical I-V curves. It seems that in-situ activation activates p-GaN similarly as the furnace activation. It was also confirmed that additional in-situ activation after out-situ activation did not degrade TJ contacts.

2.2.5. Comparison of 2-step to 1-step Growth

All previous mentioned TJ test samples were grown in 2-steps, i.e., p^{++}-GaN was exposed in the air before n^{++}-GaN growth. However, growing entire structure at once will be more desirable because the surface of p^{++}-GaN can be contaminated in the air. Unfortunately, experimental result shows much improved TJ contacts in 2-step than 1-step as shown in figure 2.13.

To check if GaN TJ can be grown in 1-step as the 2-step, a sample was grown without taking it out of the chamber after p^{++}-GaN growth. Instead, the chamber was cooled down to 100℃ before in-situ activation and n^{++}-GaN growth. For comparison, 2-step sample was processed like other samples, BHF dipped and in-situ activated. As shown in figure 2.13, the 1-step sample shows a poor J-V characteristic, more than 10 V higher than the 2-step sample at a current density of 1kA/cm^2. It could be a better comparison if BHF surface treatment was not applied to the 2-step sample. However, it is unlikely that BHF surface treatment is the main reason reducing over 10 V as already shown in figure 2.12. The main

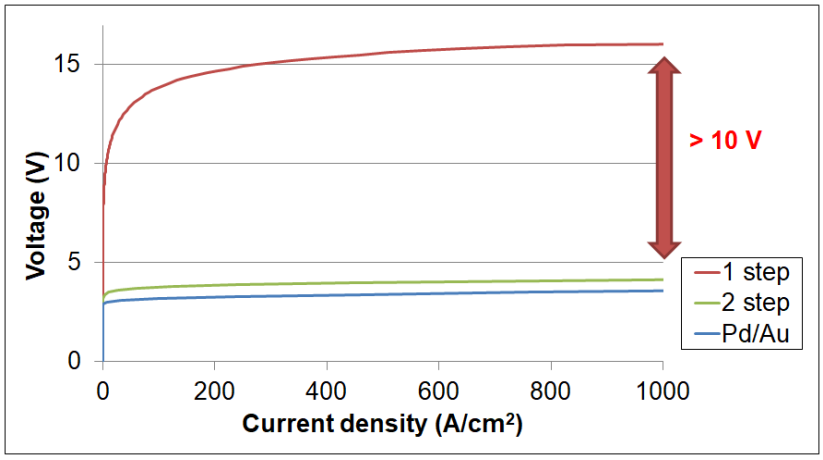


Figure 2.13 J-V characteristics of (blue) a LED test sample with metal contact and TJ test samples grown in (red) 1-step and (green) 2-step with in-situ activation step. BHF surface treatment was processed on the 2-step sample.

reason will be because the sample was taken out of the chamber by exposing it in the air. Further analysis will be discussed in the next chapter.

2.2.6. Analysis

For more analysis, a sample was grown on an m-plane GaN substrate for SIMS as shown in figure 2.14 (a). Each layer except n^{++}-GaN was grown thicker than the test structure (fig. 2.6 a) to see doping concentration clear. In one sample, four types of epitaxial structure were grown; structure A for normally activated p-GaN, B for TJ grown in 2-step, C for TJ grown in 1-step, and D for p-GaN without in-situ activation. n^{++}-GaN was grown right after p^{++}-GaN to prevent activation in structure D. After p^{++}-GaN for structure C, the sample was cooled down to 100 C, ramped up to 750℃, and in-situ activated for 10 min before n^{++}-

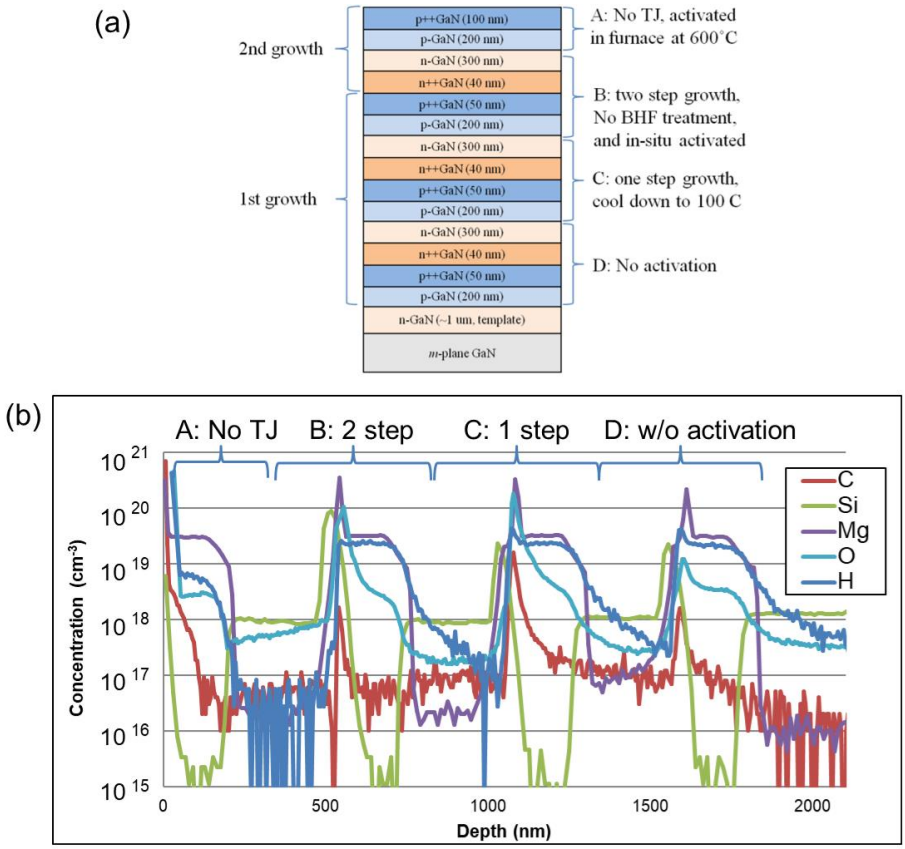


Figure 2.14 (a) An epitaxial structure grown for SIMS measurement and (b) its SIMS data.

GaN growth. The structure B was grown as structure C but taken out from the MOCVD chamber after cooling down. Lastly, the sample was activated in the furnace after structure A growth. Because the main reason for this experiment was to observe hydrogen concentration representing activation efficiency, all structures were grown on one sample to measure hydrogen at once. Hydrogen is the lightest element on the periodic table, which is difficult to be measured due to variations of each SIMS measurement while changing positions and calibrating measurement conditions. Structure A and D were grown as references for

activated and inactivated p-GaN. Structure B and C were grown to find possible elements causing effective GaN TJ contact because taking the sample out from the MOCVD chamber significantly improved the TJ contact (Fig 2.13). BHF surface treatment was not performed for structure B for clear comparison. For example, if structure B were treated in BHF and shows lower magnesium and hydrogen concentrations than structure C, the reason for lower hydrogen concentration will not be clear whether it is because of lower magnesium or efficient activation. The improvement of BHF surface treatment (Fig 2.12) was also minor compared with 2-step growth (Fig 2.13). Concentrations of C, Si, Mg, O, and H in the sample were measured by SIMS as shown in figure 2.14 (b).

At first, the hydrogen concentration is analyzed. P-GaN in structure A had much lower H concentration than in structure D, which represents the effect of normal activation. However, p^{++}-GaN layer in structure A was too close to the surface and too thin to be clearly measured. Surprisingly, H in p-GaN layer in both structure B and C show similar concentration as in D (not activated), which implies that in-situ activation was not effectively performed or p-GaN was fully deactivated during n^{++}-GaN regrowth. Either case against forming effective TJ contact. However, H in the p^{++}-GaN layer of structure B shows lower concentration than of structure C and D, which may represent partial activation as shown in figure 2.15 (a). It might be just due to deeper magnesium tails cooperated with hydrogen in n^{++}-GaN grown right after p^{++}-GaN. However, if that

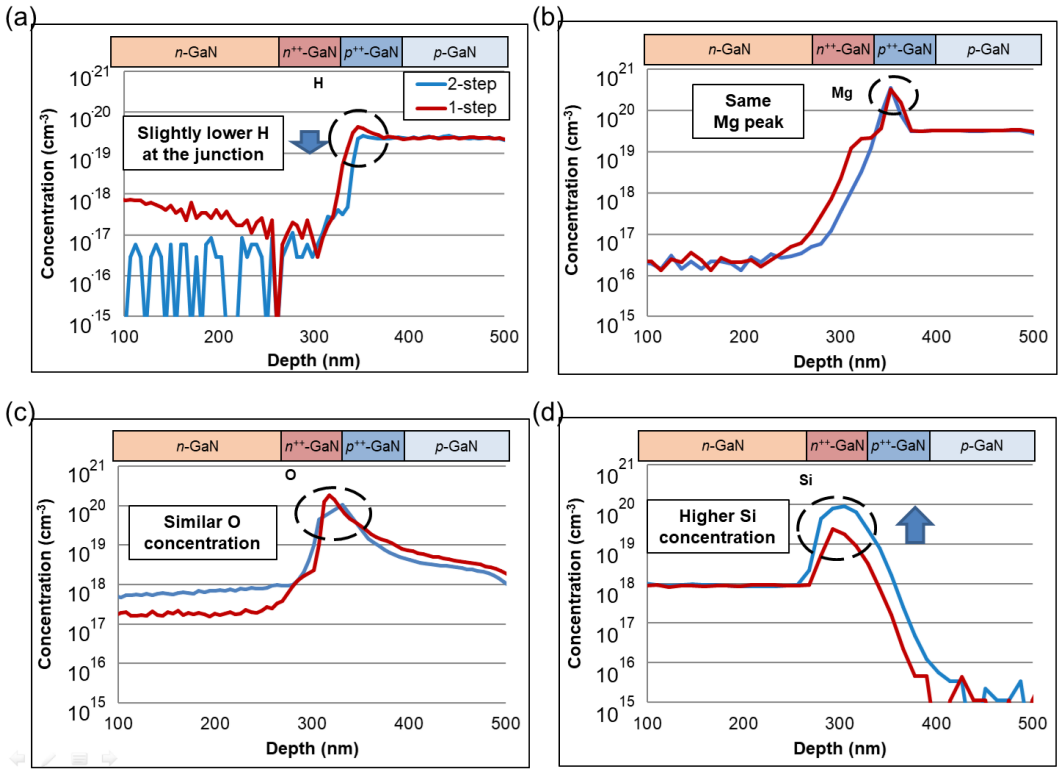


Figure 2.18 Overlaps of SIMS data between structure B and C for (a) hydrogen, (b) magnesium, (c) oxygen, and (d) silicon concentrations.

is the case, structure C should show lower hydrogen then structure D. If p^{++}-GaN of structure B is actually more activated, it is still not clear if it is because p^{++}-GaN was close to the surface or it had higher Mg doping concentration than p-GaN. The same test with thicker P^{++}-GaN layer will clear out these hypotheses and also provide hydrogen concentration when it is fully activated in structure A. However, it is still unclear why 2-step growth had lower hydrogen concentration.

Mg concentration of p-GaN layer was found to be ~$3x10^{19}$ cm^{-3} for all layers. However, resolution of SIMS measurement was not fine enough to extract

actual number in the p^{++}-GaN layer, which may explain the lower Mg peak in structure D. Mg diffusion into n^{++}-GaN layer was the most significant in the n^{++}-GaN layer grown right after the p^{++}-GaN (D), the next significant grown after nitrogen flows for more than 30 min (C), and the least significant grown after taking the sample out. The Mg diffusion seems significantly depends on Mg present in the MOCVD chamber during the n^{++}-GaN growth. Because diffused Mg may compensate Si doping in the n^{++}-GaN layer, the result of the Mg concentration in structure B also agrees with better TJ contacts using the 2-step growth.

The Si concentration of the n^{++}-GaN layer was significantly high in structure B than in structure C and D. It might be because silica from the air was accumulated on the surface when the p^{++}-GaN of structure B was exposed in air. Though Si concentration peak shows below $1x10^{20}$ cm^{-3} in SIMS data, actual Si concentration at the very junction will be much higher if the accumulated silica affected more from the junction.

As expected, the oxygen concentration was lowest when the next structure was continuously grown (D) which reduced time to cooperate with oxygen came from sapphire corral used to hold the sample during MOCVD growth. However, structure B, which was exposed in oxygen (air) before regrowth, shows similar oxygen concentration as structure C. It means that the main source for high oxygen concentration was the sapphire corral rather than the oxygen presented on

the surface. Base on this data, oxygen seems not the main reason improving TJ contact which partially disagrees with the previously reported result [46].

In conclusion, 2-step growth may partially activate p^{++}-GaN (or less deactivation) and also cause high electron carrier concentration for n^{++}-GaN due to more Si from the air and less Mg diffusion. However, simulation result with possible carrier concentrations does not predict to have efficient TJ contact, which implies that it is trap-assisted tunneling. It means that other elements from the air also accumulated on p^{++}-GaN and increased number of impurities, traps. More analysis is necessary to clear out other possibilities.

2.3. p/n-GaN Junction for Buried Tunnel Junction Contact

Two things should be confirmed to form the BTJ contacts; if the TJ contact is effective enough to be used and if the other junction is blocking current (if the p/n-GaN junction has high breakdown voltage). Because the effective TJ contact is investigated in chapter 2.2, p/n-GaN junction contact will be mainly studied.

To investigate the breakdown voltage of the p/n-GaN junction contact for the BTJ VCSEL design, test samples were prepared as illustrated in figure 2.19. To form BTJ contacts, the p^{++}-GaN and part of the p-GaN layers will be etched

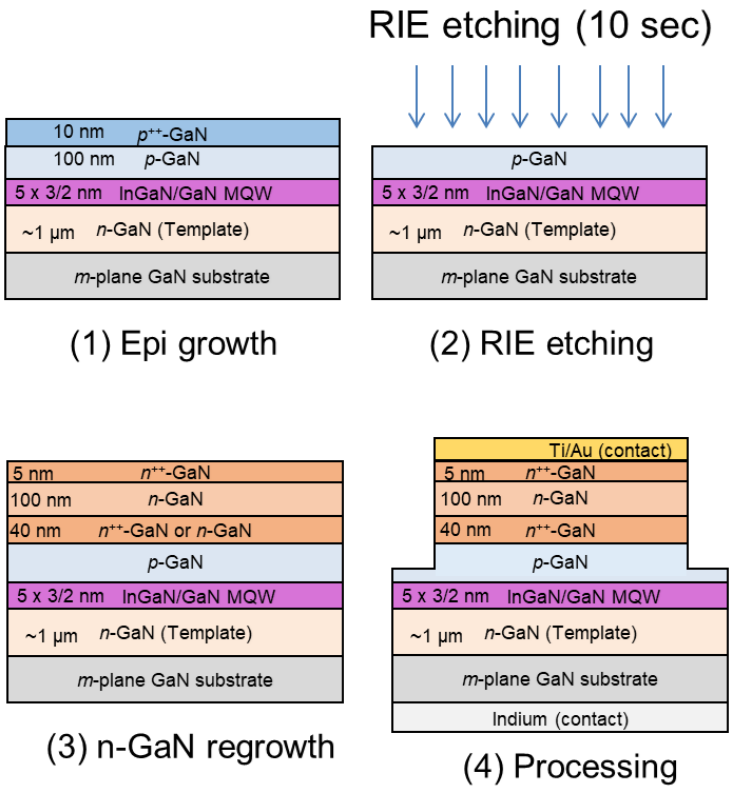


Figure 2.19 processing steps for p/n-GaN junction contact.

before n-GaN regrowth as described in processing step 2 (chapter 3). Thus, the samples were etched passing through the p^{++}-GaN layer after the first growth (2nd step in fig 2.19). For comparison, three different types of junctions were processed, A for effective TJ, B for etched p-GaN with the n^{++}-GaN junction, and C for etched p-GaN with the n-GaN junction as shown in figure 2.20. Sample B was processed for possible use to simplify the BTJ VCSEL processing steps.

After processing, electrical characteristics were measured under CW operation as shown in figure 2.20. Sample A turned on at ~3.5 V as expected,

while sample C did not break down up to 21 V. Based on this experimental result, it was very promising to have good current confinement up to a high voltage. Sample B broke down at ~10 V which is still much higher than TJ contact. Because sample C shows a better result than sample B as a current blocking layer, lightly doped p-/n-GaN junction was used for future BTJ VCESLs. Unfortunately, this test condition was not exactly the same as the BTJ VCSELs. In the BTJ processing steps, the etching was carried out after the n^{++}-GaN regrowth which requires deeper etching which can cause possible over etching and extra damage in the p-GaN layer. The p-GaN thickness of VCSEL epitaxial structures was also thinner than 100 nm. Moreover, current blocking may be degraded by heating near current aperture when VCSELs are operating at high current density.

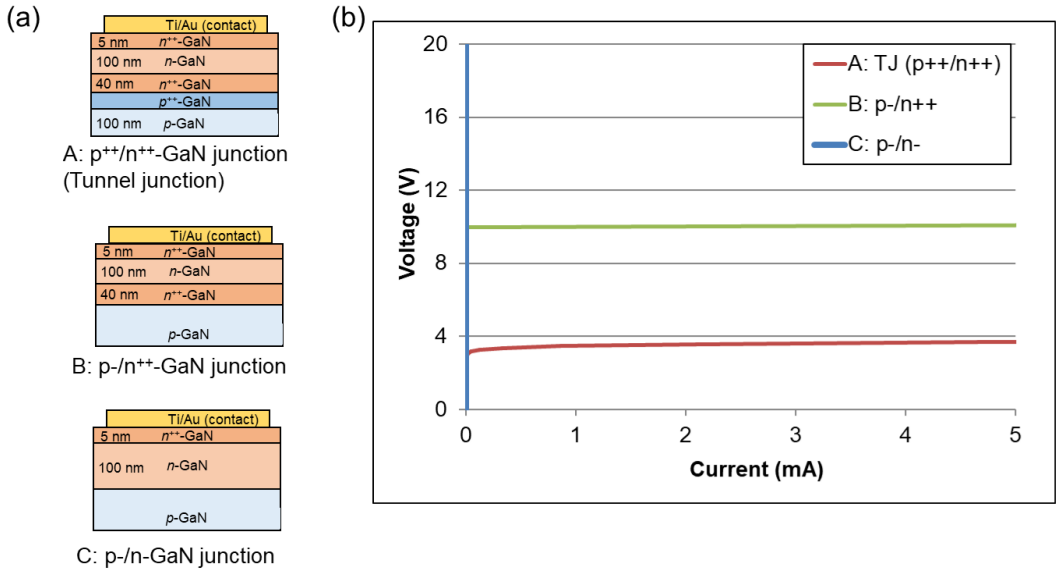


Figure 2.20 (a) Top structures above active layer for p/n-GaN junction test and (b) their I-V characteristics.

Unfortunately, Joonho remeasured the sample C and got similar result as the sample B. I might measure it when the sample was not properly contacted or there might be variations device to device.

3. Fabrication of III-N Flip-chip VCSEL

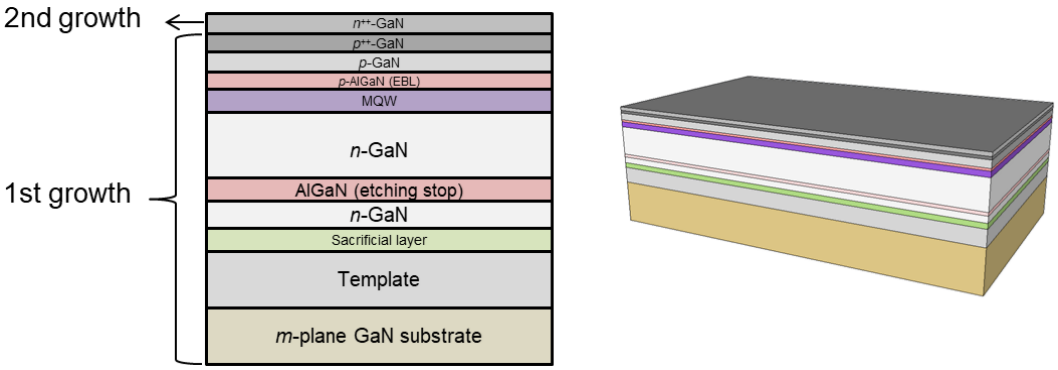
VCSEL processing requires one of the most complicated processing steps in our group, which takes at least one month only for fabrication. All processing steps including mask design, epitaxial calibration, and device characterizations, usually take more than 3 months to see the first device. Thus, I usually processed various epitaxial structures at the same time to have a higher chance to make lasing VCSELs as well as to find some tendencies. It will be frustrating to have no lasing VCSELs after 3 months of work, so it is very important to know each step right and to handle each sample carefully until the end of a process. In this chapter, general processing steps for flip-chip nonpolar III-N VCSELs with dual dielectric DBR, MOCVD-grown TJ contacts, BTJ apertures will be described. Then, VCSELs with IIAs will be briefly explained.

3.1. Buried Tunnel Junction VCSEL

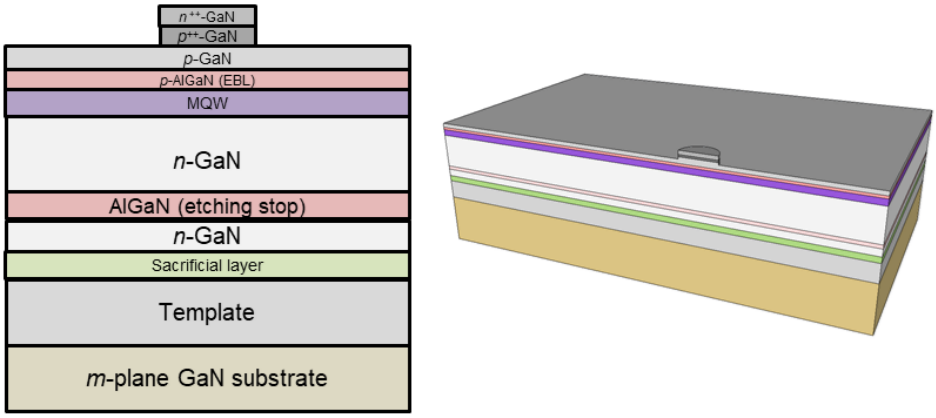
VCSEL structure and processing steps are similar to described in John T. Leonard's thesis. Few steps have been changed after confirming that Al ion implantation protects MQW from PEC etching [60]. Followings are just representative processing steps, so some factors can be changed such as the number of DBR periods, the flip-chip submount material, the thickness of metals, and so on. In this process, ion implantation outside an aperture is still used to

prevent lateral etching of the MQW from PEC etching during the flip-chip process in a later step, and also to prevent possible other leakages passing through sidewalls and etched p-GaN layers. Figure 3.1 illustrates processing steps for a BTJ VCSEL. Details of processing steps will be explained as follows.

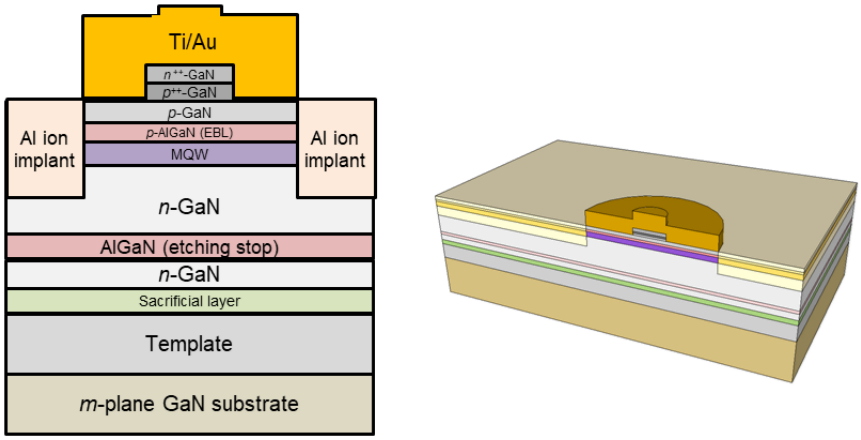
Step 1: Epitaxial growth and TJ regrowth



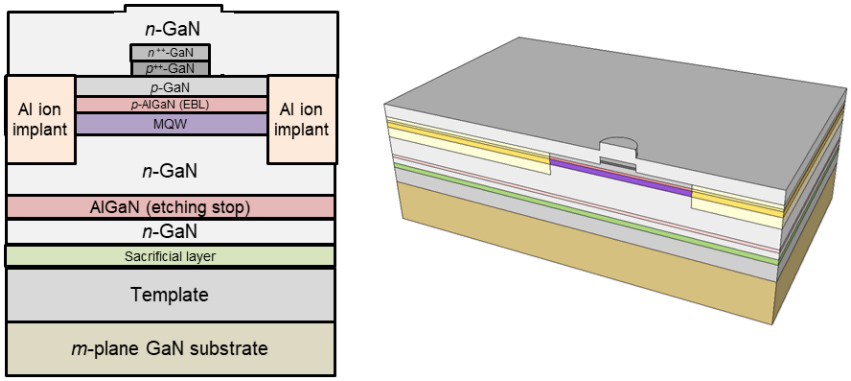
Step 2: Aperture etching



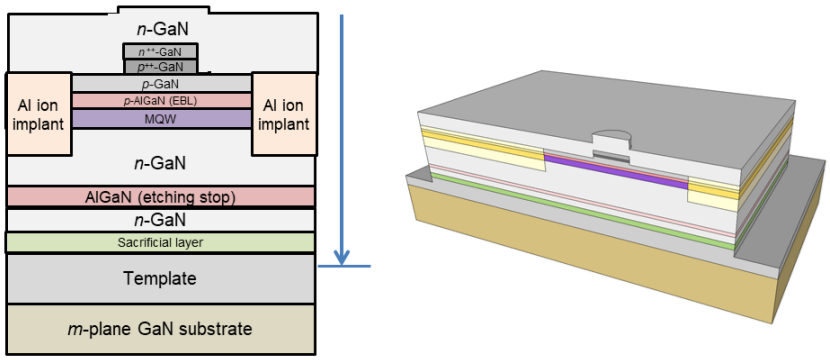
Step 3: Al Ion Implantation



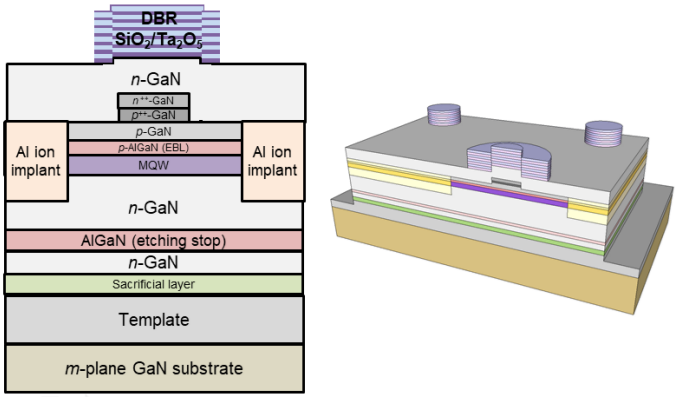
Step 4: Current Spreading Layer Regrowth



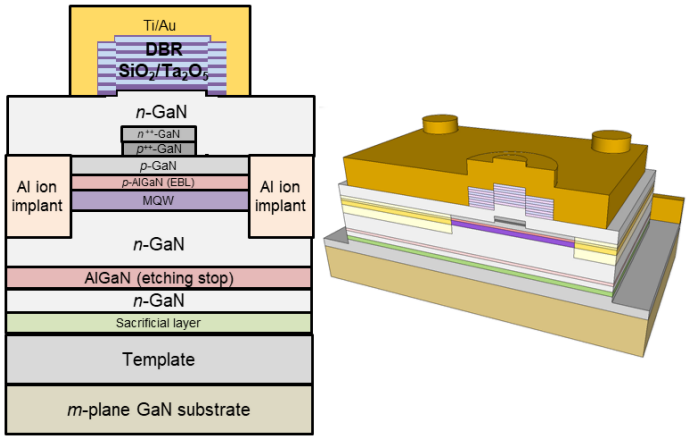
Step 5: Mesa Etching



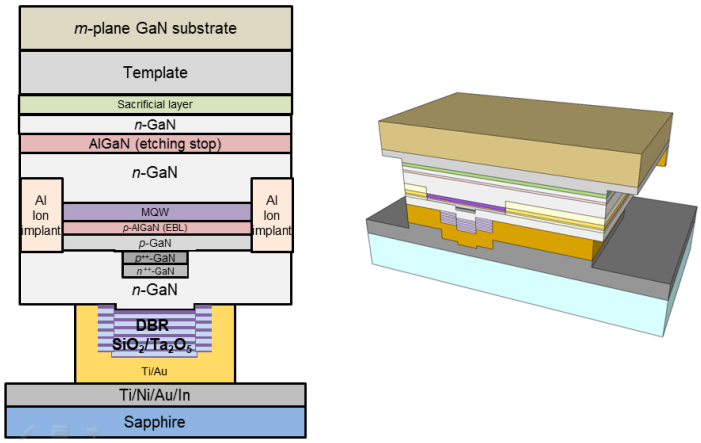
Step 6: p-DBR Deposition



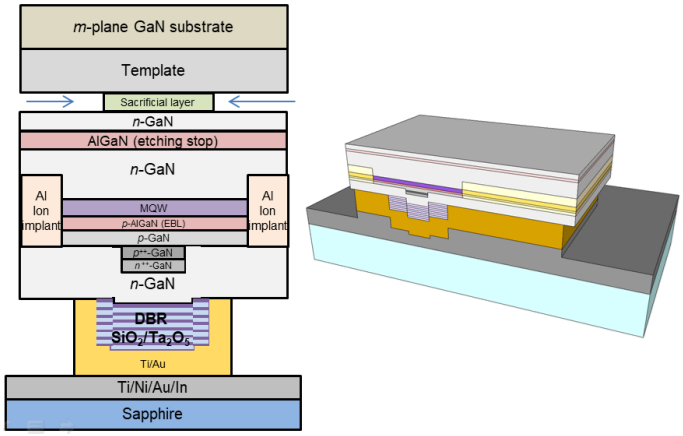
Step 7: Metal Deposition



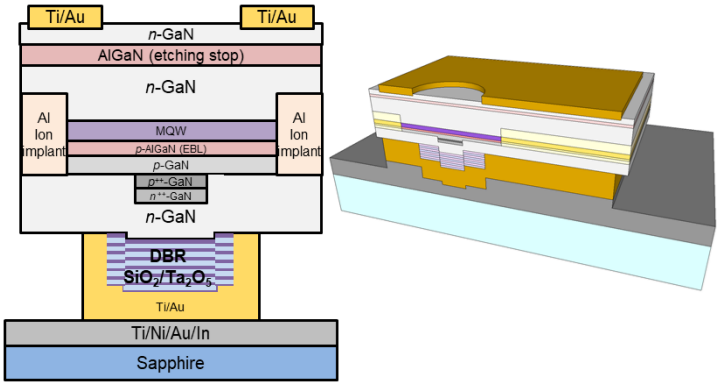
Step 8: Flip-chip Bonding



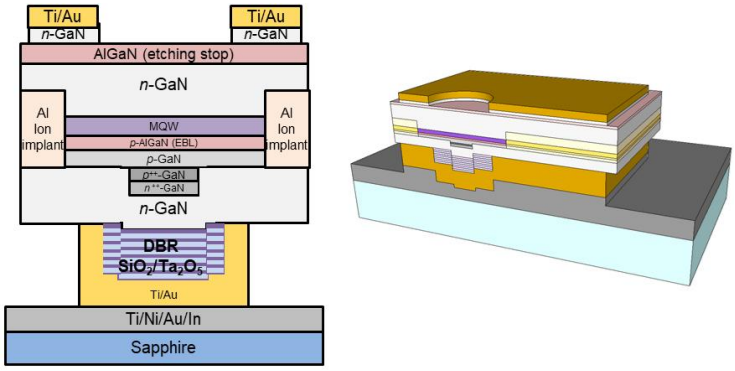
Step 9: PEC Undercut Etching and Substrate Remover.



Step 10: n-contact metal deposition.



Step 11: PEC top-down etching



Step 12: n-DBR deposition

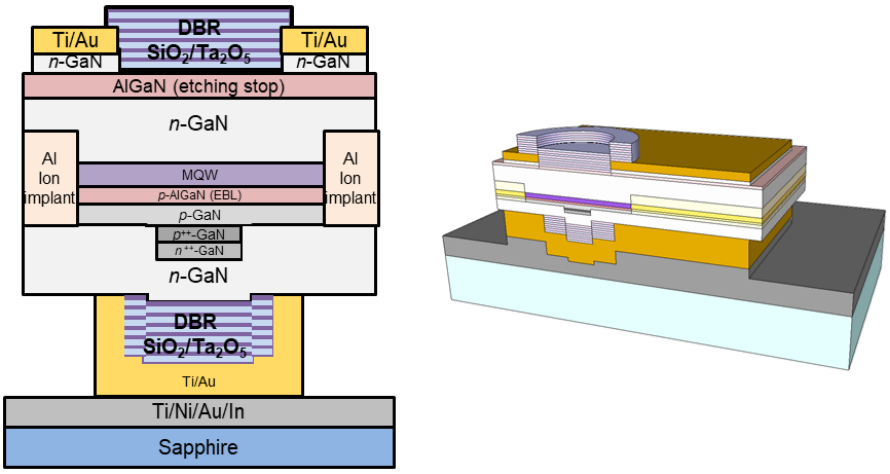


Figure 3.1 Illustration of the processing steps in 2D (left) and 3D (right) of a BTJ VCSEL.

Step 1 illustrates the main epitaxial structure grown on an m-plane GaN substrate followed by ~10 nm n^{++}-GaN regrowth for TJ contacts. Details of epitaxial structures are listed in table 4.2 (chapter 4.2). As the sacrificial layer, three QWs with 7/5 nm of InGaN/GaN layers have been used for most of my devices. Higher indium composition and number of QWs may increase etching rate during PEC undercut etching, but it may affect epitaxial structure grown above it when total InGaN layers are thicker than the critical thickness. Right above the sacrificial layer, lightly doped n-GaN is grown to be etched by PEC top-down etching. After the main epitaxial growth ending with p^{++}-GaN, activation is conducted at 600℃ for 15 min in a furnace. Then, the sample is dipped in BHF for 5 min and rinsed in DI water to remove Mg-rich film. Next, n^{++}-GaN is regrown on p^{++}-GaN by MOCVD for TJ contact. Details of TJ growth

condition is mentioned in chapter 2.2. After the n^{++}-GaN growth, alignment marks are etched ~600 nm. It is because the aperture etching depth is only few tens of nanometers, which is difficult to be seen with PR on top.

Step 2 is current aperture etching by RIE with Cl_2 gas. The etching depth should be deep enough to pass p^{++}-GaN, but the etching damage should not reach to the active layer. The damage might generate a leakage path passing through the etched p-GaN layer. An SEM image in figure 3.2 (a) shows aperture shape, n^{++}-GaN (dark) surrounded by p-GaN (bright), after the RIE etching. The clear contrast of brightness must be due to different conductivities between n^{++}-GaN (high) and p-GaN (low).

Step 3 is Al ion implantation. Firstly, Ti/Au (20/300 nm) hard mask is deposited using E-beam evaporation. Next, the sample is shipped to Leonard Kroko, Inc to perform Al ion implantation in a dose of 10^{15} ions/cm^2 at 20 KeV in normal incident followed by metal remover in heated aqua regia. As mentioned earlier, this ion implantation is still used to protect the active layer from PEC

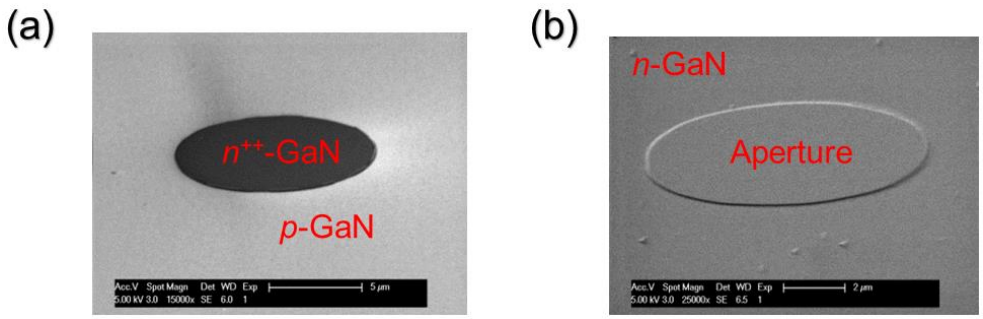


Figure 3.2 SEM images of current apertures taken after (a) aperture etching and n-GaN regrowth.

undercut etching as well as to prevent other possible leakages. But it is unlikely that the implantation affects lateral current spreading because the diameter of the circular pattern is ~4 μm wider than p-DBR. This ion implantation step can be replaced by well-developed processing techniques. For example, dielectric material like SiO_2 or Si_3N_4 can be used to protect active layer from PEC etching and one more extra etching after n-GaN regrowth might help to prevent sidewall leakage. However, only small cracks in the dielectric film can cause active layer etching and it complicates processing steps requiring 1 or 2 more lithographies.

Step 4 is n-GaN current spreading layer regrowth. The n-GaN current spreading layer is regrown by MOCVD after 20 min UV-ozone surface treatment followed by 5 min BHF surface treatment. The purpose of the surface treatments is to oxide Si accumulated on the surface and to etch it. The SEM image after 125.5 nm n-GaN regrowth in figure 3.2 shows that etched step still presents after regrowth which can cause lateral optical confinement.

Step 5 is mesa etching also carried out by RIE with Bl_3/Cl_2. The etching depth is more than 500 nm deeper than the total thickness from the sacrificial layer to the n-GaN current spreading layer. This etching step is to expose the sacrificial layer for PEC undercut etching, as well as to divide etch device.

Step 6 is p-DBR deposition composed of 17 periods of Ta_2O_5/SiO_2 layers using ion beam deposition (IBD). The thickness of each layer is calibrated to have a quarter wavelength ($\lambda/4n$). Because band gap of semiconductor materials tends

to decrease at a hot temperature, I usually target 5 ~ 10 nm longer wavelength then spontaneous emission (see chapter 4.3). As shown in figure 3.3 (a), column-like DBRs are also deposited at each corner to support the mesa during flip-chip bonding. The columns are placed away from the aperture because cracking, which can be caused by physical pressure and thermal expansion, may propagate to the aperture. The void area without DBRs is to be filled by indium during flip-chip bonding for better heat transfer. Another thing found is that outside the DBR is tapered ~1 µm as shown in the SEM image (fig 2.3 b). It must be due to undercut etching of negative photoresist (PR) and unintentionally angled deposition. It does not cause a significant issue in the current structure because of forgiving mask design with 4 µm tolerance between ends of p-DBR and aperture. However, processing steps should be optimized to reduce the tolerance for a better heatsink and lateral current spreading.

Step 7 is metal deposition for a contact on the mesa and PEC cathode on the etched n-GaN template. E-beam evaporation is used to deposit 20/1000 nm of

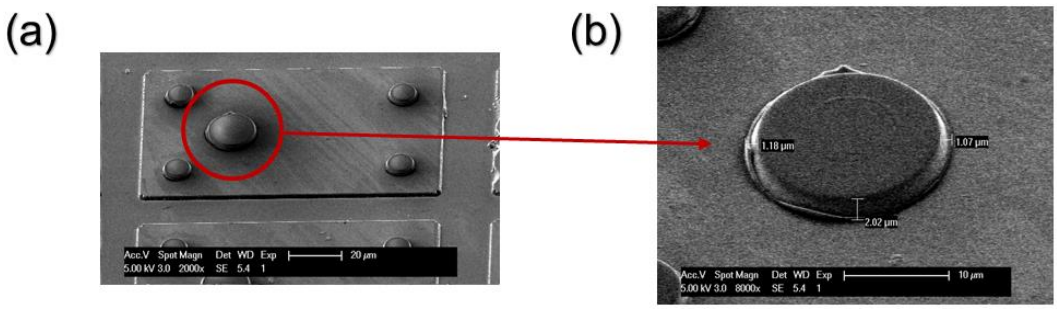


Figure 3.3 SEM images of (a) a device and (b) a DBR after p-DBR deposition.

Ti/Au. In figure 3.4 (a), narrow strip lines are for PEC cathode and yellow metals on each device are for the contact. These contacts are also used for InAu bonding.

Step 8 is flip-chip bonding. The sample was placed upside down on a piece of a sapphire substrate coated with approximately 20/100/1000/2000 nm Ti/Ni/Au/In inside a graphite fixture as shown in a picture (fig 3.4 b). Then, the sample in the fixture is softly pushed by a graphite cubic followed by heating in an oven at 200 C for 2 hours. Because aluminum is malleable material, part of the void area especially around DBRs will be filled with indium. Then, indium and gold will become indium-gold alloy. The indium-gold flip-chip bonding was optimized by Charles Forman.

Step 9 is substrate removal using the PEC undercut etching. The flip-chip bonded sample is socked in 1M KOH solution and illuminated by 405 nm LEDs. It takes from few hours to several days depending on etching condition, such as

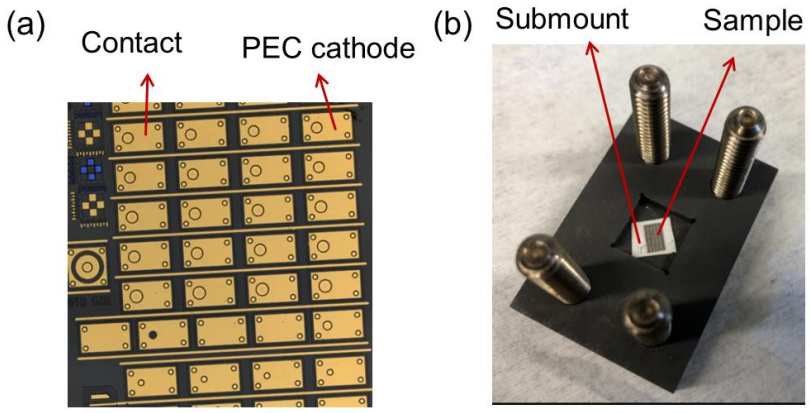


Figure 3.4 (a) A microscope image taken after metal contact and PEC cathode deposition and (b) a picture taken before flip-chip bonding inside a graphite fixture. (b) The sample is facing down to contact with a submount coated with indium.

carrier lifetime, light absorption rate, and KOH morality. GaO and InO may remain on the surface after finishing PEC etching. To remove these oxides, the sample is gently swabbed by a cotton tip in diluted tergitol surfactant. Figure 3.5 shows devices after the substrate removal. Due to the transparency of GaN, some structures under cavities were observed like DBRs (blue circles). I suspect that the gray patterns are because indium filling the void area contacted with gold and became InAu.

Step 10 is n-contact metal deposition. The doping concentration of n-GaN layer grown right after the sacrificial layer is designed to be low (Si: < 5 X 10^{18} cm^{-3}) for PEC top-down etching [39]. However, metal contact deposited on a lightly doped n-GaN layer is unlikely to form an ohmic contact. Thus, RIE etching with $SiCl_4$ gas and 270W of input power is performed on the n-GaN surface to increase n-type carrier concentrations and to remove any left oxides [61]. Then, 40/300 nm Ti/Au metal deposition is carried out using e-beam.

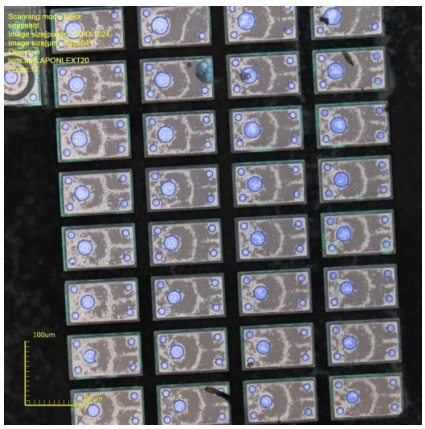


Figure 3.5 An image taken by a confocal microscope after substrate removal.

Step 11 is PEC top-down etching. The sample is soaked in 1M KOH while illuminated by 365 nm LED arrays with 345 nm filter for 5 min to etch down to AlGaN etching-stop layer. Because surface morphology smoothness is uncertain after PEC undercut etching due to long etching time and variation of etching condition, top-down etching might eliminate this uncertainty by etching only few tens of nanometers. However, it was difficult to measure ~80 nm top-down etching surrounded by metal on the etched n-GaN layer. As shown in figure 3.6, a small gap (blue circle) between metal and n-GaN was observed after PEC top-down etching, which might mean top-down and undercut etching. However, I could not see a clear difference using AFM measurement. Moreover, obvious improvement in surface morphology was also not observed. This process should be optimized and confirmed in the future.

Lastly, step 12 is n-DBR with a Ta_2O_5 spacer deposition. Before the DBR deposition, resonance wavelength is measured at low input current (< 100 μA) to estimate cavity thickness. The thickness of the spacer is decided based on the

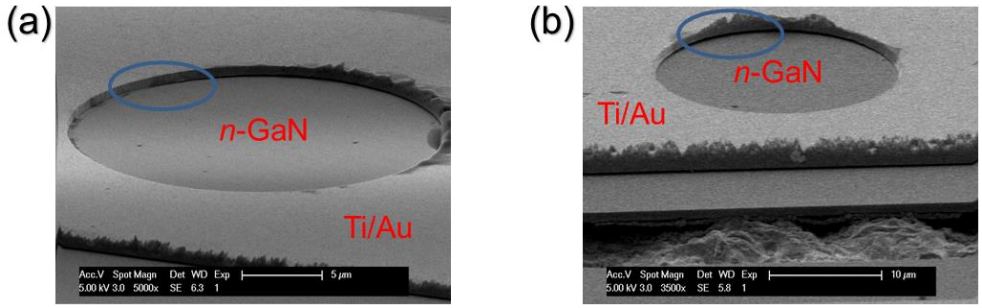


Figure 3.6 SEM images taken (a) before and (b) after PEC top-down etching.

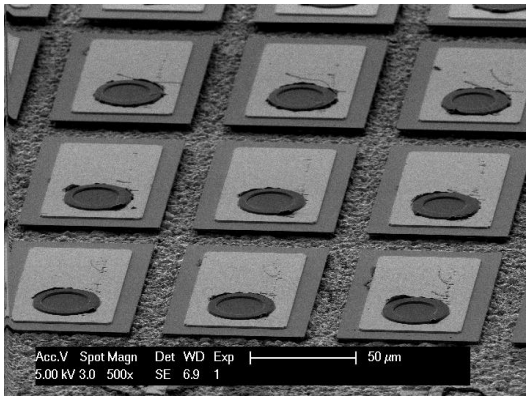


Figure 3.7 An SEM image of finished BTJ VCSELs

cavity resonance, target wavelength, and spontaneous emission. Finally, figure 3.7 shows processed BTJ VCSELs. Characteristics of VCSELs will be discussed in chapter 4.2.

3.2. Ion Implanted Aperture VCSEL

IIA VCSEL structure is similar to BTJ VCSEL structure, so does processing step. Different processing steps are for aperture structure from step 1 to step 4 in figure 3.1. Firstly, the main epitaxial structure is grown until a p^{++}-GaN layer followed by an alignment mark etch. Next, ion implantation is carried out after Ti/Au metal hard mask is deposited on apertures. Then, the metal mask is removed in aqua regia. Next, $n^{++}$and n-GaN layers are regrown at once after BHF surface treatment. The last of processing steps are the same as the BTJ VCSEL in chapter 3.1 from step 5.

However, the processing steps used for IIA VCSELs described in chapter 4.1 are slightly different. Implantation energy was 10 KeV instead of 20 KeV to reduce optical absorption in the implanted area. Mesas were etched in two steps because it was uncertain if the Al ion implantation can prevent sidewall leakage. Next, SiC substrate was used as a flip-chip submount for better heat transfer. Lastly, 13 periods of n-DBR was used to have low threshold current density, high possibility to get lasing VCSELs. There were also minor differences which would not affect the device performance. The detailed thicknesses and doping concentrations of the full epitaxial structure are shown in chapter 4.1.1.

4. Characteristics of III-N VCSELs

4.1. IIA VCSEL with MOCVD-grown TJ contact

The ion implantation aperture (IIA) is one of the typical current aperture designs for VCSELs, which has been demonstrated in many research groups including UCSB [28], [59]. When I took over this project, the recent results were IIA VCSELs with TJ contacts using the hybrid MOCVD/MBE growth technique. Thus, my next step was growing the entire epitaxial structure using only MOCVD instead of the hybrid growth, which will be necessary for mass production. One disadvantage of the hybrid growth is that the optimal miscut of MBE growth (+1° to c-direction) is different with MOCVD growth (-1° to c-direction) on the m-plane GaN. So, the MBE regrowth on a sample grown by MOCVD can roughen the surface morphology, which can be solved by the MOCVD-grown TJ. However, the MOCVD-grown TJ still suffers from the p-GaN activation issue. Due to a lack of direct comparison between the MOCVD TJ and the hybrid TJ, nothing can be concluded. However, it is unlikely that an optimized MOCVD TJ contact has lower contact resistance than an optimized hybrid TJ contact until the activation problem presents. Nevertheless, I think that the development of MOCVD TJ growth should be pursed due to chief advantages for

commercialization, and further development of MOCVD TJ growth will bring it close to hybrid TJ contact.

In this chapter, designs, characteristics, and analysis of AII VCSELs with MOCVD-grown TJ contacts will be discussed. Then, the result will be analyzed to estimate the effect of optical loss from Al ion implantation which motivates the next design, the BJT VCSEL.

4.1.1. Design

IIA VCSELs were processed starting from the main epitaxial structure grown by Charles Forman. The VCSELs were processed as described in chapter 3.2, and the GaN TJ contacts were grown as described in chapter 2.2. Information of each epitaxial layer is listed in table 4.1, and optical profile was simulated as

Table 4.1. VCSEL epitaxial layer structure grown on an m-plane GaN substrate [28].

	Epitaxial Layer	Thickness (nm)	Doping concentration (cm^{-3})	Contribution to internal loss (%)
2nd growth	n^{+}-GaN	10	10^{19}	1.8
	n-GaN	94	1.3×10^{18}	6.0
	n^{++}-GaN	40	10^{20}	9.4
1st growth	p^{++}-GaN	14	2.2×10^{20}	21.7
	p-GaN	61.2	10^{19}	12.8
	p-AlGaN	5	2.2×10^{19}	1.3
	2 × InGaN/GaN MQW	14/1	UID	
	n-GaN	759.4	2.3×10^{18}	45.7
	n^{+}-GaN	15	1.7×10^{19}	1.3
	InGaN (Sacrificial QW)	7	UID	
	n-GaN (Template)	~ 1300	1.3×10^{18}	

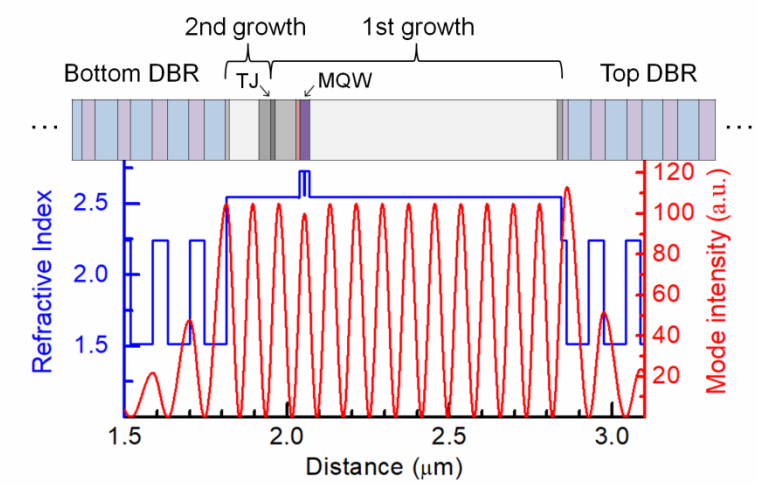


Figure 4.1 Optical mode profile overlaid with refractive index of a VCSEL cavity structure [28].

shown in figure 4.1. It was designed to have a lasing wavelength of 410 nm with a cavity thickness of ~6.5-λ. To reduce optical loss, the null of the optical mode was placed in the n^{++}-GaN layer which was grown for TJ contact. However, it is still uncertain whether optical loss of the p^{++}-GaN is higher or lower than the n^{++}-GaN layer containing Mg diffused from the p^{++}-GaN layer. Further study will be needed to accurately simulate it. SEM images of a final IIA VCSEL and before flip-chip bonding were taken as in figure 4.2.

Based on the simulation result, an internal loss (α_i), a mirror loss (α_m), and a threshold material gain (g_{th}) were calculated as ~12.61 cm^{-1}, ~0.63 cm^{-1}, ~335 cm^{-1} respectively [28]. Table 4.1 include the estimated internal loss in each layer taking into account the optical absorption, thickness, and mode intensity. It was found that about a half of the total internal loss comes from the thick n-GaN layer

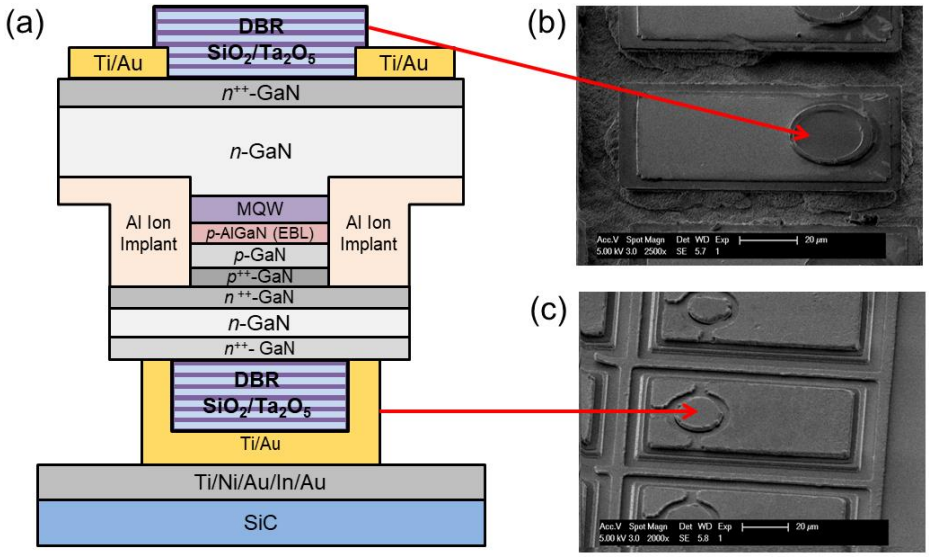


Figure 4.2 (a) Schematic of IIA VCSEL and SEM images (b) after top DBR deposition and (c) before flip-chip bonding [28].

. Total internal loss will be decreased by reducing doping concentration and thickness, although thermal impedance and conductivity may increase.

4.1.2. Pulsed Operation

Optical and electrical characteristics of the IIA VCSELs were measured after fabrication. Figure 4.3 shows the light-current-voltage (L-I-V) characteristics of two VCSELs lasing at different wavelengths under pulsed operation at room temperature. The epitaxial structure of the sample lasing at 408 nm (a) was the same as represented in table 4.1, and another sample lasing at 420 nm (b) had 15 nm AlGaN etching stop layer right above the n^{+}-GaN layer and the sacrificial

layer. The peak wavelength of spontaneous emission from the active layer was ~403 nm and ~406 nm for the 408 nm and 420 nm VCSELs, respectively.

The VCSEL lasing at 408 nm showed the threshold voltage (V_{th}) of 7.8 V at the current density (J_{th}) of 10 kA/cm^2. The voltage was applied up to 12 V which brought the maximum output power of 319 μW. Appling higher voltage could bring higher output power, though it was risky to burn the sample. A kink in the L-I curve at ~40 mA and ~70 mA was observed probably due to the appearance of higher order lasing modes. The differential efficiency (η_d) at ~50 kA/cm^2 was found to be 0.28%. The differential resistivity was 10^{-4} Ω-cm^2 at ~20 kA/cm^2, which is higher than ~5 × 10^{-5} Ω-cm^2 from the hybrid TJ contact [5]. This calculation will be more proper for the same size devices. Based on the doping concentrations and mobilities, the sheet resistances of the top layer (p-side) was 165.7 Ω/sq and the bottom (n-side) layer was 116.5 Ω/sq [47]. I believe that the low doping concentrations in n-GaN layers on the p-side caused the high

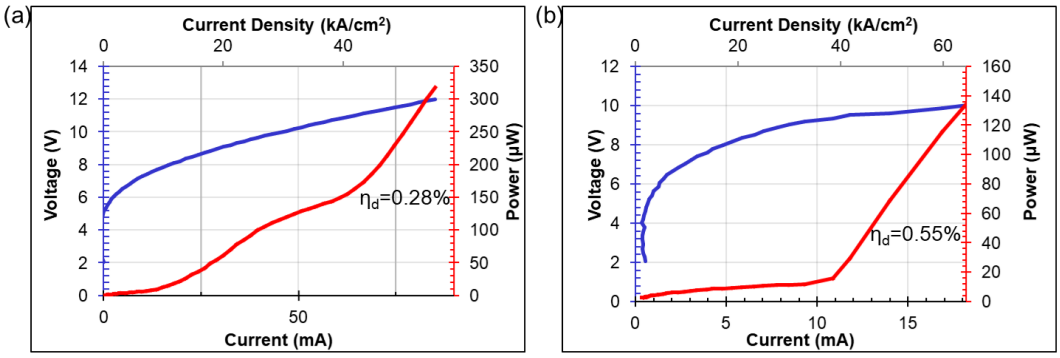


Figure 4.3 L-I-V characteristics of IIA VCSELs lasing at (a) 408 nm and (b) 420 nm under pulsed operation. The aperture diameters are (a) 14 μm and (b) 6 μm. 403 nm and 408 nm

differential resistivity which limited device performance.

The 420 nm VCSEL showed higher J_{th} (38 kA/cm^2) and V_{th} of 9.4 V probably due to the misalignment between the spontaneous emission (406 nm) and the lasing wavelength (420 nm). The input voltage was applied up to 10 V, which gave the peak output power of ~130 μW at J_{th} of 64 kA/cm^2. However it shows higher η_d (0.55 %). I suspect that it is due to advantages of longer wavelength, such as lower material absorption and scattering loss. The main advantage was the wavelength shift under CW operation which will be discussed in chapter 4.3.

4.1.3. Optical Loss of Al Ion Implantation

From differential efficiencies measured as shown in figure 4.3, the internal loss can be roughly estimated based on equation (4.1) after assuming several factors.

$$\eta_d = \frac{\eta_i \alpha_m}{\alpha_i + \alpha_m} \tag{4.1}$$

For the analysis, internal efficiency (η_i) was taken from a GaN-based edge-emitting laser paper and mirror loss was simulated based on the VCSEL structure [62]. Thus, this method includes many errors. For example, internal efficiency (66%) will be different depends on an active layer design, and mirror loss simulation does not count thickness errors and optical loss of DBRs [62].

Moreover, there will be other sources of losses from current spreading and optical scattering. Nevertheless, this analysis will offer a rough idea about our current VCSEL designs. From the 408 nm and 420 nm VCSELs, internal loss of 122 cm^{-1} and 68 cm^{-1} were estimated based on the η_d of 0.28% and 0.55%, respectively. These internal losses are much higher than simulated internal losses, 12.61 cm^{-1} for the 408 nm laser and 15.02 cm^{-1} for the 420 nm laser, which implies that critical sources of losses were not counted.

As one source of the losses, the optical loss of Al ion implantation was studied. As illustrated in figure 4.4, Al ion implantation was performed on a double side polished (DSP) m-plane GaN substrate. After the implantation, the sample was annealed in rapid thermal annealing (RTA) to mimic the annealing during the TJ regrowth. In truth, this experiment had been done before the VCSELs with MOCVD-grown TJ contacts were processed. Thus, the annealing temperature was chosen considering MBE regrowth condition. Higher temperature annealing may reduce optical loss bit more. After the annealing, transmittance and reflectance were measured by carry 500 as shown in figure 4.5. If the material is lossless, the sum of reflectance and transmittance should be 100%. The sum for the GaN substrate showed even higher than 100%, which was probably due to a degradation of the reference mirror used for the calibration. However, the implanted sample showed optical absorption in all measured wavelength spectrum. The sum of the reflectance and the transmittance on the

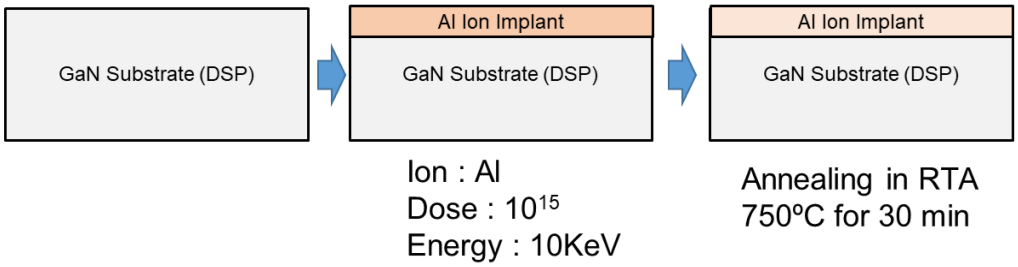


Figure 4.4 Processing steps for an ion implantation test sample.

implanted sample at 405 nm was ~96 %. By assuming 200 nm constantly implanted area from the top, ~2000 cm^{-1} of material loss was calculated. The internal loss, which is re-simulated considering the optical loss caused by the implantation out of the aperture and assuming 10% overlap, is ~41 cm^{-1} for the 420 nm laser. This value is much closer than ~15.02 cm^{-1} (simulated without considering implantation loss) to the internal loss of 68 cm^{-1} calculated based on the differential efficiency.

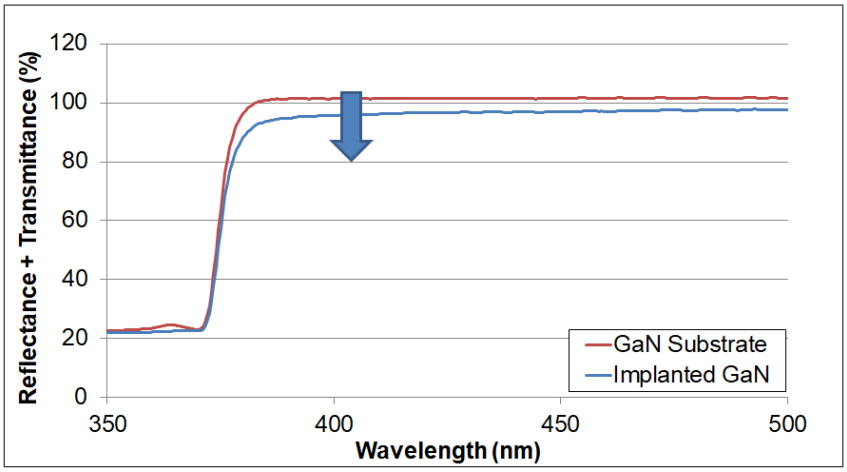


Figure 4.5 Sums of reflectance and transmittance at different wavelength for an m-plane DSP GaN substrate (red) before and (blue) after annealing and implantation.

4.1.4. CW Operation

Several VCSELs lasing at 408 nm under pulsed operation were measured under continues wave (CW) operation, though none of them were lasing. It must be because input power increased device temperature and degraded device performance. However, several VCSELs lasing at 420 nm under pulsed operation also lased under CW operation as shown in figure 4.6. It started to lase at a current density of ~30 kA/cm^2, and the output power was quickly rolled over at ~36 kA/cm^2. This CW operation could be possible because of the choice of the lasing wavelength considering the heating effect. More details will be dealt in chapter 4.3.

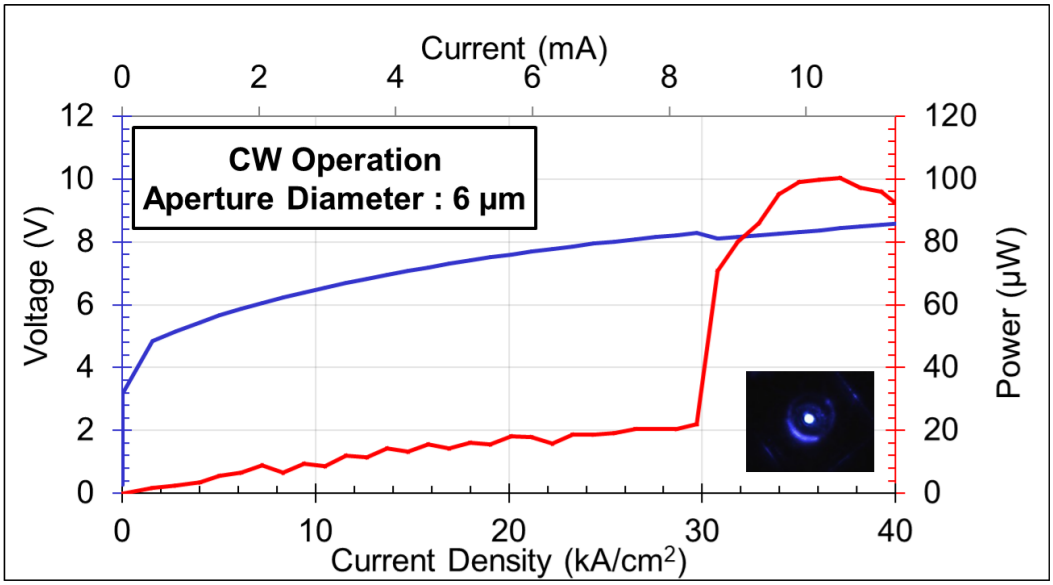


Figure 4.6 L-I-V characteristics of an IIA VCSEL lasing under CW operation.

4.2. Buried Tunnel Junction VCSEL

To avoid the optical loss caused by Al ion implantation, BTJ seems to be a promising alternative for current confinement replacing the IIA design. It does not add extra optical loss as the dielectric aperture design while allowing epitaxial regrowth as the IIA design. Moreover, the step-like structure around aperture can be used to improve lateral optical confinement. Despite the feasibility of the BTJ for VCSELs as already demonstrated in GaAs- and InP-based material system [8], [15], it has never been reported for III-N VCSELs because of the difficulties to form effective TJ contacts. Fortunately, the effective TJ contacts and VCSELs using them have been already demonstrated in UCSB [5], [27], [28], [46], [47]. Therefore, the next step was to try the BTJ VCSEL structure. As a result, the highest peak output power in UCSB, 2.8 mW (pulsed) and 726 μW (CW), was achieved. However, current leakages on the p/n-GaN junction area were still observed, which was probably due to etching damages.

In this chapter, epitaxial and structural design of the BTJ VCSEL will be discussed followed by device characteristics under pulsed and CW operation. The result will be also compared with the IIA VCSELs.

4.2.1. Design

The BTJ VCSELs were processed as described in chapter 2.2. One representative epitaxial structure for the BTJ VCSELs is described in table 4.2. After growing the main epitaxial structure until the p^{++}-GaN layer, the samples were dipped in BHF for 5 min followed by 10 nm n^{++}-GaN regrowth to form the TJ contact. Then ~40 nm GaN out of apertures was etched from the surface to define current apertures. Next, ~8 µm away from the apertures were implanted with Al ion followed by n-GaN regrowth as the current spreading layer. The rest of the processing steps were the same as IIA VCSELs with minor changes, such

Table 4.2 epitaxial structure of a BTJ VCSEL grown on an m-plane GaN substrate.

	Epitaxial Layer	Thickness (nm)	Doping concentration (cm^{-3})
3rd growth	n^{+}-GaN	85.5	7×10^{18}
	n-GaN	20	2×10^{18}
	n-GaN	20	1×10^{18}
2nd growth	n^{++}-GaN	10	10^{20}
1st growth	p^{++}-GaN	5	3.5×10^{20}
	p-GaN	81	10^{19}
	p-AlGaN	5	2.2×10^{19}
	GaN	3	UID
	InGaN (Single QW)	28	UID
	n-GaN	624.4	2.5×10^{18}
	n-AlGaN	15	$> 2.5 \times 10^{18}$
	n-GaN	80	2.5×10^{18}
	InGaN/GaN (Sacrificial MQW)	3 × 6/5	UID
	n-GaN (Template)	~ 1300	1.3×10^{18}

as top-down etching, sapphire flip-chip submount, number of n-DBR periods, and thickness of the Ta_2O_5 spacer.

4.2.2. Pulsed Operation

After the BTJ VCSEL processing, optical and electrical characteristics of the VCSELs were measured under pulsed operation. As shown in figure 4.7, the L-J-V characteristics of the VCSEL were analyzed under pulsed operation with a pulse width of 500 ns and a duty cycle of 0.5% at room temperature. The J_{th} and V_{th} were ~12 kA/cm^2 and ~9.9 V, respectively. The laser was measured up to a current of 100 mA (a current density of ~65 kA/cm^2) which gave the maximum output power of 2.8 mW. The Ŋd was 2.8% at the beginning of lasing and slowly decreased. The J-V characteristics were worse than the IIA VCSEL. It may be

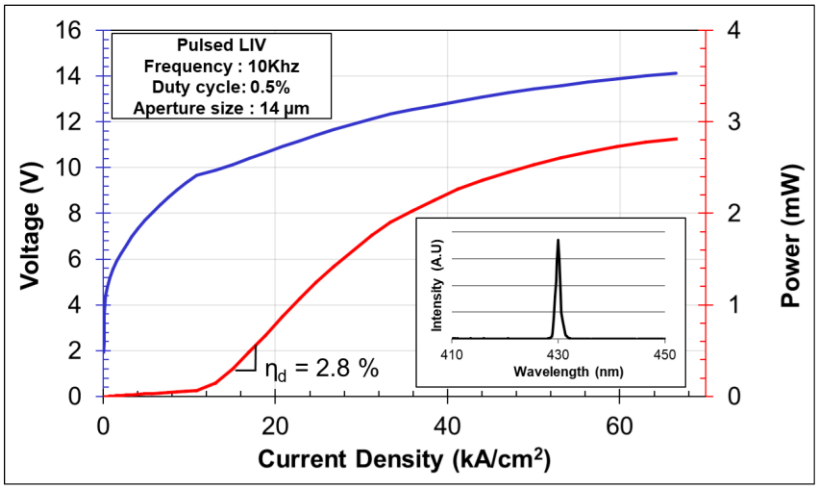


Figure 4.7 L-J-V characteristics of a BTJ VCSEL with a 14 µm aperture under pulsed operation. The lasing spectrum at 430 nm is inserted in the graph.

because the optimal TJ growth condition had been changed or the p^{++}-GaN layer was too thin; 5 nm for the BTJ VCSELs and 10 nm for the TJ test structures, and 14 nm for IIA VCSELs. Nevertheless, the BTJ VCSEL could be pumped over 14 V, which could risky for the IIA VCSELs. I suspect that the implanted p-GaN in the BTJ VCSELs had a higher breakdown voltage than the implanted p^{++}-GaN in the IIA VCSELs. It also implies that the p/n-GaN junction contacts can support high voltage when it is properly made. Moreover, the BTJ VCSEL showed much higher output power and differential efficiency than the IIA VCSELs demonstrated in the previous chapter. I suspect that it is due to lower optical loss out of aperture and better lateral optical confine.

Figure 4.8 shows variations of J_{th} and η_d as a function of aperture size. J_{th} scattered from 7 to 23 kA/cm^2 however it did not show clear tendency as the aperture size increases. Rather, it looks more constant for over 12 µm apertures. I think that it was affected less by the surface variation because the J_{th} is decided by the first lasing spot when filamentary lasing presents. However, the filamentary

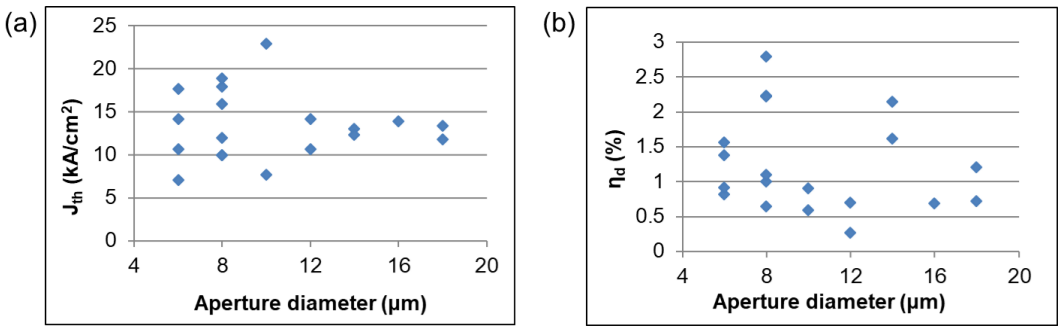


Figure 4.8 (a) Jth and (b) ηd of BTJ VCSELs for various sizes of apertures.

lasing will affect differential efficiency as shown in figure 4.8 (b). More measurement is needed for clear analysis.

4.2.3. Lasing Mode

Figure 4.9 shows microscope images of the lasing BTJ VCSELs right above threshold under pulsed operation taken by a Moticam. Typical linearly polarized (LP) modes were observed in figure 4.9 (lasers in red circles) corresponding to LP_{21} and LP_{11} (fig 4.9 a). Unlike the IIA VCSELs, the fundamental mode was not found. It must be something to do with lateral optical confinement caused by 40 nm aperture etching. The 12 µm and 10 µm aperture

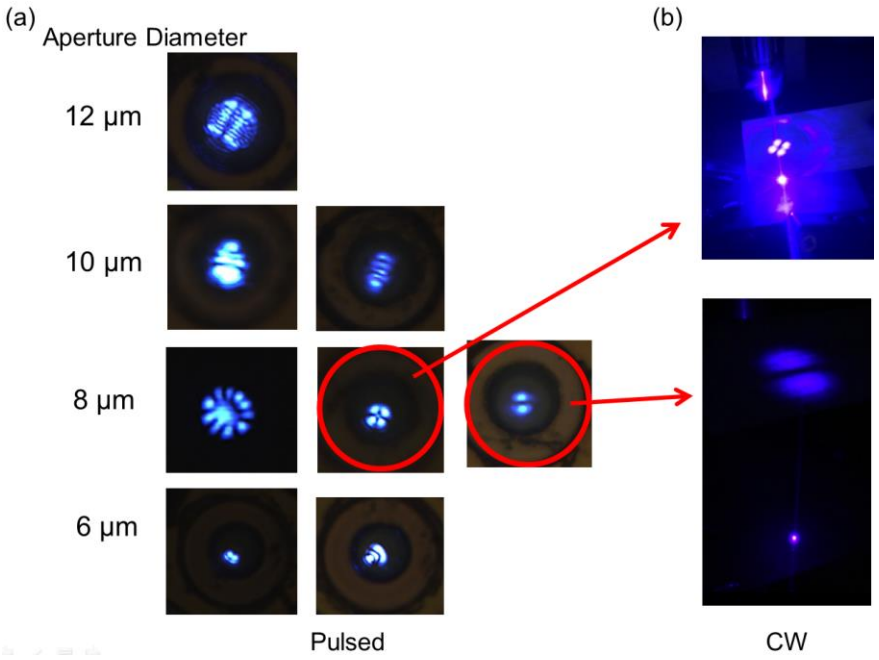


Figure 4.9 (a) microscope images of lasing BTJ VCSELs with various apertures under pulsed operation. (b) Pictures of far field patters on a paper were taken under CW operation.

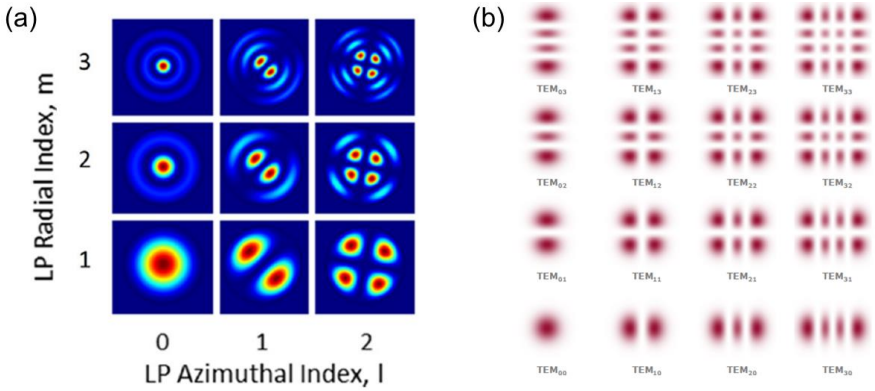


Figure 4.10 Intensity profiles of (a) linearly polarized modes and (b) rectangular transverse modes [43], [63].

lasing looks closer to rectangular transverse modes as shown in figure 4.10 (b). I suspect that it was due to the surface morphology after growth or after PEC etching. Filamentary lasing was also found in many other VCSELs, mostly in the large size (>8 μm). It may be due to many reasons, such as the surface roughness, the non-uniform current spreading, and the variation of TJ contacts. Figure 4.9 (b) shows pictures of the far field patterns illuminated on a paper under CW operation. However, the Moticam could not properly take their microscope images probably due to the output power (> 100 μW) passed its limitation.

4.2.4. CW Operation

Several BTJ VCSELs lasing at ~430 nm were measured under CW operation. Figure 4.11 shows L-J-V characteristics of a BJT VCSEL with the highest output power. The η_d (11%) was larger than under pulsed operation

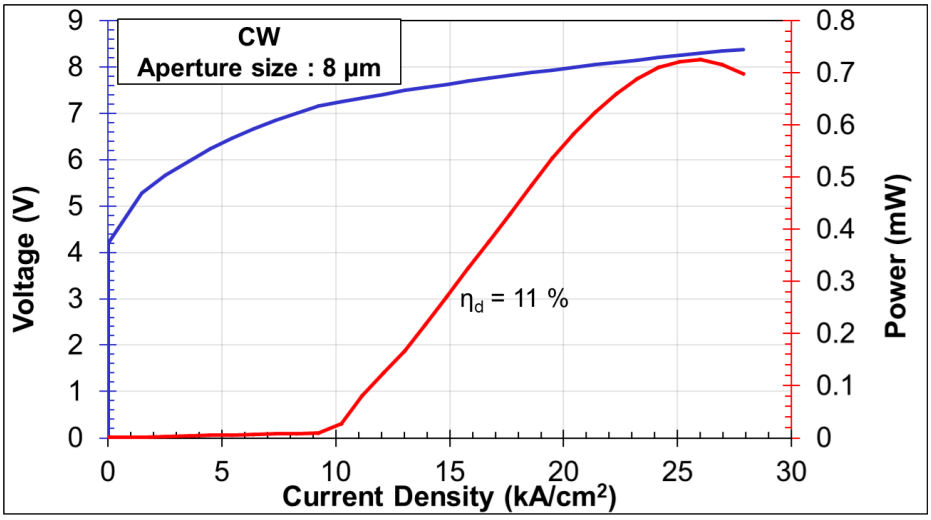


Figure 4.11 L-J-V characteristics of a BJT VCSLE under CW operation.

(2.8 %), which may be due to the heating. The heating effect is discussed in chapter 4.3. The VCSEL started to lase at ~10 kA/cm^2 and rolled over at ~26 kA/cm^2 with the peak output power of 726 μW. This output power is also much higher than IIA VCSEL results in chapter 4.1. The lower optical absorption out of the aperture must be the one main reason. However, the power was rolled over much earlier than under pulsed operation. Thus, the peak output will be increased by decreasing heat impedance and generation. Then, the heat generation can be reduced by improving I-V characteristics.

4.2.5. Analysis of Electrical Characteristic

Based on the results discussed in previous chapters, the VCSEL performance seems to be severely limited by electrical characteristics. For

example, the maximum output power of the device demonstrated in figure 1 could be higher if more current was applied, which may destroy the device because of breakdown voltage in p/n-GaN junction area or heating. Then, the current at which the power rolls over under CW operation (fig 4.11) could be higher if the overall device resistance was lower. Therefore, it is important to understand where the most resistive area presents for future design. For electrical character analysis, several other structures were also processed along with the BTJ VCSELs as shown in figure 4.12.

Structure A, B, and C were designed to separately analyze resistances in different area. Structure A, B, and C are designed to see I-V characteristics without current spreading on n-side, p-side, and both sides respectively. For example, the resistance caused by the p-side current spreading could be calculated by comparing structure A and C. Unfortunately, I could not collect reliable data as shown in figure 4.13. The structure D showed the worst I-V curve, which should

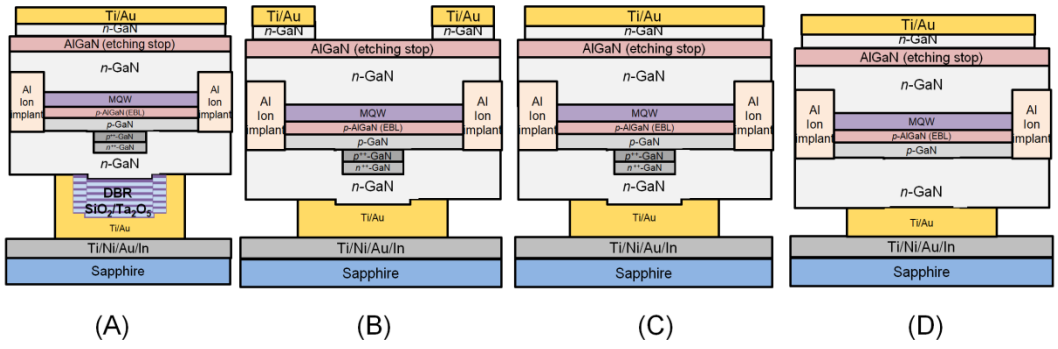


Figure 4.12 Test structures to analyze I-V characteristics of a BTJ VCSEL without current spreading on (a) n-side, (b) p-side, and (c) both sides and (d) without a TJ contact.

show the best because of the vertical current flow without the current spreading. The structure D looks turning on the latest probably due to the variation of the TJ contact. This analysis may be worth to be tried again when the variations of TJ and p/n-GaN junction contacts are minimal.

The structure D was designed to evaluate the breakdown voltage in the p/n-GaN junction contacts which will limit the maximum voltage applied on the BTJ VCSELs. When apertures were formed, entire surfaces were etched to eliminate GaN TJ contacts, current apertures. Then, they should block current flow if the BTJ structures effectively confine current. Metal was also deposited on top and bottom without DBRs allowing vertical current following without current spreading, which was severe condition than real BTJ VCSELs. Figure 4.14 shows I-V characteristics of a structure D and a lasing VCSEL in the same wafer. However, the current was started to flow at ~9 V despite the test result showed the

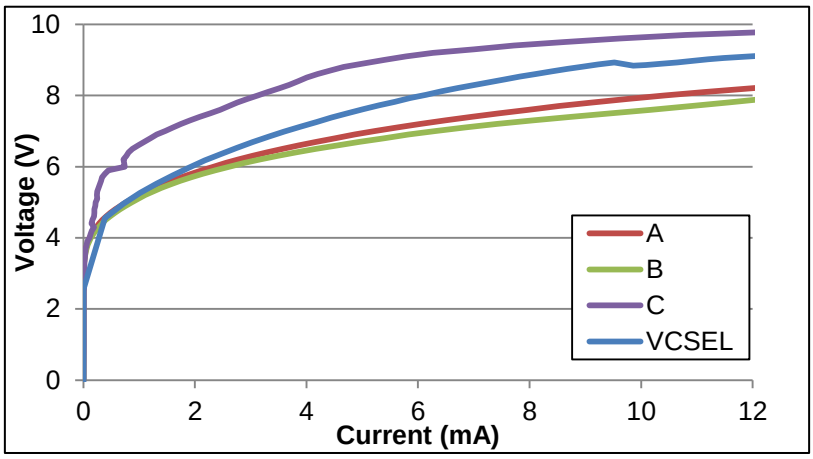


Figure 4.13 CW I-V characteristics on test structure a, b, and c (fig 4.12) and a BTJ VCSEL with a 10 µm aperture.

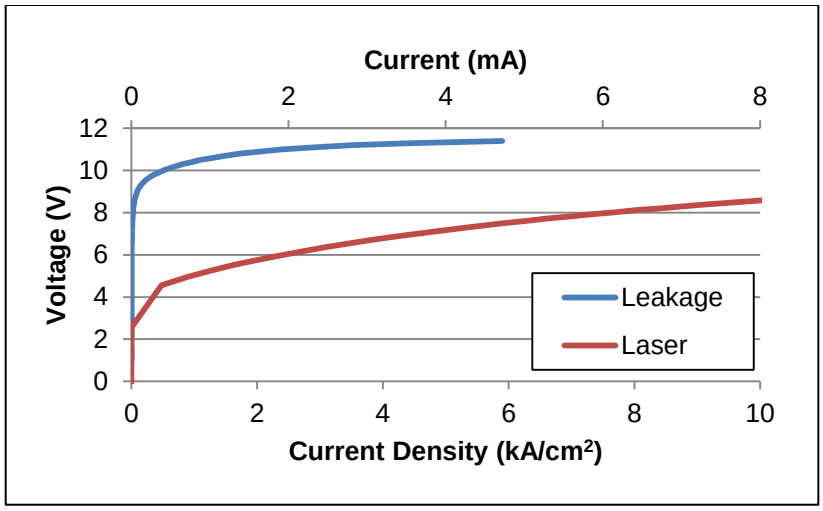


Figure 4.14 I-V characteristics of (blue) a test structure D and (red) a BTJ VCSEL under CW operation.

breakdown voltage over 20V in chapter 3.4.3. Furthermore, several samples on different epitaxial structures showed even lower breakdown voltages, which would drastically increase the threshold current densities and overall operation currents. I suspect that etching damage passing through the active layer caused the leakage path. Dimmer light was also observed in a similar structure without TJ contacts, which implies that the active layer had been damaged. Unlike the test structure, etching ~20 nm from the p^{++}-GaN in chapter 3.4.3, this structure was etched ~40 nm from the n^{++}-GaN which was etched deeper for a longer time. Furthermore, the total p-GaN thickness was also thinner than the test structure. So, longer and closer etching to active layer would bring this result. The p/n-GaN junction contact area should be mainly studied for the next device. Fortunately, this sample started to lase at ~7.2 V and rolled over at 8.3 V before the breakdown

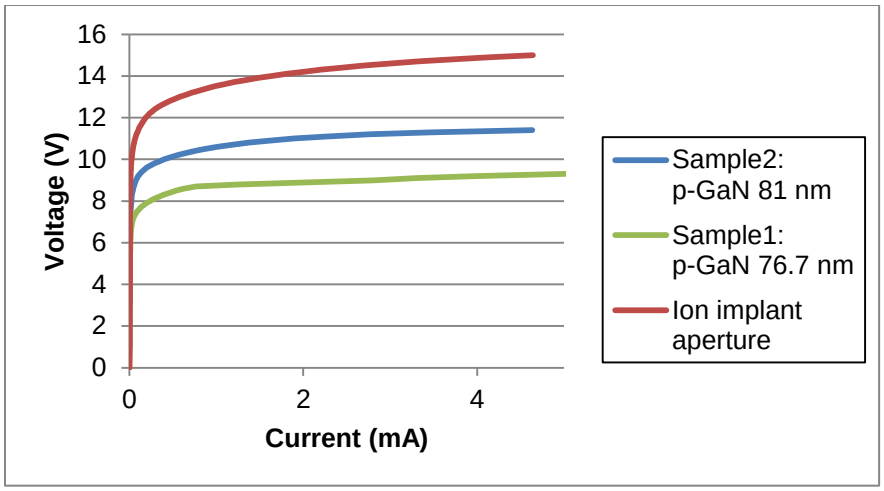


Figure 4.15 I-V characteristics of a test structure D processed on different epitaxial structures and a similar structure for ion implantation aperture.

voltage of the p/n-GaN junction contact, 9 V. Figure 4.15 shows the same measurement on the epitaxial structure having different thickness of the p-GaN layer as well as a structure on ion implanted aperture VCSELs. Epitaxial structure having thinner the p-GaN layer will be more suffered from etching damage which results in leakier device. This result also supports that leakage is caused by etching damages. The structure on ion implanted aperture means that entire mesa was Al ion implanted on the p^{++}-GaN layer.

Lastly, CTLM-like structures (an illustration in figure 4.27) were measured to verify ohmic contact between n-GaN and metal (Ti/Au) on p-side and n-side as shown in figure 4.16. On the p-side, metal contacts were deposited without any surface treatment after lithography. As shown in figure 4.16 (a), the contact came out non-ohmic, which may add additional voltage for the VCSELs.

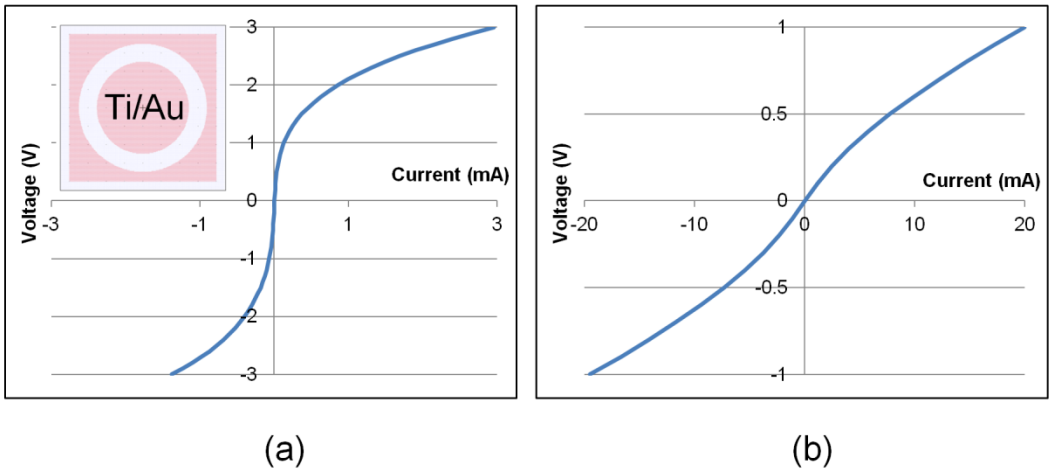


Figure 4.16 Electrical characteristics of one CTLM pattern (inserted image) for n-contacts on (a) p-side and (b) n-side. The radius of the inner circle was 25 µm and the gap was 10 µm.

It could be improved by increasing doping concentration in the top n-GaN layer and performing proper surface treatments. In contrast, contacts on n-side show almost ohmic contacts (fig 4.16 b) despite the low doping concentration in the n-GaN layer on the n-side. I think that $SiCl_4$ RIE etching at 270 W for 10 sec effectively improved the n-contacts with n-GaN.

4.3. Thermal Effects

Because low wall plug efficiency (WPE) of III-N VCSEL is very low, less than 1%, most of the input power will be converted to heat. In general, we do not want to increase temperature because it degrades VCSEL performance. Especially, heating is one of the main factors limiting the performance of VCSEL under CW operation. So, it is important to improve the thermal dissipation and to minimize

the thermal effect. Compared with GaAs- and InP-based, III-N VCSELs have higher operation voltages because of the wide band gap, the poor p-contact, the current spreading issues, higher threshold current and so on. Some of the problems can be reduced by improving electrical and optical characteristics, which is discussed in previous chapters.

In this chapter, thermal characteristics of our VCSEL structure and suggestions for future design are presented. Next, the negative effects of the heating will be discussed followed by a proposal to compensate them with experimental data. Lastly, heating effects on cavity resonance and electrical characteristics will be mentioned.

4.3.1. Thermal Impedance

Structurally, our VCSEL design poses a thermal issue because the dielectric DBR has a low thermal conductivity which was placed between submount and current aperture. Epitaxial DBR will be also just slightly better due to the low thermal conductivity of AlN and many numbers of DBR periods. To investigate the structural issue, Comsol was used for thermal simulations.

Figure 4.17 shows a simplified VCSEL structure with 8 μm diameter aperture for thermal modeling. It was assumed that 0.1 W of input power was applied in the active region. As shown in figure 4.17 (a), heat dissipated laterally

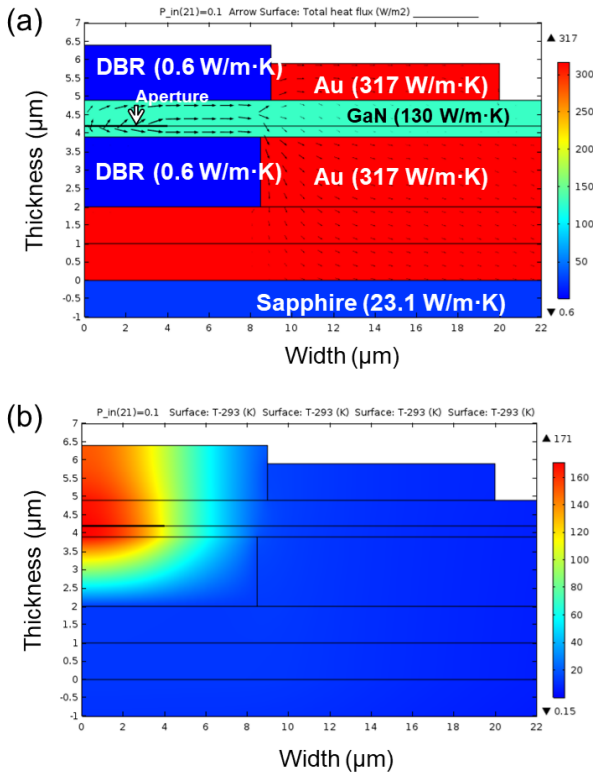


Figure 4.17 Simulated (a) heat flux and (b) temperature profile of a half of a VCSEL cross-section with an 8μm aperture at 0.1 mW input power. A cylindrical shape was assumed for simple analysis.

from aperture to gold contact because of the low thermal conductivity of the bottom DBR. As a result, the heat was trapped in the center of aperture as shown in figure 4.17 (b). 171 K additional temperature was applied in the center when 0.1 W was supplied, which means 1710 K/W of thermal impedance.

So structurally, thermal impedance will mainly depend on the thickness of GaN and the distance from the current aperture to top and bottom metals. Figure 4.18 shows how the thermal impedance decreases as the distance gets closer. When the lateral distance from the aperture to the p- and n-contact reduced to 2

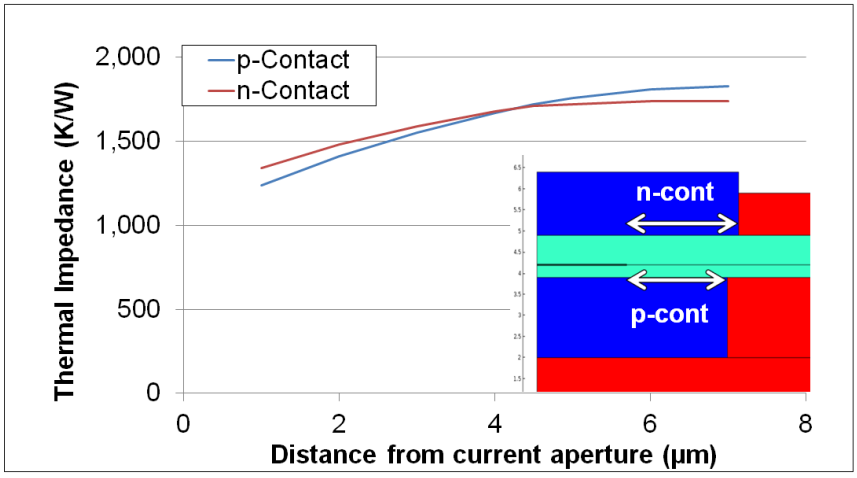


Figure 4.18 Thermal impedance change when lateral distance from a current aperture to (blue) p-contact and (red) n-contact changes. The original distance is 4.5 µm for p-contact and 5 µm for n-contact.

µm from the original design, thermal impedances reduced to 82 % and 86 % respectively. Because the submount was under the p-side and the active layer is close to p-side, reducing distance from aperture to p-contact was more effective. Thus, reducing the distance may mean that the device can handle ~18 % of more input power until the laser output power rolls over, which will improve the maximum output power under CW operation. Moreover, series resistance due to current spreading also decreases, reducing input voltage and heat.

Unfortunately, this suggestion cannot be simply processed by reducing mask design. To bring the p-contact closer, the diameter of the p-DBR must be reduced, which requires low lithography tolerance. Using a contact aligner, it is very risky to have below 1.5 µm tolerance between two masks. Bring the n-contact closer is even harder. The n-contact mask should be aligned with an

alignment mark processed before flip-chip bonding, which will be placed under the GaN cavity. Reducing the gaps may be possible using a stepper. However, I would still not try to reduce the tolerance on n-side because it does not significantly improve thermal impedance after reducing it on p-side. If the p-side gap is 2 µm, the thermal impedance changes only from 82 % to 79 % when the n-side gap changes from 5 µm to 2 µm.

To reduce the gap, the edge shape of the p-DBR should be also considered. Figure 4.19 (a) is an SEM image taken after p-DBR liftoff. The DBR was not perfectly cylindrical. The thickness gradually tapered from the edge. It must be due to undercut etching of the negative PR and unintended angled deposition by IBD. As also shown in figure 4.19 (b), the bottom DBR looks trapezoid shape (blue circle). Reducing tolerance below 1 µm will not be easy due to this tapered shape. The P-contact metal can be deposited first to avoid this issue, though one lithography step and metal deposition may be additionally required.

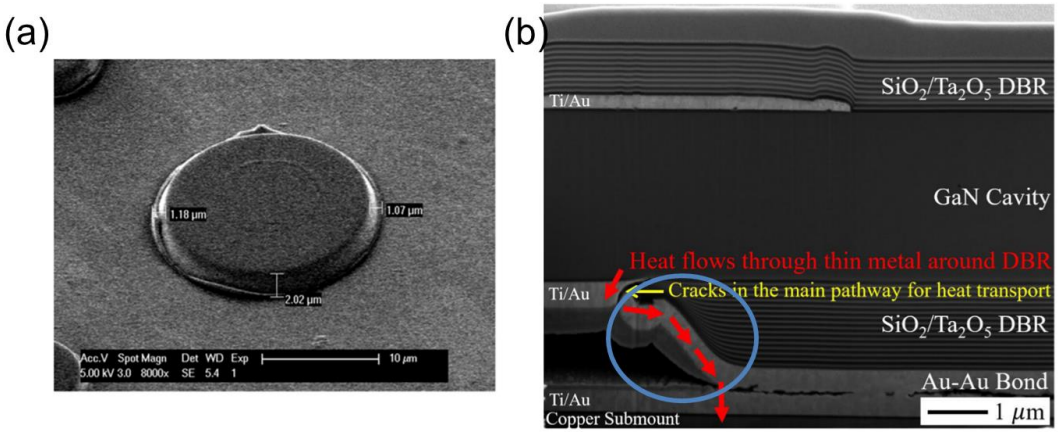


Figure 4.19 (a) An SEM (b) a FIB image of a p-DBR. The FIB image was taken by Charles [41].

Figure 4.20 shows thermal impedance change with different submounts. In theory, using materials with higher thermal conductivity will be better for heat dissipation. However, the right materials should be chosen also considering processing steps, especially flip-chip bonding and PEC etching. Materials reactive with KOH solution, such as Si and Al, will not be proper in our process. In my experiment, aluminum blocks coated with Ti/Au on top and bottom were still very reactive in the solution. The aluminum was etched in KOH with bubbles and the Ti/Au metal was easily peeled off. It might be because the metal coat was easily scratched and exposed the aluminum surface. For the flip-chip bonding, the surface roughness and flatness are also important factors in yield. I tried Au-Au flip-chip bonding with thick copper blocks after polishing with diamond grids and also with thin polished copper. However, making one unpolished copper flat and smooth takes time and is not easy. The thin copper is also easily bent. So, overall yield was low. I used SiC and sapphire submount but did not see a noticeable benefit with SiC submount. As shown in figure 4.20, thermal impedance just reduces 5% by replacing sapphire with SiC, which has more than 5 times higher thermal conductivity. And the similar effect can be easily achieved by depositing thick gold on submount. So, for my final device, more than 4 μm thick metal including Au and In is used between p-DBR and sapphire submount. Sapphire submounts were used instead of SiC due to cost matter.

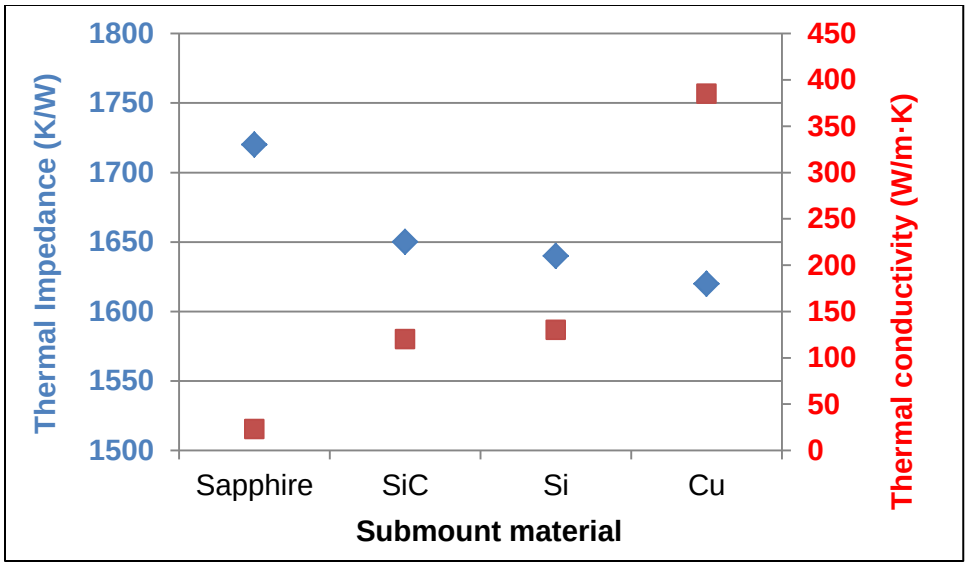


Figure 4.20 (blue) Simulated thermal impedance of a VCSEL with different submount materials and (red) their thermal conductivity.

In conclusion, 1710 K/W of thermal impedance was found for our current VCSEL design due to the low thermal conductivity of the dielectric DBR. Placing metal contact close to aperture may improve the thermal impedance, although fabrication difficulties are present.

4.3.2. Degradation of Device Performance

As temperature increases, the performance of VCSELs usually degrades due to increasing internal loss and decreasing injection efficiency. Internal loss increases as the material absorption increases due to an increment of free carriers at a hot temperature. Injection efficiency also decreases as non-radiative recombination rate increases. In this chapter, thermal effects will be investigated

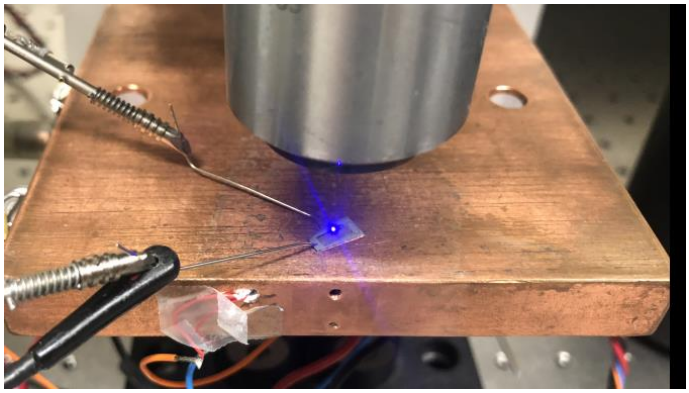


Figure 4.21 A sample is placed on a copper plate connected with a temperature controller and a thermometer.

for VCSELs by varying stage temperature as in figure 4.21.

A BTJ VCSEL chosen for this experiment had a lasing wavelength at ~417 nm and spontaneous wavelength peak at ~410 nm. The spontaneous emission was measured by quicktest. The epitaxial structure was the same as Table 4.2. Figure 4.22 (a) shows L-I curves of the VCSEL measured as increasing stage temperature under pulsed operation. As expected, an increase of threshold

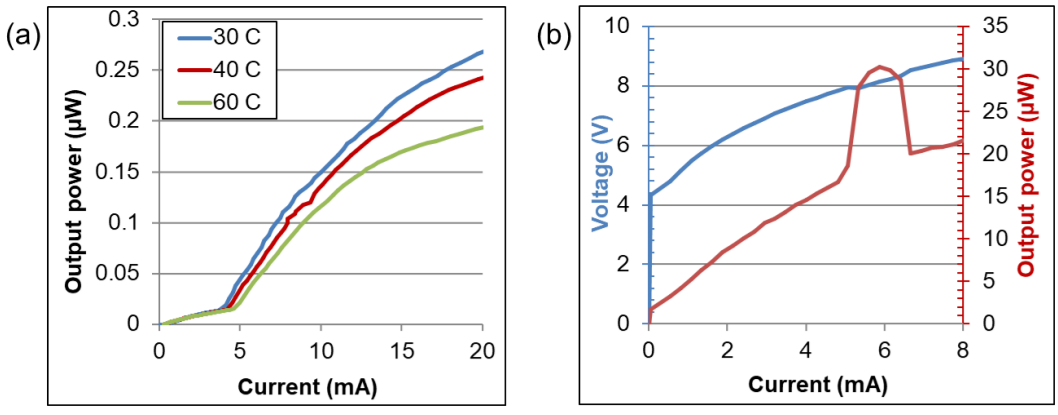


Figure 4.22 (a) L-I curves of a BTJ VCSEL at different temperatures under pulsed operation and (b) its L-I-V curve under CW operation at room temperature.

current density and a decrease of differential efficiency were observed, which result in degradation of the output power. It became worse under CW operation probably because of even hotter temperature as shown in figure 4.22 (b). It lased at higher threshold current and rolled over right after ~1 mA. The peak output power was also much lower than the result under pulsed operation.

L-I-V characteristics of an IIA VCSEL were also measured at different stage temperatures under pulsed operation. The VCSEL had the same structure as in chapter 4.1.1. Figure 4.23 (a) shows spectrum measured from a lasing VCSEL (blue) and from quicktest (red) right after its epitaxial growth. The peak wavelength of the VCSEL is 409 nm which is 6 nm longer than the spontaneous emission at 403 nm. Threshold current densities were plotted as a function of stage temperature as shown in figure 4.23 (b), which also increased as the BTJ VCSEL mentioned above paragraph. This device did not lase under CW operation. These tendencies will be a major obstacle degrading and preventing CW operation.

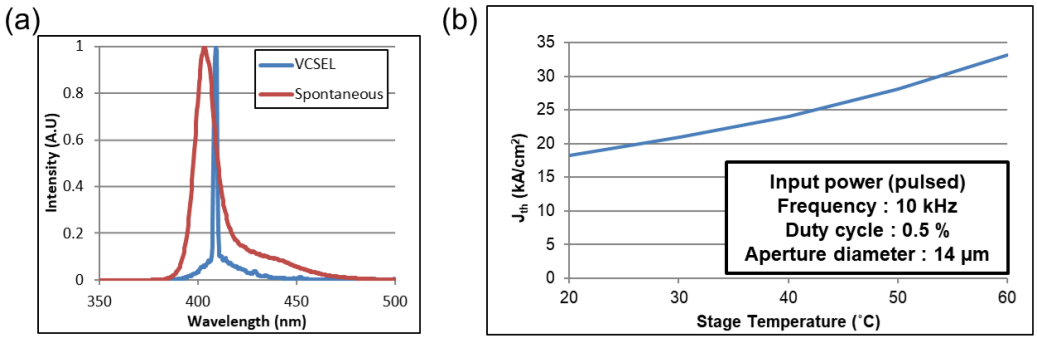


Figure 4.23 (a) spectrum of a 14 µm VCSEL and a spontaneous emission of its wafer and (b) a plot of threshold current density as a function of stage temperature.

4.3.3. Targeting Longer Wavelength

When we almost finished processing before the last DBR deposition, when most of factors are already decided including optical property, thermal impedance, epitaxial structure, and so on, there are not many things to do to improve heat dissipation. However, we can still shift a lasing wavelength using different thickness of a dielectric spacer, Ta_2O_5 in my case. The spacer changes cavity length, which changes resonance frequency. As heat increases the vibration of atoms, effective lattice constant also decreases, which reduces band gap. As a result, the wavelength from the active layer also effectively increases in hot temperature. If VCSELs are designed to lase at longer wavelength considering the thermal effect, it may be advantageous under CW operation.

For some IIA VCSEL samples, different thickness of the Ta_2O_5 spacer was deposited to target ~15 nm longer wavelength than a spontaneous wavelength. The IIA VCSELs had a similar structure as described in table 4.1, but had AlGaN etching stop layer. Figure 4.24 (a) shows spectrum measured from quicktest (red) and the lasing VCSEL (blue) under pulsed operation. The peak wavelength of the VCSEL came out as ~423 nm which is 17 nm longer than the spontaneous emission at 406 nm. Threshold current densities were plotted as a function of stage temperature as shown in figure 4.24 (b). Unlike previous result (fig 4.23), J_{th} barely changed as increasing stage temperature, and even slightly decreased,

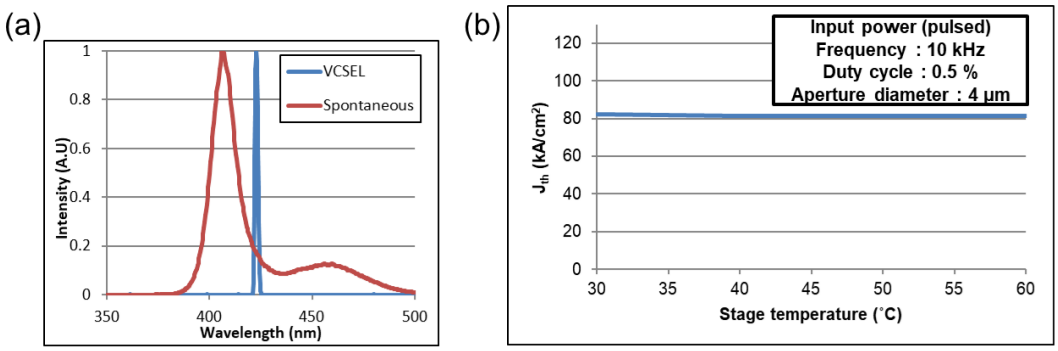


Figure 4.24 (a) spectrum of a 4 μm VCSEL and a spontaneous emission of its wafer and (b) a plot of threshold current density as a function of stage temperature.

though J_{th}. I suspect that the degradation was compensated as the wavelength shift both caused by the heat effect. With this VCSEL structure, CW lasing could be achieved as shown in chapter 4.1.4.

Another BTJ VCSEL which was on the same flip-chip submount with in chapter 4.2.2 was also used for temperature dependency. It was also designed to compensate for the thermal effect, lasing at ~430 nm which is ~20 nm longer than a spontaneous wavelength. Figure 4.25 shows L-I curves of the VCSEL measured as increasing stage temperature under pulsed operation. It also shows the opposite result as typical characteristics. The threshold current density was decreased, and differential efficiency was increased as temperature increases. It seems that the improvement of the wavelength shift overcomes the degradation caused by heating. Figure 4.25 (b) shows the threshold current density and differential efficacy of the VCSEL as a function of stage temperature. Overall performance was improved until at ~ 70 C and started to be degraded from 80 C. This will be

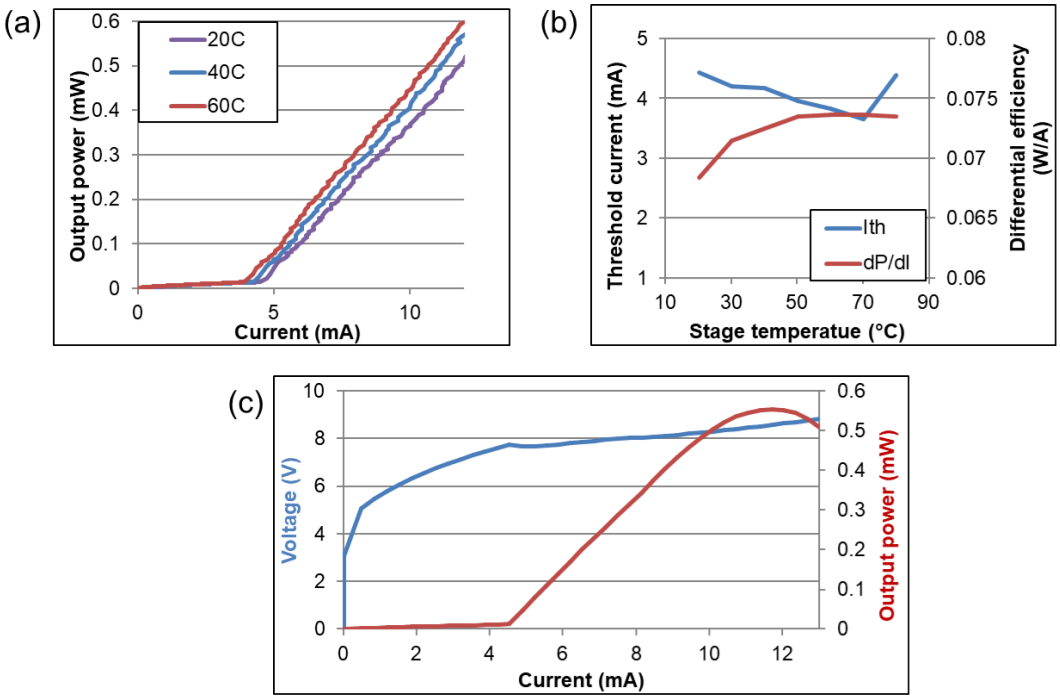


Figure 4.25 (a) L-I curves and (b) plots of I_{th} and dP/dI at different temperatures under pulsed operation and (c) L-I-V curve under CW operation for a 8 μm BTJ VCSEL.

the point where the degradation overcomes the wavelength shift. Figure 4.25 (c) is L-I-V curve under CW operation, which shows a J_{th} of ~9 kA/cm^2 and a η_d of 3.2 % (dP/dI of 0.092).

In conclusion, targeting longer wavelength considering QW wavelength shift showed better results under CW operation for IIA and BTJ VCSELs. Moreover, such results have been constantly observed in other devices, so it happened unlikely due to unintentional better mode overlap with the active layer at the longer wavelength. The tendency, decreasing threshold current and increasing differential efficiency at a hot temperature, will be because of bandgap

shrink of QW. However, higher peak output power does not necessarily only because of wavelength shift in QW. I suspect that longer wavelength is also generally advantageous due to lower material abortion and scattering loss [49].

4.3.4. Refractive Index and Conductivity

It is well known that the lasing wavelength of VCSELs shifts because refractive index changes as temperature changes. This change will depend on material property, thickness, wavelength, and so on. Figure 4.26 shows lasing wavelength shift of a BTJ VCSEL at different temperatures. As in figure 4.26 (b), wavelength almost linearly changes in our measurement range. Assuming that cavity thickness of the VCSEL is exactly 5-λ at 429.33 nm comprises of only GaN with refractive index of 2.5231 at room temperature (23℃), ~1.3 x 10^{-4} (K^{-1}) of d*n*/dT is obtained from this measurement. This result is quite close to reference 1.47 x 10^{-4} (K^{-1}) calculated based on equation (4.2), though it was done on c-plane

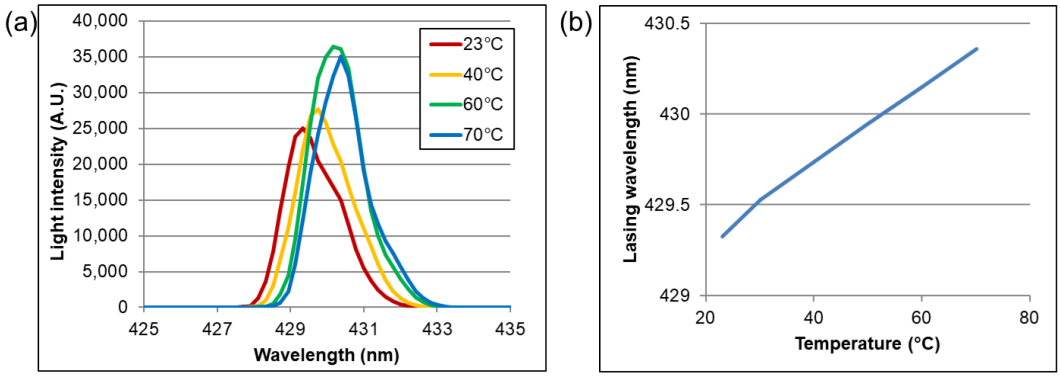


Figure 4.26 (a) Spectrum and (b) peak wavelength of a BTJ VCSEL under pulsed operation at different temperatures.

GaN on sapphire [64]. Despite poor resolution of a spectrometer used for VCSELs, the change was big enough to be observed.

$$\partial n_o/\partial T(\lambda)_{GaN} = 4.247 \times 10^4 \lambda^{-3} - 1.592 \times 10^2 \lambda^{-2} + 2.187 \times 10^{-1} \lambda^{-1} - 3.427 \times 10^{-5}\ (K^{-1}), \quad (4.2)$$

I-V curves under CW have showed lower resistance than under pulsed operation. It will be also mainly because heat increased free carrier concentration, so conductivity. Figure 4.27 is I-V curves under pulsed operation at different stage temperature overlapped with CW curve. I-V curves became better as temperature increases. However, overlap with CW data would not exactly match with stage temperature under pulsed because of a noise of pulsed measurement.

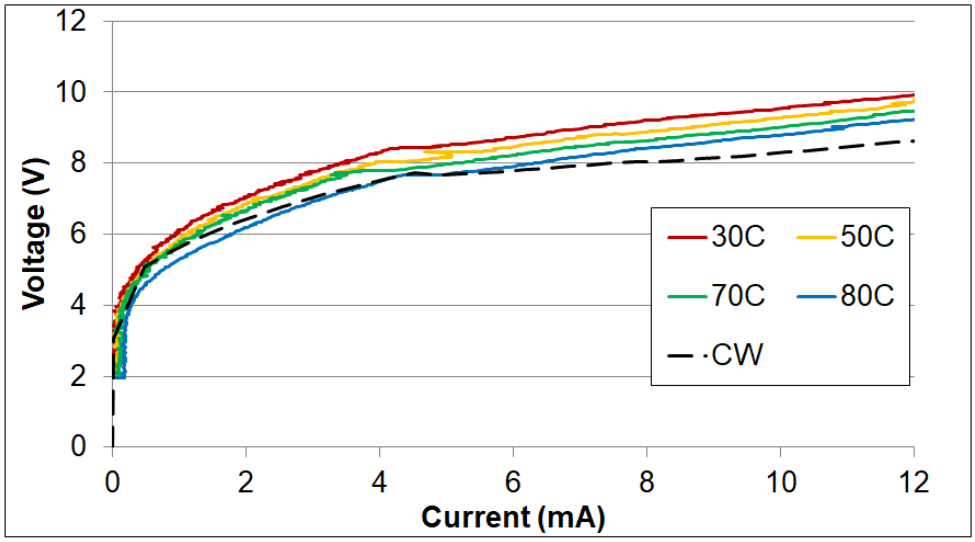


Figure 4.27 I-V curves of a BTJ VCSEL under (solid lines) pulsed operation at different temperatures and (dashed black line) CW operation at room temperature.

5. Conclusion

We have investigated epitaxial structure, TJ contact, and thermal effect for VCSEL design. Effective GaN TJ contact could be grown only by MOCVD using 2-step growth, high doping for p- and n- GaN, and BHF surface treatment. The optimized TJ growth technique applied to IIA VCSELs which brought similar result as VCSELs with hybrid MOCVD/MBE TJ contact. Moreover, CW lasing was also demonstrated by intentionally shifting lasing wavelength to compensate heating effect. Finally, VCSELs with BTJ current apertures were processed, which brought the peak output power of 2.8 mW under pulsed operation and 726 μW under CW operation.

It has been more than 8 years since the first demonstration of electrically pumped non-polar VCSELs. Yet, I think that the development of III-VCSELs is still at an early stage posing many unconfirmed and unoptimized areas. In other words, there are many chances to get publishable results. I suggest future works as follows:

1. Green VCSELs: VCSELs lasing at 15~20 nm longer than spontaneous wavelength brought the high output power and CW operation because of the heating effects. The main difficulties of green lasers come from poor quantum efficiency when indium composition of InGaN is high. Using the thermal

wavelength shift, green VCSELs may be achieved with active layers having >20 nm shorter spontaneous emissions.

2. Near UV VCSELs: We have already achieved VCSELs lasing at 403 nm or even shorter wavelength. Shifting wavelength just below 400 nm would not be so difficult. Based on our measurement, Ta_2O_5 and SiO_2 films still remain lossless until a wavelength of ~365 nm. Moreover, using TJ contacts is almost mandatory due to the severe optical absorption of ITO, and VCSELs with TJ contacts were demonstrated only in UCSB. 369.5 nm VCSELs for atomic clocks may be achievable.

3. Growing MOCVD TJ contacts in 1-step: successful TJ contacts were achieved only using the 2-step growth. However, exposing the surface in the air would never be desirable due to uncertain residues. If all reasons why the 2-step growth improves TJ contacts, the 1-step growth will be also possible.

4. Epitaxial structure optimization: changing epitaxial structure will give answers for the fundamental aspects of III-N VCSELs. However, our trials to optimize epitaxial structures, especially the active layer, have never been successful because of uncertain factors from VCSEL processing and epitaxial growth. I believe that the VCSEL performance will step up after optimizing epitaxial structure. However, this should be studied when other factors are reliable.

5. PECA VCSELs: The PECA VCSEL demonstrated by John showed an output power of ~180 μA under pulsed operation. It might not be considered high

now. However, the VCSEL still had ITO for current spreading instead of a TJ contact. Moreover, only few devices were survived until the end of the process because of physical vulnerability. If we develop the structure and put all our advanced techniques including TJ contact and longer wavelength design, it will bring much better result than previous PECA VCSELs.

There are many other future works not listed above. However, I believe that one of each may be enough for one thesis topic. Since the first III-VCSEL demonstration by Casey Holder in UCSB, the peak output power has been improved from 0.019 mW to 2.8 mW. I believe that the increasing III-N VCSEL technologies and industrial interests in III-N materials will accelerate commercialization of III-N VCSELs.

Appendix

A1. Process Flow for BTJ VCSELs

I edited following process flow based on John's and Charles's work. There are still many parts to be optimized to improve yield, to reduce process step, and to increase output performance.

181029 VCSEL Process Flow - BTJ Aperture		
Edited by SeungGeun		
Mask file name: 180426_IIA_VCSEL		
General Prep	Flip-chip substrate Prep	See end of process follower
	PR Bench	Prep PRs and check expiration date
		SPR220-1.8
		SPR220-3.0
		SPR220-7.0
		nLOF2020
		nLOF2035
Calibration (Day 1)	MOCVD	Grow XRD and emission wavelength calibrations for all relevant layers in the device
Calibration (Day 2)	XRD	Analyze XRD calibration samples using ~35 min 2-theta/omega scans (6-8hrs XRD time)
		Fit the XRD data by simulating the structure and adjusting the parameters by hand, until a good fit is obtained (do not simply fit the thickness fringes)
	Quicktest	Deposit 80 um diameter Pd/Au p-contacts using old CTLM mask and measure LIVS on the emission wavelength calibration sample, using 4-pt probe method
	Computer	Adjust the growth times and QW temperatures on the layers of interest in all the recipes. λEL>λFP is not desirable (i.e. λEL<λFP or λEL=λFP is preferred). λsacrificial>405nm is required for PEC etching. λsacrificial>420nm is required for observation under Fluorescence microscope

Growth (Day 3)	MOCVD	Grow the desired VCSEL Series
Begin Processing (Day 4)	Furnace	600C, Air, 15min
	Quicktest	Solder In dots onto corners only. Do not press through shadow mask, it will leave residue. Measure Quicktest data for the VCSELs. Save all spectrum and IV data. Regrow if power or voltage is bad
Remove Indium	Acid Bench	3:1 HCl:HNO3 Aqua Regia, 3x 10min, mix new batch each iteration, wait 5min for boiling, 120C on hotplate. End with DI+Tergitol clean, N2 dry
TJ regrowth	Acid Bench	BHF 5 min (To remove Mg film) & DI rinse
	MOCVD	Grow 10nm n++GaN
Alignment Litho	Solvent Bench	Sonicate on high: 2min Ace, 2min Iso, 3x 30s DI Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Soft bake, 110oC 90s
	Contact Aligner	Expose **"1.Alignment"**, **10s**,7.5mW/cm2, No Filter, Black chuck, **Hard contact**
	Develop Bench	Post exposure bake 110oC 60s
		Develop in AZ300-MIF **50sh**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
Alignment Etch	RIE5	Load bare carrier wafer
		Standard O2, BCl3/Cl2 preclean (Dan_01 (~10min pump down, 10min O2 clean))
		Load samples onto carrier wafer, no oil
		Dan_05 (120 nm/min) BCL3 (10sccm, 10mT, 100W, 2min), Cl2 (10sccm, 5mT, 200W, 5 min)
	Solvent Bench	Preheat AZ NMP Stripper for 10 min, 80 C
		Sonicate on low AZ NMP at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry
Aperture Litho	Solvent Bench	Sonicate on high: 2min Ace, 2min Iso, 3x 30s DI Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)

		Spin **SPR220-1.8** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Soft bake, 115oC 90s
	Contact Aligner	Expose **"2.IONIMPLANT APERTURE"**, 7.5mW/cm2, **25s,** No Filter, Black chuck, **Hard contact**
	Develop Bench	**Post exposure bake 115°C 60s**
		Develop in AZ300MIF **50s**
		30 sec DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
Aperture Etch	RIE5	Load bare carrier wafer
		Standard O2, BCl3/Cl2 preclean (Dan_01 (~10min pump down, 10min O2 clean))
		Load samples onto carrier wafer, no oil
		SLEE_02 (110 nm/min) (etch past p++ & n++GaN), Cl2 (10sccm, 5mT, 200W) **(this step should be optimized)**
	Solvent Bench	Preheat AZ NMP Stripper for 10 min, 80 C
		Sonicate on low AZ NMP at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry
Ion Implant hardmask Litho	Solvent Bench	Sonicate on low: 3min Ace, 3min Iso, 3x 30s DI Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **nLOF2020** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Soft bake, 110oC 90s
		Expose **"8.IONIMPLANT (BTJ)"**, **10s**,7.5mW/cm2, No Filter, Black chuck, **Hard contact**
		Post exposure bake 110oC 60s
		Develop in AZ300-MIF **50s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
Ion Implant hardmask Litho	Acid Bench	**HCl 1min, 3x 30s DI Dump&Rinse, N2 Dry**
	Ebeam 3	Deposit Ti/Au 200A (1A/s)/ 2000A (1A/s→100A,3A/sec→500A, 6A/sec→2000A)
	Solvent Bench	Preheat AZ NMP Stripper for 10 min, 80 C
		Sonicate on Low AZ NMP at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry

	Microscope	Inspect, liftoff more if necessary
Ion Implant	Leonard Kroko, Inc	Ship samples to Leonard Kroko
		wafer size: ~1cm2
		Ion: Al, Dose: 1015 ions/cm2, Energy: 20 keV, Normal incidence
		~3-4 day turn-around
	Acid Bench	3:1 HCl:HN03 Aqua Regia, 3x 10min, mix new batch each iteration, wait 5min for boiling, 120°C on hotplate. End with DI+Tergitol clean, N2 dry
	3D Microscope	Inspect, strip more if necessary
n-GaN Current Spreading Growth	UV Ozone	20 min (Oxidize Si on surface) (Right before regrowth)
	Acid Bench	BHF 5 min (Remove SiO2) & DI rinse
	MOCVD	Grow n-GaN (Model the structure in VERTICAL to get correct thickness)
	AFM (optional)	Measure intracavity contact RMS roughness
Mesa Litho	Solvent Bench	Sonicate on high: 2min Ace, 2min Iso, 3x 30s DI Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 30sec
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **SPR220-3.0 Program 3 (2000rpm 45s (?))** (use SPR 220-7.0 for thick cavity)
		Soft bake, 115oC 90s
	Contact Aligner	Expose **"3.MESA"**, 7.5mW/cm2, **25s,** No Filter, Black chuck, **Hard contact**
	Develop Bench	**Post exposure bake 115°C 60s**
		Develop in AZ300MIF **60s**
		30 sec DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
	Confocal Microscope	Measure PR thickness
Mesa Etch	RIE5	Load bare carrier wafer
		Standard O2, BCl3/Cl2 preclean (Dan_01 (~10min pump down, 10min O2 clean))
		Load samples onto carrier wafer, no oil

		Dan_02 (120 nm/min) (etch past sacrificial QW, PR should be thicker than etching depth) BCL3 (10sccm, 10mT, 100W, 2min), Cl2 (10sccm, 5mT, 200W)
	Solvent Bench	Preheat 1165 Stripper for 10 min, 80 C
		Sonicate on High 1165 at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry
p-DBR Litho	Solvent Bench	Sonicate on low: 3min Ace, 3min Iso, 3x 30s DI Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 1min
		Spin HMDS Program 5 (3000rpm, 30s)
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Softbake, 110oC 90s
	Contact Aligner	Expose **"4.p-DBR"**, 7.5mW/cm2, **10s**, No Filter**,** Black chuck, **Hard contact**
	PR Bench	**Post exposure bake 110C 60s**
	Develop Bench	Develop in AZ300MIF **50s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
p-DBR Dep	IBD	Calibration Sample(s) using DSP sapphire, Ellipsometer/Filmetrics, JL_FP_1i5pTa2O5… ,JL_12_FP_1i5pSiO2…
		Deposit 16 periods SiO2/Ta2O5, Co-load a DSP sapphire 1/4 wafer
	Carry 500	Measure and Model reflectance on SSP sapphire sample
	Solvent Bench	Preheat AZ NMP Stripper for 10min, 80oC
		Sonicate on Low AZ NMP at 80C for 10min. Rinse 3x 30s DI, N2 dry
	3D Microscope	Inspect, liftoff more if necessary
Intracavity contact metal and PEC cathode Litho	Solvent Bench	Spray with pipette (no sonicate) 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 1min
		Spin HMDS Program 5 (3000rpm, 30s) **(Use DSP Sapphire Corrals)**
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		Scrape off edge-bead from short edges **(don't scrape long edges)**
		Softbake, 110C 90s

	Contact Aligner	Expose **"5.INTRACAVITY METAL**", 7.5mW/cm2, **10s**, No Filter, Black chuck, **Hard contact**
	PR Bench	**Post exposure bake 110C 60s**
	Develop Bench	Develop in AZ300MIF **50s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
Intracavity Contact metal and PEC cathode Dep	Acid Bench	1:1 HCl:DI 30s, 3x 30s DI Dump&Rinse, N2 Dry
	Solvent Bench	Preheat AZ NMP Stripper for 10min, 80C
	Ebeam 3 or Ebeam 4 or Sputter 4	**Ebeam 3:** Deposit Ti/Au (300A/10,000A) **Angled chuck** **Ebeam 4:** Deposit Ti/Au (300A/10,000A) **planetary angle&rotate.** **Sputter 4:** Load samples using clips (Optional, load flip-chip substrates as well) Adjust Ti and Au gun angle to "20" Run J_Leonard Ti-Au Dep (Ar palsma clean, Ti (10nm), Au (500nm))
	Solvent Bench	Preheat AZ NMP Stripper for 10min, 80C
		Sonicate on Low AZ NMP at 80C for 10min. Rinse 3x 30s DI+Tergitol Dump, N2 dry
	3D microscope	Inspect, liftoff more if necessary
Flip-chip Substrate Only: Metal Dep	Acid Bench	**1 HCl 1 min, 3x 30s DI Dump&Rinse, N2 Dry**
	Thermal Evaporator II	Load In and Au pellets into three boats (Boat 1: Au, Boats 2,3: In)
		Use springs to hold copper mounts, kapton tape for large wafers
		Deposit 1700 nm of in followed by 200 nm of Au
Flip-Chip Bond	Scribing bench	Cleave off the areas of chip where edge bead removal occurred (scribe the backside then nick the edge of the chip)
		Label back of flip-chip substrates
	Acid Bench	Basic Pirahna clean (1:1:1 HNO3:H2O2:H2O). 80C. 5 min warm-up. Clean flip-chip substrates and samples for 10 min
	UV Ozone	20min (~6A/min)
	Finetech Flip Chip Bonder	Flip chip bond wafer to submount with In-Au Thermocompression bonding. Contact at 280C for 30s

	Or Furnace	Clamp sample to submount in graphite carrier, finger tight
		Anneal 200^{o}C 2hr
PEC Lift-off	Packaging Lab	PEC etch to remove substrate 405 nm LED Array, 3.5A (35V?), (~12 W output power, ~65 mW/cm2) 1M KOH 4 ~ 24 hour
	Microscope	Inspect, etch more if necessary
n-contact litho	Solvent Bench	Spray with pipette (no sonicate) 2min Ace, 2min Iso, 3x 30s DI+Tergitol Dump&Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110oC, let cool 1min
		Spin **LOL 2000**, 2000 rpm, 10 krpm/s, 30s (~250 nm thick)
		Softbake, 170 °C, 5min, let cool 2 min
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		edge-bead removal from short edges
		Softbake, 110oC 90s
	Contact Aligner	Expose "**6.N-CONTACT**", 7.5mW/cm2, **10s**, No Filter, Black chuck, **Hard contact**
	PR Bench	**Post exposure bake 110C 60s**
	Develop Bench	Develop in AZ300MIF **50s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
n-contact etch	RIE5	Load bare carrier wafer
		Standard O2, BCl3/SiCl4 preclean (Yonkee_01 (~10min pump down, 10min O2 clean))
		Load samples onto carrier wafer, no oil
		SLEE_05 10sec (~15nm) SiCl4 (270W)
n-contact Dep	**E-beam 3**	Load samples using clips
		Deposit Ti (40nm), Au (300nm))
	Solvent Bench	Preheat AZ NMP Stripper for 10min, 80C
		Preheat AZ NMP Stripper for 10min, 80C
		Treat in AZ NMP at 80C for 3min. Scratch where there aren't devices. Spray with pipette from the scratch. Treat in AZ NMP at 80C for 5min. Repeat Spray and AZ NMP step. Rinse 3x 30s DI, N2 dry

	3D microscope	Inspect, liftoff more if necessary
PEC Stop-etch (optional)	AFM (optional)	Measure RMS roughness in the aperture
	Packaging Lab	PEC etch to AlGaN stop-layer 365 nm LED Array, **345nm long-pass filter** 1M KOH 3min (~50nm/min) **This step is still under optimization**
	3D Microscope	Inspect
	AFM (optional)	Measure RMS roughness in the aperture
Cavity Resonance Check	Laser Testing Station	Run Spectra vs. IV program up to 70-100 kA/cm2 on each corner and middle of device
		Check cavity resonance
	Vertical	If resonance is off, model in vertical adding a Ta2O5 n-side spacer to re-align the resonance with the peak gain. **Make sure you do the vertical simulation without the n-DBR as well, since this layer will increase the cavity length**
n-DBR Litho	Solvent Bench	2min Ace, 2min Iso, 3x 30s DI Rinse, N2 dry
	PR Bench	Dehydration bake, 2min 110C, let cool 1min
		Spin **LOL 2000**, 2 krpm, 10 krpm/s, 30s (~250 nm thick)
		Edge Bead removal, Clean backside with EBR 100
		Softbake, 170 °C, 5min, let cool 2 min
		Spin **nLOF2035** Program 5 (3000rpm 30s)
		Edge Bead removal, Clean backside with EBR 100
		Softbake, 110C 90s
	Contact Aligner	Expose "**7.N-DBR**", 7.5mW/cm2, **10s**, No Filter, Black chuck, hard contact.
	PR Bench	**Post exposure bake 110oC 60s**
	Develop Bench	Develop in AZ300MIF **50s**
		2min DI rinse flowing, N2 dry
	Microscope	Inspect, develop more if necessary
	UV Ozone	20min (~6A/min)
DBR Dep	IBD	Calibration Sample(s) using DSP sapphire, Ellipsometer/Filmetrics, JL_FP_1i5pTa2O5… ,JL_12_FP_1i5pSiO2…

		Deposit 12 periods SiO2/Ta2O5 n-DBR on VCSEL and DSP sapphire 1/4 wafer
DBR Liftoff	Solvent Bench	Preheat AZ NMP Stripper for 10min, 80oC
		Treat in AZ NMP at 80C for 5min. Spray with pipette. Repeat AZ NMP and spray step. Rinse 3x 30s DI Rinse, N2 dry
	3D Microscope	Inspect, liftoff more if necessary
	Solvent Bench	no ultrasonic: 3min Ace, 3min Iso, 3x 30s DI Rinse, N2 dry
LIV Test		Congrats, you made a VCSEL!

Reference

[1] T.-Y. Seong, J. Han, H. Amano, and H. Morkoç, *III-Nitride based light emitting diodes and applications*. Dordrecht, Netherlands: Springer, 2013.

[2] C. Lee *et al.*, "Dynamic characteristics of 410 nm semipolar ($20\bar{2}\bar{1}$) III-nitride laser diodes with a modulation bandwidth of over 5 GHz," *Appl. Phys. Lett.*, vol. 109, no. 10, p. 101104, Sep. 2016.

[3] C. Lee *et al.*, "Gigabit-per-second white light-based visible light communication using near-ultraviolet laser diode and red-, green-, and blue-emitting phosphors," *Opt. Express*, vol. 25, no. 15, p. 17480, Jul. 2017.

[4] C. O. Holder *et al.*, "Nonpolar III-nitride vertical-cavity surface emitting lasers with a polarization ratio of 100% fabricated using photoelectrochemical etching," *Appl. Phys. Lett.*, vol. 105, no. 3, p. 031111, Jul. 2014.

[5] J. T. Leonard *et al.*, "Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact," *Appl. Phys. Lett.*, vol. 107, no. 9, p. 091105, Aug. 2015.

[6] J. T. Leonard *et al.*, "Nonpolar III-nitride vertical-cavity surface-emitting lasers incorporating an ion implanted aperture," *Appl. Phys. Lett.*, vol. 107, no. 1, p. 011102, Jul. 2015.

[7] S. W. Kaun, M. H. Wong, U. K. Mishra, and J. S. Speck, "Molecular beam epitaxy for high-performance Ga-face GaN electron devices," *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 074001, Jul. 2013.

[8] R. Michalzik, *VCSELs : fundamentals, technology and applications of vertical-cavity surface-emitting lasers*. Springer, 2013.

[9] T.-C. Lu, C.-C. Kao, H.-C. Kuo, G.-S. Huang, and S.-C. Wang, "CW lasing of current injection blue GaN-based vertical cavity surface emitting laser," *Appl. Phys. Lett.*, vol. 92, no. 14, p. 141102, Apr. 2008.

[10] T. Furuta *et al.*, "Room-temperature CW operation of a nitride-based vertical-cavity surface-emitting laser using thick GaInN quantum wells," *Jpn. J. Appl. Phys.*, vol. 55, no. 5S, p. 05FJ11, May 2016.

[11] H. Yu *et al.*, "Progress and prospects of GaN-based VCSEL from near UV to green emission," *Prog. Quantum Electron.*, vol. 57, pp. 1–19, Jan. 2018.

[12] T. Hamaguchi, N. Fuutagawa, S. Izumi, M. Murayama, and H. Narui, "Milliwatt-class GaN-based blue vertical-cavity surface-emitting lasers fabricated by epitaxial lateral overgrowth," *Phys. status solidi*, vol. 213, no. 5, pp. 1170–1176, May 2016.

[13] K. Ikeyama *et al.*, "Room-temperature continuous-wave operation of GaN-based vertical-cavity surface-emitting lasers with n-type conducting

AlInN/GaN distributed Bragg reflectors," *Appl. Phys. Express*, vol. 9, no. 10, p. 102101, Oct. 2016.
[14] M. Kuramoto *et al.*, "High-output-power and high-temperature operation of blue GaN-based vertical-cavity surface-emitting laser," *Appl. Phys. Express*, vol. 11, no. 11, p. 112101, Nov. 2018.
[15] L. A. Coldren, S. W. Corzine, and M. L. Mašanović, *Diode Lasers and Photonic Integrated Circuits*, 2nd ed. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2012.
[16] Bin Tian, Feitian Zhang, and Xiaobo Tan, "Design and development of an LED-based optical communication system for autonomous underwater robots," in *2013 IEEE/ASME International Conference on Advanced Intelligent Mechatronics*, 2013, pp. 1558–1563.
[17] H. Kaushal and G. Kaddoum, "Underwater Optical Wireless Communication," *IEEE Access*, vol. 4, pp. 1518–1547, 2016.
[18] T.-C. Wu, Y.-C. Chi, H.-Y. Wang, C.-T. Tsai, and G.-R. Lin, "Blue Laser Diode Enables Underwater Communication at 12.4 Gbps," *Sci. Rep.*, vol. 7, no. 1, p. 40480, Dec. 2017.
[19] D. K. Serkland *et al.*, "VCSELs for atomic sensors," 2007, vol. 6484, p. 648406.
[20] C. Lacroûte *et al.*, "Compact Yb^{+} optical atomic clock project: design principle and current status," *J. Phys. Conf. Ser.*, vol. 723, no. 1, p. 012025, Jun. 2016.
[21] C. Tamm, T. Schneider, and E. Peik, "Optical frequency standard based on a trapped $^{171}Yb^{+}$ ion," 2003, vol. 5137, p. 403.
[22] J. Carrano, "Ultraviolet light," *SPIE Newsroom*, 2003.
[23] Å . Haglund *et al.*, "Progress and challenges in electrically pumped GaN-based VCSELs," 2016, vol. 9892, p. 98920Y.
[24] E. Dupuit, A. Dandrieux, P. Kvapil, J. Ollivier, G. Dusserre, and O. Thomas, "UV spectrophotometry for monitoring toxic gases," *Analusis*, vol. 28, no. 10, pp. 966–972, Dec. 2000.
[25] C. Morryis, "Samsung Unveils The Wall, a 146-inch TV, at 2018 CES | Fortune," *Fortune*, 2018. [Online]. Available: http://fortune.com/2018/01/08/samsung-146-inch-tv-the-wall-ces-2018/. [Accessed: 09-Dec-2018].
[26] D. Bohn, "Exclusive: Intel's new Vaunt smart glasses actually look good - The Verge," *The Verge*, 2018. [Online]. Available: https://www.theverge.com/2018/2/5/16966530/intel-vaunt-smart-glasses-announced-ar-video. [Accessed: 09-Dec-2018].
[27] C. A. Forman *et al.*, "Continuous-wave operation of *m* -plane GaN-based vertical-cavity surface-emitting lasers with a tunnel junction intracavity contact," *Appl. Phys. Lett.*, vol. 112, no. 11, p. 111106, Mar. 2018.

[28] S. Lee *et al.*, “GaN-based vertical-cavity surface-emitting lasers with tunnel junction contacts grown by metal-organic chemical vapor deposition,” *Appl. Phys. Express*, vol. 11, no. 6, p. 062703, Jun. 2018.
[29] S. Izumi, N. Fuutagawa, T. Hamaguchi, M. Murayama, M. Kuramoto, and H. Narui, “Room-temperature continuous-wave operation of GaN-based vertical-cavity surface-emitting lasers fabricated using epitaxial lateral overgrowth,” *Appl. Phys. Express*, vol. 8, no. 6, p. 062702, Jun. 2015.
[30] T. Hamaguchi *et al.*, “Lateral optical confinement of GaN-based VCSEL using an atomically smooth monolithic curved mirror,” *Sci. Rep.*, vol. 8, no. 1, p. 10350, Dec. 2018.
[31] C. Holder, J. S. Speck, S. P. DenBaars, S. Nakamura, and D. Feezell, “Demonstration of Nonpolar GaN-Based Vertical-Cavity Surface-Emitting Lasers,” *Appl. Phys. Express*, vol. 5, no. 9, p. 092104, Sep. 2012.
[32] T. Takeuchi, S. Kamiyama, M. Iwaya, and I. Akasaki, “GaN-based vertical-cavity surface-emitting lasers with AlInN/GaN distributed Bragg reflectors,” *Reports Prog. Phys.*, vol. 82, no. 1, p. 012502, Jan. 2019.
[33] M. Kuramoto *et al.*, “Enhancement of slope efficiency and output power in GaN-based vertical-cavity surface-emitting lasers with a SiO_2 -buried lateral index guide,” *Appl. Phys. Lett.*, vol. 112, no. 11, p. 111104, Mar. 2018.
[34] S. Mishkat-Ul-Masabih, T. S. Luk, A. Rishinaramangalam, M. Monavarian, M. Nami, and D. Feezell, “Nanoporous distributed Bragg reflectors on free-standing nonpolar *m* -plane GaN,” *Appl. Phys. Lett.*, vol. 112, no. 4, p. 041109, Jan. 2018.
[35] R. Sharma, E. D. Haberer, C. Meier, E. L. Hu, and S. Nakamura, “Vertically oriented GaN-based air-gap distributed Bragg reflector structure fabricated using band-gap-selective photoelectrochemical etching,” *Appl. Phys. Lett.*, vol. 87, no. 5, p. 051107, Aug. 2005.
[36] Y. Zhang *et al.*, “A conductivity-based selective etching for next generation GaN devices,” *Phys. status solidi*, vol. 247, no. 7, pp. 1713–1716, Jun. 2010.
[37] G.-Y. Shiu *et al.*, “InGaN Light-Emitting Diodes with an Embedded Nanoporous GaN Distributed Bragg Reflectors,” *Sci. Rep.*, vol. 6, no. 1, p. 29138, Sep. 2016.
[38] B.-C. Shieh *et al.*, “InGaN light-emitting diodes with embedded nanoporous GaN distributed Bragg reflectors,” *Appl. Phys. Express*, vol. 8, no. 8, p. 082101, Aug. 2015.
[39] S.-M. Lee, S.-H. Gong, J.-H. Kang, M. Ebaid, S.-W. Ryu, and Y.-H. Cho, “Optically pumped GaN vertical cavity surface emitting laser with high index-contrast nanoporous distributed Bragg reflector,” *Opt. Express*, vol. 23, no. 9, p. 11023, May 2015.

[40] T. Hamaguchi *et al.*, “Lateral carrier confinement of GaN-based vertical-cavity surface-emitting diodes using boron ion implantation,” *Jpn. J. Appl. Phys.*, vol. 55, no. 12, p. 122101, Dec. 2016.
[41] C. A. Forman *et al.*, “Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers,” in *Gallium Nitride Materials and Devices XIII*, 2018, vol. 10532, p. 83.
[42] S. Lee *et al.*, “Smooth and selective photo-electrochemical etching of heavily doped GaN:Si using a mode-locked 355 nm microchip laser,” *Appl. Phys. Express*, vol. 10, no. 1, p. 011001, Jan. 2017.
[43] J. T. Leonard *et al.*, “Nonpolar III-nitride vertical-cavity surface-emitting laser with a photoelectrochemically etched air-gap aperture,” *Appl. Phys. Lett.*, vol. 108, no. 3, p. 031111, Jan. 2016.
[44] M. Ortsiefer, R. Shau, G. Böhm, F. Köhler, and M.-C. Amann, “Low-threshold index-guided 1.5 μm long-wavelength vertical-cavity surface-emitting laser with high efficiency,” *Appl. Phys. Lett.*, vol. 76, no. 16, p. 2179, Apr. 2000.
[45] J. T. Leonard *et al.*, “Smooth e-beam-deposited tin-doped indium oxide for III-nitride vertical-cavity surface-emitting laser intracavity contacts,” *J. Appl. Phys.*, vol. 118, no. 14, p. 145304, Oct. 2015.
[46] B. P. Yonkee *et al.*, “Demonstration of a III-nitride edge-emitting laser diode utilizing a GaN tunnel junction contact,” *Opt. Express*, vol. 24, no. 7, p. 7816, Apr. 2016.
[47] E. C. Young *et al.*, “Hybrid tunnel junction contacts to III–nitride light-emitting diodes,” *Appl. Phys. Express*, vol. 9, no. 2, p. 022102, Feb. 2016.
[48] A. J. Mughal, B. Carberry, J. S. Speck, S. Nakamura, and S. P. DenBaars, “Structural and Optical Properties of Group III Doped Hydrothermal ZnO Thin Films,” *J. Electron. Mater.*, vol. 46, no. 3, pp. 1821–1825, Mar. 2017.
[49] C. A. Forman *et al.*, “Continuous-wave operation of *m* -plane GaN-based vertical-cavity surface-emitting lasers with a tunnel junction intracavity contact,” *Appl. Phys. Lett.*, vol. 112, no. 11, p. 111106, Mar. 2018.
[50] E. C. Young *et al.*, “Hybrid tunnel junction contacts to III–nitride light-emitting diodes,” *Appl. Phys. Express*, vol. 9, no. 2, p. 022102, Feb. 2016.
[51] S. Pimputkar, S. Suihkonen, M. Imade, Y. Mori, J. S. Speck, and S. Nakamura, “Free electron concentration dependent sub-bandgap optical absorption characterization of bulk GaN crystals,” *J. Cryst. Growth*, vol. 432, pp. 49–53, Dec. 2015.
[52] L. T. Romano, C. G. Van de Walle, J. W. A. III, W. Götz, and R. S. Kern, “Effect of Si doping on strain, cracking, and microstructure in GaN thin films grown by metalorganic chemical vapor deposition,” *J. Appl. Phys.*, vol. 87, no. 11, p. 7745, May 2000.
[53] H. Xing *et al.*, “Memory Effect and Redistribution of Mg into Sequentially

Regrown GaN Layer by Metalorganic Chemical Vapor Deposition," *Jpn. J. Appl. Phys.*, vol. 42, no. Part 1, No. 1, pp. 50–53, Jan. 2003.
[54] M. Hansen, L. F. Chen, S. H. Lim, S. P. DenBaars, and J. S. Speck, "Mg-rich precipitates in the *p* -type doping of InGaN-based laser diodes," *Appl. Phys. Lett.*, vol. 80, no. 14, pp. 2469–2471, Apr. 2002.
[55] K. . O'Donnell *et al.*, "The dependence of the optical energies on InGaN composition," *Mater. Sci. Eng. B*, vol. 82, no. 1–3, pp. 194–196, May 2001.
[56] J. Neugebauer and C. G. Van de Walle, "Role of hydrogen in doping of GaN," *Appl. Phys. Lett.*, vol. 68, no. 13, p. 1829, Jun. 1998.
[57] D. Hwang, A. J. Mughal, M. S. Wong, A. I. Alhassan, S. Nakamura, and S. P. DenBaars, "Micro-light-emitting diodes with III–nitride tunnel junction contacts grown by metalorganic chemical vapor deposition," *Appl. Phys. Express*, vol. 11, no. 1, p. 012102, Jan. 2018.
[58] Y. Kuwano *et al.*, "Lateral Hydrogen Diffusion at p-GaN Layers in Nitride-Based Light Emitting Diodes with Tunnel Junctions," *Jpn. J. Appl. Phys.*, vol. 52, no. 8S, p. 08JK12, Aug. 2013.
[59] T. Hamaguchi, N. Fuutagawa, S. Izumi, M. Murayama, and H. Narui, "Milliwatt-class GaN-based blue vertical-cavity surface-emitting lasers fabricated by epitaxial lateral overgrowth," *Phys. status solidi*, vol. 213, no. 5, pp. 1170–1176, May 2016.
[60] G. C. Chi, F. W. Ostermayer, K. D. Cummings, and L. R. Harriott, "Ion beam damage-induced masking for photoelectrochemical etching of III-V semiconductors," *J. Appl. Phys.*, vol. 60, no. 11, pp. 4012–4014, Dec. 1986.
[61] A. T. Ping, Q. Chen, J. W. Yang, M. A. Khan, and I. Adesida, "The effects of reactive ion etching-induced damage on the characteristics of ohmic contacts to n-Type GaN," *J. Electron. Mater.*, vol. 27, no. 4, pp. 261–265, Apr. 1998.
[62] R. M. Farrell *et al.*, "Determination of internal parameters for AlGaN-cladding-free *m* -plane InGaN/GaN laser diodes," *Appl. Phys. Lett.*, vol. 99, no. 17, p. 171115, Oct. 2011.
[63] "Encyclopedia of Laser Physics and Technology - modes, waveguide, propagation modes, optical fiber, resonator, resonator, field distribution." [Online]. Available: https://www.rp-photonics.com/modes.html. [Accessed: 22-Dec-2018].
[64] N. Watanabe, T. Kimoto, and J. Suda, "The temperature dependence of the refractive indices of GaN and AlN from room temperature up to 515 °C," *J. Appl. Phys.*, vol. 104, no. 10, p. 106101, Nov. 2008.