Title
Materials Synthesis and Characterization for Micro-supercapacitor Applications

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Publication Date
2013

Peer reviewed|Thesis/dissertation

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By

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A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Chemical and Biomolecular Engineering

in the

Graduate Division

of the

University of California, Berkeley

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Fall 2013

Abstract

Materials Synthesis and Characterization for Micro-supercapacitor Applications

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Supercapacitors represent a critical energy storage device technology for applications which require higher power density and/or cycle lifetime than existing battery technologies. Micro-scale supercapacitors, in particular, can enable novel applications in autonomous, wireless microsensors and microelectronics. If these micro-supercapacitors can be fabricated in a planar, on-chip geometry, the energy storage and the devices to be powered can be integrated on a single chip, improving scalability and reducing cost. The primary components of a supercapacitor are the electrodes and electrolyte. The properties of the electrode and electrolyte materials have a significant effect on device performance, and thus, there is significant opportunity for engineering materials to improve the energy density, power density, cycle lifetime, cost, safety, manufacturability, and harsh environment performance of micro-supercapacitors. Furthermore, these properties could be intelligently tailored for specific applications.

This manuscript provides some background on the principles underlying supercapacitor materials selection and testing, and presents several approaches to engineer these materials. Electrode materials which are investigated include photoresist derived porous carbon, vertically aligned carbon nanotubes, and 3D templated graphene. Electrolytes which are explored include various aqueous salts (and their impact on device cycle lifetime performance) as well as ionic liquid based gels (or ionogels). Furthermore, efforts to fabricate flexible micro-supercapacitors are discussed.

For on-chip energy storage involving high temperature operation, yttria-stabilized zirconia is investigated as the electrolyte. Silicon carbide (SiC)-based material for the electrode and its metal contact stability are also investigated, as the stability of these contacts during operation is an important consideration for the performance of high temperature micro-supercapacitors. Epitaxial graphene growth on SiC thin films is presented as one approach to stabilizing metal-to-SiC contacts.

Contents

1 Introduction

Ever since the widespread adoption of electricity in the 19th and 20th centuries, interest in energy storage technologies has grown in order to enable a variety of applications ranging from electrical grid level storage to powering vehicles and mobile consumer devices. A variety of energy storage mechanisms have been developed, each suited to particular applications based on the specific technical requirements. For example, for large scale electrical grid storage, large amounts of energy needs to be stored and discharged over many cycles and hence large-scale pumped hydroelectricity is more commonly used than batteries. However, batteries would be a more likely storage method of choice for powering consumer electronics and vehicles. These examples demonstrate that each energy storage technique has certain advantages and disadvantages, and that these factors impact the applications that would be relevant for a given energy storage type. In Figure 1.1, which is known as a Ragone plot, the mass energy and power density for a few different energy storage types are plotted. The energy density is a measure of how much electrical energy can be stored per unit mass, volume, or area, while the power density gives how quickly the energy can be charged and discharged. All other things being equal, an ideal energy storage device would have extremely high energy and power density. However, due to real world limitations, each technology fills its own niche in the energy landscape and is hence optimal for its own set of applications.

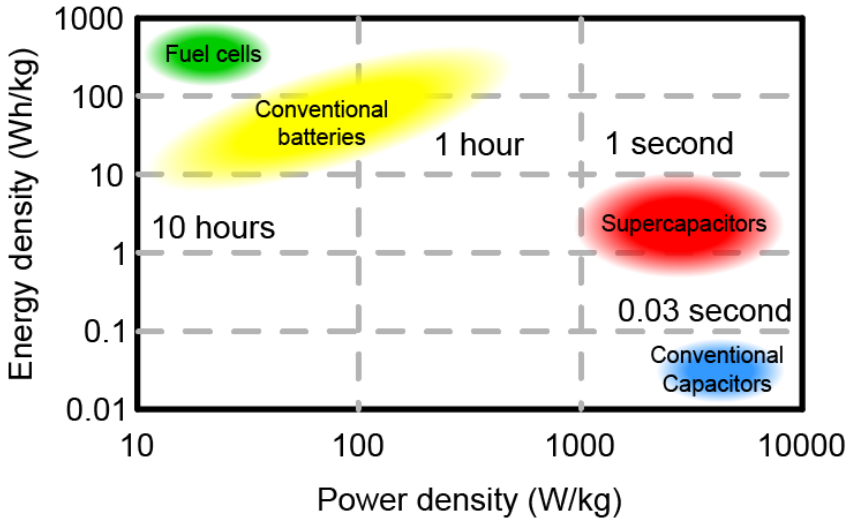

Figure 1.1 Ragone plot showing energy density vs. power density for various devices. Adapted from Stan Zurek, used under a Creative Commons Attribution-ShareAlike license.

1.1 Supercapacitors and their properties

Supercapacitors, also known as electrical double layer capacitors (EDLCs) or ultracapacitors, occupy a niche in the Ragone plot intermediate to batteries and capacitors. In simplistic terms, this means that supercapacitors store more energy than capacitors, but discharge that energy more slowly, and that supercapacitors store less energy than batteries, but discharge that energy more rapidly. This difference in performance stems from the fundamental energy storage mechanism of each technology, illustrated in Figure 1.2.

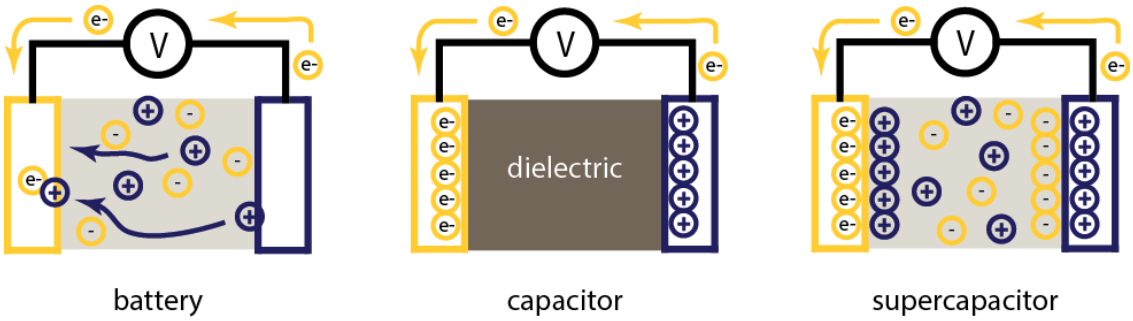

Figure 1.2 Illustration of charge storage mechanism for batteries, capacitors, and supercapacitors.

Capacitors are composed of two electrodes which are separated by an intervening dielectric layer. When a potential difference is applied across the two electrodes, equal and opposite charge builds up on the two electrodes. When a current path is introduced between the two electrodes in the form of a load resistance (the device to be powered), the charge can then dissipate and the resulting current can be utilized. Batteries, in contrast to capacitors, have an ionically conducting electrolyte between the two electrodes. Energy is stored through reversible chemical reactions in each electrode. During charging, oxidation occurs at one electrode and reduction at the other. Upon discharge, the reactions are reversed. Capacitors are said to store energy electrostatically, that is, using charge storage without chemical reaction, while batteries store energy chemically, relying on chemical conversions at the two electrodes. Supercapacitors utilize some principles of both capacitors and batteries. Like batteries, supercapacitors are composed of two electrodes and an ionically conducting electrolyte. However, unlike batteries, instead of storing charge through electrochemical reactions in the electrode bulk, all of the charge is stored at the interface of electrode and electrolyte. Upon charging, mobile ions in the electrolyte migrate toward the electrode surface and an area of high charge density is formed near the interface. The interface can therefore be thought of as similar to a capacitor, with equal and opposite charges (electrons or holes in the electrode and charged ions in the electrolyte) separated by a small distance. Typically, supercapacitor electrodes are designed to have an extremely high specific surface area, leading to large interfacial areas for charging. The details of this charge storage mechanism will be discussed in Chapter 2.

This difference in operation mechanism yields very different operational properties, some of which are revealed in the Ragone plot. The high energy density of batteries stems from the large potential energy stored in electrochemical redox reactions, while the high power density of capacitors stems from the purely electrostatic charge storage, which can be charged and discharged quickly. Supercapacitors, which rely only on interfacial charging, fall in the middle of this spectrum: they possess higher energy density than capacitors due to their large specific surface area and higher power density than batteries due to their nonreliance on kinetically and transport limited electrode reactions. Other practical considerations besides energy and power density are cycle lifetime (resistance to performance degradation from repeated charge/discharge cycles), self-discharge (loss of charge when not in use), safety, and cost. Batteries are currently limited to thousands of cycles before significant performance degradation due to the side reactions and phase changes inherent in electrochemical energy storage. In supercapacitors, since the charging occurs at the electrode/electrolyte interface, minimal volumetric or phase change occurs. Careful selection of materials can also minimize unwanted side reactions. Hence, supercapacitors can achieve extremely long cycle lifetimes exceeding 10^4 to 10^6 cycles [1, 2].

While ideal double layer supercapacitors should not experience self-discharge, in reality, various factors can contribute to charge loss over time, and this is an area of active study. Batteries also experience this phenomenon due to a thermodynamic driving force, but typically exhibit a lower rate of self-discharge than most supercapacitors [1]. Regarding safety and cost, much depends on the choice of materials. While the carbon based electrodes used in supercapacitors are typically less toxic and cheaper than the electrodes required for battery chemistries, the selection of electrolyte can vary in both cost and safety and will be further discussed in Chapter 2.

1.2 Potential applications for supercapacitors

The unique properties of supercapacitors make them preferable for a variety of applications which require high power density and/or frequent cycling. Macroscale supercapacitors have been proposed for a variety of applications including uninterruptable power supplies, electric vehicles (for operation and/or energy recovery), and power levelers for electronics. All of these applications utilize the fast charge/discharge rate of supercapacitors and favorable cycle lifetime relative to batteries. In fact, in Germany, some mass transit vehicles have been outfitted with supercapacitors rather than batteries in order to harvest braking energy [3]. Since supercapacitors have a higher charging rate capability than batteries, this use of the former can yield increased vehicle energy efficiency. In Shanghai, China, some buses utilize supercapacitors for vehicle propulsion, recharging a bank of supercapacitors from overhead lines at each bus stop [4]. Since supercapacitors can charge quickly, bringing the energy storage to full capacity takes less time than loading and unloading passengers. These examples demonstrate only a few of the possible applications of macroscale supercapacitors.

Microscale supercapacitors have been proposed as a replacement or complement to micro-batteries and energy harvesters for applications including biomedical implants, microsensor arrays, and portable electronics [5, 6]. For all of these applications, autonomous operation is desired; that is, extensive wiring or frequent battery changes would be undesirable. These planar, on-chip supercapacitors can be integrated with the microelectromechanical systems (MEMS) or microelectronics device to be powered, thus maintaining small form factors and potentially reducing cost. Furthermore, if energy harvesting components (such as photovoltaics, vibrational energy harvesters, or thermoelectrics) can also be integrated with these devices, fully autonomous wireless operation could be enabled.

1.3 Outline of this work

This work will discuss the current theory regarding supercapacitor operation and performance testing (Chapter 2) and then discuss in detail three candidate carbon based materials for micro-supercapacitors. First, Chapter 3 will describe the fabrication of photoresist-derived carbon electrodes. Chapter 4 will report the fabrication of a flexible micro-supercapacitor device from the photoresist-derived carbon, and Chapter 5 will describe a procedure to electrochemically activate the material to increase energy density and probe the lifetime cycling of the activated material. Vertically aligned carbon nanotube arrays are investigated for flexible applications in Chapter 6, and 3D templated thin graphite electrodes are discussed in Chapter 7. Next, harsh environment applications will be discussed, centering on high temperature supercapacitor materials such as yttria-stabilized zirconia (Chapter 8) and metal contact materials for SiC-based microsystems (Chapter 9). Finally, Chapter 10 will summarize the work and offer perspectives on possible future research directions.

2 Supercapacitor theory

Unlike batteries, which store energy through electrochemical reactions in the electrode bulk, supercapacitors store energy primarily at the electrode/electrolyte interface. This charge storage takes place via two separate phenomena: electrostatic double-layer charging and faradaic charge transfer, also known as pseudocapacitance.

2.1 Double-layer capacitance

Double-layer charging occurs when a potential is applied across two electrodes connected by an ionically conducting electrolyte. Charged ions migrate to the electrode/electrolyte interfacial region, with positive ions migrating to one electrode, and negative ions to the other. For ideally polarizable electrodes, where no charge transfer between the electrode and electrolyte occurs, this phenomenon creates an interfacial region at each electrode, where positive charges in the electrolyte balance negative charges in one electrodes and vice versa for the other electrode. The amount of charge that builds up at the electrode, Δq, for a potential difference, ΔV, is equal to the capacitance,

$$C = \frac{\Delta q}{\Delta V} \tag{2.1}$$

This buildup of opposite charges resembles a dielectric capacitor, whose capacitance is given by

$$C = \frac{A\varepsilon\varepsilon_0}{d} \tag{2.2}$$

where d is the separation between parallel plates of area A, and ε and ε_0 are the relative permittivity of the dielectric and the permittivity of free space respectively. The specific areal capacitance of a parallel plate capacitor is quite small; for a micrometer scale separation and a relative permittivity of 100 (water has a $\varepsilon \sim 80$), the capacitance is on the order of 100 nF per cm^2. In contrast, since the distance, d, separating the charges in a capacitive double-layer is quite small, double-layer capacitances of 15-50 $\mu F/cm^2$ can be achieved on carbon electrodes [7, 8], an improvement of over 2 orders of magnitude. Since these electrodes can also be highly porous or textured, total surface area can be very high, giving very large volumetric and gravimetric capacitances.

Several physical models have been proposed to describe the region near these interfaces, beginning with the Helmholtz double-layer model, proposed in 1853 [9] and illustrated in Figure 2.1a. This model proposes a simple capacitor-like system, with ions from the electrolyte adsorbed onto the oppositely charged electrode surface. However, this oversimplified model does not account for thermal fluctuations of the adsorbed ions, which was added to the model by Gouy in 1910 [10]. This new model proposed a more diffuse layer of charges, including both anions and cations, and is illustrated in Figure 2.1b. A gradient of charge is still apparent, with a larger concentration of positive ions near the negatively charged surface, but the double-layer is not as concentrated as in the Helmholtz model. In 1913, Chapman derived a rigorous mathematical model of the Gouy model, combining the Boltzmann energy distribution and the Poisson equation for charge distribution [11]. Unfortunately, the Guoy-Chapman model did not

accurately predict experimental results and a further refinement was added by Stern in 1924 [12]. The Stern model combined the Helmholtz model of adsorbed charges and the Guoy-Chapman model of a diffuse layer (Figure 2.1c) and proposed relating the double-layer capacitance, C_{DL} to the combination of these capacitive contributions, C_H and C_{diff}, through Eq. 2.3,

$$\frac{1}{C_{DL}} = \frac{1}{C_H} + \frac{1}{C_{diff}} \qquad 2.3$$

which combines these two contributions in series. In addition to this equivalent circuit treatment, Stern also recognized the ions as having a finite size, rather than being point charges as in the Guoy-Chapman model. This size, which can be defined by the solvation shell size, gives a minimum electrode-charge distance, which more accurately represents reality. Finally, in 1947, Grahame performed experimental work on determining the double-layer capacitance for a mercury electrode and distinguished an inner Helmholtz layer and an outer Helmholtz layer as well as a diffuse ion region (Figure 2.1d) [13]. Due to the relatively large size of most electrolyte anions relative to cations, cations are more likely to have a solvation layer that prevents them from approaching the electrode as closely as unsolvated anions. Adsorbed ions have a much smaller distance to the electrode (and are thus said to form the "inner" Helmholtz layer) than solvated ions (which form the "outer" Helmholtz layer). Thus, the double-layer capacitance tends to be higher for anions at a positively charged electrode compared to solvated cations at a negatively charged electrode, and this difference depends highly on the specific cation, anion, and solvent used in the electrolyte. The specifics of the diffuse layer will also be dependent on the electrode geometry, as highly porous electrodes, which are common in supercapacitor applications, can lead to more complex double-layer formation from confinement effects [14]. Further refinements on the Grahame model have been developed more recently, particularly in relation to these effects of confinement on double-layer formation in porous media [15, 16].

Since porous electrodes are frequently used in supercapacitors to maximize the

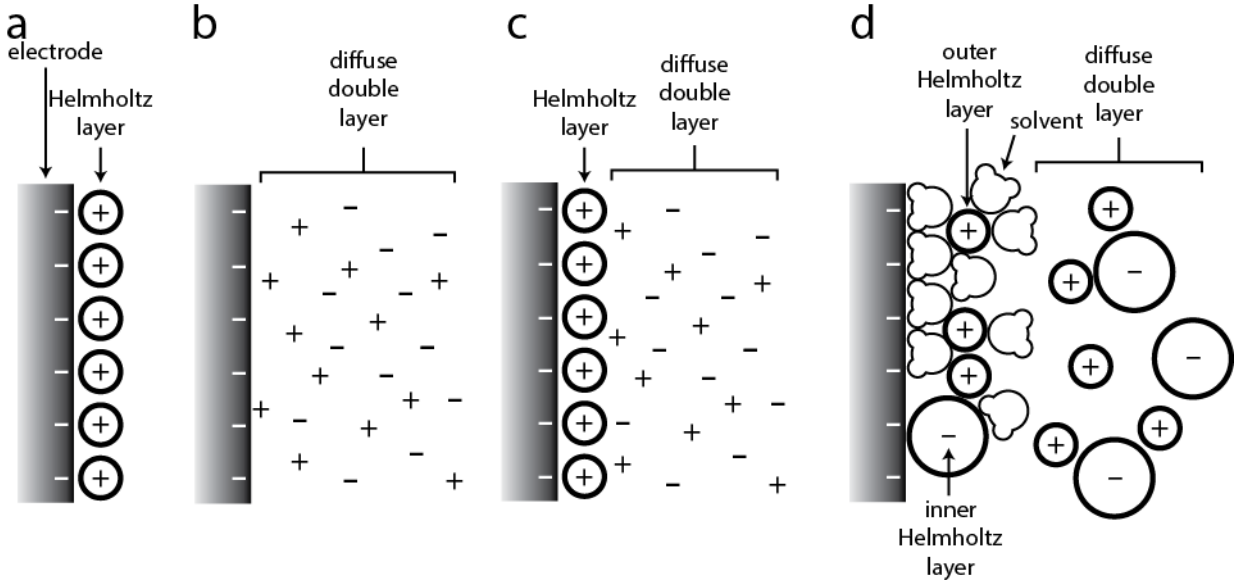

Figure 2.1 Various physical models of the electrode/electrolyte interface in a supercapacitor. a) Helmholtz model, b) Guoy-Chapman model, c) Stern model, d) Grahame model (solvent molecules not all illustrated for clarity).

electrode/electrolyte interfacial area, understanding of double-layer formation in these pores is essential to maximizing device performance. Recent experimental and theoretical work shows that when pore size is reduced to below the radius of a solvated ion (on the order of 1 nm), ions can adsorb onto electrode surfaces directly, without a solvation layer, leading to increased overall capacitance [14, 15, 16, 17]. However, ionic transport in these pores will necessarily be limited, and the resistance to movement of ions can results in rate limitations [18]. Thus, the increased capacitance yielded by ion confinement in pores may lead to trade-offs with power performance.

2.2 Pseudocapacitance

While double-layer formation stores charge electrostatically, pseudocapacitance stores charge through redox reactions at the electrode surface. Whereas in ideal double-layer capacitors, no charge transfer occurs across the electrode/electrolyte interface, pseudocapacitance does involve such charge transfer. For example, RuO_2 electrodes have been shown to store significant amounts of charge through numerous electron-proton transfer processes [1, 8]. Reactions such as

$$\mathrm{Ru}^{4+} + e^- \rightarrow \mathrm{Ru}^{3+} \quad (2.4)$$

$$\mathrm{O}^{2-} + \mathrm{H}^+ \rightarrow \mathrm{OH}^- \quad (2.5)$$

and others have been proposed to illustrate the charge storage mechanism. As evident from Eq. 2.4, electrons are transferred in this reaction; these electrons are supplied by the external circuit (which is connected to the opposite electrode) during charging, and the current from the reverse reaction can be used to perform electrical work. This reversible charge storage through redox reactions is also termed "Faradaic," in contrast to the "non-Faradaic" processes that drive double-layer charging.

For carbon based electrode materials, charge storage is primarily non-Faradaic, but overall energy storage can be augmented through pseudocapacitance by three primary methods [1, 7, 18]:

1) introduction of reactive surface functionalities (typically oxygen or nitrogen)

2) deposition of electroactive polymers such as polyaniline or polypyrrole

3) deposition of electroactive transition metal oxides such as RuO_2, MnO_2, etc.

These methods can result in extremely high increases in overall capacitance. For example, the deposition of polyaniline on carbon fibers has been shown to increase the gravimetric capacitance from 30 F/g to 150 F/g [19]. However, since these pseudocapacitive modifications use electrochemical charge storage rather than purely electrostatic (as in pure double-layer capacitors), these modifications can be detrimental to cycle lifetime if the relevant reactions are not fully reversible [18, 1, 20]. Therefore, using pseudocapacitance to augment overall energy storage can be a trade-off between increased energy density and decreased cycle lifetime. A second performance trade-off can be the achieved power density, as reaction kinetics can limit the rate at which pseudocapacitive energy can be stored and discharged.

2.3 Supercapacitor characterization

Numerous techniques can be used to characterize the electrical performance of supercapacitor materials and devices. Some supercapacitor properties which are most commonly probed are the

capacitance, the energy and power densities, the equivalent series resistance (ESR), and the lifetime cycling performance. Each technique that will be presented in this section can be used to obtain one or more of these properties.

2.3.1 Two vs. three electrode measurements

Before a detailed discussion of the electrochemical characterization techniques, a distinction should be made between two and three electrode measurements. As illustrated in Figure 2.2, two electrode measurements involve a full device measurement, with two (typically) symmetric electrodes. On the other hand, in a three electrode setup, the material to be characterized is measured against counter and reference electrodes. The counter electrode is typically an inert material, such as Pt, which is used to supply the necessary current during measurement. The reference electrode is composed of a material with a well-known redox potential, e.g. the saturated calomel electrode, which is composed of the Hg/Hg_2Cl_2 redox pair, or the Ag/AgCl electrode. This reference electrode is used to accurately measure the potential at the working electrode relative to a known reference. The two electrode system is typically used to characterize fully fabricated devices, while the three electrode system is advantageous for examining the fundamental electrochemical properties of the electrode material system. An additional difference between the two measurements is that specific capacitance values (in units of F/g, F/cm^3, or F/cm^2) obtained from the two electrode system will typically be on the order of 4 times smaller than for the three electrode, half-cell system. This discrepancy arises because the two electrode system involves double layer charging at both electrodes, which can be considered two capacitors in series; whereas, the half cell only presents one double layer. This accounts for a factor of 2. The second factor of 2 comes from the area of the electrodes. Typically, for micro-supercapacitors, the capacitance is normalized by dividing by the projected area of the electrode(s) to obtain a specific capacitance normalized by area; thus, for the two electrode measurement, the projected area of symmetric electrodes is twice as large as the area of a single electrode. Therefore, the specific capacitance derived from the two electrode system can be thought of as the device capacitance, C_{device}, and the capacitance derived from the three electrode system as the material capacitance, C_{material}. The two can be related by the following

$$C_{\text{material}} = 4C_{\text{device}} \tag{2.6}$$

This equation only applies for symmetric electrodes where the capacitance is normalized by the projected area of the electrodes. Some reports of C_{device} normalize by the area of the full device including the interelectrode gap [21, 22, 23], rather than by the area of the electrodes only, and the multiplicative factor to determine C_{material} must be increased based on the geometry of the system.

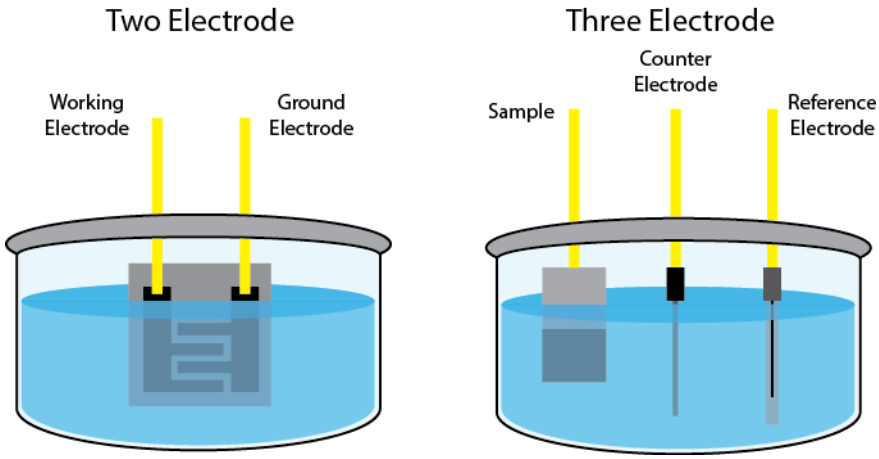

Figure 2.2 Schematic illustration of two and three electrode measurements for on-chip supercapacitor materials.

2.3.2 Cyclic voltammetry

Cyclic voltammetry is a technique where the potential at the working electrode is swept back and forth across a given potential window at a constant rate. The resulting current is measured and plotted against the potential. A sample illustration of the voltage plotted against time is shown in Figure 2.3a. For an ideal supercapacitor, the capacitance is constant regardless of scan rate and can be calculated via Eq. 2.7,

$$C = \frac{I}{s} \tag{2.7}$$

where I is the measured current and s is the applied potential scan rate. For such an ideal capacitor, the resulting current is plotted in Figure 2.3b,c. During the positive voltage sweep, the current should be a positive constant, and during the negative sweep, the negative of this constant. CV plots are typically shown as in Figure 2.3c, with the current plotted against the potential. For an ideal supercapacitor, which follows Eq. 2.7, the CV shape will be a rectangle which is symmetric about the zero-current axis.

However, in reality, supercapacitors do not typically show such ideal behavior, and if they do, it is under idealized conditions such as extremely low scan rates. Various non-idealities arise under more realistic scenarios; for example, at high scan rates, CV plots appear as in Figure 2.4a, with

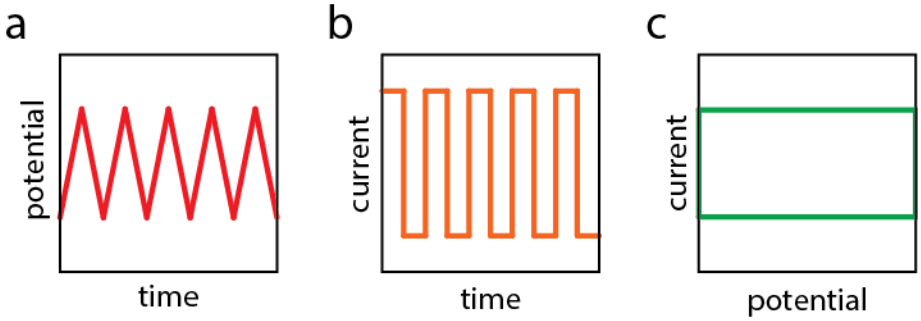

Figure 2.3 a) Cyclic voltammetry potential sweeps plotted vs. time, b) the resulting measured current of an ideal supercapacitor plotted vs. time, c) the CV curve, showing the current plotted vs. potential.

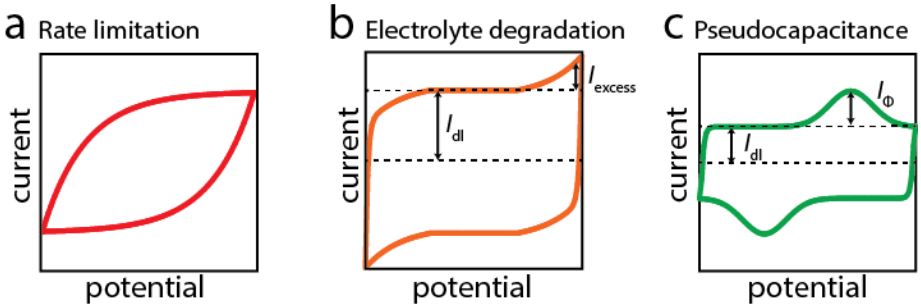

Figure 2.4 Sample supercapacitor CV nonidealities: a) sweep rate limitations, b) potential window that exceeds electrolyte stability window, c) pseudocapacitive charge storage

a characteristic leaf-like shape. For all supercapacitors, sufficiently high scan rates lead to "rounding-off" of the CV corners. This behavior arises from rate limiting phenomenon such as electrical transport limitations in the electrode or from ionic transport limitations in the electrolyte. At fast enough scan rates, the interfacial double layer does not have sufficient time to form due to these transport limitations.

A second nonideality seen in all supercapacitor devices is electrolyte degradation. All electrolytes have a limited voltage stability window which, if exceeded, leads to faradaic reactions of the electrolyte. For example, aqueous electrolytes have a maximum potential window of ~ 1 V. At excessively high or low potentials, water can be oxidized or reduced to form oxygen and hydrogen, respectively. These reactions, which require charge transfer across the electrode/electrolyte interface, lead to increases in current above that of the double-layer charging current. This current, labeled in Figure 2.4b as I_{excess}, contributes to electrolyte reactions and not to charge storage, and should not be included when calculating the capacitance using Eq. 2.7. Furthermore, this electrolyte degradation can ultimately lead to reduced performance during lifetime cycling.

Unlike current arising from electrolyte degradation, pseudocapacitive current does contribute to the energy storage capabilities of a device. Reversible faradaic reactions at the electrode surface, as described in Chapter 2.2, can lead to capacitive currents which augment the capacitance from double-layer charging. This additional capacitive current is labeled as I_{Φ} in Figure 2.4c, which shows a sample CV plot for a pseudocapacitive system.

When calculating the capacitance from CV data, Eq. 2.7 may be applied in various ways, each of which may give results at variance with the others. A few possible methods are listed in

Table 2.1. Since each calculation can yield different results, the calculation method used should be clearly stated when reporting capacitance data.

Table 2.1 Methods for calculating capacitance from CV results

Capacitance calculation method	Equation		Advantages/disadvantages
Average current	$C = \frac{I_{+,\text{avg}} - I_{-,\text{avg}}}{2s}$	2.8	Includes charging and discharging current, but may obtain spurious results from electrolyte degradation
Average discharge current	$C = -\frac{I_{-,\text{avg}}}{s}$	2.9	Discharge current may be more relevant for practical applications; also may obtain spurious results from electrolyte degradation
Midpoint current	$C = \frac{I_{+,V=V_{\text{mid}}} - I_{-,V=V_{\text{mid}}}}{2s}$	2.10	Excludes electrolyte degradation, but does not account for pseudocapacitive reactions that do not occur at potential window midpoint.

2.3.3 Galvanostatic charge/discharge

While CV can be used to calculate the capacitance of an electrode material or device, galvanostatic charge/discharge tests are often preferable for this purpose [24]. This technique involves applying a constant charging current until a maximum potential is reached, followed by application of an equal magnitude discharge current to a minimum potential. The potential is monitored as a function of time. Since a constant current is used, rather than a constant voltage sweep rate as in CV, galvanostatic charge/discharge tests may more accurately reflect real world performance. Some typical galvanostatic charge/discharge plots are shown in Figure 2.5. For an ideal supercapacitor, the charge and discharge plots should be symmetrical and should each display a constant slope throughout (Figure 2.5a). The capacitance can be easily calculated via Eq. 2.11

$$C = \frac{I}{\Delta V/\Delta t} \tag{2.11}$$

where I is the applied current magnitude and $\Delta V/\Delta t$ is the slope of the discharge curve. Comparison of Eq. 2.11 with Eq. 2.7 reveals the similarity between capacitance calculation for CV and galvanostatic charge/discharge. The only difference is that the denominator is held constant in the former, while the numerator is held constant in the latter.

Real world supercapacitors do not always yield such linear plots under all conditions, and nonlinearity can be evidence of various nonidealities in the supercapacitor operation. Figure 2.5b shows one such nonideality, an exceeding of the electrolyte stability window. Decreases in the slope of the charge or discharge curve typically indicate charge transfer across the electrode/electrolyte interface. This charge transfer can arise from reactions in the electrode, the electrolyte, or both. When the reactions occur in the electrolyte, this leads to electrolyte degradation over time, and indicates that the potential window should be reduced to within the

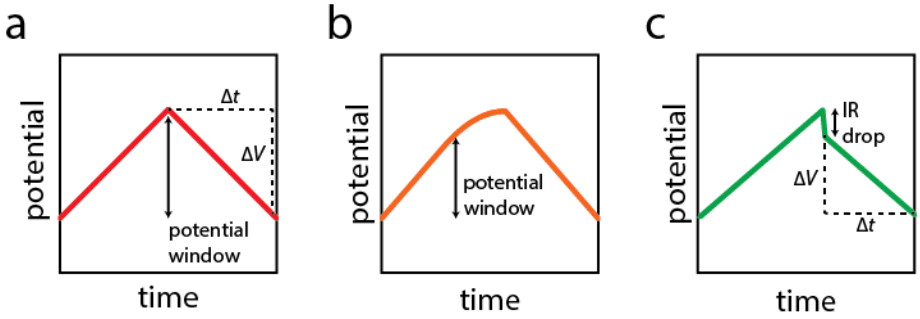

Figure 2.5 Sample galvanostatic charge/discharge plots. a) An ideal charge/discharge cycle with the slope indicated, b) a charging curve which exceeds the electrolyte stability window, leading to excess charge transfer, c) a discharge curve which is preceded by a large IR potential drop.

electrochemical stability window of the electrolyte. Electrode reactions, on the other hand, could contribute to pseudocapacitive charge storage if the behavior is reversible; irreversible behavior leads to electrode degradation and is undesirable.

Figure 2.5c shows a second nonideal behavior which occurs for all supercapacitors at high enough currents and is thus analogous to the "leaf-shape" seen in the CV plots (Figure 2.4a). This step change in current results from an instantaneous voltage drop when switching from charging to discharging. This voltage drop, known as the IR drop, arises due to ohmic resistances in the system. These resistances are a combination of electrode resistance, electrolyte resistance, and any contact resistances. For a full device, the DC equivalent series resistance, or ESR, can be calculated from this IR drop via Eq. 2.12.

$$ESR = \frac{\text{IR drop}}{2I} \tag{2.12}$$

Since this IR drop reduces the total usable voltage window, ΔV in Eq. 2.11, a low ESR is desirable for applications which require high currents.

2.3.4 AC impedance spectroscopy

AC impedance spectroscopy is a third technique commonly used to probe supercapacitor materials and devices. This technique involves the application of an alternating potential with a wide range of frequencies and measuring the amplitude and the phase shift of the resulting current (see Figure 2.6a). At each frequency, the impedance, Z, is calculated via Eqs. 2.13 and 2.14.

$$Z = |Z|e^{j\theta} \tag{2.13}$$

$$|Z| = {}^{V_p}\!/_{I_p} \tag{2.14}$$

where $|Z|$ is the magnitude of the impedance, j is the imaginary unit, θ is the phase shift, and V_p and I_p are the peak voltage and current amplitude, respectively. These impedance data are typically plotted in one of two ways: a Bode plot, which plots $|Z|$ and $-\theta$ vs. frequency, or a Nyquist plot, which plots the imaginary component of impedance against the real component. The real and imaginary components of impedance, Z' and Z'', can be obtained via Eqs. 2.15 and 2.16.

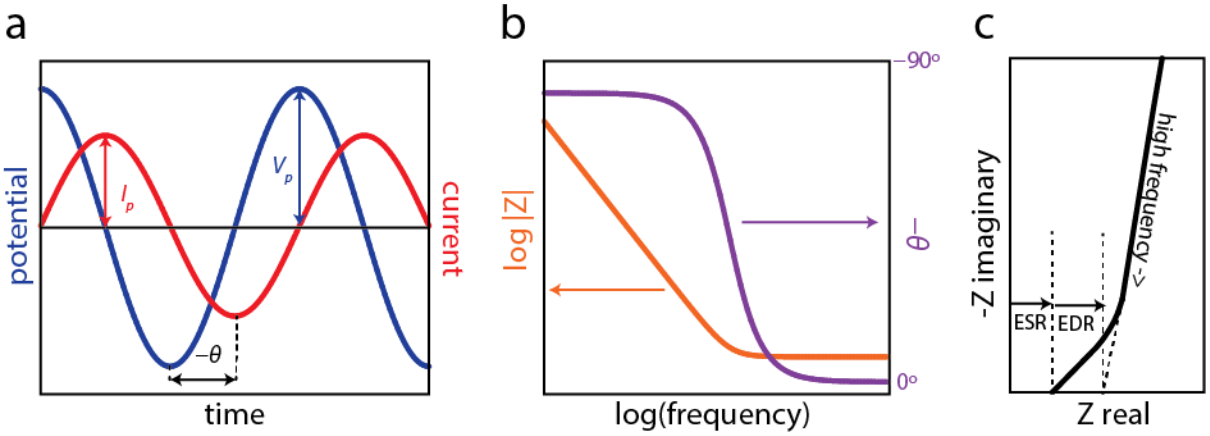

Figure 2.6 a) Sample AC impedance plot showing applied voltage and measured current vs. time for an arbitrary frequency, b) sample Bode plot showing impedance and negative phase shift plotted vs. frequency, c) sample Nyquist plot showing equivalent series resistance and equivalent distributed resistance on the plot.

$$Z' = |Z| \cos\theta \quad 2.15$$

$$Z'' = |Z| \sin\theta \quad 2.16$$

The Bode plot shown in Figure 2.6b shows a typical Bode plot for a supercapacitor. The impedance and phase data can be best understood by using an equivalent circuit model for the device. An ideal supercapacitor can be represented by a simple equivalent circuit, a resistor in series with a capacitor (Figure 2.7).

The resistor in this circuit represents the ESR of the device and the capacitance represents the double layer capacitance. The impedance of these components, Z_R and Z_C, and the total RC impedance, Z_{RC} are given in Eqs. 2.17-2.19.

$$Z_R = R \quad 2.17$$

$$Z_C = \frac{1}{j\omega C} \quad 2.18$$

$$Z_{RC} = R + \frac{1}{j\omega C} \quad 2.19$$

The angular frequency ω is given by $2\pi f$, where f is the frequency in Hz. C represents the capacitance of the capacitor. The impedance plot in Figure 2.6b can be easily understood from Eq. 2.19. At high frequencies, the capacitive term is negligible, and the impedance is dominated by the series resistance term. For ideal RC supercapacitors, therefore, the ESR can be easily estimated from the impedance at the high frequency limit. At low frequencies, the capacitive term dominates and the impedance increases indefinitely with decreasing frequency. The phase angle can be calculated from the circuit component analysis using Eq. 2.20.

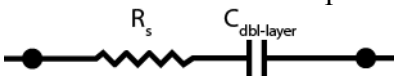

Figure 2.7 Equivalent circuit representation of an ideal RC supercapacitor

$$\theta = \cos^{-1}\frac{R}{\sqrt{R^2 + \left(\frac{1}{\omega C}\right)^2}} \quad 2.20$$

From this equation it is clear that at high frequencies, the phase angle approaches 0°, while at high frequencies, the phase shift goes to –90°. Most actual supercapacitors do not show phase angles that reach –90°, and instead approach some constant phase of n×–90°, where n is a number between 0 and 1 and defines the ideality of the system. This nonideal behavior is reflected in the phase angle data in Figure 2.6b. Frequently, instead of modeling the system as a perfect RC circuit, analysis requires the replacement of the capacitor component with a constant phase element (CPE), which has an impedance given by

$$Z_{CPE} = \frac{1}{Q_0(j\omega)^n} \quad 2.21$$

where Q_0 and n are both frequency independent. Using a CPE in place of a capacitor allows for modeling a system where the phase angle does not reach –90°, even at very low frequencies. This nonideal behavior can arise from a variety of sources including electrode surface roughness, distribution of capacitance in porous electrodes, and faradaic charge transfer reactions [1, 25, 26, 2]. The dependence of phase angle on frequency can also be used to evaluate the frequency response of a device. The frequency at which the phase angle crosses –45° can be used as a figure of merit describing how fast a supercapacitor can be cycled. The fastest reported micro-supercapacitor devices have an f_{-45} on the order of 1 kHz [27], whereas pseudocapacitive supercapacitors which rely on kinetically limited faradaic reactions may only approach –45° at mHz frequencies [28].

The Nyquist plot in Figure 2.6c shows the behavior of a typical supercapacitor with a porous electrode. In an ideal RC circuit, the Nyquist plot would resemble a vertical line at $Z' = R$. Replacing the capacitor component of the equivalent circuit with a CPE results in a subvertical line. A 45° region, known as a Warburg region, in the high frequency regime is typical for a porous electrode, and a detailed derivation is given by De Levie [29]. Briefly, at high frequencies, the current does not reach inner pore surfaces, and hence resistance and double layer capacitance both decrease. The resistive component can be represented by two values, the ESR, which has its usual meaning as the sum of the electrode, bulk electrolyte, and contact resistances, and an equivalent distributed resistance (EDR), which gives the electrolyte resistance to transport in porous electrodes at high frequencies. The difference between ESR and EDR are shown in Figure 2.6c. It should be noted that Figure 2.6b and c do not represent data for a single device. The Warburg region seen in Figure 2.6c would correspond to a –45° phase angle in the Bode plot at high frequencies.

2.3.5 Cycle lifetime

Since supercapacitors store charge primarily electrostatically, rather than electrochemically, as in batteries, supercapacitors tend to have a relatively long cycle lifetime, particularly when utilizing primarily double layer capacitance. When pseudocapacitive redox reactions are introduced, however, irreversibilities can lead to reduced lifetime performance [18, 30]. In order to probe the lifetime cyclability of an electrode material or device, repetitive charge and discharge cycles may be performed using either CV or galvanostatic charge/discharge. The testing parameters of

potential sweep rate, potential window, and specific current should be selected to reflect real world conditions. For example, for CV cycling, extremely low scan rates (< 10 mV/s) or high scan rates (> 10 V/s) are unlikely to be utilized in device operation, and hence can give misleading results. These test parameters, as well as other details like the electrolyte composition and sample size should be stated when reporting cycle lifetime results. Since long cycle lifetime is a commonly cited advantage of supercapacitors over batteries, materials and devices should be cycled many times; testing on the order of 10^4 to 10^6 cycles is typical.

2.3.6 Energy and power density

Besides lifetime cycling performance, energy and power density are the primary figures of merit for evaluating supercapacitor materials and devices. For macroscale devices, a gravimetric or volumetric density is typically reported, whereas for microscale, on-chip applications, an areal or volumetric density is more informative from a device integration perspective [31, 24]. The energy density, E, of a device can be calculated via Eq. 2.22

$$E = \frac{1}{2}CV^2 \tag{2.22}$$

where C is the specific capacitance in units of F/cm^2 or F/cm^3 obtained from CV or galvanostatic discharge, and V is the maximum accessible potential window in V. For galvanostatic discharge data, V is the voltage window not including any IR drop. E is frequently given in units of Wh/cm^2 or Wh/cm^3 and thus a factor of 1/3600 is typically inserted into Eq. 2.22. The power density can be calculated in one of two ways,

$$P = \frac{E}{\Delta t} \tag{2.23}$$

$$P_{max} = \frac{V^2}{4ESR} \tag{2.24}$$

where Δt represents the discharge time (obtained via CV or galvanostatic charge/discharge) and the ESR is typically determined from galvanostatic charge/discharge. Equation 2.24 provides a maximum available power, while Eq. 2.23 gives the total power output during discharge. Both methods are acceptable; however, when discrepancies arise, Eq. 2.23 should be used since it gives a more accurate picture of a real world discharge situation.

Each CV scan rate or galvanostatic discharge current can be used to determine a corresponding value for E and P. These values can be plotted on a logarithmic Ragone plot to determine the operational window of a device. When comparing materials or devices, the method of calculation should be clearly stated as some reports normalize using the area or volume of the electrode(s), and others of the full device, as discussed in Section 2.3.1.

2.4 Supercapacitor electrode materials

The material composition of a supercapacitor electrode has two primary requirements. First, it must be sufficient electrically conductive to transport charge carriers to the interface with the electrolyte. Second, it must be electrochemically stable. A material which is reactive with the electrolyte would be unsuitable for long term electrochemical cycling (unless this reactivity was

designed and controlled to yield pseudocapacitive charge storage). In addition to these two requirements, achieving high energy and power densities introduces a third condition, a high specific surface area. From Eq. 2.2, we can clearly see that the capacitance scales with the interfacial area. Therefore, in addition to electrical conductivity and electrochemical stability, the electrode material must also have high surface area. Flat, smooth electrodes give double-layer capacitance values of 15-50 $\mu F/cm^2$ [7, 8], which results in an energy density on the order of nWh's per cm^2. Where higher energy density is required, electrodes must be rough, porous, or particulate in order to increase the electrode/electrolyte interface. However, increasing porosity can have the secondary effect of reducing power density, as ionic transport in micropores may be limited at fast cycling rates. In many materials, a balance must be struck between increasing energy and power density through structural modifications depending on the specific application. Other materials selection considerations include safety, cost, and environmental impact.

The most commonly used material in macroscale supercapacitors is activated carbon, due to its large surface area, electrical conductance, and relative abundance [32, 18, 7, 33, 34, 35, 36]. Activated carbon is also amenable to surface modifications that can yield a pseudocapacitive augmentation of capacitance (see Section 2.2). For microscale applications, however, an additional consideration when selecting an electrode material is the ease of deposition and patterning, as well as the adhesion to the substrate. Many electrode materials have been considered for these types of applications, and several reviews discuss a number of these candidates [7, 37, 32, 35, 34, 38, 33].

2.5 Supercapacitor electrolytes

Besides the electrodes, the other necessary component of a supercapacitor is the electrolyte. The electrolyte must meet the criteria of electrochemical stability and ionic conductivity. Most supercapacitors currently use liquid phase electrolytes, but solid-state electrolytes are also a growing area of research for integrated on-chip applications, as well as high temperature device applications.

2.5.1 Liquid electrolytes

Common electrolytes include aqueous salt solutions, organic salt solutions, and ionic liquids. Some of the advantages and disadvantages of these electrolytes are summarized in Table 2.2 along with a few examples. One primary difference between the performance of these electrolytes is the electrolyte potential stability window. Since the energy density is proportional to the square of the stability window (see Eq. 2.22), increased electrochemical stability leads to larger energy density. Aqueous electrolytes have a limited stability window of ~1 V, whereas organic and ionic liquid electrolytes have shown stability windows of 2 and 3.4 V, respectively [7]. While most research efforts are focused on improving the electrode, optimization of the electrolyte is an area of research where significant energy density improvements can be made through increasing the electrolyte stability window. In addition to the stability window, the cation and anion size must also be considered for microporous electrodes. As discussed in Section 2.1, ionic confinement effects can have significant impacts on the device energy and power, and the electrolyte ion size can be selected to take advantage of the specific electrode micropore size. Finally, the affinity of the electrolyte for the electrode material must also be considered, as good electrolyte wetting of the full electrode surface is necessary for double-layer formation.

Table 2.2 Summary of liquid electrolytes investigated for supercapacitor applications

Electrolyte Type	Examples	Advantages	Disadvantages
Aqueous	KCl, H_2SO_4, KOH, Na_2SO_4	Inexpensive, not flammable, nontoxic, biocompatible	Electrochemical stability window limited to ~ 1 V
Organic	Tetraethyl Ammonium Tetrafluoroborate (TEA BF_4) in acetonitrile or propylene carbonate	Higher electrochemical stability window than aqueous	May be flammable, may be toxic, more expensive than aqueous, lower ionic conductivity than aqueous
Ionic Liquid	1-Ethyl-3-methylimidazolium bis(trifluoromethyl-sulfonyl)	Higher electrochemical stability window than organic, higher temperature stability	Expensive, lower ionic conductivity than aqueous

2.5.2 Solid-state electrolytes

While liquid electrolytes are most commonly used for macroscale supercapacitor applications, interest in solid-state electrolytes is increasing, particularly for micro-scale and flexible applications. In these applications, liquid electrolytes present encapsulation challenges; solid-state electrolytes could eliminate these concerns and simplify device fabrication. Several options exist for solid-state electrolytes. One common solid state electrolyte is an aqueous electrolyte/polymer gel, such as H_2SO_4/poly(vinyl alcohol) [39, 22, 40], KOH/polyethylene oxide [41], or H_3PO_4/poly(vinyl alcohol) [42]. These electrolytes provide similar electrochemical performance to the aqueous electrolytes themselves and have the additional advantage of being solid-state and flexible. Ionic liquids have also been incorporated into gels to form solid-state, flexible electrolytes [43, 44, 22]. These "ionogels" offer the same advantage over aqueous gels as their liquid-phase counterparts. Both aqueous gels and ionogels have been incorporated into flexible as well as rigid microscale supercapacitors [22].

In addition to these gel electrolytes, ceramic electrolytes have also been investigated for higher temperature operation, including $RbAg_4I_5$ [45], Li_2S-P_2S_5 composite [46], LiF [47], $Li_{2.94}PO_{2.37}N_{0.75}$ [48], and yttria-stabilized zirconia (YSZ) [49]. These electrolytes typically show lower ionic conductivity than the aqueous and ionic liquid based gels, but are highly interesting for applications which require high temperature operation. Many of these electrolytes are inspired by work on high temperature batteries and fuel cells, and many other options from these related areas may still prove promising for micro-supercapacitor applications. While gels can be fairly easily deposited onto microscale devices, these ceramic electrolytes present additional challenges for deposition and patterning, which will be discussed in more detail in Chapter 8.

3 Photoresist-derived porous carbon electrodes for micro-supercapacitors[1]

As discussed previously, activated carbon is the most commonly used material for macroscale supercapacitors, due to its high specific surface area, good conductivity, and large scale availability. However, for microscale applications, activated carbon is difficult to deposit and pattern [50]. Therefore, a variety of other carbon-based materials have been investigated for microscale applications including onion-like carbon [23], inkjet printed activated carbon [5], carbon nanotubes [51, 52], carbide-derived carbons [50, 53, 54], graphene [22, 55, 56, 37], reduced graphene oxide and carbon nanotube composites [21], and graphene/carbon nanotube carpets [27]. Another possible candidate material for micro-supercapacitor electrodes is porous carbon derived from pyrolyzed photoresist [57]. Photoresist is a commonly used material in lithographic patterning, and hence is easily patternable and amenable to on-chip integration. The synthesis procedure utilizes a photoresist pyrolysis technique that is akin to the fabrication of carbon-based MEMS devices [58, 59, 60]. Other efforts to use pyrolyzed photoresist as a supercapacitor electrode material have yielded very low specific capacitance values (<0.1 mF/cm^2) prior to electrochemical activation, deposition of an active material, and/or patterning of high aspect ratio 3D microstructures [61, 62, 63]. Whereas these previous studies primarily utilize H_2/N_2 forming gas and a 1000 °C temperature for the pyrolysis environment, we demonstrate that a two-step process using Ar followed by H_2/Ar at 900 °C yields significantly improved capacitive performance.

3.1 Fabrication techniques

The synthesis of the porous carbon layer consists of two primary steps, photoresist deposition and pyrolysis, as shown in Figure 3.1. SPR-220-7 photoresist (MicroChem) is spin-coated at 1800 rpm to a thickness of ~ 10 μm (as determined by profilometry) on a Si substrate. This is followed by a 3 minute soft bake at 115 °C on a hot plate. If patterning is desired, the photoresist can then be patterned using standard lithographic techniques before pyrolysis. After photoresist deposition (and optional patterning), the sample is loaded into a hot-wall CVD furnace (Thermo Scientific Lindberg Blue M), prebaked at 300 °C in ~1 Torr Ar (Praxair), for 30 minutes. This prebake is intended to drive off water and volatile solvents [64, 65, 66] in order to reduce the formation of macroscale gas bubbles in the film during pyrolysis. Then, the temperature is increased to 900 °C in the same ambient at an approximate rate of 40 °C/min. Once 900 °C is reached, the gas is changed to 10%H_2/90% Ar (Praxair) and the sample is held at 900 °C for 1 hour. This change in gaseous pyrolysis ambient at the pyrolysis temperature contrasts crucially with previous photoresist pyrolysis studies which used only one gas throughout, primarily H_2/N_2 [58, 61, 62, 63]. The sample is then cooled at a rate of about 25 °C/min to room temperature in the same H_2/Ar gas environment. It should be noted that pyrolysis temperatures of 800 °C and 1000 °C are also tested, but yield inferior capacitance results, leading to the selection of 900 °C as an optimal temperature.

[1] A modified version of this work was published in B. Hsia, M. S. Kim, M. Vincent, C. Carraro and R. Maboudian, "Photoresist-derived porous carbon for on-chip micro-supercapacitors," Carbon, vol. 57, pp. 395-400, June 2013.

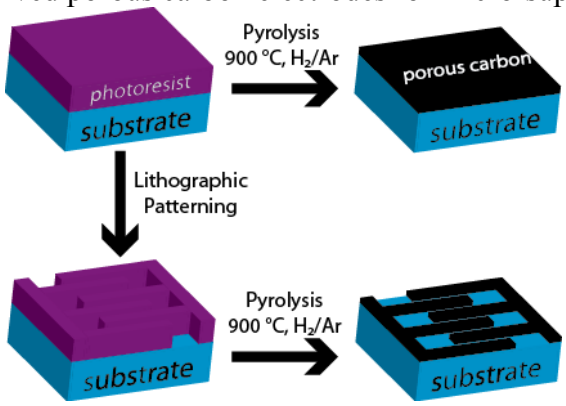

Figure 3.1. Process schematic for synthesis of unpatterned and patterned porous carbon electrodes.

After pyrolysis, a copper wire is contacted to the surface of the unpatterned film using silver epoxy and the electrochemical properties of the film are studied via a commercial potentiostat (CH Instruments, 660D Model) in 3.5 M KCl solution with an Ag/AgCl reference electrode and Pt wire counter electrode. The film's physical properties are further studied via Raman spectroscopy (HORIBA Jobin Yvon LabRam), 4-point sheet-resistance probe (Signatone S-301-4), atomic force microscopy (Digital Instruments Nanoscope IIIa), and X-Ray photoelectron spectroscopy (Omicron). Water contact angle (Rame Hart 100) measurements are used to determine the wettability of the pyrolyzed samples. In order to minimize the effect of surface contamination, samples are sonicated in isopropyl alcohol followed by sonication in deionized water and thorough N_2 drying immediately before contact angle measurements.

3.2 Film characterization

Figure 3.2 shows an optical image of patterned photoresist on a Si substrate before and after annealing and a cross-sectional scanning electron micrograph (SEM) of the annealed photoresist.

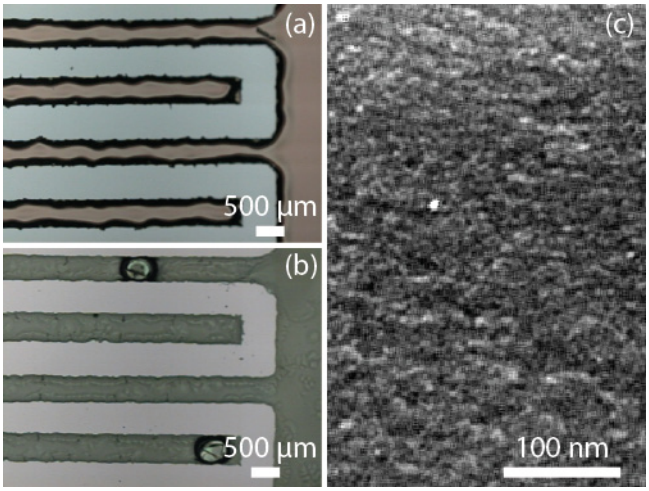

Figure 3.2. Optical image of patterned SPR-220 photoresist (a) before and (b) after pyrolysis. (c) Cross-sectional SEM image of pyrolyzed photoresist.

While the thickness decreases from ~10 to ~1 µm during pyrolysis (measured via cross-sectional SEM), the footprint of the electrode remains approximately the same due to good adhesion with the underlying substrate, highlighting that standard photolithography techniques can be employed effectively. Raman spectroscopy confirms the carbonaceous nature of the pyrolyzed material (as seen in Figure 3.3) with signature graphitic D- and G-peaks around 1350 and 1600 cm^{-1}, respectively. A characteristic Raman spectrum of commercial activated carbon (Sigma Aldrich) is shown for comparison. Atomic force microscopy (AFM) analysis shows a smooth film surface which has a root-mean-square roughness of 0.5 nm over a scan range of 2 x 2 μm^2. This relatively smooth surface morphology is similar to that observed for previous photoresist pyrolysis studies [61]. Four-point probe yields a sheet resistance of 120 Ω/□ for 1-µm thick pyrolyzed material.

3.3 Electrochemical characterization

CV experiments show good capacitive behavior at all measured scan rates. A representative behavior is shown in Figure 3.4a for 3 scan rates in 3.5 M KCl aqueous electrolyte. The sharp peaks at the extreme edges of the voltage window likely result from the oxidation/reduction processes of the aqueous electrolyte and do not contribute to pseudocapacitive energy storage. However, the reversible reduction and oxidation of oxygen containing moieties at the carbon surface is probably responsible for the current increases observed around -0.1 V and +0.6 V and has been previously reported in other carbon based electrodes [62, 7]. These functional groups are likely generated during pyrolysis due to the high oxygen content of phenolic photoresists and contribute to pseudocapacitance. The disappearance of these peaks at high scan rates indicates that these faradaic processes are likely kinetically limited. The rounding-off of the CV curve at the initiation of the cathodic and anodic sweeps for the 1 V/s scan is a result of the ESR, which will be discussed later in further detail. Specific capacitance values are calculated from the CV

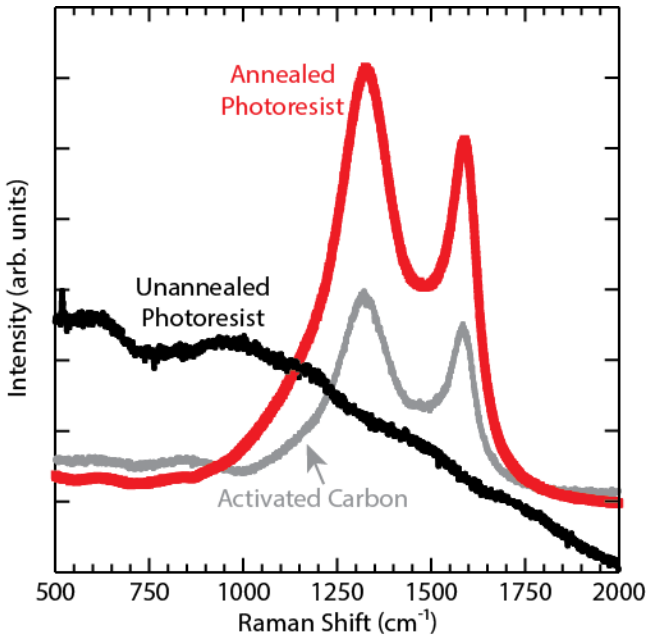

Figure 3.3 Raman spectra of photoresist, pyrolyzed photoresist, and commercial activated carbon for comparison. Pyrolyzed photoresist and activated carbon share similar peak shape and location, with broad D- and G-peaks at 1350 cm^{-1} and 1600 cm^{-1} respectively.

scans by Eq. 2.8 and divided by the electrode projected area. The measured specific capacitance of a 1 µm film is determined to be between 1.5 and 3.5 mF/cm^2 for all measured scan rates (see Figure 3.4b), resulting in a volumetric capacitance in the range of 15 – 35 F/cm^3. The decrease in capacitance at high scan rates can be attributed to a combination of factors including the

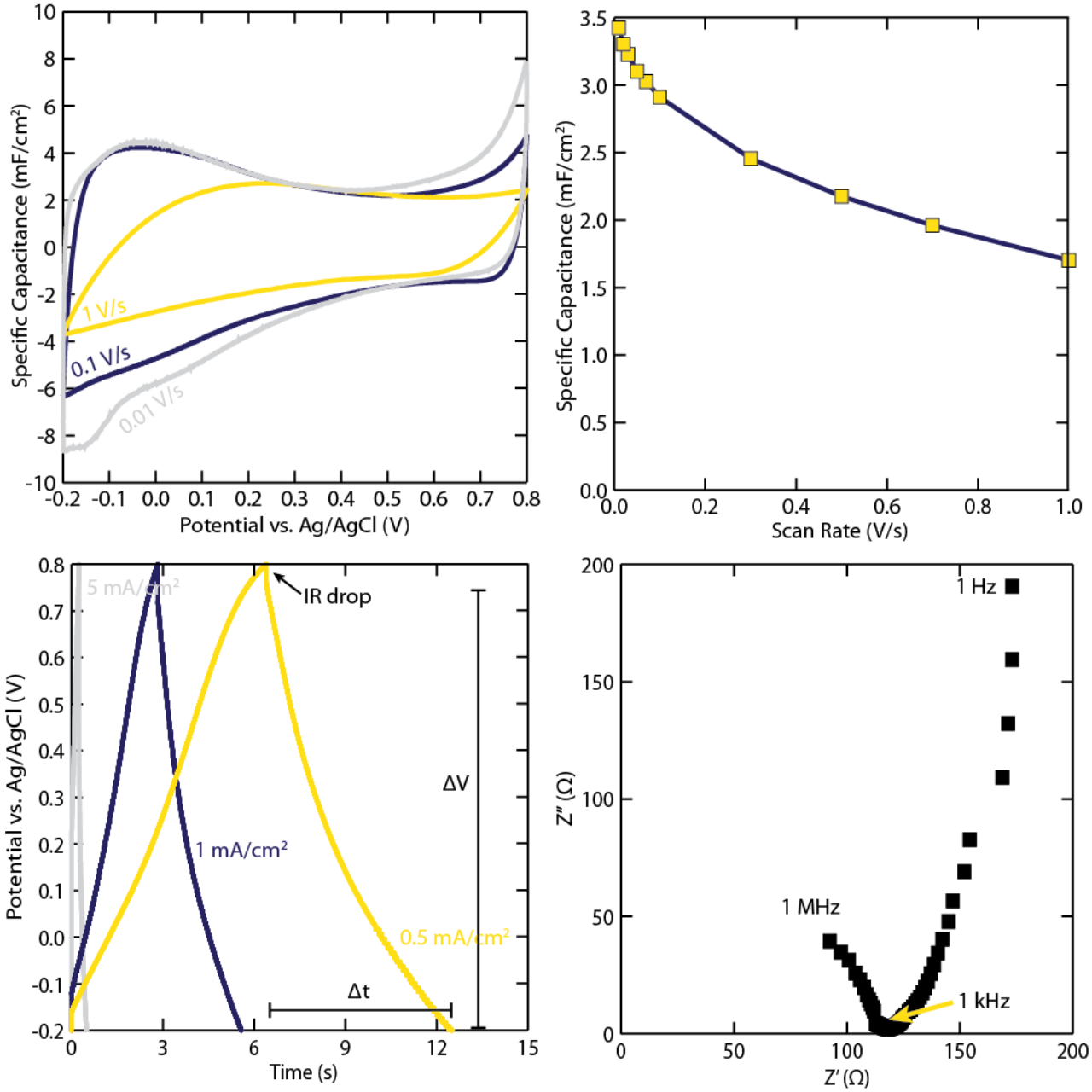

Figure 3.4 (a) Cyclic voltammograms for 1-µm thick pyrolyzed photoresist electrode. The specific current for each run is normalized by scan rate and plotted as "specific capacitance" for ease of viewing; the actual capacitance does not vary across the voltage sweep. (b) Specific capacitance, calculated from CV, at different scan rates. (c) Galvanostatic charge/discharge curves. The ΔV and Δt used for the capacitance calculation for the 0.5 mA/cm^2 scan are shown as an example. (d) AC impedance spectra. DC voltage is 0; AC amplitude is 5 mV. Electrolyte is 3.5 M KCl. Counter and reference electrodes are Pt and Ag/AgCl respectively.

kinetically limited pseudocapacitive reactions mentioned earlier and diffusion limited charge transport in the film's micropores [67].

As a further probe of the electrochemical properties of the film, galvanostatic charge discharge cycles are performed (Figure 3.4c). The electrode is charged and discharged at a constant current, and the voltage is measured. The capacitance can also be calculated from these measurements using Eq. 2.8; in the case of galvanostatic discharge, Eq. 2.11 is used. For currents of 0.5, 1, and 5 mA/cm^2, the specific capacitance is calculated to be 3.2, 3.0, and 2.1 mF/cm^2, respectively, in good agreement with the capacitance values obtained from the CV measurements. The non-linearity of the charge and discharge curves confirms the contribution of pseudocapacitive faradaic reactions to the capacitance, as an ideally polarizable electrode with no charge transfer to the electrolyte would have linear charge and discharge curves. The galvanostatic measurements additionally provide quantitative information about the ESR. The rapid change in current at the start of each charge/discharge half cycle is commonly termed the IR drop and is indicative of an ohmic resistance, which can be attributed to electrode resistance, contact resistance, and electrolyte resistance. ESR can be estimated from the IR drop by dividing the voltage drop by twice the current [24], resulting in the value of about 40 Ω for a 0.32 cm^2 sample with 1-μm thick pyrolyzed material. AC impedance spectroscopy (ACI, Figure 3.4d) can also be used to estimate ESR, by measuring the impedance at frequencies approaching ∞ [1]; due to the limitations with our potentiostat, the high frequency limit beyond 1 MHz is not accessible, but by extrapolating the apparent Nyquist semi-circle to the high frequency limit, an ESR value of about 25 Ω is obtained, which is in reasonable agreement with the estimates from galvanostatic charge/discharge measurements. ESR limits a device's maximum power, and the high ESR measured here likely results from diffusional resistance in pores [67] as well as the relatively high sheet resistance of the pyrolyzed photoresist film (120 Ω/□). Higher pyrolysis temperatures have previously been shown to reduce pyrolyzed polymer sheet resistance [58, 61, 68, 69], but may also result in decreased porosity [64], as is briefly discussed below.

The theoretical energy density of the supercapacitor can be calculated using Eq. 2.22. For a voltage window of –0.2 to 0.8 V, the theoretical energy density is calculated to be on the order of 1-1.5 mJ/cm^2 for the scan rates measured here, yielding volumetric energy densities of the order 10-15 mJ/cm^3.

A long-term stability test is performed via repetitive CV scans at a scan rate of 100 mV/s. The capacitance values, as obtained using Eq. 2.8 and normalized to the initial value, are presented in Figure 3.5. Although the reason for the initial decline is not known, the results demonstrate the excellent long-term stability of the film in an aqueous electrolyte. A second stability test, performed at a scan rate of 5 V/s over 500,000 cycles shows similar behavior. This robust performance compares favorably to those reported by Beidaghi et al., which showed a 12% capacitance fade over only 1000 cycles for an electrochemically activated pyrolyzed SU-8 micro-supercapacitor [62].

3.4 Impact of pyrolysis parameters

The measured capacitance even at high scan rates of >1.5 mF/cm^2 is nearly 3 orders of magnitude higher than the values reported by Ranganathan et al. for AZ-4300 photoresist pyrolyzed at 1000 °C in 5%H_2/95%N_2 gas [61]. In order to probe the large disparity between these results, SPR-220-7 is pyrolyzed using the aforementioned parameters, but instead of using one gaseous environment for heating and another for pyrolysis as done in this paper, the 10%H_2/90%Ar gas is flowed throughout the entire procedure, including heating and cooling. This procedure is intended to emulate the previous works that employed forming gas throughout the procedure. These films yield specific capacitances on the order of 25 μF/cm^2, much lower than the values achieved here using the alternative two-gas procedure. Pyrolysis in an Ar-only environment is also probed, yielding a capacitance of ~ 200 μF/cm^2, also quite low relative to those annealed with the two-gas procedure. Starting with the same SPR-220 film thickness of 10 μm, the thickness after pyrolysis is measured via cross-sectional SEM to be 1.0, 0.95, and 1.1 μm for the films pyrolyzed in the two-gas, H_2/Ar only, and Ar only environments respectively. For comparison, a SU-8-2007 film is also pyrolyzed using the two-gas procedure after subjecting it to a blanket exposure and development step, and the resulting capacitance is on the order of 1 mF/cm^2, similar to the SPR-220-7 film which has been the focus of the present paper. This result implies that within the range of parameters examined, it is the synthesis details, and not the choice of photoresist, that is responsible for the improved capacitance. Another procedural difference between this work and Refs. [61, 62] is the final pyrolysis temperature (900 °C vs. 1000 °C). A test of the resultant film from the two-gas procedure at 1000 °C yielded significantly lower capacitance (< 1 μF/cm^2) than that of the 900 °C film, likely due to decreased specific surface area in the film pyrolyzed at 1000 °C. The porosity of the pyrolyzed photoresist films is a result of the evolution of volatiles during pyrolysis [70]. Jenkins and Kawamura show that porosity of pyrolyzed phenolic resins (which are chemically similar to positive photoresists like SPR-220) depends highly on pyrolysis temperature, with a maximum micropore volume achieved at about 700 °C [64]. However, pyrolysis of photoresist at 700 °C yields a high resistance film [61, 64]; a temperature of 900 °C is selected to optimize both parameters. The analysis indicates that the pyrolysis temperature, in addition to the two-gas procedure, is crucial for the formation of a porous film.

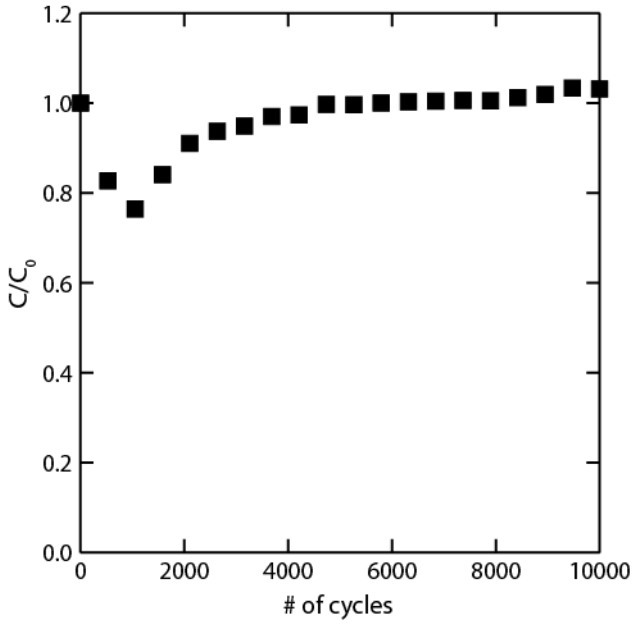

Figure 3.5. Plot of capacitance over 10,000 charge/discharge cycles, normalized by original capacitance value. Scan rate is 100 mV/s, and voltage window -0.2 V to 0.8 V. Electrolyte is 3.5 M KCl. Counter and reference electrodes are Pt and Ag/AgCl respectively.

In order to probe the source of differences between the two-gas and one-gas pyrolyzed SPR-220 samples, water contact angle measurements are carried out (Figure 3.6). Measurements show that the samples annealed with Ar/H_2 gas or Ar throughout are significantly more hydrophobic than those which result from the two-gas procedure. These results suggest improved electrolyte wetting of interior pore surfaces is likely responsible for the higher capacitance from the two-gas

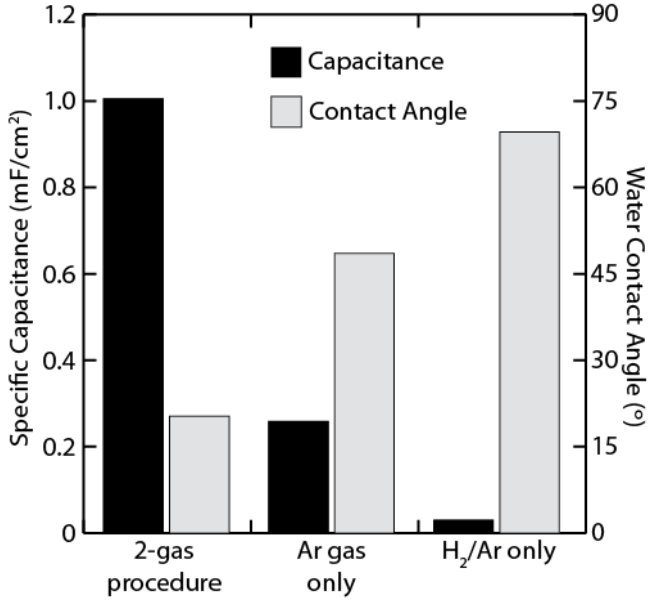

Figure 3.6. Comparison of SPR-220 films pyrolyzed under various gaseous environments. Capacitance is calculated from CV at a 100 mV/s scan rate. Water contact angle is shown on the right hand axis.

pyrolysis. The more hydrophilic the film, the greater the double layer surface area available for charging. As to the underlying mechanism for the variation in film wettability, Lyons et al. demonstrated that pyrolyzed phenolic resins differ in volumetric shrinkage depending on pyrolysis atmosphere: films pyrolyzed in pure N_2 are about twice as thick as those pyrolyzed in pure H_2, implying significant reactivity between the H_2 and the carbonizing film leading to a smaller, and perhaps denser film [69, 71]. In our case, the thickness differences are not as large (1.1 vs. 0.95 μm for Ar vs. H_2/Ar), but follow the same general trend. Thermogravimetric analysis and mass spectrometry undertaken during pyrolysis in high vacuum or inert environments show that much of the mass loss occurs at T < 600 °C, and further carbonization occurs at higher temperatures but accounts for a small fraction of the overall mass loss [61, 65, 66, 64]. Therefore, in our procedure, the majority of the carbonization likely proceeds primarily in an inert (Ar) environment and before H_2 is introduced. According to Lyons et al., this environment should lead to a thicker film than one in which H_2 is present throughout [69]. Introduction of H_2 at 900 °C can then lead to additional carbon removal, potentially by the etching of the pores. This high porosity can contribute to the low observed water contact angle (and improved wetting) of the two-gas pyrolyzed sample by capillary action. Unfortunately, the porosity of the films could not be reliably determined via BET analysis because the amount of material produced is too small to yield reliable adsorption measurements. This is an area that requires further investigation. The slightly improved wetting of the Ar-only sample compared to the forming gas only sample may be a result of more oxygen-containing functional groups on the Ar-only sample (confirmed via XPS, which showed a O:C ratio of 23% for the Ar-only procedure vs. 13% for both the 2-gas and forming-gas only procedures) [72].

3.5 Conclusion

In summary, we have developed a highly porous carbon material from photoresist which is easily deposited and patterned and can be integrated into planar, on-chip supercapacitor applications. The capacitances achieved are on the same order of magnitude as other, more complex planar supercapacitor fabrication techniques and show robust cycle behavior exceeding half a million cycles. The process is readily scalable to large wafer fabrication and can be easily integrated into microdevice fabrication. Furthermore, the storage capacity can be tailored by modulating thickness via spin speed changes or additional spin coats. This fabrication method holds promise for the low-cost, facile production of on-chip supercapacitors for micro-energy storage.

4 Flexible micro-supercapacitors with photoresist-derived porous carbon electrodes

Most commonly, micro-supercapacitors are fabricated on rigid substrates such as Si, but growing interest in flexible electronics applications such as wearable electronics and roll-up displays has stimulated the development of flexible energy storage solutions, including flexible micro-supercapacitors [73, 74]. While carbon-based electrodes have been investigated for rigid microscale applications, such as onion-like carbon [23], inkjet printed activated carbon [5], carbon nanotubes [51], carbide-derived carbons [50, 53, 54], graphene [22, 55, 37], reduced graphene oxide and carbon nanotube composites [21], graphene/carbon nanotube carpets [27], and photoresist-derived porous carbon [57]. However, limited work has been reported on the development of carbon-based flexible micro-supercapacitors. Possible candidates for micro-supercapacitor electrode materials that can be deposited directly on flexible substrates include pseudocapacitive polymers such as polypyrrole [73] and polyaniline [75], and carbon-based electrodes including laser-scribed graphene oxide [22], reduced graphene oxide [55], and inkjet-printed graphene [76].

Another promising method for flexible micro-supercapacitor fabrication is the transfer of prepatterned electrodes onto flexible substrates, analogous to the dry transfer of carbon nanotubes onto polymer substrates for flexible electronics [77, 78]. This technique has the advantage of good device-to-substrate adhesion [77] and allows for the use of high temperature-processed materials on polymer substrates, which would otherwise be impossible given the limitations imposed by glass transition temperature of many polymers. Additionally, lithographic patterning can be done using traditional microfabrication processes designed for rigid substrates prior to transfer. In this study, pyrolysis of patterned photoresist is used to form porous, high specific surface area carbon electrodes (see Chapter 3 and Ref. [57]). This technique is simple and can utilize existing microfabrication infrastructure for easy integration with micro-devices. The subsequent transfer to a polymer substrate is demonstrated to yield a robust, flexible micro-supercapacitor device with good electrochemical performance.

4.1 Experimental

4.1.1 Sample preparation

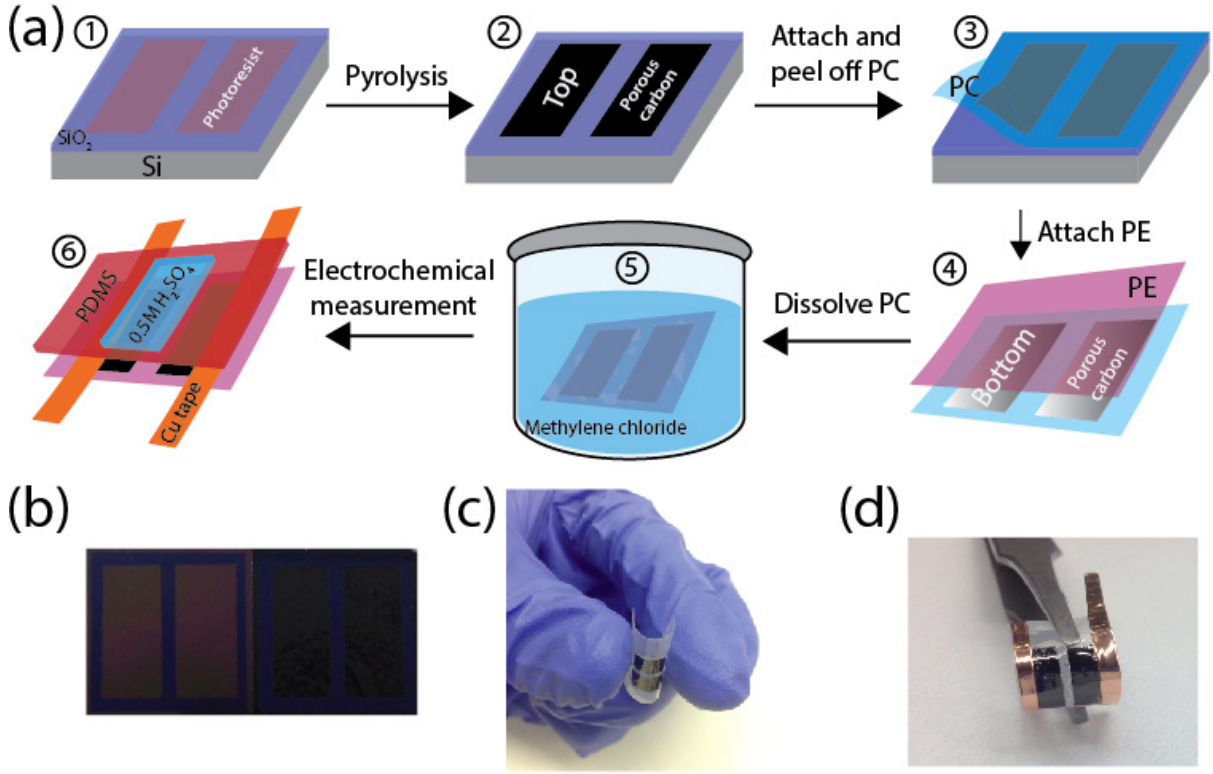

Figure 4.1 (a) Schematic illustration of flexible micro-supercapacitor fabrication process, PC is polycarbonate, PE is polyethylene, and PDMS is polydimethylsiloxane. Photographs of (b) patterned photoresist electrodes before (left) and after (right) pyrolysis, (c) photoresist-derived porous carbon electrodes transferred to polyethylene and being flexed and (d) fully-fabricated device.

Figure 4.1a shows a schematic illustration of the flexible planar microsupercapacitor fabrication process. The synthesis of the photoresist-derived porous carbon film is previously described in detail in Chapter 3 [57]. Briefly, a layer of SiO_2 is deposited via thermal oxidation on 4" Si (100) wafers. Then, a commercial positive photoresist (SPR-220-7.0) is spin-coated onto the wafer and is patterned in a two-pad configuration using photolithography. The substrate is heated for 1 hr in a hot-wall tube furnace (Thermo Scientific Lindberg Blue M) in a gas atmosphere of H_2 and Ar and at 900 °C, resulting in the pyrolysis of the photoresist [57]. The size and shape of these electrodes are identical to that of the patterned photoresist, demonstrating the good pattern fidelity post-pyrolysis (Figure 4.1b). After pyrolysis, a double-transfer process is used to move the patterned electrodes to a flexible substrate. First, the porous carbon film is transferred to polycarbonate (PC, thickness of 100 µm, McMaster-Carr) by melting the PC onto the sample at 300 °C in air for 3 min. After cooling to room temperature, the PC is carefully peeled off from the substrate. Then, a polyethylene film (PE, thickness of 100 µm, McMaster-Carr) is applied to the exposed surface of the transferred carbon film by melting the PE to the polycarbonate at 200 °C in air for 5 min. During this process, a pressure of about 18 kPa is applied on the top of the sample to reduce curling from any thermal mismatch and to maximize porous carbon-to-PE

adhesion. After cooling to room temperature, the transferred film with PC and PE is immersed in methylene chloride solution overnight to dissolve the PC. Figure 4.1c shows an optical image of the device after the 2nd transfer. Copper tape is the attached as a current collector (Figure 4.1d). As will be discussed, a double transfer process is necessary, as the surface of the carbon film after one transfer is found to have significantly different morphological and electrochemical properties than the opposite surface.

4.1.2 Film characterization

The surface roughness of the carbon film is investigated via atomic force microscopy (AFM, Digital Instruments Nanoscope IIIa) in tapping mode. The surface wettability is probed via water contact angle measurements (Rame Hart Model 290).

4.1.3 Electrochemical analysis

The electrochemical performance of the flexible microsupercapacitor is measured via cyclic voltammetry (CV), galvanostatic charge/discharge, and AC impedance spectroscopy using a commercial potentiostat (AC Instruments, 660D Model). To obtain these measurements, an adhesive conductive tape (Cu/Ni tape, Ted Pella, #16067) is connected to the edge of each carbon film pad, (see Figure 4.1d), and a polydimethylsiloxane (PDMS) stamp is used to isolate the conductive tape from the electrolyte. A central hole is cut into the PDMS and filled with electrolyte for testing. All the electrochemical measurements are performed in an aqueous electrolyte of 0.5 M H_2SO_4.

4.2 Results and discussion

4.2.1 Comparison of single and double-transferred electrodes

Due to the temperature limitations of most bulk flexible materials, many substrates would not survive the pyrolysis temperatures required to form conductive porous carbon films. Therefore, in order to fabricate a flexible device using pyrolyzed photoresist electrodes, post-pyrolysis transfer to a flexible substrate is required. However, a single transfer is found to yield a different film surface relative to the as-pyrolyzed surface. The first transfer (step 3 in Figure 4.1a) exposes the electrode surface which is at the photoresist/substrate interface during pyrolysis, and hence, this surface is denoted as the “bottom” film surface, while the second transfer (step 5 in Figure 4.1a) re-exposes the surface in contact with the gas (H_2 and Ar) during pyrolysis, and is denoted as the “top” surface. In this study, both the top and bottom surfaces are examined to compare the differences in electrochemical performance.

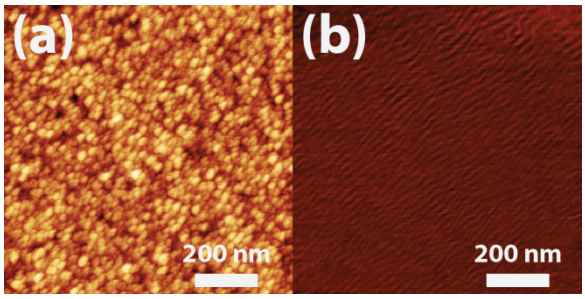

Figure 4.2 AFM images of the (a) top and (b) bottom surface of the photoresist-derived porous carbon film. Both images have a z-scale of 10 nm.

The atomic force microscopy (AFM) images of the top (as measured before transfer) and bottom (as measured after first transfer) of the carbon film, shown in Figure 4.2, illustrate the morphological differences in the two surfaces. The top surface of the film is significantly rougher than the bottom with RMS roughness of 1.3 and <0.3 nm, respectively. The bottom surface also shows no apparent porosity. This difference results from two experimental factors: first, the bottom surface of the photoresist is in contact with the smooth oxide substrate during pyrolysis, leading it to form a matching smooth surface; and second, the mechanism of pore formation during pyrolysis involves the vaporization of volatile photoresist components (which escape from the vapor/photoresist interface) and the etching effects of H_2 (which is present only at the vapor/photoresist interface) [57, 64]. Transport limitations may not allow these processes to propagate all the way through the film thickness.

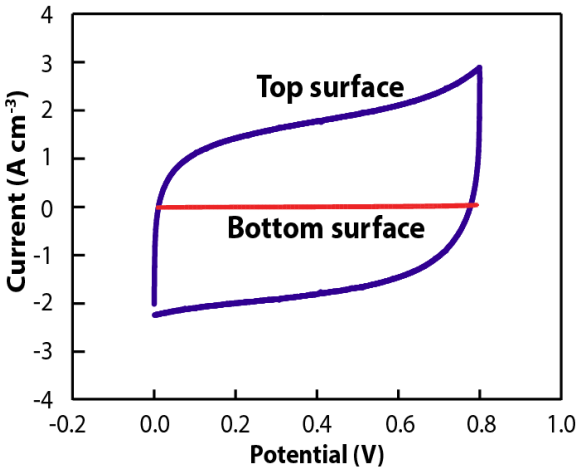

Figure 4.3 Cyclic voltammograms obtained on the photoresist-derived porous carbon electrode after one transfer (bottom surface) and after two transfers (top surface). The scan rate used is 100 mV s^{-1}. Electrolyte used is 0.5 M H_2SO_4.

In accordance with the AFM results, cyclic voltammetry (CV) results show that the top surface, obtained by double transfer, yields about 75 times higher areal capacitance at a scan rate of 100 mV s^{-1} compared to the bottom surface, obtained after single transfer (Figure 4.3). The bottom of the film yields an areal capacitance of ~10 µF cm^{-2}, a value that is about two times higher than that of a smooth film [28]. The specific areal capacitance of the top surface is measured to be significantly higher, 0.75 mF cm^{-2}, in agreement with our previous work with untransferred,

unpatterned porous carbon films [23]. Water contact angle measurements are performed to compare the wetting of both surfaces. The top and bottom surfaces yield contact angles of 12° and 60° respectively, which confirms that the top surface is more hydrophilic than the bottom surface, resulting in more effective wetting of the pores by aqueous electrolytes. A double-transfer process is therefore necessary to obtain high energy density for the device.

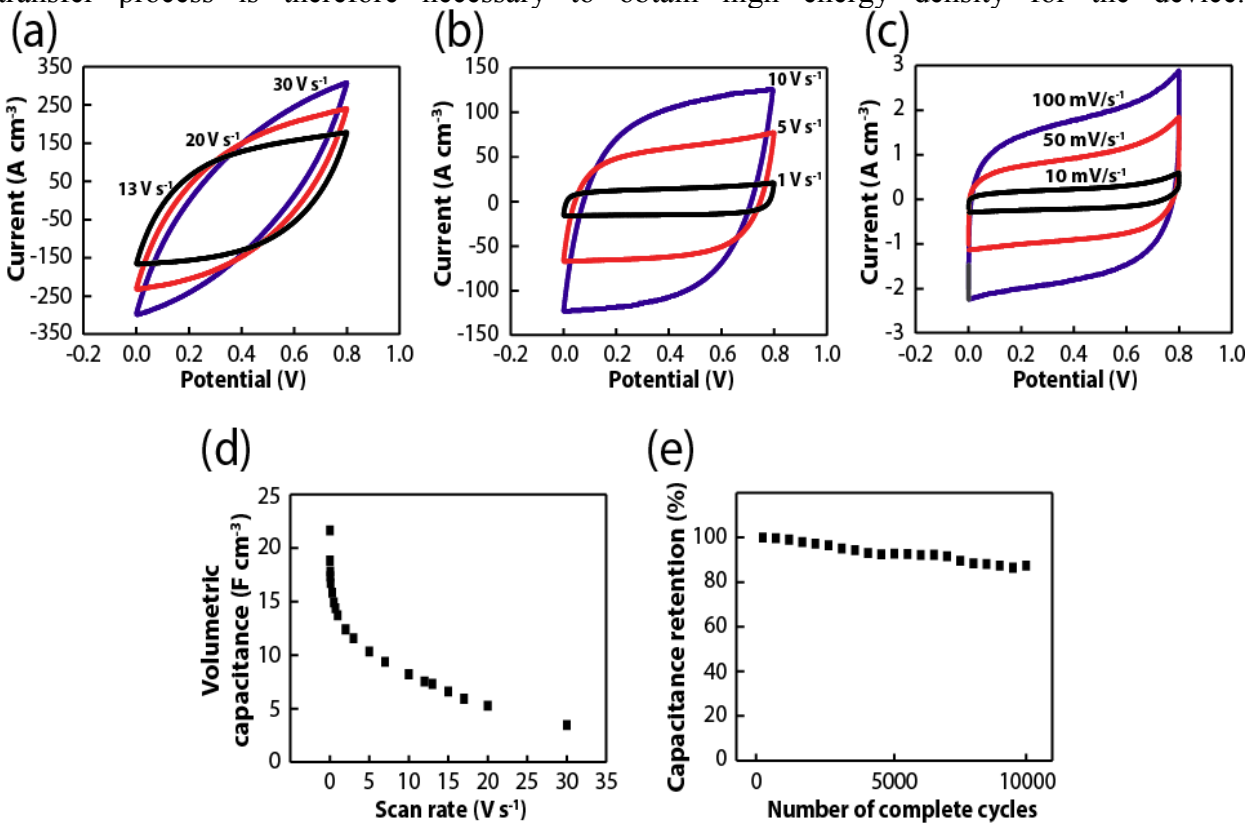

Figure 4.4 Cyclic voltammograms of fabricated flexible micro-supercapacitor at scan rates of (a) 13 to 30 V s^{-1}, (b) 1 to 10 V s^{-1}, and (c) 10 to 100 mV s^{-1}. (d) Calculated volumetric capacitance as a function of scan rate. (e) Lifetime of the flexible supercapacitor over 10,000 CV cycles from 0 to 0.8 V at a scan rate of 100 mV s^{-1}. Electrolyte used is 0.5 M H_2SO_4. All values are based on the total working electrode volume.

4.2.2 Electrochemical performance

The CV curves of the flexible micro-supercapacitor at several different scan rates are shown in Figure 4.4. The CV shape is semi-rectangular at scan rates of up to 10 V s^{-1}, indicating ideal capacitive performance (see Figure 4.4a-c). Since the CV curves retain a rectangular form even at the high scan rate of 10 V s^{-1}, this is a good indication of the high-power capability of the device. The skewing of the CV shape at higher scan rates indicates some power limitations arising from the electrode resistance as well as the electrolyte resistance in the pores [67]. Our previous work suggests that the carbon film consists of a highly porous network [57], leading to possible mass transfer limitations. Therefore, at higher scan rates, where the ions must access the micro-pores inside of the film in a short amount of time, the capacitance of the film is lower [79]. Figure 4.4d, which shows higher capacitance at lower scan rates, illustrates this effect. The volumetric capacitance of the device is calculated from Eq. 2.8 and normalized by the projected active area of both electrodes and the thickness of the porous carbon film (measured via cross-

sectional SEM, 0.9 µm). The active area includes only the portion of electrode directly in contact with electrolyte. The calculated volumetric capacitance of the device ranges from 1.7 to 11 F cm^{-3} over the tested scan rates. Lifetime CV cycling shows that the flexible micro-supercapacitor exhibits robust cycling stability, maintaining ~86% of the initial capacitance over 10,000 complete charge/discharge cycles as shown in Figure 4.4e.

Galvanostatic charge/discharge has been performed at various currents densities, up to nearly 0.5 kA cm^{-3}. The charge/discharge curves are linear, indicating ideal capacitive behavior (see Figure 4.5a and b). A small IR drop can be seen at the start of each discharge cycle, with larger drops seen at higher current densities. The volumetric capacitance and ESR can be calculated from Eqs. 2.11 and 2.12. The capacitance values obtained via charge/discharge measurements show good agreement with the calculated capacitance from CV (see Figure 4.5c). The ESR is calculated to be 8 Ω·cm^2 at a current of 277 A cm^{-3}.

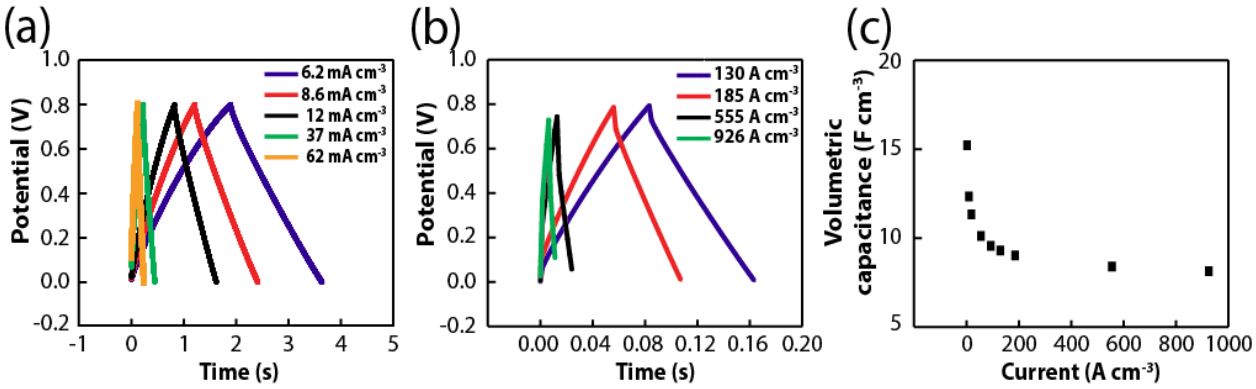

Figure 4.5 Galvanostatic charge/discharge curves of flexible micro-supercapacitor for different currents, (a) 3.1 to 31 mA cm^{-3}, (b) 65 to 463 A cm^{-3}, and (c) corresponding volumetric capacitances. Electrolyte used is 0.5 M H_2SO_4. All values are based on the total working electrode volume.

Another figure of merit for evaluating device cycling speed is the -45° phase angle crossover frequency, obtained from AC impedance data; a high frequency implies fast cycling performance. As seen in Figure 4.6a, the -45° crossover frequency of our device is ~122 Hz in the aqueous electrolyte. The crossover frequency value is somewhat lower than other high power microsupercapacitors fabricated on rigid substrates and measured in aqueous electrolytes, e.g., 200 Hz for reduced graphene oxide and carbon nanotube (rGO-CNT) composites [21], and 460-1343 Hz for graphene/carbon nanotube carpets-based micro-supercapacitors (G/CNTs-MCs) [27], but is significantly higher than other porous electrode materials such as activated carbon, which show -45° crossover frequencies of less than 10 Hz (estimated from impedance data in references [23] and [5]). Flexible micro-supercapacitors based on laser scribed graphene electrodes show a crossover frequency of ~50 Hz in aqueous solution, indicating that the device presented in this paper has a faster cycling performance [22]. The Nyquist plot shown in Figure 4.6b shows a sub-vertical line which indicates a deviation from ideal capacitive behavior, likely due to the film's distribution of pore size leading to limited utilization of film micro-pores at high frequencies [80].

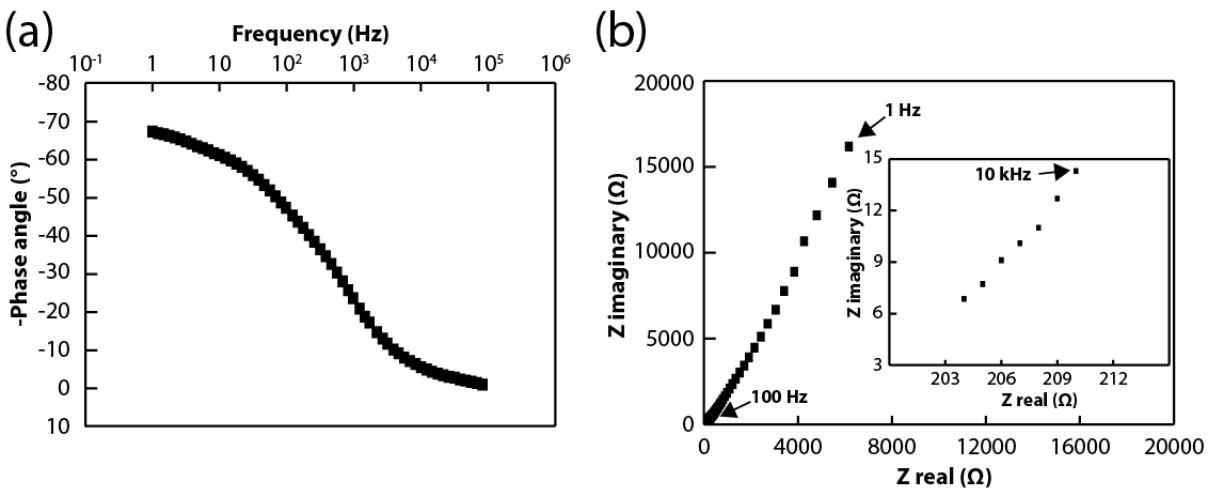

Figure 4.6 AC impedance spectroscopy results of flexible micro-supercapacitor with AC amplitude of 5 mV and DC voltage of 0 V. (a) Negative phase versus frequency plot for the micro-supercapacitor where the -45° crossover frequency is at 122 Hz. (b) Nyquist plot for the flexible micro-supercapacitor. The inset shows the high frequency regime. Electrolyte used is 0.5 M H_2SO_4.

4.2.3 Energy and power density

The theoretical energy and power densities of the device are calculated from CV data using Eqs. 2.22 and 2.23. The flexible micro-supercapacitor presented in this paper provides outstanding energy density as shown in Figure 4.7. The theoretical power and energy densities range from 0.05 – 56 W cm^{-3} and 0.8 – 1 Wh cm^{-3}, respectively. Despite a simple two-pad geometry and a rather simple fabrication process, the energy density is competitive with other recently reported flexible and rigid micro-supercapacitors measured in aqueous electrolytes [22, 21, 27]. The device does not yield the highest power density due to the transport limitations inherent in a porous network, but the achieved power is still competitive as indicated by the good CV performance at high scan rates and the high crossover frequency in the AC impedance results. Furthermore, a dense interdigitated electrode geometry has been shown to improve power performance in other carbon-based micro-supercapacitors, and the simple geometry of the presented micro-supercapacitor likely further contributes to the power limitations due to the large mean ionic diffusion path [22]. Optimization of the electrode geometry for improved power performance is currently under investigation. Standard photolithography provides high resolution patterning of photoresist on the nanoscale; numerous geometries or configurations of electrodes can be fabricated and integrated on-chip with micro-devices.

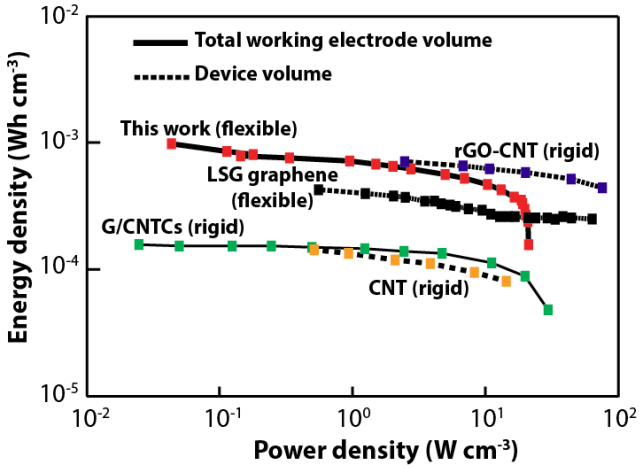

Figure 4.7 Ragone plot comparing the present flexible micro-supercapacitor to other micro-supercapacitors. All the results are measured in aqueous electrolytes. "Device volume" indicates that the energy and power density are given in reference to the volume of the fully-fabricated device including electrode, inter-electrode gap, and current collector volume. These density values will necessarily be smaller than the values given in reference to the electrode volume only. Laser-scribed graphene (LSG), reduced graphene oxide and carbon nanotube (rGO-CNT) & carbon nanotube (CNT), graphene and carbon nanotube carpet based micro-supercapacitor (G/CNTCs) data are obtained from reference [22], [21], and [27] respectively. The type of substrate, flexible or rigid, is indicated in the plot.

4.2.4 Flexing performance

In order to determine the mechanical stability of the micro-supercapacitor upon flexing, the 1 x 1 cm^2 device is placed on the round surface of a cylinder with varied radii of 17.5, 12.5, and 5 mm. One end of the sample edge is fixed to the cylinder wall, and the other edge is manually bent to the cylinder surface and allowed to unbend. The device is bent 100 times at the largest radius of curvature, tested in the unbent configuration, bent 100 times at the next largest curvature, tested, and finally bent 100 times at the smallest curvature, resulting in 300 total bending cycles. Flexing tests showed good capacitive performance retention after repeated bending. As seen in Figure 4.8, the cyclic voltammogram shows a consistent rectangular shape at 100 mV s^{-1} after repetitive bending of the device at three different radii. There is only a ~2% deviation in the volumetric capacitance after 300 flexing cycles. Other flexible electrode materials such as laser-scribed graphene have been demonstrated to yield good micro-supercapacitor performance in the bent configuration, but robust mechanical stability has not yet been demonstrated [22], and is an important consideration for applications which require repeated flexing cycles. The flexible micro-supercapacitor presented in the work shows consistent performance after repeated flexing, demonstrating the mechanical stability of the film, and is therefore promising for flexible energy storage applications.

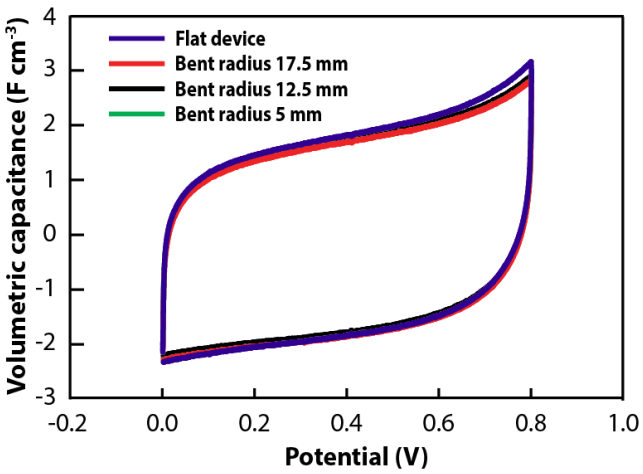

Figure 4.8 Cyclic voltammogram comparison of the device before and after bending cycles. Scan rate used is 100 mV s^{-1}.

4.3 Conclusion

In summary, we have fabricated a flexible micro-supercapacitor using photoresist-derived porous carbon electrodes. The electrodes can be easily patterned and integrated for on-chip energy storage applications by using existing lithographic techniques. Furthermore, the electrode fabrication can be scaled to wafer-scale processing and the pyrolyzed electrodes can be easily transferred to flexible substrates while demonstrating excellent electrochemical performance including high energy and power densities, robust lifetime cycling performance, and high flexibility. This technique holds promise for the fabrication of high performance flexible micro-supercapacitors that are scalable and easily integrated with existing microfabrication technologies.

5 Electrochemically activated porous-carbon supercapacitor electrodes[2]

In addition to its high area available for double-layer capacitance, activated carbon presents the additional benefit of being amenable to surface chemical modification. Proper functionalization of the carbon surface can yield additional storage capacity through pseudocapacitive redox reactions [34, 18, 7, 32]. The overall energy and power densities of a supercapacitor depend not only on the electrode surface area, but also on the selection of electrolyte, which is typically either an aqueous or organic salt solution, or an ionic liquid [34, 7, 35]. Use of an aqueous electrolyte limits the available voltage due to electrolyte breakdown, but typically results in higher capacitance and lower electrolyte resistance [34, 7, 32, 35]. Aqueous electrolytes have the additional benefits of being inexpensive and environmentally benign. In pseudocapacitive supercapacitors, the selection of a particular aqueous salt may also be expected to have a significant impact on overall performance as well as cycle lifetime.

The electrochemical modification of carbon electrodes has been demonstrated both to improve their overall surface area and to introduce electroactive functional groups which can contribute to pseudocapacitance [81, 82, 62]. This technique offers promise in increasing the overall specific capacitance of supercapacitor devices. However, as this technique modifies the carbon material's structure and chemical composition, the effects on long term performance must be determined. In this Chapter, we examine the lifetime cycling performance of an activated carbon electrode fabricated from pyrolyzed photoresist in KCl and H_2SO_4 electrolyte. This fabrication technique is chosen due to its inherent scalability, particularly for on-chip micro-supercapacitor applications [57]. Electrochemical activation is inspired by Refs. [82] and [62], and is performed in 0.5 M H_2SO_4 solution which is deaerated with bubbling N_2 for at least 20 minutes prior to activation. A 1.9 V bias (vs. Ag/AgCl) is applied for 1 hour, followed by 25 minutes of reduction at -0.3 V.

[2] A modified version of this work was published in: B. Hsia, M. S. Kim, C. Carraro and R. Maboudian, "Cycling characteristics of high energy density, electrochemically activated porous-carbon supercapacitor electrodes in aqueous electrolytes," J. Mater. Chem. A, vol. 1, pp. 10518-10523, 2013.

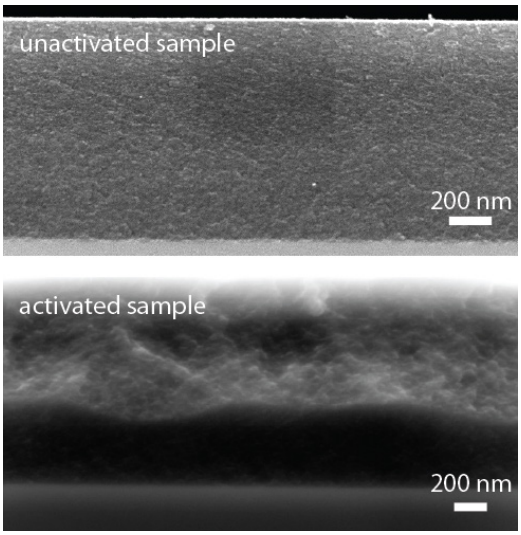

Figure 5.1 Cross-sectional SEM images of pyrolyzed photoresist film before and after activation.

5.1 Film characterization

The pyrolysis of SPR-220 photoresist results in a porous carbon film with good capacitive properties without additional activation [57]. After activation, a portion of the film is electrochemically modified to exhibit a rougher, more porous morphology, as evident from cross-sectional SEM images (Figure 5.1). The overall thickness decreases from 1.4 µm to 1.2 µm. A similar change in morphology after electrochemical activation has been previously investigated on glassy carbon electrodes [82]. Based on differential electrochemical mass spectrometry performed by Sullivan et al., the primary reaction product during oxidation is CO_2, which arises from the electrochemical etching of the carbon film [82]. This etching increases access to closed pores and increases the overall surface area. In addition to increasing the film porosity, this process also leads to the formation of oxygen-containing surface functional groups,

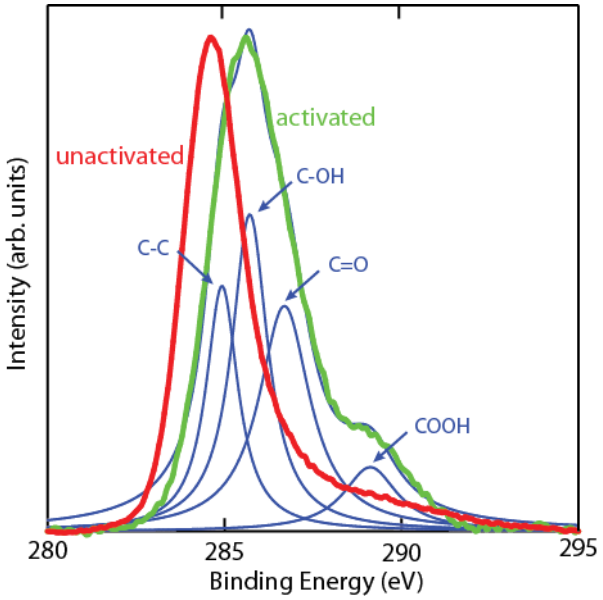

Figure 5.2 C 1s x-ray photoelectron spectra of pyrolyzed photoresist before and after activation. Peak deconvolution is shown for activated film

as is apparent from XPS (Figure 5.2). Following activation, the C 1s XPS peak clearly shifts and develops a high energy shoulder which can be attributed to the presence of oxygen-containing functionalities. The spectra shown in Figure 5.2 were obtained using a Shirley background subtraction and fitted with Lorentzian peaks. Comparison of the C 1s and O 1s peak intensities reveals that the O:C ratio at the film surface increases from 12% before activation to 71% after activation. Both the increased surface area for double layer charging and the introduction of pseudocapacitive surface functional groups, are expected to contribute to an increase in the overall capacitance of the film. In addition, improved film and pore wetting has been observed in previous activation experiments, and may further contribute to increased capacitance through increased active surface area [7].

5.2 Electrochemical testing

The effect of electrochemical activation on the galvanostatic charge/discharge behavior is summarized in Figure 5.3. While the unactivated film discharges in about 2.7 s at a constant current of 1 mA/cm^2, the same current density fully discharges the activated film in 42 s, demonstrating the higher overall energy density of the activated film. An extremely small IR drop is seen in both cases, indicative of a low equivalent series resistance, a key consideration for high power applications. The nonlinear shape of the discharge curve is indicative of the capacitive contribution of faradaic redox reactions [1].

CV sweeps confirm the improved capacitive performance of the electrochemically activated film. Figure 4 shows the CV results before and after activation, as measured in KCl and H_2SO_4 electrolyte at a scan rate of 100 mV/s. In both electrolytes, the activated sample shows significantly higher current density than the as-pyrolyzed sample. The specific capacitance is calculated from the CV results via Eq. 2.8 and normalized by the projected area of the film in cm^2. The specific areal capacitance calculated for the activated film as measured in H_2SO_4 is 30 mF/cm^2 at a scan rate of 100 mV/s, revealing a 30x increase with respect to unactivated sample. The corresponding specific volumetric capacitance and energy density are ~ 250 F/cm^3 and 35

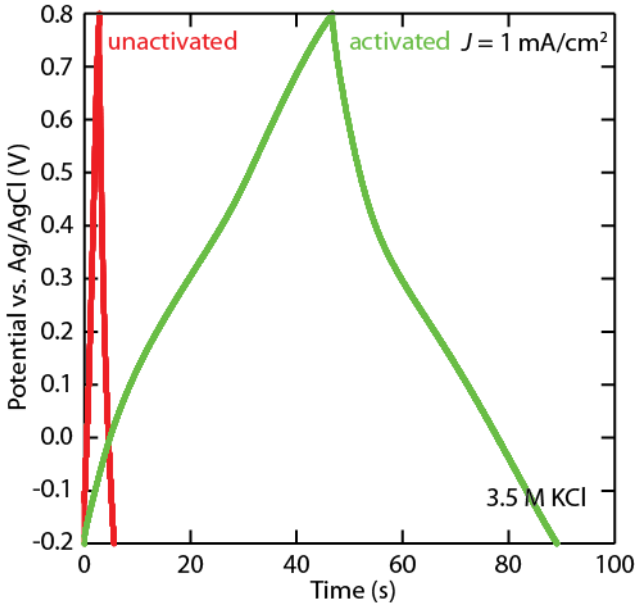

Figure 5.3 Galvanostatic charge/discharge curves for activated and unactivated pyrolyzed photoresist film. Electrolyte is 3.5 M KCl. Current density is 1 mA/cm^2.

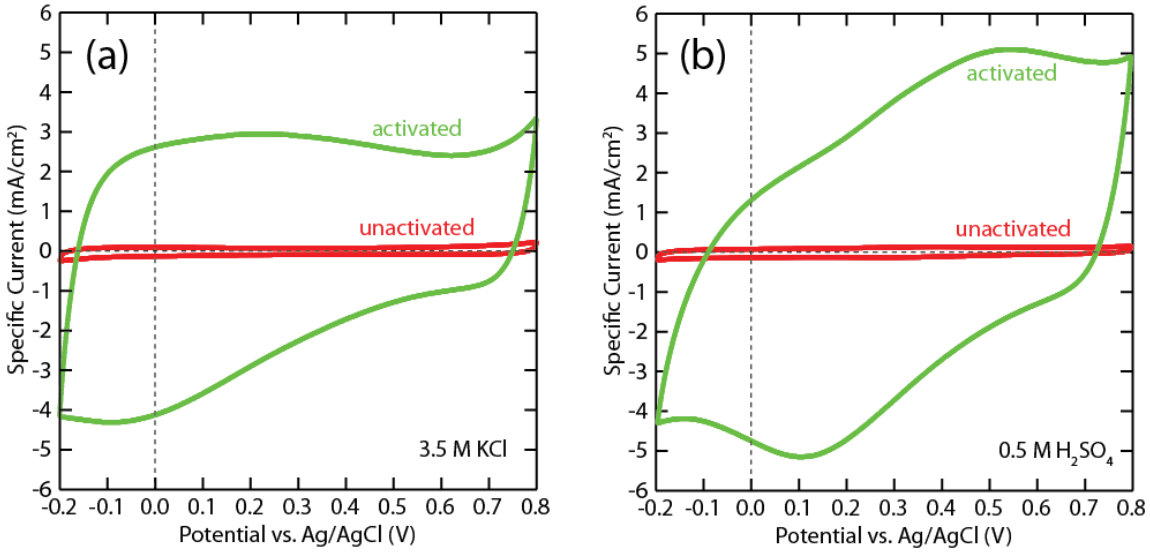

Figure 5.4 Cyclic voltammetry comparison of activated and unactivated pyrolyzed carbon thin film electrodes. (a) CV performed in 3.5 M KCl electrolyte. (b) CV performed in 0.5 M H_2SO_4 electrolyte. Scan rate is 100 mV/s.

mWh/cm^3. The calculated areal capacitance as measured in KCl is 24 mF/cm^2. In comparison to carbon-based electrodes which rely primarily on double-layer capacitance (and not pseudocapacitance), such as graphene/carbon nanotube carpets [27], onion-like carbon [23], and laser-scribed graphene [83], the areal capacitance achieved in this work is larger by an order of magnitude, demonstrating the higher energy storage capabilities of pseudocapacitive electrodes. The capacitance values also compare favorably to other pseudocapacitive carbon microsupercapacitors as in Ref. [62], where a similar pyrolysis and activation procedure is used to fabricate 3D microstructured supercapacitor electrodes from SU-8 photoresist. In their work, a nearly identical areal capacitance of 30 mF/cm^2 was demonstrated for the same scan rate; however, due to the large overall thickness of the 3D microstructure, the achieved volumetric capacitance was ~ 20 F/cm^3, an order of magnitude less than the value demonstrated in this work. This significant deviation likely arises from a difference in pyrolysis procedure as detailed in Ref. [57].

Not only the magnitude of the current is changed in the CV curves through activation, but the shape is modified as well. Before activation, the CV curve is fairly rectangular, indicating nearly ideal capacitive performance. After activation, on the other hand, large peaks are apparent, particularly when measured in the acidic solution, indicating the increased occurrence of faradaic reactions at the electrode surface. These redox reactions are well documented for carbon electrodes and have been attributed to reactions such as [18, 30]:

$$\text{R–C–OH} \leftrightarrow \text{R–C=O} + \text{H}^+ + \text{e}^- \quad (5.1)$$

$$\text{R–COOH} \leftrightarrow \text{R–COO} + \text{H}^+ + \text{e}^- \quad (5.2)$$

These oxygen-containing functional groups, which are formed during electrochemical activation, can be reversibly oxidized and reduced and can hence contribute to pseudocapacitance.

5.3 Comparison between KCl and H_2SO_4 electrolytes

Comparison of the CV curves after activation (shown in Figure 5.4) as measured in the two electrolytes is also instructive: the shape of the CV curve as measured in H_2SO_4 shows a reversible character, with fairly symmetric oxidation and reduction peaks, whereas the measurement in KCl results in a broad reduction peak between -0.2 and 0.3 V without a corresponding oxidation peak of equal magnitude. This electrolyte dependence is can be understood given the participation of hydronium ions in the proposed faradaic reactions. The Nernst equation, which governs the potential of a redox system, can be used to elucidate this phenomenon:

$$\Delta E = \frac{RT}{nF} \ln \frac{a_{\mathrm{O}}}{a_{\mathrm{R}}} \tag{5.3}$$

where ΔE is the shift in reduction potential, R the ideal gas constant, T the temperature, F the Faraday's constant, a_{O} the activity of the oxidant (H^+ in this case), a_{R} the activity of the reductant, and n the number of electrons transferred in the redox reaction. In this case, where the precise nature of the reactions is uncertain, a rigorous quantitative analysis is difficult, but the trend of increasing reduction potential with increasing acidity is, nonetheless, qualitatively clear. Due to this shift in reduction potential in acidic solution, the reversible redox peaks can be clearly seen in the CV sweeps of the samples in 0.5 M H_2SO_4, but not in KCl, where the potential may remain outside the measurement window (further expansion of the CV window is not particularly instructive, as outside of this window, significant water oxidation and reduction begins to occur). Therefore, higher pseudocapacitance can be expected in acidic solutions in comparison to neutral electrolytes. A similar result was observed for voltammogram studies of activated carbon nanotube electrodes in NaCl and H_2SO_4 electrolytes [84].

5.4 Comparison of cycle lifetime in KCl and H_2SO_4 electrolytes

The robust cycle lifetime of supercapacitors is a commonly cited advantage over battery alternatives [1, 35]. This robust performance stems from the purely electrostatic mechanism of charge storage in double-layer capacitors. However, supercapacitors that rely primarily on pseudocapacitive charge storage vary in their cycle performance due to irreversibilities in their faradaic reactions [18, 30]. If the redox reactions that contribute to pseudocapacitance are not completely reversible, a gradual decrease in capacity can be expected. As discussed previously, the electrolyte used can have a significant impact on these phenomena, with the H_2SO_4 electrolyte resulting in a higher reversibility than the KCl electrolyte in the CV analysis. In order to further probe this effect, 10,000 repetitive CV scans were conducted at a scan rate of 100 mV/s in both KCl and H_2SO_4 solutions for the unactivated and activated samples. The capacitance change for each test is plotted in Figure 5.5. For the activated samples (Figure 5.5b), the lifetime test as performed in KCl shows rapid performance degradation over time, with a capacitance loss of nearly 95%, as a result of the irreversibility of the faradaic redox reactions. Superior reversibility in the H_2SO_4 electrolyte results in significantly improved performance stability, which shows a capacitance loss of only 3%. For the unactivated samples, the test in KCl shows good stability, as has been previously reported [57], while the test in H_2SO_4 actually shows an increase in capacitance over 10,000 cycles.

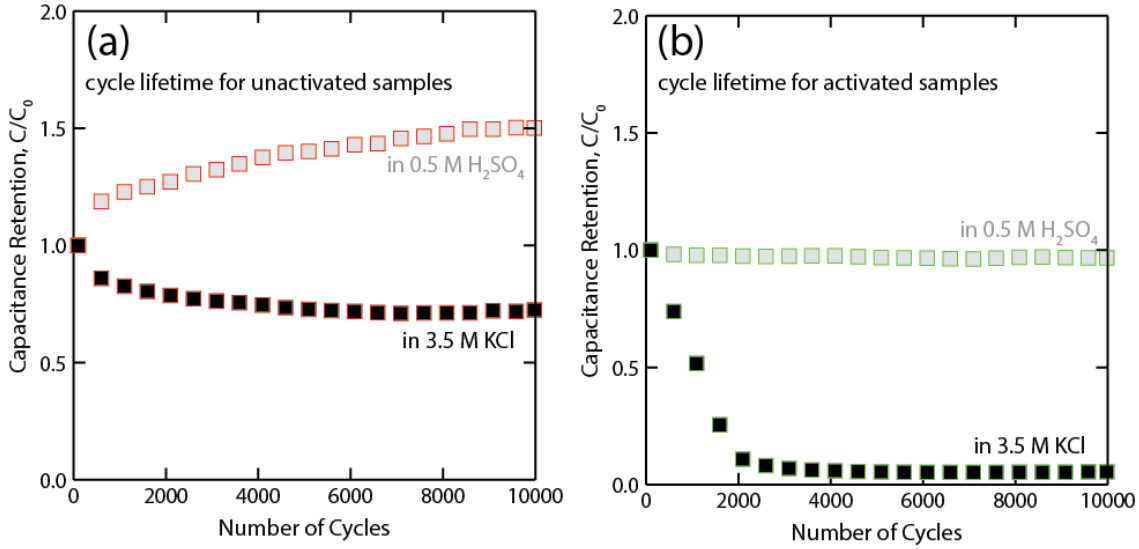

Figure 5.5 Comparison of lifetime cycling tests in 3.5 M KCl and 0.5 M H_2SO_4 for activated and unactivated samples. Capacitance values are calculated from CV data.

In order to probe the sources of the variance in lifetime performance for the activated and unactivated samples in various electrolytes, it is instructive to investigate the progression of the CV shape over the lifetime test. Figure 5.6 shows a superimposition of all 10,000 CV cycles. The observed behavior varies significantly depending on both the electrode and the electrolyte. In the case of lifetime cycling in 3.5 M KCl (Figure 5.6a-b), the current magnitude, and hence the capacitance, decreases for both the unactivated and activated samples, indicating either that the area for double layer charging is decreasing with cycling or that the pseudocapacitive contribution to capacitance is decreasing. Given the more significant decrease in capacitance for the electrochemically activated sample, the latter explanation is likely the primary contributor to the reduction in performance with cycling. As previously discussed, the irreversibility of faradaic reactions in KCl likely results in decreasing pseudocapacitance over many cycles. In contrast, the CV shape and size for the activated sample in H_2SO_4 is remarkably consistent over the duration of the test (Figure 5.6d). Hence, for the electrochemically activated films, the use of an acidic electrolyte not only improves the overall capacitance, but also the cycle lifetime performance due to the contribution of reversible faradaic reactions to pseudocapacitance. For the unactivated samples, the sample in H_2SO_4 is apparently being activated during the test itself through the repeated oxidation and reduction cycles (Figure 5.6c). An increase in the current can be clearly seen throughout the progression the lifetime test, and the shape of the CV curve after 10,000 cycles resembles that of the electrochemically activated samples. Since the voltages used in the lifetime cycling are less than those used in the electrochemical activation, the increase in overall capacitance after cycling is not large (a 50% increase in capacitance over 10000 cycles), but the behavior is nonetheless similar.

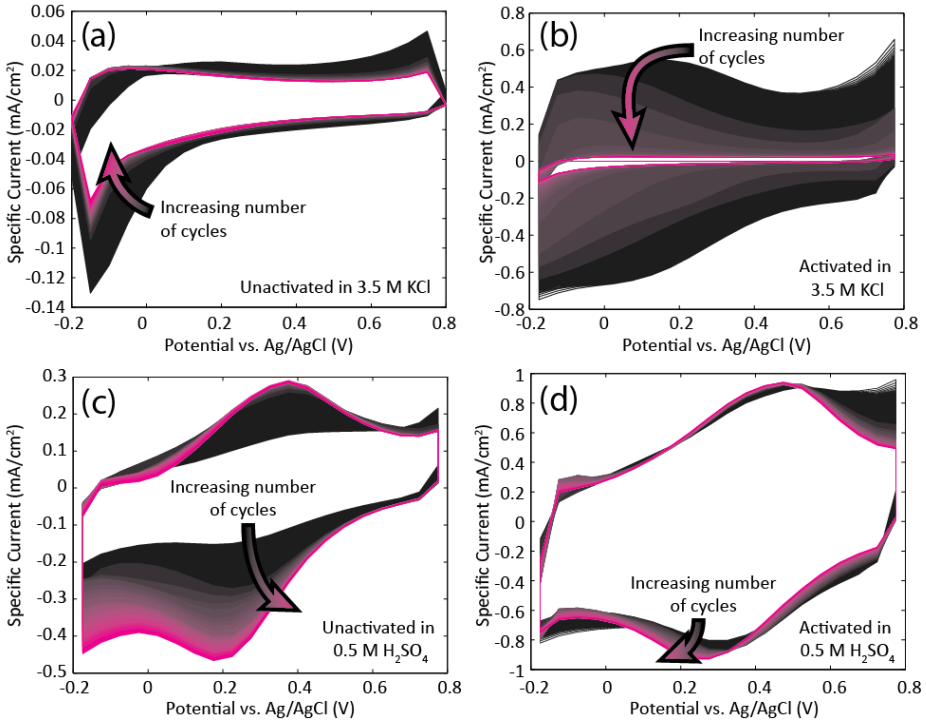

Figure 5.6 The evolution of cyclic voltammograms over 10000 cycles scanned at 100 mV/s for (a) an unactivated electrode cycled in 3.5 M KCl, (b) an activated electrode cycled in 3.5 M KCl, (c) an unactivated electrode cycled in 0.5 M H_2SO_4, (d) an activated electrode cycled in 0.5 M H_2SO_4. The arrows show the direction of increasing cycles.

5.5 Conclusion

In summary, the electrochemical activation of photoresist-derived porous carbon electrodes can yield significantly improved capacitance, but selection of an operating electrolyte is crucial to long term robust performance. A 0.5 M H_2SO_4 medium results in highly improved capacitance as well as lifetime cyclability relative to a 3.5 M KCl solution. This finding may hold true for other activated carbon electrolyte materials including carbon nanotubes and graphene oxide which rely on pseudocapacitive redox reactions, and is a focus of future investigation. The careful consideration of electrolyte and its impact on the long term performance of pseudocapacitive supercapacitors is crucial for the practical application of these types of energy storage devices.

6 Vertically aligned carbon nanotubes electrodes for flexible micro-supercapacitors

The increasing energy demand of future portable devices and the general trend towards miniaturizing electronics is driving increasing research on electrochemical double layer capacitors (EDLCs), commonly referred to as supercapacitors. Supercapacitors are positioned with respect to energy and power densities between traditional batteries and capacitors on the Ragone plot [35]. One key challenge is to integrate such energy storage devices into flexible electronics, such as wearable devices [85] and roll-up displays [86]. Although there has been progress recently on flexible macroscale supercapacitors [87, 40] which consist of two high surface area electrodes with a separator in between, only micro-supercapacitors, characterized by a planar architecture, are prospective candidates for direct on-chip integration with the micro-sensors and microelectronics they are to power [50, 5]. While traditional supercapacitors utilize liquid phase electrolytes, use of solid-state electrolytes would significantly simplify micro-device fabrication and packaging to meet the various needs of next generation portable devices [44]. Ionogels, which consist of ionic liquids in a semi-solid matrix, have been demonstrated to be effective solid-state electrolytes with good mechanical compliance and large electrochemical windows [44, 88, 22] and are hence a promising electrolyte material for solid-state flexible micro-supercapacitors.

Various materials are currently considered for application in flexible electrode structures including activated carbon [89], graphene [83], semiconductor nanowires [90], and polymers [40]. Due to their large effective surface area, favorable electrical properties, and mechanical and chemical integrity [91, 92], carbon nanotubes are also considered as a possible electrode material. Flexible electrodes based on entangled networks of CNTs have been frequently reported [93, 94, 95, 43, 96]. However, only vertically aligned CNTs optimize the morphology of the material for maximum energy and power [97, 98]. Vertically aligned arrays allow for improved electrolyte ion diffusivity into the depth of the electrode material [51], which can improve device power performance [98]. Also, in random networks of CNTs fabricated using wet chemistry, the electrochemically accessible surface area is decreased through nanotube bundling, while in VACNT arrays, typically dry processed, the electrolyte is expected to access the entire axial length of individual CNTs. This allows a larger proportion of the surface to be in contact with the electrolyte ions, resulting in higher energy density [99, 100]. Another argument in favor of VACNTs is that the mechanical integrity along the tube axis enables the design of truly 3-dimensional electrode patterns, which is critical for micro-supercapacitors as the areal footprint is of primary importance. Furthermore, the cost of CNTs has decreased consistently in the past and this trend is expected to continue with the mass production of CNTs on an industrial scale [101] making CNTs increasingly viable for commercial application.

A limiting factor with the VACNT-based structures is given by the low electrical conductivity perpendicular to the nanotube axis, typically in the range of only a few S cm^{-1} [102]. For rigid planar supercapacitors, the poor conductivity has been addressed by growing VACNTs on optimized catalyst layers to decrease the resistance [52] or by incorporating a graphene layer between the VACNTs and the Ni current collector to reduce the contact resistance [27].

However, these techniques present significant fabrication and transfer challenges for scalable fabrication of flexible microdevices. Recently, Chen et al. demonstrated fabrication of interdigitated electrodes by transferring pre-patterned VACNT electrodes with a sputtered Au current collector to a flexible substrate [103, 104]. However, this technique lacks the scalability required for high volume manufacturing due to the tedious metal catalyst patterning and manual Scotch® tape transfer process. Moreover, the reliability under mechanical fatigue tests of such taped devices is not reported and may be limited due to possible poor substrate/electrode adhesion.

In this study, we take advantage of a laser-assisted dry transfer technique [105] to fabricate a VACNT-based flexible micro-supercapacitor in a scalable and cost effective way. A thin film of sputtered Ni is used to enhance the in-plane electrical conductivity of the VACNT electrodes and an ionogel is used to create a fully solid state device. Benefiting from the superior mechanical flexibility of both the patterned electrodes and the ionogel electrolyte, our all solid-state micro-supercapacitors show promising energy and power performance even under significant mechanical bending strain.

6.1 Fabrication techniques

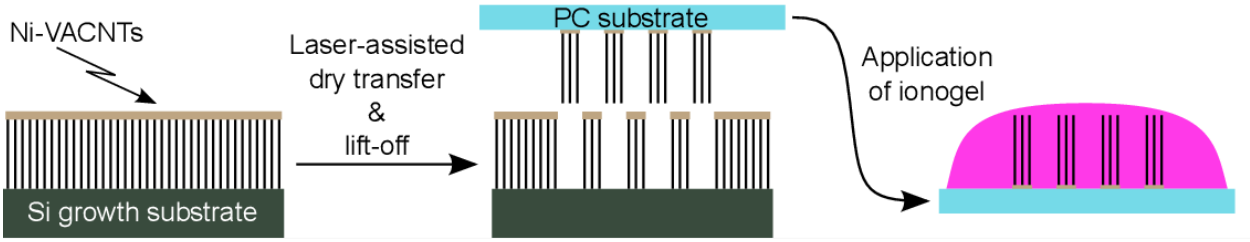

Figure 6.1 Schematic illustration of device fabrication (side view): VACNTs are grown by chemical vapor deposition on a Si substrate and a Ni layer is sputtered on top of the VACNTs. Interdigitated Ni-VACNT electrodes are simultaneously patterned and transferred onto flexible polycarbonate substrate by a laser-assisted dry transfer. In the last step the ionogel is applied on the patterned electrode structures, completing the micro-supercapacitor fabrication.

Figure 6.1 outlines the overall device fabrication steps. The interdigitated electrodes were prepared by first growing a film of vertically aligned CNTs with a chemical vapor deposition (CVD) process. This step was followed by sputtering a thin Ni layer on top of the VACNTs, to improve the in-plane electrical conductivity. Then, a laser-assisted dry-transfer process was used to transfer the patterned Ni-sputtered VACNTs (Ni-VACNTs) onto a flexible polycarbonate (PC) substrate. In the last step, an ionic-liquid gel (ionogel) is applied onto the patterned electrodes to yield the final flexible micro-supercapacitor device reported herein. The details are described below.

6.1.1 Ni-VACNT electrode fabrication

The multi-walled VACNTs used in this study were grown using a CVD process as previously described in detail [106]. Briefly, a buffer layer was prepared by RF sputtering of 15 nm alumina on a Si (100) wafer (Edwards Auto 306). Subsequently, a 4 nm Fe catalyst layer was deposited by e-beam evaporation (Edwards EB3). The wafer was then cleaved with a diamond scribe into individual pieces (1.5×1.5 cm^2), which were then loaded into a high temperature tube furnace (Lindberg Blue M). The furnace was operated at ambient pressure and all gases used were of

ultra high purity grade (99.999%). To remove air and residual moisture, the tube was purged for about 10 min with 400 SCCM Ar. Then the Ar mass flow was reduced to 220 SSCM and the system was heated to 740 °C within 14 min. Upon reaching 450 °C, H_2 was added into the system at a mass flow rate of 80 SCCM. Following this heat-up phase, the catalyst was annealed for 15 min at 740 °C. Finally, 200 SCCM C_2H_4 was introduced into the system to trigger the growth of carbon nanotubes. The growth conditions were maintained for 120 s to produce multi-walled VACNTs of 50 ± 2 μm in height. This film thickness was measured using optical microscopy and confirmed by scanning electron microscopy (SEM, LEO 1550) and proved to be optimal for the subsequent laser transfer.

In order to increase the in-plane electrical conductivity of the VACNTs without losing the intrinsic vertical alignment of the individual nanotubes, a layer of Ni was DC sputtered (Edwards Auto 306) on top of the previously grown VACNT forest. The nominal thickness of the Ni layer was about 350 nm, which was measured using SEM on a Si (100) substrate simultaneously coated. The Ni-VACNTs were then patterned and transferred with a laser-assisted dry transfer technique on PC sheets (125 μm thickness) as reported previously [105]. The advantage of this laser-assisted dry transfer was its speed and customizability due to the fact that no photolithographic mask was needed. Instead, the pattern was written by selectively directing the beam of a continuous Ar ion laser (λ=514 nm, Lexel 3000) with a galvanometer mirror system (Scanlab hurryScan II 14) on the Ni-VACNT substrate, on which the sheet of PC had been placed. Laser scanning was conducted at a speed of 1 mm s^{-1} with a laser power of 38 mW.

6.1.2 Ionogel preparation

The ionogel preparation closely followed the procedure in Ref. [88]. All samples were prepared in a N_2 rich, low humidity environmental chamber (<0.2% relative humidity) to reduce the presence of water. This is because the samples prepared in ambient conditions showed undesirable electrochemical behavior at high voltages (> 1 V) due to water electrolysis. Tetramethyl orthosilicate (TMOS, Sigma-Aldrich, 99.999% purity), formic acid (FA, Alfa Aesar, 97% purity), and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMI TFSI, Iolitec, 99% purity) were mixed in a 1:6:6 molar ratio (TMOS:FA:EMI TFSI) in a glass vial. This ratio was selected for its high ionic liquid content and good mechanical properties [88]. The mixture was mechanically stirred for 5 minutes. A small amount (~ 5 μL) of the mixture was transferred via micropipette onto the patterned Ni-VACNT sample. The mixture was allowed to gel for over 24 hr in the environmental chamber.

6.1.3 Characterization

As electrolyte wettability of the electrode is a key consideration for supercapacitors, the static contact angle of the ionogel (and, for reference, of deionized water) on VACNTs was measured using a goniometer (Rame Hart 100). The contact angle of the ionogel mixture was measured before gelation.

Electrochemical tests were performed in a N_2 rich, low humidity environmental chamber using a potentiostat (CH Instruments, 660D Model). Cyclic voltammetry (CV) is used to determine specific capacitance. A potential window of 0 to 3 V was tested at various scan rates (ranging from 0.1 to 500 V s^{-1}) to probe the rate dependence of the device. Constant-current charge and discharge cycles were performed to quantify the equivalent series resistance (ESR) of the device

through the IR drop [24]. AC impedance spectroscopy (potential amplitude of 5 mV) was used to probe the frequency response of the device.

6.2 Results & Discussion

6.2.1 Ni-VACNT electrodes

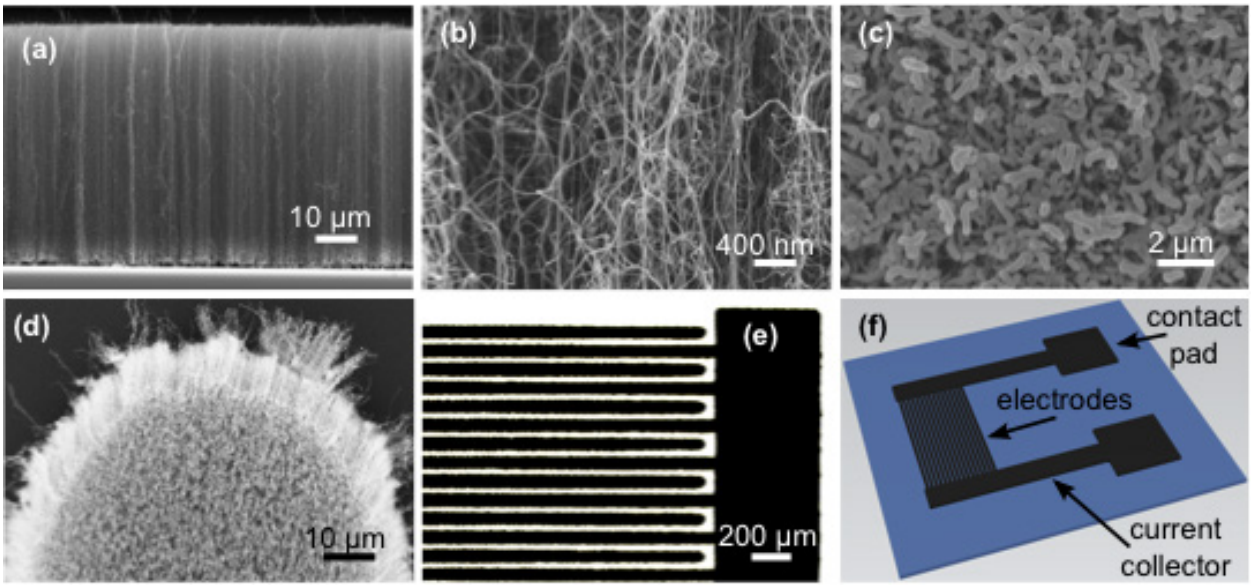

Figure 6.2 (a) SEM side-view of transferred Ni-VACNTs on PC substrate; (b) side-view close-up showing entanglement; (c) SEM top-view of sputtered Ni-VACNTs before transfer; (d) SEM top-view of a transferred line; (e) Optical microscopy top-view of interdigitated lines; (f) Illustration of interdigitated electrodes including the side current collectors and the contact pads.

Figure 6.2a,b shows SEM side-view images of transferred Ni-VACNTs on a PC substrate. The VACNTs remain well aligned after transfer. The Ni layer, located at the interface with the PC, infiltrated the nanotube forest to a depth of a few micrometers. In Figure 6.2b, strong entanglement is observed which stems from the CNT growth by the CVD process. A top view of the sputtered Ni on the VACNT forest is given in Figure 6.2c, showing that the Ni is deposited on the top of the VACNTs not as a complete film, but rather connecting adjacent CNTs at the tips. Each interdigitated finger corresponds to a single pass of the laser, whose beam shape causes the rounded finger ends seen in Figure 6.2d,e. The 16 fingers (8 per electrode) are about 65 µm wide and 3 mm long, with a center-to-center distance between two neighboring fingers of 100 µm. The thickness of the array is 48-52 µm. The entire laser scanning process for the interdigitated fingers takes about 48 s. A model of the complete transferred pattern is shown in Figure 6.2f. This illustration also includes the contact pads to which electrical contacts were made using silver epoxy.

To probe the effect of the Ni layer, the electrical conductivity of transferred VACNT lines with a high length to width ratio of > 10,000 were measured by two-point technique with a semiconductor parameter analyzer (HP 4155A). The I-V curves yielded an ohmic response, resulting in an in-plane electrical conductivity on the order of 5 S cm^{-1} for the Ni-VACNT lines. This represents an improvement by about one order of magnitude in comparison to the conductivity values measured on plain VACNT lines, indicating that the metallic Ni layer

significantly improves in-plane conductivity. A more detailed characterization of the transport properties is currently ongoing.

6.2.2 Contact angle

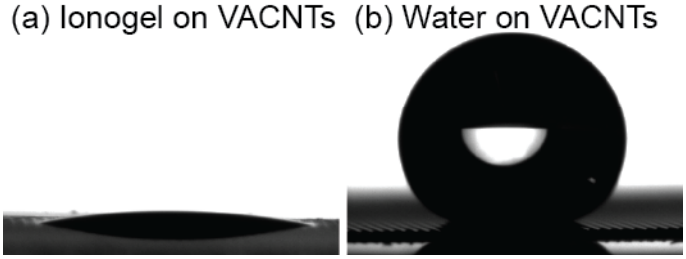

Figure 6.3 Images of (a) ionogel mixture (before gelation) and (b) deionized water droplets deposited on VACNT array. Ionogel shows much higher wetting affinity than deionized water.

VACNTs pose an organized, heterogeneous surface with nanoscale roughness and the static contact angle of water droplets placed on the CNT forest can achieve high values [107, 108]. The static water contact angle was measured to be 160° indicating the superhydrophobic characteristic of the VACNTs (as seen in Figure 6.3). In contrast, the ionogel mixture before gelation featured a contact angle of 20°, indicating favorable wetting of the VACNTs by the ionogel. These results highlight that, in the case of VACNTs and other hydrophobic electrode materials, EMI TFSI ionic liquid based electrolytes yield in a much higher electrode/electrolyte interfacial layer and hence higher capacitance than their aqueous counterparts.

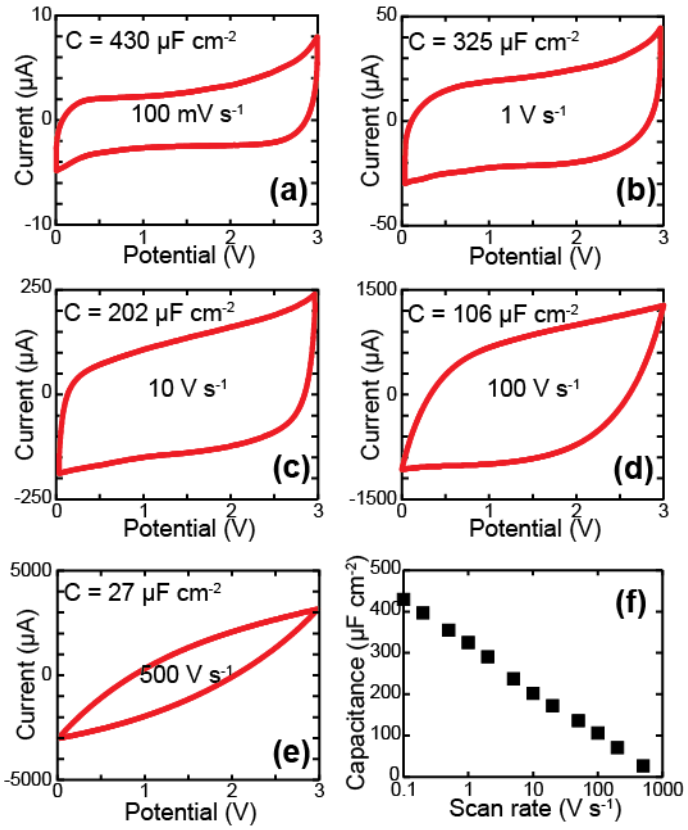

Figure 6.4 (a-e) Cyclic voltammograms of fabricated VACNT-on-PC micro-supercapacitors with TMOS:FA:EMI TFSI ionogel electrolyte at various scan rates. (f) Capacitance dependence on scan rates shown on a semilog plot.

6.2.3 Cyclic voltammetry

The fabricated Ni-VACNT micro-supercapacitor was subjected to cyclic voltage sweeps at various scan rates, and the results are summarized in Figure 6.4. Fairly rectangular CV sweeps are obtained at scan rates up to 10 V s^{-1}, showing good capacitive behavior even at comparably high scan rates. At low scan rates, an anodic peak is apparent at high voltages. The presence of this peak points to rate limited charge transfer at the electrode/electrolyte interface. We speculate that this charge transfer arises in part from the reaction of residual water in the ionogel. A close examination of Figure 6.4a shows the onset of increasing current to occur around 1 – 1.5 V (increasing further at higher potentials), the expected potential at which aqueous electrolytes begin to react [35]. There is also a reduction peak present at low potentials, which may arise from the reversible reduction of nickel oxides, which has been shown to contribute to pseudocapacitive charge storage [109]. Further elucidation of the electrochemical behavior is ongoing.

The specific capacitance, C, can be calculated via the equation, $C = I_{avg}/sA$, where I_{avg} is the average current magnitude of the cathodic and anodic sweeps, s is the voltage scan rate, and A is the projected area of the whole interdigitated zone (0.064 cm^2), including electrodes, current collector next to the interdigitated electrodes, and gap. A volumetric specific capacitance can also be determined by further dividing by the thickness of the VACNT array, 50 μm. Specific areal capacitance is plotted in Figure 6.4f as a function of scan rate. The rounding off of the

voltammogram edges and the decrease in capacitance at high scan rates (about 110 μF cm^{-2} per decade) are likely due to limitations arising from the resistance of the VACNT arrays and the contact resistance, which is ameliorated by the sputter-deposition of Ni film prior to transfer; films transferred without sputtering show significant rounding off even at scan rates below 5 V s^{-1}. The contribution of long ion diffusion lengths along the nanotube axial direction may also contribute to the reduction in capacitance at high scan rates, particularly given the long nanotubes used in this study relative to those reported in Ref. [27] (50 μm vs. 10-20 μm). A recent theoretical study by Wang and Pilon shows that for double-layer capacitors, sufficiently low CV scan rates yield capacitance values which are independent of scan rate, and can be considered the intrinsic capacitance [110]. However, in the "diffusion limited" regime, the capacitance drops off sharply with increasing scan rate, showing a logarithmic decay similar to that observed in Figure 6.4f. The onset of this regime depends on factors including the ionic diffusion constant and the electrode thickness and resistivity, where low diffusion rate and high resistivity lead to fast drop off of capacitance with scan rate [110]. The fabricated VACNT device is possibly in this "diffusion limited" regime at all measured scan rates, but this analysis does not reveal whether the rate limitations are caused by high electrode resistance or by resistance to ionic transport. The kinetic limitation of pseudocapacitive reactions may further augment this sharp dropoff of capacitance with scan rate. Further quantitative comparison is made in the AC impedance spectroscopy analysis (Section 6.2.5).

The calculated specific capacitance of the device is 430 μF cm^{-2} (86 mF cm^{-3}) for a scan rate of 0.1 V s^{-1}, lower than the results obtained for recently reported CNT-based micro-supercapacitors (3.93 mF cm^{-2} electrode area, calculated to be ~2.7 mF cm^{-2} device area) which used a graphene-on-Ni current collector and a liquid phase electrolyte, but were fabricated on a rigid Si substrate via a more complex, multi-step synthesis technique [27].

6.2.4 Constant current charge/discharge

Figure 6.5a,b shows the charge/discharge curves for the fabricated device at a variety of currents (device area = 0.064 cm^2). The discharge curve is quite linear, with a minimal IR drop visible at the start of each discharge curve. At higher scan rates, the IR drop becomes more apparent. The slight curvature clearly visible in the charging curve and partially visible in some of the discharge curves arise from pseudocapacitive charge transfer, as detailed in the CV discussion. The magnitude of the potential drop can be used to estimate the device equivalent series resistance (ESR) [24], which is calculated to be 450 Ω (29 Ω cm^2) for the fabricated device. As previously discussed with regards to the CV results, this fairly large ESR is likely due to the resistance of the Ni-VACNT film (resistivity of ~ 0.2 Ω·cm). The sputtered Ni film was instrumental in bringing the ESR down from > 5000 Ω for a similar device without Ni. Additional investigation is ongoing in order to further reduce the ESR and achieve higher power performance. The specific capacitance can also be calculated from the charge/discharge using Eq. 2.11. The specific areal capacitance as a function of current density is given in Figure 6.5c, showing similar capacitance values as the CV results.

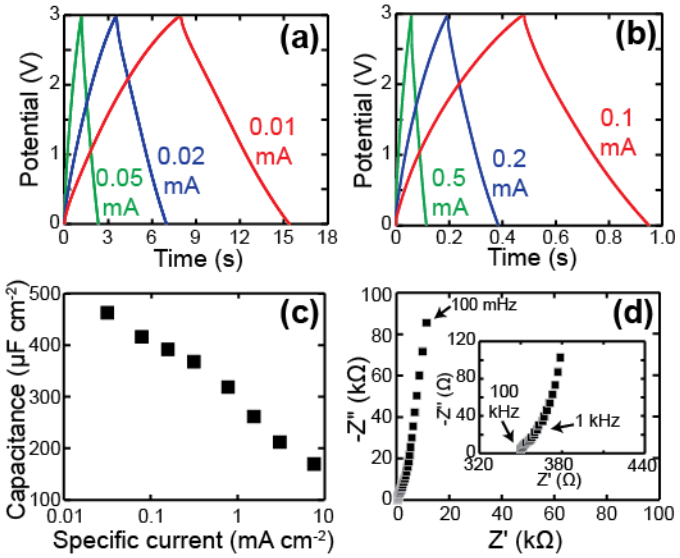

Figure 6.5 (a,b) Galvanostatic charge/discharge curves for fabricated Ni-VACNT supercapacitor for a variety of currents. (c) Capacitance values calculated from discharge curves plotted against specific areal current. (d) Nyquist plot of AC impedance data; inset shows the high frequency behavior.

6.2.5 AC impedance spectroscopy

AC impedance spectroscopy was used to probe the frequency response of the fabricated device. Figure 6.5d shows the Nyquist plot for this device, which displays the typical semi-vertical plot of a double-layer capacitor. The impedance at the high frequency limit gives an approximation for ESR and is measured to be ~ 350 Ω, in reasonable agreement with the charge/discharge results. This ESR, again, is likely dominated by the resistivity of the VACNT array. The frequency at which the phase angle crosses -45° is frequently cited as a figure of merit describing the frequency response, with higher frequency denoting faster device switching. For this device, the frequency at -45° is 47 Hz. This fast frequency response is comparable to laser-scribed graphene flexible micro-supercapacitors (30 Hz) [22]. Given the significant improvement in power performance effected by Ni deposition, it is likely that further improvement could result from optimization of this process, in order to reduce the film and contact resistance.

6.2.6 Flexibility testing

The capacitive performance under flexion was tested through a variety of methods. First, the fabricated device was conformally wrapped around cylinders of known radii and tested in the flexed configuration. The CV results are plotted in Figure 6.6a and show minimal change in all configurations, demonstrating good performance under flexion. In addition to performing under flexion, flexible devices are expected to operate under repeated bending cycles as tested in mechanical fatigue tests. A second test thus involved repetitive mechanical bending of a device geometry simplified for ease of measurements. The simplified device was constructed of two parallel Ni-VACNT lines with a pitch of 100 µm. The ionogel was deposited on a small area on and between the VACNT lines, creating a simple supercapacitor over 3 mm of the two parallel lines. The lines were electrically contacted to the potentiostat with silver paint and copper clamps. One clamp was fixed, while the other was attached to a linear motor with an initial clamp-to-clamp distance of 9.8 mm. A picture of the setup is shown in Figure 6.6b. As the mobile clamp moved towards the fixed clamp, the sample buckled along the central axis, where the ionogel was located, inducing a significant bending primarily along the device area. In this flexing geometry, the buckling behavior of the PC substrate creates areas of high local stress in contrast to the distributed stress of the circular bending test. In order to test the device performance under this buckling behavior, the clamp-to-clamp distance was cycled 1000 times to 85% of the original distance and back to an unbent position. The capacitance and ESR was measured periodically in the unbent position via galvanostatic charge/discharge and are plotted as a function of cycle number in Figure 6.6c. A capacitance retention of over 90% was found over the full 1000 bending cycles. This impressive retention is promising for device applications which involve repeated bending and unbending, and has not been demonstrated in other reported solid-state flexible micro-supercapacitor materials such as laser-scribed graphene and ionogel based devices [22].

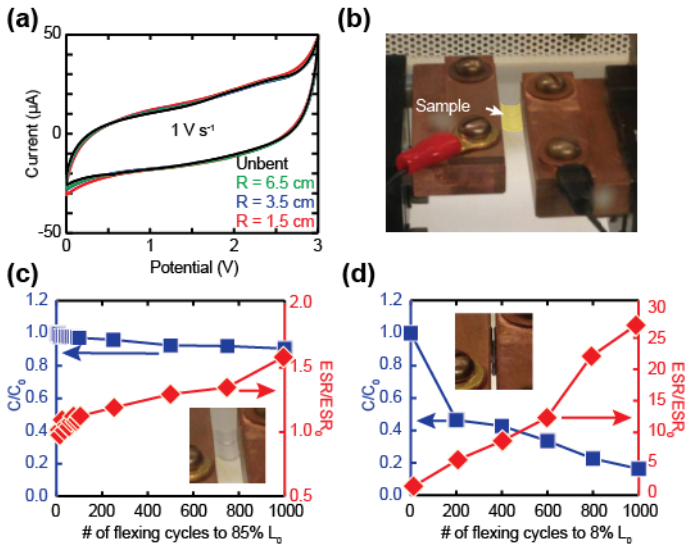

Figure 6.6 (a) Cyclic voltammograms of fabricated VACNT/ionogel micro-supercapacitor bent around cylinders of various radii. CV plots overlap well, demonstrating good flexing performance. (b) Picture of repetitive cycling test setup with sample highlighted in yellow. (c,d) Relative capacitance and ESR as a function of number of bending cycles to 85% and 8% of original sample length (9.8 mm). Insets show pictures of device at maximum bending.

A 50% increase in ESR can be seen during mechanical cycling, likely due to the high local stresses exerted on the interface of the Ni-VACNT and PC substrate during buckling and a resulting increase in contact resistance. This increasing resistance likely has a significant effect on the observed decrease in capacitance. In order to test the failure point of the device, the sample was almost completely folded (a clamp-to-clamp distance 8% of the original value) and unfolded 100 times. Impressively, the device still functions after this extreme bending, albeit with a significantly reduced capacitance (see Figure 6.6d). We attribute this highly promising behavior under mechanical fatigue tests to the strong interfacial adhesion, both between the Ni-coated nanotubes, the PC substrate and the ionogel.

6.2.7 Energy and power density

The energy, E, and power density, P, can be calculated from the charge/discharge data via Eqs. 2.22 and 2.24 [27]. The areal energy density calculated for the fabricated device is 0.1-0.5 μWh cm^{-2} with a maximum power density of about 10 mW cm^{-2}. VACNTs on graphene-on-Ni current collectors in ionic liquid show higher energy and power densities (1.0-4.8 μWh cm^{-2} and ~100 mW cm^{-2}, respectively, per electrode area) [27], but must be fabricated on a rigid substrate. Flexible, all solid state micro-supercapacitors fabricated via laser-scribing of graphene oxide yield 1.0-1.6 μWh cm^{-2} and ~100 mW cm^{-2} using ionogel electrolyte [22]. Therefore, comparison to these state-of-the-art micro-supercapacitors show slightly lower energy and power densities for our Ni-VACNT flexible device, realized with a facile, scalable fabrication process. However, the promising mechanical stability of the proposed device, particularly under repeated bending cycles, is nonetheless promising for future flexible device applications.

6.3 Conclusion

In summary, all solid-state flexible micro-supercapacitors were fabricated with a facile and scalable method using VACNT electrodes with an ionogel electrolyte on a flexible PC substrate. The VACNTs were patterned and transferred in a single maskless step using a laser-assisted dry transfer process. An additional sputtered Ni layer was used to improve device power performance in an inexpensive way. The fabricated device yielded good energy and power performance and was highly flexible. The electrochemical properties were preserved under bending and a high capacitance retention was demonstrated over a large number of mechanical fatigue test cycles. This novel combination of electrode materials and solid-state ionogel electrolyte shows significant promise for flexible microdevice energy storage applications.

7 3D templated graphene electrodes for supercapacitors

3D graphene architectures have been proposed for a variety of applications, including chemical sensing, catalysis, hydrogen storage, and electrochemical energy storage [111]. The assembly of 2D graphene sheets into 3D structures is attractive for these applications due to the high conductivity of graphene and the high specific surface area and good mass transport provided by a 3D network. For supercapacitor applications, in particular, the 3D graphene is desirable as an electrode material, due to its high porosity (good ion transport) and high electrical conductivity (good electrical transport), as well as its high surface area to mass ratio. Additionally, the carbon is amenable to surface modification and active material deposition, which can increase the total energy density through pseudocapacitive reactions [7, 112]. Previous efforts to fabricate 3D graphene structures are reviewed in Ref. [111] and include the growth of graphene via chemical vapor deposition (CVD) on commercial Ni foams [113, 114, 115] and the self-assembly of graphene oxide flakes onto sacrificial polymer microsphere templates [116, 117, 118]. The former technique provides the advantage of relatively pristine graphene growth using CVD but yields a moderate specific surface area due to the large (~100 μm) pore size of commercial Ni foams, while the latter allows for controlling pore size distribution through microsphere size selection but yields an incompletely reduced graphene. In both cases the template material (Ni foam, polymer spheres) can be removed to yield a lightweight, conductive, porous carbon material which can be used as a supercapacitor or battery electrode with good electrochemical performance. Moreover, these materials can be used in the absence of binders, conductive fillers, or additional current collectors, which increases the proportion of electrochemically active material in a device. In this chapter, a novel method is described to combine these two techniques to fabricate a bicontinuous 3D graphene foam of controlled geometry through CVD graphene growth on a templated electrodeposited Ni scaffold. As a practical demonstration of the utility of the technique, the resulting material is then tested as a supercapacitor electrode material.

7.1 Methods

Fabrication of the free-standing 3D graphene foam consists of 4 steps and is schematically illustrated in Figure 7.1. First, a 3D opaline array of polystyrene (PS) microspheres is deposited onto a substrate. Second, Ni is electrodeposited onto the sample and the PS is removed to form a reverse-opal scaffold (inspired by Ref. [119]). Third, graphene is deposited onto the Ni scaffold via CVD. Finally, the Ni is etched to yield a free-standing foam composed of conjoined hollow graphene spheres.

7.1.1 Substrate preparation

100 nm of Ni (with a 5 nm Ti adhesion layer) is deposited onto a 6” Si wafer via e-beam evaporation (Thermionics VE-100). The wafer is diced into 1.5 cm × 1 cm chips and cleaned with ultrasonication in acetone followed by sequential rinses with isopropyl alcohol and deionized water.

7.1.2 Polystyrene microsphere deposition

Numerous methods exist for the controlled deposition of microspheres into closely packed arrays on planar substrates [120, 121]. For thin depositions of spheres (1-8) layers, a Langmuir-Blodgett

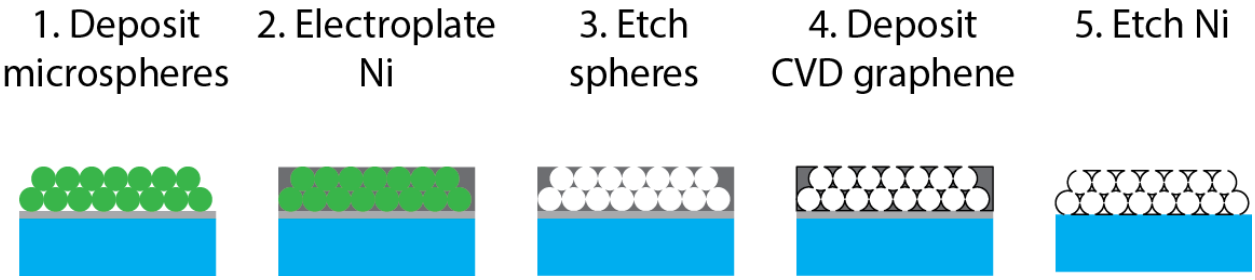

Figure 7.1 3D templated graphene electrode fabrication.

sequential dip coating process is used for good control of the number of layers [122, 123]. Polystyrene spheres (Thermo Scientific) are diluted to a 0.1 wt% colloidal suspension in a 1:1 by weight ethanol to deionized (DI) water ratio. The sample is partially immersed into a beaker filled with water and the diluted suspension is deposited onto the water surface via micropipette. A drop of sodium dodecyl sulfate is used to pack the surface spheres into a close packed array. The sample is slowly withdrawn from the beaker, leaving a monolayer of spheres on the Ni surface. The sample is annealed for 3-5 minutes at ~95 °C on a hot plate, and the deposition is repeated to achieve the desired number of layers. Each sample is then annealed for at least 20 min at 95 °C to improve adhesion before Ni electrodeposition.

7.1.3 Ni electrodeposition

A high throwing power Ni sulfate bath (composed of 30 g/L $NiSO_4$ hexahydrate, 38 g/L $NiCl_2$ hexahydrate, 180 g/L anhydrous $NaSO_4$, and 25 g/L boric acid) is prepared for electrodeposition [124]. The deposition is performed with stirring at room temperature, using a deposition current of 1-3 mA/cm^2 and a Ni wire counter electrode. After deposition of the desired amount of Ni, the sample is immersed in tetrahydrofuran for 10 minutes to dissolve the polystyrene spheres.

7.1.4 CVD graphene growth

The high temperatures (1000-1050 °C) used in typical CVD graphene growth with a CH_4 precursor [113, 114, 115] are unsuitable for this technique, as the reverse opal electrodeposited structure is found to collapse at temperatures > 600 °C. Therefore, a lower temperature liquid precursor, benzene, is used to deposit graphene at 600 °C [125]. After loading the sample into the center of a hot-wall CVD tube furnace, a crucible with 1 mL benzene is placed near the inlet. The crucible is covered with aluminum foil, and a small hole is poked in the foil. After a 10 min Ar purge (at ambient pressure), the temperature is raised to 600 °C and held for 2 min under continuously flowing Ar. The sample is then allowed to cool slowly (~ 12 °C /min) to give a thicker graphene deposition, which gives sufficient mechanical stability for a free-standing foam, without polymer supports required for transfer [115]. After deposition, the Ni is etched overnight in concentrated HCl. After etching, the carbon foam floats to the surface, where it is scooped up by an arbitrary substrate (polycarbonate sheets in this case).

7.1.5 Electrochemical testing

Electrical connection to the foam is made via silver epoxy. The silver epoxy is coated with a nonconducting resin to prevent contact with the electrolyte. Three electrode testing (Pt counter, Ag/AgCl reference) is performed using a CH Instruments potentiostat in an aqueous 3.5 M KCl electrolyte. Cyclic voltammetry (CV), galvanostatic charge/discharge, and AC impedance spectroscopy are used to determine the electrochemical properties of the foams.

7.2 Results and discussion

7.2.1 Material characterization

Scanning electron microscopy (SEM) is used to examine the morphological characteristics of the material during the fabrication process. Figure 7.2a-e shows representative SEM images of the deposited polystyrene sphere template, the Ni scaffold, and the carbon foam after Ni removal. The PS sphere array shows an imperfect opal packing of spheres. Since the resulting graphene takes on the approximate shape of these spheres, improvement of crystalline packing would likely yield improved specific surface area and is an area for further optimization. Nonetheless, the resulting foam shows a good fidelity reproduction of the original sphere template. The visible pores in the hollow graphene spheres represent the area of contact between the original PS spheres and are crucial for allowing good ion transport and utilization of both "sides" of the graphene spheres. This pore size can be tuned through electropolishing, as presented by Zhang et al. [119], but no polishing is performed in this work. The hollow graphene spheres also show variation in thickness along the shell of the sphere, suggesting a polycrystalline growth of multilayer graphene.

Raman spectroscopy is used to confirm the graphitic nature of the carbon network. Figure 7.2f shows a representative Raman spectrum that displays the signature G and 2D peaks of graphitic carbons. The large G to 2D intensity ratio indicates multilayer graphene [126], and the presence of a D peak indicates defects in the graphitic carbon. Although Li et al. showed minimal D peak intensity for graphene grown on Cu foils using benzene at a growth temperature as low as 300 °C [125], in this work, the D peak is present even at growth temperatures of 600 °C. This difference is likely due to the relatively low quality of electrodeposited Ni compared to Cu foils. The optimization of Ni electrodeposition is an area for possible future study.

7.2.2 Electrochemical characterization

Cyclic voltammetry at a variety of scan rates was performed on all fabricated foams. A representative CV cycle is shown in Figure 7.3a. A semi-rectangular plot can be seen with slight

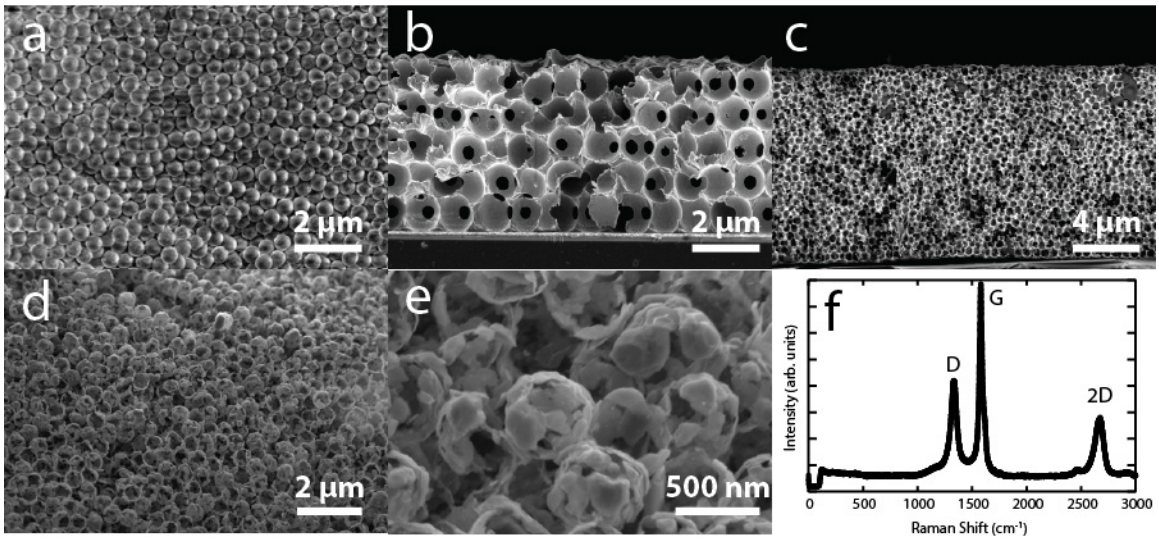

Figure 7.2 SEM images of a) top view of polystyrene spheres, b,c) cross-sectional view of Ni scaffold, d,e) hollow graphene spheres. f) Raman spectrum of 3D graphene foam.

features visible at 0.2-0.5 V vs. Ag/AgCl in both the cathodic and anodic scan. These features likely represent the reversible oxidation and reduction of residual Ni that was not fully removed during the HCl etch. Galvanostatic discharge plots (Figure 7.3b) show similar results; a pseudo-linear discharge curve is apparent with slight non-linearity apparent at similar potentials as the features seen in CV. The specific capacitance of the foams can be calculated via Eq. 2.8 and normalized by the projected area of the sample. The volumetric capacitance can be calculated by dividing by the thickness of the foam. Figure 7.3c,d show the calculated areal and volumetric capacitances for all fabricated samples. The areal capacitance (capacitance per unit of *projected* surface area), C_A, can be calculated from the intrinsic specific capacitance (capacitance per unit of *real* surface area), C_i, from

$$C_A = C_i A_A n \tag{7.1}$$

where A_A is the real surface area of the foam per projected area per layer and n is the number of sphere layers. Assuming utilization of the full inside and outside surface of the hollow graphene spherical shell, and neglecting the area of the pores in the shell, A_A is simply two times the surface area of a sphere of diameter d, divided by the projected area of the same sphere, multiplied by a packing fraction, which for close-packed circles is $\pi/\sqrt{12}$,

$$A_A = \frac{2(\pi d^2)}{\pi d^2/_4}\left(\frac{\pi}{\sqrt{12}}\right) = \frac{4\pi}{\sqrt{3}} \tag{7.2}$$

Since C_i is a constant, and A_A is a constant, C_A is linearly dependent on n. In contrast, the volumetric capacitance, C_V, is given by

$$C_V = \frac{C_A}{t} \tag{7.3}$$

where t is the film thickness. For a close packed sphere array, the thickness of the film is given by

$$t = d\left(1 + n\frac{\sqrt{6}}{3}\right) \tag{7.4}$$

Therefore,

$$C_V = \frac{\frac{4\pi}{\sqrt{3}} C_i\, n}{d\left(1 + (n-1)\frac{\sqrt{6}}{3}\right)} \tag{7.5}$$

which, for large n, simplifies to

$$C_V \approx \frac{\frac{4\pi}{\sqrt{3}} C_i\, n}{dn\frac{\sqrt{6}}{3}} = \frac{4\pi}{\sqrt{2}}\frac{C_i}{d} \qquad 7.6$$

Hence, from simple geometric considerations, assuming close-packed arrays, the areal capacitance is expected to increase linearly with the number of layers (holding sphere diameter constant) and to be independent of the sphere diameter. In contrast, the volumetric capacitance is expected to remain nearly constant with number of layers and decrease linearly with increasing sphere diameter. These trends are qualitatively reflected in the results. The highest measured areal capacitance is expected to be achieved on the samples with the most layers (regardless of sphere size), and the 7 layer, 1 µm diameter sample gives the highest areal capacitance of 490 µF/cm^2. The highest volumetric capacitance is expected to be achieved on the samples with the smallest spheres, and a volumetric capacitance of 1.7 F/cm^3 is measured on the 5 layer, 500 nm diameter sample. All of these values are obtained from CV performed at a scan rate of 30 mV/s. The theoretical energy and power densities of this material can be calculated via Eq. 2.22 and 2.23. The maximum areal energy density is achieved on the 7 layer, 1 µm diameter spheres, 67 nWh/cm^2. The maximum power density for the same sample is 1.8 µW/cm^2.

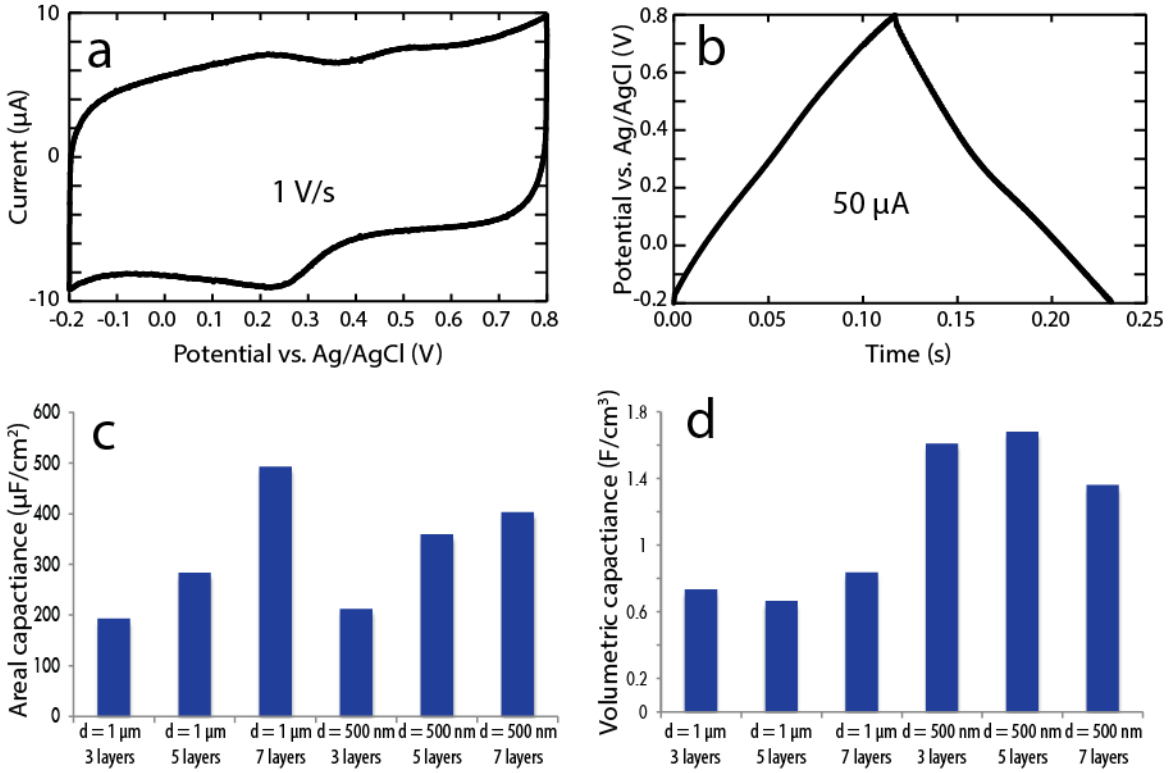

Figure 7.3 a) CV for graphene grown on 5 layer, 500 nm diameter scaffold, b) Galvanostatic charge/discharge plot for graphene grown on 5 layer, 500 nm diameter scaffold, c) Plot comparing areal specific capacitance for all tested samples calculated from CV (scan rate of 30 mV/s), d) plot comparing volumetric capacitance for all tested samples calculated from CV (scan rate of 30 mV/s).

7.3 Conclusion

While the energy and power density that results from this work is a few orders of magnitude lower than state-of-the-art carbon electrode materials, this work is a proof of concept demonstration of CVD graphene growth on template electrodeposited Ni scaffolds. Much higher energy densities should be achievable simply through increasing the number of sphere layers (areal energy density) or reducing the size of the spheres (volumetric energy density). Other templates such as anodized alumina [127] and diblock copolymers could be utilized to precisely control electrode geometries. This process is highly promising for engineering electrodes for tuning energy and power densities.

8 Materials for harsh environment supercapacitors

The aforementioned supercapacitor electrode and electrolyte materials are primarily suited for operation at ambient pressures and temperatures. However, for applications which require high temperatures, high pressure, reactive ambients, or other harsh environments, many of the material systems discussed would not exhibit good performance. Carbon based materials such as activated carbon, carbon nanotubes, and graphene can all oxidize in oxygen containing environments at high temperatures. Buckyballs and carbon nanotubes have been shown to rapidly degrade at ~450 °C and ~ 700 °C in air [128]. While encapsulation may be a solution, more stable electrode materials, such as SiC nanowires (NWs) [90, 129] could provide additional stability against high temperature oxidation. Furthermore, common electrolytes are also limited in high temperature stability. Aqueous electrolytes undergo phase change at 100 °C and most room temperature ionic liquids will degrade at temperatures above 250 °C [130]. For powering microdevices and microsensors in geothermal energy, aerospace, nuclear power, and other high temperature applications, more thermally stable materials must be investigated. This chapter discusses yttria-stabilized zirconia as a possible solid state electrolyte and several techniques for conformal deposition on high surface area electrodes, such as SiC NWs.

8.1 Yttria-stabilized zirconia solid state electrolyte

Supercapacitors, also known as double-layer capacitors or ultracapacitors, are comprised of two essential components, the electrodes, which conduct electrons and holes and connect to an external circuit, and the electrolyte, which conducts ions to and from its interface with the electrodes. Unlike batteries, which store energy via electrochemical redox reactions in the bulk of an electrode, supercapacitors rely on charge storage only at the electrode-electrolyte interface. This difference in storage mechanism allows supercapacitors to achieve higher power densities and longer cycle lifetimes than most batteries [1]. For applications that require large power loads or frequent cycling, supercapacitors can therefore provide an optimum energy storage medium. In room temperature supercapacitors, the electrolyte is typically a liquid phase ionic conductor, such as an aqueous salt solution, an organic salt, or an ionic liquid [35]. For high temperature energy storage applications such as automotive, aerospace, and geothermal microsensors and electronics, however, the instability of these traditional electrolytes renders them unusable, and alternative materials must be found. For example, Masarapu et al. have demonstrated good cycling behavior for a supercapacitor with carbon nanotube electrodes and a tetraethylammonium tetrafluoroborate-polypropylene carbonate electrolyte at up to 100 °C, the highest reported cycling temperature for a liquid electrolyte supercapacitor [131]. A clay/ionic liquid composite electrolyte has been demonstrated to operate at 200 °C, but this is the highest temperature reported for liquid based electrolytes [132]. Additionally, the use of liquid electrolytes presents significant fabrication and packaging obstacles if on-chip integration with microdevices is desired. Current micro-supercapacitor efforts have focused on the development of patternable electrodes [52, 5, 133, 62, 54, 50, 57], but have primarily used liquid based electrolytes for capacitance testing.

Due to the temperature limitations and fabrication challenges presented by liquid electrolytes, interest in an all-solid-state inorganic supercapacitor has been on the rise. Inorganic solid electrolytes that have been investigated for supercapacitor applications include $RbAg_4I_5$ [45],

Li_2S-P_2S_5 composite [46], LiF [47], $Li_{2.94}PO_{2.37}N_{0.75}$ [48], and yttria-stabilized zirconia (YSZ) [49]. However, many of these solid ionics degrade at high temperature (T ≥ 300 °C) and would be unsuitable for harsh environment applications [134]. One exception is YSZ, which only has appreciable ionic conductivity at high temperatures (T ≥ 300 °C), and is stable at temperatures up to 1200 °C [135]. YSZ conducts ionic charges through an oxygen vacancy hopping mechanism. An atomic lattice model of YSZ is shown in Figure 8.1. Although Hendriks et al. demonstrates the fabrication and testing of a YSZ-based supercapacitor, the mechanical milling methods used are incompatible with microfabrication technology and would be impractical for an on-chip energy storage solution [49]. Additionally, the referenced work derives capacitance from AC impedance equivalent circuit analysis and potential step measurements, and assumes that all charge storage is from double-layer capacitance, ignoring possible faradaic reactions at the electrode surface. The AC impedance and potential step data are not shown, making the reported capacitance values difficult to reproduce and hence of limited value for other researchers. In this work, we report more detailed electrochemical measurements of a YSZ-based micro-supercapacitor fabricated via e-beam evaporation of YSZ and operated at a temperature of 300 °C.

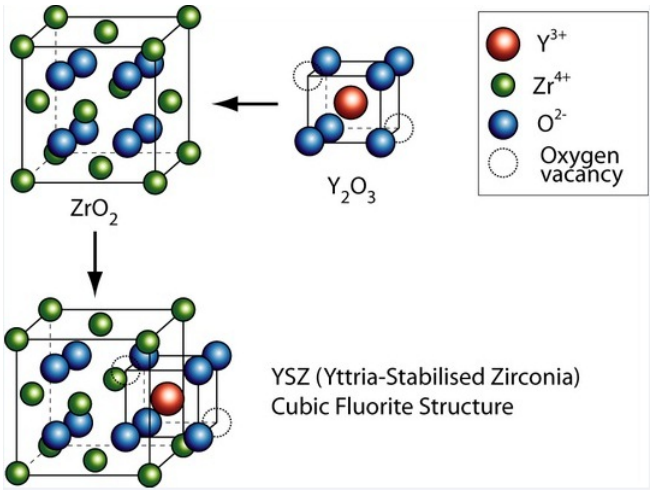

Figure 8.1 Atomic structure of YSZ. Used under a Creative Commons Attribution-ShareAlike license.

8.1.1 Experimental

A 100-nm thick layer of SiO_2 is grown thermally on Si (100) substrate and acts to electrically isolate the substrate. Approximately 200 nm YSZ is deposited via e-beam evaporation (Thermionics VE-100) onto the SiO_2-coated Si wafer, with the evaporation source being a pressed YSZ powder (Sigma-Aldrich #464228, 99.9% purity). Substrate temperature is not controlled during the evaporation process. After dicing the wafer into 1.1x1.1 cm^2 dies, samples are loaded into a hot-wall CVD reactor (Thermo Scientific Lindberg Blue M) and sintered at 1200 °C for 3 hours in air at atmospheric pressure. The crystalline quality of the YSZ film is characterized via X-Ray diffraction (XRD, Siemens D5000). Pt contacts (20-50 nm thickness with a 5 nm Ti adhesion layer) are evaporated and patterned on the YSZ film using a shadow mask. Figure 8.2 (inset) shows the sample geometry. Alumel wires (Omega #SPAL-010) are contacted to the Pt contact pads using a high temperature Ni-based conductive adhesive paste (Durabond 952). After 24 hours of room temperature curing, the sample is introduced into the

center of the hot-wall CVD reactor with high vacuum electrical feedthroughs for high temperature testing. All electrochemical testing is conducted in vacuum of < 20 mTorr using a galvanostat/potentiostat (CH Instruments, 660D Model). In order to perform a two-probe measurement, the reference and counter electrode leads are electrically shorted.

8.1.2 Results & Discussion

Figure 8.2 shows the XRD spectra of the YSZ powder as well as the evaporated film after sintering. Sharp YSZ peaks are apparent after sintering, indicating crystallization during the process. The electrochemical properties of the YSZ film are probed via cyclic voltammetry (CV), galvanostatic charge/discharge, and AC impedance spectroscopy (ACI). CV results are shown in Figure 8.3 for a variety of temperatures. For all temperatures below 250 °C (Figure 8.3a), the voltammogram shape is strongly rectangular, with a slight positive slope at higher temperature, likely a result of small ohmic leakage currents. The rectangular shape at a scan rate of 100 mV/s, with little to no rounding at the edges of the voltage window, indicates a low equivalent series resistance (ESR), a measure of electrolyte or circuit resistance. Since the ionic conduction of YSZ is quite low at these temperatures (< 10^{-5} S/cm) [134], the capacitive behavior observed here cannot be attributed solely to double layer capacitance and is likely primarily driven by a simple dielectric capacitance with YSZ functioning as a dielectric layer rather than an electrolyte. Above 250 °C, maxima and minima in the voltammogram (Figure 8.3b) become apparent, implying the contribution to current of faradaic reactions at the electrode surface at higher temperatures [8], likely the reduction/oxidation of Pt at the electrolyte interface, which has been previously reported [136, 137]. According to Kenjo et al., these reactions primarily occur at the Pt/YSZ interface through monolayer oxygen adsorption [137]. The symmetry of the peaks in the voltammogram about the x-axis indicates good reversibility [8]. For a reversible Nernstian reaction, we expect the potential difference between the cathodic and anodic peaks, ΔE_p, to be about $2.3RT/nF$ [138], or 0.11 V for a 1-electron transfer process at 300 °C. The measured ΔE_p is between 0.11 and 0.13 for scan rates between 100 mV/s and 1 V/s, confirming good redox reversibility; higher scan rates result in lower measured capacitances and

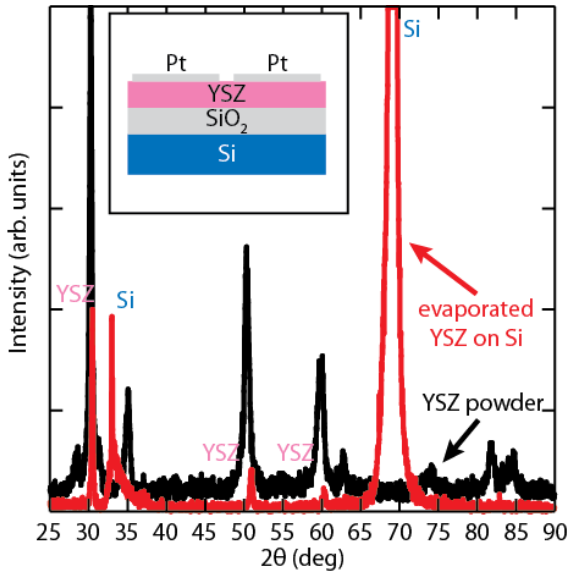

Figure 8.2 XRD spectra of YSZ powder (black) and evaporated YSZ on SiO_2/Si after sintering (red). Inset shows the fabricated sample geometry.

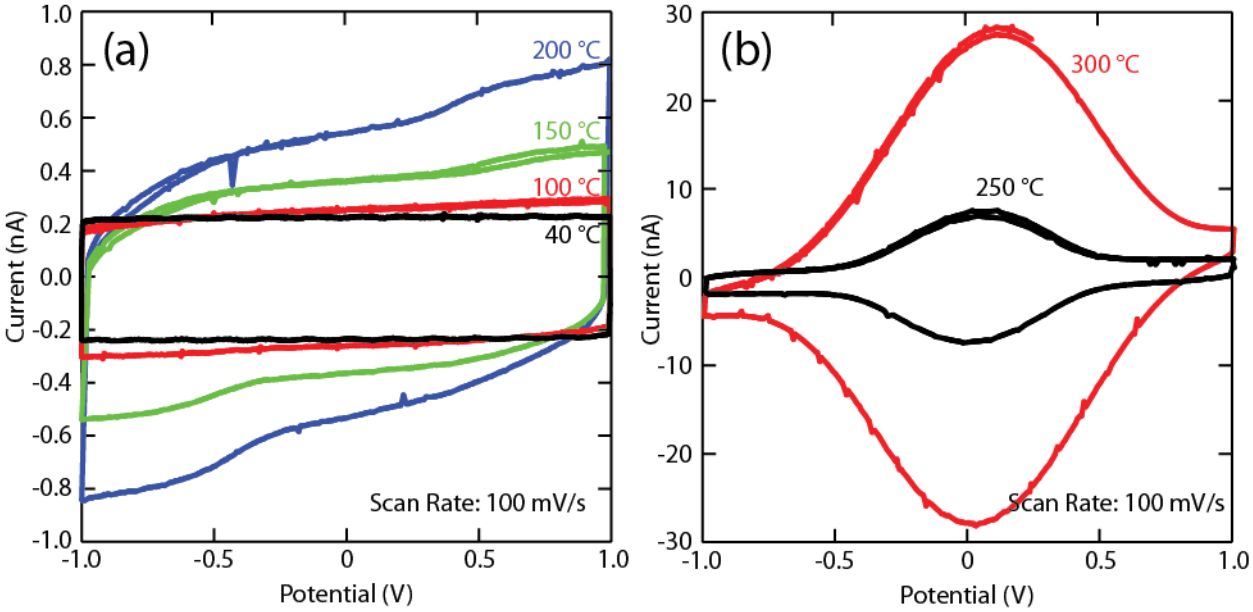

Figure 8.3 Cyclic voltammograms of Pt/YSZ supercapacitor at various temperatures. (a) Low temperature testing (b) High temperature testing.

increased peak splitting in the CV shape. From Figure 8.3, the large pseudocapacitive contribution of the Pt-oxide monolayer reduction/oxidation reactions relative to the dielectric and double layer capacitance is apparent. The total capacitance of the device can be calculated from the CV results from Eq. 2.8. The calculated capacitance for a scan rate of 100 mV/s is given in Table 8.1 for each temperature tested. A capacitance of 130 nF at 300 °C corresponds to a specific areal capacitance of ~800 nF/cm^2 for a Pt/YSZ electrode at this temperature. This value is achieved by multiplying the capacitance by 2 (for two identical capacitors in series) and then dividing by the area of one electrode.

Table 8.1 Capacitance calculated from electrochemical characterization techniques.

Temperature (°C)	**C from CV (nF)**	**C from C/D (nF)**	**C from ACI (nF)**
40	2.3	2.9	2.1
100	2.6	3.0	2.4
150	3.7	3.7	2.4
200	5.2	5.7	2.5
250	28	100*	68†
300	130	330*	160†

*Smaller voltage range (-0.3 V to 0.3 V) used for calculation

†Pseudocapacitive contribution

The abrupt change in electrochemical behavior at high temperatures is also seen in the galvanostatic charge/discharge behavior (Figure 8.4). The curves at low temperature, charged and discharged with a current of 1 nA, are quite linear, the expected response for an ideal

capacitor. As temperature is increased, the curves become increasingly nonlinear, and at T ≥ 250 °C (Figure 8.4b), the behavior changes drastically, with sharp increases in slope at $|V| > 0.4$ V. A current of 10 nA is used for the higher temperature measurements to reduce the time required for charging and discharging. The shape of the discharge curve is typical for a mass transfer limited redox process [138]. As the concentration of charged species at the Pt/YSZ interface is consumed through reduction/oxidation, the ions must be replaced through diffusion. At an extreme enough potential, $|V| > 0.4$ V in this case, the reactants are depleted and the potential shifts rapidly with further applied current (this same mass transfer limitation leads to the maxima and minima seen in the CV curves). At higher temperatures, the ion diffusion rate is higher, allowing for increased charge storage before onset of this transition. The capacitance can also be calculated from these data using Eq. 2.11. These results are reported in Table 8.1, where the limited voltage window of -0.4 to 0.4 V is used for the higher temperature calculations. This smaller voltage window is used to capture the linear portion of the discharge curve, excluding of the onset of the potential transition. The values are in good agreement with those derived from CV measurements; the large deviation for the higher temperature measurements results from using the smaller voltage window in the calculation.

AC impedance spectroscopy can also provide valuable insight into the electrochemical performance of the fabricated device. Figure 8.5 shows the ACI spectra for an applied potential amplitude of 5 mV. The low temperature measurements show ideal capacitive behavior, with a near vertical line in the complex-plane impedance response. These data can be easily fit with a standard RC circuit, where the capacitance as a function of frequency can be calculated via Eq. 2.18. The capacitance is fairly constant for the frequency spectrum probed (10 Hz to 1MHz) and so an average value of C can be used. The results show good agreement with those calculated from CV and are tabulated in Table 8.1. At temperatures above 250 °C, the impedance response changes to resemble a semicircle with a semi-vertical tail. Using an equivalent circuit model (Figure 8.5 insert), the contributions of pseudocapacitance and geometric/double-layer

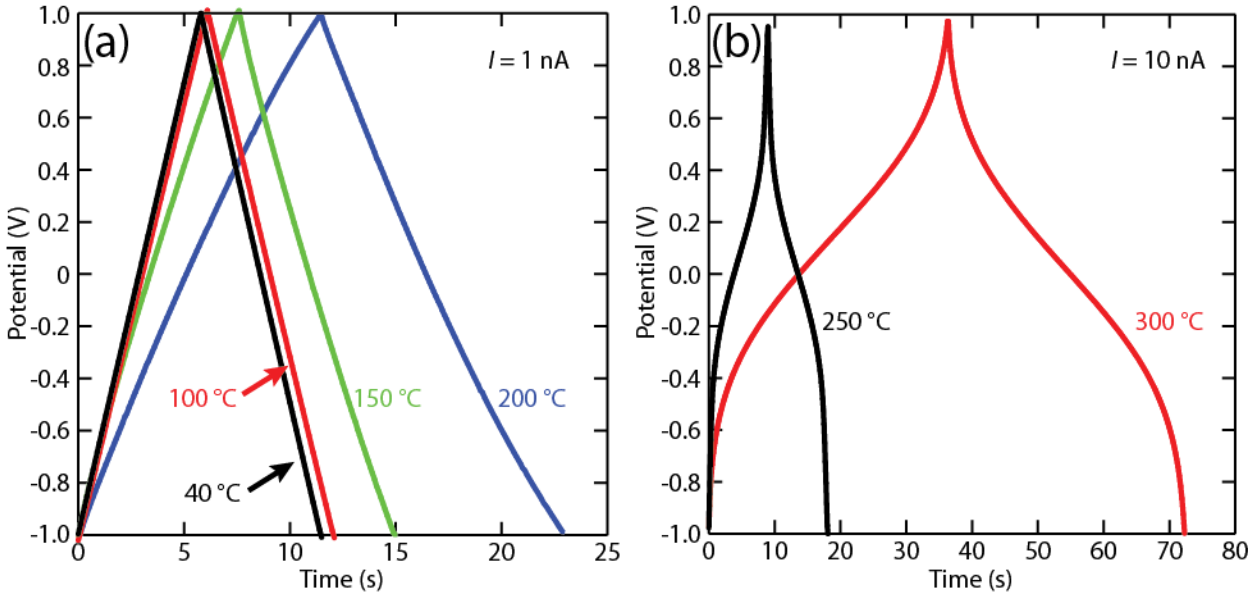

Figure 8.4. Galvanostatic charge/discharge curves for Pt/YSZ supercapacitor device. (a) Low temperature measurements conducted with a current of 1 nA. (b) High temperature measurements conducted with a current of 10 nA.

capacitance can be elucidated. Numerous equivalent circuit models have been previously proposed for the YSZ system [139], but they frequently neglect contributing circuit elements representing double-layer capacitance or pseudocapacitance. Here, a typical pseudocapacitive model [1, 8, 28] is combined in parallel with the dielectric capacitance in an attempt to fully deconvolute the impedance elements. Constant phase elements (CPE) are used as circuit components in place of capacitors, due to the nonideality of the device behavior. Capacitance can be calculated from the CPE model via Eq. 8.1 [140]:

$$C = Y_0(\omega_m'')^{n-1} \quad 8.1$$

where Y_0 is the admittance, ω_m'' is the frequency at which the imaginary component of impedance reaches a maximum on the semicircle, and n is an ideality factor which is 1 for ideal capacitors. Since this equivalent circuit model contains two CPE elements with similar frequency response, what would otherwise be two semicircular components appears to be one in the Nyquist plot. Therefore, as an approximation, the same ω_m'' can be used to estimate both the double-layer and pseudocapacitance.

Table 8.2 Capacitance values derived from equivalent circuit analysis for high temperature AC impedance tests.

Capacitive Circuit Element	Capacitance @ 250 °C (nF)	Capacitance @ 300 °C (nF)
Dielectric Capacitance	2.6	2.6
Double-layer Capacitance	7.7	5.6
Pseudocapacitance	68	160

The modeled capacitance values are shown in Table 8.2 for the higher temperature

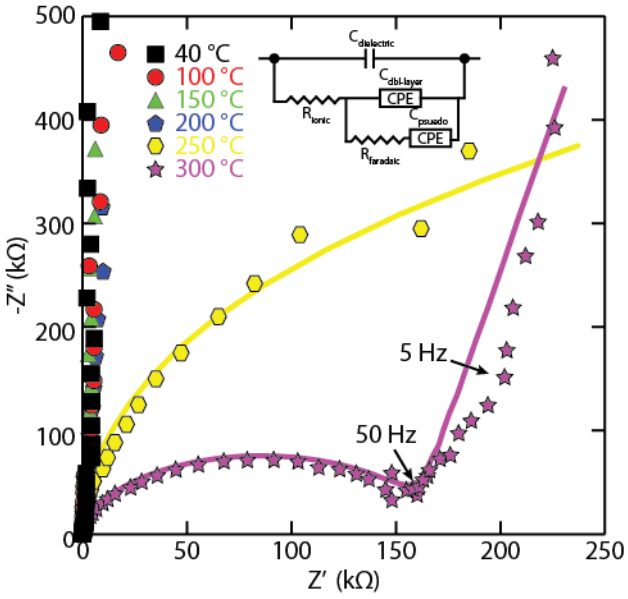

Figure 8.5. AC impedance spectra for Pt/YSZ supercapacitor device at various temperatures. Applied voltage amplitude is 5 mV. Inset shows equivalent circuit model used to model 250 and 300 °C data.

measurements. Good agreement with the values derived from CV is achieved. The contribution of dielectric capacitance is found to be 2.6 nF for the 250 and 300 °C measurements, which is nearly identical to the low temperature capacitance calculated from the CV, galvanostatic discharge, and AC impedance measurements. The total capacitance is dominated by pseudocapacitance, with values in good agreement with the CV results (see Table 1).

The energy and power densities of this device operating at 300 °C can be calculated using Eqs. 2.22 and 2.23 to be 26 nJ/cm^2 and 4 nW/cm^2 respectively, where a maximum voltage of 0.4 V, a *C* of 340 nF, and a discharge current, *I*, of 10 nA is used. At a current of 100 nA, the corresponding energy and power densities are 24 nJ/cm^2 and 40 nW/cm^2. The energy and power density values of this micro-supercapacitor are not optimal, given the limited Pt/YSZ interface area available for charge storage in this planar geometry; higher surface area electrodes with conformal YSZ deposition will be necessary for applications which require larger amounts of energy and power. Atomic layer deposition of YSZ has been recently demonstrated and could be utilized for this purpose, and is currently under investigation [141].

8.1.3 Summary and future work

In summary, a high temperature all solid-state micro-supercapacitor has been fabricated using evaporated Pt and YSZ as electrode and electrolyte materials. Thorough electrochemical testing reveals that the reversible reduction/oxidation of the Pt electrodes contributes to significant pseudocapacitive charge storage T > 250 °C. The magnitude of pseudocapacitive charge storage dominates that of double layer charging in the high temperature regime. This successful demonstration of a high temperature micro-supercapacitor could enable development of on-chip integrated energy storage for harsh environment applications.

While YSZ is a promising material for high temperature supercapacitor electrolyte applications, planar supercapacitors do not yield sufficient energy density for practical use. Therefore, higher surface area electrodes must be integrated with the YSZ electrolyte in order to improve the electrode/electrolyte interfacial area. One primary challenge for this integration is the conformal deposition of YSZ onto these electrode structures. In Section 8.1, the YSZ was deposited using e-beam evaporation. However, e-beam evaporation is a line-of-sight deposition technique, and thus cannot be used to coat fully coat porous or nanowire electrodes.

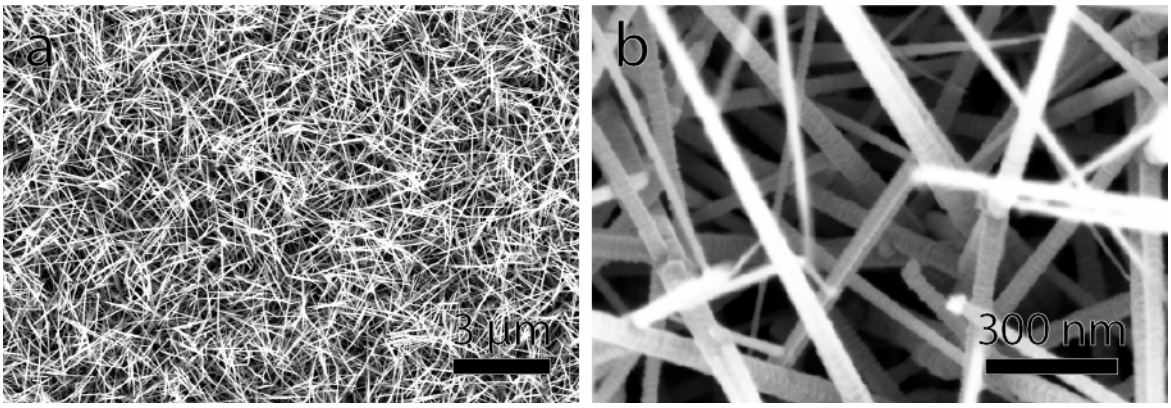

Figure 8.6 SEM images of SiC NWs at (a) low magnification and (b) high magnification. Lunet Luna assisted with the acquisition of these images.

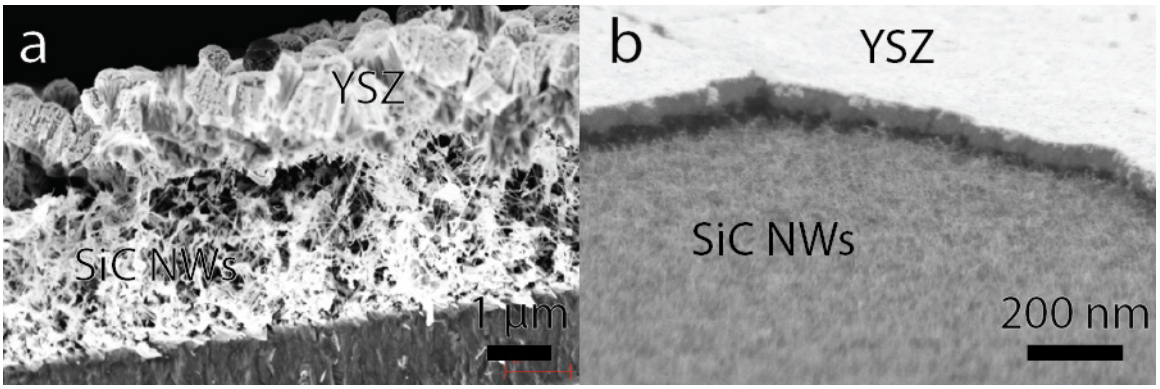

Figure 8.7 a) YSZ deposited on SiC NWs via e-beam evaporation, b) YSZ deposited on SiC NWs via dip coating of YSZ suspension

One example of the challenges presented by deposition of solid state electrolytes on high surface area electrodes can be seen in Figure 8.6 which shows the morphology of CVD grown SiC NWs [129]. Line-of-sight techniques clearly cannot fully coat the surface of these nanowires. Hence, full utilization of the SiC NW surface area is not possible using e-beam evaporation or sputtering of YSZ. In Figure 8.7, SEM images of YSZ deposited on SiC NWs via e-beam evaporation and dip-coating of a YSZ/EtOH suspension are shown. In both cases, the YSZ deposits in a film on top of the SiC NWs, without coating the dense NW forest. This behavior is undesirable for supercapacitor applications and other techniques must be explored.

Possible deposition techniques that could yield conformal deposition of YSZ on high surface area electrodes include atomic layer deposition (ALD) [141], chemical vapor deposition (CVD) [142], and solution based processes [143]. A possible process flow for device fabrication via ALD is given in Figure 8.8. Further investigation is necessary into the feasibility of these techniques for supercapacitor fabrication.

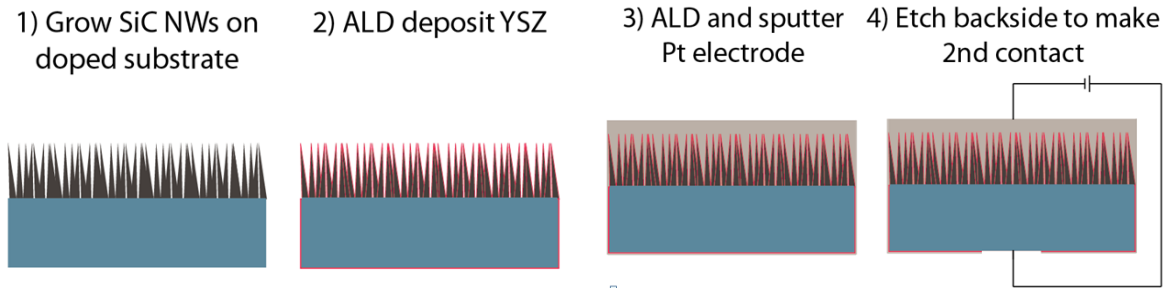

Figure 8.8 Proposed process flow for fabrication of SiC NW/ YSZ microsupercapacitors via ALD deposition of YSZ and metal contact.

9 Contact materials for harsh environments

For microelectronic and MEMS application which operate at harsh environments, such as high temperature or reactive chemical ambients, one of the challenges to device performance stability is the stability of the metal contacts [144]. For predictable device performance, whether the device is a microsensor or a microscale energy storage device (as discussed in Chapter 8), the contact resistance between the metal and the active material must be low and stable under real-world environmental conditions. For on-chip micro-supercapacitors in particular, high ohmic resistances in the device circuit, including contact resistance, can lead to reduced total potential windows and poor power performance. This chapter will discuss the high temperature stability of ohmic metal contacts to SiC, which is a popular material for harsh environment microscale applications, including micro-supercapacitors [129, 90].

9.1 Contacting SiC

Ohmic contacts to SiC are crucial for the development of SiC-based technologies. Ohmic contacts are defined as contacts with linear I-V characteristics. This contrasts with Schottky contacts, which show rectifying I-V behavior. Schottky contact behavior arises from the Schottky barrier which arises at metal-semiconductor junctions, illustrated in Figure 9.1. These barriers are due to a number of factors including the difference between the metal work function, Φ_{metal} and the semiconductor electron affinity, χ_{semi}, described by the Schottky-Mott model,

$$\Phi_B = \Phi_{\text{metal}} - \chi_{\text{semi}} \qquad 9.1$$

All metal-semiconductor junctions have a Schottky barrier, but ohmic contacts can be achieved through various strategies such as thinning the interfacial depletion region through local high doping density, and others [145, 146].

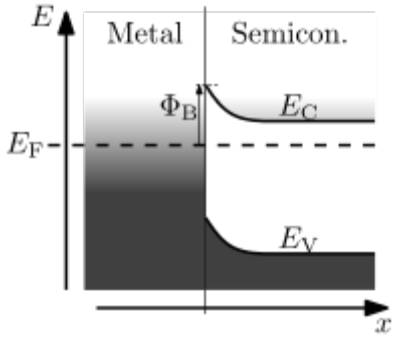

Figure 9.1 Band diagram of metal-semiconductor Schottky barrier formation.

SiC presents some unique challenges to ohmic contact formation due to its large bandgap relative to Si, which has a bandgap of 1.1 eV. Cubic SiC has a bandgap of about 2.4 eV, and hexagonal 4H-SiC has an even higher bandgap of about 3.2 eV. This large bandgap leads to large Schottky barrier heights for contact to most metals, and also results in very different barrier heights for n-type and p-type SiC metallization. For this reason, different metals are frequently used for contacting n-doped and p-doped SiC [145, 146]. In addition to formation of ohmic contacts, the

long term reliability of the contacts must be studied in order to understand failure mechanisms and properly design fabrication strategies.

9.2 Contacts to n-type polycrystalline 3C-SiC

Both Pt and Ni contacts have been shown to result in ohmic contacts on CVD deposited polycrystalline 3C-SiC thin films [147, 148]. However, high temperature stability tests of these contacts show that the contact resistance of these contacts increase over time at high temperatures [147]. The following sections describe a novel method to stabilize the contact resistance of these contacts at high temperature using an epitaxially grown graphitic carbon layer. Section 9.2.1 describes a study on the growth of epitaxial graphene on 3C-SiC thin films [149], and Section 9.2.2 probes the high temperature performance of Pt to SiC contacts which utilize this interfacial graphitic carbon layer [54].

9.2.1 Epitaxial graphene growth on 3C-SiC(111)/AlN(0001)/Si(100)[3]

Graphene, a two-dimensional sheet of carbon atoms arranged in a honeycomb lattice, has attracted significant interest since its isolation in 2004 [150]. Graphene possesses several unique electronic, mechanical, and optical properties including ballistic electron transport [150], high room-temperature carrier mobility [150], high mechanical strength [151], and high optical transmittance [152]. These properties, among others, make graphene an attractive candidate for applications including nanoelectronics [153], chemical and biochemical sensors [154], and transparent electrodes [152]. The widespread adoption of graphene in these applications depends on the development of graphene synthesis techniques. Currently, the most common synthesis methods suffer from a lack of scalability (mechanical exfoliation from graphite), complex film transfer requirements (chemical vapor deposition growth on metals [155, 156]), or poor structure and morphology (reduction of graphene oxide [157, 158]). High-temperature thermal decomposition of single-crystal SiC surfaces is an established method to produce high-quality epitaxial graphene on a wafer scale [159]. With this method, continuous micron-scale graphene domains with electron mobilities exceeding 1800 $cm^2\ V^{-1}\ s^{-1}$ have been produced on the Si-terminated face of hexagonal SiC(0001) [160]. On the C-terminated face, high temperature annealing yields many layers of graphene that nonetheless yield even higher mobilities, greater than 250,000 $cm^2\ V^{-1}\ s^{-1}$ [161]. However, a prominent drawback of this technique is the high cost and limited size of single-crystal SiC substrates. A more cost-effective technique may be the high-temperature graphitization of SiC thin films on low-cost substrates including Si (100) [162], Si (111) [163, 164, 165], and Si (110) [164]. Deposition on Si (100) wafers would also allow leveraging of existing Si microfabrication technology for device development. However, the use of silicon substrates for SiC thin film growth is challenged by the large lattice mismatch (20%) between SiC and Si, which leads to strain and poor film adhesion, and damage to the Si/SiC interface by CVD byproducts and Si outdiffusion during growth. Furthermore, from the device point of view, the use of dielectric materials is critical in many designs, including for electrical isolation of the device from the underlying substrate and for the designs employing back-gating of the substrate. The graphitization of SiC directly grown on Si dictates that the SiC thin film serves as both the graphitization source and the electrical insulation layer, hindering the ability to tailor these two properties separately.

[3] A modified version of this work was published in: B. Hsia, N. Ferralis, D. Senesky, A. P. Pisano, C. Carraro and R. Maboudian, "Epitaxial Graphene Growth on 3C–SiC (111)/AlN (0001)/Si (100)," Electrochem Solid-State Lett, vol. 14, pp. K13-K15, 2011.

These limitations can be overcome by introducing a highly-textured AlN (0001) buffer layer between the Si substrate and the SiC thin film. The small lattice and thermal expansion coefficient mismatches between 3C-SiC (111) and AlN (0001) (~1%) improve adhesion and reduce the SiC film strain. AlN also acts as a barrier for Si outdiffusion during graphitization, and its resilience to chemical etching from the chlorinated precursors often used for SiC thin film growth reduces the formations of pits and voids in the underlying Si substrate [166]. In addition, the AlN layer, with a wide energy band-gap of 6.2 eV, can effectively insulate the graphene/SiC from the underlying substrate, which would allow for graphitization of doped or very thin SiC films for device applications. Furthermore, the hexagonal lattice of the AlN results in the formation of a high-quality epitaxial 3C-SiC (111) film [167]. The (111) orientation of the 3C-SiC is notable in that its surface closely resembles the hexagonal polytype of SiC, which is most frequently used in current graphene synthesis. Recently, graphene grown on 3C-SiC (111) has been shown to closely resemble graphene grown on the Si-face of 6H- and 4H-SiC (0001) in terms of stacking (Bernal, ABAB), growth structure (formation of a $(6\sqrt{3}\times6\sqrt{3})R30°$ carbon interfacial layer preceding the growth of the first graphene monolayer), and electronic structure (linear bands near the K and K' points) [165]. Using an AlN buffer layer allows for a hexagonal-like surface for growth while still using Si (100) substrates. Otherwise, SiC (111) growth would require a matching Si orientation, and hence the use of less common Si (111) substrates.

A 1 μm thick highly-textured AlN (0001) buffer layer was deposited on p-type Si (100) via reactive sputtering [167]. 3C-SiC thin films were grown at 1200 °C and 1.1 Torr, using a hot-wall low pressure chemical vapor deposition (LPCVD) reactor (Thermo Electron Corporation) with methyltrichlorosilane (MTS) in hydrogen carrier gas as the precursor [167]. The resulting films were characterized by X-ray diffraction (XRD, Siemens D5000), atomic force microscopy (AFM, Digital Instruments Nanoscope IIIa), and Raman spectroscopy (HORIBA Jobin Yvon LabRam, excitation provided by a He–Ne laser, 633 nm). SiC film thickness was measured using cross-sectional scanning electron microscopy (JEOL JSM-6490LV); deposited films ranged from < 50 nm to ~1 μm in thickness. Graphitization was performed in ultra-high vacuum (UHV) via electron beam heating to approximately 1400 °C at pressures on the order of 10^{-9} Torr for 5 minutes. Auger electron spectroscopy (AES, Physical Electronics) and Raman spectroscopy were used to determine the approximate average number of graphene layers and their quality.

Figure 9.2 shows a typical XRD spectrum of the SiC/AlN/Si. The AlN displays the wurtzite (0001) orientation, with 2θ peaks at 36.2° and 76.7°, corresponding to the (0002) and (0004) planes respectively. Cross-sectional SEM shows columnar AlN (0001) grain formation [167]. The 3C-SiC film is clearly epitaxial, with only (111) and (222) 3C-SiC peaks appearing at 35.8° and 75.6°. No other SiC orientations are present. The closely matched lattice parameters of SiC and AlN are clearly seen by the overlapping Bragg diffraction peaks in Fig. 1 (inset). This epitaxial relationship stands in contrast to SiC directly deposited on Si, which requires pretreatment steps or risks high film stress and defect density due to a large lattice mismatch [168, 169].

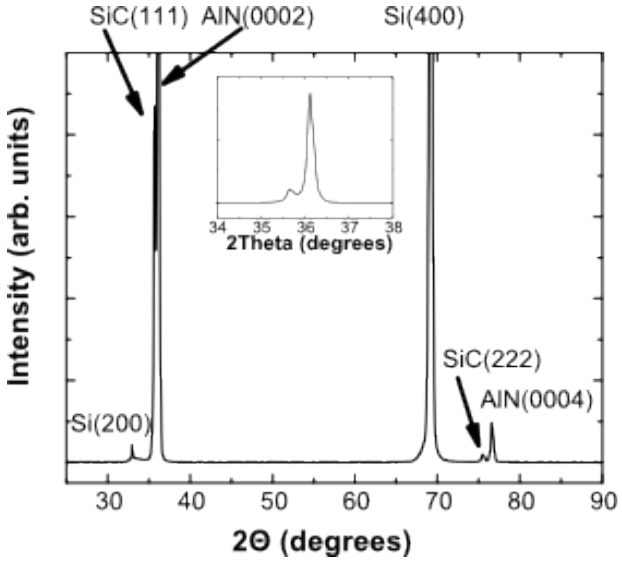

Figure 9.2 XRD spectrum of SiC/AlN/Si sample before graphitization. (111) is only SiC orientation present. Inset shows small area of the spectrum showing only the SiC (111) and AlN (0002) diffraction peaks.

A typical Raman spectrum of the SiC/AlN/Si after graphitization is shown in Figure 9.3. After graphitization, all the samples, regardless of thickness, displayed peaks at 1344 ± 3, 1596 ± 3, and 2682 ± 6 cm^{-1}, corresponding to the D, G, and 2D peaks [170]. The G-peak position is blue-shifted by about 15 cm^{-1} and the 2D-peak shift by about 40 cm^{-1} in comparison to exfoliated graphene. These peak shifts can be attributed to graphene film compressive strain of about 0.5% [171].

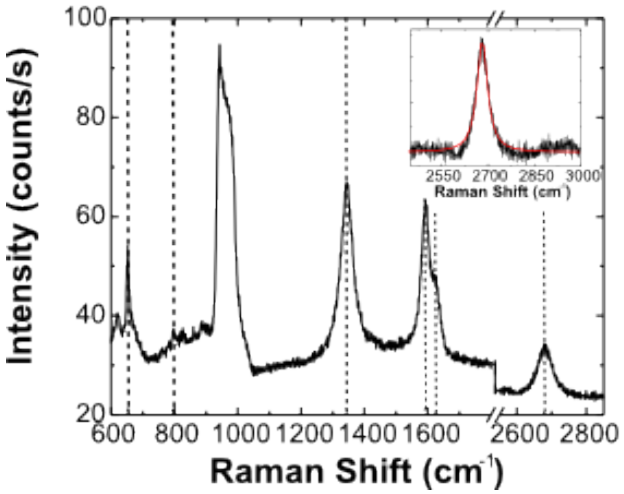

Figure 9.3 Representative Raman spectrum of SiC/AlN/Si after graphitization. Peak at 650 cm^{-1} is AlN TO peak. Small feature ~800 cm^{-1} is the SiC TO peak. Graphene's D-, G-, D', and 2D peaks are visible at 1345, 1593, 1626, and 2681 cm^{-1} respectively. The inset shows the 2D peak, which can be fit with a single Lorentzian with FWHM of 41 cm^{-1}, in agreement with Ref. [158].

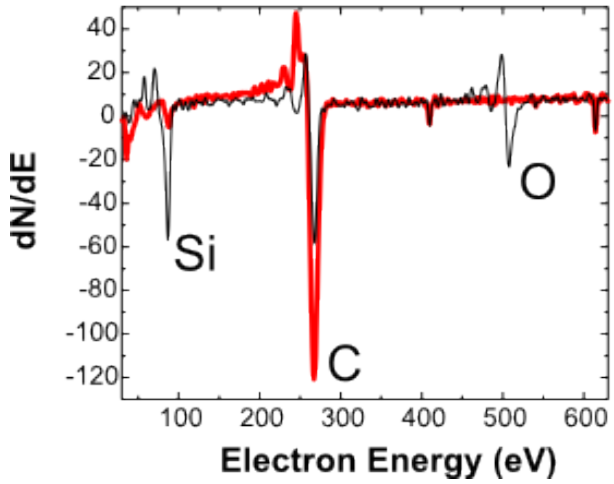

Figure 9.5 Auger electron spectra of SiC/AlN/Si surface before (black thin line) and after (red thick line) graphitization. Increase in C:Si ratio during graphitization is apparent.

The full-width-at-half-maximum (FWHM) of the 2D peak under our synthesis conditions varied between 40 cm^{-1} (as seen in the inset in Figure 9.3) and 60 cm^{-1}, which indicates a monolayer to a few-layers of epitaxial graphene [172]. This variation occurred both within-sample and between-samples. By measuring the ratio of the Si and C Auger peaks, the approximate number of layers can also be estimated [173]. Figure 9.4 shows a representative Auger electron spectrum that corresponds to the Raman spectrum in Figure 9.3. The AES C:Si intensity ratio indicates an average graphene thickness of 1.8 monolayers in addition to the C-rich buffer layer, in agreement with the Raman results. The Raman D-peak, located at ~1350 cm^{-1}, is often referred to as the "defect peak." The name arises from the fact that the D-peak does not occur in pristine graphene, in contrast to the G- and 2D- peaks. Therefore, the intensity ratio of the G- and D- Raman peaks can be used as an indicator of graphene domain size through the Tuinstra-Koenig (T-K) relation [170, 174]. For the samples processed using our procedure, the I(G)/I(D) ratio increases from

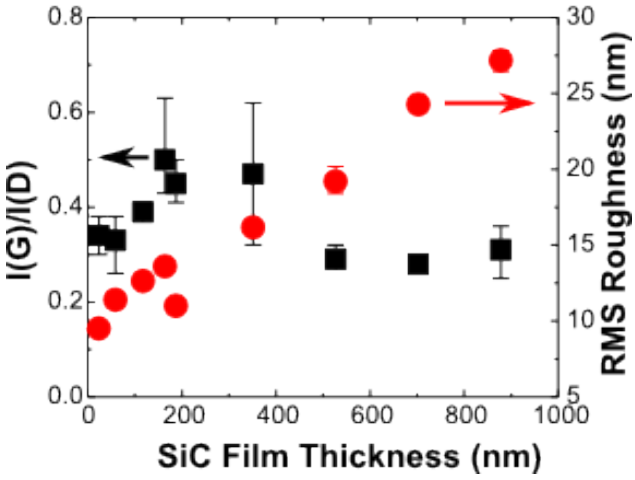

Figure 9.4 G-peak to D-peak intensity ratio (black squares) and surface roughness (red circles). Error bars show range of measurements within a single sample. The two points near 200 nm show sample-to-sample variability and are displaced for visual clarity.

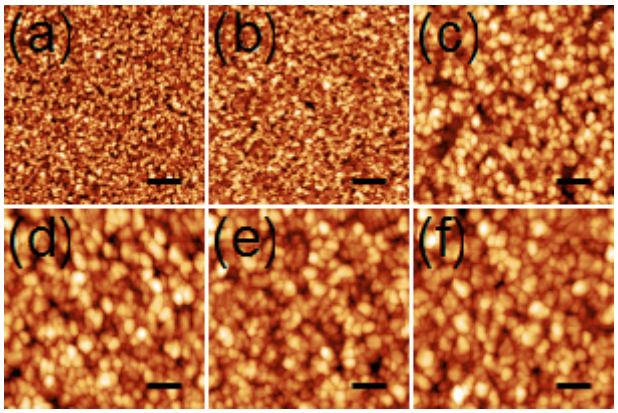

Figure 9.6 AFM images of SiC surface corresponding to (a) ~60, (b) 175, (c) 350, (d) 525, (e) 700, and (f) 875 nm thicknesses. RMS roughnesses are (a) 11, (b) 11, (c) 16, (d) 20, (e) 25, and (f) 28 nm. Scale bar is 1 μm. Z-scale is 200 nm.

~0.35 to ~0.5 as the SiC film thickness increases to 200 nm (as shown in Figure 9.5). These I(G)/I(D) ratios correspond to graphene domain sizes between 10 and 25 nm [170]. These domain sizes exceed those reported for graphene grown on SiC (110)/Si (110), about 12 nm [164]. The ratio decreases to a value of about 0.3 for film thicknesses exceeding 400 nm. Hence, the highest quality graphene is produced from ~200-300 nm SiC films. Figure 9.6 shows atomic force micrographs for SiC films of various thicknesses. As thickness increases, two trends are immediately apparent: the increase in the size of surface-projected grains and the increase in surface roughness (as quantified by root mean squared, or RMS). Both of these factors likely impact the graphene domain size. The initial increase in graphene domain size as the SiC film thickness increases to its optimum is likely due to the increasing size of SiC surface grains [168]. The surface-projected grain size for the thinnest films is on the order of tens of nanometers, the same order of magnitude as the graphene domain size as estimated by the T-K relation. The small size of the grains likely serves as an upper limit to graphene domain size. The increased surface roughening may serve as a competing effect for thicker films, and likely contributes to the reduced graphene domain size for films thicker than 400 nm. More study of this phenomenon is necessary to draw firmer conclusions.

In summary, high-quality epitaxial graphene is successfully grown on 3C-SiC (111) films on AlN/Si substrates. The quality of the graphene is highly dependent on film thickness and roughness. Domain sizes of up to 25 nm were achieved with an optimum film thickness of about ~250 nm. While this domain size is small, it is larger than previously reported domain sizes on thin-film SiC [164]. Further improvement is possible through utilization of techniques including Ar- or Si-assisted graphitization [160, 175], surface polishing, and improvements in AlN crystallinity. Ar- and Si-assisted graphitization have been shown to improve graphene domain size on single-crystal SiC substrates, but would require precise pressure and temperature control since graphitization temperatures would approach the melting temperature of the Si substrate under these conditions. This method may prove to be a more economically feasible production method of graphene. Furthermore, the use of an AlN buffer layer allows one to electrically insulate the SiC thin film from the underlying substrate, and in this way, enables the optimization of the SiC layer (e.g., its doping level and thickness) for graphene synthesis and application.

9.2.2 Enhanced ohmic contact via graphitization of polycrystalline silicon carbide[4]

Rapid advances in the growth, doping and processing of SiC [176, 177] have led to the realization of several electronic and microelectromechanical systems (MEMS) devices for harsh environment applications [178, 179]. For SiC-based devices, one of the critical challenges to overcome is the realization of chemically and electrically stable ohmic contacts with low resistivity for electrical contacts and interconnects. One general approach to form low ohmic contacts on SiC is to lower the energy barrier height at the metal/SiC interface by depositing a metal with appropriate work function. However, in practice, the barrier height is found to depend on the semiconductor's properties including the surface termination and crystallinity, and the interfacial chemistry of the metal/semiconductor junction [180, 181]. In addition to low barrier height, the metal/SiC interface must be thermally stable in order to obtain optimum performance for high-temperature, high power and high frequency devices [182]. To solve these problems, a surface treatment prior to SiC metallization, to both lower the metal-to-SiC contact resistivity and prevent the interfacial reactions, is of great interest. This section explores the use of a interfacial graphitic layer to improve the metal-to-SiC contact high temperature performance.

9.2.2.1 Methods

The circular transmission line model (CTLM) method is used to characterize the contact behavior and contact resistivity [181], as shown in Figure 9.7. Briefly, the CTLM method measures the resistance of circular gaps of varying gap size. As the gap size approaches zero, an increasing proportion of the measured resistance arises from contact resistance (as opposed to sheet resistance). The contact resistance can be calculated from

$$R = \frac{R_s}{2\pi}\ln\left(1+\frac{d}{r_0}\right)+\frac{R_s}{\pi r_0}L_T \tag{9.2}$$

The radius r_0 of each CTLM structure is 250 μm, and the gap width, d, is selected to be 5, 10, 15 or 20 μm. R_s and L_T are the sheet resistance and transfer length, respectively. The transfer length is given by

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \tag{9.3}$$

where ρ_c is the contact resistivity. Hence the contact resistivity can be extracted from a linear regression which plots R vs. $\ln(1 + d/r_0)$. The CTLM test structure is fabricated via a one-mask

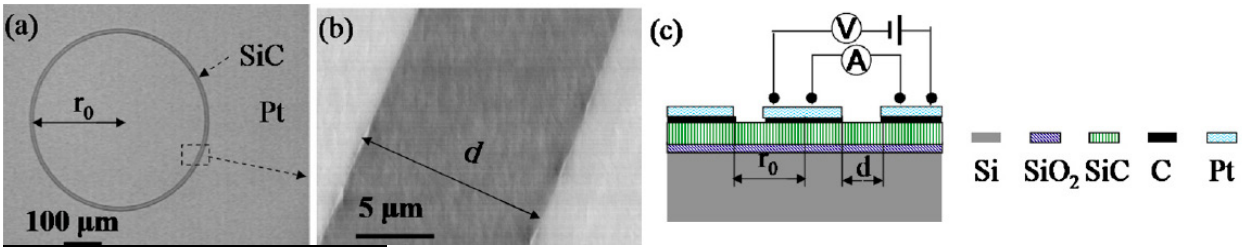

Figure 9.7 CTLM test structure. (a) Optical and SEM image of CTLM structure, (b) close-up SEM image of CTLM structure, (c) schematic side-view and 4-point probe testing setup.

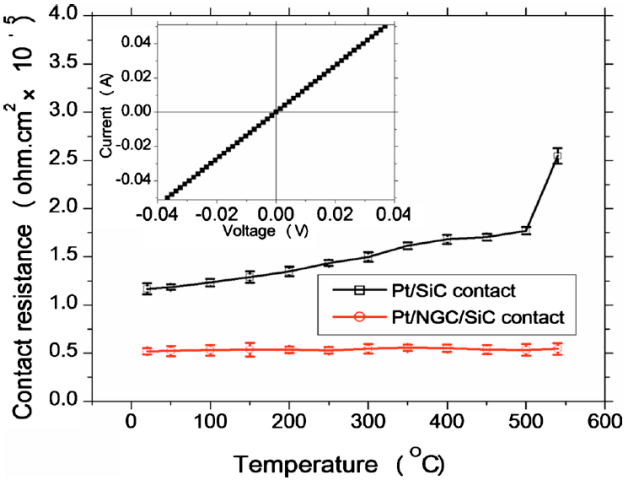

Figure 9.8 Contact resistance vs. temperature for Pt/SiC and Pt/NGC/SiC contacts. Inset: representative I-V curve on Pt/SiC contact at room temperature with r_0 = 15 μm CTLM.

process as described in Ref. [183]. The polycrystalline SiC film has a thickness of ~2.5 μm, a resistivity of 0.01 Ω.cm, and is electrically isolated from the Si (100) substrate by 1 μm silicon oxide. The carbon layer is formed by annealing the samples at 1300 ºC for 5 min in an ultrahigh vacuum (UHV) chamber (~10^{-9} Torr) [149]. The Pt film thickness is 200 nm.

The current-voltage (I-V) behavior is measured by the four-point probe method as depicted in Figure 9.7c, using a Keithley 2400 source meter. The samples are heated by an Isotemp hotplate in air for temperatures up to 540 °C with a ramp up rate of 80 ºC/min. The temperature is held for 3 minutes at each tested temperature while I-V measurements are taken. Two samples at each condition are investigated. The testing of each sample is repeated 3 times at each temperature at 1 minute interval.

9.2.2.2 Results and discussion

A representative I-V plot obtained on Pt to as-deposited SiC contact is shown in the inset to Figure 9.8. The linear behavior indicates ohmic contact. The platinum contacts to the as-deposited and annealed SiC are both found to be ohmic. The contact resistivity values from room temperature to 540 °C are shown in Figure 9.8, where Pt/SiC refers to the Pt to the as-deposited SiC contact, while Pt/NGC/SiC refers to the Pt to the annealed SiC contact. Two major differences are observed. First, the room temperature contact resistivity of the Pt/NGC/SiC contact is 5.2 $\times 10^{-6}$ Ω.cm^2, which is about half of the Pt/SiC contact resistivity. Secondly, Pt/SiC contact resistivity increases progressively with temperature and reaches 2.5 $\times$ 10^{-5} Ω.cm^2 at 540 °C, while the contact resistivity of the Pt/NGC/SiC contact remarkably exhibits little change with temperature. To understand the observed behavior, the results of the surface and bulk characterizations are reported next.

The surface carbon structure, expected upon UHV annealing, is investigated by Raman scattering (YJ HORIBA Labram), which is a well-developed technique to investigate bonding and structure of carbonaceous materials [170]. As shown in the inset of Figure 9.9, after annealing, the carbon disordered (D) and ideal graphite (G) peaks appear at 1345.5 cm^{-1} and 1595.8 cm^{-1}, respectively. The peak intensity ratio of the two peaks, I(D)/I(G) is about 1.8, indicative of a highly disordered NGC film. Auger electron spectroscopy (Physical Electronics, model Φ10-155A) is used to

estimate the thickness of the carbon layer. Compared to the as-deposited SiC film, AES analysis (Figure 9.9) shows that the annealed film exhibits an increased C to Si atomic concentration ratio of 4.1. For single crystalline SiC, this ratio corresponds to 1.4 carbon layers on the SiC surface [173]. Assuming this analysis is applicable to SiC, the thickness of the carbon layer is around 1 atomic layer.

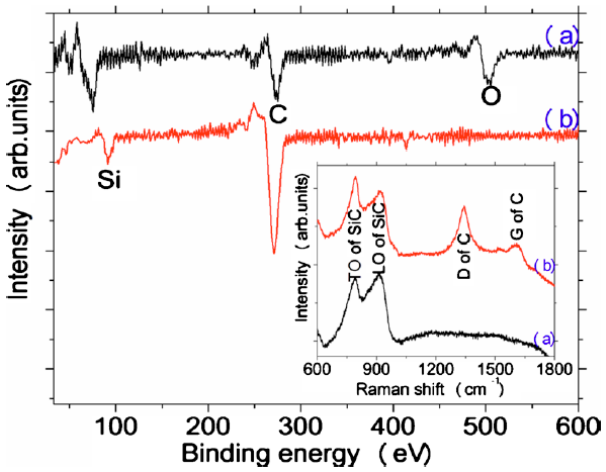

Figure 9.9 AES and Raman (excitation wavelength of 632.8 nm) spectra (inset) of (a) as-deposited SiC, (b) after annealing at 1300 °C in ultrahigh vacuum.

The formation of low-resistance ohmic contacts to SiC is determined by metal-semiconductor barrier height, surface states and interfacial chemistry [184]. The electron affinity of 3C-SiC is 4.0 eV, and the work function of Pt and graphite are 5.7 and 5.0 eV respectively. Thus, the introduction of the thin layer of graphitic carbon between SiC and Pt may reduce the barrier height, allowing for the formation of low-resistance ohmic contacts. Another major obstacle to low-resistance ohmic contact formation is the presence of oxide films. For the as-deposited film, as shown in AES spectra (Figure 9.9), even after HF treatment and quick rinse in deionized water, the oxygen signal is still present, while the surface of the annealed sample is oxygen free.

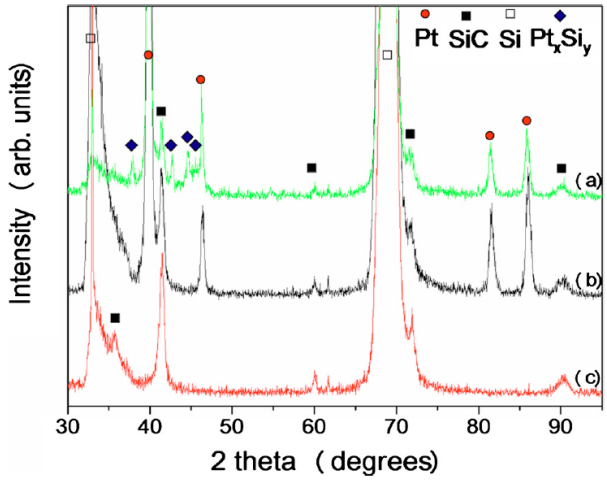

Figure 9.10 XRD spectra of (a) Pt/SiC contact, (b) Pt/NGC/SiC contact (both after 540 °C testing in the air), (c) SiC film with surface carbon layer.

The electrical, mechanical, and structural properties of the bulk SiC film are also investigated to discern their possible role in the observed contact resistance behavior. Film sheet resistance measurements show that film resistivity remains unchanged at about 0.01 Ω.cm after annealing. This indicates that in the short annealing period of 5 minutes, the dopant is not activated appreciably. As shown in Figure 9.9, the SiC transverse-optical (TO) and longitudinal-optical (LO) peaks of the as-deposited and annealed samples indicate the cubic structure of the SiC film. The Raman TO peak of the as-deposited SiC is located at 790 cm^{-1}, while that of the annealed SiC is located at 792 cm^{-1}. The shift in the TO peak position away from the expected TO peak position of 796 cm^{-1} can be used to characterize the in-plane bi-axial residual strain (ε_{bi}) of the polycrystalline 3C-SiC films grown [185]. The TO shifts of 6 cm^{-1} and 4 cm^{-1} for the as-deposited and annealed SiC films correspond to bi-axial strains of 0.51% and 0.33%, respectively. The XRD spectra (Figure 9.10) of the as-deposited and annealed SiC film show the polycrystalline cubic structure, with main peak position at $2\theta = 41.4°$, corresponding to the 3C-SiC (200) orientation. A close-up scan of this peak shows that the full width at half maximum (FWHM) of the as-deposited and annealed film are 1° and 0.83°, respectively. According to the Scherrer Equation [186], crystalline size is inversely proportional to peak width. Thus, a 17% decrease in the FWHM of the annealed film corresponds to a 17% increase in grain size.

SiC film stress and grain size could affect the metallization behavior. It is known that the tensile stress in polycrystalline films arises from voids and missing atoms at grain boundaries: the lower the tensile stress, the lower the density of defects at grain boundaries [187]. Also, larger grain sizes reduce the density of grain boundaries. Since annealing leads to both a reduction in tensile stress and a growth in grain size, vacancy defect density is reduced, which may be responsible for the better ohmic contact formation on the annealed samples.

The Pt/NGC/SiC contact shows enhanced stability at high temperature in air, as shown in Figure 9.8. In order to investigate possible phase changes due to exposure to high temperatures in air during the I/V measurements, the XRD spectra (Siemens D5000) of the Pt/SiC and Pt/NGC/SiC contacts after exposure in air at 540 °C are taken and shown in Figure 9.10. The Pt/SiC and Pt/NGC/SiC substrates both show Pt (111), Pt (220), Pt (311) and Pt (222) peaks. In addition, the Pt/SiC sample shows $Pt_{12}Si_5$ (440), PtSi (112), PtSi (202) and Pt_6Si_5 (611) phases, while no Pt

silicide phase is observed in the Pt/NGC/SiC contact after high temperature testing. It has been reported that degradation in Pt/SiC contacts after annealing at 500 °C is due to formation of a silicide layer [188]. The platinum-silicide formation can occur at temperatures as low as 350 °C [189]. Reaction between Pt and SiC may be responsible for the increase in contact resistivity of the Pt/SiC contact structure at elevated temperatures. No phase change is found for Pt/NGC/SiC contacts; the presence of graphitic carbon is suggested to create a thermal barrier to the reaction between Pt and SiC, leading to more thermally stable contacts.

9.2.2.3 Conclusion

In conclusion, the reduced barrier height, oxide-free surface, reduced vacancy defects and reduced reactions between Pt and SiC are suggested to be responsible for the reduced contact resistivity and enhanced thermal stability of Pt to graphitized SiC. The controlled growth of interfacial nanocrystalline graphite, as presented here, could vastly improve the contact quality between SiC and metals, and open the door to investigations of various metal-to-SiC contact studies and stable contact performance at elevated temperatures. Further study of the long term performance of these contacts is also an important area of study and preliminary work can be seen in Ref. [190].

9.3 Contacts to p-type SiC

Silicon carbide (SiC) is a wide bandgap semiconductor that is a promising material for many high power and harsh environment applications due to its advantageous physical, mechanical, thermal, and electrical properties [191]. In particular, SiC has been proposed as a material base for high temperature electronics and microdevices due to its high thermal conductivity, high breakdown field, and wide bandgap [192, 193, 194, 195, 196]. However, low resistance, high temperature stable ohmic contacts to SiC are required for high frequency, predictable device performance at high temperatures, and this remains an area of ongoing research [192, 193, 145, 146]. SiC occurs in a variety of polytypes and can be monocrystalline, polycrystalline, or amorphous; each of these SiC materials exhibits different properties and may require different metallization strategies. For electronics applications specifically, monocrystalline 4H-SiC is the most commonly used SiC crystal due to its superior electronic properties [196]. Dopant type also significantly affects metallization parameters: due to the large bandgap of 4H-SiC (3.2 eV), n-type and p-type SiC exhibit very different Schottky barrier heights (SBHs) for any given metallization, and therefore must also be investigated separately [145, 146]. p-type 4H-SiC, in particular, presents a challenge for metallization as the large bandgap and large electron affinity of 4H-SiC lead to a valence band greater than 6 eV from the vacuum level. Most common metallization materials have work functions between 4 and 5.5 eV, leading to large SBHs for most metal to p-type 4H-SiC contacts [145, 146].

In order to form ohmic contacts to p-type 4H-SiC, most investigators have utilized Al-based contacts (such as Ti/Al) which form Schottky contacts as deposited, but yield ohmic contacts after annealing to temperatures ~ 1000 °C. This high temperature requirement for ohmic contact formation, however, presents a possible barrier to electronics fabrication, as these high temperatures could affect the performance of transistors, diodes, and other components [197]. In order to reduce the required annealing temperature, several groups have included Ni in the contact metal, as Ni reacts with SiC to form Ni silicides at temperatures as low as 500 °C [146]. Ni/Ti/Al contacts have been demonstrated to yield contact resistivity $< 1 \times 10^{-4}$ Ω cm^2 after

annealing at a temperature of 800 °C [197, 198, 199], and are hence an extremely promising candidate for p-type 4H-SiC metallization.

In addition to minimizing the contact resistance of metallization, high temperature contact stability is a second primary concern for SiC metallization. Ni/Ti/Al contacts have shown good aging performance for 10 h at 400 °C in an Ar ambient [197]; however, to our knowledge, no high temperature aging for p-type 4H-SiC contacts has been performed in air and for longer periods. While encapsulation technologies to isolate devices from oxidative ambients are improving, they add additional process complexity and cost, and reliability studies on contacts to n-type SiC have been performed with good success [146]. Similar studies on p-type metallizations are necessary for continued advancement of SiC harsh environment technology. In this paper, we present in-air testing of Ni/Ti/Al contacts to p-type 4H-SiC for 100 hr at 450 and 600 °C.

9.3.1 Methods

A 100 mm 4H-SiC wafer was purchased (Ascatron) with the following epitaxial layers: a 500 nm n-type buffer layer, a 5-10 µm n^- isolation layer (< 5×10^{15} cm^{-3}), and a 200 nm p^+ active layer (> 5×10^{19} cm^{-3}). After dicing the wafer into 1×1 cm^2 chips (American Precision Dicing), circular transmission line model (CTLM) structures were patterned using a standard lift-off process. Samples were sonicated in acetone and rinsed with IPA prior to photolithography. After photoresist patterning, samples were dipped in concentrated HF for 10 s followed by a thorough DI water rinse. Ni (25 nm) and then Ti (50 nm) were deposited via e-beam evaporation (Thermionics VE-100). Al (300 nm) was deposited via DC sputtering (Edwards Auto 306). Sonication in acetone was used for lift-off. Annealing was performed at 800 °C for 2 min in Ar using a rapid thermal annealer (AccuThermo AW610).

450 °C and 600 °C thermal aging were performed on a hot plate and in a hot wall CVD tube furnace, respectively. The sample was periodically removed from the heat source, allowed to cool to room temperature, and tested with a Signatone S-1160 4-point probe station. 100 h of total heating time was performed for the 450 °C test; the 600 °C test was limited to 20 h due to contact oxidation and the resulting inability to measure resistance via probe station. Each sample was divided into 4 quadrants which contained 4 CTLM rings each (radius of 250 µm, gap widths of 5, 10, 15, and 20 µm). The sheet resistance and contact resistivity is derived from the I-V characteristics of each CTLM ring [181]. Each ring was tested twice and the resulting resistance averaged for subsequent calculations.

9.3.2 Results

Figure 9.11a shows the I-V characteristics of a 20-µm-gap CTLM structure before and after annealing. The transition from Schottky to ohmic behavior is apparent. All I-V plots measured during aging showed clear ohmic behavior. Figure 9.11b shows the relationship between measured resistance and gap length, d, and circle radius, r_0. A linear relationship with $R^2 > 0.99$ was achieved for all measurements, both before and during thermal aging; the sheet resistance and contact resistivity can be extracted from the slope and intercept of this linear fit [181]. Good agreement is seen between the 4 quadrants on a die, indicating uniform doping, metallization, and annealing across the die.

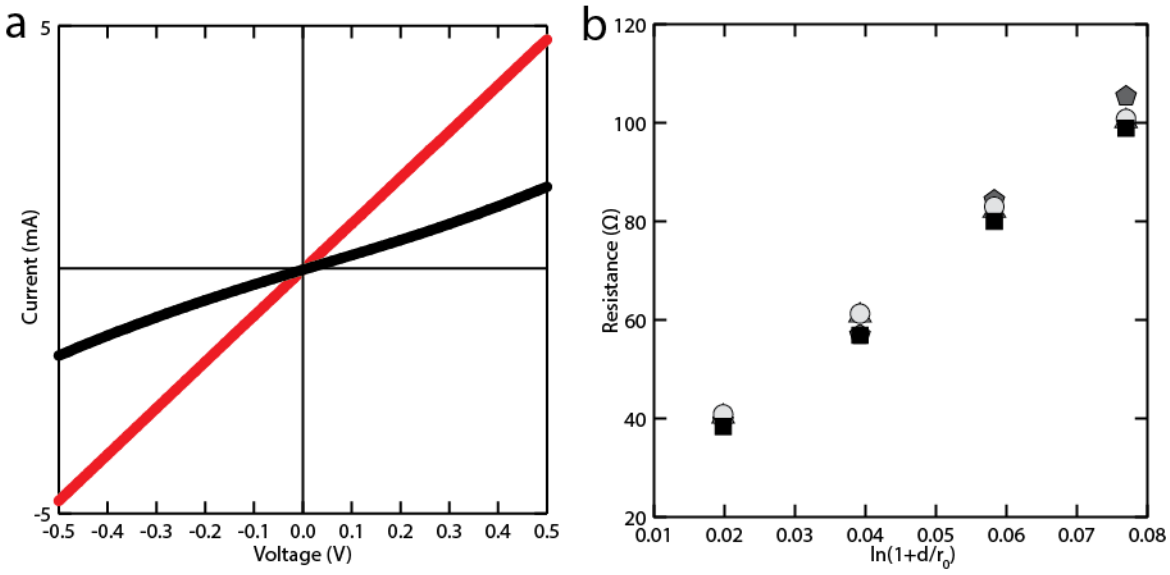

Figure 9.11 a) IV behavior of sample CTLM structure before (black) and after (red) rapid thermal annealing, b) resistance of CTLM structures with varying gap size.

The sheet resistance obtained from the CTLM method was 6000-7000 Ω/□. From the nominal 200 nm thickness of the p^+ layer, this gives a film resistivity of 120-140 mΩ cm. The pre-aging contact resistivity was 2.9×10^{-4} Ω cm^2 for the 450 °C sample, with a range of 1.8 to 3.8×10^{-4} Ω cm^2 across the 4 quadrants on the die. The 600 °C sample contact resistivity was slightly higher, 7.5×10^{-4} Ω cm^2, with a range of 6.7 to 8.4×10^{-4} Ω cm^2. This difference is likely due to slight variations inherent in the annealing process or dopant levels. The aging results are presented in Figure 9.11. The contact resistivity of the 450 °C sample remains stable throughout the 100 h testing. The 600 °C sample, on the other hand, shows a gradual increase in contact resistivity, and the testing is ended at 20 h, as the CTLM structures were no longer measureable using the probe station, despite large applied pressure.

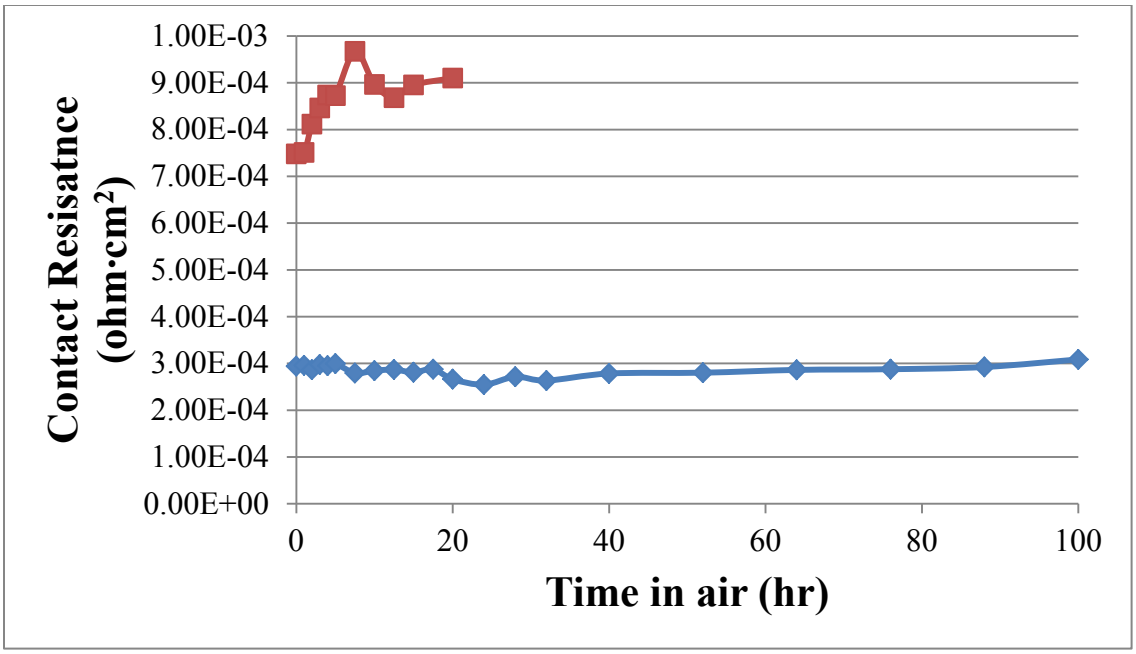

Figure 9.12 Aging data for contact resistance testing at 450 (blue) and 600 °C (red).

9.3.3 Discussion

The excellent linear fit obtained for the resistance data indicates the reliability of the contact resistance values obtained from the CTLM method. The measured contact resistance, which had a minimum value of 1.8×10^{-4} Ω cm^2 and a maximum of 8.4×10^{-4} Ω cm^2, is somewhat higher than other reported literature values for the Ni/Ti/Al contacts. For example, Konishi et al. obtained a value of 6.6×10^{-5} Ω cm^2 for Ni/Ti/Al (same thicknesses) annealed at 800 °C under UHV conditions [197]. Tsukimoto et al. achieved a similar value, 7×10^{-5} Ω cm^2, by annealing Ni/Ti/Al (35 nm/50 nm/300 nm) at 800 °C for 30 min, also under UHV conditions [198]. The higher contact resistance obtained in this work may stem from the annealing, which was performed under flowing Ar in a rapid thermal annealing chamber. The chamber likely contains residual oxygen, which would contribute to contact oxidation and subsequent resistance increase. The high vapor pressure of Al makes UHV annealing an unattractive option due to significant evaporation of Al, but these referenced works indicate that it may reduce contact resistance nonetheless.

The mechanism of ohmic contact formation of Al-containing metals to p-type 4H-SiC remains controversial, with explanations varying from Al interdiffusion causing locally high p-doping at the SiC interface to interface Al intrusions leading to field emission to reduction of barrier height from the formation of intermetallic species [145, 146, 200]. Further analysis, such as elemental depth profiling is necessary to elucidate the mechanisms responsible for both ohmic contact formation in this work, and degradation of contact performance at 600 °C. Nonetheless, the initial data is promising for the use of Al/Ti/Ni contacts to p-type 4H-SiC for high temperature applications.

10 Conclusions and future work

On-chip micro-supercapacitors present a promising avenue of research for the powering of microscale devices. The electrostatic charge storage mechanism of supercapacitors make them more attractive than their battery counterparts for applications which require high power loads or frequent cycling. In order to improve the energy and power density of proposed micro-supercapacitor devices, the electrode and electrolyte must both be engineered to increase electrode surface area, control and utilize pseudocapacitive charge transfer reactions, improve the electrochemical potential window, and increase the electrode and electrolyte conductivities. This dissertation presents efforts to achieve these goals through scalable fabrication processes of photoresist-derived porous carbon electrodes, transfer of porous carbon electrodes to flexible substrates, electrochemical activation to improve carbon electrode pseudocapacitance without negatively affecting cycle lifetime, fabrication of all solid-state VACNT/ionogel flexible micro-supercapacitors, and fabrication of templated 3D graphene electrodes. Furthermore, high temperature micro-supercapacitor materials are discussed, particularly yttria-stabilized zirconia solid-state electrolyte. Finally, in order to enable full device fabrication of high temperature micro-supercapacitors, as well as other microdevices, the contact metallization stability of SiC at high temperatures is explored. Further areas for study include the tuning of energy and power density of carbon-based electrodes through modification of parameters such as material porosity and conductivity, conformal deposition of ceramic electrolytes (like YSZ) onto high surface area electrode structures, and integration of energy storage on-chip with energy harvesters. Further study into the mechanisms of various metal SiC contacts at high temperature is also necessary in order to properly engineer methods for improving the contact stability of various metal systems on both n-type and p-type SiC. Hopefully, through intelligent design based on these fundamental learnings, high energy and power devices can be fabricated for a variety of applications in both ambient and harsh environments.

11 Bibliography

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