Title

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Journal

Applied Physics Letters, 115(6)

ISSN

0003-6951 1077-3118

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Publication Date

2019-08-05

DOI

10.1063/1.5103268

Peer reviewed

Applied Physics Letters

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Cite as: Appl. Phys. Lett. **115**, 062101 (2019); https://doi.org/10.1063/1.5103268
Submitted: 25 April 2019 . Accepted: 12 July 2019 . Published Online: 06 August 2019

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Applied Physics Letters ARTICLE scitation.org/journal/apl

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Submitted: 25 April 2019 · Accepted: 12 July 2019 ·
Published Online: 6 August 2019

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ABSTRACT

Cadmium arsenide (Cd_3As_2) is a three-dimensional Dirac semimetal with many unique electronic properties that are of interest for future device applications. Here, we demonstrate field effect transistors using Cd_3As_2 as the channel material. We show that current densities exceed 5 A/mm and that very low contact resistances can be achieved even in unoptimized device structures. These properties make Cd_3As_2 of great interest for future high-speed electronics. We report on the current modulation characteristics of field effect transistors as a function of temperature. At low temperatures, the modulation exceeds 70%. We discuss material and device engineering approaches that can improve the device performance at room temperature.

Three-dimensional topological semimetals promise numerous opportunities for next-generation electronic and photonic devices. For example, thin films of the three-dimensional Dirac semimetal Cd_3As_2[1–4] exhibit room temperatures mobilities of 20 000 $cm^2/V\,s$ (Ref. 5) and, at cryogenic temperatures, mobilities of up to 9×10^6 $cm^2/V\,s$ have been reported in bulk crystals.[6] Moreover, reported Fermi velocity values for Cd_3As_2 are as high as 1.5×10^6 m/s.[3] This is higher than that of most other Dirac semimetals and also exceeds the saturation velocities of carriers in traditional semiconductors used in radio frequency (RF) applications (see Table I). While a large Fermi velocity is usually associated with a low density of states,[7] Cd_3As_2 possesses two Dirac nodes ("valleys") within the first Brillouin zone, thereby effectively doubling the charge densities that can be accommodated. Furthermore, Cd_3As_2 can be integrated with conventional semiconductors in epitaxial heterostructures, using established thin film deposition methods, such as molecular beam epitaxy (MBE).[5] These properties make Cd_3As_2 of great interest to future high-speed electronic devices, such as field effect transistors (FETs) that can exhibit high current densities and transconductance, which are needed for next-generation RF technologies.

To realize high-performance FETs with Cd_3As_2 channels, many additional materials and device parameters, such as contact resistances and current modulation, are important and must be evaluated. Moreover, to understand the device performance, the unique characteristics of three-dimensional Dirac semimetals must be taken into consideration. For example, while there is no bandgap in the bulk material, the Dirac nodes become gapped in thin (<60 nm) Cd_3As_2 films.[8–10] Even if the bulk is gapped, however, Cd_3As_2 still possesses surface states that are inherent to the topological invariant.[1] In previous low-temperature transport studies, the two-dimensional Dirac nature of these surface states was demonstrated.[8–10] In thin films, an electric field applied via a top gate is therefore expected to mostly modulate the carriers in the surface states. In the present study, we demonstrate FETs using thin, (112)-oriented Cd_3As_2 channels. We evaluate the FET characteristics and discuss materials and device parameters that determine the FET performance.

Figure 1(a) shows a schematic of the heterostructures used in this study, which consisted of thin (112)-oriented Cd_3As_2 films, grown on (111)GaAs substrates with a 130 nm-thick (111)GaSb buffer layer by molecular beam epitaxy (MBE). Growth parameters, the film's structure and materials properties have been reported elsewhere.[5,11] Unless stated otherwise, the Cd_3As_2 film thickness was 30 nm. Several different types of devices were processed, including Hall bars, transmission lines (TLM), and FETs. For all devices, the ohmic contacts consisted of Au/Pt/Ti (200 nm/50 nm/50 nm) layers, which were deposited using e-beam evaporation. Active device areas were isolated using Ar-ion milling. Resistance and Hall measurements were carried using 100 μm × 50 μm Hall bar structures. For the FETs [see Fig. 1(b) for a schematic], a 20 nm-thick aluminum gate oxide was deposited using atomic layer deposition (ALD). Immediately before gate oxide

TABLE I. Fermi or saturation velocities for different topological materials and semiconductors reported in the literature.

Material	Material class	Fermi or saturation velocity ($\times 10^6$ m/s)	References
Graphene	2D Dirac semimetal	1.05	19
Cd_3As_2	3D Dirac semimetal	1.5	3
Na_3Bi	3D Dirac semimetal	0.425	20
TaAs	Weyl semimetal	0.36	21
Bi_2Se_3	3D topological insulator	0.54	22
Bi_2Te_3	3D topological insulator	0.4	23
InAs	Semiconductor	0.8	24
GaAs	Semiconductor	0.1	25
InP	Semiconductor	0.2	26
GaN	Semiconductor	0.2	27

deposition, the sample surface was cleaned using the trimethylaluminum precursor,[12] which improved the gate leakage and carrier mobility. Due to the limited thermal stability of Cd_3As_2, ALD was performed at a low temperature (120 °C), which limits the quality of the gate oxide. Finally, Au/Pt/Ti (200 nm/50 nm/50 nm) metal layers were deposited as gate contacts. Hall and transistor measurements as a function of temperature were carried out in a Physical Property Measurement System (Quantum Design Dynacool). The current-voltage (I-V) characteristics were measured using a Keithley 4200A-SCS parameter analyzer. Room temperature I-V and capacitance-voltage (C-V) measurements were carried out using semiconductor parameter analyzers (HP 4155B and HP B1500A, respectively).

At room temperature, the sheet carrier density was $1.5 \times 10^{12}\,cm^{-2}$ and the Hall mobility was $4000\,cm^2/V\,s$ for devices without a gate oxide. As shown in Fig. 1(c), carrier freeze out was observed upon lowering the temperature, while below 80 K, the carrier density became independent of the temperature. Following our earlier studies, the thermally activated carriers are ascribed to bulk carriers, while the carrier density in the gapless surface states is relatively independent of the temperature.[8,9] Figure 1(d) presents a schematic band picture for this case. Figure 1(c) also shows that the sheet carrier density increases by $\sim 2.5 \times 10^{12}\,cm^{-2}$ after ALD, similar to our previous observation[10] (also see the supplementary material for more detailed information). Most of these excess carriers do not freeze out, indicating that they mostly reside in the surface states.

Figure 2(a) shows TLM data from two Cd_3As_2 films having different thicknesses. The 65-nm-film showed a very low contact resistance (R_c) of 0.34 Ω mm. The higher contact resistance of the thinner (30 nm) film (1.15 Ω mm) is expected, because of the lower sheet carrier density. We note that there are multiple approaches that are commonly used to reduce contact resistances in devices, such as optimizing ohmic metal stacks, anneals, gate-recessed device structures, and selective doping of source and drain regions, all of which can be implemented for Cd_3As_2 FETs as well. Figure 2(b) shows two terminal I-V characteristics of a 30-nm-thick film. The current density exceeds 5 A/mm at a carrier density $5 \times 10^{12}\,cm^{-2}$. Such extremely high current densities are of great interest for future high frequency transistors.

Figure 3(a) shows an optical micrograph of a FET. The drain-current vs gate voltage (I_D-V_G) characteristics are shown in Fig. 3(b). The current density is 0.5 A/mm and increasing V_D will further increase I_D because the transistor is still operating in the linear region. The current modulation, however, is only 10% for this particular device.

To understand the factors limiting current modulation, Fig. 3(c) shows the I_D-V_G characteristics of a long channel (300 μm) device at different temperatures (2 K to 300 K). The current modulation increases significantly when the temperature is decreased. In addition, at low temperatures, the I_D-V_G characteristics show an upturn at negative bias, consistent with accumulation of holes when the Fermi level crosses the Dirac point of the surface states.[10] Due to the lower hole mobility,[13] the upturn is quite small. High magnetic field Hall measurements provide further evidence for holes at negative voltages (see the supplementary material). The signatures of hole carriers vanish above 80 K, which is the temperature when thermally excited bulk carriers start to overwhelm the transport.

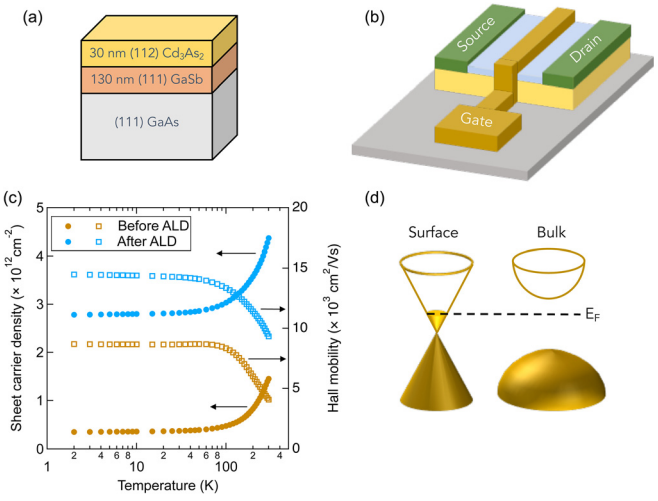

FIG. 1. (a) Schematic of the heterostructure. (b) Schematic of a Cd_3As_2 channel FET. (c) Temperature dependence of the sheet carrier densities determined from the Hall effect and extracted mobility. (d) Proposed schematic of the relevant electronic states.

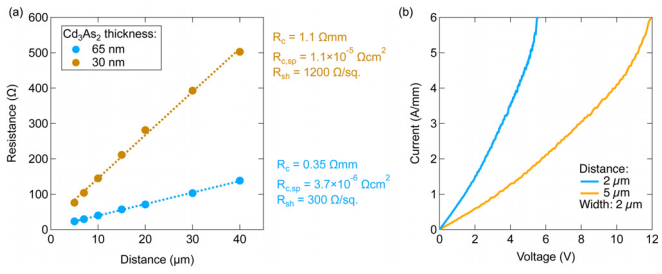

FIG. 2. (a) TLM data used for determining the contact and sheet resistances (R_{sh}), which are given in the legend for two samples with different Cd_3As_2 thicknesses. $R_{c,sp}$ is the specific contact resistance. (b) Two terminal I-V measurements performed on a 30-nm-thick Cd_3As_2 film.

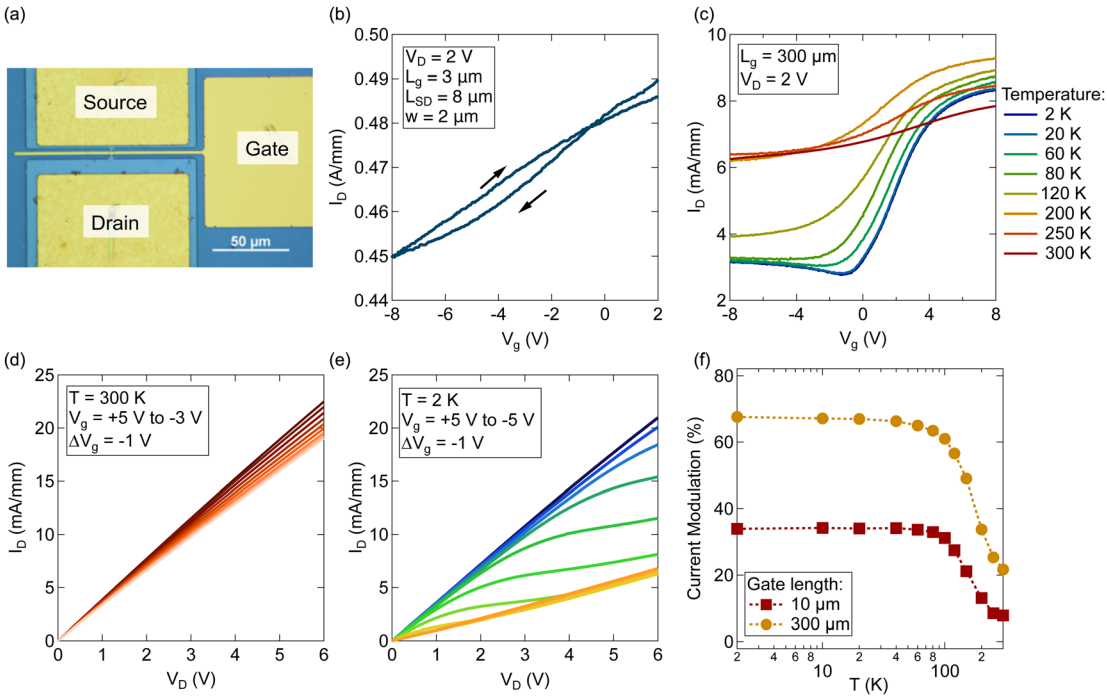

FIG. 3. (a) Optical micrograph of a Cd_3As_2 FET. The gate length (L_g) is 3 μm, the source-drain separation is 8 μm, and the width of the channel is 2 μm. (b) I_D-V_G characteristics of a FET measured at 300 K. (c) I_D-V_G characteristics of a FET with $L_g = 300$ μm as a function of temperature. (d) and (e) I_D-V_D characteristics at 300 K and 2 K of a FET with $L_g = 300$ μm. (f) Temperature dependence of the current modulation of Cd_3As_2 FETs with different gate lengths.

Figures 3(d) and 3(e) show the I_D-V_D characteristics of the same device measured at 300 K and 2 K, respectively. The device performance markedly improves as the temperature is lowered. The absence of saturation of I_D is consistent with the expectation for gapless Dirac surface states. Figure 3(f) summarizes the current modulation at different temperatures. The longer channel device shows a higher current modulation, which reaches 70% at 2 K. The current modulation remains high up to 80 K and then decreases.

The results suggest that one of the main causes for the low current modulation at high temperatures is the thermal activation of bulk carriers. The gapless Dirac surface states screen the applied electric field and limit the modulation of the bulk carriers by V_G. Below 80 K, the contribution of the bulk carriers is minimized, a large current modulation can be achieved, and V_G tunes the Fermi level through the Dirac point of the surface states. The current modulation is furthermore affected by traps at the interface between the low temperature ALD oxide and the Cd_3As_2 channel. Specifically, the amount of charge modulated in the capacitance-voltage (C-V) measurements is much higher than the current modulation (see the supplementary material). This shows that a substantial fraction of V_G modulates the charge trapped in the interface states rather than the charge in the channel. Charge traps at the interface or near the interface region give rise to the hysteresis seen in Fig. 3(b).

The results point to specific steps that can be taken to improve the room temperature performance of Cd_3As_2-based FETs. The main challenge that needs to be addressed is the low current modulation. One approach is to use thinner channels, which lower the bulk carrier density by increasing the bulk gap. The bulk bandgap can also be increased by epitaxial strain. Furthermore, to improve current modulation, the oxide-film interface needs to be optimized to reduce the high trap densities that are associated with the low temperature ALD process that was used here. These two steps for improving modulation promise a large benefit for the figure of merit of RF devices. For example, a modest improvement in the room temperature current modulation (to about 30%–50%) over the present results could lead to large improvements of the cut-off frequency, even without a gap, as has been shown for graphene devices.[14–17] For very thin films, gaps can also be obtained in the surface states.[18] This reduces screening by the surface carriers and should also allow for Cd_3As_2 FETs to reach saturation and turn off.

In summary, Cd_3As_2 FETs show extremely high current densities and low contact resistances, which are very promising for RF applications. Gapless surface states, residual bulk carriers, and high trap densities at the interface with a low-quality dielectric limited the current modulation. The tunability of the electronic states of three-dimensional Dirac semimetals affords numerous possible approaches to overcome these limitations, some of which we have suggested here.

See the supplementary material for data showing the influence of pre-ALD surface treatments, results from C-V measurements, FET transconductance data, a discussion of the influence of lateral fields on the FET performance, and results from Hall measurements at larger magnetic fields.

This research was supported by the U.S. Army Research Office (Grant No. W911NF-16-1-0280) and the SRC/DARPA funded JUMP program (Task ID 2778.032). This work made use of the MRL Shared Experimental Facilities, which are supported by the MRSEC Program of the U.S. National Science Foundation under Award No. DMR 1720256.

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