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Los Angeles

An on-chip ESD sensor for use in advanced packaging

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy in Electrical and Computer Engineering

by

Kannan Kalappurakal Thankappan

2021

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Abstract of the Dissertation

An on-chip ESD sensor for use in advanced packaging

by

Kannan Kalappurakal Thankappan

Doctor of Philosophy in Electrical and Computer Engineering

University of California, Los Angeles, 2021

Professor Subramanian S. Iyer, Chair

Electrostatic discharge (ESD) in integrated circuits (ICs) occurs due to charge transfer between two components in close proximity with voltage imbalance. As a result of an ESD event, a high transient current (up to few tens of Amps) and large voltage (up to several tens of kV) can develop between the two components. This fast (~ 150 *ns*) transient phenomenon can cause serious damage or degrade the performance of affected ICs. ESD results in about 35% of IC field returns and is the cause of several billion dollars loss to the semiconductor industry per year. Even though most modern ICs have on-chip ESD protection circuitry embedded, static charge accumulation during transport and handling may exceed the limits of ESD protection and cause damage to the ICs. Advanced packaging schemes existing today are not amenable to rework if one or more dielets are ESD compromised. An on-chip ESD sensor would help in identifying and preventing the assembly of ESD compromised dielets in any advanced packaging schemes. In this dissertation, two approaches for on-chip ESD detection that can be employed on any die are presented: variable dielectric width capacitor, and vertical MOSCAP array. The variable dielectric width capacitor approach employs metal plates terminated with sharp corners to enhance local electric field and facilitate easy breakdown of the thin dielectric between the metal plates. The vertical MOSCAP array consists of a capacitor array connected in series. Both approaches were designed, simulated, fabricated, and experimentally characterized on GlobalFoundries 22 *nm* fully depleted silicon-on-insulator (FDSOI) technology. The designed vertical MOSCAP arrays were able to detect ESD events ≥ 6 V while the variable dielectric width capacitor based sensor is able to detect ESD volt-

ages $\geq 40\ V$. A Bayesian method was formulated for the estimation of ESD voltage using the sensors and experimentally validated. Mathematical formulation for sensitivity and confidence in ESD voltage estimation was developed which matches the results of Monte-Carlo simulations. A sensitivity of 1 parts per million is achievable with 4 sensors for an ESD voltage detection of $7.4\ V$. The simulation study further indicates that the error in voltage estimation can be reduced from 25% to 8% by increasing the number of sensors from 1 to 8.

Finally, a novel high-power delivery network for the Silicon interconnect fabric (Si-IF), a heterogeneous wafer-scale integration platform, is also proposed. The system is capable of 42 kW output power delivery to dielets when supplied with a 50-kW input power. Power delivery network (PDN) modelling and simulations have been carried out to determine impedance spectrum and I^2R losses. A 100 W experimental prototype was designed and evaluated to check the feasibility of the proposed architecture.

The dissertation of Kannan Kalappurakal Thankappan is approved.

Dwight Streit

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University of California, Los Angeles

2021

To my mother

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Publications

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Kannan K.T., Subramanian Iyer, "ESD challenges in Wafer Scale Systems", Govt. Microcircuit Applications and Critical Technology Conference (GOMACTech), Virtual conference, March 29-April 1, 2021.

Ujash Shah*, Kannan K.T.*, Timothy S. Fisher, Subramanian Iyer, "Power Delivery and Thermal Management for Heterogeneous Wafer-scale Systems", Govt. Microcircuit Applications and Critical Technology Conference (GOMACTech), Virtual conference, March 29-April 1, 2021 (* denotes equal contribution)

Kannan K.T., Subramanian Iyer, "Deep Trench capacitors in Silicon Interconnect Fabric", IEEE 70th Electronic Components and Technology Conference (ECTC), May 26-29, 2020, Lake Buena Vista, FL.

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Siva C. Jangam, Adeel Bajwa, Kannan K.T., Premsagar Kittur, Subramanian S. Iyer, "Electrical Characterization of High Performance Fine Pitch Interconnects in Silicon Interconnect Fabric", IEEE 68th Electronic Components and Technology Conference (ECTC), May 29-June 1, 2018, San Diego, CA.

Siva C. Jangam, Adeel Bajwa, Kannan K.T., Subramanian S. Iyer, "Characterization of Fine-Pitch Interconnections ($\leq 10\mu m$) on Silicon Interconnect Fabric for Heterogeneous Integration", International Symposium on Microelectronics, Vol. 2018. No. 1. International Microelectronics Assembly and Packaging Society(IMAPS), May 29-June 1, 2018, San Diego, CA.

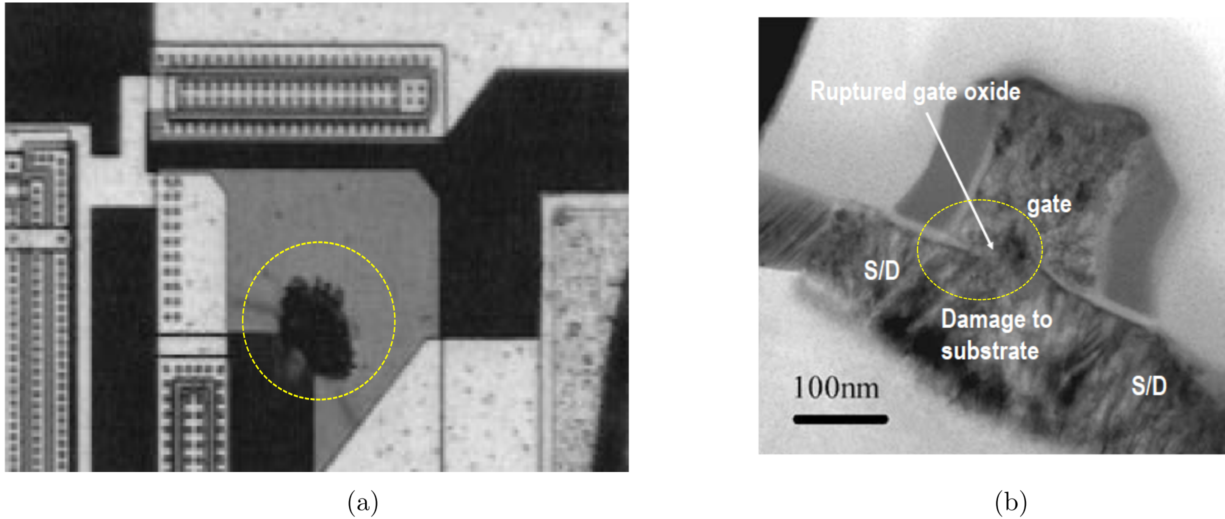
Chapter 1

Introduction

1.1 Electrostatic discharge

Electrostatic discharge (ESD) has become one of the most prevalent problems in the semiconductor industry. ESD happens everywhere – industry, home, business, during transport and so on. ESD occurs due to electrostatic charge transfer between two components in close proximity with voltage imbalance. ESD can be initiated by a direct contact or a dielectric breakdown between the two components. As a result of an ESD event, a high transient current (up to few tens of Amps) and large voltage (up to several tens of kV) can develop between the two components. This fast ($\sim 150\ ns$) transient phenomenon can cause serious damage or degrade the performance of affected ICs [1]. ESD is different from electromagnetic interference (EMI) which occurs due to electric and magnetic field coupling between a source and a victim equipment/ device (the field coupling can be through radiation, inductive/capacitive or direct contact). An ESD event can cause local damage to metals, oxides, junctions, and other device components (Fig. 1.1), resulting in either complete or partial device failure [2]. About 35 % of the IC field returns are reported to be ESD induced, with annual costs estimated to be several billions of dollars [1, 3].

There are three principle sources of charge [2] which can give rise to damaging ESD



(a) (b)

Figure 1.1: Damage in ICs [3, 4] (a) Blown polysilicon resistor due to ESD (b) Ruptured gate oxide

events:

1. A charged person/equipment coming in contact with a device and discharging the stored charge to or through the device to ground. People and equipment can become charged while interaction (contact and separation) with another object/material. For example, a person walking on a floor can generate voltages up to 4 kV depending on the footwear used [5, 6]. When the person comes in contact with an electronic device, charge transfer to the device can occur, possibly causing device malfunction.

2. The device itself can act as one plate of a charged capacitor. When the device comes in contact with an effective ground, the discharge pulse can create damage to the device.

3. A device in the electrostatic field associated with a charged object. The device in this field can have a potential induced across it, and upon contact with a grounded surface, electric discharge can occur, which may cause damage.

Maxwell's method [7] is used to analyse and determine device potentials and the transfer of charge during typical discharges. A system involving n multiple conductors can be

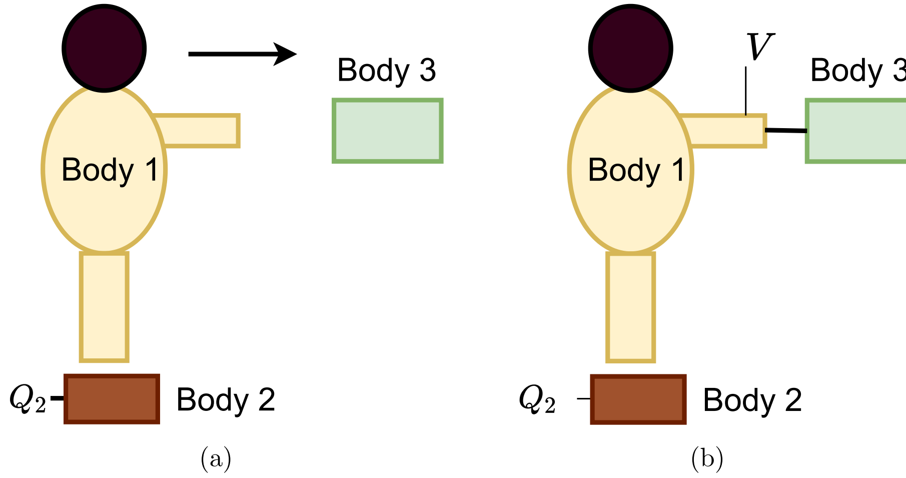


Figure 1.2: Charged human body and floating device (a) approach (b) contact. Adapted from [7]

described by the Maxwell's equations as

$$\begin{aligned}
Q_1 =& C_{11}V_1 + C_{12}V_2 + \cdots + C_{1n}V_n, \\
Q_2 =& C_{21}V_1 + C_{22}V_2 + \cdots + C_{2n}V_n, \\
& \cdots\cdots \\
Q_n =& C_{n1}V_1 + C_{n2}V_2 + \cdots + C_{nn}V_n,
\end{aligned}$$

where $C_{11}, C_{22}, ...C_{nn}$ etc are the coefficients of self-capacitance, and $C_{12}, ..C_{1n}$ etc are coefficients of mutual capacitance. As an example, consider, the following case where a human body with insulated shoes walking over a carpet is approaching a semiconductor device. Triboelectrification between the carpet and shoes results in shoes getting charged to equal and opposite polarity to charge on carpet. Two cases are possible: (i) The semiconductor device is floating and (ii) The semiconductor device is grounded.

Case-1 (device is floating): The system of Maxwell's equations are given below for the human body approaching the device [7]. Here body-1 refers to human body, body-2 refers to the shoes, and body-3 refers to the device, as shown in Fig. 1.2(a)

$$0 = C_{11}V_1 + C_{12}V_2 + C_{13}V_3 \tag{1.1}$$

$$Q_2 = C_{21}V_1 + C_{22}V_2 \tag{1.2}$$

$$0 = C_{31}V_1 + C_{33}V_3 \tag{1.3}$$

If it is assumed that there is negligible coupling of electric flux from body-2 to body-3 ($C_{23} = C_{32} = 0$), the bulk of electric flux associated with body-2 (shoes) couples to body-1 ($C_{12} = -C_{22}$), and the bulk section of human body is greater compared to the shoes ($C_{11} > C_{22}$)

$$V_1 - V_3 = \frac{Q_2(1 + C_{13}/C_{33})}{C_{11} - C_{13}^2/C_{33}} \tag{1.4}$$

Assuming body-3 to be small compared to body-1, this implies that $C_{13} = -C_{33}$ which makes the potential difference $V_1 - V_3$ to be zero. So, for the charged human body approaching a floating integrated circuit, a discharge will probably not occur. When contact is made between body-1 and body-3 as shown in Fig. 1.2(b) the system of equations gets modified as follows:

$$q_1 = C_{11}V_1 + C_{12}V_2 + C_{13}V_3 \tag{1.5}$$

$$Q_2 = C_{12}V_1 + C_{22}V_2 \tag{1.6}$$

$$q_3 = C_{13}V_1 + C_{33}V_3 \tag{1.7}$$

But $V_1 = V_3 = V$, and $q_1 + q_3 = 0$, thus the system equations can be rewritten as:

$$q_1 = C_{11}V + C_{12}V_2 + C_{13}V \tag{1.8}$$

$$Q_2 = C_{12}V + C_{22}V_2 \tag{1.9}$$

$$q_3 = C_{13}V + C_{33}V \tag{1.10}$$

The solution then yields:

$$V = \frac{-C_{12}/C_{22}Q_2}{C_{11} + 2C_{13} + C_{33} - C_{12}^2/C_{22}} \tag{1.11}$$

Plugging in $C_{12} = -C_{22}$ and $C_{11}\gg$ C_{22}:

$$q_3 = \frac{(C_{13} + C_{33})Q_2}{C_{11} + 2C_{13} + C_{33}} \tag{1.12}$$

If body-3 is very small compared body-1 ($C_{13} = -C_{33}$), the charge transfer $q3$ then approaches zero.

Case-2 (device is grounded): When body-3 is grounded, the system of Maxwell's equation Fig. 1.3(a) can be written as:

$$0 = C_{11}V_1 + C_{12}V_2 \tag{1.13}$$

$$Q_2 = C_{12}V_1 + C_{22}V_2 \tag{1.14}$$

$$Q_3 = C_{13}V_1 \tag{1.15}$$

Here it is assumed that there is negligible coupling of electric flux from body-2 to body-3 ($C_{23} = C_{32} = 0$). Body-1 potential then comes out to be:

$$V_1 = \frac{Q_2}{C_{12} - (C_{11}C_{22})/C_{12}} \tag{1.16}$$

For typical applications where: $C_{12} = -C_{22}$ and $C_{11}\gg$ C_{22}:

$$V_1 = \frac{Q_2}{C_{11}} \tag{1.17}$$

As body-1 approaches body-3, the discharge can be modelled by a fine conductor connecting the two bodies (Fig. 1.3(b)). Body-1 and body-3 are now at same ground potential. The system of equations then becomes:

$$Q_1 = C_{12}V_2 \tag{1.18}$$

$$Q_2 = C_{22}V_2 \tag{1.19}$$

$$Q_3 = C_{23}V_2 = 0 \tag{1.20}$$

$$Q_1 = \frac{C_{12}Q_2}{C_{22}} \tag{1.21}$$

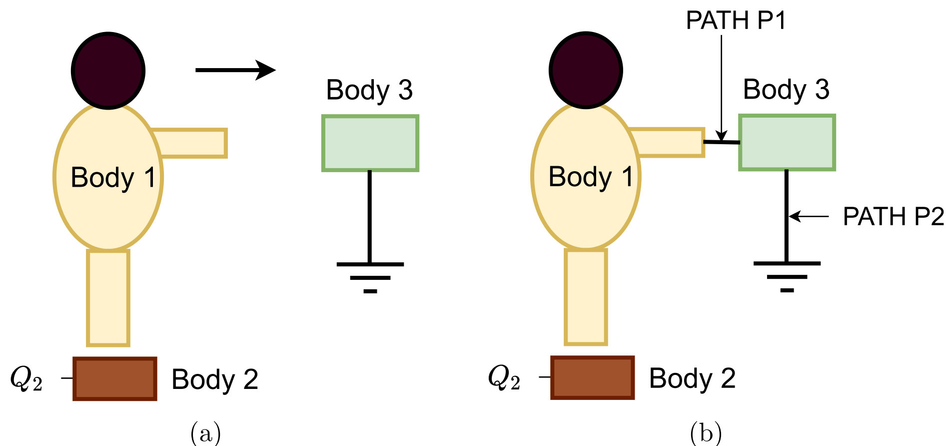


Figure 1.3: Charged human body and grounded device (a) approach (b) contact. Adapted from [7]

if $C_{12} = -C_{22}$,

$$Q_1 = -Q_2 \tag{1.22}$$

The charge transferred to the device would be $-Q_2$. If the device is approached in a grounded state, a charge equal to that trapped on the shoes of the human body is transferred. In summary, the potential difference between the device and the conductor before contact, and the amount of charge transferred during the contact, depend on the system capacitance coefficients and the electrical state of the conductor [7, 8].

1.1.1 ESD models

To emulate real life ESD events, ESD models are used. Three basic models are used: (i) the human body model, (ii) machine model, and (iii) charged device model.

The human body model (HBM) emulates a charged human body coming in contact with an electronic device. HBM is modelled by a 150 pF capacitor, which is charged to a high-voltage and then discharged by a switch(S) through a 1-2 $k\Omega$ series resistor to the device under test to ground. The test setup and typical waveform for an HBM [1] is shown in Figure 1.4

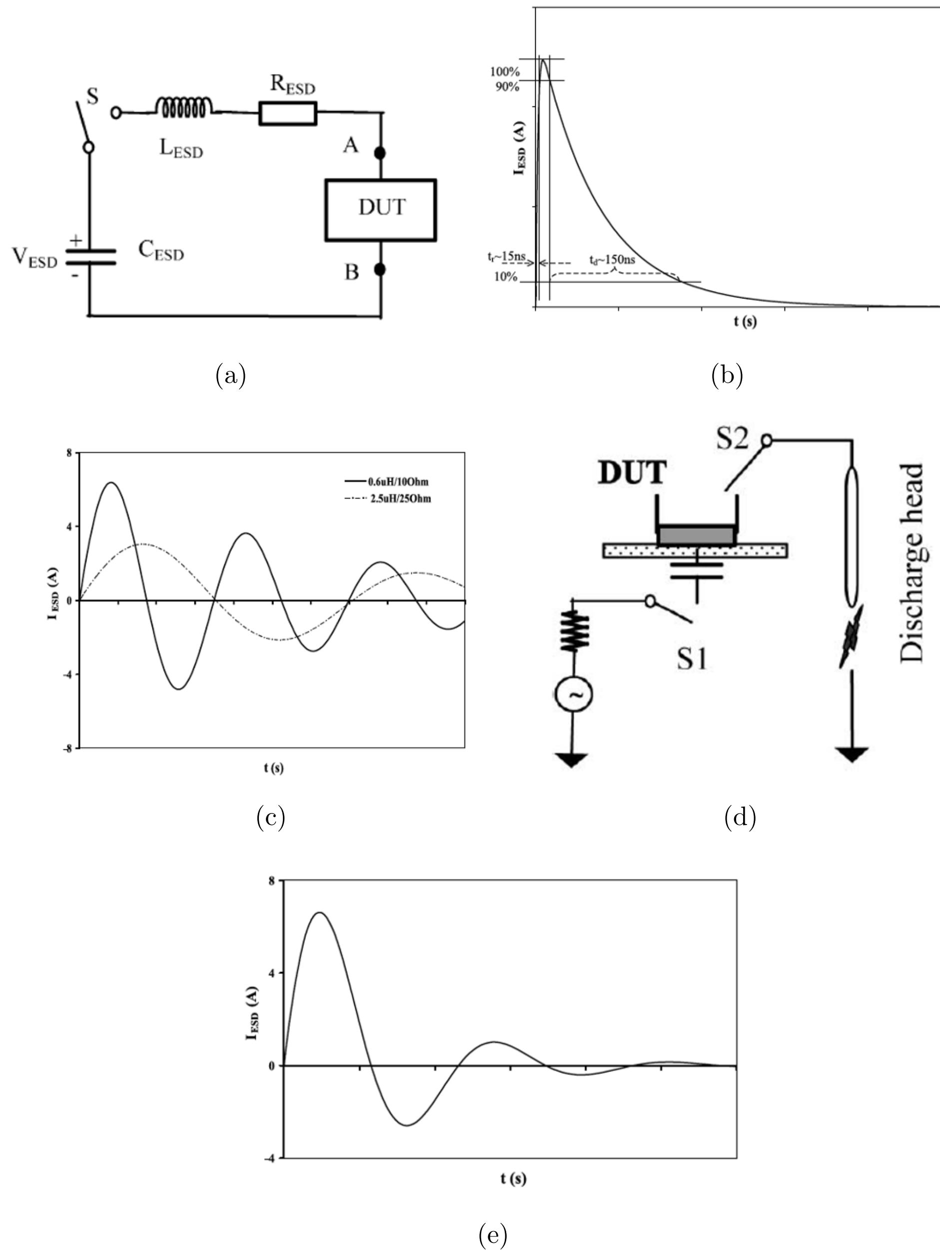


Figure 1.4: ESD models [1] (a) Test setup for HBM and MM (b) Typical HBM discharge waveform (c) Typical MM discharge waveform (discharge voltage level $\sim$ 400 V) (d) Test setup for CDM (e) Typical CDM discharge waveform at a discharge level of 1100 V

The machine model (MM) emulates the case where a charged machinery comes in contact with the IC, for example during automated process in IC production and assembly. A MM test setup consists of a high-voltage supply in series with a resistor that charges a capacitor (100 pF) to a high voltage. The discharge of the capacitor to the device under test (DUT) occurs on closure of a switch(S) that disconnects the capacitor from the high voltage supply and connects it to the DUT through a negligible resistor and inductor. Typical MM ESD events produce an oscillatory discharging waveform with a high peak current and shorter rise time as compared to the HBM (Fig. 1.4(c)).

The charged device model (CDM) simulates self-induced discharging of devices where ungrounded electronic parts become charged during manufacturing and assembly and later discharge to a grounded surface. A CDM test setup is shown in Figure 1.4(d). Initially, switch S1 is closed and S2 is open which charges the DUT to a high voltage. In the second stage, S1 is open and S2 is closed which discharges the DUT pin. CDM typically has a fast impulse-like waveform as shown in Figure 1.4(e). In CDM, charge originates within the device due to self-induced charging and subsequent discharging through the pin. In HBM and MM, the charges originate from an external source. Device internal protection structures sometimes becomes ineffective against CDM due to the internal charge generation. Voltage drops experienced during CDM due to the transient high current can damage the internal structure of a device [1, 9].

1.1.2 ESD protection

Fundamentally, two approaches are employed in protecting electronic devices from ESD: (i) reducing likelihood of ESD and (ii) adding ESD protection circuitry on to the electronic devices. ESD occurs as a result of a voltage imbalance. An ESD event occurs in four stages: 1) generation of charge, 2) transfer of charge due to voltage imbalance, 3) conduction of charge, and 4) damage due to charge transfer and associated transient current and voltage. In order to reduce the likelihood of ESD, charge generation mechanisms which causes ESD have

to be reduced. The first method involves use of protection equipment to control generation of static charges. This includes room ionizers, local ionizers, ESD wrist straps etc. The second method adds additional circuit elements on ICs which provides an alternate path for charge conduction in case of an ESD event [10, 11].

1.1.2.1 Workstation and room level ESD controls

An ESD event occurs when there is a voltage difference between two bodies and a low impedance connection exists between the two bodies, allowing for charge transfer which may cause damage to one or the two bodies involved. If the voltage difference between the two bodies is small, minimal charge transfer happens. Similarly, if the impedance connecting the two bodies is high, charge transfer might not happen. These two principles are used in ESD prevention mechanism i.e., to make the generated/developed voltage to be low enough and to provide a high impedance path between the two bodies, so that minimal charge transfer happens [10].

Moisture content in the air plays a key role in determining the magnitude of charge developed on an object, as it defines the electrical resistance of the air. In dry areas, large charge build-up can happen before they are dissipated. If the moisture content is high, charge is bled off through the air easily. If the moisture content is low, it allows for the charge to increase on objects without being dissipated. ESD events are more common in winter because the air is dry and the moisture content is low in air, which allows for charge build-up and generation of high ESD voltages. The typical safe working range of relative humidity is 30-70 % [12, 13].

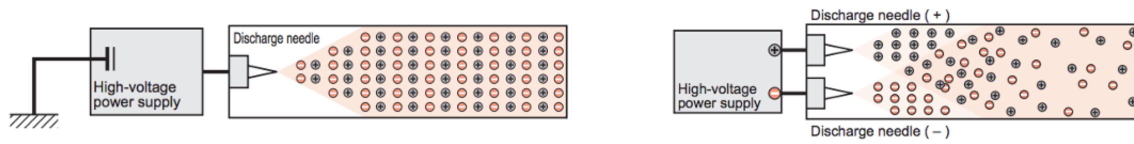
Air conductivity can be controlled by injecting conductive species in the air. In order to ensure that no net charge is introduced, charges must be injected in balance (equal number of positive and negative charges). Room ionizers are used to do this, and they basically remove static charges from surfaces that cannot be grounded. Ionizers neutralize objects and people entering a work area. The two important aspects of air ionizers are: (i) charge

neutralization time, which is the time require to neutralize a given amount of charge by the ionizer, and (ii) ion-imbalance, which provides a measure of ionizers' ability to generate an equal amount of positive and negative charges. If there is an imbalance, potential gradients form in the air, impacting the ionizer performance [10, 14].

Ionizers are classified based on the method used for charge generation – electrical or nuclear. Electrical ionizers can further be classified into AC and DC ionizers (Figure 1.5(a)). In AC ionizers, an AC voltage is applied to the discharge needles and produces positive ions and negative ions alternately in each half cycles. In DC method, either positive or negative ions are produced depending on the polarity of the DC voltage applied. Thus both positive and negative voltage sources are required to maintain charge neutrality. AC method creates positive ions and negative ions efficiently and generates a stable environment with high ion flux density. However, the DC method generates positive ions and negative ions constantly and doesn't include a generation cycle like the AC method. Thus the neutralization rate of DC ionizer is faster [15]. Nuclear ionizers use a nuclear source for ionization. For example, an Alpha ionizer (Figure 1.5(b)) utilizes the nuclear source Polonium 210, which emits alpha particles. The alpha particles (helium nucleus) collide with air molecules, and knock out electrons over a distance approximately 3 cm [16]. Alpha ionization is used commercially for applications involving explosive or flammable environments.

Typical ionizers include over-head ionizers [17], bench top ionizers [18], and gun ionizers [19] as shown in Figure 1.6. These can cover high voltage ranges (1000s of Volts) with a balance of $\pm$ 1 Volt and a discharge time in the range of few seconds (time taken by the ionizer to discharge a test object from 1000 V to 100 V)

Other major sources of charging in a manufacturing area are floors and carpets [20]. Here the use of anti-static finishes can reduce charge generation. The surface should neither induce a static charge on the parts nor provide a rapid discharge path [10]. The workstation should be designed so as to minimize static charge generation and transfer (Fig. 1.7). The use of highly conductive work surfaces (for example stainless steel) can create a hazard. This is because a metal/ high conductive surface can act as a large charge sink without any



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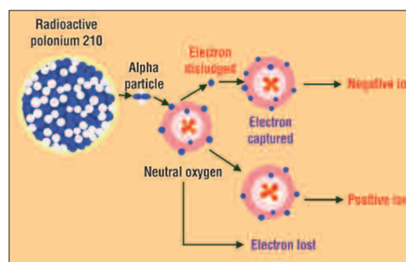


(b)

Figure 1.5: Types of ionizers [15, 16](a) DC and AC static ionizers (b) nuclear ionizer principle

Figure 1.6: Over-head [17], bench top [18] and gun ionizers [19] (from left to right)

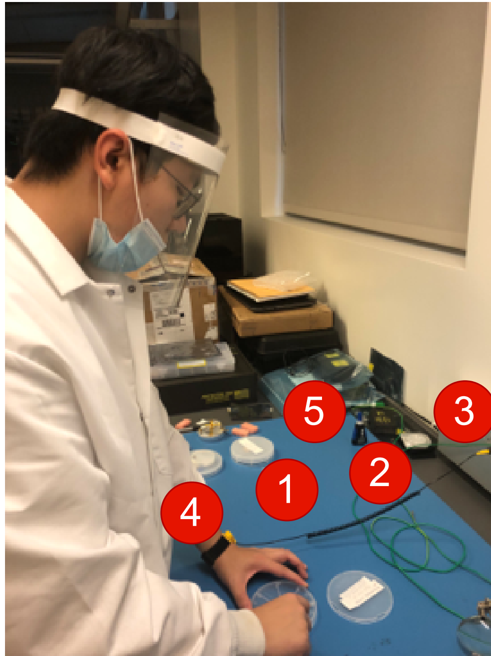
significant change in its potential and a rapid discharge from a charged object to metal/ high conductive surface due to the potential difference may create spark/ hazards. A static dissipative surface with a sheet resistance of 10^5–10^9 $\Omega/\square$ is effective in providing an ESD safe environment [21, 22].

Personal ESD protection equipment includes ground straps which dissipate static charge on the body to ground in a controlled manner [23]. Clothing can also cause ESD damage. For example, synthetic fibres used in many clothes can often generate charge that can damage equipment. In winter, sweaters worn can cause charging of human body during normal body movements like searching for a tool [10]. Providing a common ground area in the workplace minimizes risk of an ESD event. All elements of the work area that are connected should be brought to a common ground point to ensure same electrical potential. Similarly, in the work place ESD safe chairs can be used, which come with metal casters and metal footplate to conduct static charge away from a user's body to ground.

For storage and transport of ESD sensitive parts, special coatings or metal foils can be used to reduce the generated static or to shield from external fields [24]. Static-shielding bags creates a Faraday cage effect for the electronics inside them. Shielding bags protects electronics inside them from a direct electrostatic discharge and also prevent build up of static electricity. Static shielding bags typically consist of three layers: (i) an inner layer made of polyethylene plastic which does not create or hold any form of charge, meaning the triboelectric charging does not take place and so no static charge is generated inside, (ii) a middle layer made of aluminium which acts as a shielding layer, and (iii) the outer layer which is made up of a form of polyester with a dissipative coating. This is used to add another layer of protection and to stop build-up of any static electricity outside the bag [25].

1.1.2.2 On-chip ESD protection

ESD circuit protection employs single devices or circuits at I/O pads and power supply pins of ICs. The basic principle is to provide an alternate discharge path for the ESD current



1 Working surface mat
2 Working surface mat grounding cord
3 Earth bonding point plug
4 Wrist strap
5 Earth bonding point bar
Optional:
6 Foot grounders
7 Floor mat
8 Floor mat grounding cord

Figure 1.7: ESD prevention methodologies in workplace. Workstation with ESD controls and a person with necessary ESD protection equipment.

without affecting the circuitry, and to clamp the pad/pin level voltage to a safe level in case of an ESD event. An ideal ESD structure should feature low-impedance and non-destructive discharging paths to shunt ESD pulses of all modes. Reverse connected diodes as shown in Fig. 1.8 is a common method used for ESD protection. Here the diode operates in reverse mode/forward mode depending on the polarity of the ESD pulse at the I/O pad with respect to the VDD and GND pins. Zener diodes are typically used here. Diodes in forward bias can carry large amounts of current, however the low turn on voltage limits its application. Multiple diode strings in forward bias mode are used to improve the low turn-on voltage [1].

In a grounded-gate NMOS (ggNMOS) structure as shown in Fig. 1.9 the drain (D) is connected to an I/O pad and the gate (G) is grounded. When a positive ESD pulse appears at the I/O pin, the drain-body junction becomes reverse biased until breakdown happens. The generated hole current flows into ground via the body terminal and this creates a positive body-source junction voltage. This turns on the parasitic lateral NPN transistor,

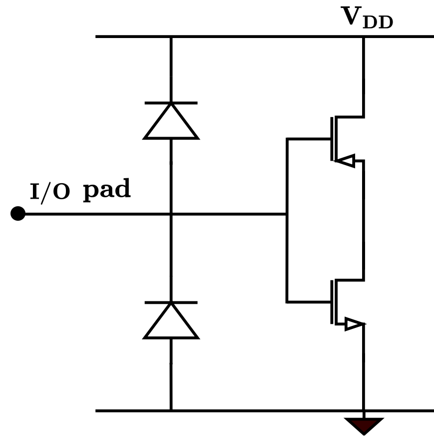


Figure 1.8: Diode ESD protection

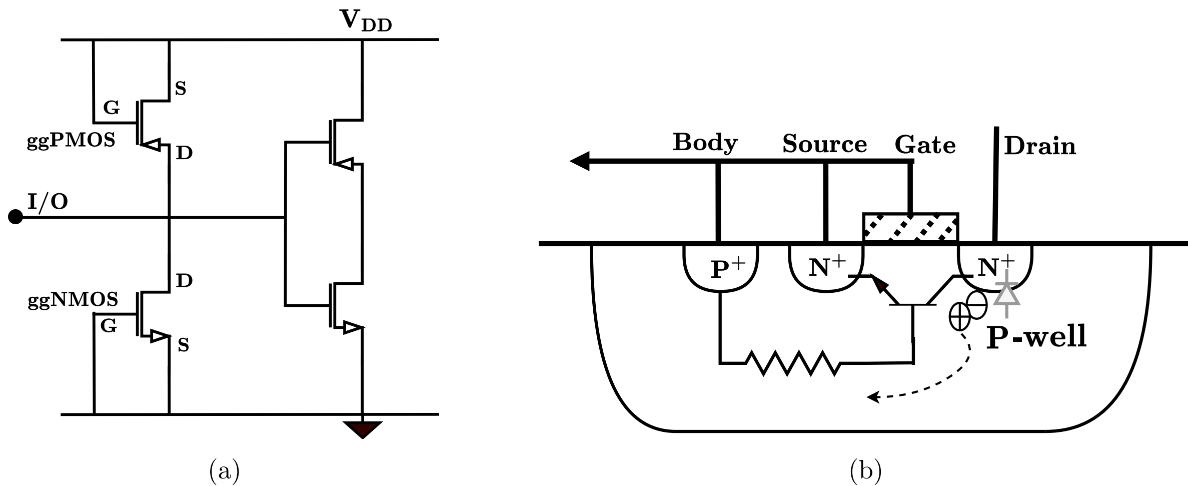


Figure 1.9: A ggNMOS ESD protection structure [1] (a) Schematic (b) Cross-section

forming a low-impedance discharging path to shunt the ESD current and thereby protecting the ICs. In case of a negative ESD transient, charge flows through the parasitic diode. The advantage of ggNMOS protection lies in its active protection mechanism that can be optimized. Disadvantages include non-SPICE-compatible snapback I-V, low area efficiency, and parasitic capacitance added to the I/O pads [1].

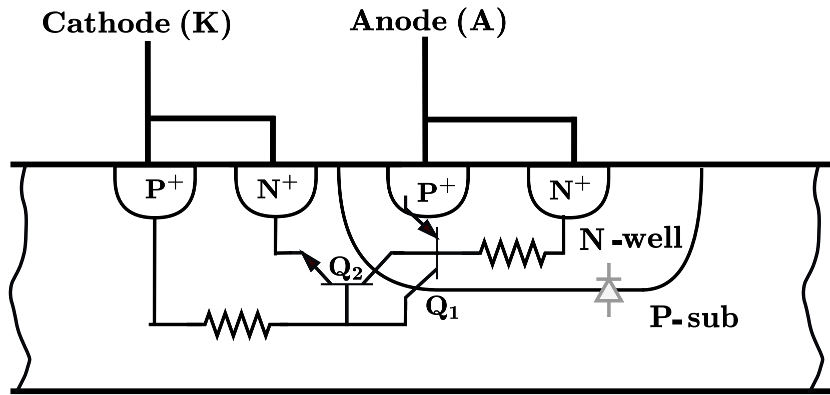
Silicon controlled rectifiers (SCRs), typically used in power applications, can also be used for ESD protection. SCRs occur inherently in CMOS technologies, due to the complementary nature of devices requiring a p-well/n-well for isolation. SCRs in CMOS technology is shown

in Fig. 1.10. A pnp transistor Q1 is formed by the anode(A) as emitter, n-well as base, and p-substrate as collector, and a npn transistor Q2 is formed by the cathode(K) as emitter, p-substrate as base and n-well as collector. When a positive ESD voltage appears at the anode with respect to the cathode, it breaks down the base-collector (BC) junction of the transistor Q1. The generated hole current flows through the p-substrate to the cathode, resulting in a voltage drop across the p-substrate resistance (R_{sub}) that forward biases the base-emitter (BE) junction of transistor Q2. The transistor Q2 turning ON causes a large current to flow from the n-well to the cathode. The voltage drop across R_{n-well} due to this current supplies the base voltage required for Q1, and a voltage at the anode is no longer needed to provide bias for Q1. The voltage at the anode now begins to decrease, resulting in a negative resistance region. The circuit is in latch up condition and can sink large current. For the case of a negative ESD voltage at the anode with respect to the cathode, the p-sub to the n-well diode is forward biased. Since this p-sub/n-well diode is a wide area that is forward biased during the discharge, no latch up occurs and usually no damage is seen [1, 26].

A gate-coupled NMOS couples a fraction of the ESD charge to the gate of the NMOS, as shown in Fig. 1.11(a). This is implemented using a high-pass filter circuit consisting of a capacitor (C2) and a resistor (R1). When an ESD pulse occurs, enough charge is coupled into the resistor such that it weakly turns on the NMOS device. The snap back voltage (V'_{t1}, I'_{t1}) is reduced as shown in Fig. 1.11(b) [26].

Output pins often do not include a direct connection to the CMOS gates. Thus the voltage clamping requirements are comparatively relaxed for output pins as compared to input pins. Typically, output stages include buffers with large sizes and high current driving capability. These can often be modified to provide adequate ESD protection while maintaining buffer functionality[1]. Power clamps as shown in Fig. 1.12 are used for supply pads protection. An ESD transient results in low voltage at the capacitor, causing the big NMOS to turn on through a series of inverters. The NMOS transistor sinks the current.

Layout considerations include providing a ballast resistance in a multi-finger NMOS. In a



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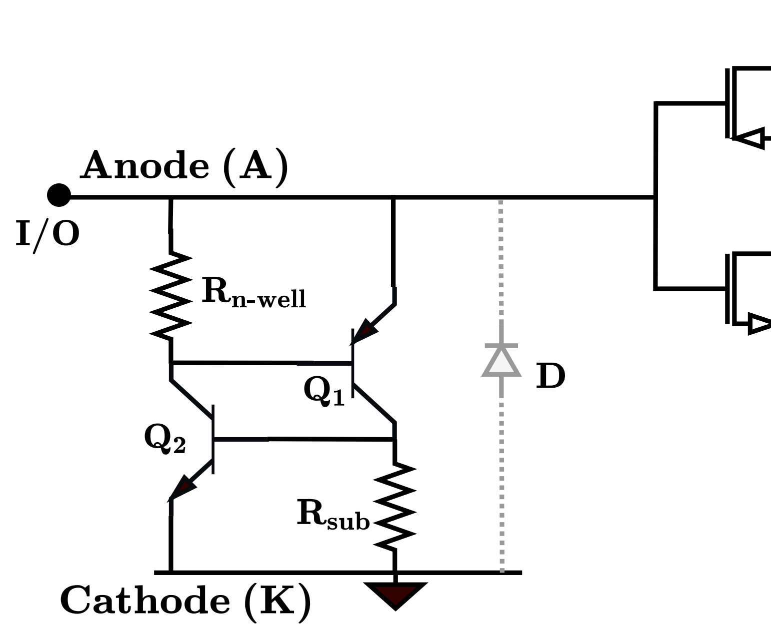
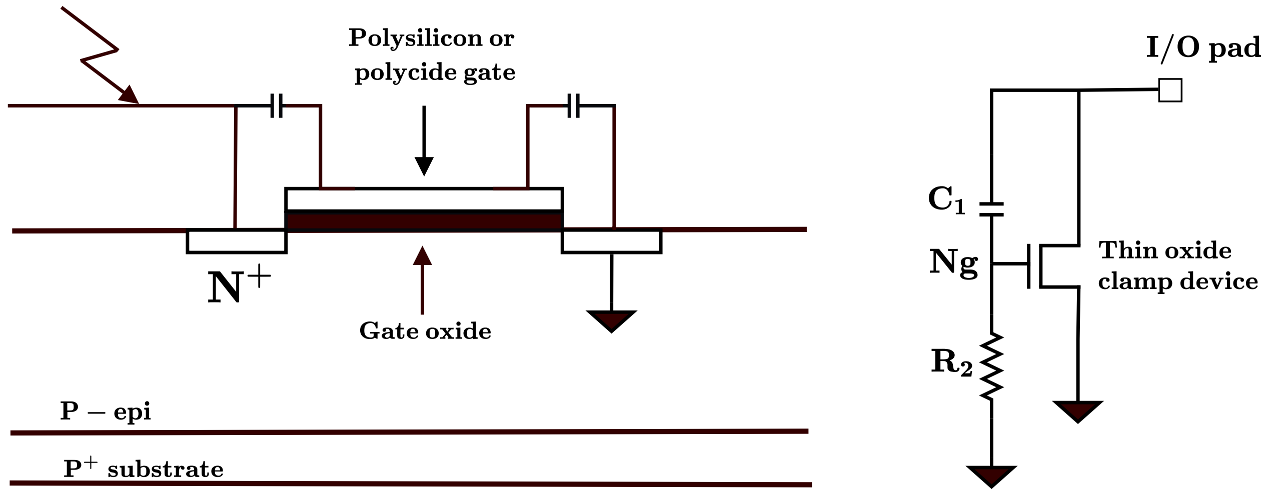


(b)

Figure 1.10: SCR ESD protection [1](a) Cross-section (b) Schematic



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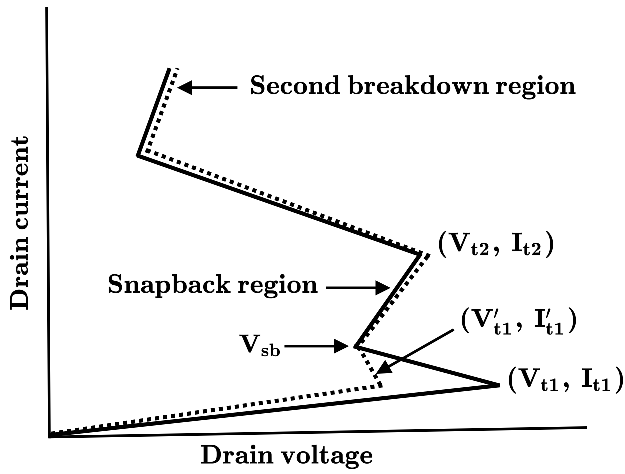


(b)

Figure 1.11: A gate coupled NMOS structure [26] (a) Cross-section (b) I-V characteristic

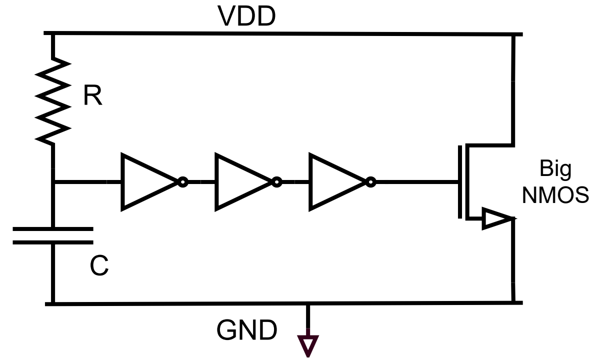


Figure 1.12: NMOS power clamp

regular layout, the distances from the drain region of each finger to the grounded guard ring are different. This results in asymmetry of the substrate resistance and causes the central fingers of NMOS to be more easily triggered on under ESD stresses. By introducing the ballast resistance $R_{ballast}$ as shown in Fig. 1.13, the turn-on resistance of the multi-finger NMOS is increased, and results in the uniform turn on of multi-fingers [27]

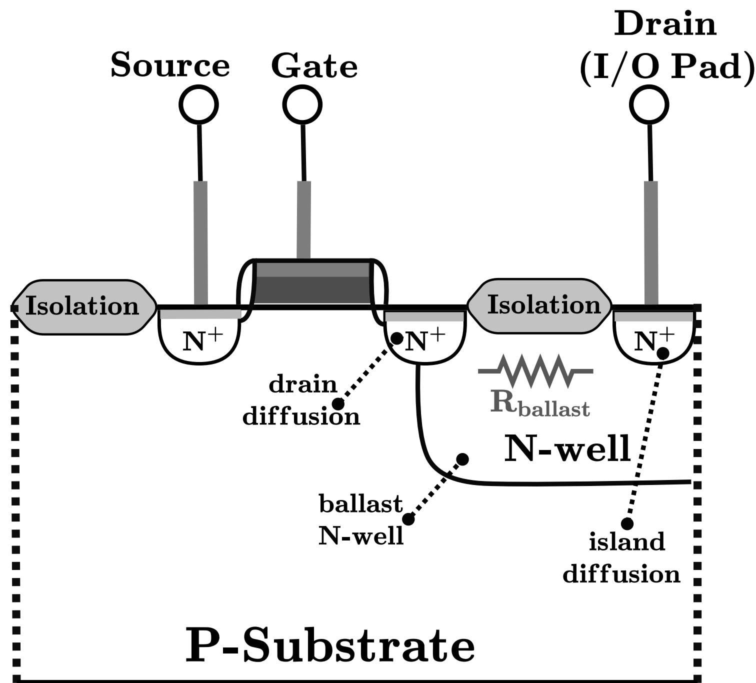


Figure 1.13: Use of ballast N-well to increase the ballast resistance of NMOS [27]

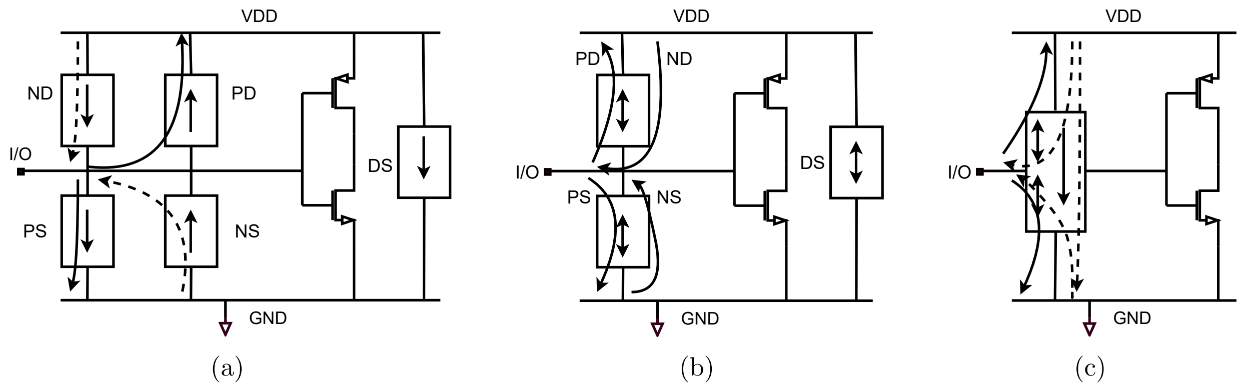


Figure 1.14: Complete ESD protection (adapted from [1]) (a) single direction (b) dual direction (c) all-in-one ESD protection structure

Complete ESD protection can involve multiple devices to shunt all possible ESD paths i.e., I/O-to-VDD in both positive and negative directions (PD and ND), similarly I/O-to-GND in both directions (PS and NS), as well as VDD-to-GND (DS), as shown in Fig. 1.14[1]. Even though it provides full ESD protection, it consumes too much Silicon footprint and impacts circuit performance. A dual-direction ESD protection structure can also be used as indicated in Fig. 1.14(b). All-in-one ESD structures (Fig. 1.14(c)) can also be used. This gives higher area efficiency and low parasitics.

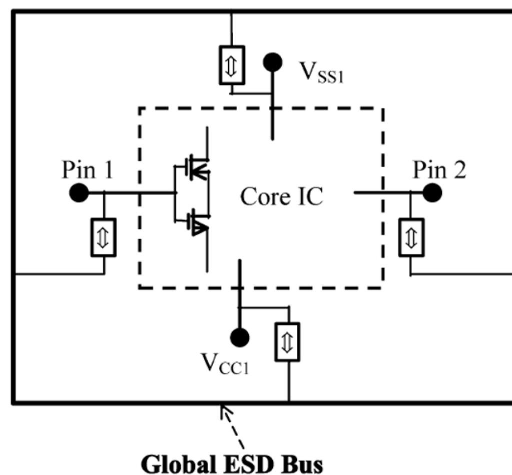
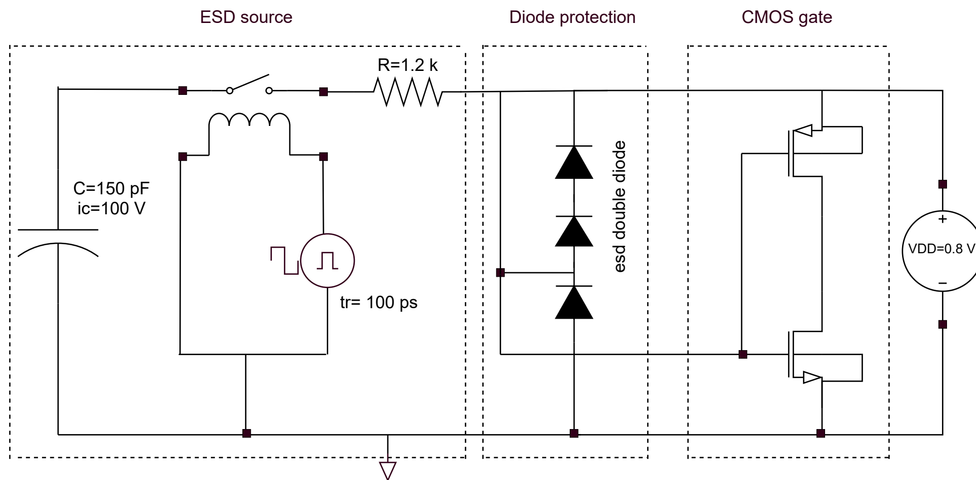


Figure 1.15: ESD global bus[1]

Global ESD protection (Fig. 1.15) includes bus placement on a chip with dual-direction ESD devices being used. This solution uses fewer ESD protection devices, with minimal footprint and parasitic capacitance effects. The Silicon substrate is connected to the ESD bus for better heat dissipation [1].

1.2 ESD in advanced packaging

ESD precautions like proper grounding, shielding, and static-free environment creation are taken during the fabrication, and assembly stages of dielets in advanced packaging schemes. Typical ESD considerations in die-die bonding include placing small ESD clamps at the receiver inputs (primary and secondary diode clamps) providing a common ground, proper power distribution network design, etc. as described in the previous section. Even though dedicated ESD protection circuits are included in most modern ICs, static charge accumulation during transport and handling can exceed the limits of a protection network, especially at finer pitches where area and performance are at a premium, causing ESD damage. For example Fig. 1.16 shows a common diode based protection for a CMOS gate. Here when an HBM event of 100 V happens (associated charge = $150pF \times 100V$), the voltage at the CMOS gate shoots upto 1.8 V. This may cause damage to the gate oxide. In addition, ESD protection devices add parasitic capacitance in the I/Os connecting dielets, thereby limiting the overall latency, max data-rate/link, energy per bit (pJ/b), and max bandwidth per mm [28, 29]. There is a proliferation of dies integrated from multiple sources in any advanced integration platforms. Today's advanced packaging schemes like 3D ICs, Silicon interposer, fanout wafer level packaging etc are not amenable to rework if one or multiple of the dielets are ESD compromised. The entire high value module have to be discarded even in cases where only one die is ESD compromised. Thus known good dies becomes extremely important before the assembly process. One possible ESD qualification could be an on-chip ESD monitor, designed into the chip using standard layout and ground rules within the technology. An on-chip ESD monitor can track the unit process that caused an ESD event.



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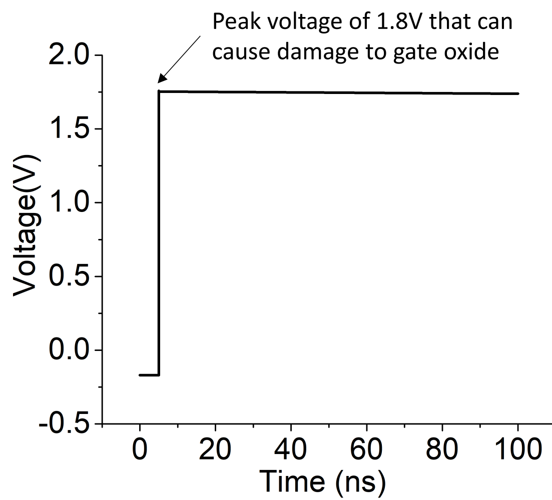


(b)

Figure 1.16: ESD protection to a CMOS gate (a) diode based (b) Voltage waveform at the CMOS gate for a HBM event of 100V

This helps in potentially avoiding the assembly of parts that may have been compromised due to ESD events and thus the yield of the packaging can be increased significantly.

1.3 Organization of this Dissertation

The thesis is organized as follows: In Chapter 2 an advanced heterogeneous integration scheme called Silicon interconnect fabric (Si-IF) is introduced. Susceptibility to ESD in the assembly process of Si-IF is examined with metal oxide semiconductor capacitor (MOSCAPs) as test vehicle. Chapter 3 proposes two schemes for on-chip ESD monitor, designed into the chip using standard layout and ground rules within the technology. These sensors allow to pinpoint the occurrence of a prior ESD event at any point in the supply chain and potentially avoid the assembly of compromised dies in any advanced packaging schemes. Simulation, modelling, working principle and experimental characterization of the two schemes are presented. In Chapter 4 a Bayesian method is developed for estimating the ESD voltage using these sensors and validated with experimental results. Mathematical formulation for sensitivity, confidence in ESD voltage estimation are developed that matches the result of Monte-Carlo simulations. Finally, the conclusion and future outlook of this dissertation is presented in Chapter 5. A novel high-power delivery architecture for wafer-scale systems on Si-IF, enabling 40-60 kW power delivery, is outlined in Appendix A. Experimental prototype results for power delivery are also presented.

Chapter 2

ESD susceptibility in Silicon-Interconnect fabric

2.1 Silicon-Interconnect Fabric

The Silicon-Interconnect Fabric (Si-IF) [30, 29] is a novel heterogeneous integration platform that is package-less, and highly scalable. Si-IF technology aims to replace the classical PCB-based systems and enable integration of the system on a single packaging hierarchy. Here bare dielets are assembled on a pre-wired silicon wafer (Fig. 2.1) using fine-pitch die-wafer interconnects ($\leq 10\mu m$) at a small inter-dielet spacing ($\leq 100\mu m$). The dies are attached to the silicon wafer using solder-less metal-metal thermal compression bonding. The Si-IF substrate is highly scalable and integrates dies on a silicon wafer up to a diameter of 300 mm. A demonstration of the wafer-scale assembly of dies on the Si-IF are presented in Fig. 2.2.

Existing packaging technologies use many disparate materials like Si, Cu, FR-4, solder, molding compound, underfill, etc. which have different thermomechanical properties. The mismatch of these material properties causes Chip-Package-Interaction (CPI) related failures, impacting the device performance. Si-IF uses Si, Cu, and SiO_2 which matches the material constituents on the die, significantly reducing the probability of CPI failures. Here, silicon,

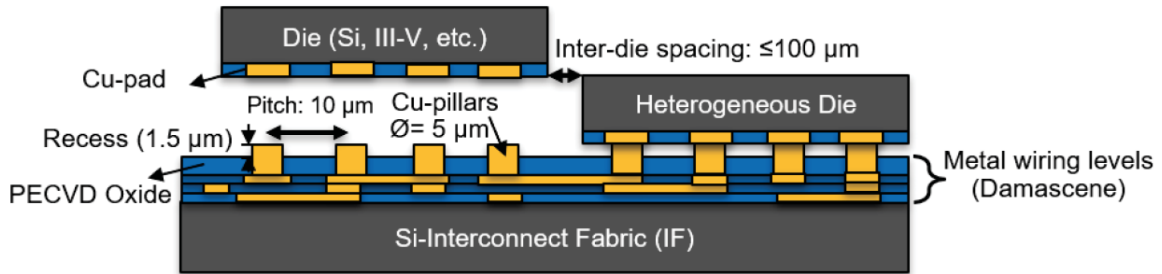


Figure 2.1: Schematic of fine pitch assembly on Si-IF [31]

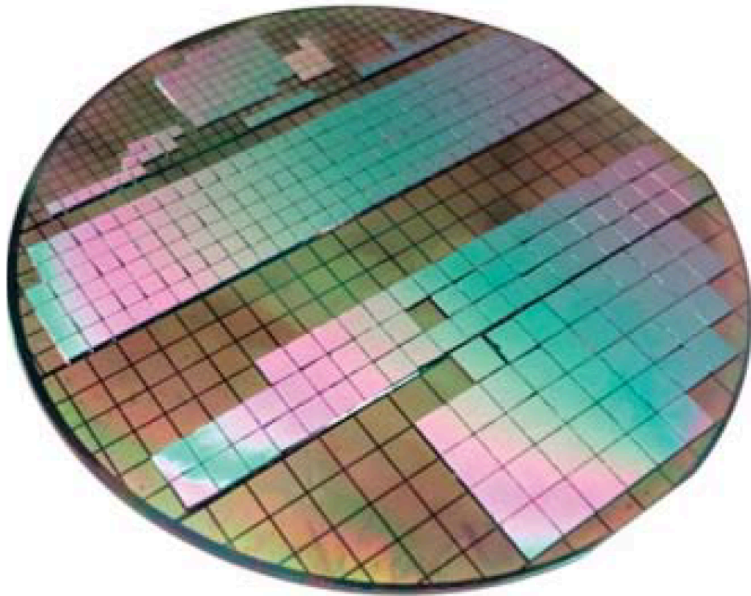


Figure 2.2: About 370 dies (1×1 mm^2 to 5×5 mm^2) at $\leq 100\mu m$ inter-dielet spacing on a 100 mm Si-IF, corresponding to an active area $> 3100\ mm^2$ [31]

which is an excellent heat spreader (149 W/mK), is used as the substrate, resulting in better thermal management as compared to conventional packaging schemes. Also, the use of silicon as the substrate enables mature fabrication techniques developed for CMOS processing, thus enabling fine wiring dimensions of $\leq 2\mu$m. All these features result in significant improvement in data bandwidth of about 120-300$\times$ and energy consumption per bit ($\leq 100\times$) as compared to conventional PCB-based integration schemes [29, 31].

2.2 Impact of employing ESD protection in Si-IF

The parasitic of the Si-IF links have been experimentally characterized [28]. The resistance, capacitance, inductance, and conductance of the links per unit length are, respectively, 4.6 m$\Omega/\mu m$, 0.2 fF/μm, 0.42 pH/μm, and 1 S/μm. This results in low insertion loss and RC-like behaviour for the short links on Si-IF. This enables the usage of simple cascaded inverters as transceivers for data transfer between dielets. The Si-IF links were simulated (Fig. 2.3) using simple cascaded inverters as transceivers for two scenarios: (a) transceivers without electrostatic discharge (ESD) protection, and (b) with ESD protection [29]. The overall latency from the input of the driver to the output of the receiver through Si-IF links is $\sim$ 20% higher for the case where ESD protection diodes were included. ESD protection diodes can add more than 0.1 pF of parasitic capacitance per link. Since the Si-IF link capacitance (0.1 pF per link) is comparable to the capacitance of the ESD protection diodes, the link driver circuit size should be increased by almost 2X. Thus, adding ESD protection caps degrades the overall latency (1.4X), max data-rate/link (3X), and max bandwidth per mm (3X) [29]. If the Si-IF assembly process is robust to ESD failures, ESD protection could be minimized. The assembly process reliability of Si-IF is evaluated in the next section.

2.3 Si-IF assembly process and experimental setup

During the assembly process, dielets are picked up from a waffle tray using a pick tool with a rubber tip. The dielets are subsequently transferred to a ceramic place tool. The dielets are then precision-aligned ($\pm 1\mu m$ accuracy) and attached by TCB to the Si-IF (Fig. 2.4) using optimized process parameters (bonding pressure, temperature, and time). During the aforementioned process, triboelectric charging of dielets and various machine contacts can lead to an ESD event [32]. The bonding tool is equipped with an ionizer that removes any charge accumulation on the dielet and substrate surface during the place process.

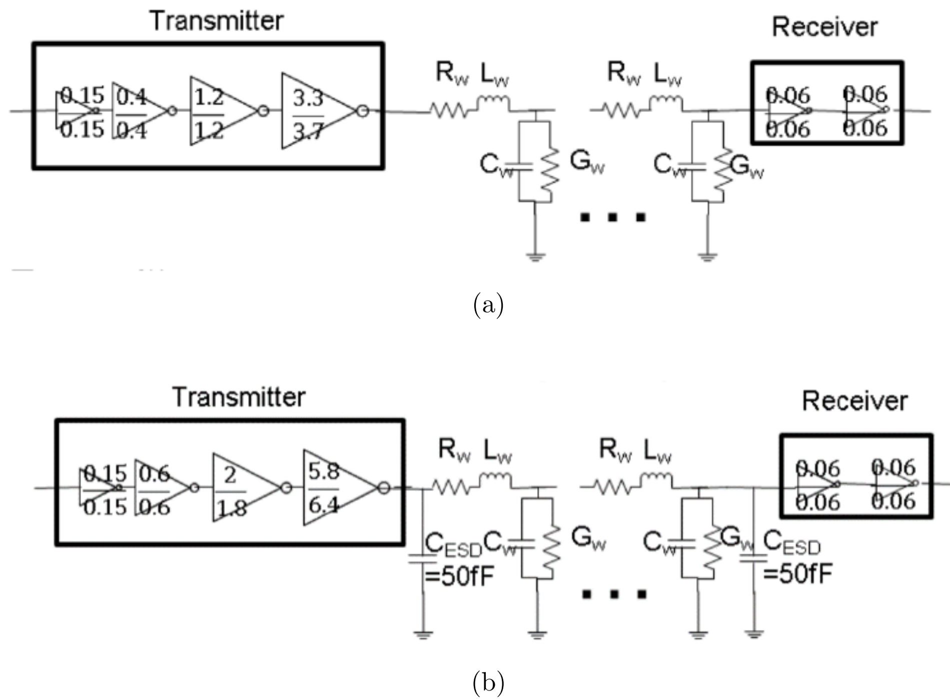


Figure 2.3: Schematic of transceiver circuit (a) without ESD protection and (b) with ESD protection [29]

Both dielets and the Si-IF are designed with a single metal layer on a thin film dielectric to form simple metal oxide semiconductor capacitors (MOSCAPs) which are used to detect dielectric breakdowns. During the assembly process, as dielets are attached to the Si-IF, the

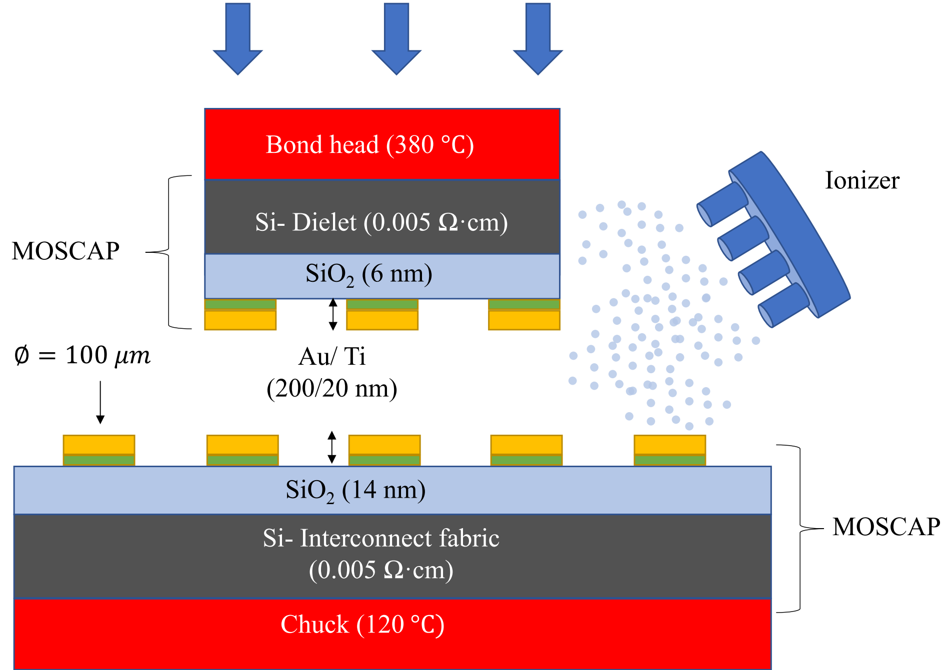


Figure 2.4: Cross-sectional image of dielet and Si-IF in the assembly process.

thin oxide layer of the MOSCAP can break due to an ESD event or the applied bonding pressure. A breakdown is examined by characterizing the current-voltage (I-V) curve of the dielet and the Si-IF before and after the assembly process. Various oxide thicknesses are fabricated to determine the minimum required thickness to sustain different breakdown mechanisms. The effectiveness of the ionizer as an ESD protection mechanism is also investigated. MOSCAP dielets and Si-IF wafers are made on heavily doped silicon (N-doped, $\rho = 0.005\ \Omega \cdot cm$) for good electrical conductivity. Silicon dioxide is used as the thin dielectric layer. A silicon dioxide layer (dry oxidation at 1100) with varying thicknesses of 6, 14, 22, 36, and 55 nm was used on the dielet. A similar silicon dioxide layer with varying thicknesses of 14, 22, and 55 nm was used on the Si-IF. Titanium/gold (20/200 nm) pads were evaporated to complete the MOSCAP structure (Fig. 2.5).

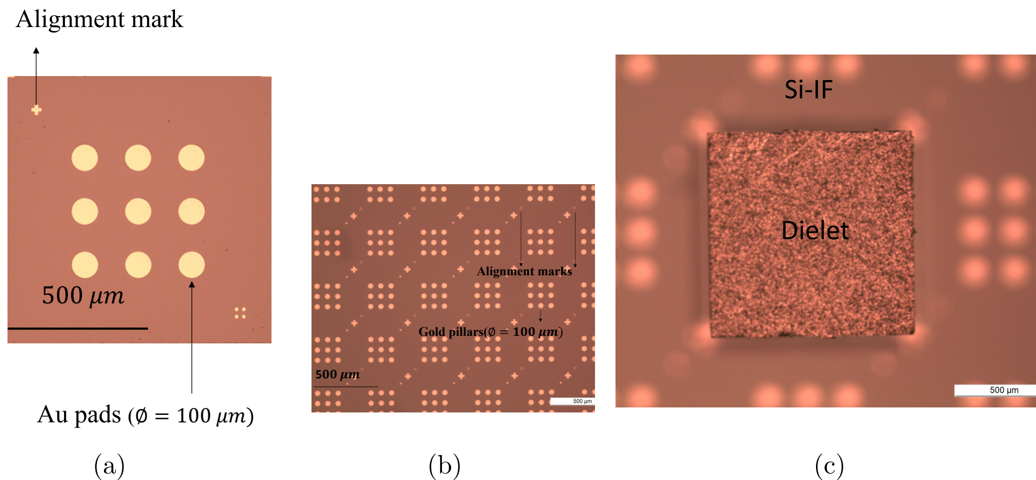


Figure 2.5: (a) Top view of dielet, (b) Si-IF, and (c) dielet bonded to Si-IF.

2.4 Experimental results and discussion

In the Si-IF TCB process, a bonding temperature of 250 and a bonding time of 3 seconds were used. To evaluate the effects of charge build up during the assembly process, the bonding pressure was varied from 50 to 140 MPa with the ionizer on or off. The integrity results of dielets with 6 nm oxide are shown in Fig. 2.6. The percentage of pads broken in Fig. 5 refers to the number of broken MOSCAP structures out of the total number of MOSCAP structures on a given die. To construct each of these plots, about 50 devices were tested, and their post breakdown conductivities were noted and binned. With the ionizer turned on (red squares in Fig. 2.6), the effect of ESD is neutralized as no oxide breakdown is observed. With the ionizer turned off (black squares in Fig. 2.6), oxide breakdown is observed only in dielets with a 6 nm oxide. Dielets with oxide thickness of 14, 22, and 55 nm did not undergo any electrical breakdown. In addition, since the thinnest oxide on the Si-IF was 14 nm, the Si-IF wafers exhibited no breakdown. The breakdown field of a thermally grown oxide is typically 1 V/nm [33], we, therefore, estimate that the induced voltage of the assembly process is 6-14 V. This induced voltage is neutralized when the ionizer is turned on.

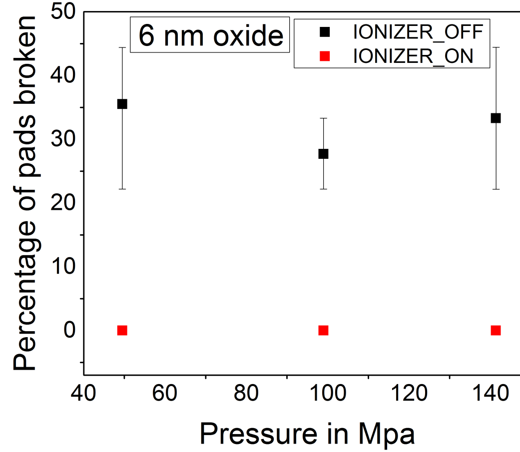


Figure 2.6: ESD effect on dielet breakdown with ionizer off and on.

The effect of bonding pressure on the breakdown of dielets [34, 35] was also evaluated. To eliminate potential ESD events, i.e., to isolate the pressure related breakdown of the dielets, the ionizer was turned on. In this experiment, the TCB pressure was varied from 200 to 700 MPa while other TCB-related parameters were kept constant (bonding temperature of 250 °C and bonding time of 3 seconds). Oxide breakdown of dielets with a 6 nm oxide is observed for bonding pressure higher than 200 MPa, as shown in Fig. 2.7. The I-V characteristic of these broken dielets is shown in Fig. 2.8. A typical breakdown voltage of a virgin (i.e., not assembled) 6 nm thick oxide dielet is approximately 5-7 V, represented by the black squares curve in Fig. 2.8. The breakdown current in this case is limited to 1 mA, set by the compliance limit. The I-V characteristics of a dielet that was broken down by an ESD-related event (undergo Si-IF assembly process with ionizer turned off) are the blue triangles in Fig. 2.8, exhibiting an ohmic behaviour. The red curve in Fig. 2.8 represents the I-V characteristic of an electrically broken down dielet due to the high bonding pressure (750 MPa), similarly to the ESD-related breakdown, an ohmic behaviour is also observed in this case. Note, both broken dielet I-V curves (blue triangles and red circles) are measured

on electrically broken-down samples.

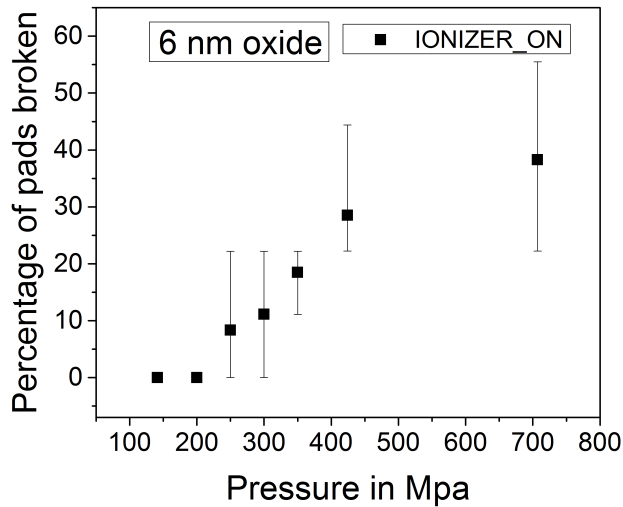


Figure 2.7: Effect of pressure on dielet breakdown.

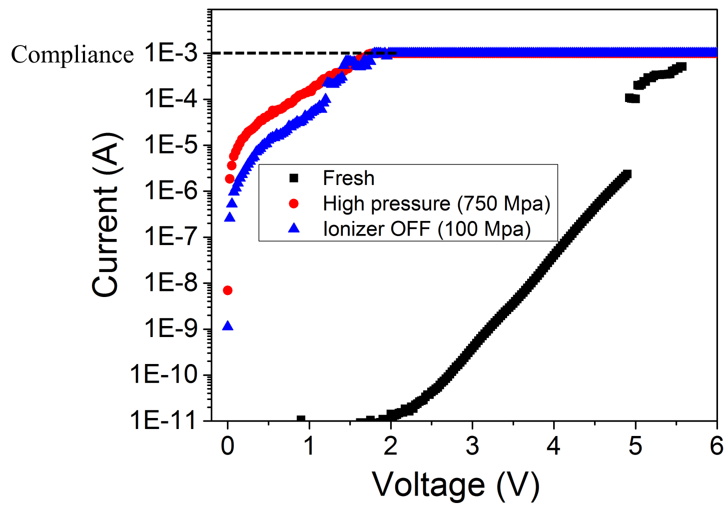


Figure 2.8: I-V characteristics of broken down dielets by different mechanisms.

A hard breakdown is characterized by a large change in current between a virgin sample measurement and post-breakdown I-V characteristic. During a hard breakdown, the power

dissipated exceeds the threshold of irreversible thermal damage, resulting in an ohmic I-V curve of the broken devices. In case of a soft breakdown, however, a smaller change in current is observed between a virgin and a broken device [36]. Here, a percolation path is likely formed in the oxide, exhibiting a power-law conductance for post-broken devices. Also, the thermal damage in soft-breakdown is reversible [37, 38, 39]. Since a large change in current between virgin and broken devices (for both ESD and high pressure related breakdowns), and an ohmic post-breakdown I-V characteristic is observed, the samples are concluded to undergo a hard breakdown.

2.5 Conclusions

We have demonstrated that the Si-IF assembly process is reasonably robust to ESD failures. The developed voltage in the assembly process of 6-14 V can be effectively removed by turning the ionizer on. This minimizes the ESD protection requirement on die-die internal interconnects during the bonding process. In any advanced packaging platforms, as dielets are sourced from multiple vendors and require many supply chain handoffs, an on-chip ESD sensor (similar to tilt and rough handling indicators used in shipping and handling of goods) would be useful to ensure that dielets are ESD safe prior to the assembly process.

Chapter 3

On-chip ESD monitor

3.1 Introduction

Currently, ESD events significantly contribute to device failure at all stages of IC production, test, assembly, and field usage [1, 3]. ESD protection circuits are included in most modern ICs. Nonetheless, static charge accumulation during transport and handling can exceed the limits of a protection network, causing ESD damage [10]. In advanced packaging schemes, bare dies from a variety of sources need to be integrated using advanced methods such as the Silicon Interconnect Fabric technology or fan-out wafer level packaging such as FlexTrate^{TM} [40]. An accurate ESD sensor can allow us to pinpoint at which stage in the supply chain an ESD event has occurred and potentially avoid the assembly of parts that may have been compromised. The ESD sensor is analogous to the tilt and rough handling indicators used in packaging and shipping which tells the customer whether the product has been mishandled during shipping.

Here, an on-chip ESD detection circuit, which can track the electrostatic history of the IC from the manufacturing process until the end-of-life, is demonstrated. This on-chip ESD monitor tracks the unit process (assuming that testing is possible and performed after each unit process) that suffered an ESD event. An ESD diagnostic structure must have the

following features: (i) be stand-alone or easily integrable with different dies, (ii) be non-volatile, i.e. damage or effects of charge accumulation should be permanent, and (iii) should be quantitative and correlated to the pad size. Two schemes are presented here: (a) a variable dielectric width capacitor, and (b) a vertical MOS capacitor (MOSCAP) array.

3.2 Variable dielectric width capacitor

The basic working principle of the variable dielectric width capacitor is presented in 3.2.1. Evaluation of the electric field within the proposed structure and ESD test simulations are provided in 3.2.2. Implementation of the variable dielectric width capacitor in GlobalFoundries (GF) 22 nm fully depleted silicon-on-insulator (22FDX) technology, along with the experimental results, is presented in 3.2.3.

3.2.1 Working principle

The basic structure of the variable dielectric width capacitor consists of a dielectric material separating two metal plates terminated with sharp corners, as shown in Fig. 3.1. Sharp corners are incorporated in this structure to increase the local electric field intensity which will ensure that the thin dielectric between the metal plates breaks down easily. The ESD monitor module consists of rows and columns populated with metal plate pairs of varying area and separation. Each plate pair has a pad area of A_i and a separation of d_i. The structure is subjected to ESD events during the packaging, assembly, or any other unit process (Fig. 3.2). If charge has accumulated on the metal pads, as one of the pad is grounded, it will cause a significant voltage difference between them. Consequently, a large current will flow from the high potential plate to the grounded plate through the thin dielectric causing a dielectric breakdown. The voltage that is developed across a plate pair i, denoted V_i, is directly proportional to the area of the plate A_i. The magnitude of the electric field E_i that is developed between the metal pads when one of the plates is grounded depends on the plate

separation d_i. The breakdown strength of the dielectric is denoted by $E_{BD,I}$. The criterion for breakdown is $E_i(V_i, d_i) > E_{BD,I}$, i.e., the electric field between the metal pads becomes greater than the breakdown strength of the thin dielectric. The I-V curve of each plate pair (all rows and columns) could be measured at any time to observe whether an ESD event has occurred. The induced ESD voltage of the unit process is estimated by identifying the broken plate pairs. A more accurate evaluation of the induced voltage can be performed by increasing the granularity of A_i and d_i within the array.

3.2.2 Evaluation of electric field and ESD simulations

The potential $\varphi(\rho, \phi)$ and electric field $E(\rho, \phi)$ in cylindrical coordinates (ρ, ϕ, z) inside a two-dimensional wedge with angle β $(0 \leq \phi \leq \beta)$ bounded by a grounded conductor (Fig. 3.3) [41], when the radial distance (ρ) is small is given by

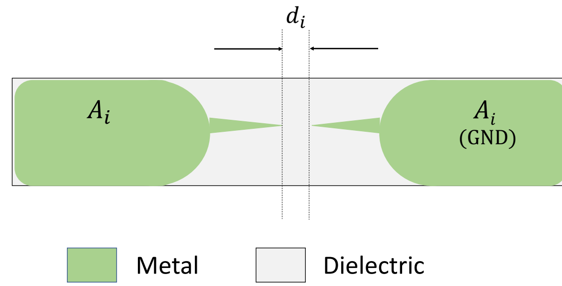
$$\varphi(\rho, \phi) \approx \rho^{\frac{\pi}{\beta}} sin(\frac{\pi\phi}{\beta}) \tag{3.1}$$

The associated electric field is

$$E = -\nabla\varphi = -\frac{\pi}{\beta}\rho^{\frac{\pi}{\beta}-1}(\hat{\rho}sin(\frac{\pi\phi}{\beta}) + \hat{\phi}cos(\frac{\pi\phi}{\beta})) \tag{3.2}$$

Thus, the magnitude of the electric field $|E| \to 0$ as $\rho \to 0$ for $\beta < \pi$, and $|E| \to \infty$ as $\rho \to 0$ for $\beta > \pi$. The intensity of high local electric fields near sharp corners is exploited in the implementation of the variable dielectric width capacitor. When one of the metal plates in a plate pair is grounded, the charge density on the non-grounded plate near the sharp edge becomes high, resulting in a very high electric field, which can break down the dielectric between the plates.

Electric field simulation of the structure in ANSYS Maxwell as a function of the width of the dielectric between the pads (i.e., separation between sharp corners), is shown in Fig. 3.4. Breakdown strength of some dielectric materials that could be employed in the ESD monitor are also indicated in Fig. 3.4. For example, the maximum electric field between



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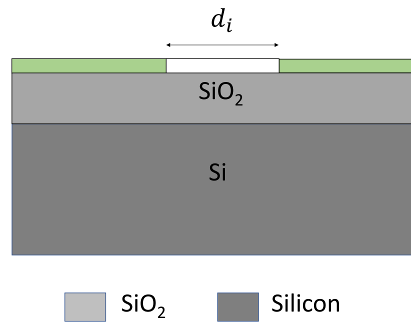

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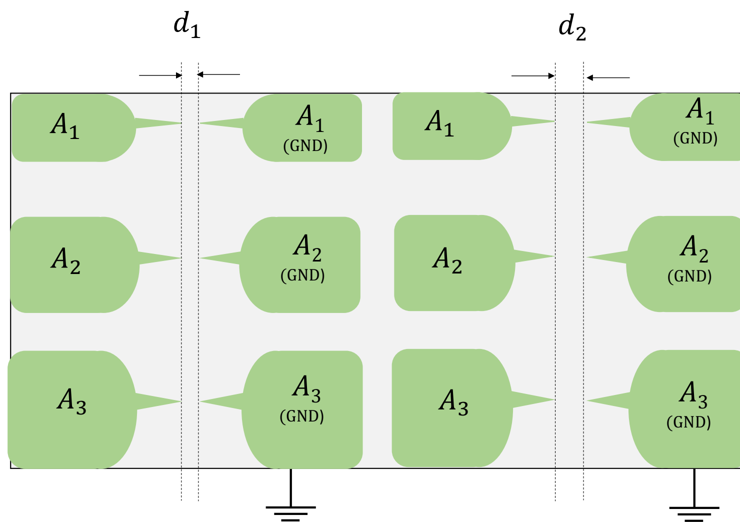

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Figure 3.1: Pairs of metal plates terminated with sharp corners separated by a thin dielectric. (a) Top view, (b) cross-sectional view, and (c) metal plate array.

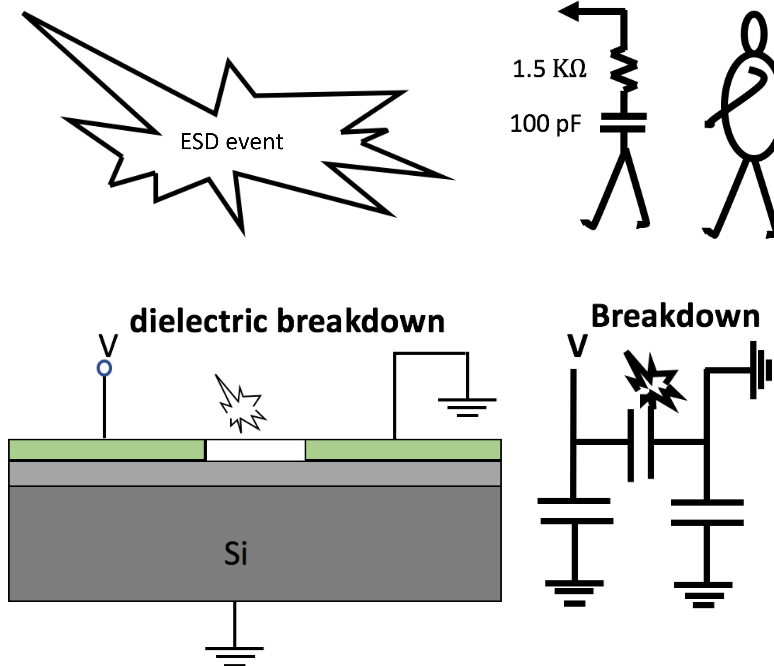


Figure 3.2: Working principle of the ESD sensor unit. A Human body touching the ESD sensor. One of the metal plates of the ESD sensor is grounded. If the voltage V developed is greater than the break down strength of the thin dielectric between the metal plates, it undergoes breakdown.

metal plates that are separated by 40 nm of dielectric material, is $1.2 \times 10^8 V/m$ when biased at 5V. If, therefore, the dielectric chosen for the 40 nm separation is silica, exhibiting a typical breakdown strength of $\sim 1 \times 10^7 V/m$, a voltage of 5 V across the plate pair will suffice to break the silica dielectric.

Classically, damage originating in ESD was considered to be a production problem, and was addressed by ESD safe procedures, like earth mats, operator wrist straps, etc. However, with increased use of plastic and synthetic materials in the modern environment and widespread use of metal oxide technologies, the effect of ESD on electronic systems has become more significant and is no more considered only as a production problem [42]. ESD-induced field returns of ICs during assembly, test, and field usage has led to the development

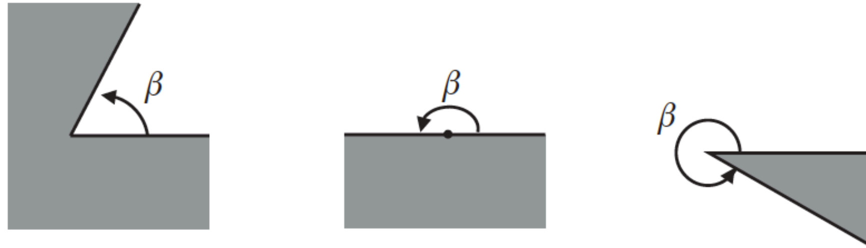
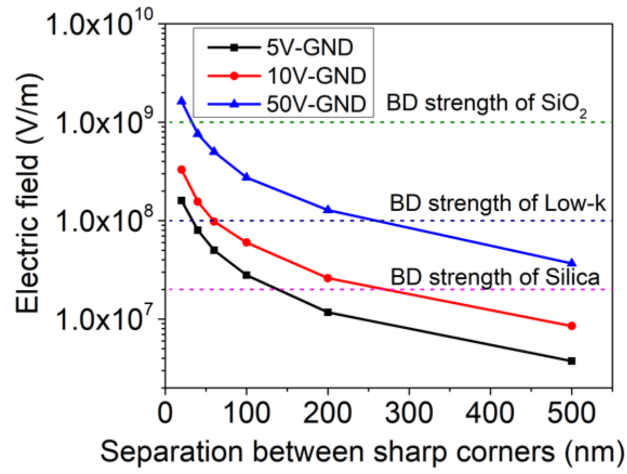


Figure 3.3: Side view of a two-dimensional wedge ($0 \leq \phi \leq \beta$) cut out of perfectly conducting (shaded) matter. The conductor is held at zero potential and otherwise fills all of the space [41].

of ESD testing standards to test for robustness and ensure ESD protection of any electronic equipment. For ESD qualification of ICs, test standards have been developed by various organizations, including JEDEC, ESDA, and MIL-STD [43]. There are three main ESD test models based on ESD events that the test is emulating: human body model (HBM), charge device model (CDM), and machine model (MM).

CDM emulates ESD charging followed by a rapid discharge, similar to what is seen in automated handling, manufacturing, and assembly of IC devices. A CDM calibration setup, as shown in Fig. 3.5, consists of a charge plate, to which a high voltage supply is attached. A thin insulation layer isolates the device under test (DUT) from the charge plate. The DUT is placed on the insulation layer with its pins facing up. This results in the DUT being capacitively coupled through the FR4 dielectric and charged by the charge plate. During the test, a grounded plate approaches the DUT and discharges the current through a 1 Ω resistor. The discharge current through the resistor is monitored by an oscilloscope. JEDEC specifies a standard size metal coin for calibration of the test setup. The test environment was modelled in ANSYS Maxwell using a 25 mm (Fig. 3.6(a)) standard size coin as the DUT. All capacitances pertaining to the test setup were extracted as shown in Table 3.1. A CDM circuit simulation (Fig. 3.6(b)) was performed with the extracted capacitance values, and the discharge current and voltage waveforms (Fig. 3.6(c)) were verified with the literature reported values [44, 45].



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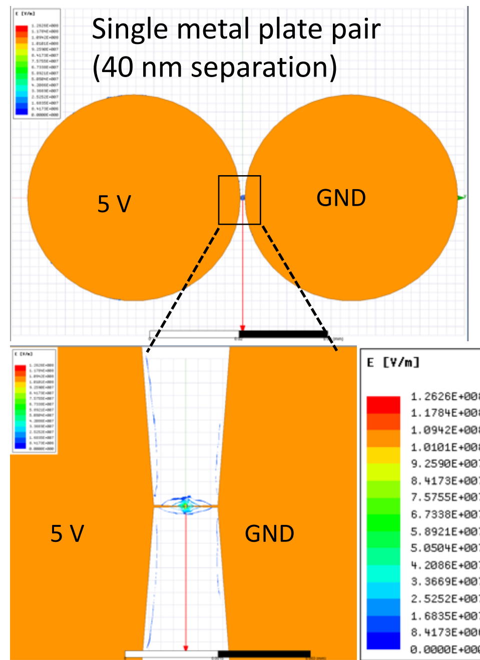


(b)

Figure 3.4: Simulated electric field profile. (a) Simulation of electric field as a function of distance between the sharp corners (BD stands for break down). (b) Electric field lines for a 5 V- GND system at 40 nm separation.

Table 3.1: Extracted capacitance values for 25 mm metal coin calibration

Parameter	Values
Diameter (mm)	25.4
Metal to field cap (C2)	55.7 pF
Metal to ground cap(C1)	1.8 pF
Field to ground cap(C3)	23.8 pF

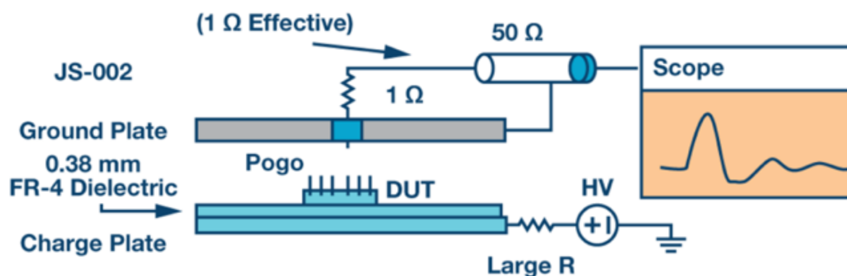
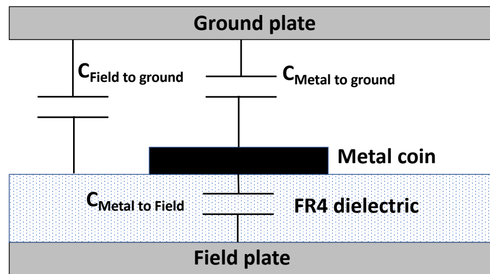


Figure 3.5: CDM Test setup [46].

Upon verifying the test setup, a CDM simulation with the ESD detector as the DUT was set up in ANSYS Maxwell and various capacitance values were extracted. CDM circuit schematic and simulation results with the ESD detector as the load are shown in Fig. 3.7. A test voltage of 5 V is applied to the charge plate. The ESD sensor is charged to 4.3 V. At $t = 1ns$, metal plate Met2 is grounded. Met2 undergoes a small oscillation and settles to 0 V. Prior to grounding Met2 ($0 \leq t \leq 1ns$), the voltage difference between the two plates $V_{Met1} - V_{Met2}$ was zero. At $t = 1ns$, the difference in voltage shoots up to 7 V and then settles to 4 V. This shows the voltage development across the sharp corners, which results in a high local electric field and a possible dielectric breakdown between the metal plates when one of the metal plates is grounded.

The HBM emulates an electrostatically charged human touching the pins of an IC, typi-



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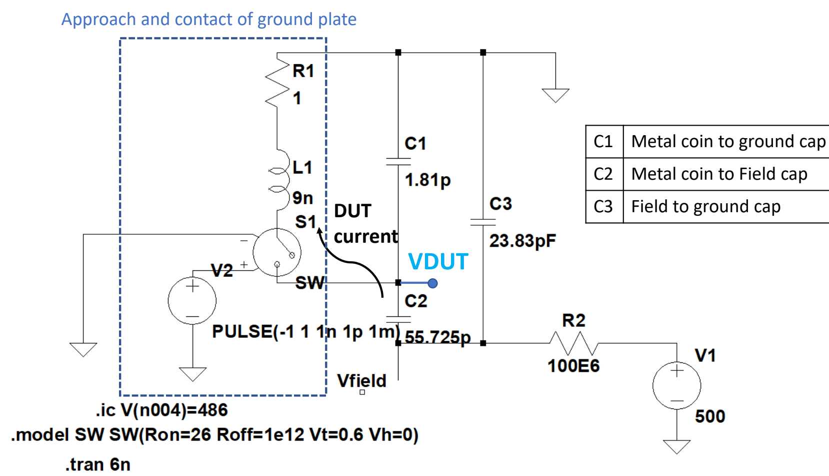

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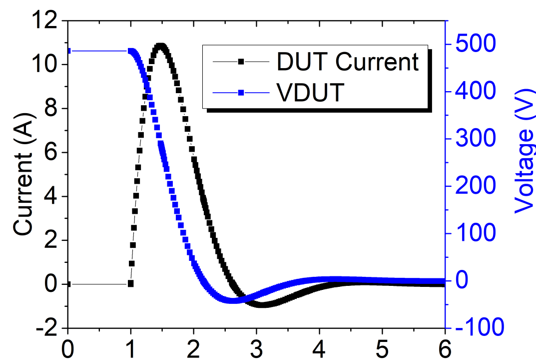

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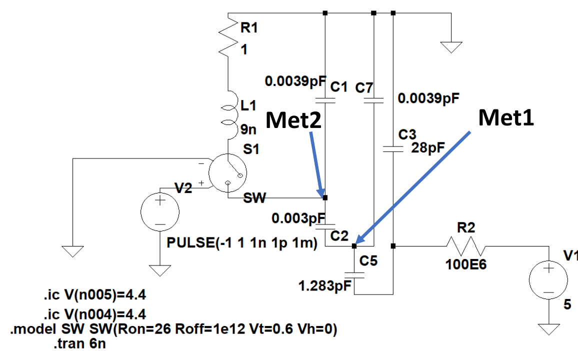
Figure 3.6: (a) Simulated Calibration model of the test setup with a JEDEC specified metal coil (b) Circuit simulation with extracted capacitance values(c) Simulated voltage and current waveform for the calibration test setup at 500 V CDM



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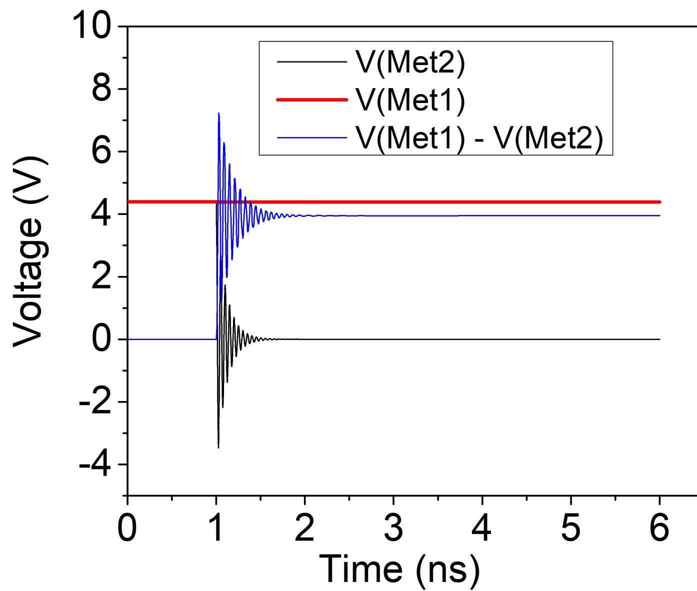


(b)

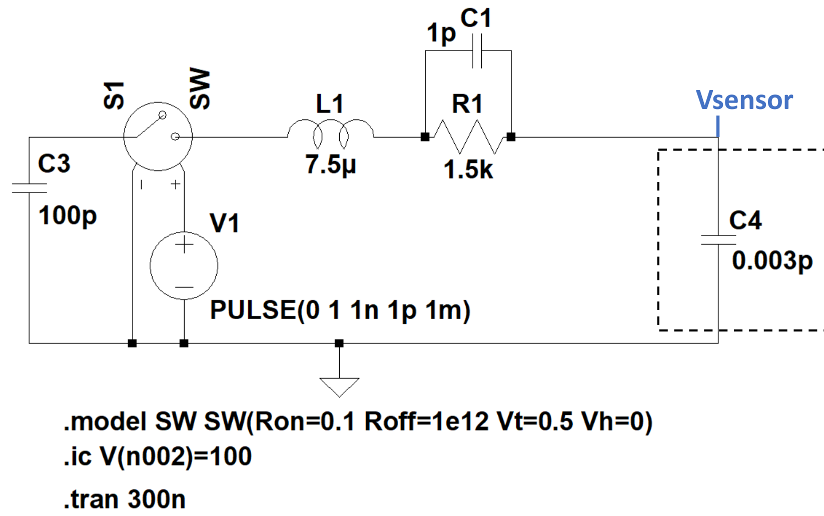
Figure 3.7: CDM simulation. (a) LT-Spice implementation of CDM with ESD detector as DUT, and (b) corresponding voltage waveforms.

cally generating a discharge current with a rise time of a few nanoseconds and a decay time of about 150 ns [47, 48]. The small signal impedance of humans standing over a ground plane and holding a metal object varies non-linearly with frequency, from 3 $k\Omega$ at low frequency (< 1 MHz), to less than 50 Ω at high frequency (> 1 GHz). This impedance can be modelled with discrete elements and transmission lines with good correlation to human ESD events [49]. In case of an HBM ESD event, the static charge is initially stored in the body of the human, and transferred to the IC when a body part of the human comes in contact with the system. The equivalent circuit diagram of an HBM ESD event along with the ESD detector as the DUT for an input test voltage of 100 V (associated charge of 150 pF $\times$ 100 V = 15 nC) is shown in Fig. 3.8. The ESD sensor instantaneously ($\sim$ 150ns) acquire the applied voltage of 100 V since the capacitance of the ESD sensor is significantly smaller than the typical HBM capacitance. This ensures that a breakdown of the sensor occurs instantaneously.

The MM ESD standard represents the electrical discharge from a charged conductive source into a component or an object. Unlike the HBM, the MM equivalent capacitor discharges through a small parasitic series resistance, resulting in an oscillatory input pulse. This is comparable to the pulse generated by a charged machine part touching an IC pin. MM simulation of the ESD sensor for an input voltage of 100 V is shown in Fig. 3.9. Similar to the HBM simulation, both metal plates acquire the applied voltage instantaneously, again ensuring that a breakdown occurs when one of the metal plates is grounded. All of the ESD simulations demonstrate the functionality of the ESD detector unit.

3.2.3 Fabrication in GF 22 nm FDSOI and experimental results

The variable dielectric width capacitor was designed, simulated, and fabricated using GF 22 nm FDSOI technology. Instead of sharp corners, rectangular shaped metal lines (limited by the process technology) were used. The lowest metal line (M1) is used to define the metal structure of the variable dielectric width capacitor. This was done as the dielectric



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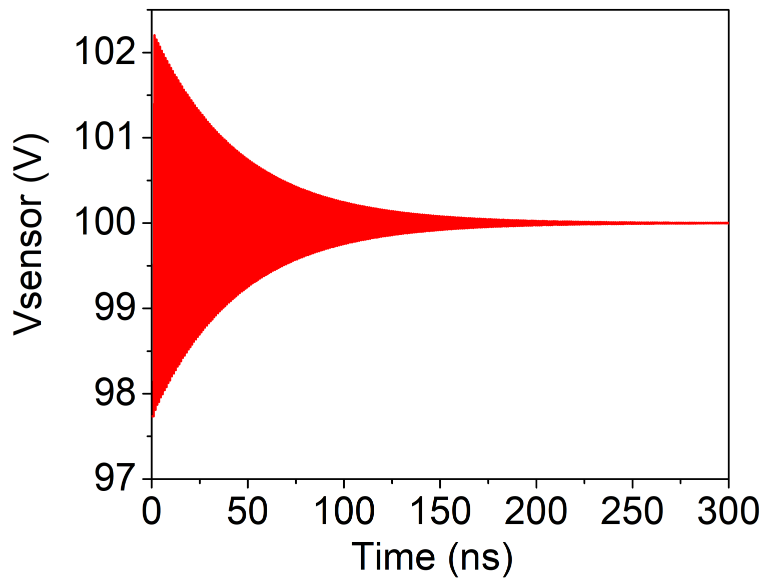

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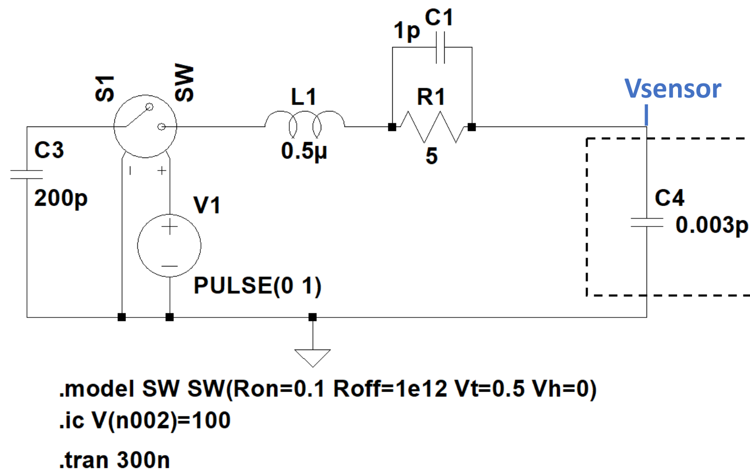
Figure 3.8: HBM simulation. (a) LT-Spice implementation of HBM with ESD detector as DUT, and (b) corresponding voltage waveforms.



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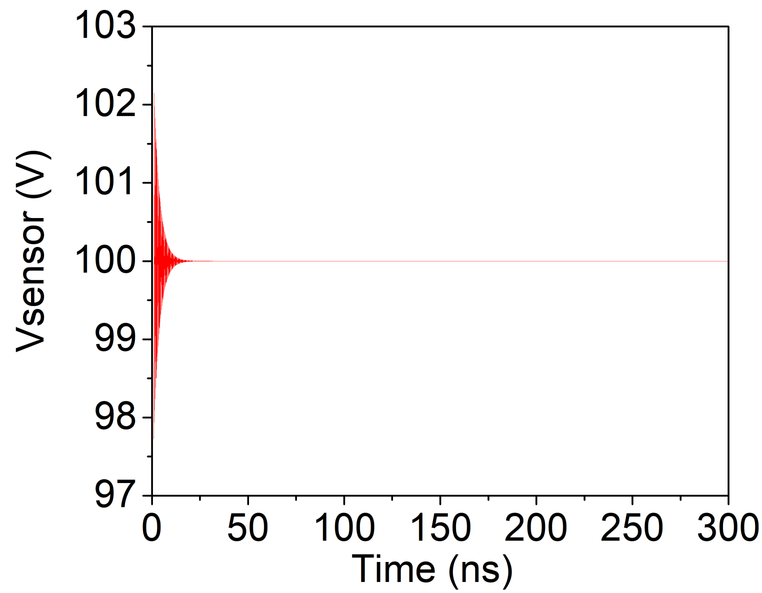


(b)

Figure 3.9: MM simulation. (a) LT-Spice implementation of MM with ESD detector as DUT, and (b) corresponding voltage waveforms.

is thinnest, and intra-level metal spacing achievable is minimum at the M1 level. Electrical connection from M1 goes through vias and other higher metallic layers (M1, M2, etc.) and is terminated at the top metal pad of the FDSOI technology, as shown in Fig. 3.10. The electric field simulation for the metal M1 lines separated by an 80 nm dielectric is shown in Fig. 3.11. The electric field value is 5×10^8V/m for an applied voltage of 20 V, which can cause a dielectric breakdown if the chosen thin dielectric is a low-k material [50, 51, 52]. Note, the electric field between the M1 metal lines is not as high as for the simulated case of sharp corners since the metal lines are rectangular shaped.

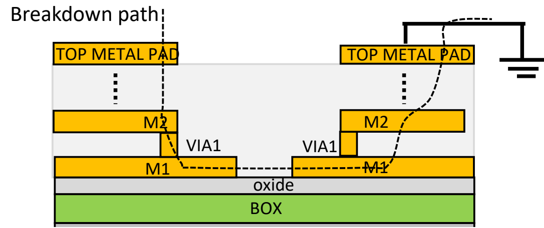


Figure 3.10: Cross-sectional view of variable dielectric width capacitor in GF 22 nm FDSOI technology.

Two metal separations, 40 nm and 80 nm, are used in the GF 22 nm FDSOI implementation. For a silicon dioxide inter-layer dielectric exhibiting a breakdown strength of $\sim$1 V/nm, a breakdown voltage of, respectively, 40 V and 80 V is expected. The variable dielectric width capacitor is experimentally characterized in two steps. First,both of the metal pads were grounded. This ensures that both metal pads are uncharged. In the second step of the characterization the applied voltage is varied on one of the pads, while the other metal pad remains grounded. The extracted I-V curve enables us to identify the breakdown voltage of the structure. The breakdown characteristics of the two implementations are shown in Fig. 3.12. The 40 nm dielectric width capacitor breaks down in the range of 38 V to 41 V, while the 80 nm dielectric width capacitor breaks down in the range of 77 V to 81 V. The extracted I-V characteristics of the two structures are shown in Fig. 3.13. Note,

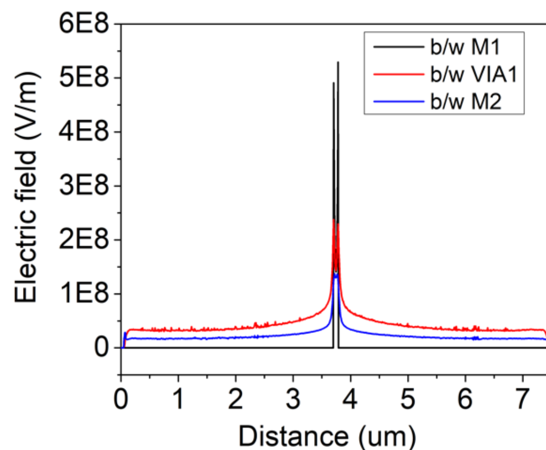


Figure 3.11: Simulation of electric field lines between the two M1 metal plates for the variable dielectric width capacitor from Fig. 3.10 for a 20 V applied to one ESD pad while the other pad is at zero volts.

after breakdown the current drops rapidly due to a possible accelerated electro-migration or a thermally induced void formation in the metal lines caused by the high-power dissipation immediately after the breakdown event. To ensure that the ESD event is stored, the dielectric breakdown needs to be decoupled from generation of thermally induced voids and electro-migration within the metal interconnect, which can happen as a result of high current associated with the breakdown event. For example, the peak current for a 40 V HBM event, assuming 150 ns discharge time would be $(100\ pF \times 40)/150\ ns = 26\ mA$. The current carrying capability of the interconnect has to, therefore, be increased, for example, by adding more vias and increasing interconnect width to support 26 mA of current.

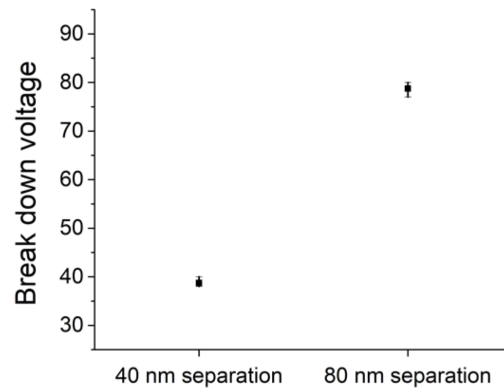
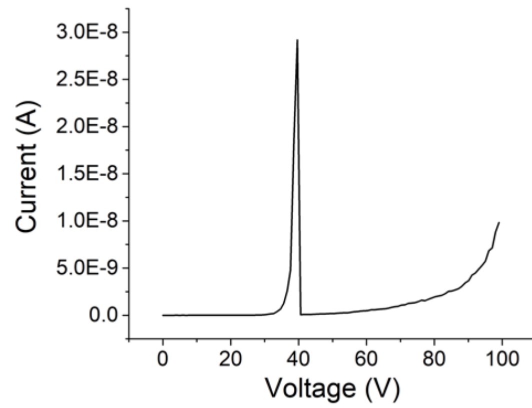


Figure 3.12: Experimentally determined breakdown voltage characteristics of the variable dielectric width capacitor with a dielectric thickness of 40 nm and 80 nm from about 10 measurements.



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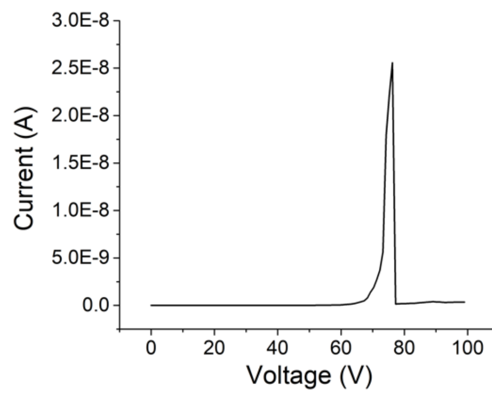

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Figure 3.13: Experimental I-V Characteristics of the variable dielectric width capacitor with (a) 40 nm, and (b) 80 nm metal separation.

3.3 Vertical MOSCAP Array

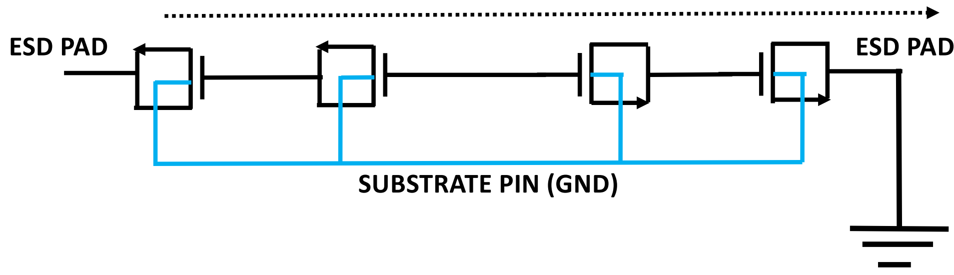
The second on-chip ESD monitor approach is the vertical MOSCAP array. The MOSCAPs in the array are realized using MOSFETs in the given technology. The working principle of the vertical MOSCAP array is outlined in 3.3.1. Design and experimental results for vertical MOSCAP arrays in GF 22 nm FDSOI are shown in 3.3.2.

3.3.1 Working principle

The basic structure of the vertical MOSCAP array consists of an array of capacitors in series. Capacitors in the array are realized using MOSFETs. The gate of the MOSFET is used as one terminal and the source and drain, tied together, serve as the second terminal of the capacitor. The basic working principle of the vertical MOSCAP array is similar to that of the variable dielectric width capacitor (Fig. 3.14). Both terminals of the capacitor arrays are exposed, and are subjected to ESD events. After any unit process in which an ESD event occurs, a voltage difference is developed between the un-grounded and grounded pads. The voltage is divided equally across the capacitors within the array, as the individual capacitors are of equal size (similar capacitance). Capacitor arrays with a smaller breakdown strength than the developed voltage will undergo breakdown. The induced ESD voltage is estimated by measuring the I-V curves of all the transistor arrays and identifying the transistor arrays where breakdown has occurred.

3.3.2 Fabrication in GF 22 nm FDSOI and experimental results

A schematic of the vertical MOSCAP array fabricated in GF 22 *nm* FDSOI is shown in Fig. 3.15. Here the capacitors are realized by using the gate as one terminal, and the source and drain, tied together, as the second terminal. The antenna rules provided with the technology ensure that the voltage at the internal floating nodes of the circuit do not cause breakdown of the individual capacitors within the array. Use of higher metal levels (M1-M2-



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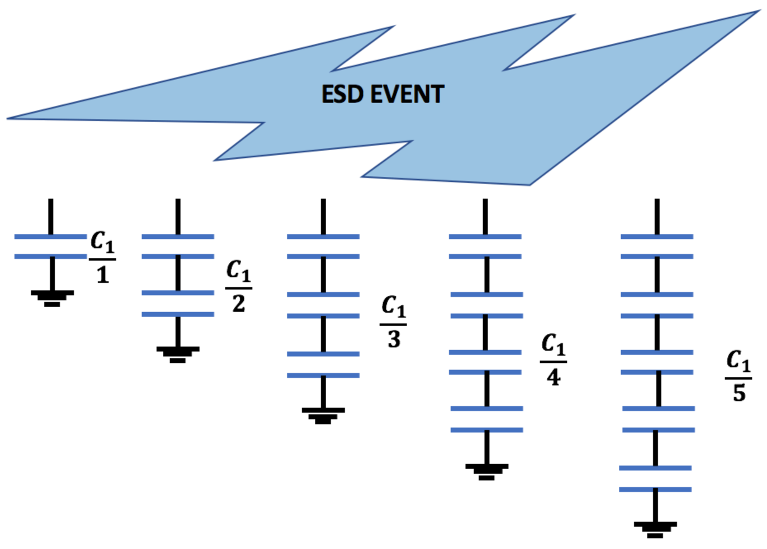

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Figure 3.14: Working principle of a vertical MOSCAP array (a) A four transistors array.Charge accumulation due to ESD events, results in voltage V being developed between the two ESD pads of which one is grounded. Capacitors in the array can break down depending on the magnitude of the voltage V developed between the ESD pads. (b) Multiple transistor arrays in parallel with common ESD event to all. Capacitor arrays with a smaller breakdown strength than the developed voltage, will undergo breakdown.

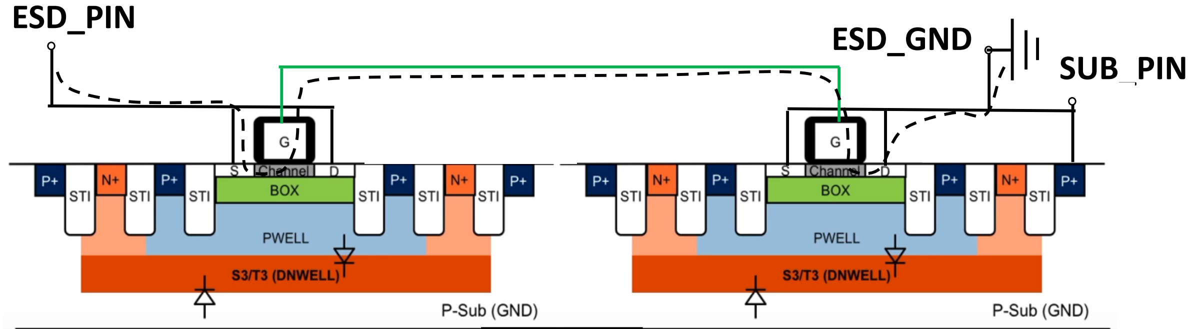


Figure 3.15: Cross-sectional view of a two transistor vertical MOSCAP array in GF 22 nm FDSOI technology, indicating the breakdown path when one of the ESD pad is grounded.

M1) to avoid a long single metal line (M1-M1-M1) is one example of avoiding an antenna violation. Antenna didoes are typically used at the I/O terminal pads and help to protect from breakdown of the gate oxide during fabrication by providing an alternate path for charge leakage (during plasma processing, sputtering, reactive-ion-etching, etc.) [53, 54]. However, antenna diode protection is not used at the terminals of the ESD monitor, as shown in Fig. 3.16, since adding the alternate path for breakdown (provided by the antenna diodes) defeats the purpose of the ESD detection circuit. Thin and thick gate oxide transistors were used in the design of the MOSCAP arrays. The following arrays were included in the fabricated test chip: two thin oxide transistors (2T thin), two thick oxide transistors (2T thick), four thin oxide transistors (4T thin), four thick oxide transistors (4T thick), and six thick oxide transistors (6T thick), with expected breakdown voltages of, respectively, 7 V, 12 V, 14 V, 24 V, and 36 V.

The experimental characterization of the MOSCAP array follows the same procedure as outlined for the variable dielectric width capacitor. In the first step, both terminal pads are grounded to dissipate any charge on the pads. In the second step, voltage is varied at one pad, keeping the other pad at ground until a breakdown is observed. The breakdown

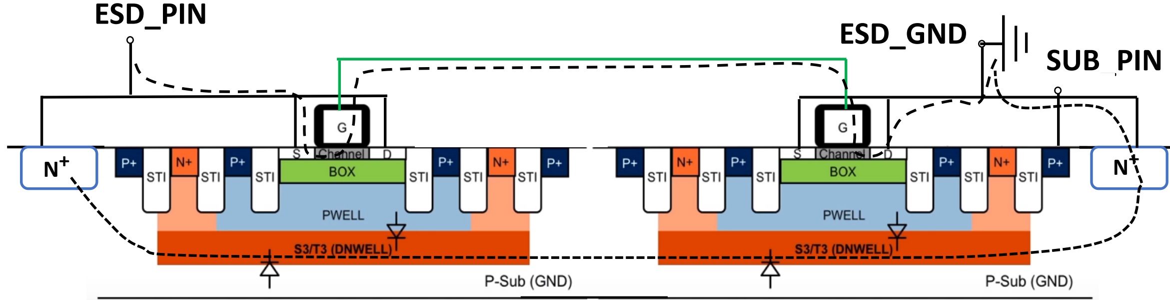


Figure 3.16: Cross-sectional view of a two transistor vertical MOSCAP array in GF 22 nm FDSOI technology with antenna diodes connected at the input, showing alternate path for breakdown.

voltage is noted from the I-V curve. If both ESD pads were initially charged to a voltage greater than the breakdown voltage, as a result of any ESD event, then grounding one of the ESD pads would have resulted in immediate breakdown. Thus, the breakdown voltage of the structure is determined.

In general, an oxide film loses its insulating property in two steps [55]. In the first step, traps are generated in the oxide that increase the leakage current through the oxide. The generation rate of traps depends on the type of dielectric. In case of high-k dielectrics stacked with interfacial SiO_2 (similar to the one used in GF 22 nm FDSOI technology), since high-k dielectrics have higher bulk defect density than SiO_2, the expected generation rate of traps is higher as compared to an SiO_2-only dielectric of the same thickness [56]. These traps could be the growth of an oxygen-deficient filament, facilitated by the grain boundaries of the overlaying high-k film [57]. Eventually due to the leakage current, these traps complete a percolation path through the oxide, bridging the two electrodes across the dielectric. Breakdown occurs when the number of injected carriers in the dielectric reaches a threshold value [58]. Power dissipation through the initial percolation path controls the second stage of the breakdown transient, which determines the post-breakdown conduction property of the oxide [55]. A hard breakdown is characterized by a large change in voltage

or current during the breakdown transient and a post-breakdown I-V characteristic that is essentially ohmic. The power dissipated during breakdown is high enough to melt silicon and allow the molten silicon to flow through the oxide. This results in an ohmic short-circuit across the oxide, as the power dissipated exceeded the threshold of irreversible thermal damage. A soft breakdown is detected by a much smaller change of voltage or current after breakdown and by post-breakdown characteristics which can be described by a power law [36]. The thermal damage in soft-breakdown is reversible [38, 39].

I-V characteristics of the five vertical MOSCAP array structures are shown in Fig. 3.17. A validation sweep is performed after the test sweep to ensure that breakdown has actually occurred during the test sweep. Transistors were also swept in the negative voltage direction to ensure that a breakdown has occurred. Breakdown characteristics of the MOSCAP array are shown in Fig. 3.18. The 2T thin structure breaks down at 6-7.5 V, 4T thin at 12-15.5 V, 2T thick at 11-12 V, 4T thick at 22-24 V, and 6T thick at 32-35 V.

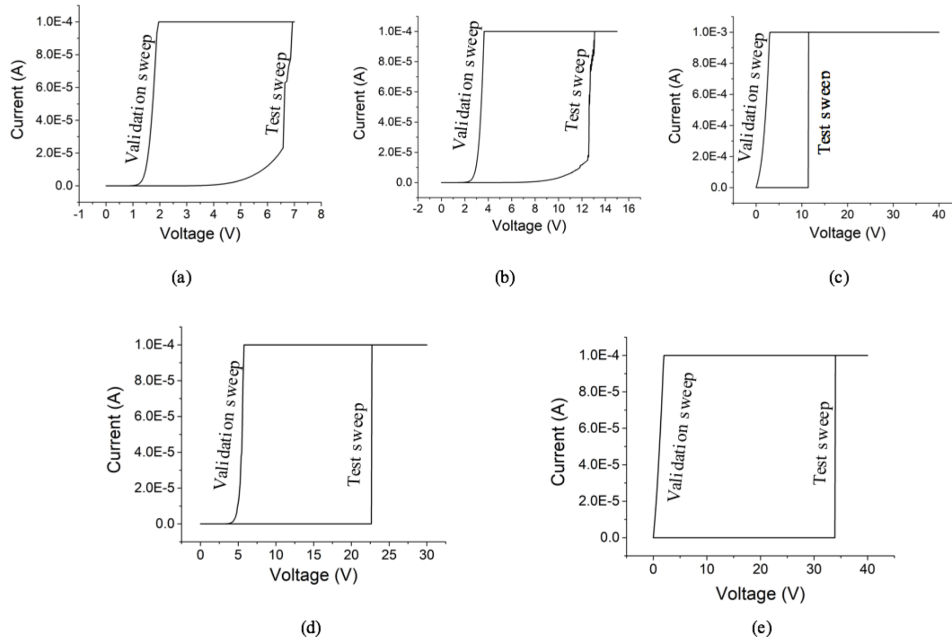


Figure 3.17: Experimental I-V characteristic of vertical MOSCAP array. (a) 2T thin oxide transistor array. (b) 4T thin oxide transistor array, (c) 2T thick oxide transistor array, (d) 4T thick oxide transistor array, and (e) 6T thick oxide transistor array.

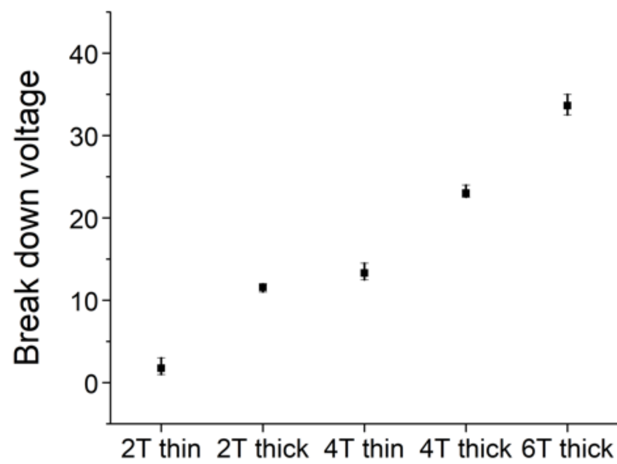


Figure 3.18: Experimental breakdown characteristics of vertical MOSCAP array.

3.4 Theoretical Analysis of the ESD Sensor

The basic working principle of ESD sensors when employed in ICs is presented. The sources of ESD could be direct contact, triboelectric charging or field induced charging. For the case of direct contact with the ESD source, consider the model shown in Fig. 3.19. Here the ESD source capacitance is represented as C_{hbm}, with resistance R_{hbm} and is charged to V_{hbm}. The charge accumulated in the ESD source capacitor is $Q_{hbm} = C_{hbm}V_{hbm}$. Let the capacitance per unit area for unit thickness be denoted as $C'_{ox}(C'_{ox} = \frac{Cd_{ox}}{A})$ and the breakdown field of oxide be denoted by E_{br}. The ESD sensor is assumed to have an oxide of area A_{os}, with an oxide thickness d_{os}, resulting in a sensor capacitance $C_{sen} = A_{os}C'_{ox}/d_{os}$. The effective series resistance (ESR) of the sensor is denoted by R_{sen}. Similarly let a device macro in the chip be represented as C_{max} with an ESR of R_{mac}. The macro is assumed to have an oxide of area A_{om}, with an oxide thickness d_{om}, resulting in a macro capacitance $C_{mac} = A_{om}C'_{ox}/d_{om}$. The charge required for the breakdown of sensor is

$$Q_{br} = C_{sen} \cdot V_{br} = \frac{C'_{ox}}{d_{os}} \cdot A_{os} \cdot E_{br} \cdot d_{os}.$$

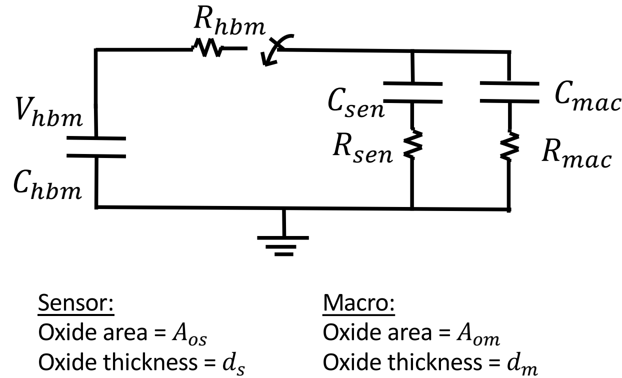


Figure 3.19: Theoretical model of ESD sensor for the case of direct contact with ESD source.

Upon contact between the ESD source (at voltage V_{hbm}) and the ESD sensor capacitance C_{sen} and macro capacitance C_{max} (both assumed to be initially uncharged), transfer of charge takes place (Fig. 3.19). Here the ESD event is represented by the closing of the switch. The

ESD current will charge the ESD sensor capacitors until the capacitor starts to conduct current by tunnelling [59, 60].

At time t = 0, current through the sensor is

$$I_{t=0} = \frac{V_{hbm}}{R_{hbm} + (R_{sen}||R_{mac})} \frac{R_{mac}}{R_{sen} + R_{mac}},$$

and the current density would be $\frac{I_{t=0}}{A_{os}}$. For very thin oxide, the tunnelling of current occurs at low voltage (around 1 V). When the ESD sensor is subjected to a large current density, it will charge quickly and ultimately undergo breakdown (the ESD sensor capacitor will not withstand more than a few volts before it undergoes breakdown). During ESD discharge, current is forced through the ESD capacitor, exhibiting a current source-like behaviour [61]. When the oxide is subjected to very high current density, the amount of charge required to break the oxide is low [62], resulting in instantaneous breakdown of the oxide. The voltage that would be developed is given by

$$V = \frac{C_{hbm} \cdot V_{hbm}}{C_{hbm} + C_{sen} + C_{mac}}.$$

Here both the sensors and macro are subjected to the same voltage V. Breakdown of the sensor occurs if

$$\begin{aligned} C_{sen} \cdot V \geq & Q_{br}, \\ \implies C_{sen} \cdot V \geq & \frac{C'_{ox}}{d_s} \cdot A_{os} \cdot E_{br} \cdot d_s = C'_{os} A_{os} \cdot E_{br}. \end{aligned}$$

The maximum oxide area of the ESD sensor is therefore

$$A_{os} \leq \frac{C_{sen} \cdot V}{C'_{ox} \cdot E_{br}}.$$

In case of field induced charging/CDM model as in Fig. 3.5, the equivalent circuit can be drawn as shown in Fig. 3.20. Here, to the first order, both the sensor and macros see the same voltage V assuming grounding occurs to both at the same time (note that here there

is no direct contact with the ESD source). The sensor breaks down if

$$C_{sen} \cdot V \geq Q_{br},$$
$$\implies C_{sen} \cdot V \geq \frac{C'_{ox}}{d_s} \cdot A_{os} \cdot E_{br} \cdot d_s = C'_{os} A_{os} \cdot E_{br}.$$

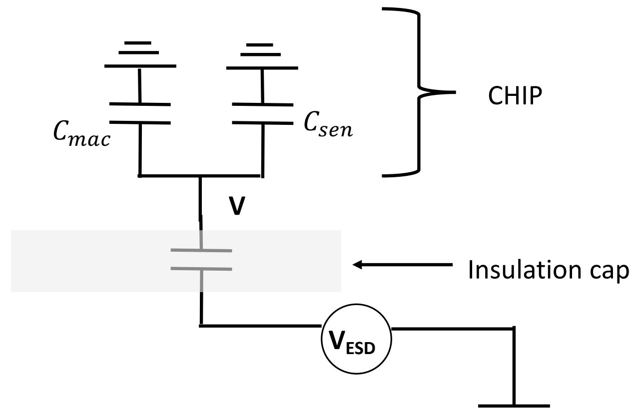


Figure 3.20: Theoretical model of ESD sensor in case of field induced charging.

Thus, the area constraints of the ESD monitor for a given ESD voltage detection for HBM, MM, and CDM of the IC can be found.

3.5 Conclusions

Two approaches for an on-chip ESD detector are proposed. Variable dielectric width capacitor is suitable for high voltage detection. The lower limit of voltage detection using variable dielectric width capacitor is limited by the minimum metal separation supported by the given technology (40 nm in case of GF 22 nm FDSOI). This method is area efficient since transistors are not used in the implantation of the variable dielectric width capacitor. The second approach, vertical MOSCAP arrays, is ideally suited for low voltage detection. The granularity in ESD voltage level detection can be tuned by using thin and thick gate

oxide devices. For high voltage detection that requires a large number of transistors however, this approach becomes area inefficient. The proposed prototypes, variable dielectric width capacitor and vertical MOSCAP array, can be included in any die, manufactured by using any process to help with ESD monitoring during packaging, assembly and transport. A mathematical model of the sensors employed in the ICs when subjected to an ESD event is presented. Determination of ESD voltage using the sensors with multiple experiments/runs is presented in the next chapter.

Chapter 4

ESD voltage estimation using sensors

4.1 Introduction

In the previous chapter, modelling and I-V characterization of the ESD sensors was carried out, and statistical distribution of break down voltage across multiple samples was noted. In using these ESD sensors to determine the ESD voltage, two random events are involved. Prior to the experiment, ESD is a random event with some unknown probability distribution. The oxide breakdown in the ESD sensors follows a Weibull random distribution. For example, consider an IC-1 that consists of ESD sensors all of type-A (say type-A refers to one particular thickness of the oxide). In the first run, we pass it through an ESD environment and at the end of the experiment/run, say 4 devices are broken, while 6 remain unbroken. In the second run, we pass IC-2 (we can also pass the IC-1, but it has only 6 devices unbroken) through the ESD environment and this time 6 devices are broken (4 remained unbroken) as shown in Figure 4.1. The goal here is to estimate the probability density function (PDF) of the ESD environment using the observed evidence i.e., 4 devices broke in the first run and 6 devices broke in the second run. A Bayesian method is developed for ESD voltage estimation using these sensors in Section 4.2. In Section 4.3, ESD testing of the sensors is carried out with an ESD gun for high voltage (high-charge injection) and with a modified setup for low voltage

testing (or low charge injection). Section 4.4 uses the Bayesian method developed in 4.2 to estimate the applied ESD voltage from the observed evidence in Section 4.3 and compares it to the actual applied ESD voltage.

4.2 Problem statement and Bayesian method formulation

The two random events involved in determining the ESD voltage using the sensors are (i) oxide breakdown of the sensors (ii) ESD voltage being subjected to the ICs in multiple runs. The goal is to estimate the probability density function (PDF) of the ESD environment from the observed evidence in multiple runs. In general, the problem statement can be defined as follows. We start with X copies of device type A, Y copies of device type B, ..., Z copies of device type C. Assume that at the end of one experiment/run, x, y, ..., and z number of devices of type A, B, ..., C broke down respectively (x', y', ..., z' of A, B, ..., C didn't break). Then the problem can be stated as

$$\text{f}(V|x\,of\,A\,and\,y\,of\,B\,...and\,z\,of\,C\;broken)dV$$
$$= \frac{p(x\,of\,A\,and\,y\,of\,B\,...\,z\,of\,C|V)f(V)}{\int_0^{V_L} p(x\,of\,A\,and\,y\,of\,B\,...\,z\,of\,C|V)f(V)dV}$$
$$= \frac{\binom{X}{x}(P_A(V))^x(1-P_A(V))^{x'}\cdots ZC_z(P_C(V))^z(1-P_C(V))^{z'}}{\int_0^{V_L}(\binom{X}{x}(P_A(V))^x(1-P_A(V))^{x'}\cdots ZC_z(P_C(V))^z(1-P_C(V))^{z'})f(V)dV} \tag{4.1}$$

where $f(V)$ is the PDF of ESD voltage. $P_A(V), P_B(V), \ldots, P_C(V)$ represent the probability of breakdown of ESD sensors of type $A, B, \ldots, C$, respectively, with voltage V.

$$\text{P}_A(V) = 1 - e^{-(\frac{V}{\lambda_A})^{k_A}} \tag{4.2}$$

$$\text{P}_B(V) = 1 - e^{-(\frac{V}{\lambda_B})^{k_B}} \tag{4.3}$$

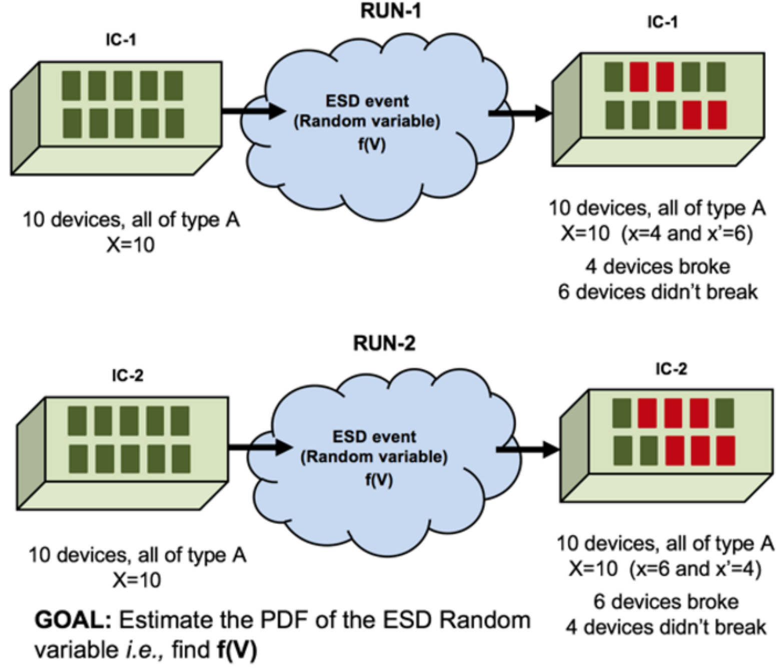
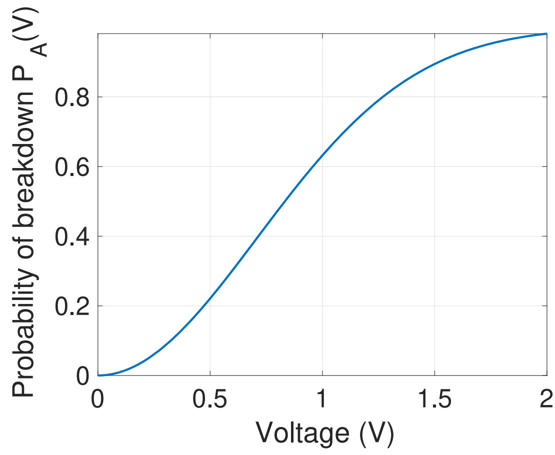


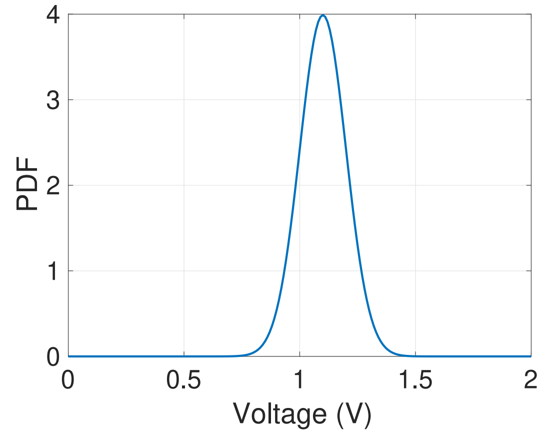
Figure 4.1: An example demonstrating an IC with ESD sensors passing through an ESD environment

where λ_A and k_A are the Weibull parameters for the device type-A, λ_B and k_B for device type-B and so on. $\binom{X}{x}$ represents X combination x. Here, the breakdown of sensor- A is independent of sensor- B, C when all are subjected to the same voltage V because the electric field setup (which initiates the breakdown) across sensor-A is independent of the electric field across sensor-B, C and there is no coupling of electric field across different sensors. Similarly, each copy of sensor-A breakdown independent of other copies of A when subjected to the same voltage. For the first run, as we are unaware of $f(V)$, we assume a uniform PDF with an upper voltage limit V_L. After the first run, posterior probability updating of $f(V)$ is done, i.e., $f(V|x \text{ of } A, \ldots, \text{ and } z \text{ of } C)$ after the first experiment becomes the new $f(V)$ for the second experiment. With multiple runs, $f(V)$ approaches the actual ESD voltage.

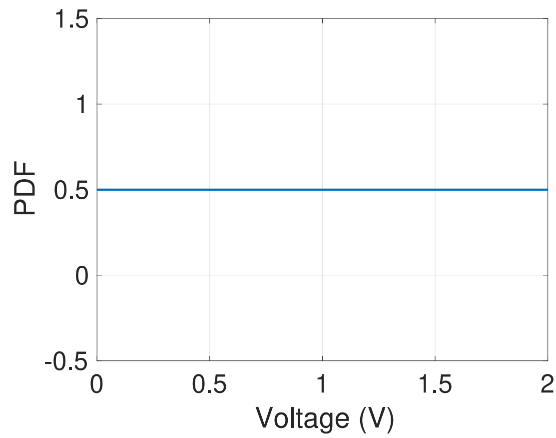
To illustrate the approach here, consider there are N experiments/runs each with X copies of device-A. The probability of breakdown of device-A with voltage V, $P_A(V)$, is



(a)



(b)



(c)

Figure 4.2: ESD voltage estimation. (a) $P_A(V)$ of device-A. (b) Actual ESD voltage PDF, assumed to be a normal distribution here. (c) Initial starting assumption for ESD PDF (for the first run).

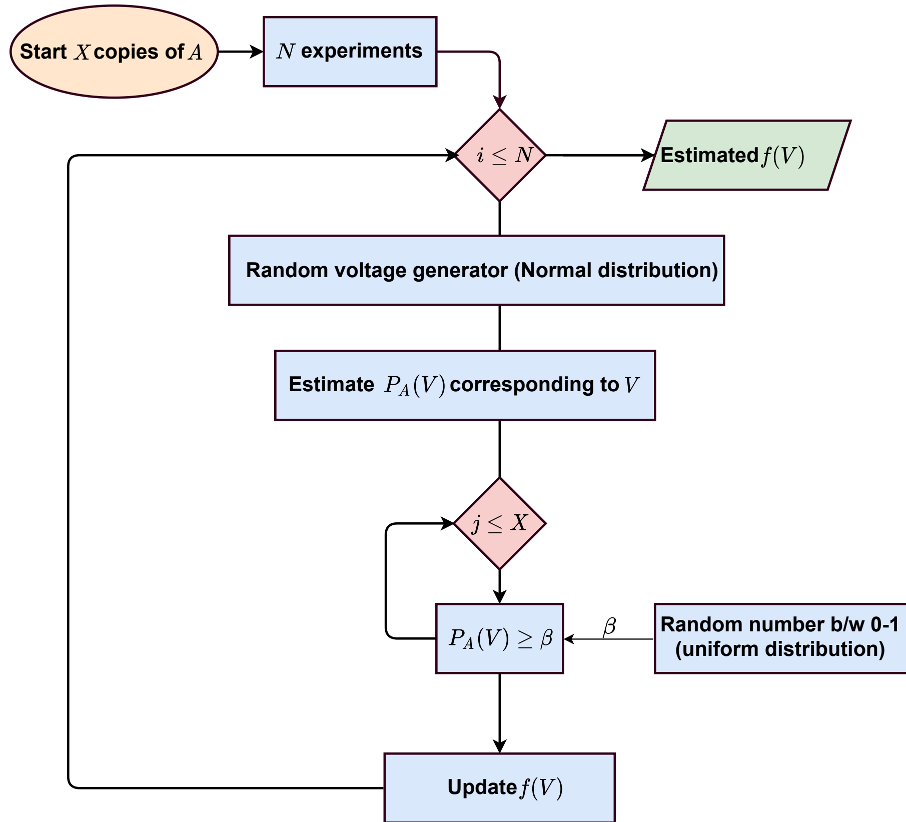


Figure 4.3: Flow chart for Bayesian update of ESD voltage

as shown in Figure 4.2(a). Device-A and $P_A(V)$ shown in this example are not the real fabricated devices in GF22FDX technology. The upper voltage limit of 2 V and $P_A(V)$ shown here are are to illustrate the concept only. Assume that the actual ESD PDF present is a normal distribution as shown in Figure 4.2(b). At the end of N experiments/runs, the estimated PDF would closely match the normal distribution. For the very first run, we are unaware of the ESD PDF, so we assume a uniform ESD PDF with upper voltage limit V_L as shown in Figure 4.2(c). In a single run, all the X copies of device-A are subjected to the same voltage value V (This V could be any value in the voltage normal distribution of Figure 4.2(b) for a given run. V varies with each run/experiment). Device-A has some $P_A(V)$ corresponding to the V value in each run. But among X copies of device-A, some will break and some won't break even though all are subjected to the same voltage value V.

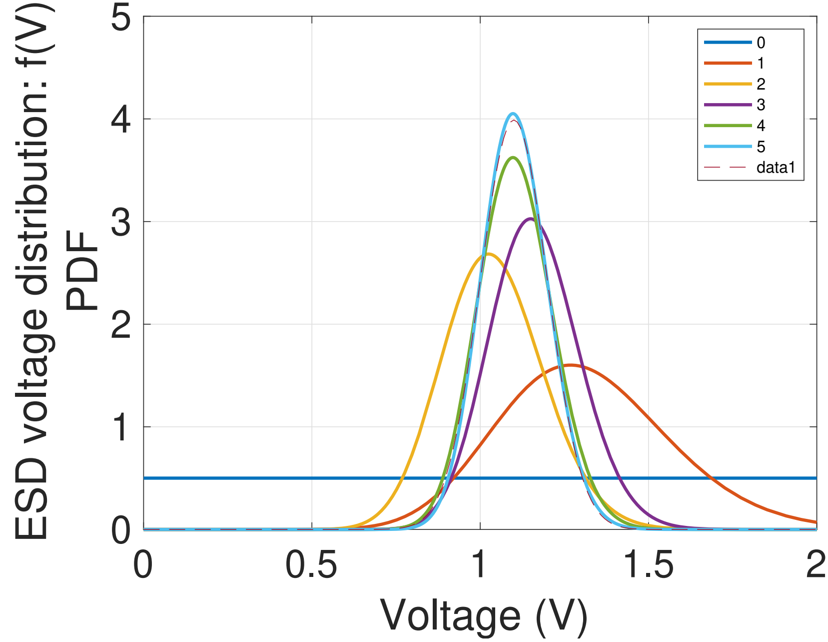
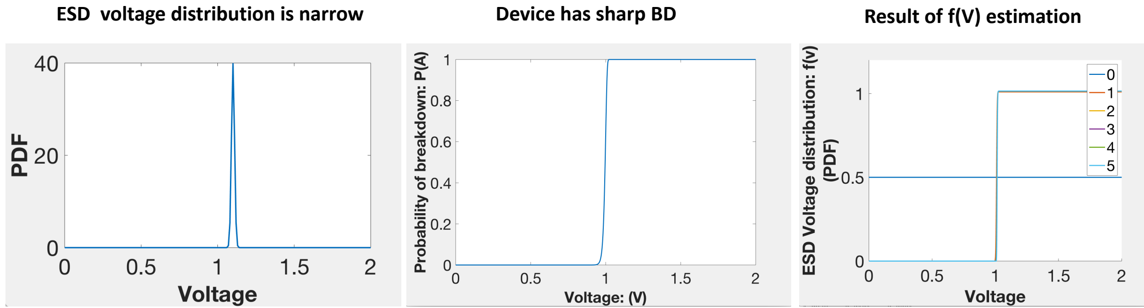


Figure 4.4: ESD voltage estimation with each run. Dotted line represents the actual ESD voltage. (0) represents the initial assumed ESD PDF. (1), (2), (3), (4), (5) represents posterior updating of f(V) after each experiment. At the end of run (5), f(V) approaches the actual ESD voltage

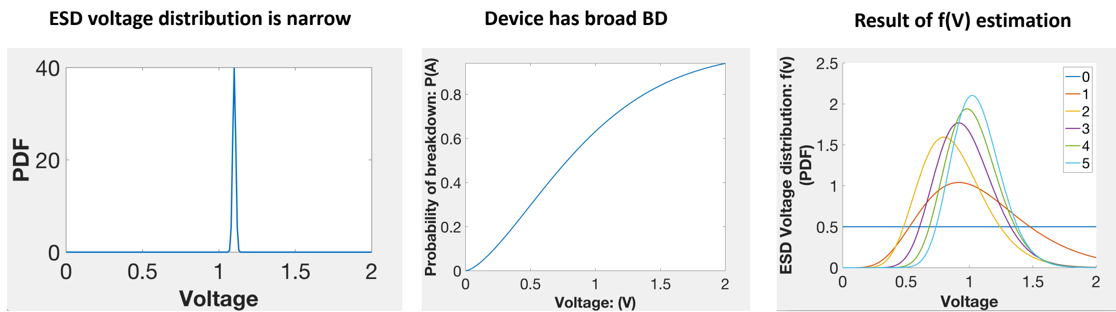
To simulate this, a random number β is generated (between 0-1) for each copy of device-A and is compared with $P_A(V)$. If $P_A(V) > \beta$, that particular device undergoes breakdown. At the end of the first experiment, a PDF update is done based on the number of devices broken out of X copies. This is repeated for each experiment i until $i = N$, at which point the last updated $f(V)$ is given. The entire process flow chart is shown in Figure 4.3. The results for N=5, X=10 for the device type-A of Figure 4.2(a) is shown in Figure 4.4. The dotted line is the actual ESD voltage assumed (same as in Figure 4.2(b)). (0) represents the initial assumption of uniform ESD PDF voltage. (1), (2), (3), (4), and (5) represent posterior updating of f(V) after each experiment. In this case, at the end of experiment-5, the estimated ESD PDF closely matches the actual ESD PDF.

4.2.1 Different cases in ESD voltage estimation

There are 4 different cases in ESD voltage estimation, depending on whether the actual ESD voltage distribution is narrow or broad, and the sensor breakdown is sharp or broad. In case-1 where ESD breakdown voltage distribution is narrow and the device has sharp breakdown characteristics, estimated PDF would be similar to a step waveform as indicated in Fig. 4.5(a). When the ESD breakdown voltage distribution is narrow and the device has broad breakdown range as in case-2 (Fig. 4.5(b)), the estimation evolves to be a bell-shaped curve. In case-3 when the ESD breakdown voltage distribution is broad and the device has sharp breakdown characteristics, the f(V) estimate is sharp (Fig. 4.5(c)). Case-4 represents the most general case, where both the ESD breakdown voltage distribution and device breakdown are broad. The resulting f(V) is a bell shaped curve and approaches the actual ESD voltage distribution with multiple runs, as indicted in Fig. 4.5(d).



(a)



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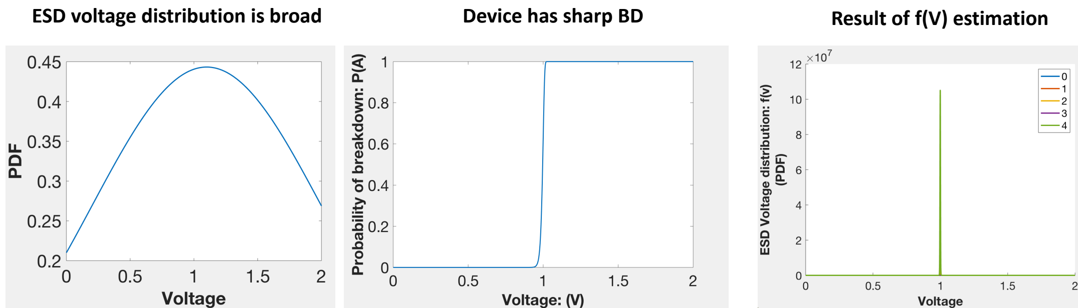

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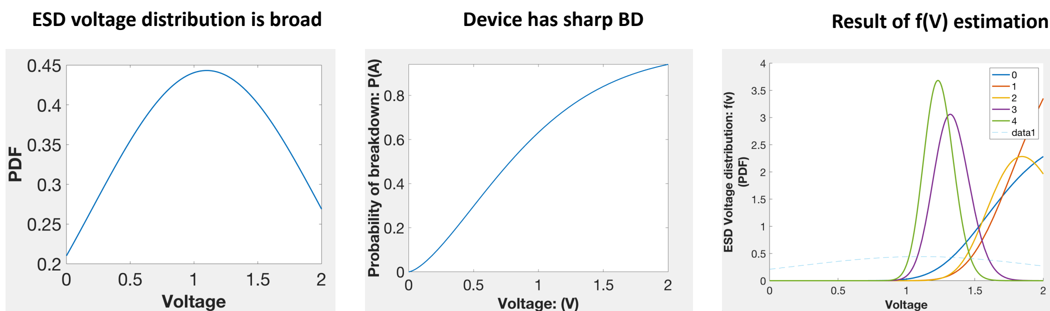


(d)

Figure 4.5: Different Cases (a),(b),(c) and (d) in ESD voltage estimation

4.3 ESD testing of the sensors

A handheld, battery operated ESD simulator (16.5kV ESD Simulator for IEC/EN 61000-4-2 from EMC, www.esdguns.com) was used for testing the sensors at high voltages. The simulator is suitable for performing ESD tests on systems in accordance with the standard IEC/EN 61000-4-2, MIL-STD-461G test standards. Two types of discharge can be done with the gun: (i) air discharge and (ii) contact discharge. Air discharge voltage is adjustable from 200 V to 16 kV in steps of 100 V, whereas contact discharge voltage ranges from 200 V to 10 kV in steps of 100 V. The discharge capacitance of the ESD gun is 150 pF and discharge resistance is 330 Ω. In case of contact discharge, the probe of the generator is placed directly on the test object. The actual impulse triggering takes place via a relay contact and reduces the influencing factors such as approach speed and air humidity. The test setup is shown in Figure 4.6 along with the ESD gun in discharge mode in Figure 4.7. For ESD testing at discharge voltages below 200 V, the test setup shown in Figure 4.8 is used. Here an external cap (C_{hbm} = 150 pF) is charged to the desired voltage V_{hbm} and the stored charge is then released to the devices under test by momentary closure of a switch. The ESD sensors in the ICs are connected in parallel to an active daisy chain unit in the IC. Here, C_{hbm} and R_{hbm} represent the ESD capacitance and resistance of a HBM model. C_{ESD-A}, C_{ESD-B} and C_{active_daisy} represent the ESD sensor capacitance of device type-A, device type-B, and active daisy-chain macro respectively. R_{active_daisy} and ESR represent the series resistance of the ESD sensors and active-daisy chain. ESR and R_{active_daisy} comes from the contact wire resistance and resistance of the metal traces to the ESD sensor, including the back end of the line (BEOL) metal contacts. C_{hbm} is initially charged to voltage V_{hbm} from a voltage source V_s. C_{ESD-A}, C_{ESD-B} and C_{active_daisy} are initially uncharged. Upon momentary closure of the switch, charge sharing takes place. The wire resistances and ESR of the ESD sensor is about 15 Ω and is negligible compared to R_{hbm}. Charge sharing takes place according to

$$
\begin{aligned}
C_{hbm}V_{hbm} =&(C_{hbm} + C_{ESD-A} + C_{ESD-B} + C_{active_daisy})V \\
V =&\frac{C_{hbm}V_{hbm}}{C_{hbm} + C_{ESD-A} + C_{ESD-B} + C_{active_daisy}}
\end{aligned} \tag{4.4}
$$

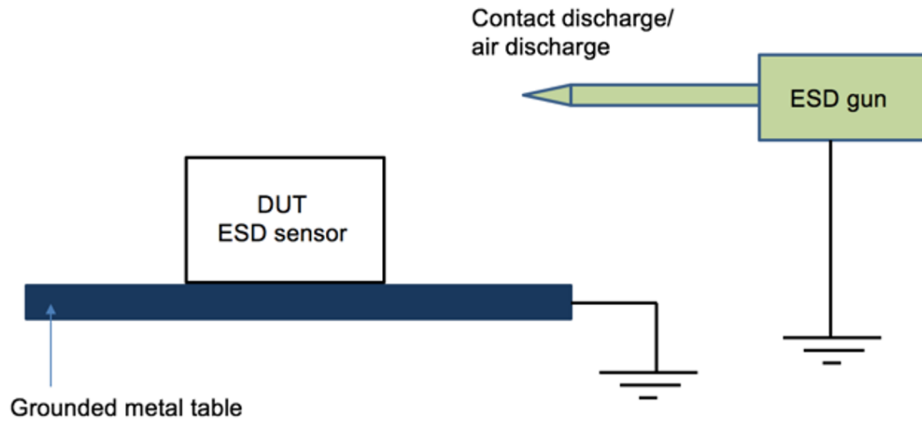


Figure 4.6: ESD gun testing of the sensors.

Figure 4.7: ESD gun in discharge mode.

The exact voltage that appears across the ESD sensor V is simulated for different applied voltages V_{hbm}. Plugging in the resistance and capacitance values i.e., C_{hbm}=150 pF, C_{ESD-A}

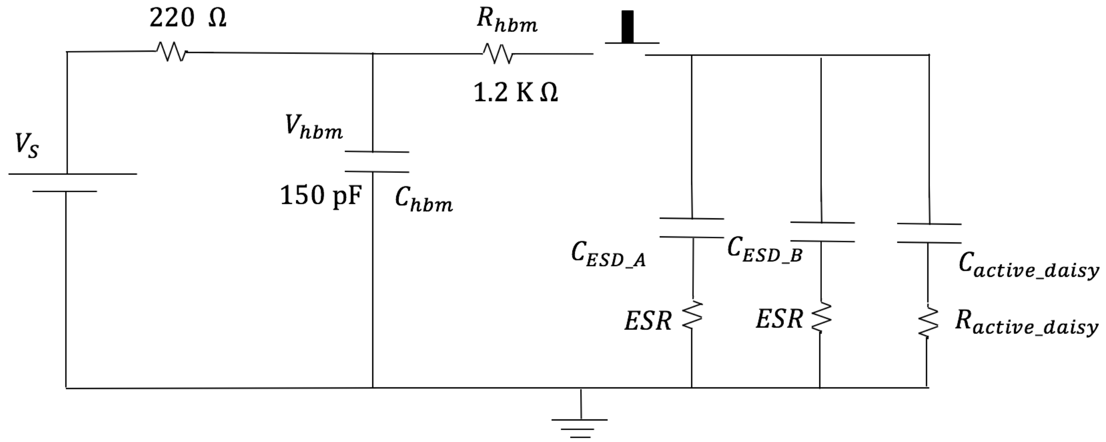


Figure 4.8: Test setup for ESD testing at low voltages. ESD sensors are in parallel with an active daisy chain macro.

$= 0.24\ pF$, $C_{ESD-B} = 0.12\ pF$, $C_{active_daisy} = 10\ pF$, $ESR = 15\ \Omega$, R_{hbm}= 1.2 $k\Omega$, and R_{active_daisy}= 15 Ω gives $V = 7.5\ V$ for an applied voltage of 8 V (V_{hbm}=8 V), and V=14.05 V for an applied voltage of 15 V. Before application of the ESD pulse, the sensors (device type-A and type-B) and the macros were characterized, shown in Figure 4.9 . Figure 4.9(a) shows the active daisy chain where a square wave output is obtained for an input square wave. Figure 4.9(b) and Figure 4.9(c) show I-V characterization of the sensor type-A and sensor type-B respectively. The current at low voltages are of the order of 100 nA. Characteristics of the daisy chain macro and ESD sensors after ESD pulse are shown in Figure 4.10. Here the ESD pulse applied was 15 V (or the charge injected is equal to $15V \cdot 150\ pF = 2.25\ nC$) The output of the daisy chain macro becomes a short-circuit as shown in Figure 4.10(a) with short circuit current of about 10 mA. Both the ESD sensors are broken (Figure 4.10(b) and Figure 4.10(c)) as indicated by the current at low voltages (current is of the order of 0.1 mA and the I-V characteristics becomes almost linear). Depending on the voltage applied (or charge injected), sensors may or may not breakdown. Also, for the same voltage applied to sensors of same type, some may or may not break down as oxide breakdown in sensors is random. The experimental data is shown in Table 4.1 Individual sensors and macros in standalone mode were also tested with the same conditions, and the experimental results are

summarized in Table 4.2, Table 4.3, and Table 4.4. Table 4.5 shows the case when sensors A and B were tested in parallel (with no macro).

Table 4.1: ESD testing with sensors and active macros. Broken devices are denoted by the ✓symbol and not-broken by the × symbol

	Applied charge	Type-A	Type-B	Macro	No: of runs
Case-I	$3\ V \times 150\ pF$	×	×	×	10
Case-II	$8\ V \times 150\ pF$	✓	×	✓	7
Case-III	$15\ V \times 150\ pF$	✓	×	✓	2
	$15\ V \times 150\ pF$	✓	✓	✓	2
Case-IV (ESD gun)	$200\ V \times 150\ pF$	✓	✓	✓	5

Table 4.2: Standalone ESD testing of sensors-A.

	Applied charge	Type-A	No: of runs
Case-I	$3\ V \times 150\ pF$	×	6
Case-II	$8\ V \times 150\ pF$	✓	5
Case-III	$15\ V \times 150\ pF$	✓	5
Case-III	$200\ V \times 150\ pF$	✓	5

Table 4.3: Standalone ESD testing of sensors-B.

	Applied charge	Type-A	No: of runs
Case-I	$3\ V \times 150\ pF$	×	6
Case-II	$8\ V \times 150\ pF$	×	5
Case-III	$15\ V \times 150\ pF$	×	1
	$15\ V \times 150\ pF$	✓	3
Case-III	$200\ V \times 150\ pF$	✓	5

Table 4.4: Standalone ESD testing of Macro.

	Applied charge	Type-A	No: of runs
Case-I	$3\ V \times 150\ pF$	$\times$	5
Case-II	$8\ V \times 150\ pF$	✓	4
Case-III	$15\ V \times 150\ pF$	✓	4
Case-III	$200\ V \times 150\ pF$	✓	4

Table 4.5: ESD testing with sensors A and B in parallel.

	Applied charge	Type-A	Type-B	No: of runs
Case-I	$3\ V \times 150\ pF$	$\times$	$\times$	5
Case-II	$8\ V \times 150\ pF$	✓	$\times$	5
Case-III	$15\ V \times 150\ pF$	✓	$\times$	1
	$15\ V \times 150\ pF$	✓	✓	3
Case-IV (ESD gun)	$200\ V \times 150\ pF$	✓	✓	4

4.4 Applied ESD voltage prediction from observed evidence

In the case of real ESD events, the ESD voltage to which the IC was subjected to would be unknown. Only the number of experiments/runs and the number of devices broken in each run would be available. Estimation of the applied ESD voltage using the Bayesian approach developed in Section 4.2 was done using the observed data in Table 4.1. To verify the approach developed in Section 4.2, the estimated ESD voltage is to be compared with the actual ESD voltage applied.

The observed evidence is the number of sensors broken in each case (i.e., entries corresponding to Case-I, Case-II, Case-III, and Case-IV in Table 4.1). The probability of breakdown of the sensors $P_A(V)$ and $P_B(V)$ is given. $P_A(V)$ and $P_B(V)$ were obtained before the

experiment by characterizing a large number of devices and is shown in Figure 4.11. The estimated ESD voltage for each of the cases is shown in Figure 4.12.

Figure 4.12(a) shows Case-I, where the Bayesian method predicts an applied ESD voltage $\leq 5\ V$ with equal probability. The actual ESD voltage applied in Case-I is $3\ V$ (from Table 4.1). Note that the $3\ V$ applied is less than the breakdown range of both the sensors.

In Case-II (Figure 4.12(b)), the estimated ESD voltage after accounting for the voltage drop ($0.5\ V$) is $8.15V$ ($7.69\ V + 0.5\ V = 8.19\ V$). In this case, the actual applied ESD voltage is $8\ V$ (from Table 4.1).

In Case-III (Figure 4.12(c)), the estimated ESD voltage is $15.26\ V$ after taking into account for the voltage drop of $0.95\ V(14.31\ V + 0.95\ V = 15.26\ V)$. Here, $14.31\ V$ is the peak in $f(V)$ estimation. In this case, the actual applied ESD voltage is $15\ V$ (from Table 4.1).

Finally, in Case-IV, the estimated ESD voltage is $\geq 16\ V$. Here the applied ESD voltage is $200\ V$ and is much greater than the breakdown of both the sensors. In this case, as all the sensors broke down, the Bayesian method predicts an ESD voltage $\geq 16\ V$ (Fig. 4.12(d)).

ESD estimation from standalone tests for sensors-A and sensors-B are compared with the results in Fig. 4.12. In Case-I, sensor-A used alone (results from Table 4.2) and Sensor-B used alone (results form Table 4.3) would predict voltages as shown in Fig. 4.13(a). With sensor-A alone it would predict ESD voltage $\leq 5V$ with equal probability as none of the sensors broke down. Similarly, with only sensor-B it would predict ESD voltage $\leq 12V$ with equal probability as none of the sensor-B broke down. When both sensors-A and B are used for the experiments as in Table 4.1, the Bayesian estimate would predict ESD voltage $\leq 5V$ as both the sensors didn't undergo breakdown (Fig. 4.12(a)).

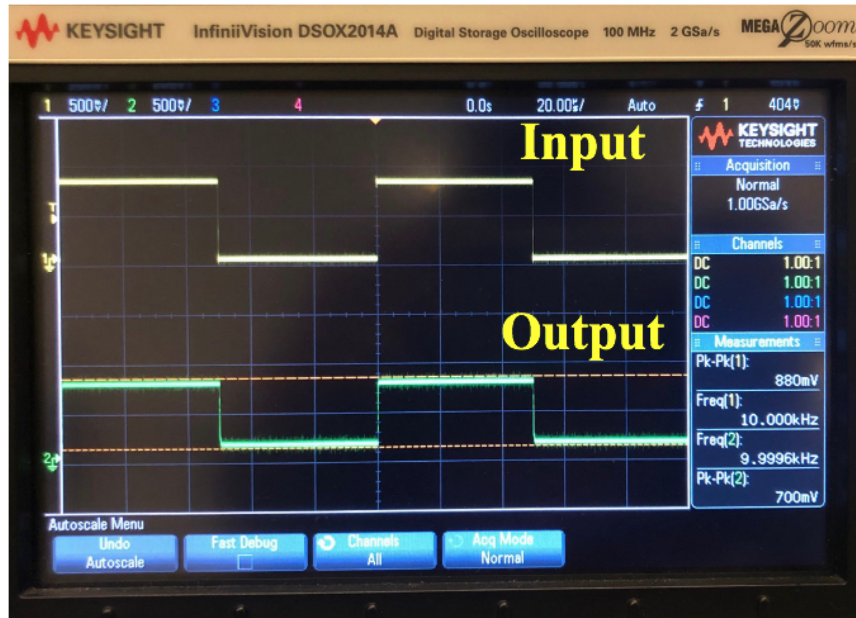
Results for Case-II when A and B are tested separately are shown in Fig. 4.13(b). Here estimation from sensor-A predicts voltage $\geq 8V$ with equal probability as all sensors broke down, while results from B alone would predict ESD voltage $\leq 15V$ with equal probability as none broke down. Compare this result with Fig. 4.12(b), where both A and B were used. Here the result predicted peak voltage $8.15\ V$ as all the A broke down, but no B broke down.

(similar to a logic "and" operation of standalone cases with sensors-A and B)

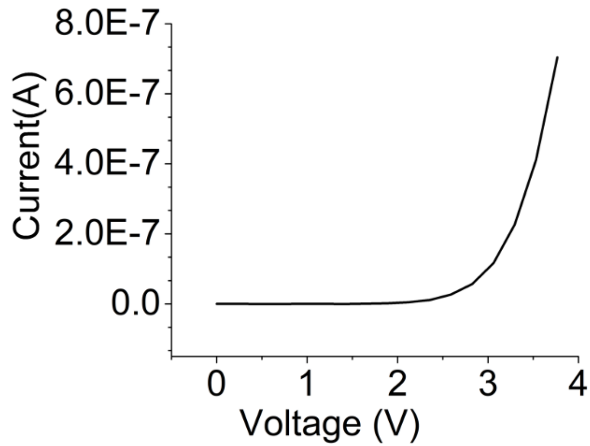
For Case-III, results from sensor-A alone (Table 4.2) would again predict ESD voltage $\geq 8V$ with equal probability as all sensors broke down (Fig. 4.13(c)). Results from B alone would predict a peak close to 15 V because here 1 sensor did not undergo breakdown out of the 4 (results from Table 4.3). So, the Bayesian estimate would give a high confidence for voltage around $\sim 15V$. (Note that results from Table 4.1 predict a voltage peak of 15.26 V as shown in Fig. 4.12(c))

Finally, standalone results for case-IV is shown in Fig. 4.13(d). Here the Bayesian estimation from sensor-A alone (Table 4.2) would predict a breakdown voltage ≥ 8 V with equal probability as all sensors broke down, while results from sensor-B alone (Table 4.3) experiments would predict voltage $\geq 16V$ with equal probability. If we compare this with the experimental data from Table-1 where both sensors A and B were used, it gives an estimate ≥ 16 V (similar to a logic "and" operation of standalone cases with sensors-A and B).

In summary, when multiple sensor types are used in parallel, the predicted ESD voltage from the observed evidence closely matches the actual ESD voltage



(a)



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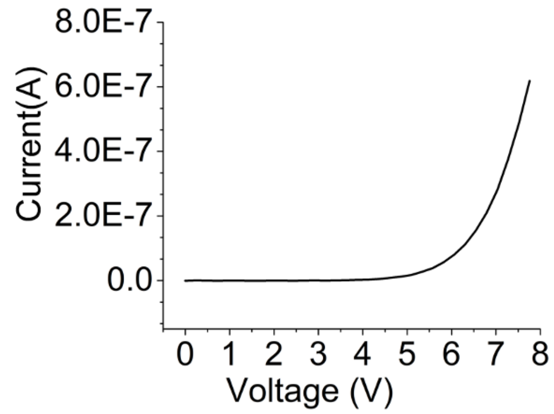
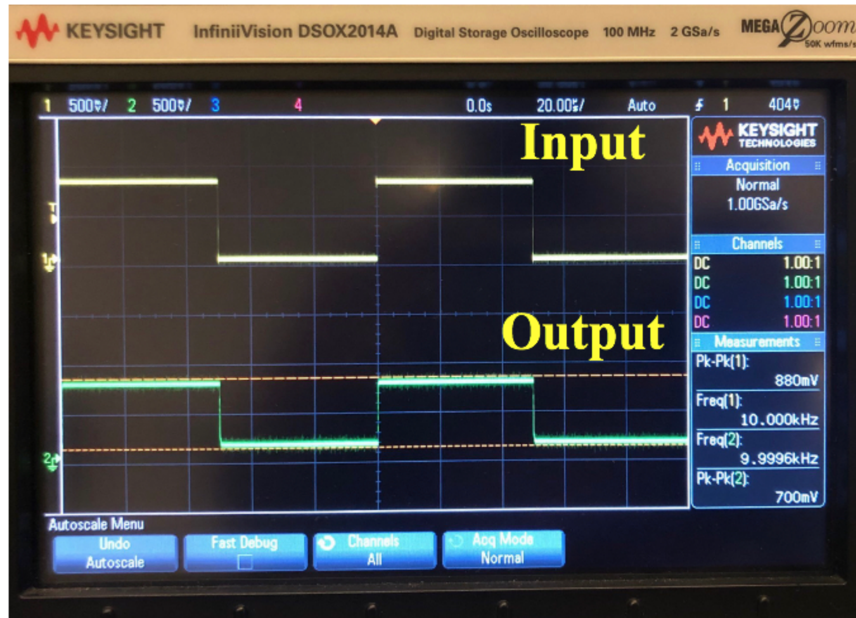
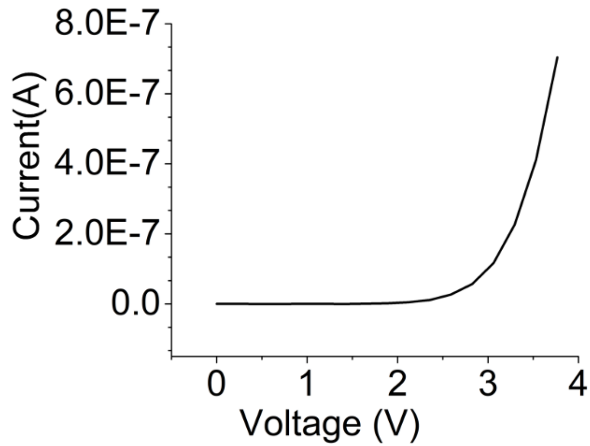


(c)

Figure 4.9: Characterization of (a) daisy chain macro, (b) ESD sensor type-A (c) type-B before application of ESD pulse.



(a)



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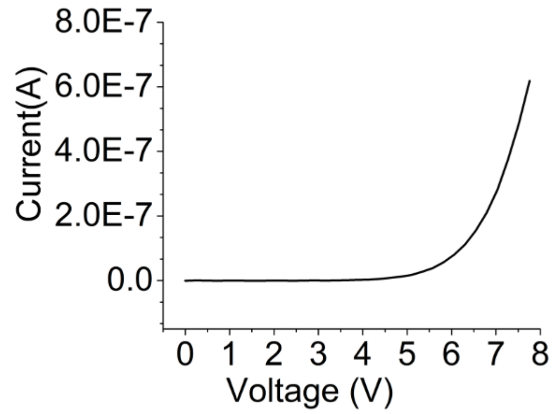
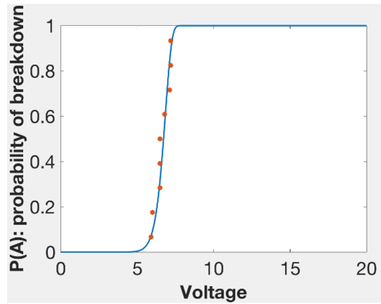
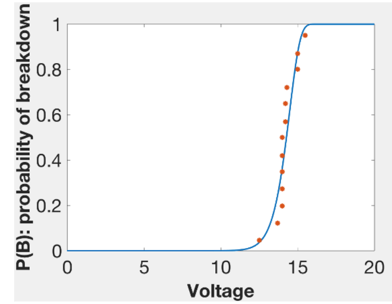


(c)

Figure 4.10: Characterization of (a) daisy chain macro, (b) ESD sensor type-A (c) type-B after application of ESD pulse.

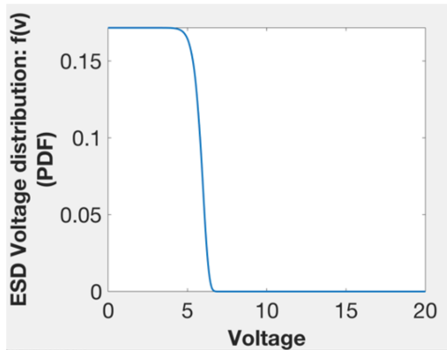


(a)

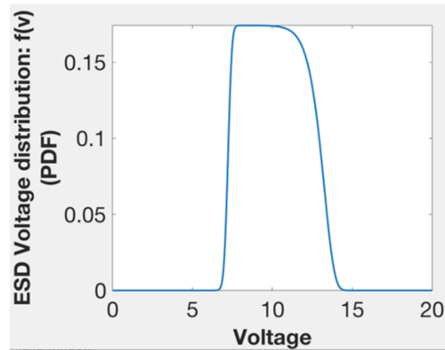


(b)

Figure 4.11: Probability of breakdown (a) sensor type-A and (b) sensor type-B. ′∗′ denotes the experimental data and the solid line denotes the Weibull curve fit.



(a)



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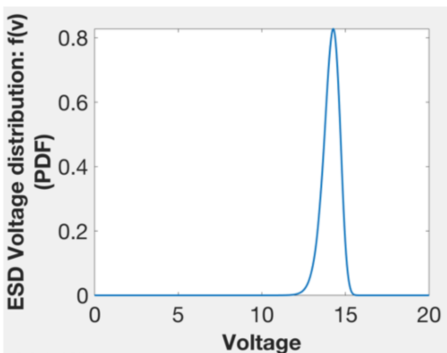

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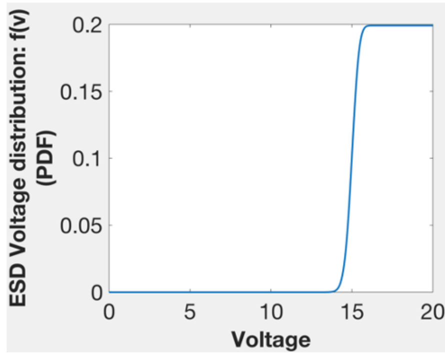
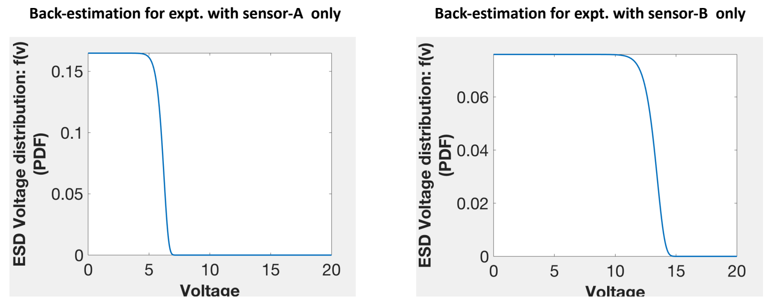
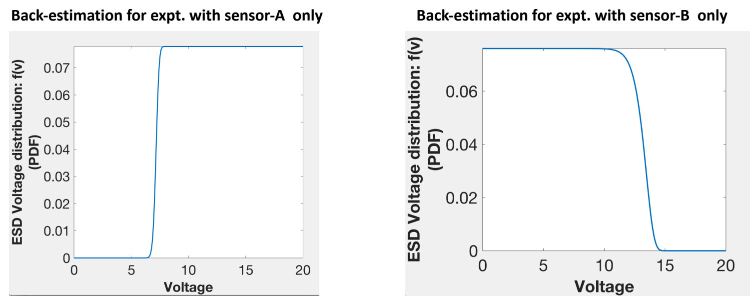


(d)

Figure 4.12: Estimation of ESD voltage using the Bayesian method (a) Case-I (b) Case-II (c) Case-III and (d) Case-IV



(a)



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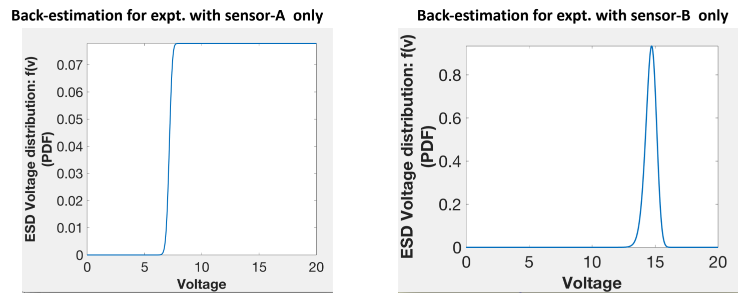

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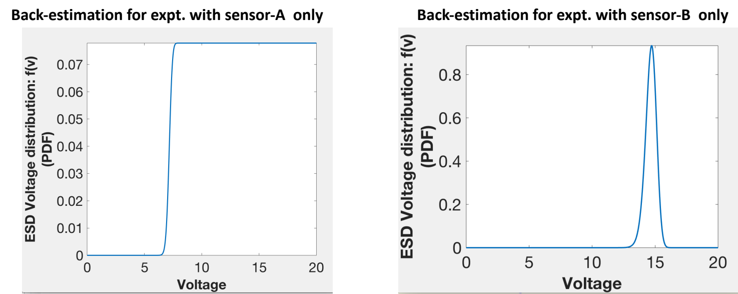


(d)

Figure 4.13: Back-estimation of ESD voltage with control samples (a) Case-I (b) Case-II (c) Case-I (d)Case-IV

4.5 Sensitivity Of ESD Sensors

A chip manufacturer would like to know how many sensors are required per chip to minimize the odds of missing an ESD event. To illustrate with an example, consider there are 4 sensors of type-A and an actual ESD voltage of 7.2 V occurred. From Fig. 4.11(a) we calculate the probability of breakdown of sensor A at 7.2 V, i.e., $P_A(V = 7.2) = 0.968$. Here we miss the ESD event if all the 4 devices did not break. Mathematically, $(1 - P_A)^4 = 10^{-6}$, or 1 out of 1 million ICs will miss the ESD event of 7.2 V or higher here. In general, if we have X devices of type-A in parallel as shown in Fig. 4.14 (x broke and x' didn't break), we miss the ESD event if all X devices do not break, i.e.,

$$(1 - P_A(V))^X = e^{-X(\frac{V}{\lambda_A})^{k_A}} \tag{4.5}$$

Figure 4.15 shows the minimum number of sensors required to be employed in an IC that ensures an ESD event greater than a certain voltage is not missed. For example, for a sensitivity of 10 parts per million (ppm) for ESD voltages greater than 7.3 V, 4 sensors of type-A would suffice. Similarly, the sensitivity graph of sensor type-B is shown in Fig. 4.16. The graphs in determining the minimum number of sensors required for achieving a required sensitivity for the manufacturer.

In case of a package with multiple dies, the worst case would be the package failing when at least one of the dies is ESD compromised. For example, consider NVIDIA A100 [63] which consists of a hierarchy of two assemblies. The package basically consists of 6 HBMs and 1 processor die as shown in Fig. 4.17. Each HBMs are in turn stack of 5 dies. Extensive screening done at the HBM die side ensures that the dies are good (Known Good Dies). Continuing with the same example of 4 sensors of type-A per die and an actual ESD voltage of 7.2 V, sensitivity per die is 10^{-6} ppm. The package sensitivity would be determined by the case in which at least one of the dies fail to detect ESD events or 1-(all the 7 dies detect ESD). Package sensitivity is $1-[(1-10^{-6})^6(1-10^{-6})^1] = 6.99\times10^{-6} = 6.99$ ppm. In general, package sensitivity to ESD is

$$1 - \{[1 - (1 - P_A(V))^X]^{N_1}[1 - (1 - P_A(V))^X]^{N_2}\}$$

where N_1 is the number of HBMs and N_2 is the number of processor dies.

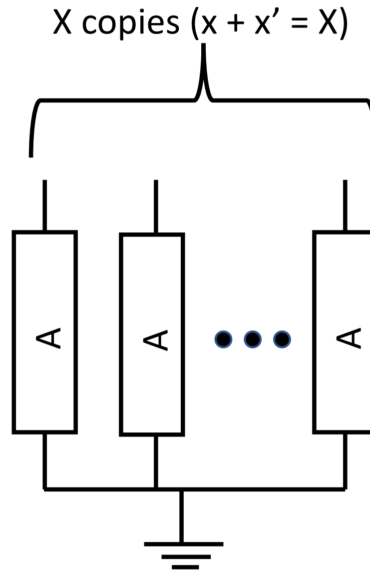


Figure 4.14: Multiple copies (X) of sensor type-A in parallel in ICs.

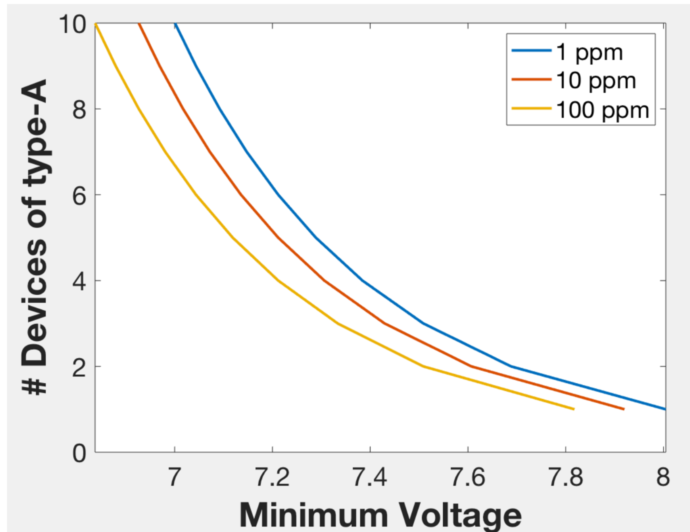


Figure 4.15: ESD sensitivity graph for sensor type-A.

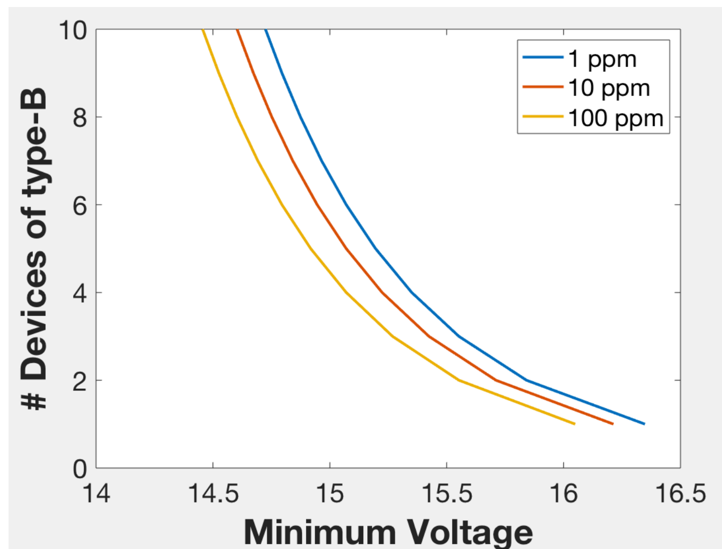
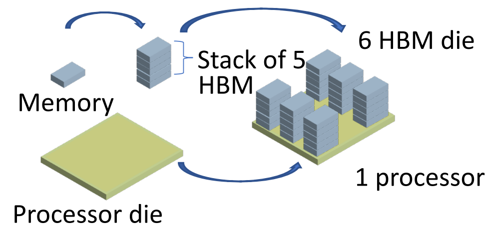
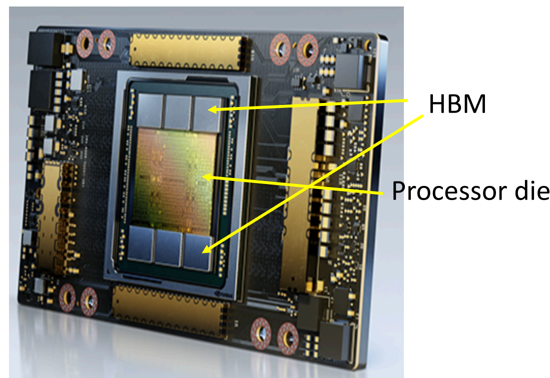


Figure 4.16: ESD sensitivity graph for sensor type-B.



(a)



(b)

Figure 4.17: NVIDIA A100 (a) Hierarchy of two assemblies (b) NVIDIA A100 package [63]

4.6 Confidence Measurement in ESD Voltage Estimation

The error in measuring the ESD voltage when an ESD event is detected, and the number of sensors required to increase precision in detecting ESD voltage are formulated in this section. To illustrate with an example, consider there are 4 sensors of type-A and an actual ESD voltage of 7.2 V occurred. There are 5 possible configurations with 4 devices, i.e. (0 broke, 4 intact), (1 broke, 3 intact), (2 broke, 2 intact), (3 broke, 1 intact), and (4 broke, 0 intact). Bayesian estimation of the ESD voltage for each of the 5 possible outcomes are shown in Fig. 4.18. From each of the graphs, we can calculate the $P(\text{ESD voltage estimate} \mid x,\ x')$ for

any $x,\ x'$ configuration. To evaluate the probability that the ESD voltage is between say, 6 and 8 V given 4 sensors, i.e., P(ESD voltage is between 6and8 V | given 4 sensors), we need to combine all the estimate from all the possible configurations. The error in voltage estimation in this case is P(ESD voltage estimate is outside 6 and 8 V | given 4 sensors). The error could also be written as $1-P$(ESD voltage is between 6 and 8 V | given 4 sensors). But note, each configuration is not equally likely and it depends on the ESD voltage. In the present example, when the actual ESD voltage is 7.2 V, the probability of each configuration $P(x, x')$ is different. $P(0,4) = 1.2917 \times 10^{-4}$; $P(1,3) = 0.0043$; $P(2,2) = 0.0544$; $P(3,1) = 0.3041$; $P(4,0) = 0.6370$. Thus, the expected probability of the ESD voltage between 6 and 8 V given we have 4 sensors is the confidence level in the voltage estimation. The error can be written as Error $= 1 - \mathbb{E}[P$(ESD voltage is between 6 and 8 V | given 4 sensors)].

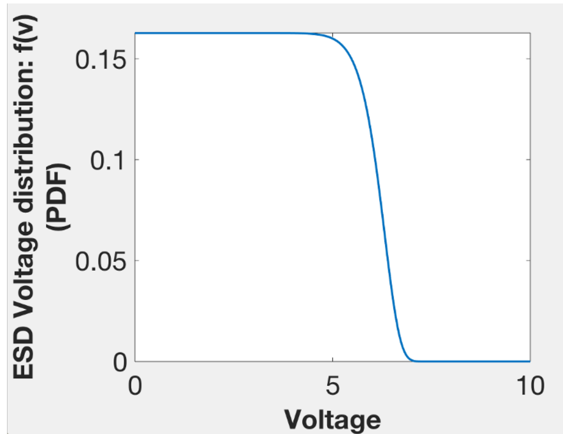
In general, the error could be stated as

$$\text{Error} = 1 - \mathbb{E}\Big[P\left(V_1 < V < V_2|X\right)\Big]$$

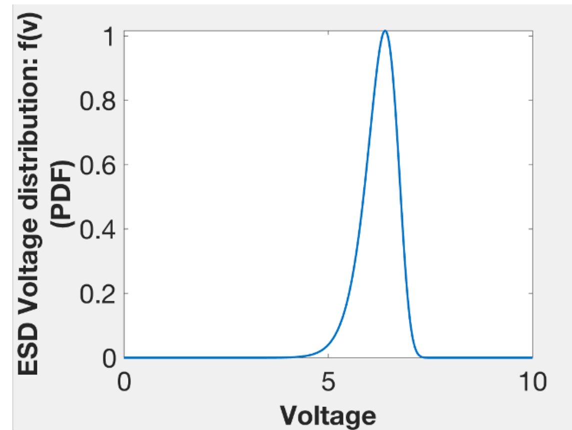
Note that here the granularity of the voltage interval ($V_1 < V < V_2$) becomes important. In addition, overall root mean square error (RMSE) without any granularity under consideration needs to be evaluated. For evaluating RMSE, the peak voltage from the Bayesian estimation is compared with the actual applied ESD voltage as indicated in Fig. 4.19. The error then could be stated as

$$\text{Error}^2 = (V_{\text{peak}} - V)^2$$
$$\text{RMSE} = \sqrt{\frac{\sum \text{Error}^2}{\text{Total observations}}}$$

First, the confidence measurement is evaluated based on Monte-Carlo simulations. Monte-Carlo simulation provides an elegant non-parametric approximate solution for statistical problems especially when a closed form solution does not exist. For example, the expected error has a closed form statistical solution which can be calculated. However, the expected RMSE does not have a simple statistical closed form solution. Similarly, one can define other



(a)



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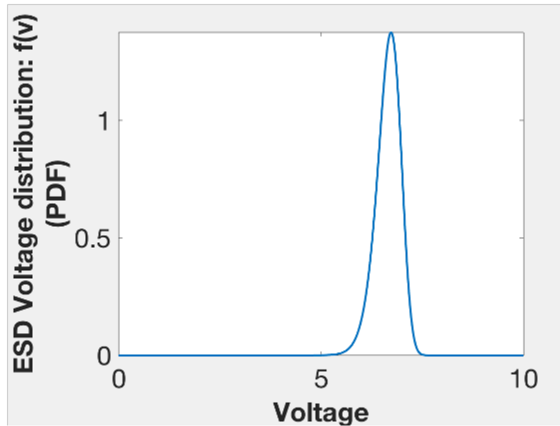

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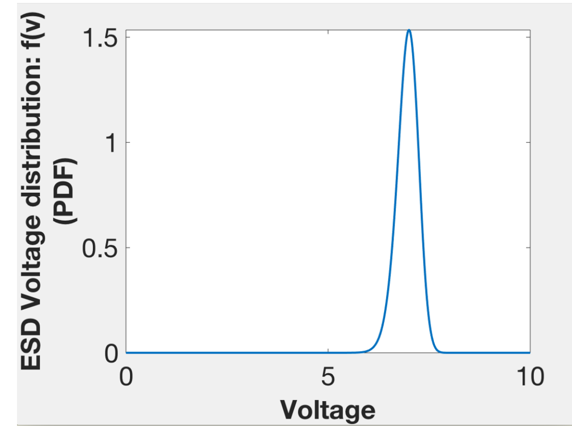

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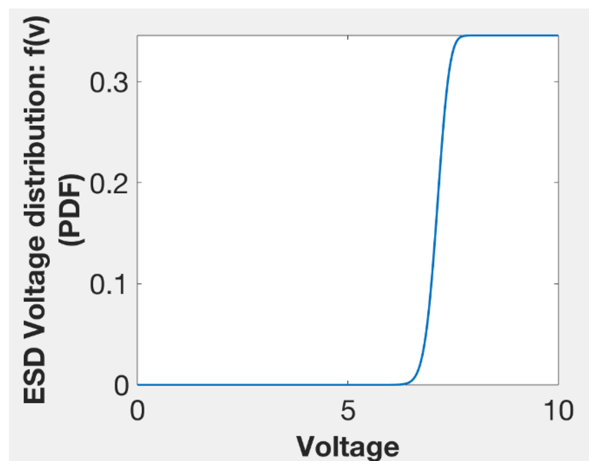


(e)

Figure 4.18: Bayesian estimation of the ESD voltage in each possible outcome for the case of 4 sensors of type-A. (a) $x = 0,\ x' = 4$, (b) $x = 1,\ x' = 3$ (c) $x = 2,\ x' = 2$, (d) $x = 3,\ x' = 1$, (e) $x = 4,\ x' = 0$

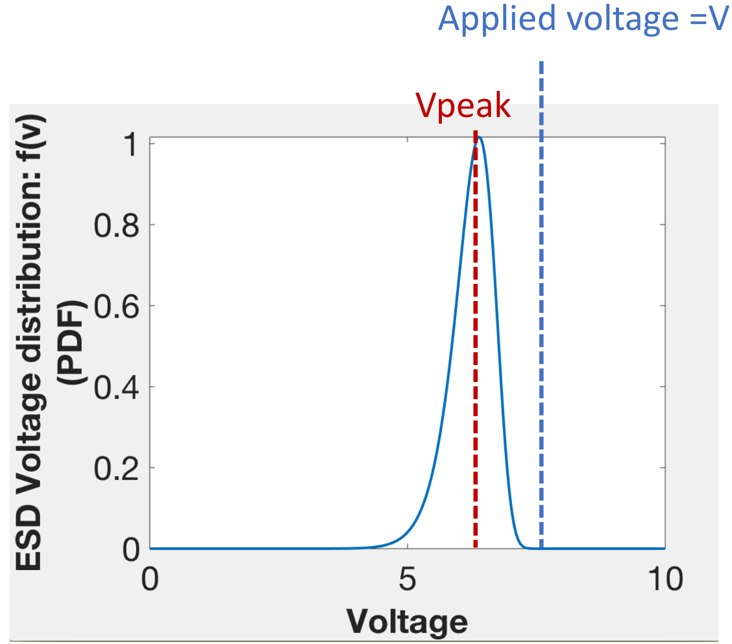


Figure 4.19: Root mean square error calculation.

measures like difference between 90 percentile and 10 percentile estimated voltage prediction as the most likelihood cutoff voltage range. These measures are non-parametric statistical measures and can only be computed via Monte Carlo approximation [63, 64]. We further show that the empirical solution computed via Monte Carlo and the theoretical closed form solution gradually converge as demonstrated in the case of expected error.

The flow chart for estimating the confidence in ESD voltage measurement is shown in Fig. 4.20. Consider there are X copies of sensor type-A, and the Monte-Carlo simulation is run for N runs. For each run $i \leq N$, a random voltage V is generated between the voltage intervals V_1 and V_2. For the generated random number V, $P_A(V)$ is evaluated. The number of broken devices is initialized to zero ($x = 0$). There are X copies of device-A in each run, and out of X devices some will break and some won't even though all are subjected to the same voltage V. A second random number β is generated (between $0 - 1$) for each copy of device-A and is compared with $P_A(V)$. If $P_A(V) \geq \beta$, that particular device

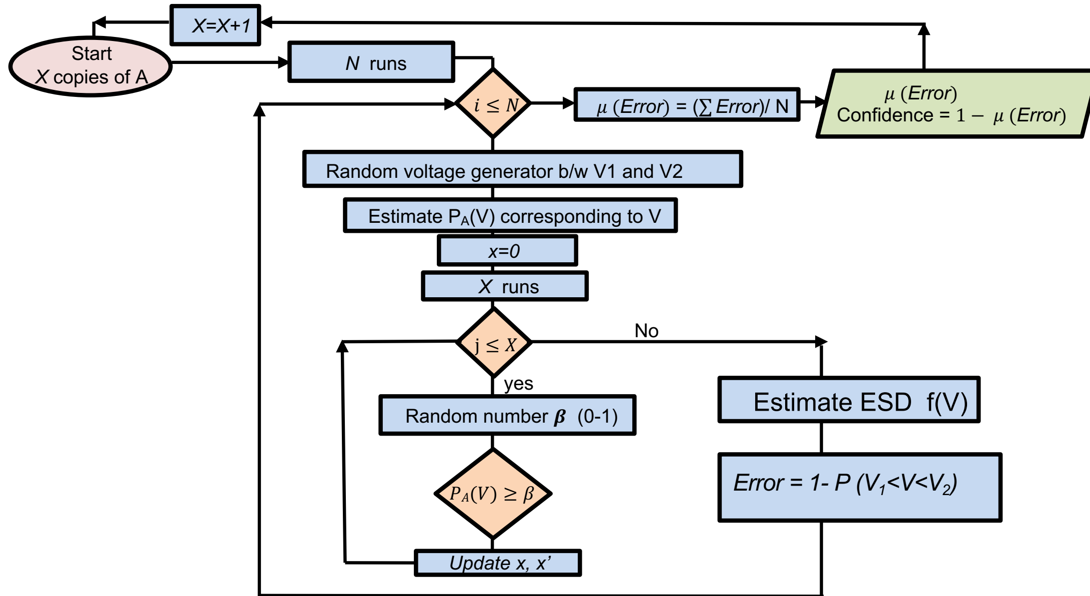


Figure 4.20: Monte-Carlo simulation for estimating confidence in ESD voltage measurement.

undergoes breakdown. At the end of first run, updated values are obtained for x and x' and Bayesian estimate $f(V)$ is obtained. From $f(V)$, the probability of voltage falling between V_1 and V_2 ie $P(V_1 < V < V_2)$ is evaluated. Error for the first run is then calculated as $1 - P(V_1 < V < V_2)$. This is repeated for N runs, at the end of which the mean error is calculated as $\mu(\text{Error}) = (1/N)\sum \text{Error}$. The confidence is $1 - \mu(\text{Error})$. If the required confidence level is not met, the number of devices is increased from X to $X + 1$, and the entire process flow is run again.

For determining the RMSE, the flow chart is presented in Fig. 4.21.

The initial part is similar to the flow chart in Fig. 4.20. After determining the ESD $f(V)$ after a run, the peak value is estimated and then compared with the generated voltage V (or the actual ESD voltage). The peak error is then calculated as $\text{peak_err} = (V_{\text{peak}} - V)^2$. At the end of N runs, RMSE is calculated as RMSE=$\sqrt{\frac{\sum \text{peak_err}}{N}}$. The experiment can then

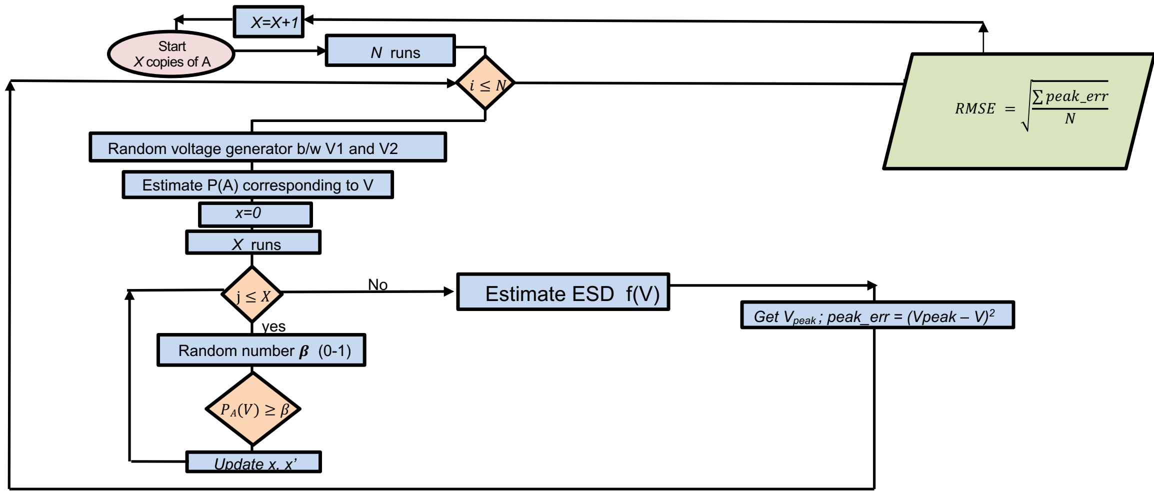
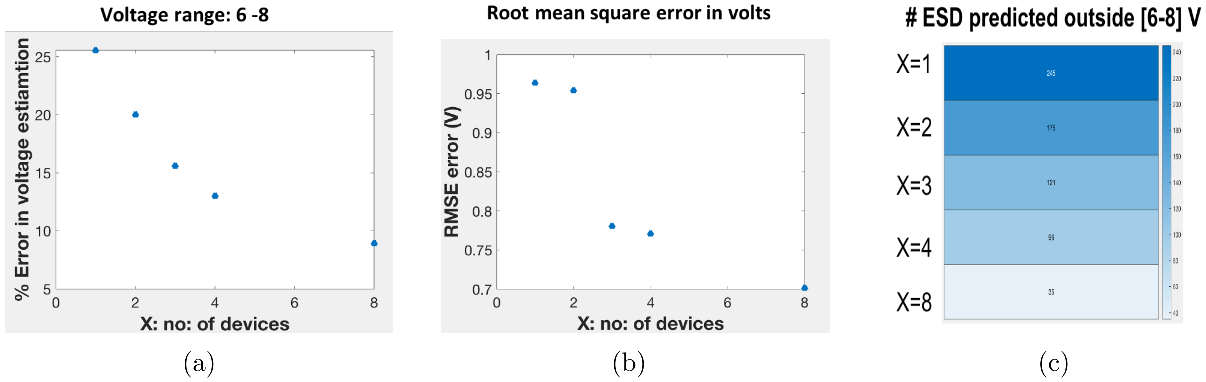


Figure 4.21: Root mean square estimation flow chart.



(a) (b) (c)

Figure 4.22: Confidence estimation from Monte-Carlo simulations (a) Percentage error in voltage estimation as a function of number of devices (b) RMSE (c) heat map showing number of cases predicted outside the voltage interval. Lighter shade means fewer predicted outside the given range.

be repeated by increasing the number of devices from X to $X + 1$.

The simulation results for the sensor type-A is shown in Fig. 4.22 for a voltage range $6 - 8\ V$. The error in voltage estimation is shown in Fig. 4.22(a). As the number of devices increases, the error in voltage estimation reduces and saturates. The RMSE is shown in

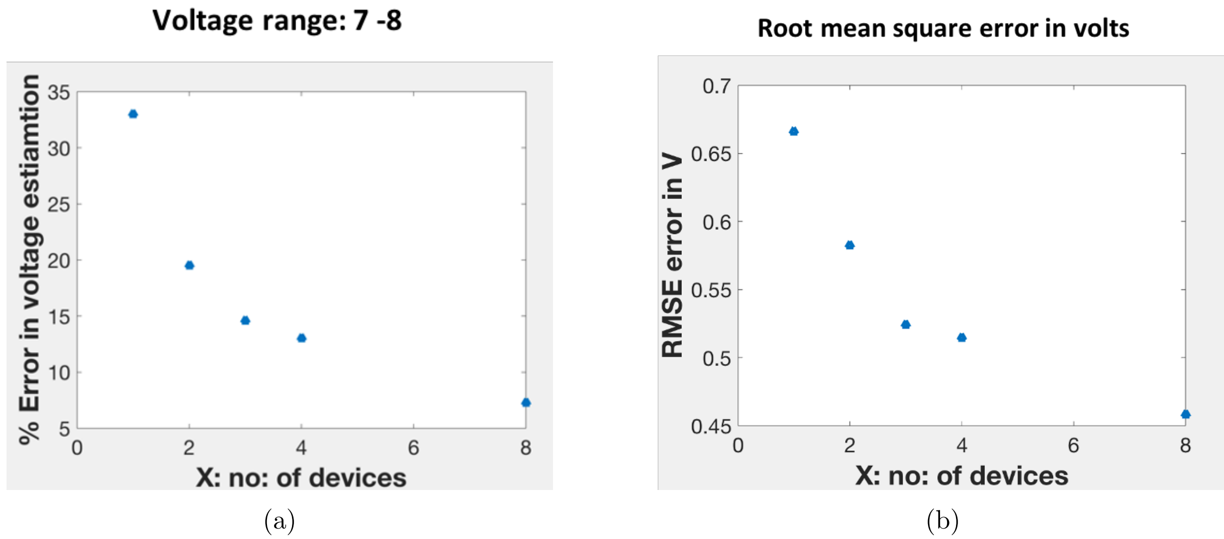
Fig. 4.22(b) and is less than 0.75 V as the device number increases. A heat map of the number of cases missed inside the voltage interval is shown in Fig. 4.22(c). As the number of devices increases from $X = 1$ to $X = 8$, the number of cases predicted outside the voltage interval reduces significantly. Simulation results for a smaller voltage interval ($7 - 8$ V) for the same sensor type-A is shown in Fig. 4.23. A similar trend is observed as in Fig. 4.22, with RMSE less than 0.5 V for 8 or more devices.

A mathematical formulation for the expectation of probability can be written as

$$
\begin{aligned}
&\mathbb{E}\Big[P(V_1 < V < V_2|X)\Big] \\
&= \sum_{x+x'=X} P(V_1 < V < V_2|x, x') \times P(x, x'|V_1 < V < V_2) \\
&= \sum_{x+x'=X} \frac{P(x, x'|V_1 < V < V_2) \times P(V_1 < V < V_2)}{P(x, x')} \times P(x, x'|V_1 < V < V_2)
\end{aligned}
$$

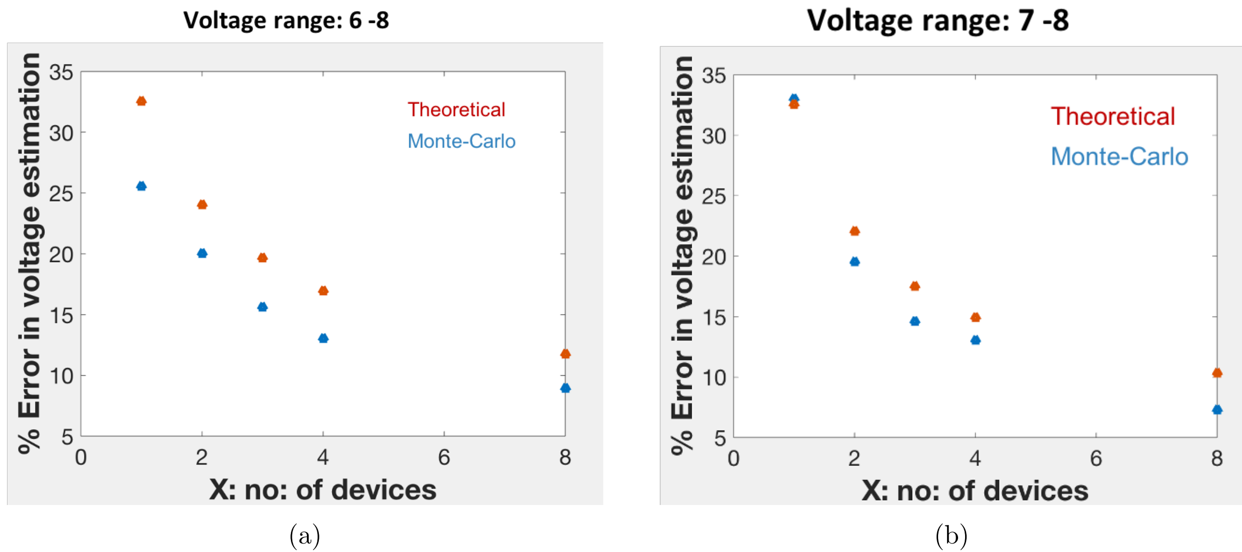
$$
\begin{aligned}
&= \sum_{x+x'=X} \frac{\int_{V_1}^{V_2} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV}{\int_0^{V_L} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV} \times P(x, x'|V_1 < V < V_2) \\
&= \sum_{x+x'=X} \frac{\int_{V_1}^{V_2} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV}{\int_0^{V_L} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV} \times \frac{P(x, x', V_1 < V < V_2)}{P(V_1 < V < V_2)} \\
&= \sum_{x+x'=X} \frac{\int_{V_1}^{V_2} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV}{P(V_1 < V < V_2)} \times \frac{P(x, x', V_1 < V < V_2)}{\int_0^{V_L} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV} \\
&= \sum_{x+x'=X} \frac{\int_{V_1}^{V_2} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV}{P(V_1 < V < V_2)} \times \frac{\int_{V_1}^{V_2} P(x, x'|V) \times f(V) dV}{\int_0^{V_L} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV} \\
&= \sum_{x+x'=X} \frac{\Big[\int_{V_1}^{V_2} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV\Big]^2}{\int_{V_1}^{V_2} f(V) dV \int_0^{V_L} \binom{X}{x} (P_A(V))^x (1 - P_A(V))^{X-x} f(V) dV}
\end{aligned}
$$

Comparison of the mathematical formulation and Monte-Carlo simulation is shown in Fig. 4.24(a) for the voltage interval [$6-8$ V] and Fig. 4.24(b) for the voltage interval [$7-8$ V]. A good agreement with the Monte-Carlo simulation is observed.



(a) (b)

Figure 4.23: Confidence estimation from Monte-Carlo simulations for a smaller voltage interval (a) Percentage error in voltage estimation as a function of number of devices, (b) RMSE plot.



(a) (b)

Figure 4.24: Comparison between Monte-Carlo simulation and Mathematical formulation (a) for the voltage range $6 - 8\ V$, (b) Voltage range $7 - 8\ V$

4.7 Conclusions

In using the sensors for the estimation of ESD voltage, two random events are encountered. The breakdown of sensors of the same type is random even though all are subjected to the same voltage in each run/experiment. The ESD voltage subjected to the sensors in multiple runs is also a random variable. A Bayesian method was developed for the estimation of ESD voltage using the observed evidence from the sensors after each run. ESD testing of the sensors was carried out at high voltages using an ESD gun and at low voltages using a modified test setup. The estimated ESD voltage from the observed number of broken-down sensors closely matches the actual ESD voltage. Mathematical formulation for sensitivity and confidence in ESD voltage estimation was developed and shows good agreement with Monte-Carlo simulations.

Chapter 5

Conclusion

5.1 Summary

ESD results in significant device failures at all stages of IC production, test, assembly, and field usage. The losses in the semiconductor industry due to ESD are estimated to be several billion dollars per year. Even though most modern ICs have on-chip ESD protection circuitry, static charge accumulation during transport and handling may exceed the limits of the protection circuitry and may cause damage to the ICs. Most importantly, any advanced packaging schemes existing today are not amenable to rework if one or multiple dielets are ESD compromised, resulting in the loss of an entire high value module.

In this dissertation, a study was completed to examine the susceptibility of ESD on an advanced packaging scheme called Silicon Interconnect Fabric (Si-IF) in Chapter 2. MOSCAPs were used as test vehicles to examine the effect of ESD on the integrity of dielet assembly on the Si-IF. The assembly process was found to be robust to ESD failures.

In Chapter 3, two schemes for on-chip ESD monitoring (a variable dielectric width capacitor, and a vertical MOSCAP array) suitable for any die using ground rules within that technology was proposed. An on-chip ESD sensor would be useful to ensure that dielets are ESD safe prior to the assembly process in any advanced packaging schemes. Both ap-

proaches were simulated, fabricated, and experimentally characterized in GlobalFoundries 22 *nm* FDSOI process technology.

A Bayesian method formulation for ESD voltage estimation was developed in Chapter 4, and validated with experimental results. Sensitivity of the ESD sensors when employed in ICs was also evaluated. Mathematical formulation of expected probability aids deterministic and precise estimation of sensor voltage, which was further matched with Monte-carlo simulations.

5.2 Outlook

In this dissertation, a passive on-chip ESD sensor scheme that can be employed on any die is demonstrated. A method for estimating the ESD voltage was formulated and validated with experimental results. In addition, a novel high power delivery architecture for wafer scale systems is proposed and experimental results with prototype boards are presented in Appendix A. Major directions for the future are suggested below:

1. Typical ESD protection mechanisms impacts the performance of ICs significantly. Novel ESD protection mechanisms with negligible parasitic capacitance is certainly a promising future research direction.

2. An active on-chip ESD sensor that can record and store ESD events, enabling multiple usage, is suggested for future research.

Appendix A

High-power delivery architecture for Si-IF

A.1 Introduction

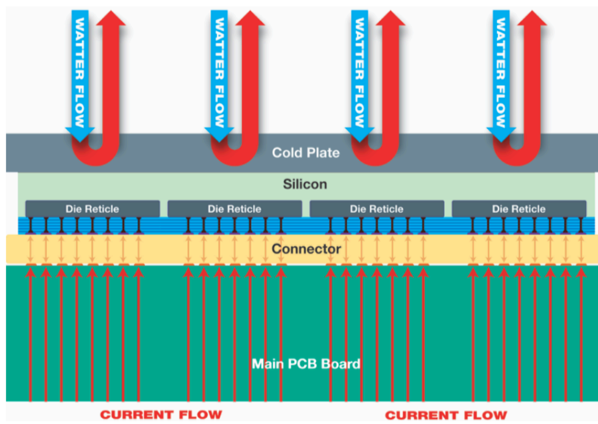
Modern applications require integration of several key functionalities in a single system. Ever-growing data-bandwidth requirements are pushing the boundaries of the traditional PCB-based integration schemes and necessitate novel system architecture and integration schemes [65]. A high compute AI and data analytic system like the NVDIA DGX-100 (Fig. A.1(a)) takes about a total power of 6.5 kW and performs about 5 quadrillion (10^{15}) floating-point operations per second (FLOPS). The physical size of the systems [66] is about 6 rack units (RU), which translates to 26.4 cm $\times$ 48.2 cm $\times$ 89.7 cm (H $\times$ W $\times$ L). The SuperBlade SBE-820H [67] multi-node server (Fig. A.1(b)) used in enterprise cloud and high performance computing (HPC) applications takes up to 17.6 kW power and is 8 RU in size (35.56 cm $\times$ 44.7 cm $\times$ 81.2 cm). The Cerebras CS-2 for AI and data learning uses wafer scale processors in which homogeneous chips communicate on a silicon wafer. This enables them to have power per unit area slightly lower compared to multi chip modules that communicates through package, transceivers, etc. Their sandwich of silicon wafer, the custom connector,

PCB, and cold plate (Fig. A.1(c)) enables them to keep the wafer temperature comfortable for the electronics [68]. The CS-2 [69] offers 1.2 Tb/s system I/O, takes about 23 kW of power (Fig. A.1(d)), and is about 15 RU (66 cm tall).

Fine pitch integration in the Si-IF enables high packing density of dielets, with high power density (up to 1 Wmm^{-2}) across the entire fabric, and similarly requires high heat flux removal. These requirements can vary significantly based on the needs of the heterogeneous components present on the Si-IF, with an estimated total power delivery of $40-60$ kW for a 300 mm diameter Si-IF. Peripheral power delivery becomes inefficient for large wafer scale systems due to the increased I^2R losses, and voltage drop across the power delivery network (PDN). In addition, placing multiple power components across the wafer makes it area inefficient. A novel segmented power delivery network (PDN) is required and is discussed with a targeted power delivery of $40-60kW$ to a 300 mm diameter Si-IF. The thermal management part for the PDN is covered in detail by U. Shah *et al.*[70]

(a)

(b)



(c)

(d)

Figure A.1: (a) Nvidia DGX A100 [66] (b) SuperBlade SBE-820H [67] (c) Cerebras wafer-scale-processors [68] (d) Front view of CS-2 with power supplies and I/O in the top left provide power and data [69]

A.2 Power delivery network in Si-IF

Current high-power systems-on-chip have power densities of 0.5 W/mm^2, with future power loads expected to exceed 1 W/mm^2 [71]. Integration of such power-hungry systems on a 300 mm diameter Si-IF would require power delivery and heat extraction of up to 50 kW. The proposed architecture (Fig. A.2, Fig. A.3, and Fig. A.4) here involves power delivery starting from the power board with DC-DC converters. A high voltage DC input supply (50 kW, 48 V input for 40 kW power delivery to the wafer) goes into these power boards. Multiple power boards are vertically stacked and connected to a common PCB for granular routing to the silicon wafer. This PCB, called power platform PCB, is segmented, embedded in PDMS, a flexible molding compound, and interconnected using the FlexTrate process [40]. Multi-strand power cables from the power board are solder-connected to the power platform PCB. Here, FlexTrate acts as a stress buffer layer for CTE mismatches between the silicon wafer, power platform PCB, and power cable connections from the power board. The electrical connection goes through the power board, segmented power platform PCBs embedded in PDMS, BGA connections from the power platform PCBs to the Si-IF, through-wafer vias (TWVs) in the Si-IF, and decoupling capacitors within the Si- IF, and terminates on the dies mounted on top of the Si-IF.

The input voltage to the system is 50 kW, 48 V DC supply. The estimated power loss is about 6 kW in the power boards, about 2 kW as I^2R losses, resulting in about 42 kW of power available to the dielets on the Si-IF. The block diagram for the power delivery is shown in Fig. A.4. The system input can come from a $3-$phase supply, which is connected to a high voltage DC power supply. The programmable DC power supply can deliver 50 KW of power at 48 V DC. 48 V DC is used as the primary bus voltage to reduce the power distribution losses and to enable use of smaller wire gauges due to the reduced current levels. But this approach necessitates DC-DC converters (for down converting the 48 V DC to the required operational voltage of about ~ 1 V) in the PDN. Isolated point-of-load converters are used for the DC-DC conversion. The power delivery network also contains decoupling caps in the

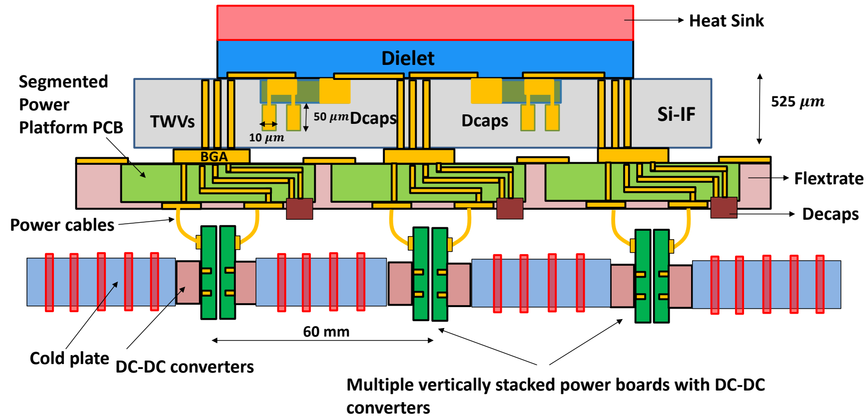


Figure A.2: Cross-sectional view of PDN.

power board, segmented PCBs and in Si-IF (deep trench capacitors) to extend the frequency range of operation.

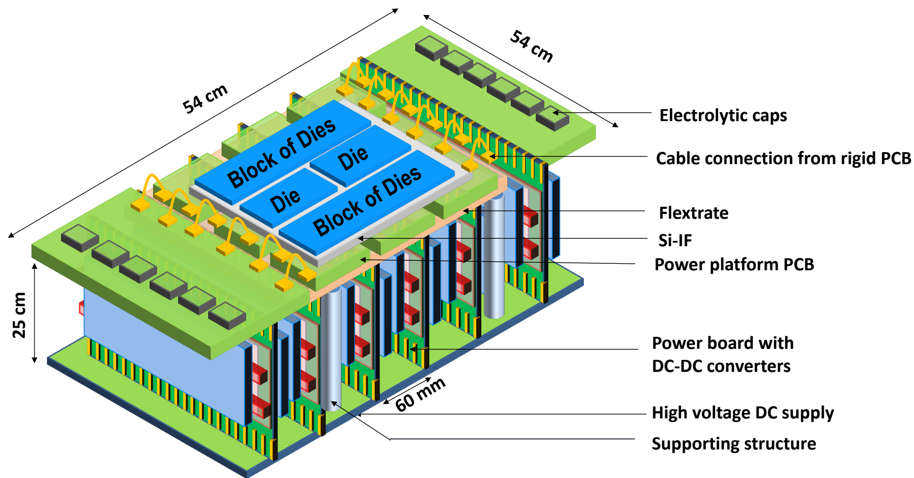


Figure A.3: 3-D view of PDN.

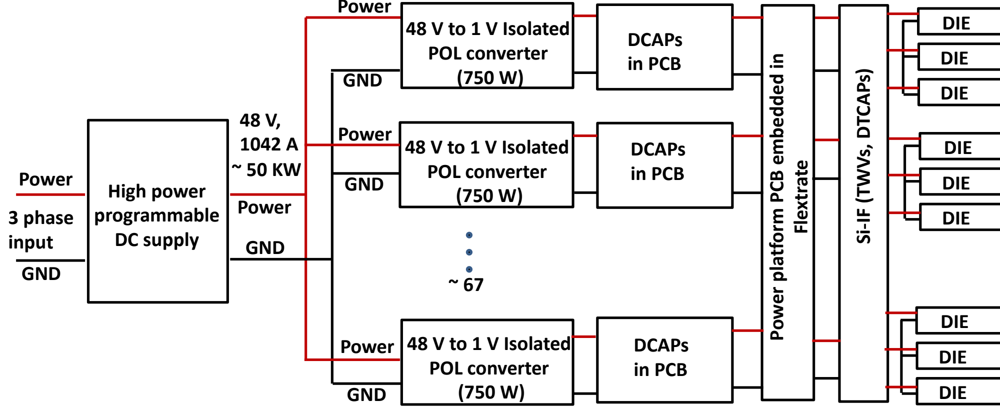


Figure A.4: Block diagram of the power delivery network .

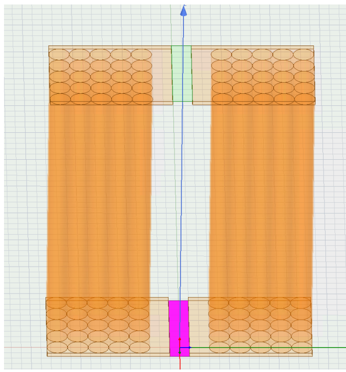
A.2.1 PDN modeling and simulations

A 300 mm silicon wafer with 90% area utilization would give us an effective area of 63600 mm^2 (equivalent square of side 252 mm). The total number of BGAs (assuming a diameter of 0.5 mm and pitch 1 mm) possible would be $\frac{252\ mm}{1\ mm} * \frac{252\ mm}{1\ mm} = 63504$. The number of BGAs used for the current return path (GND BGAs) would be $\frac{63504}{2} = 31,752$. Assuming 5 TWVs (100 μm diameter, 200 μm pitch) per BGA contact, the total number of TWVs is $63504 * 5 = 317,520$. The number of GND TWVs would be $\frac{317520}{2} = 158,760$. Assuming a total current delivery of 40 kA to the wafer, current per BGA would be $\frac{40,000}{31,752} = 1.26\ A$, with current density $\frac{1.26\ A}{\pi * 0.255\ mm * 0.25\ mm} = 6.4\ \frac{A}{mm^2}$. As the number of TWVs per BGA is 5, the current per TWV would be $\frac{1.26\ A}{5} = 0.252\ A$, and current density $\frac{0.252\ A}{\pi * 50\ \mu m * 50\ \mu m} = 32\ \frac{A}{mm^2}$, within the maximum current density capability of copper [72]. TWVs (100 μm diameter, 200μm pitch) in Si-IF have been demonstrated by M. H. Lin *et al.*[73]. The extracted inductance and resistance of the BGAs and TWVs are shown in Table A.1.

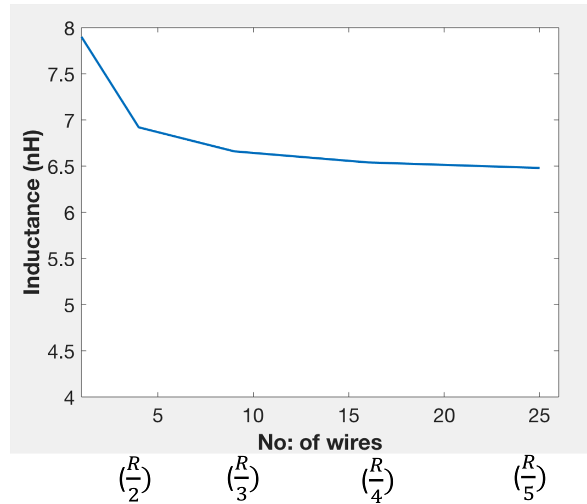
Multi-strand cables are used to carry current from the power board to the compliant power platform PCBs. Inductance extraction using ANSYS HFSS for AWG-4 wire (radius

Table A.1: R and L contribution per pair of a BGA contact (each BGA has 5 TWVs)

Component	Inductance	Resistance
BGA (0.5 mm ϕ, 1 mm pitch, 300 μm thick)	95.8 pH	2.6 $m\Omega$
TWV (100 μm ϕ, 200 μm pitch, 500 μm thick, 5 TWVs per BGA)	93.6 pH	0.64 $m\Omega$



(a)



(b)

Figure A.5: (a) ANSYS HFSS model of multi-strand wire (b) Extracted inductance with number of wire strands. As the number of wires with lower radius increases, the overall cross-sectional area is kept constant.

= 2.5947 mm, spacing of 3mm and length 15 mm) is shown in Fig. A.5.

The resistance contribution for the pair of AWG-4 wires including the solder contact resistances is $\sim 2.628 * 10^{-4}\ \Omega$

A lumped circuit model (Fig. A.6) with extracted inductance, resistance, decoupling capacitors at different stages was developed to estimate the impedance. For a die size of

25 mm^2 with a power density of 1 W/mm^2, a supply voltage of 1 V, a load current of 25 A, and with 10% ripple, the target impedance [74] is given by

$$Z_0 = \frac{V_{DD} * ripple}{I} = \frac{1 * 0.10}{25} = 4\ m\Omega \quad \text{(A.1)}$$

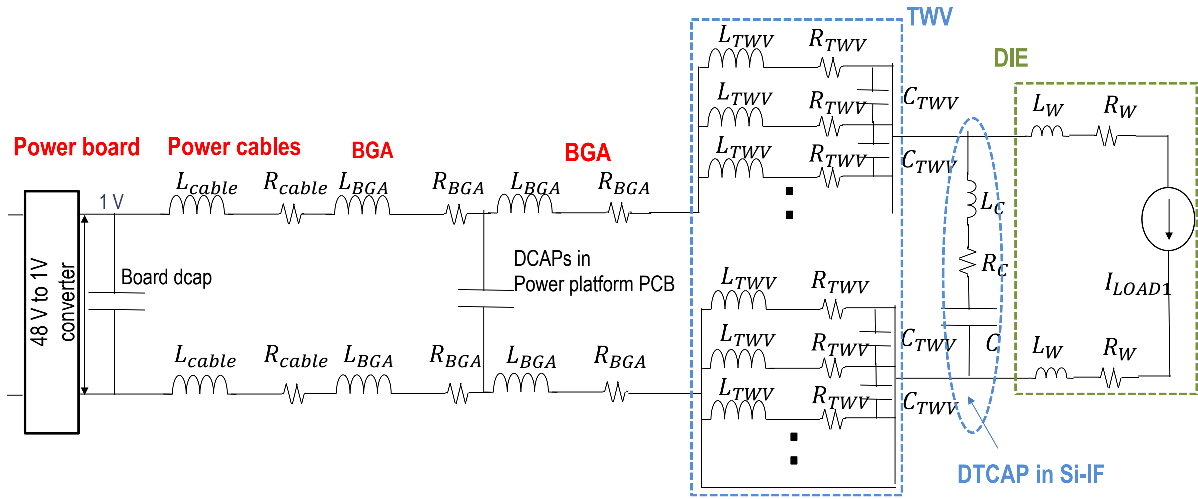


Figure A.6: Circuit model of PDN.

Decoupling capacitors are placed at various stages of the PDN (board decoupling capacitors, capacitors in the power platform PCB, and deep trench capacitors (DTCAPs) in Si-IF) to effectively decouple the high impedance part of the PDN from the load at high frequencies. The required cap value that satisfies the target impedance requirement is given by

$$C \geq \frac{L_1}{Z_0 * (R_1 + R_C)}, \quad \text{(A.2)}$$

where L_1 and R_1 are the upstream (towards the source side) inductance and resistance respectively of the PDN from the point of insertion of the decoupling cap, and R_C is the ESR of the decoupling capacitor. While inserting the decoupling caps, the impedance at the

resonant peak [74] given by

$$Z_{peak} = Q_{tank}\sqrt{\frac{L_1}{C}} = \frac{1}{R_1 + R_C} * \frac{L_1}{C}, \tag{A.3}$$

The resonant peak impedance Z_{peak} is to be less than the target impedance Z_0. The impedance spectrum corresponding to a sample die size of 5 mm $*$ 5 mm = 25 mm^2 is shown in Fig. A.7. The voltage drop across the PDN at any frequency can be estimated from the impedance spectrum graph. From the impedance spectrum graph, the output voltage from the power board supply needs to be $1 - 1.1$ V, which takes into account 100 mV peak-peak ripple of the DC-DC converter.

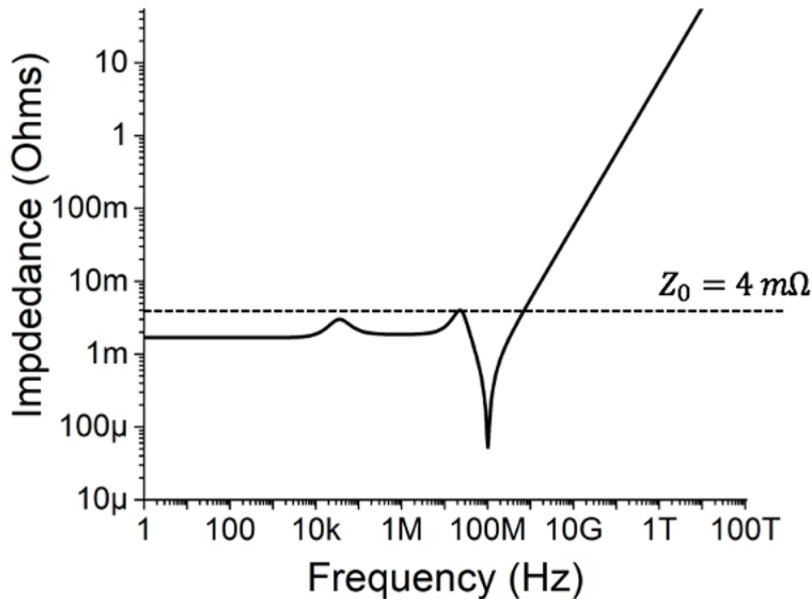


Figure A.7: Impedance spectrum of PDN.

A.3 Construction of power boards

Power boards down-convert the high voltage DC of 48 V to 1 V. Each power board has multiple DC-DC converters, and several of these power boards are vertically stacked Fig. A.3.

Commercial off the shelf (COTS) components are used in the power board. Various components used in the power board include DC-DC converters (realized using voltage regulators and current multipliers), fuses, EMI filters, decoupling capacitors, and multi-strand power cables. A factorized power architecture [75] with separation of regulation, isolation, and voltage transformation is employed here. The major components (Fig. A.8) include small, efficient building blocks called the pre-regulator module (PRM) and voltage transformation module (VTM). The PRM and downstream VTM current multiplier minimize distribution and conversion losses and provide an isolated, regulated output voltage. The advantages include lower physical area and volume space of power converters, and reduced distribution losses.

A PRM from VICOR corporation (PRM48AF480T400A00) is used [76], which is a non-isolated, zero voltage switching (ZVS) buck-boost topology with a fixed high frequency switching ($1.35\ MHz$) and covers a wide input range ($36 - 75\ V$) giving a regulated output of $48\ V$. The VTM from VICOR (VTM48EF015T115A00) [77] is an isolated ZVS and zero current switching (ZCS) IC that employs a Sine amplitude converter topology (SAC) [78], with a fixed high frequency switching ($> 1\ MHz$). It is a fixed ratio converter ($V_{OUT} = V_{IN} * K$), with the input being driven by the PRM. The input voltage range is $26 - 55\ V$ and output $0.7 - 1.4\ V$, with an output current of about $100\ A$.

EMI filters are used to filter the switching frequency harmonics of the PRMs coupling into the DC source, as well as VTM switching frequency harmonics coupling into the PRM. A simplified series damped filter topology [79] is used here, as shown in Fig. A.9. The output impedance of the EMI filter is designed to be sufficiently smaller than the input impedance of the converter for system stability [79]. In addition, the transfer function of the EMI filter gives adequate attenuation ($\sim 40\ dB$) at the switching frequency ($\sim 1\ MHz$), ensuring minimal coupling.

There are two modes of operation with PRMs and VTMs: adaptive loop and remote sense [76, 77]. The adaptive loop mode of operation is shown in Fig. A.8. Here an internal regulatory mechanism within the PRM regulates the output voltage without the need for

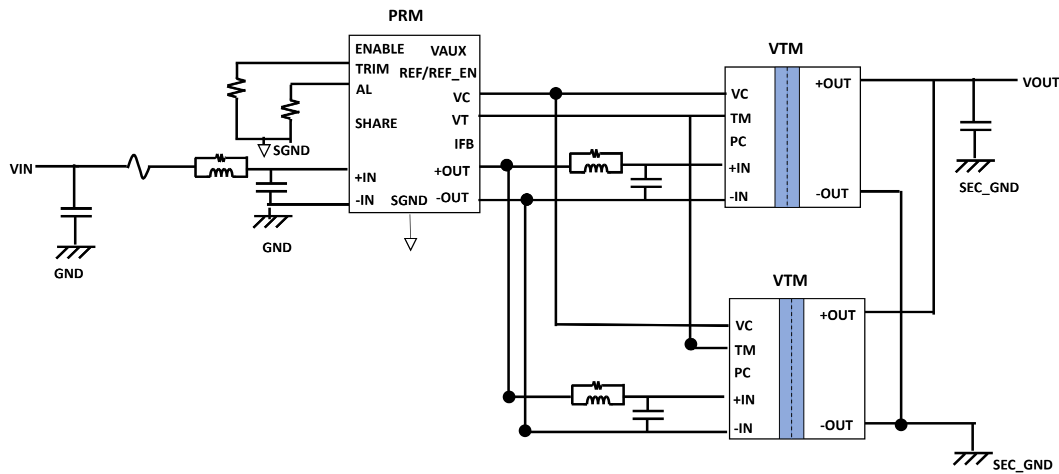
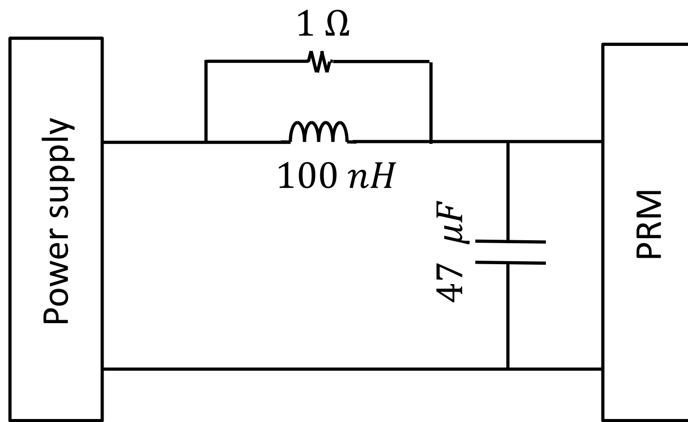


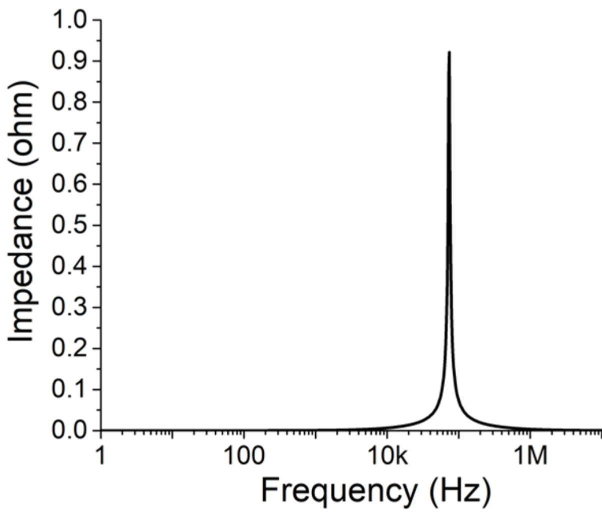
Figure A.8: Circuit schematic of PRM driving 2 VTMs in power board.

voltage feedback [76]. The configuration is nominally set to provide a fixed 48.0 V output at PRM and the TRIM pin of the PRM can be used to adjust the output from $20-55$ V. The PRM output goes as the input to the VTM and a scaled output appears at the VTM. In remote sense mode of operation (Fig. A.10), the internal regulation mechanism is disabled, and voltage regulation is achieved through an external control loop and current sensors. These typically include a precision voltage reference, an operational amplifier for closed loop feedback compensation, and a current sense IC for monitoring the current from the PRMs [76].

Design of a single power board is shown in Fig. A.11. Each power board delivers about 6 kW, and in total about 9 power boards would be required. A single power board here refers to two subunits of vertical PCBs separated by a small gap of ~ 2 mm. Each PCB has 16 columns, numbered $n = 1$ to $n = 16$ as shown in Fig. A.11. The two VTMS and one PRM in a single column can give a maximum of about 200 W, and 16 such columns can give 3.2 kW. Similarly, the backside subunit PCB can also give about 3.2 kW. The input to the power board can be connected through board connectors/copper lugs. The input power goes through a current fuse and EMI filter, and connects to the PRM. Resistors are used for



(a)



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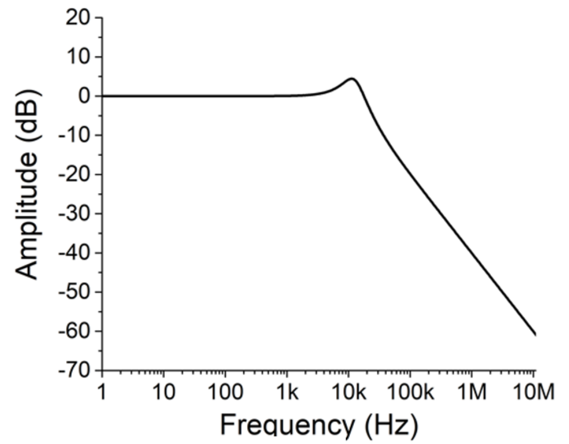

(c)

Figure A.9: EMI filter between power source and VTM (a) Simplified series damped filter topology (b) Output impedance of the EMI filter (c) Transfer function of the EMI filter.

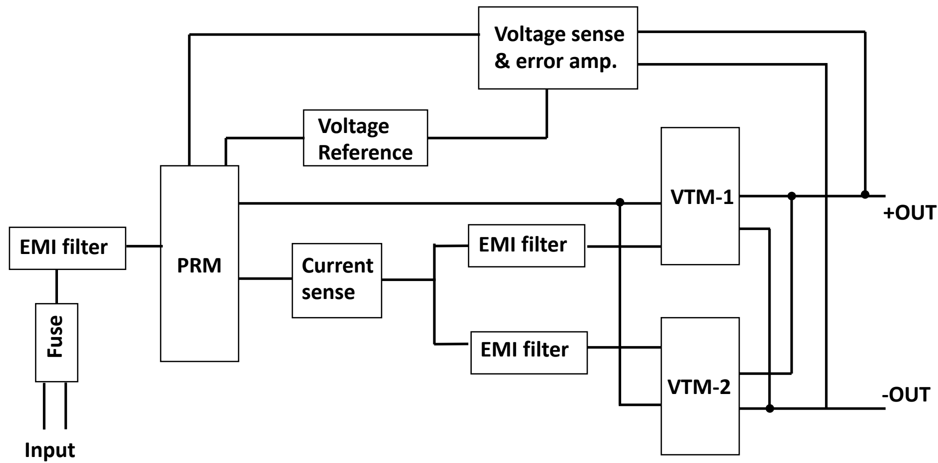

Figure A.10: Remote sense mode of operation with PRM and VTMs.

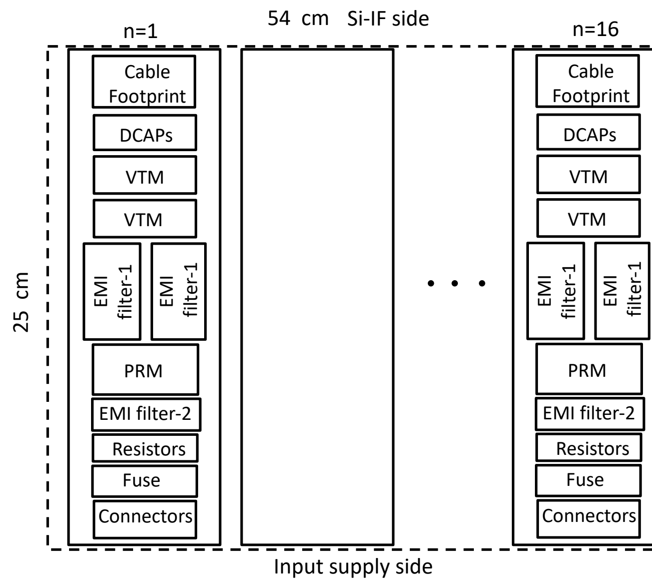

Figure A.11: Footprint of the power board.

tuning the output voltage and for internal feedback regulation. One PRM drives two VTMs (each can deliver a current of about 100 A at 1 V). EMI filters are inserted between VTMs and the PRM as well for suppressing switching frequency harmonics of a VTM coupling into

a PRM. Output capacitors are placed at the VTM outputs, compensating the inductance of the output power and ground planes from the VTMs. The output current is taken through AWG cables connected to copper lugs at the end.

A.4 Experimental results for prototype boards

PRM and VTM test evaluation boards [80, 81] from VICOR were procured and set up (Fig. A.12) for a $\sim 100\ W$ design (half a column in the power board), along with other discrete components. The two boards are connected together using board connectors, and variable 300 W, 100 $m\Omega$ resistors are used as the load. The power board prototype is tested with an input system voltage of 48 V. Both adaptive mode (internal regulation) and remote sense (external feedback and control) mode of operation were tested and verified for various load conditions, including no load connection and over-load conditions.

Figure A.12: Prototype power board ($\sim 100\ W$) testing with PRMs and VTMs.

Output voltage from the VTM along with the ripple content is shown in Fig. A.13 for a 9 $m\Omega$ load, corresponding to a load current of $\sim 111\ A$. The output voltage is 1.004 V, with a ripple magnitude of 34 mV (peak to peak) at 1.42 MHz. Other load conditions are summarized in Table A.2. The power boards operate at an efficiency of about 88% across different load conditions in down converting the 48 V DC to 1 V DC.

Figure A.13: Output voltage at the VTM for a 9 milli-ohm load along with the ripple content.

Table A.2: Prototype results of power board

Input/Output specs	Load $9\ milli-ohms$	$13\ milli-ohms$	No Load
Input Voltage	48 V	48 V	48 V
Input current drawn	2.642 A	1.815 A	0.75 A
Input power	126.816 W	87.12 W	3.6 W
Output voltage	1.004 V	0.999 V	1.001 V
Load current	111.1 A	76.2 A	-
Ripple	34 mV (pp)	34 mV (pp)	23 mV (pp)
Ripple frequency	1.42 MHz	1.41 MHz	1.42 MHz
Efficiency	88%	87.4%	-

The output current from the power boards is connected to the compliant power platform with segmented PCBs in FlexTrate as in Fig. A.14. Granular routing to the dies on wafer is done through the power platform PCB. The estimated size of each power platform PCB is about 3 $cm \times 3$ cm, with decoupling caps and AWG wires (from the power board) placed at the back side. The front side of the compliant power platform PCB is attached to the silicon wafer through BGAs. Each column in the power board (~ 200 A at 1 V) gets connected to a single segmented power platform PCB. Current from the power boards outside the shadow of the wafer is delivered through cables attached to the segmented PCBs at the wafer periphery, as shown in the 3-D view (A.3). The power and ground planes in different segmented PCBs are connected to each other through copper wires on FlexTrate. Each power platform PCB has VDD and GND pads on all the four sides for enabling copper wire connections from adjacent PCBs as shown in Fig. A.14. The design is also compatible with multi-VDD power delivery. Prototype design of the compliant power platform is currently a work in progress.

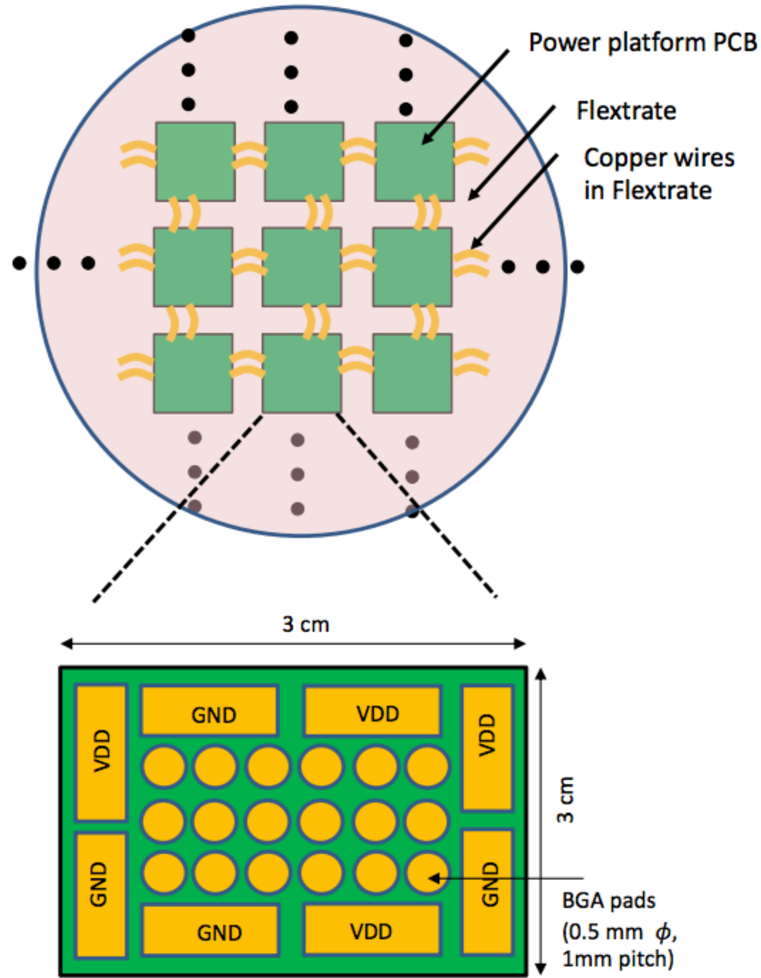

Figure A.14: Power platform PCB embedded in Flextrate.

A.5 Conclusions and Future work

A novel high-power delivery network for the Si-IF technology is described. A $50-kW$ input power goes into the system and about 42 kW is being delivered to the dielets on the silicon wafer after accounting for various losses in the network. PDN specifications and simulations

have been carried out to determine the output voltage to be delivered from the power board. Design and experimental testing with evaluation boards were performed, validating the power board design. Major directions for the future are suggested below:

1. Prototype experimental results for power boards in the Si-IF PDN was presented. Compliant power platform PCB enables granular routing to the dies on wafer. Design and assembly of the compliant power platform PCB to the silicon wafer is currently a work in progress.

2. Integration of passive components such as capacitors in the Si-IF will enhance the performance by reducing the total foot print as compared to assembling surface-mount capacitors in Si-IF. Deep trench capacitors (DTCAPs) in Si-IF present a promising alternative. DTCAPs with high specific cap density greater than 100 $fF/\mu m^2$, low effective series resistance ($\leq 1\ m\Omega$), break down voltage greater than typical operating voltage, and process flow compatible for integration in Si-IF is suggested.

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