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Journal

IEEE Transactions on Power Electronics, 39(7)

ISSN

0885-8993 1941-0107

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Publication Date

2024-02-28

DOI

10.1109/TPEL.2024.3370166

Peer reviewed

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The Switching Bus Converter: A High-Performance 48-V-to-1-V Architecture with Increased Switched-Capacitor Conversion Ratio

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***Abstract*—This paper proposes a switching bus converter, an efficient and compact hybrid switched-capacitor (SC) voltage regulator, for direct 48 V to Point-of-Load (PoL) power conversion in data centers. The proposed topology merges a 2-to-1 SC front-end with two 8-branch series-capacitor-buck (SCB) modules through two switching buses. Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. In addition, this paper conducts a comparative performance analysis of different regulated hybrid SC topologies, which reveals that a larger SC conversion ratio is advantageous for achieving higher performance. Through the two-phase operation of the SCB modules, the proposed topology extends the maximum duty ratio and enables a larger SC conversion ratio. A hardware prototype was designed and built with custom two-phase coupled inductors and synchronous bootstrap daughterboards to validate the theoretical potential of the proposed topology. The hardware prototype was tested up to 500-A output current at 1-V output voltage, achieving 93.4% peak system efficiency, 86.1% full-load system efficiency, and 464-W/in^3 power density. Moreover, the theoretical benefits of a larger SC conversion ratio were experimentally verified with measured performance at different SC conversion ratios.**

***Index Terms*—Comparative analysis, coupled inductor, commutation loop, point-of-load (PoL), hybrid switched-capacitor (SC) converter, high conversion ratio, voltage regulation module (VRM), switching-bus-based architecture, synchronous bootstrapping.**

I. Introduction

Data center electricity consumption is forecast to grow rapidly in the next decade and is expected to account for 8% of global electricity demand by 2030 [3], [4]. It is therefore imperative to develop more energy-efficient and power-dense solutions for data center power delivery in order to keep energy use in check [5]. As modern data centers shift towards the 48-V bus architecture, point-of-load (PoL) converters with a high step-down ratio (e.g., 48-to-1) and voltage regulation capability are needed to provide the low voltage ($\leqslant$ 1.0 V) and high current ($\geqslant$ 100 A) required by power-hungry microprocessors (e.g., CPUs, GPUs, ASICs, etc.).

The main challenges of 48-V-to-PoL power conversion include: i) high conversion ratio, ii) high output current, iii) high efficiency, iv) high power density, and v) fast transient response. Various solutions have been proposed to address these challenges, and they can be classified into two categories: 1) transformer-based solutions [6]–[11], and 2) hybrid switched-capacitor (SC) solutions [12]–[28].

In transformer-based solutions, highly optimized LLC converters are used for efficient fixed-ratio conversions, combined with an upstream buck-boost module [6], a multi-phase buck converter [7], [8], a series-stacked buck converter with partial power processing [10], or a current doubler rectifier [9], [11] for output voltage regulation. Although transformer-based solutions can provide galvanic isolation, it is typically not necessary for 48-V-to-PoL applications [29].

As an emerging family of topologies, hybrid SC converters have received increased attention, since they can leverage both the greatly superior energy density of capacitors compared to magnetics [30], [31] and the better figure-of-merit (FOM) of low-voltage switching devices compared to high-voltage devices [32]. To date, resonant switched-capacitor (ReSC) converters have also demonstrated superior performance to transformer-based converters for non-isolated fixed-ratio power conversions in data center applications [33]–[35].

In hybrid SC solutions, efficient and compact fixed-ratio SC networks are used to step down the input voltage first, followed by a buck-type stage for the rest of the voltage conversion task and output voltage regulation. Moreover, the inductors in the buck-type stage can enable complete soft-charging of the flying capacitors in the SC stage if the circuit is properly designed and operated [36]. Since the total conversion ratio is allocated between the SC stage and the buck-type stage, if the SC stage can achieve a larger conversion ratio, the conversion burden on the buck-type stage will be alleviated. When the output voltage is constant, buck converters with lower conversion ratios require smaller inductors and achieve higher efficiency. Given that the converter volume is typically dominated by inductors, it is favorable to design the SC stage to take on most of the voltage conversion task so that the inductor volume can be reduced, which contributes to higher power density.

This paper proposes a high-performance hybrid SC converter based on a switching bus architecture for direct 48-to-1-V power conversion in data centers. The proposed topology merges a 2-to-1 SC front-end and two 8-branch series-capacitor-buck (SCB) modules through two switching buses. In order to theoretically compare the performance of different

Portions of this manuscript were presented at the 2023 IEEE Applied Power Electronics Conference and Exposition (APEC) [1] and the 2023 IEEE Energy Conversion Congress and Exposition (ECCE) [2], respectively. This manuscript includes additional explanations of operating principles, discussions on the advantages of the switching-bus-based architecture, and in-depth theoretical analysis, as well as more hardware design considerations and experimental results.

regulated hybrid SC topologies, this paper conducts a comparative analysis which reveals that a larger SC stage conversion ratio is favorable for achieving both higher efficiency and higher power density. Through the two-phase operation of the SCB modules, the proposed topology extends the limit on duty ratio and enables a very large SC stage conversion ratio of 16-to-1. A 500-A hardware prototype was designed and built with custom two-phase coupled inductors and synchronous bootstrap daughterboards to validate the functionality and performance of the proposed topology, achieving 93.4% peak system efficiency, 86.1% full-load system efficiency (including gate drive loss), and 464-W/in^3 power density (by box volume). Moreover, the theoretical benefits of a larger SC stage conversion ratio were experimentally verified with measured performance at different SC stage conversion ratios.

The remainder of this paper is organized as follows. First, Section II details the topology and operating principles of the proposed switching bus converter, discusses the advantages of the switching-bus-based architecture, reveals the benefits of a larger SC stage conversion ratio for regulated hybrid SC topologies, and explains how this works achieves a large SC stage conversion ratio through the two-phase operation of the SCB modules. Then, Section III presents a hardware prototype with custom two-phase coupled inductors and synchronous bootstrap daughterboards and discusses its design considerations and practical implementation challenges. Finally, Section IV shows the experimental waveforms, measured performance at different SC stage conversion ratios, loss analysis, and performance comparison with state-of-the-art academic works and commercial products.

II. Switching Bus Converter

A. Proposed Topology

Fig. 1 shows the schematic drawing of the proposed switching bus converter. In the proposed topology, a 2-to-1 SC front-end (i.e., Stage 1) is merged with two 8-branch series-capacitor-buck (SCB) modules (i.e., Modules A and B in Stage 2) through two switching buses (i.e., Switching buses A and B). As the key waveforms in Fig. 2 shows, the bus voltages v_{swA} and v_{swB} always switch between two different levels, rather than being DC. Therefore, this type of intermediate bus between conversion stages is referred to as a *switching bus*. The concept of a switching bus was first introduced in [23]. The advantages of the proposed switching-bus-based architecture over the existing DC-bus-based architecture will be explained in Section II-C.

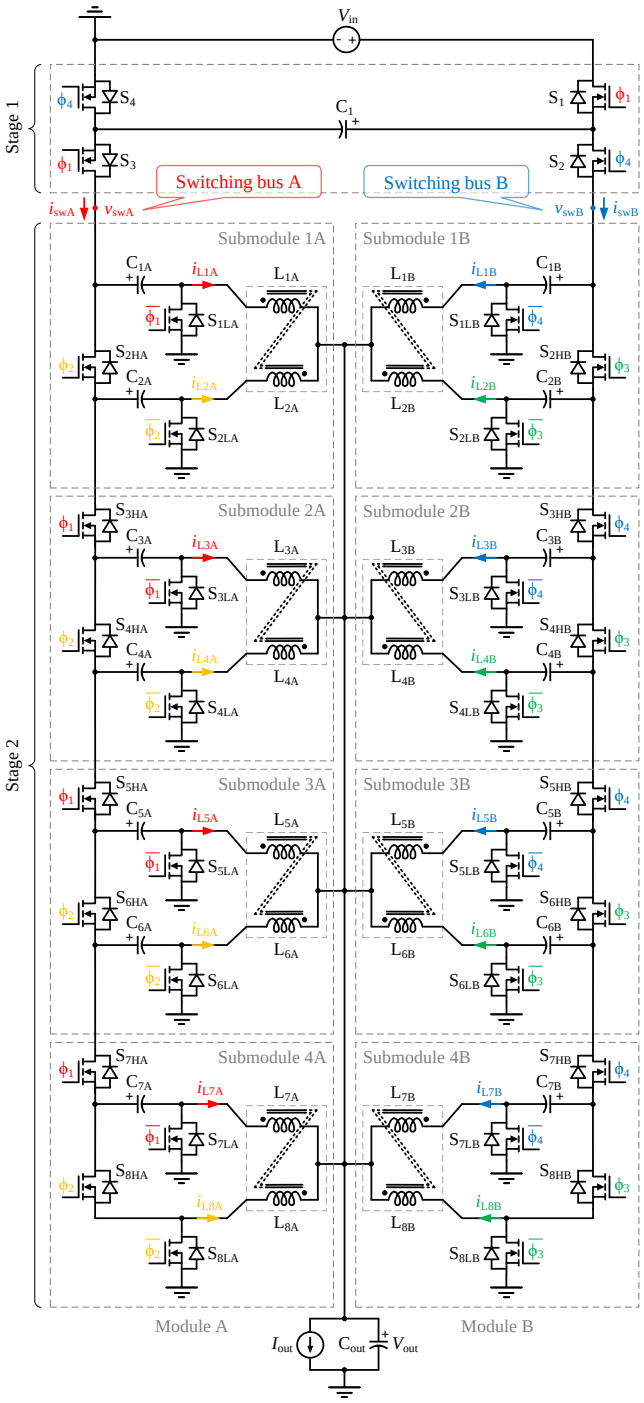


Fig. 1: Schematic drawing of the proposed switching bus converter.

B. Operating Principles

Fig. 2 illustrates the key waveforms, control signals, and equivalent circuits of the proposed switching bus converter. Each SCB module operates in a two-phase fashion, with a 180° phase shift between neighboring branches. Each SCB module consists of four submodules, within which each pair of inductors is negatively coupled. The two-phase coupled inductor design will be detailed in Section III-A. The control signals in the two modules are staggered to achieve inter-module interleaving at the output.

In periodic steady state, the average voltage across flying capacitor C_1 is $\frac{1}{2}V_{\mathrm{in}}$ and the average voltages across flying capacitors $\mathrm{C}_{k\mathrm{A/B}}$ are $\frac{8-k}{16}V_{\mathrm{in}}$ $(k = 1, 2, \cdots, 7)$. C_1 is softly charged by $\mathrm{L}_{1\mathrm{A}}$ through Switching bus A in operating modes ① and ②, and softly discharged by $\mathrm{L}_{1\mathrm{B}}$ through Switching bus B in operating modes ⑤ and ⑥. All other flying capacitors in Stage 2 $\mathrm{C}_{k\mathrm{A/B}}$ $(k = 1, 2, \cdots, 7)$ operate with complete soft-charging as well. All inductor currents and capacitor voltages are naturally balanced as a result of the negative feedback mechanism of the series-capacitor-buck converter, as explained in [37] and [17]. A detailed explanation about the automatic

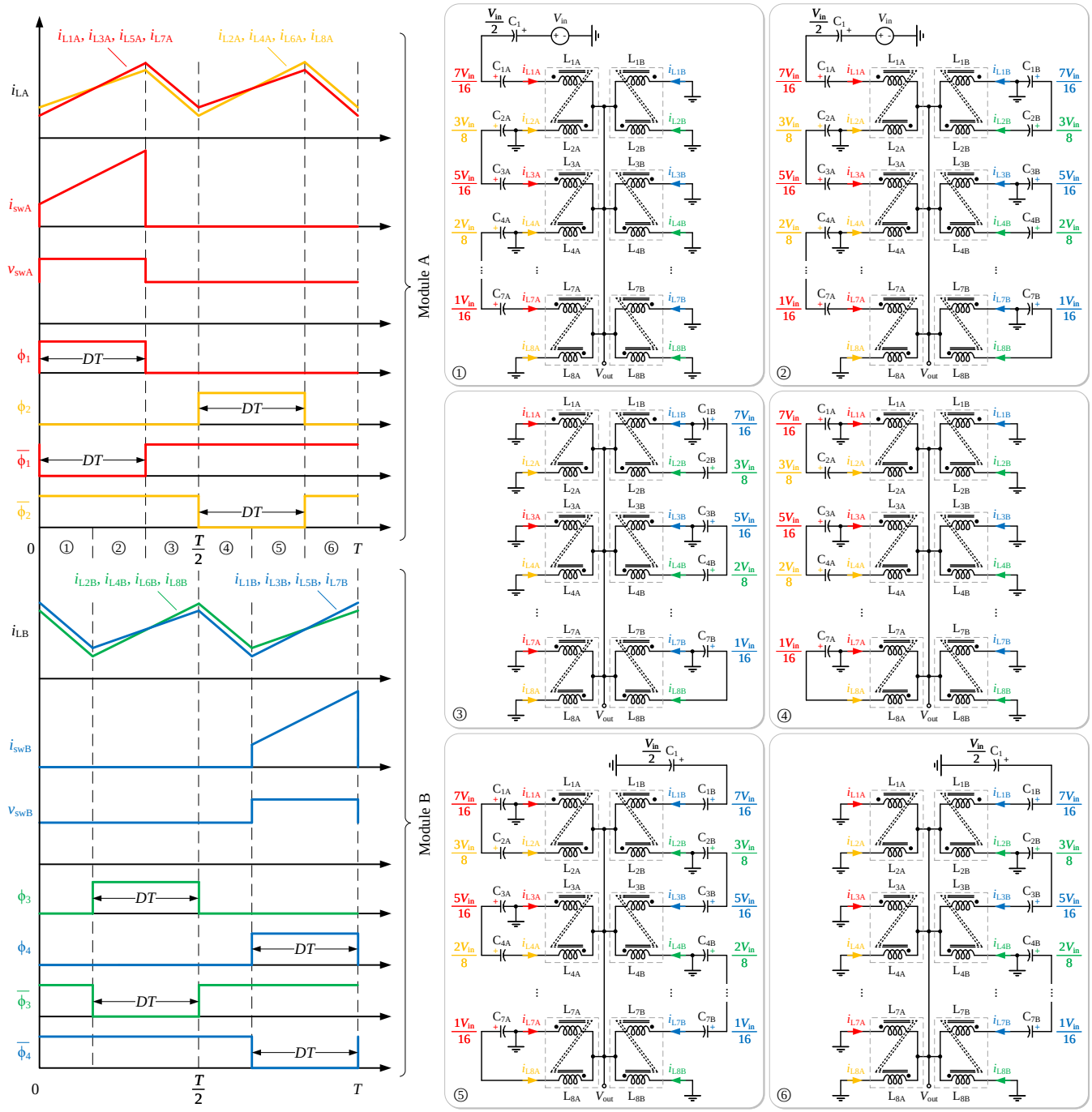


Fig. 2: Key waveforms and control signals of the proposed switching bus converter. The equivalent circuits for the six operating modes are shown on the right-hand side. The sequence of operating modes: ①→ ②→ ③→ ④→ ⑤→ ⑥→ ①→ ②→ ③→ ⋯ .

current sharing and natural voltage balancing mechanisms of the proposed topology is provided in Appendix A. The low-side switches $S_{1LA/B-8LA/B}$ can operate with zero-voltage switching (ZVS) turn-ON, provided continuous forward inductor current and sufficient deadtime. The output voltage V_{out} can be regulated by duty cycle control:

$$V_{out} = \frac{D}{16} V_{in}, \tag{1}$$

where V_{in} is the input voltage and D is the buck stage duty ratio as annotated in the clocking scheme in Fig. 2.

C. Advantages of the Switching-Bus-Based Architecture

The most straightforward approach to combining two (or multiple) conversion stages is to link them with an intermediate DC bus, as illustrated in Fig. 3(a). This DC-bus-based architecture typically requires a large and bulky bus capacitor (C_{bus}) to maintain a stiff DC bus voltage (V_{DC}), which hinders converter miniaturization.

Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture shown in Fig. 3(b) has three advantages that promise higher performance:

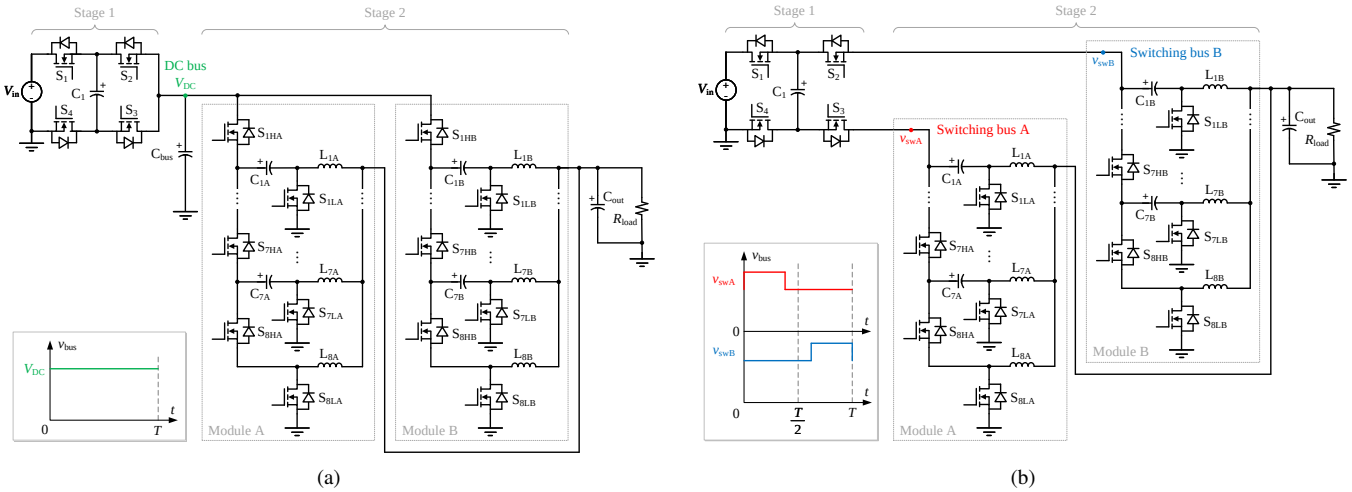


Fig. 3: Comparison between the existing DC-bus-based architecture and the proposed switching-bus-based architecture. (a) DC-bus-based architecture. (b) Switching-bus-based architecture. Compared to the DC-bus-based architecture, the switching-bus-based architecture does not require bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

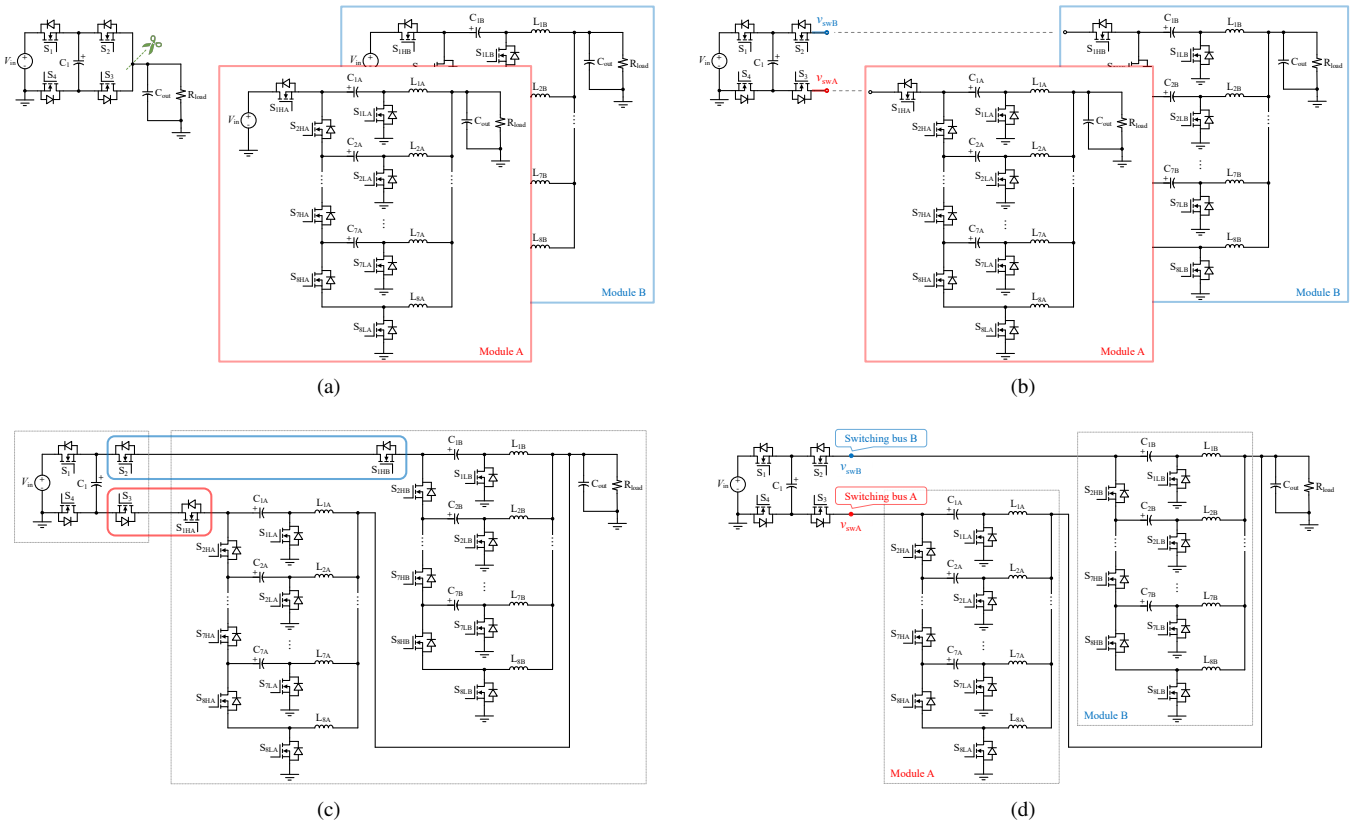


Fig. 4: Illustration of the two-stage merging process of a 2-to-1 SC front-end followed by two SCB modules, resulting in a switching bus architecture. (a) First, open the output node of the 2-to-1 SC converter in Stage 1, leaving two floating nodes v_{swA} and v_{swB}. (b) Second, connect a series-capacitor buck (SCB) module to each of the floating nodes through a switching bus. (c) Third, since none of the switching buses need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, switches $\mathrm{S_{1HA}}$ and $\mathrm{S_{1HB}}$ are removed. (d) Finally, obtain the topology of one switching bus converter.

- It does not require bus capacitors to maintain a stiff DC bus voltage.
- One redundant switch can be removed on each switching bus while two stages are merged.
- It ensures complete soft-charging operation.

Fig. 4 illustrates the two-stage merging process of a 2-to-1 SC front-end followed by two SCB modules, resulting in a switching bus architecture. First, open the output node of the 2-to-1 SC converter in Stage 1 as shown in Fig. 4(a), leaving two floating nodes v_{swA} and v_{swB}. Second, as illustrated in

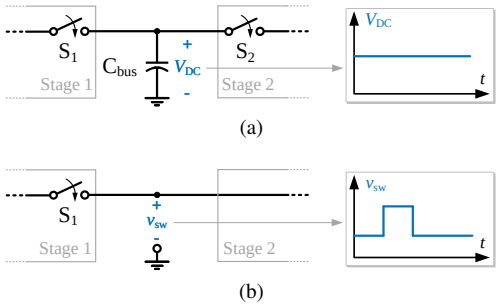


Fig. 5: General representation of (a) a DC bus and (b) a switching bus.

Fig. 4(b), connect a series-capacitor buck (SCB) module to each of these floating nodes through a switching bus. After this combination, we can see that the highest high-side switch S_{1HA} in Module A is connected in series with S_3 and S_{1HB} in Module B is in series with S_2. Since none of the switching buses need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, compared to the DC-bus-based architecture, the switching-bus-based architecture enables a reduction in the number of switches.

In addition, the switching-bus-based architecture ensures complete soft-charging operation for all flying capacitors with a simple clocking scheme, whereas complete soft-charging operation is only achievable with split-phase control [38] in some topologies [15], [25] or even unachievable in other topologies [19], [22], leading to higher power loss and greater controller complexity.

Fig. 5 shows the general representation of a DC bus and a switching bus. The switching bus concept can be generalized to construct a family of regulated hybrid SC topologies through the combination of different SC topologies. For example, the concept of a switching bus was first introduced in [23], where a Dickson^2 topology was constructed by merging a 3-to-1 Dickson front-end and three 3-branch SCB modules through three switching buses. Other switching-bus-based regulated hybrid SC topologies include the MLB converter [20] and the CaSP converter [17], with all benefiting from a similar reduction in switch count due to the strategic merging of adjacent stages. In addition, the switching bus concept can also be employed to construct fixed-ratio multi-resonant SC topologies [35] for intermediate bus converters (IBCs) in data center applications.

D. Theoretical Analysis and Topological Comparison

To compare the theoretical potential of the proposed topology to that of existing 48-V-to-1-V hybrid SC topologies, this paper uses two metrics for topological comparison [2].

The first metric is the normalized switch stress M_S, defined as the total switch volt-ampere (VA) stress normalized to the output power

$$M_S = \frac{\sum_{\text{switches}} V_{ds,i} I_{d(rms),i}}{V_{out} I_{out}}, \tag{2}$$

where $V_{ds,i}$ is the peak blocking voltage across switch i when assuming no capacitor voltage ripple, and $I_{d(rms),i}$ is the RMS value of the current through switch i when assuming no inductor current ripple. The normalized switch stress M_S indicates how much VA stress the switches in a topology experience when transferring one per-unit watt of power from the input to the output. A lower M_S is desirable, as it indicates lower switching losses and lower conduction losses and thus higher efficiency. A lower M_S also indicates a smaller switch size, which is favorable for higher power density. Fig. 6 shows the normalized switch stress M_S of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion.

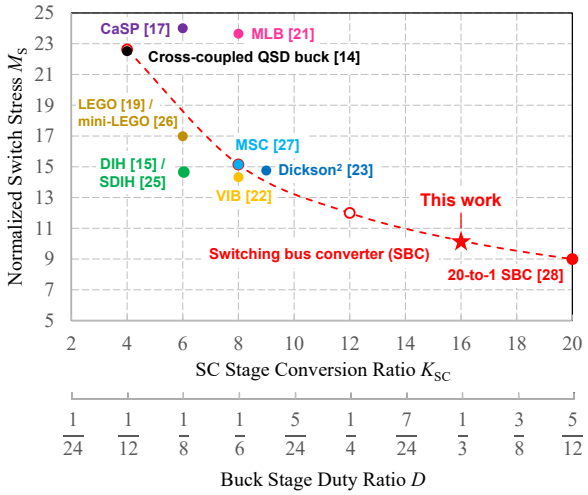


Fig. 6: Normalized switch stress M_S of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. In the analysis of normalized switch stress, capacitor voltage ripples and inductor current ripples are assumed to be negligible. A lower normalized switch stress M_S is more desirable. With a larger SC stage conversion ratio K_{SC}, the buck stage duty ratio D can be extended.

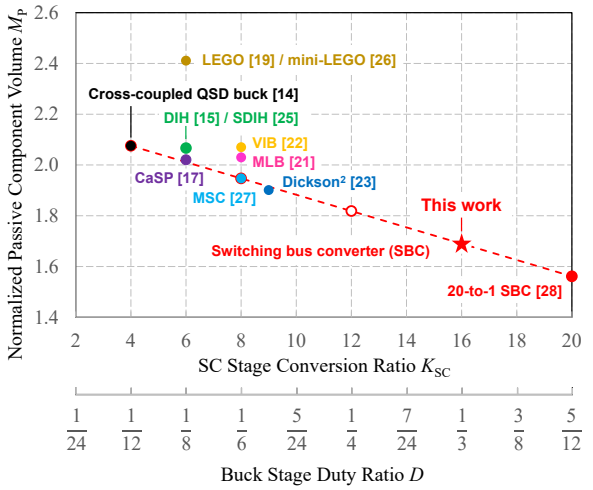


Fig. 7: Normalized passive component volume M_P of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion (assuming 30% peak-to-peak inductor current ripple and 10% peak-to-peak capacitor voltage ripple at full load, and the volumetric energy density of capacitors is 100 times higher than inductors). A smaller normalized passive component volume M_P is more desirable.

The second metric is the normalized passive component volume M_P, which can be assessed with an energy-based approach by analyzing the peak energy stored in each passive component [31], [39]. The normalized passive component

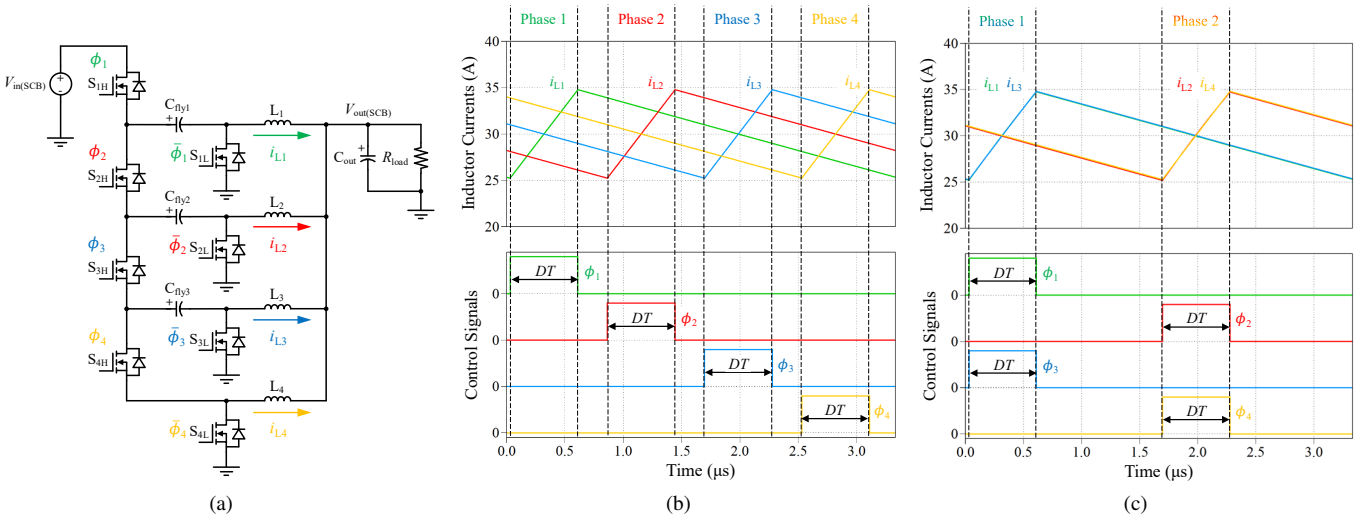


Fig. 8: Four-branch series-capacitor-buck (SCB) converter. (a) Schematic drawing. (b) Multi-phase operation. (c) Two-phase operation.

volume M_{P} indicates the total passive component volume needed to meet given ripple requirements on the inductor currents and flying capacitor voltages when transferring one per-unit watt of power from the input to the output. A smaller normalized passive component volume is desirable, as it indicates higher power density. More details of the definition of the normalized passive component volume M_{P} can be found in [2]. Fig. 7 shows the normalized passive component volume M_{P} of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion.

In general, a regulated hybrid SC topology consists of two stages: 1) a fixed-ratio SC stage for efficient and compact voltage conversion, and 2) a multi-phase buck-type stage for the remainder of the voltage conversion task, output voltage regulation, and soft-charging operation. With a larger SC stage conversion ratio, the conversion burden on the following buck-type stage can be alleviated, enabling buck-type stage efficiency improvement and inductor size reduction. Given that magnetic components are much less energy dense compared to capacitors [30] and typically dominate the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden so that the inductor volume of the buck-type stage can be reduced.

In the proposed switching bus converter, the SC stage conversion ratio can be changed by varying the number of submodules in Stage 2. The more submodules, the larger the SC stage conversion ratio. As shown in Figs. 6 and 7, as the SC stage conversion ratio increases, both the normalized switch stress M_{S} and the normalized passive component volume M_{P} decrease, meaning that a larger SC stage conversion ratio is advantageous to both higher efficiency and higher power density. This conclusion will be experimentally verified with the measured performance at different SC stage conversion ratios in Section IV-C. Compared with existing 48-V-to-1-V hybrid SC demonstrations, this work achieves a lower normalized switch stress and a smaller normalized passive component volume with a much larger SC stage conversion ratio, showing great potential for both higher efficiency and higher power density than prior solutions.

E. Two-Phase Operation of SCB Modules: Enabling A Larger SC Stage Conversion Ratio and Higher Performance

Figs. 6 and 7 show that a larger SC stage conversion ratio is desirable to achieve higher performance. In order to achieve a larger SC stage conversion ratio, this work modifies the control scheme of the SCB modules in Stage 2, from multi-phase operation to two-phase operation.

The series-capacitor-buck (SCB) topology was first proposed in [40] with multi-phase operation and then extended in [41] with two-phase operation. Fig. 8 shows a four-phase SCB converter as an example. In the multi-phase operation illustrated in Fig. 8(b), each inductor operates in an individual phase, whereas in the two-phase operation illustrated in Fig. 8(c), the inductors are grouped together into two phases with a 180° phase shift.

Compared to the two-phase operation, the multi-phase operation can achieve a smaller net output current ripple through multi-phase interleaving. However, the two-phase operation can extend the maximum duty ratio from $\frac{1}{N}$ to $\frac{1}{2}$, where N is the number of branches in a SCB converter. As a result, the upper limit on the number of branches ($N_{\mathrm{m-ph}}$ and $N_{2-\mathrm{ph}}$) can be increased:

$$\text{Multi-phase operation: } N_{\mathrm{m-ph}} < \sqrt{\frac{V_{\mathrm{in(SCB)}}}{V_{\mathrm{out(SCB)}}}} \tag{3}$$

$$\text{Two-phase operation: } N_{2-\mathrm{ph}} < \frac{V_{\mathrm{in(SCB)}}}{2V_{\mathrm{out(SCB)}}}, \tag{4}$$

where $V_{\mathrm{in(SCB)}}$ and $V_{\mathrm{out(SCB)}}$ are the input and output voltages of the SCB converter, respectively. For the proposed switching bus converter, the input and output voltages of the SCB modules in Stage 2 are $V_{\mathrm{in(SCB)}} = 24$ V and $V_{\mathrm{out(SCB)}} = 1$ V, respectively. Therefore, the maximum allowable numbers of branches in the SCB modules for multi-phase operation and two-phase operation are $N_{\mathrm{m-ph(max)}} = 4$

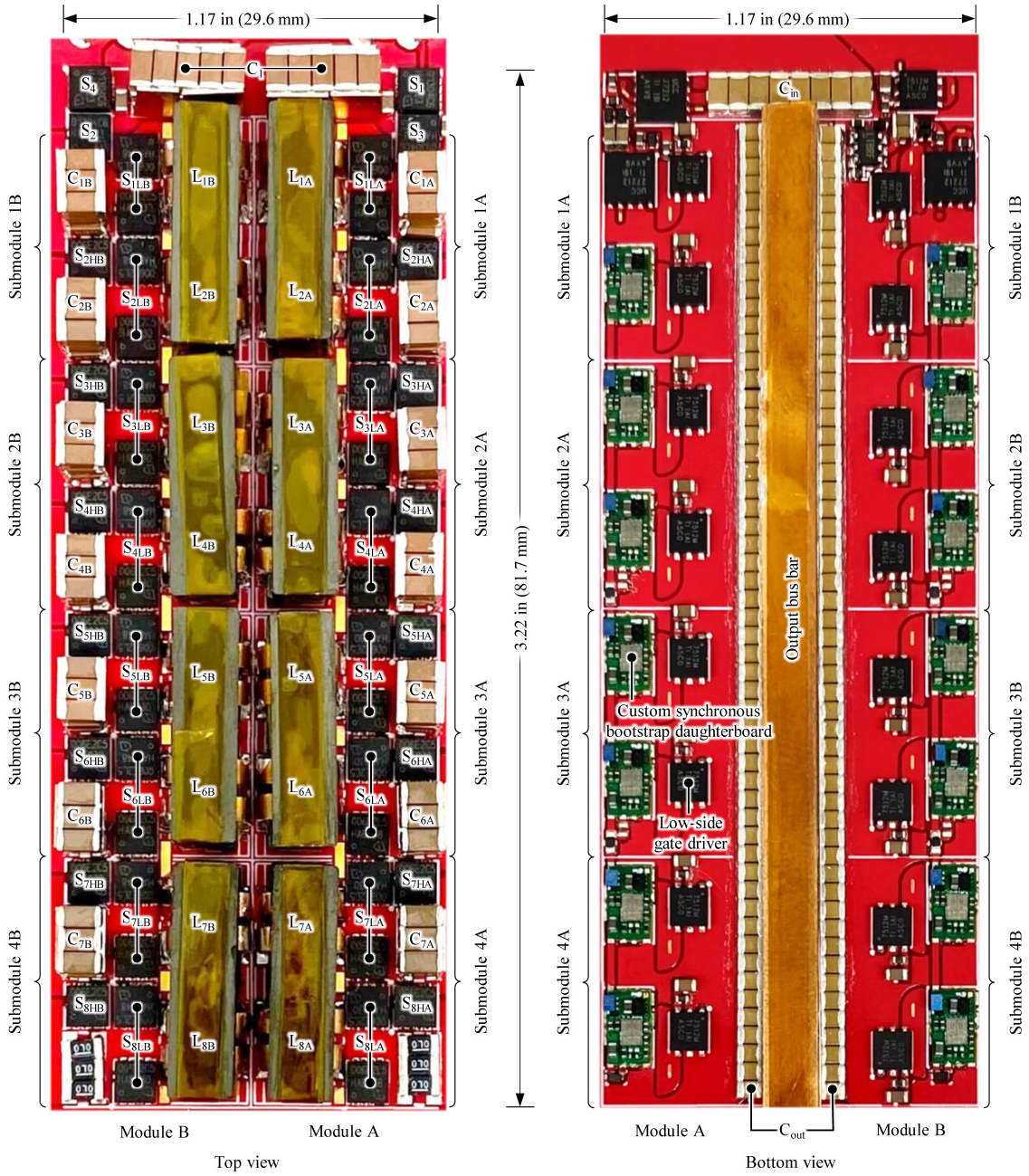


Fig. 9: Photograph of the hardware prototype. Dimensions: $3.22 \times 1.17 \times 0.29$ in^3 ($81.7 \times 29.6 \times 7.3$ mm^3).

and $N_{2-\mathrm{ph(max)}} = 10$, respectively. Compared to the multi-phase operation, the two-phase operation can extend the upper limit on the number of branches and thus better leverage the benefit of a larger SC stage conversion ratio. In addition, the two-phase operation enables a faster transient response with an extended maximum duty ratio.

One possible concern about the two-phase operation is that it sacrifices the net output current ripple reduction compared to the multi-phase operation. However, this does not generally mean that the two-phase operation necessitates the need for a larger output capacitor. In PoL applications, the size of the output capacitor is typically determined by the requirements for transient performance (i.e., maximum overshoot and undershoot on output voltage). With a sufficiently large output capacitor to satisfy the transient performance requirements, the steady-state output voltage ripple is typically much smaller than the maximum tolerable value allowed by microprocessors. In other words, the output capacitor is usually oversized in terms of steady-state output voltage ripple suppression. Therefore, the output capacitance does not need to be increased when using the two-phase operation. In fact, since the two-phase operation enables a faster transient response compared to the multi-phase operation, the output capacitance can be reduced.

A major contribution of this work is to reveal that a larger SC stage conversion ratio enables higher performance of regulated hybrid SC topologies, which can be achieved through the two-phase operation of SCB modules.

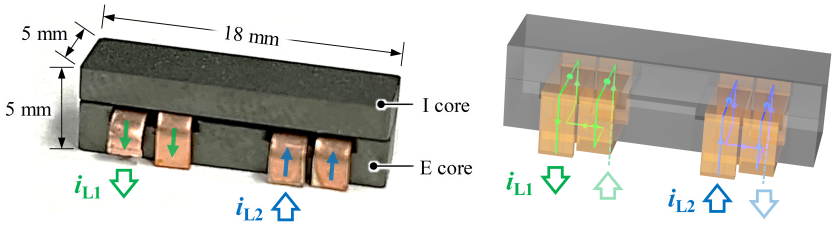
TABLE I: Component list of the hardware prototype

Component	Part number	Parameters
MOSFET S_{1-4}	Infineon IQE013N04LM6CG	40 V, 1.35 mΩ
MOSFET $S_{2HA/B-8HA/B}$	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
MOSFET $S_{1LA/B-8LA/B}$	Infineon IQE006NE2LM5CG, IQE006NE2LM5	25 V, 0.65 mΩ (in parallel)
Flying capacitor C_1	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 μF*×30 (in parallel)
Flying capacitor $C_{1A/B-5A/B}$	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 μF*×9 (in parallel)
Flying capacitor $C_{6A/B,\ 7A/B}$	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μF*×9 (in parallel)
Coupled inductor $L_{1A/B-8A/B}$	Custom two-phase coupled inductor	See Table II for details
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 μF*×8 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μF*×108 (in parallel)
Low-side gate driver	Texas Instruments UCC27512	4-A peak source, 8-A peak sink
High-side gate driver in Stage 1	Texas Instruments UCC27212	4-A peak source, 4-A peak sink
High-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source, 5-A peak sink

* The capacitance listed in this table is the nominal value before DC derating.

(a) (b)

Fig. 10: (a) Side view of the hardware prototype. (b) Photograph of the gate drive circuitry, including the custom synchronous bootstrap daughterboards (dimensions: $5.8 \times 3.5 \times 1.0$ mm^3) used to power the high-side switches.



(a) (b)

Fig. 11: Custom two-phase coupled inductor. The two phases are negatively coupled. Each winding has two turns that are connected with a PCB trace beneath the E core. (a) Photograph with dimensions annotated. (b) 3D rendering with current paths annotated.

TABLE II: Key parameters and operating conditions of the two-phase coupled inductor

Parameter	Value
Coupling coefficient	-0.8
Per-Phase steady-state inductance	606.5 nH
Per-Phase transient inductance	200 nH
Overall transient inductance	12.5 nH
Per-Phase DC resistance	0.48 mΩ
Per-Phase saturation current	40 A
Output voltage	1.0 V
Switching frequency	150 kHz
Nominal duty ratio	0.333
Per-Phase current ripple	7.33 A

III. Hardware Prototype and Practical Implementation Challenges

A 48-V-to-1-V hardware prototype was designed and built to verify the functionality and performance of the proposed switching bus converter. Fig. 9 shows an annotated photograph of the prototype, with the main circuit components listed in Table I. Fig. 10 presents the side view of the hardware prototype and a zoomed-in photograph of the gate drive circuitry, including the custom synchronous bootstrap daughterboards used to power the high-side switches.

All flying capacitors are stacked up to 3 layers to match the height of the coupled inductors so that the box volume of the prototype can be fully utilized. The stacked flying capacitors serve as natural heat sinks due to their connection with power MOSFETs through thermally conductive PCB traces. In addition, the distributed switch and capacitor network provides an inherent heat spreading. The switching frequency of this prototype is 150 kHz. The 1.3-mm thick PCB has 8 layers, with 2 oz copper on each layer.

A. Two-Phase Coupled Inductor

As demonstrated in [21], compared with discrete inductors, two-phase coupled inductors can reduce the core volume by approximately half while preserving the same equivalent per-phase steady-state inductance. To improve power density, the two-phase coupled inductor shown in Fig. 11 was customized and assembled for this prototype. The two phases are negatively coupled through the magnetic core combined from an E core and an I core. The magnetic cores were fabricated with DMEGC DMR96A Mn-Zn ferrite material. Each winding has two turns, and each turn is made from a piece of 0.5 mm thick and 2 mm wide copper. To reduce the total height of the coupled inductor, the two turns are connected with a PCB trace beneath the E core.

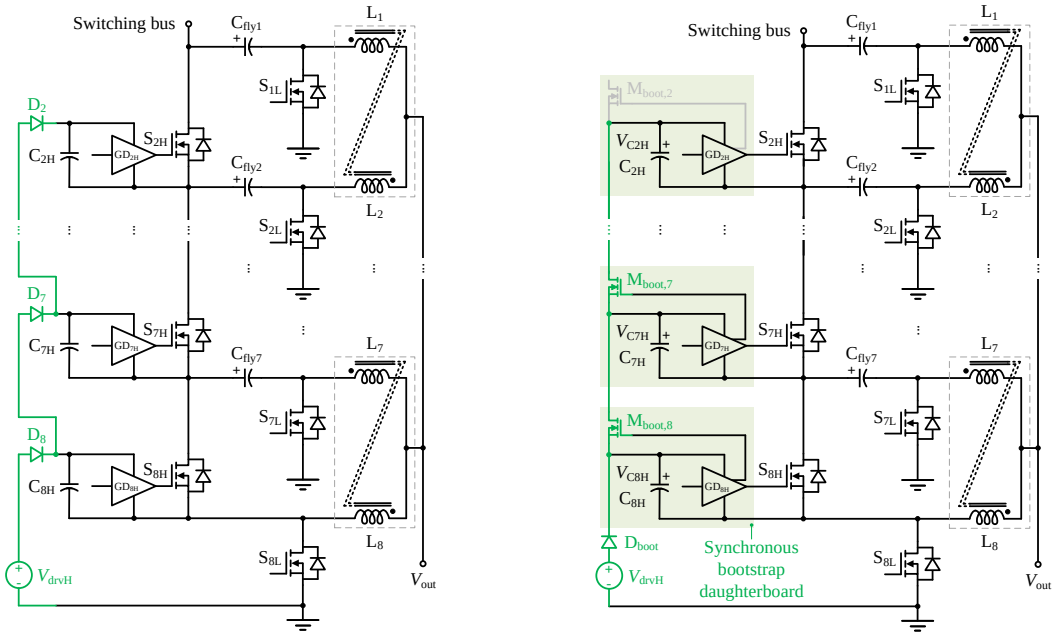


Fig. 12: Comparison between two gate drive techniques for the high-side switches in Modules A and B. (a) Conventional cascaded bootstrapping that suffers from accumulative voltage drops across bootstrap diodes. (b) Synchronous bootstrapping that replaces bootstrap diodes with active FETs [43].

The key parameters and operating conditions of this two-phase coupled inductor are listed in Table II. Operating at a duty ratio of 0.333, the equivalent per-phase steady-state inductance of this coupled inductor is 606.5 nH, leading to a peak-to-peak inductor current ripple of 7.33 A at 150-kHz switching frequency and 1.0-V output voltage. More details about the analysis and design of the two-phase coupled inductor can be found in Appendix B.

B. Gate Drive Circuitry for High-Side Switches

One practical challenge of the hardware implementation is the gate drive circuitry for the high-side switches in Stage 2 (i.e., $S_{2HA/B-8HA/B}$). Due to the large number of high-side switches, conventional cascaded bootstrapping [42] illustrated in Fig. 12(a) suffers from accumulative voltage drops across bootstrap diodes, leading to considerable gate drive loss.

To address this challenge, this work adopts the synchronous bootstrap technique [43] illustrated in Fig. 12(b), with a synchronous bootstrap daughterboard customized for this demonstration, as shown in Fig. 10(b). By replacing bootstrap diodes with active FETs, the voltage drops in the bootstrap circuit can be greatly reduced, thus improving the gate drive efficiency. Experimental results in Fig. 13 show that the total voltage drop in the bootstrap circuit across seven daughterboards is only 0.7 V, which is typically the voltage drop across one bootstrap diode in the conventional cascaded bootstrap circuit.

In Stage 1, the gate-driven charge pump circuit [42] is used to power high-side switches S_1 and S_2. S_3 is powered by cascaded bootstrapping through a single diode.

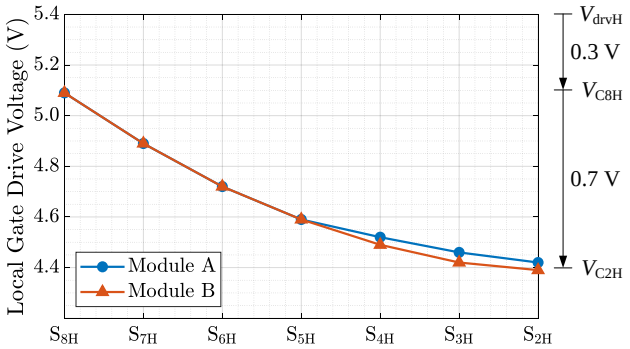


Fig. 13: Measured local gate drive voltages of Modules A and B in the hardware prototype. The high-side gate drive supply voltage (V_{drvH} in Fig. 12(b)) is 5.4 V. The voltage drop across the bootstrap diode (D_{boot} in Fig. 12(b)) is roughly 0.3 V. The total voltage drop across the seven daughterboards is only 0.7 V.

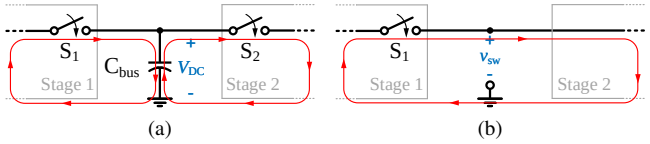


Fig. 14: Illustration of the commutation loops in (a) the DC-bus-based architecture and (b) the switching-bus-based architecture.

C. Commutation Loop Optimization

Another implementation challenge is the commutation loop optimization. Large commutation loop inductance can be detrimental in multiple ways, including large voltage spikes during switching transitions that can cause device over-voltage, increased overlap loss if the switching transition has to be

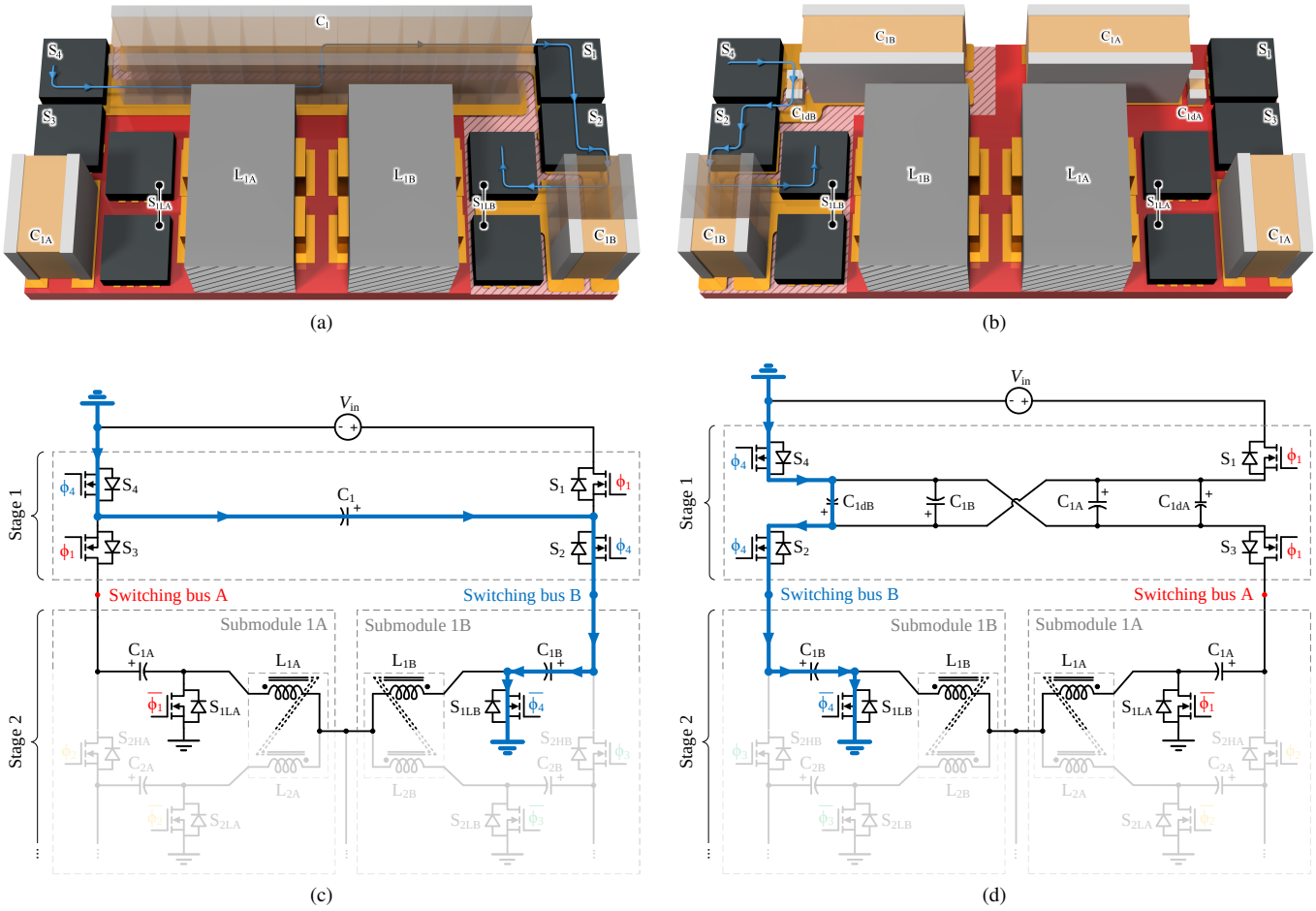


Fig. 15: (a) Original PCB layout of Stage 1 and Submodules 1A and 1B that directly follows the schematic drawing in Fig. 1, leading to a large commutation loop (highlighted in blue) with a parasitic inductance of 2.75 nH (obtained through Ansys FEM simulation). (b) Improved PCB layout with Submodule 1A plus S_3 and Submodule 1B plus S_2 swapped, the flying capacitor bank C_1 split, and two small decoupling capacitors C_{1dB} and C_{1dA} added that dramatically reduces the size of the commutation loop (highlighted in blue) with a parasitic inductance of 1.76 nH (obtained through Ansys FEM simulation), demonstrating a reduction in parasitic inductance approximately by half. (c) Schematic drawing of the original PCB layout with the commutation loop highlighted in blue. (d) Schematic drawing of the improved PCB layout with the commutation loop highlighted in blue.

slowed (e.g., with larger the gate resistance) to mitigate the voltage spike, increased parasitic inductance loss, and high-frequency ringing which leads to electromagnetic interference (EMI) [44]–[46].

As illustrated in Fig. 14(a), in the DC-bus-based architecture, the commutation loops in the two stages can be decoupled through the bus capacitor C_{bus}. However, in the switching-bus-based architecture, the two small commutation loops in Fig. 14(a) merge into one large loop through the switching bus, as illustrated in Fig. 14(b).

Fig. 15(a) shows the original PCB layout of Stage 1 and Submodules 1A and 1B that directly follows the schematic drawing in Fig. 1, which leads to a large commutation loop (highlighted in blue) with a parasitic inductance of 2.75 nH (obtained through Ansys FEM simulation). To reduce the size of the commutation loop, we swapped the positions of Submodule 1A plus S_3 and Submodule 1B plus S_2, split the flying capacitor bank C_1 into C_{1A} and C_{1B}, and added two small decoupling capacitors C_{1dA} and C_{1dB}, as demonstrated in Fig. 15(b). It can be seen that this improvement dramatically shrinks the commutation loop, reducing its parasitic inductance by one-third from 2.75 nH to 1.76 nH. The schematic drawings of the original and improved PCB layout are shown in Figs. 15(c) and (d), with the commutation loop highlighted in blue.

IV. Experimental Results and Analysis

Table III lists the key parameters and test conditions of the hardware prototype presented in Section III. A TDK-Lambda GEN 60-85-3P480 60-V DC power supply was used to provide the 48-V input voltage, and a Chroma 63203 600-A DC electronic load was used to sink the output current. A Yokogawa WT3000E precision power analyzer was used to measure the input voltage, input current, and output voltage, and the DC electronic load measured the output current.

A. Experimental Waveforms

Fig. 16 shows the simulation and experimental waveforms of the switching bus voltages v_{swA} and v_{swB}. As shown in Figs. 16(a) and (b), at no load, the bus voltages switch between two different levels (21 V and 24 V), as has been

TABLE III: Key parameters and test conditions

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	1.0 V
Full-load output current	500 A
Per-phase average inductor current at full load	31.25 A
Switching frequency	150 kHz
Gate drive voltage of Stage 1	8.0 V
High-side gate drive voltage of Stage 2	5.4 V
Low-side gate drive voltage of Stage 2	5.0 V
Prototype box volume*	1.08 in^3
Power component volume†	0.331 in^3

* The box volume is defined as the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry.
† The power components included in the volume calculation are switching devices, flying capacitors, and buck inductors.

explained in Section II and illustrated in Fig. 2. At full load, the flying capacitor voltage ripples are superimposed on the switching bus voltage waveforms. As shown in Figs. 16(c) and (d), the experimental waveforms are in good agreement with the simulation waveforms. Fig. 17 presents the simulation and experimental waveforms of flying capacitor voltages C_1 and C_{1B}-C_{7B}. As can be seen, the measured flying capacitor voltages are naturally balanced and in excellent agreement with the simulation waveforms. Moreover, the smooth and continuous capacitor voltage waveforms confirm the complete soft-charging operation of all flying capacitors.

B. Measured Performance and Loss Analysis

The proposed converter was tested up to 500-A output current at 1.0-V output voltage, achieving a power density of 464 W/in^3 by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry). Fig. 18 shows the thermal image of the prototype running continuously at full load with fan cooling only. As can be observed in the thermal image, the distributed switch and capacitor network inherently facilitates heat dissipation, and the vertically-stacked flying capacitors function as natural heat sinks, which mitigates the hot-spot cooling challenges and enables easier thermal management. It should be noted that custom heat sinks can be added to the MOSFETs for better thermal performance without increasing the box volume since there is currently 4 mm of unused space above the MOSFETs.

Fig. 19 presents the measured efficiency of the hardware prototype. It achieved 94.7% peak power stage efficiency at 104-A output current and 86.4% full-load power stage efficiency at 500-A output current. With the gate drive loss included, it achieved 93.4% peak system efficiency at 132-A output current and 86.1% full-load system efficiency at 500-A output current.

In order to gain deeper insights into the origins of power loss in the prototype and to identify potential avenues for performance improvement, a comprehensive loss breakdown was conducted at both the peak system efficiency point and full-load point, as shown in Fig. 20. The frequency-dependent losses (i.e., MOSFET switching loss, body-diode conduction loss, MOSFET gate drive loss, coupled inductor core loss, and parasitic inductance loss) represent a large portion of the total loss at the peak system efficiency point, while the conduction losses (i.e., MOSFET conduction loss, flying capacitor ESR conduction loss, coupled inductor winding loss, and PCB trace conduction loss) are dominant at the full-load point. The PCB trace conduction loss accounts for roughly a quarter of the total loss at the peak system efficiency point and nearly half of the total loss at the full-load point. In future work, the PCB trace conduction loss can be reduced with thicker copper layers or a more compact PCB layout enabled by higher switching frequency.

TABLE IV: Comparison of measured performance at different SC stage conversion ratios (K_{SC})

K_{SC}	16	12	8
Nominal duty ratio	0.333	0.25	0.167
Switching frequency*	150 kHz	200 kHz	250 kHz
Per-phase inductor current ripple ratio*	12%	12%	12%
Overall output current at full load	500 A	380 A	260 A
Power density†	464 W/in^3	464 W/in^3	464 W/in^3
Peak power stage efficiency	94.7% (at 104 A)	93.7% (at 82 A)	92.3% (at 64 A)
Full-load power stage efficiency	86.3%	86.1%	85.4%
Peak system efficiency	93.4% (at 132 A)	92.2% (at 112 A)	90.7% (at 80 A)
Full-load system efficiency	86.1%	85.7%	85.0%

* In all configurations, the switching frequency was adjusted to maintain the same per-phase inductor current ripple ratio, defined as the ratio of the peak ripple amplitude to the average value of the inductor current.
† To facilitate a fair full-load efficiency comparison, all three configurations were designed to achieve the same power density.

C. Comparison of Measured Performance at Different SC Stage Conversion Ratios

As revealed in the comparative analysis in Section II-D, for regulated hybrid SC topologies, a larger SC stage conversion ratio is favorable for achieving higher performance. To experimentally verify this conclusion, this subsection compares and analyzes the performance of the hardware prototype measured at different SC stage conversion ratios.

Due to the good modularity of the hardware prototype presented in Section III, the converter can be easily reconfigured for different SC stage conversion ratios. The SC stage conversion ratio of the configuration shown in Figs. 1 and 9 is 16-to-1, which comes from the multiplication of the 2-to-1 SC conversion ratio of Stage 1 and the 8-to-1 SC conversion ratio of Stage 2. By removing Submodules 4A and 4B and short-circuiting flying capacitors C_{6A} and C_{6B}, Stage 2 can be reconfigured to have a 6-to-1 SC conversion ratio, making the SC stage conversion ratio of the prototype 12-to-1. Similarly, an 8-to-1 SC stage conversion ratio can be achieved with Submodules 3A, 3B, 4A and 4B removed and flying capacitors C_{4A} and C_{4B} short-circuited. The gate drive circuitry is designed to be reconfigurable as well.

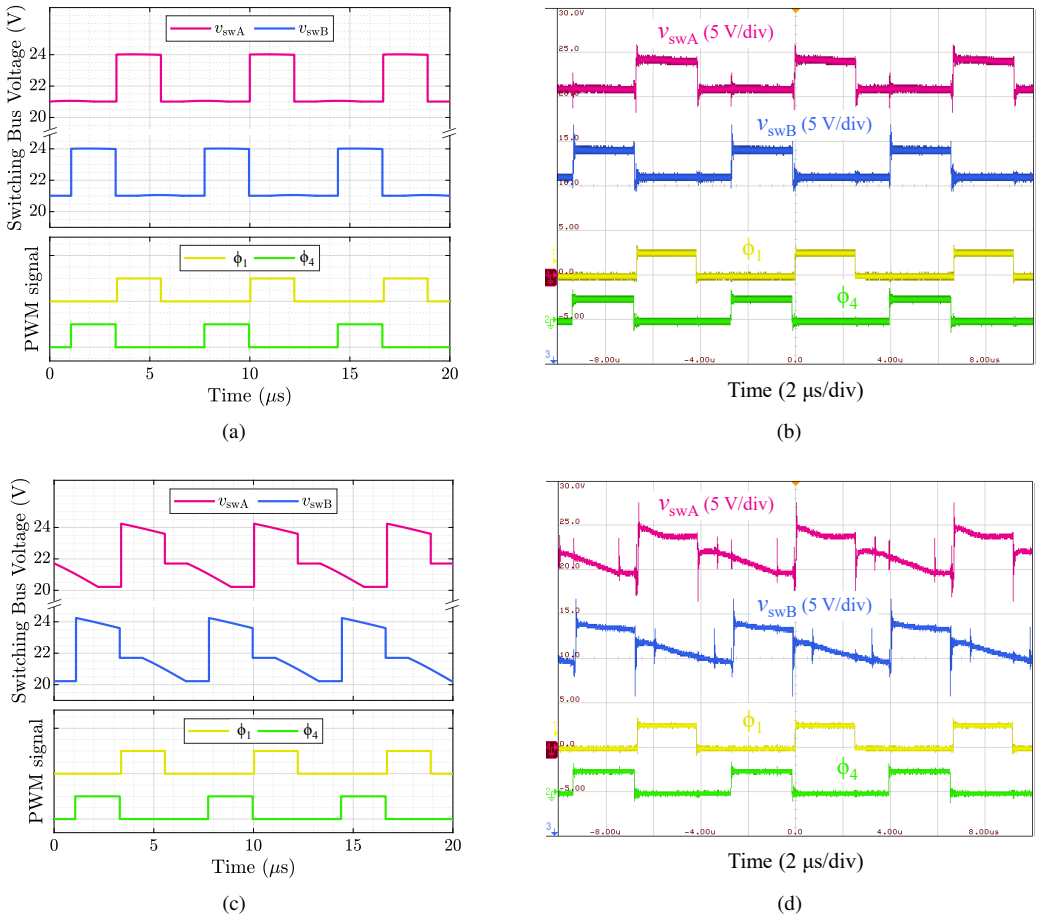


Fig. 16: Waveforms of switching bus voltages v_{swA} and v_{swB}. (a) Simulation waveforms at no load. (b) Experimental waveforms at no load. (c) Simulation waveforms at full load. (d) Experimental waveforms at full load.

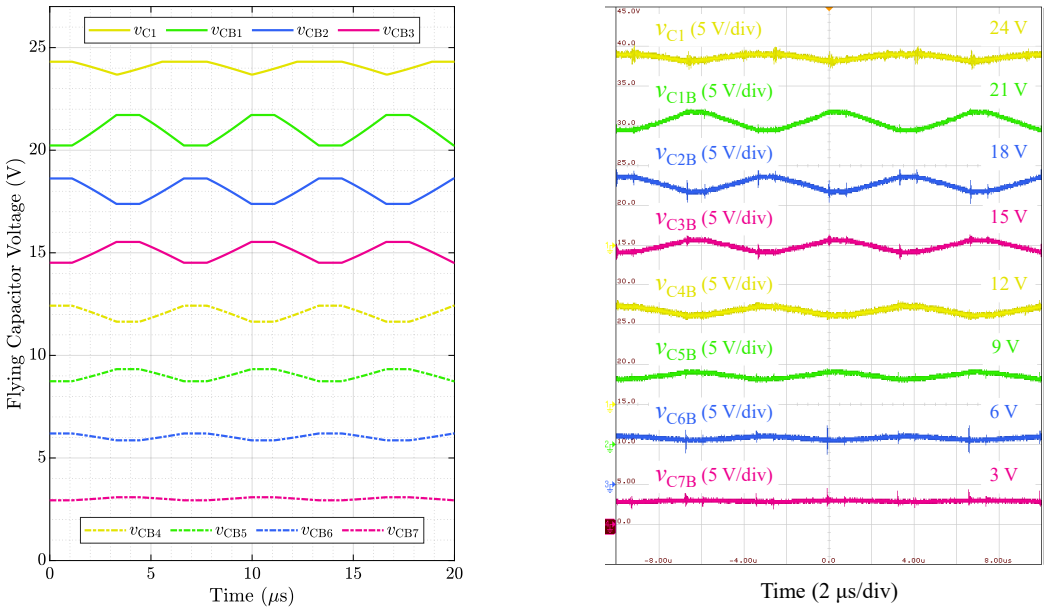
Fig. 21 shows the measured efficiency at different SC stage conversion ratios (K_{SC}), with the operating conditions and key performance listed in Table IV. In all configurations, the switching frequency was adjusted to maintain the same per-phase inductor current ripple ratio, defined as the ratio of the peak ripple amplitude to the average value of the inductor current. To facilitate a fair full-load efficiency comparison, all three configurations were designed to achieve the same power density.

As can be observed in Fig. 21 and Table IV, with a larger SC stage conversion ratio, the hardware prototype achieved both higher peak efficiency and higher full-load efficiency, which experimentally verifies the theoretical benefits revealed in the comparative analysis in Section II-D. In theory, as shown in Figs. 6 and 7, the performance of the converter can be improved by further increasing the SC stage conversion ratio from 16-to-1 to 20-to-1 (maximum allowable SC stage conversion ratio for 48-V-to-1-V conversion as explained in Section II-E), with one additional submodule added to each of the SCB modules. One major benefit of a larger SC stage conversion ratio is the switch voltage stress reduction. In practice, however, although the peak blocking voltages of the high-side switches $\mathrm{S}_{1\mathrm{HA/B}-8\mathrm{HA/B}}$ and the low-side switches $\mathrm{S}_{1\mathrm{LA/B}-8\mathrm{LA/B}}$ are 6 V and 3 V, respectively, with a 16-to-1 SC stage conversion ratio and 48-V input voltage, the best-performance switching devices (Infineon IQE006NE2LM5CG and IQE006NE2LM5) available on the market for this application are rated at 25 V. Given that the switching devices are overrated, the theoretical potential of the 20-to-1 configuration cannot be fully realized. This is why the hardware prototype presented in this paper adopts a SC stage conversion ratio of 16-to-1. To fully realized the theoretical potential of the proposed switching bus topology, lower voltage devices with better figure-of-merit are needed.

D. Performance Comparison with the State of the Art

Table V compares the performance of this work to that of the state-of-the-art 48-V-to-1-V academic works in previous literature, demonstrating the high efficiency and high power density of this work. It is worth noting that the 20-to-1 switching bus converter (SBC) is an extension of this work with a larger SC stage conversion ratio that achieves excellent performance.

Table VI shows a performance comparison between this work and existing 48-V-to-1-V commercial products. It can be seen that this preliminary laboratory prototype achieves outstanding efficiency and power density, even when compared



(a) (b)

Fig. 17: Waveforms of flying capacitor voltages v_{C1} and $v_{C1B-C7B}$. (a) Simulation waveforms at full load. (b) Experimental waveforms at full load.

TABLE V: Performance comparison between this work and the state-of-the-art 48-V-to-1-V academic works

Year	Reference	Output Current	Operating Frequency*	Power Density**	Power Stage Efficiency	System Efficiency†
2023	This work	500 A (31.3 A/phase)	150 kHz	464 W/in^3 (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2023	20-to-1 SBC [28] (extension of this work)	1200 A (30 A/phase)	200 kHz	607 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 87.9%	92.4% 87.5%
2023	MSC [27]	450 A (28.1 A/phase)	400 kHz	621 W/in^3 (by box volume)	Peak efficiency: 93.1% Full-load efficiency: 86.2%	91.7% 85.8%
2023	Mini-LEGO [26]	240 A (20 A/phase)	1.5 MHz	1390 W/in^3 (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2022	SDIH [25]	105 A (52.5 A/phase)	750 kHz	598 W/in^3 (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2022	Dickson^2 [23]	270 A (30 A/phase)	280 kHz	360 W/in^3 (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [22]	450 A (28.1 A/phase)	417 kHz	232 W/in^3 (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [21]	60 A (30 A/phase)	250 kHz	263 W/in^3 (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	LEGO [19]	450 A (37.5 A/phase)	1 MHz	294 W/in^3 (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [14]	40 A (20 A/phase)	125 kHz	150 W/in^3 (by power component volume)	Peak efficiency: 95.1%‡ Full-load efficiency: 92.7%‡	N/A N/A
2020	Sigma [10]	80 A	1 MHz	420 W/in^3 (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

* Switching frequency of the voltage regulation stage.
** The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.
† Gate drive loss is included in the calculation of system efficiency. ‡According to direct correspondence with the author.

to highly optimized commercial power modules with advanced packaging.

In the switching bus converter, the conversion burden on the buck stage can be alleviated by increasing the SC stage conversion ratio, which enables inductor volume reduction. This means that the target power density can be achieved with a lower switching frequency, contributing to lower switching losses and higher efficiency.

TABLE VI: Performance comparison between this work and existing 48-V-to-1-V commercial products

Release Year	Reference	Output Current	Operating frequency*	Power Density**	System Efficiency†
2023	This work	500 A	150 kHz	464 W/in^3	Peak: 93.4%, Full-load: 86.1%
2021	ADI LTM4664 [47]	50 A	350 kHz	415 W/in^3	Peak: 90.8%, Full-load: 88.0%
2018	Bel Power Solutions ST4-1V0M07G [48]	70 A	450 kHz	167 W/in^3	Peak: 91.5%, Full-load: 90.5%
2016	TI LMG5200POLEVM-10 [49]	50 A	600 kHz	N/A	Peak: 90.7%, Full-load: 87.6%
2012 2015	Vicor PRM48AF480T400A00 [50] +2×VTM48EF012T130C01 [51]‡	200 A	1.03 MHz 1.20 MHz	236 W/in^3	Total efficiency: 89.7%‡

* Switching frequency of the voltage regulation stage.
† Gate drive loss is included in the calculation of system efficiency.
**Power density calculated by the box volume.
‡Recommended and provided by Vicor's online Power System Designer.

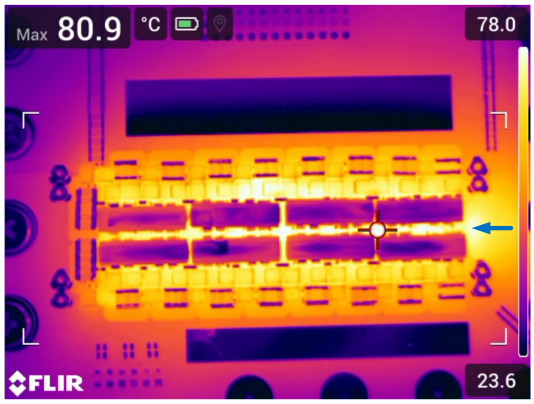


Fig. 18: Full-load thermal image at thermal equilibrium with fan cooling only ($V_{\text{in}} = 48$ V, $V_{\text{out}} = 1.0$ V, $I_{\text{out}} = 500$ A). The blue arrow on the right-hand side indicates the direction of airflow.

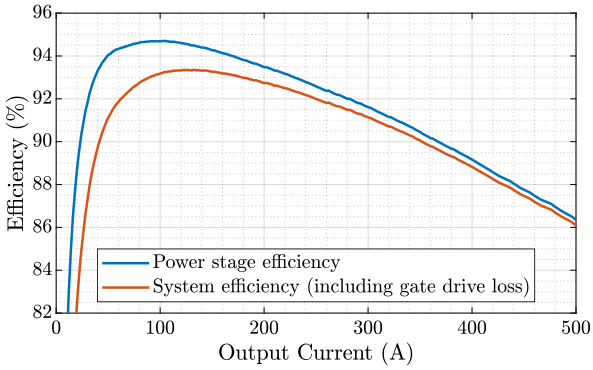


Fig. 19: Measured 48-to-1-V efficiency. Peak efficiency: 94.7% at $I_{\text{out}} = 104$ A (93.4% at $I_{\text{out}} = 132$ A including gate drive loss). Full-load efficiency: 86.4% (86.1% including gate drive loss) at $I_{\text{out}} = 500$ A.

V. Conclusion

This paper presents a switching bus converter for direct 48-V-to-PoL power conversion in data centers. In the proposed topology, a 2-to-1 SC front-end is merged with two 8-branch SCB modules through two switching buses, achieving a SC stage conversion ratio of 16-to-1. Compared to the existing DC-bus-based architecture, the proposed switching-bus-based architecture does not require DC bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

Through a comparative analysis based on the normalized switch stress and the normalized passive component volume, this paper reveals that a regulated hybrid SC topology with a larger SC stage conversion ratio has the potential to achieve both higher efficiency and higher power density, which is experimentally verified with measured performance at different SC stage conversion ratios. In order to achieve a larger SC stage conversion ratio, this work modifies the control scheme of the SCB modules from multi-phase to two-phase operation, which extends the maximum duty ratio and allows for more SCB branches.

In order to validate the theoretical potential of the proposed topology, we designed and built a modular hardware prototype with custom two-phase coupled inductors. The synchronous bootstrap technique, implemented on custom daughterboards, was used to overcome the accumulative voltage drops seen when using conventional cascaded bootstrapping diodes. Additionally, the PCB layout was optimized for smaller commutation loops along the switching buses.

The hardware prototype was tested up to 500-A output current at 1-V output voltage, achieving 93.4% peak system efficiency, 86.1% full-load system efficiency (including gate drive loss), and 464-W/in^3 power density (by box volume). Compared to state-of-the-art 48-V-to-1-V academic works and commercial products, this switching bus converter prototype achieved both excellent efficiency and power density. The performance of this hardware prototype demonstrates the great potential of the switching-bus-based architecture and underscores the benefits of a larger SC stage conversion ratio.

Appendix A
Automatic Current Sharing and Natural Voltage Balancing Mechanisms

This Appendix explains the automatic current sharing and natural voltage balancing mechanisms of the proposed switching bus converter. First, a quantitative analysis is performed to show that the balanced state is the natural equilibrium of the converter in periodic steady state (PSS). Second, a qualitative analysis is provided to intuitively explain how the converter counteracts any temporary imbalance in inductor currents and capacitor voltages and restores them to their balanced states after disturbance.

A. Quantitative Analysis

1) Automatic Current Sharing Mechanism: Denote the average currents of the inductors and capacitors in the switching bus converter as $\langle i_{\text{L}jA/B}\rangle$ $(j = 1, 2, \cdots, 8)$, $\langle i_{\text{C1}}\rangle$,

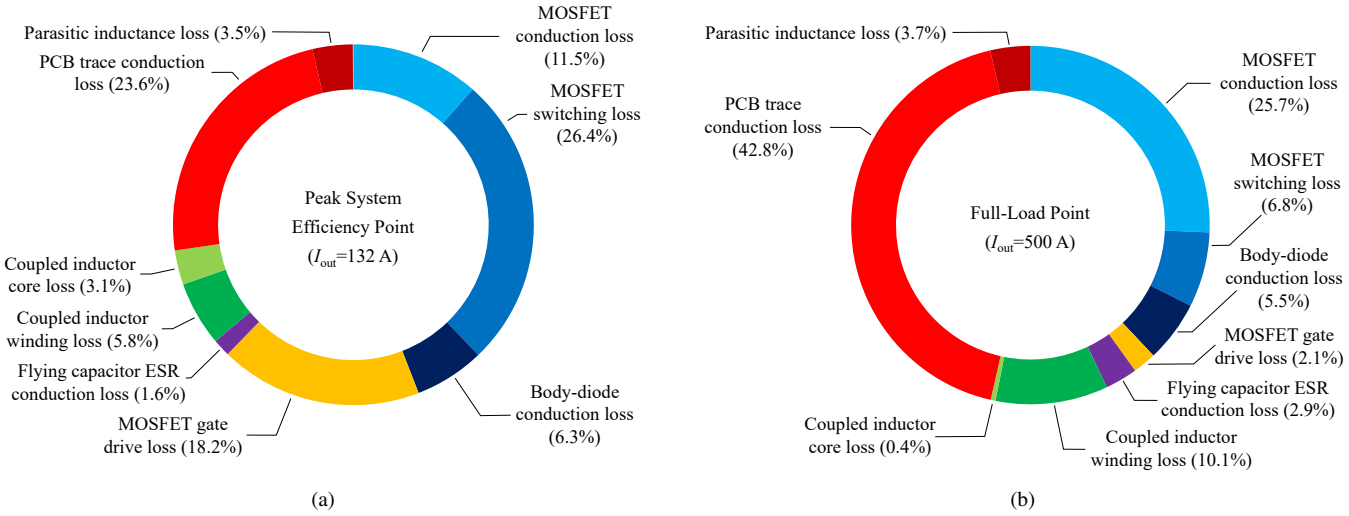


Fig. 20: Loss breakdown of the hardware prototype. (a) Loss breakdown at the peak system efficiency point. (b) Loss breakdown at the full-load point.

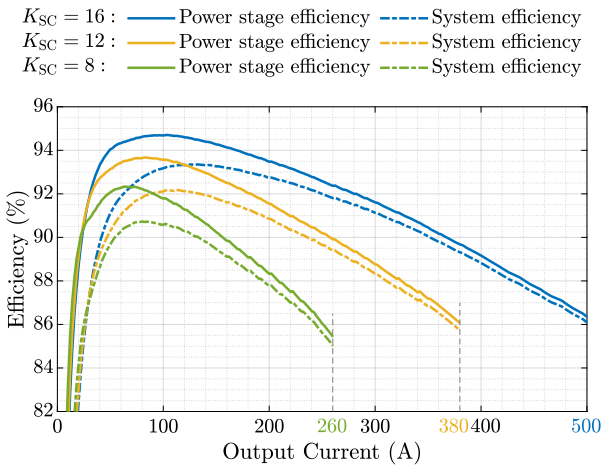


Fig. 21: Measured 48-to-1-V efficiency at different SC stage conversion ratios (K_{SC}).

$\langle i_{CkA/B}\rangle$ $(k = 1,2,\cdots,7)$, and $\langle i_{Cout}\rangle$. According to Kirchhoff's current law (KCL), the average current flowing through the capacitors in Fig. 1 can be expressed as

$$\langle i_{C1}\rangle = D\left(\langle i_{L1A}\rangle - \langle i_{L1B}\rangle\right) \tag{5}$$

$$\langle i_{CkA/B}\rangle = D\left(\langle i_{LkA/B}\rangle - \langle i_{L(k+1)A/B}\rangle\right) \quad (k = 1,2,\cdots,7) \tag{6}$$

$$\langle i_{Cout}\rangle = \sum_{j=1}^{8}\langle i_{LjA}\rangle + \sum_{j=1}^{8}\langle i_{LjB}\rangle - I_{out} \tag{7}$$

where D is the duty ratio, and I_{out} is the output current.

In PSS, the average capacitor currents must be zero, i.e.,

$$\langle i_{C1}\rangle = 0 \tag{8}$$

$$\langle i_{CkA/B}\rangle = 0 \quad (k = 1,2,\cdots,7) \tag{9}$$

$$\langle i_{Cout}\rangle = 0 \tag{10}$$

Substituting (8)–(10) into (5)–(7) yields

$$\langle i_{L1A}\rangle = \langle i_{L2A}\rangle = \cdots = \langle i_{L8A}\rangle = \langle i_{L1B}\rangle = \langle i_{L2B}\rangle = \cdots = \langle i_{L8B}\rangle = \frac{1}{16}I_{out} \tag{11}$$

This implies the output current can be evenly shared among all inductors in the natural equilibrium.

2) Natural Voltage Balancing Mechanism: Denote the average voltages of the inductors and capacitors in the switching bus converter as $\langle v_{LjA/B}\rangle$ $(j = 1,2,\cdots,8)$, $\langle v_{C1}\rangle$, $\langle v_{CkA/B}\rangle$ $(k = 1,2,\cdots,7)$, and $\langle v_{Cout}\rangle$. According to Kirchhoff's voltage law (KVL), the average voltage applied across the inductors in Fig. 1 can be expressed as

$$\langle v_{L1A}\rangle = D\left(V_{in} - \langle v_{C1}\rangle - \langle v_{C1A}\rangle\right) - \langle v_{Cout}\rangle \tag{12}$$

$$\langle v_{L1B}\rangle = D\left(\langle v_{C1}\rangle - \langle v_{C1B}\rangle\right) - \langle v_{Cout}\rangle \tag{13}$$

$$\langle v_{LjA/B}\rangle = D\left(\langle v_{C(j-1)A/B}\rangle - \langle v_{CjA/B}\rangle\right) - \langle v_{Cout}\rangle \quad (j = 2,3,\cdots,7) \tag{14}$$

$$\langle v_{L8A/B}\rangle = D\langle v_{C7A/B}\rangle - \langle v_{Cout}\rangle \tag{15}$$

where V_{in} is the input voltage.

In PSS, the average inductor voltages must be zero, i.e.,

$$\langle v_{L1A}\rangle = 0 \tag{16}$$

$$\langle v_{L1B}\rangle = 0 \tag{17}$$

$$\langle v_{LjA/B}\rangle = 0 \quad (j = 2,3,\cdots,7) \tag{18}$$

$$\langle v_{L8A/B}\rangle = 0 \tag{19}$$

Substituting (16)–(19) into (12)–(15) yields

$$\langle v_{C1}\rangle = \frac{1}{2}V_{in},\ \langle v_{Cout}\rangle = \frac{D}{16}V_{in},\ \langle v_{CkA/B}\rangle = \frac{8-k}{16}V_{in}\ (k = 1,2,\cdots,7) \tag{20}$$

which means the capacitor voltages can naturally balance themselves in the equilibrium.

Equations (11) and (20) show that the balanced state is the natural equilibrium of the switching bus converter in PSS.

It is worth noting that this quantitative analysis is independent of the values of inductors and capacitors. Therefore, the automatic current sharing and natural voltage balancing mechanisms do not rely on component accuracy and can tolerate passive component tolerance, variations, and derating.

B. Qualitative Analysis

Due to a negative feedback mechanism, the switching bus converter can counteract any temporary imbalance in inductor currents and capacitor voltages and restore them to their balanced states. This subsection qualitatively explains the automatic current sharing of inductor $\mathrm{L_{1A}}$ and the natural voltage balancing of capacitor $\mathrm{C_{1A}}$ as examples.

1) Automatic Current Sharing Mechanism: Consider the case where $\langle i_{\mathrm{L1A}}\rangle > \frac{1}{16}I_{\mathrm{out}}$ (the average current through $\mathrm{L_{1A}}$ in the balanced state) and all other inductor currents and capacitor voltages are in their balanced states.

Due to this deviation of $\langle i_{\mathrm{L1A}}\rangle$ from the equilibrium, the average current flowing into $\mathrm{C_1}$ and $\mathrm{C_{1A}}$ in operating modes ① and ② in Fig. 2 will be higher than that flowing out of them in operating modes ④–⑥. As a result, the net charge flowing into $\mathrm{C_1}$ and $\mathrm{C_{1A}}$ in each switching cycle is positive, leading to an increase in $\langle v_{\mathrm{C1}}\rangle$ and $\langle v_{\mathrm{C1A}}\rangle$, which makes $\langle v_{\mathrm{C1}}\rangle > \frac{1}{2}V_{\mathrm{in}}$ and $\langle v_{\mathrm{C1}}\rangle > \frac{7}{16}V_{\mathrm{in}}$. Consequently, the switch-node voltage applied to the left-hand side of $\mathrm{L_{1A}}$ in operating modes ① and ② will be lower than $\frac{1}{16}V_{\mathrm{in}}$ (the voltage applied to the left-hand side of $\mathrm{L_{1A}}$ in the balanced state). This means that $\langle i_{\mathrm{L1A}}\rangle$ will then start to decrease until $\langle i_{\mathrm{L1A}}\rangle = \frac{1}{16}I_{\mathrm{out}}$.

Similarly, if $\langle i_{\mathrm{L1A}}\rangle < \frac{1}{16}I_{\mathrm{out}}$, the net charge flowing into $\mathrm{C_1}$ and $\mathrm{C_{1A}}$ in each switching cycle will be negative, forcing $\langle v_{\mathrm{C1}}\rangle$ and $\langle v_{\mathrm{C1A}}\rangle$ to decrease, which makes $\langle v_{\mathrm{C1}}\rangle < \frac{1}{2}V_{\mathrm{in}}$ and $\langle v_{\mathrm{C1}}\rangle < \frac{7}{16}V_{\mathrm{in}}$. As a result, $\langle i_{\mathrm{L1A}}\rangle$ will increase until $\langle i_{\mathrm{L1A}}\rangle = \frac{1}{16}I_{\mathrm{out}}$.

This negative feedback mechanism applies to other inductor currents as well. In addition, the inductor currents can be evenly shared between the two SCB modules due to this current-voltage interaction through capacitor $\mathrm{C_1}$.

2) Natural Voltage Balancing Mechanism: Consider the case where $\langle v_{\mathrm{C1A}}\rangle > \frac{7}{16}V_{\mathrm{in}}$ (the average voltage across $\mathrm{C_{1A}}$ in the balanced state) and all other inductor currents and capacitor voltages are in their balanced states.

Due to this deviation of $\langle v_{\mathrm{C1A}}\rangle$ from the equilibrium, the switch-node voltage applied to the left-hand side of $\mathrm{L_{1A}}$ in operating modes ① and ② is lower than $\frac{1}{16}V_{\mathrm{in}}$ (the voltage applied to the left-hand side of $\mathrm{L_{1A}}$ in the balanced state). As a result, $\langle i_{\mathrm{L1A}}\rangle$ will decrease below $\frac{1}{16}I_{\mathrm{out}}$. Therefore, the average current flowing into $\mathrm{C_{1A}}$ in operating modes ① and ② will be higher than that flowing out of it in operating modes ④–⑥. Consequently, the net charge flowing into $\mathrm{C_{1A}}$ in each switching cycle will be positive, which forces $\langle v_{\mathrm{C1A}}\rangle$ to increase until $\langle v_{\mathrm{C1A}}\rangle = \frac{7}{16}V_{\mathrm{in}}$.

Similarly, if $\langle v_{\mathrm{C1A}}\rangle < \frac{7}{16}V_{\mathrm{in}}$, $\langle i_{\mathrm{L1A}}\rangle$ will increase beyond $\frac{1}{16}I_{\mathrm{out}}$, causing the net charge flowing into $\mathrm{C_{1A}}$ in each switching cycle to be negative. As a result, $\langle v_{\mathrm{C1A}}\rangle$ will increase until $\langle v_{\mathrm{C1A}}\rangle = \frac{7}{16}V_{\mathrm{in}}$. This negative feedback mechanism applies to other capacitor voltages as well.

In summary, the quantitative analysis proves that the balanced state is the natural equilibrium of the converter in PSS, while the qualitative analysis shows that the converter can counteract any temporary imbalance in inductor currents and capacitor voltages due to the negative feedback mechanism explained above, thereby restoring them to their balanced states. This means that the balanced state is naturally a stable equilibrium of the converter in PSS. Therefore, the inductor currents and capacitor voltages can be naturally balanced in PSS without any active balancing control.

It is worth noting that the above analyses are based on the assumption that the converter operates in the continuous capacitor voltage mode (CCVM). With very large voltage ripples on the flying capacitors, capacitor voltage clamping can occur through the reverse conduction of the switching devices, driving the converter into a discontinuous capacitor voltage mode (DCVM) [52]. In DCVM, inductor currents can no longer be automatically balanced. Instead, a modified duty cycle scheme can be used to recover the inductor current balancing. The discussion of the DCVM operation of the switching bus converter is beyond the scope of this paper.

Appendix B
Analysis and Design of the Two-Phase Coupled Inductor

As a rule of thumb, the peak-to-peak inductor current ripple ($\Delta i_{\mathrm{L,pp}}$) of a buck converter is typically designed to be 20% to 40% of the full-load output current [53]. For the hardware prototype presented in this paper, the inductor current ripple ratio was selected as 25%. Given a per-phase full-load current of 31.3 A, the maximum allowable peak-to-peak inductor current ripple is $\Delta i_{\mathrm{L,pp(max)}} = 25\% \times 31.3 = 7.8$ A. In order to meet this current ripple requirement, the per-phase steady-state inductance should not be lower than

$$L_{\mathrm{ss(min)}} = \frac{(1-D)V_{\mathrm{out}}}{f_{\mathrm{sw}}\Delta i_{\mathrm{L,pp(max)}}}, \tag{21}$$

where D is the duty ratio, V_{out} is the output voltage, and f_{sw} is the switching frequency. In this design, the nominal duty ratio is $D = \frac{1}{3}$, $V_{\mathrm{out}} = 1.0$ V, $f_{\mathrm{sw}} = 150$ kHz, and $\Delta i_{\mathrm{L,pp(max)}} = 7.8$ A. Therefore, $L_{\mathrm{ss(min)}} = 570$ nH. In addition, the height of the coupled inductor was constrained to 5 mm to align with the thickness of the three-layer stacked flying capacitors.

Considering the ripple requirement and height constraint, the two-phase coupled inductor presented in Section III-A was designed. It consists of an E core, an I core, and two windings. Each winding has two turns. The selection of the number of turns can be approached as an integer programming problem. The objective is to minimize the core volume while satisfying the requirements on steady-state inductance, dc resistance of the windings, and saturation current. A lower number of turns contributes to a reduction in the dc resistance and an increase in saturation current. However, it diminishes the steady-state inductance at the same time. Conversely, increasing the number of turns can facilitate achieving the target saturation current but at the cost of increased dc resistance and reduced saturation current. Two turns per winding provided the optimal solution for this prototype, as it achieved a good trade-off among the steady-state inductance, the dc resistance of the windings, and the saturation current.

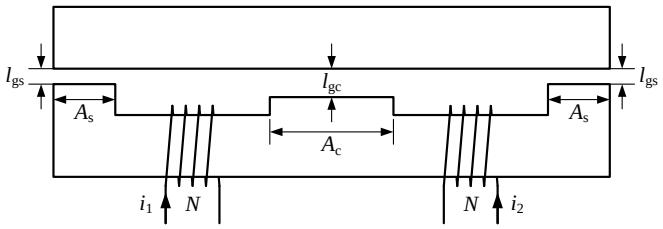


Fig. 22: Core geometry of the two-phase coupled inductor. l_{gs} and l_{gc} are the lengths of the air gap in the side legs and the center leg, respectively. A_s and A_c are the cross-sectional areas of the side legs and the center leg, respectively. The currents in the two windings are i_1 and i_2, respectively. Each winding has N turns. In this design, $N = 2$.

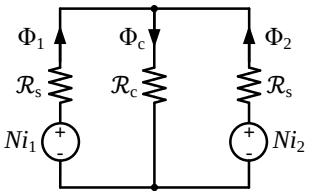


Fig. 23: Magnetic circuit model of the two-phase coupled inductor. $\mathcal{R}_s$ and $\mathcal{R}_c$ are the magnetic reluctances of the side legs and the center leg, respectively. Ni_1 and Ni_2 are the magnetomotive forces (MMFs) applied by the two windings around the cores. Φ_1, Φ_2, and Φ_c are the magnetic fluxes in the side legs and the center leg.

A. Magnetic Circuit Model

Fig. 22 illustrates the core geometry of the two-phase coupled inductor, with its magnetic circuit model shown in Fig. 23. Since the initial relative permeability of the core material (DMR96A [54]) is $\mu_r = 3300$ which is much greater than 1, it is assumed that the magnetic reluctances of the air gap are much higher than those of the cores. Therefore, the reluctances of the side legs and the center leg are dominated by the air-gap reluctances and can be approximated as

$$\mathcal{R}_s = \frac{l_{gs}}{\mu_0 A_s} \tag{22}$$

$$\mathcal{R}_c = \frac{l_{gc}}{\mu_0 A_c} \tag{23}$$

where μ_0 is the permeability of vacuum, l_{gs} and l_{gc} are the lengths of the air gap in the side legs and the center leg, respectively, and A_s and A_c are the cross-sectional areas of the side legs and the center leg, respectively. In this design, $l_{gs} = 0.0254$ mm (1 mil), $l_{gc} = 0.3054$ mm, $A_s = 10$ mm^2, and $A_c = 20$ mm^2. Therefore, the side-leg and center-leg reluctances are $\mathcal{R}_s = 2.02 \times 10^6$ H^{-1} and $\mathcal{R}_c = 1.22 \times 10^7$ H^{-1}, respectively.

Based on this magnetic circuit model, the self and mutual inductances of the coupled inductor can be obtained as

$$L = \frac{N^2 (\mathcal{R}_s + \mathcal{R}_c)}{\mathcal{R}_s (\mathcal{R}_s + 2\mathcal{R}_c)} \tag{24}$$

$$M = -\frac{N^2 \mathcal{R}_c}{\mathcal{R}_s (\mathcal{R}_s + 2\mathcal{R}_c)} \tag{25}$$

which yields $L = 1066$ nH and $M = -914$ nH.

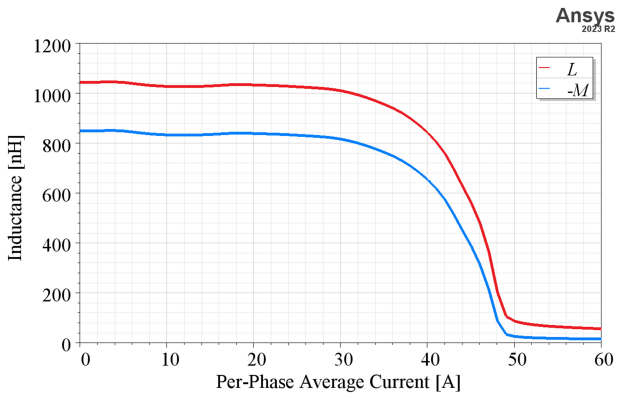


Fig. 24: Self and mutual inductances of the two-phase coupled inductor obtained from Ansys FEM simulation.

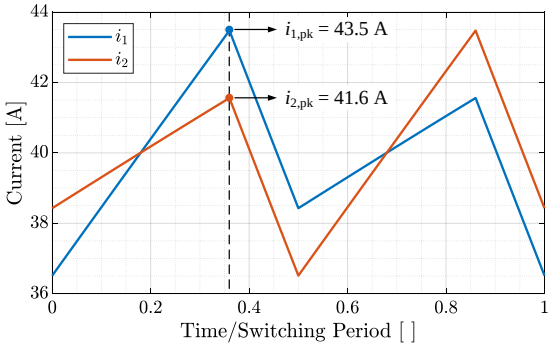


Fig. 25: Current waveforms of the coupled inductor at a per-phase average current of 40 A (the designed saturation current). The waveforms were obtained from circuit simulation with $L = 1040$ nH and $M = -840$ nH. The magnetic cores are most prone to saturation when the current in one phase reaches its peak value, as annotated with the dashed line. The corresponding winding currents are $i_{1,pk} = 43.5$ A and $i_{2,pk} = 41.6$ A.

B. Simulation Results

Fig. 24 shows the self and mutual inductances of the two-phase coupled inductor obtained from Ansys FEM simulation. It can be seen that the self and mutual inductances at 0-A per-phase average current are $L = 1040$ nH and $M = -840$ nH, which align well with the values calculated from the magnetic circuit model. It is reasonable that the calculated values are slightly higher than the simulated values since the core reluctances are ignored in the model. The steady-state inductance can be calculated as

$$L_{ss} = \frac{L^2 - M^2}{L + \frac{D}{D'} M} \tag{26}$$

which yields $L_{ss} = 606$ nH. Since $L_{ss} > L_{ss(min)} = 570$ nH, this design can satisfy the current ripple requirement. In addition, it can also be observed from Fig. 24 that the inductances drop sharply when the per-phase average current is above 40 A which is the designed saturation current of this coupled inductor.

Fig. 25 illustrates the current waveforms of the coupled inductor at a per-phase average current of 40 A (the designed saturation current). The magnetic cores are most prone to saturation when the current in one phase reaches its peak value. At this moment, the sum of and the difference between the two

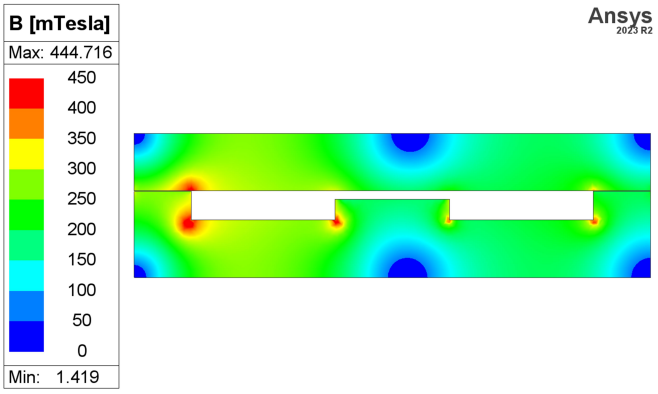


Fig. 26: Magnitude of flux density on the cross-section of the cores at a per-phase average current of 40 A (the designed saturation current). In this FEM simulation, the current in the left-hand side winding is 43.5 A and the current in the right-hand side winding is 41.6 A.

currents simultaneously reach their peaks, thereby maximizing the magnitude of flux density in the cores. Fig. 26 shows the magnitude of flux density on the cross-section of the cores at this moment, where $i_{1,\mathrm{pk}} = 43.5$ A and $i_{2,\mathrm{pk}} = 41.6$ A. The saturation magnetic flux density of the core material (DMR96A) at 100°C is 430 mT. As can be observed in Fig. 26, only a small portion of the magnetic cores saturate. This demonstrates that the coupled inductor is able to handle the target saturation current of 40 A.

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