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A K-Band High Power and High Isolation Stacked-FET Single Pole Double Throw MMIC Switch Using Resonating Capacitor

Duy P. Nguyen, *Student Member, IEEE*, Anh-Vu Pham, *Senior Member, IEEE* and Farshid Aryanfar

***Abstract* — A K-band monolithic microwave integrated circuit (MMIC) transmit and receive (T/R) single pole double throw (SPDT) switch with low insertion loss, high isolation and ultra-high output power is demonstrated using 0.15-µm Gallium Arsenide (GaAs) technology. A shunt field effect transistor (FET) configuration is used to provide low insertion loss and high isolation while the stacked-FET is employed to improve power handling capability. The novel GaAs switch exhibits a minimum measured insertion loss of 1.4 dB and less than 2.5 dB from 22 GHz to 26 GHz as well as 44 dB isolation. The measured input 1-dB power compression point (P_{1dB}) exceeds 4 Watts.**

***Index Terms*—T/R switch, stacked-FET, K-band, Gallium Arsenide, MMIC.**

I. Introduction

K-band systems have been found in variety of applications such as: satellite, radar and digital point-to-point radio services [1]. These systems demand a low loss, high isolation and high power SPDT switches. Although PIN diode switches can handle high power due to their high breakdown voltage [2], they are not monolithically compatible with other devices in a front-end module and consume high dc current. On the other hand, GaAs MMIC switches are not only more attractive in a fully integrated system but they also consume very little DC power. A pseudomorphic high-electron-mobility transistor (pHEMT) GaAs MMIC switch has a much higher switching speed than the PIN diode one [3]. The major issues of a GaAs T/R switch are low isolation at high frequency and limited power handling capability due to the gate-drain parasitic capacitance C_{gd} and relatively low breakdown voltage of the GaAs technology.

Several techniques have been introduced to improve GaAs MMIC switch isolation and power handling capability. In [4], authors used the ohmic-electrode-sharing technology for a Ka-band switch; however, the design gives only 20.6 dB isolation in a conventional series-shunt topology. The impedance transformation switch was introduced in [5] to improve the isolation to 30 dB. Parasitic cancelling switch was proposed in [6] to enhance isolation at Ka-band and 28.9 dB isolation was reported. In all three designs, the power is limited to only 21 dBm. A multiple stacked-FET switch was introduced in [2,7] to enhance output power at high frequency. In [2], a stacked metal–semiconductor field effect transistors (MESFET) switch achieved 31 dBm output power but had low isolation due to the increasing on-resistance.

In this paper, we present the design and development of a novel dual shunt stacked-FET T/R switch. The switch employed a stacked-FET topology to enhance power handling capability and a resonating capacitor to achieve high isolation

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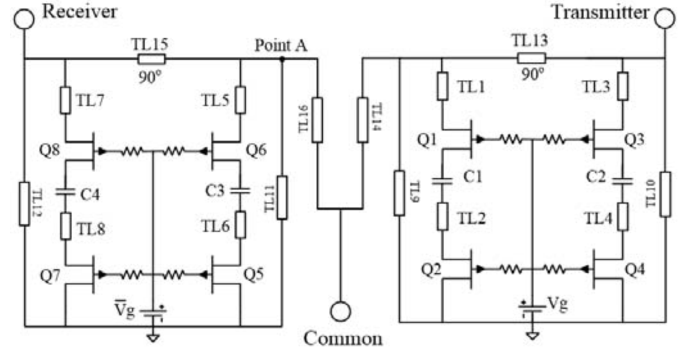

Fig. 1. Schematic diagram of the proposed stacked-FET switch

The switch fabricated in a 0.15-µm GaAs pHEMT process TQP15 from Qorvo exhibits 2.5 dB insertion loss and better than 44 dB isolation from 22 GHz to 26 GHz. The measured input P_{1dB} is 36 dBm over the frequency range. This is the first time a resonating capacitor is used to enhance isolation of a high power stacked-FET switch. To the best of our knowledge, our proposed switch has the highest P1dB of all reported GaAs MMIC switch at K-band.

II. Circuit Design

Fig. 1 shows the configuration of the proposed dual shunt stacked-FET switch. The transmitter (T_x) and receiver (R_x) arms are symmetrical. Each arm consists of four pHEMTs to form a stacked-FET dual-shunt topology. In the T_x arm, the transistor Q_1 is placed on top of Q_2 to form a stack connection. A large resistor is put at the gate of each transistor to allow some voltage swings at this node. Similar connections are applied to Q_3, Q_4 as well as the R_x arm. When the T_x arm is on (T_x and Common is a thru path), all the transistors Q_1, Q_2, Q_3 and Q_4 would be turned off by setting their bias voltage below the pinch-off value. At the same time, Q_5, Q_6, Q_7 and Q_8 would be turned on to isolate the signal at the receiver arm. C1-C4 are the resonating capacitors which are employed in our novel design to enhance isolation.

A. Resonating capacitor for high isolation design

When a pHEMT is used in a switching application, it can be modelled as a small resistor when being turned on (R_{on}) or a large capacitor when being turned off (C_{off}). Fig. 2a shows the equivalent circuit of Q3 and Q4 being turned off and Q7 and Q8 being turned on. The key point to enhance the switch isolation is the use of dual-shunt topology. During operation, the isolation port (bottom half of Fig. 2a) would be connected to the ground through a very small resistance. The 90° TL16 transforms the low impedance at point A in Fig. 1 to the high impedance presenting at the common node while the 90° TL15 isolates the turned-off port from the leakage signal coming from the common node to further reinforce the switch isolation. Compared to the conventional series-shunt topology

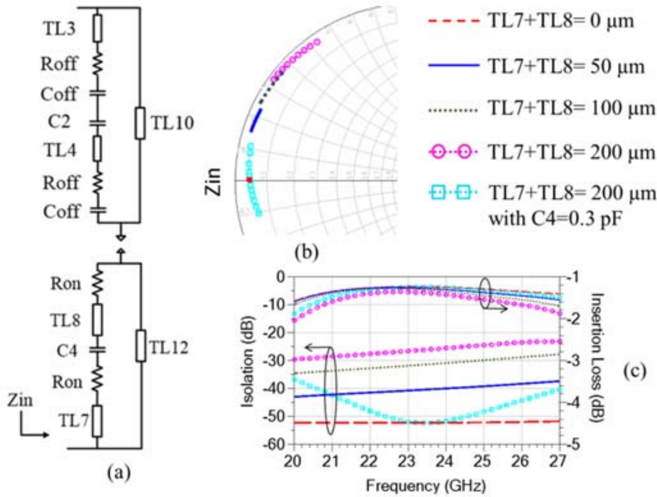

Fig. 2. Switch equivalent circuit during operation (a); input impedance of the turned off arm (b) and isolation with different TL lengths (c)

in [4,6], the isolation of our approach is increased by at least 15 to 20 dB. At high frequency, the connecting transmission lines TL7, TL8 will dramatically change the impedance Z_{in}. Fig. 2b shows the Z_{in} for various lengths of TL7+TL8. When the input impedance looking into the transistor deviates from the real axis, the isolation is significantly degraded. Fig. 2c shows the simulated isolation of the circuit when the total length of the TL7 and TL8 varies from 0 μm to 200 μm. When the total length (TL7+TL8) is large, the isolation is degraded up to 30 dB and the insertion loss also increases (Fig. 2c). In a stacked-FET layout (Fig. 4), the minimum required length of TL7 and TL8 is 200 μm to avoid the overlaps of two FETs and the input line and the top FET. To increase isolation, we propose to add a resonating capacitor C_4 (C_4 = 0.3 pF in our design) to bring the impedance back to the real axis (Fig. 2b). As a result, we can retrieve excellent isolation and insertion loss in the frequency band of interests.

B. Stacked-FET Configuration

A major issue of GaAs MMIC switches is the power handling capability. The gate-drain breakdown voltage of the 0.15-μm GaAs FET is ~12 V which limits the maximum RF voltage swing. We propose a stacked-FET configuration to overcome this issue. Fig. 3 shows a stacked-FET configuration which consists of two identical pHEMT transistors with equal gate bias voltage and bias resistors. Assume that the relative position of the gate to drain and gate to the source are symmetrical; then C_{gd} and C_{gs} would be equal and form a voltage divider at each transistor. If the gate bias resistors are large enough to ensure adequate isolation between the two gates, the voltage swing will be equally divided between the two transistors. Therefore, the voltage swing across C_{gd1}, C_{gs1}, C_{gd2} and C_{gs2} would be identical and equal to the total RF voltage swing divided by 4 (Fig. 3).

Let's denote the pinch off voltage, gate-drain breakdown voltage and peak to peak RF voltage swing are $V_{pinch\text{-}off}$, $V_{break\text{-}down}$ and V_{RF}, respectively. With the above analysis, the peak voltage swing across drain-gate and gate-source of each transistor will be $V_{RF}/4$ and it swings around the DC bias voltage at the gate. On the positive half cycle, if the gate-source voltage swing goes higher than the pinch-off voltage,

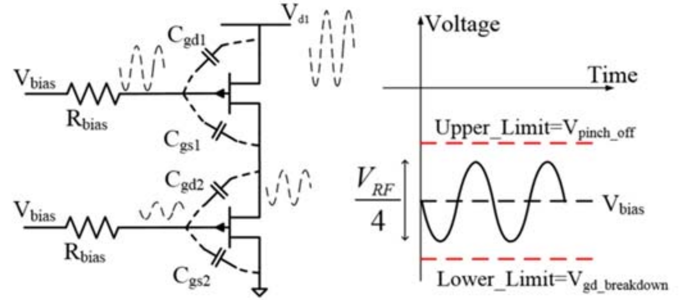

Fig.3. Stacked-FET configuration and voltage swing limitation

the FET will be gradually switched on and compression occurs. On the negative half cycle, if the voltage swing goes lower than the gate-drain breakdown voltage, compression will also occur. The maximum voltage swing is then given by

$$|V_{Bias} - V_{Breakdown}| \leq \frac{V_{RF}}{4} \leq |V_{Pinchoff} - V_{Bias}| \quad (1)$$

For a depletion mode pHEMT process, V_{bias}, $V_{pinchoff}$ and $V_{breakdown}$ defined in (1) are negative values. Based on (1), there is a value of V_{bias} which can maximize the voltage swing limitation. This optimal value of bias voltage is derived as

$$V_{Bias_opt} = \frac{V_{Breakdown} + V_{Pinchoff}}{2} \quad (2)$$

Then, the maximum power for a given bias voltage is

$$P_{max} = \frac{V_{RF}^2}{2Z_0} = \frac{8\left[\min(|V_{Bias} - V_{Breakdown}|, |V_{Pinchoff} - V_{Bias}|)\right]^2}{Z_0} \quad (3)$$

At high input power, the large voltage swing can make the gate-drain voltage to exceed the transistor breakdown voltage and cause device failures. To guarantee safe operations, the typical bias voltage is chosen 1 V back-off from its optimal value. From (3), when $V_{breakdown}$= 12 V, $V_{pinch\text{-}off}$=-1 V and V_{bias}= -5 V, the highest input power that the switch can handle without any compression is 2.56 Watts. Hence, the P_{1dB} is expected to be 2 to 3 dB higher than this power level.

III. EXPERIMENTAL RESULTS

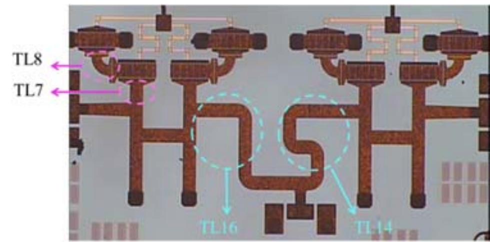

Fig. 4. Chip photo of the fabricated switch (2.6 mm x 1.2 mm)

The chip size is 2.6 mm x 1.2 mm. The transistor size is 720 μm. Gate bias resistors are chosen to be 1 KΩ and are realized on-chip. The resonating capacitors are realized by two metal-insulator-metal (MIM) cap in series. Two lines TL14 and TL16 in Fig. 1 are realized asymmetrically in the layout to save the die area. Intensive electromagnetic (EM) simulation was done to ensure the two transmission lines have equal effective electrical length. The switch was measured using a Keysight network analyzer PNA-X (N5247A) with on-wafer probing and TRL calibration. DC supplies are provided through board traces which are wire-bonded to the chip DC pads. The power measurement was performed with the input signal driven by a high power amplifier.

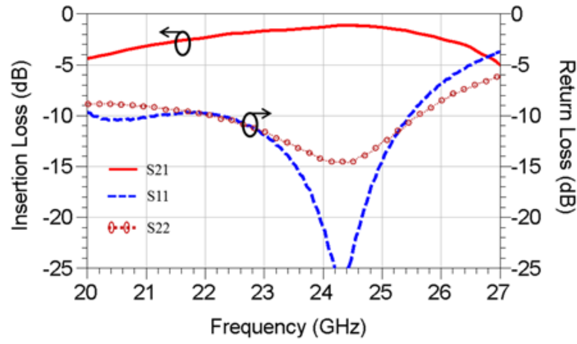

Fig. 5. Measured S-parameter at $\overline{Vg}$=0 V and Vg= -5 V

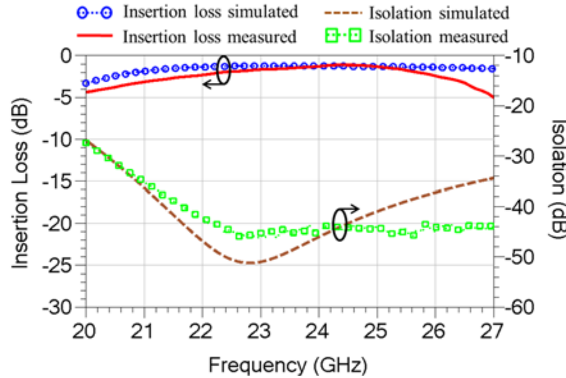

Fig. 6. Simulated versus measured insertion loss and isolation

Fig. 5 shows measured S-parameters of the proposed switch at $\overline{Vg}$=0 V and Vg=-5 V. The minimum insertion loss is 1.4 dB at 24.5 GHz. The switch exhibits less than 2.5 dB insertion loss, better than 10 dB return loss from 22 GHz to 26 GHz.

Fig. 6 demonstrates the insertion loss and isolation of the switch where the experimental results are compared to the full wave electromagnetics simulated results. The measured isolation is better than 44 dB from 22 GHz to 26 GHz. Experimental results are well correlated with the simulated ones in the frequency range. When we reverse the control signals of the SPDT switch, a similar response is recorded since the switch is symmetrical. When the bias voltage is swept from -4 V to -6 V, small signal response is maintained almost the same with a slight change in return loss.

Fig. 7 shows the output power and insertion loss of the switch at 0 V/ -5 V gate bias and at 24.5 GHz. The switch exhibits only 0.25 dB insertion loss degradation at 34 dBm input power. The measured power agrees with our calculation in (3). The measured input P_{1dB} is 36 dBm. Similar compression behaviour is also observed at 22 GHz and 26 GHz. Fig. 8 presents the compression behaviour of the switch at 24.5 GHz at different bias conditions. The bias voltage V_g = -6 V gives the best response and the V_g= -4 V gives the worst response of all three as expected. Table I compares our work with other GaAs MMIC switches at the same frequency range.

IV. Conclusion

We demonstrate a SPDT T/R MMIC switch using a dual-shunt topology with a resonating capacitor stacked-FET configuration in a 0.15-µm GaAs process. Our experimental results demonstrate 2.5 dB insertion loss, 44 dB isolation and 36 dBm input P_{1dB} from 22 GHz to 26 GHz. Our switch has the highest P_{1dB} among all reported GaAs MMIC T/R switch at K-band.

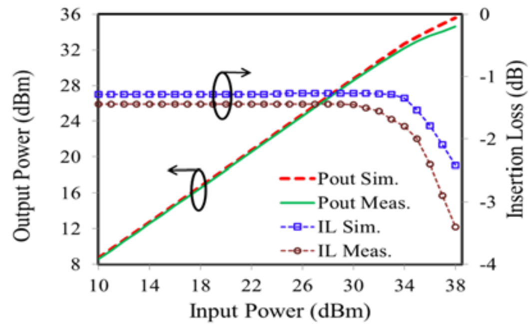

Fig. 7. Output power and insertion loss at 24.5 GHz and 0 V/-5 V bias

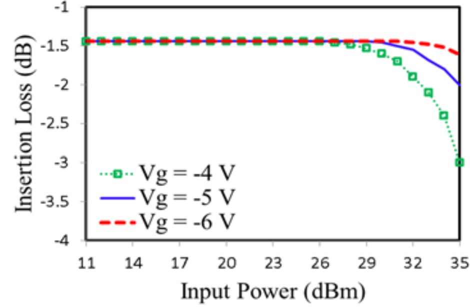

Fig. 8. Output power and insertion loss at 24.5 GHz and 0 V/-5 V bias

TABLE I
COMPARISON TO PREVIOUS WORK

Ref	Freq (GHz)	Ins. Loss (dB)	Isolation (dB)	P1dB (dBm)	Chip size (mm^2)
[2]	21-27	2	20	30	4.47
[3]	20-40	2	25	23	1.61
[4]	DC-60	1.64	20.6	21	0.55
[5]	38-45	2	30	19	2
[6]	18-28	3.1	28.9	NA	2.18
[8]	DC-60	3	25	27.5	1
This work	**22-26**	**2.5**	**44**	**36**	**3.12**

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