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Design and Fabrication of Optically Pumped Hybrid Silicon-AlGaInAs Evanescent Lasers

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Abstract—We present the design and fabrication of a novel laser structure, the hybrid silicon evanescent laser. This structure utilizes offset AlGaInAs quantum wells (QWs) bonded to a silicon waveguide. With this structure, the optical mode is predominantly confined in the passive silicon waveguide and is evanescently coupled to the AlGaInAs strained QWs. The optimal design of the optical waveguide for delivering sufficient optical gain to reach the lasing threshold, while confining most of the optical mode in the silicon waveguide, for efficiently coupling the output power into silicon passive devices, is described. The silicon waveguide is fabricated on a silicon-on-insulator (SOI) wafer using a CMOS-compatible process, and is subsequently bonded with the AlGaInAs QW structure using low temperature O_2 plasma-assisted wafer bonding. We demonstrate optically pumped silicon evanescent lasers operating continuous wave (CW) up to 60 °C. The lasers emit a wavelength of 1.5 μm with a minimum threshold of 23 mW and a maximum single-sided fiber-coupled CW output power of 4.5 mW at the room temperature.

Index Terms—Semiconductor lasers, silicon-on-insulator technology.

I. INTRODUCTION

SILICON is an attractive material for a photonics platform because it is transparent at the communication wavelengths of 1.3 and 1.5 μm and it is pervasive in the integrated electronics industry. Silicon is inefficient for light generation, and this has been the major hurdle for the realization of an electrically pumped laser on silicon, a key element for photonic integrated circuits. Raman lasers and amplifiers [1], [2] have an advantage that optical gain is achieved in pure silicon crystals, but they require an external laser source. Another promising approach, namely, materials engineered silicon structures, includes porous silicon [3], nanocrystalline-silicon [4], SiGe quantum cascade structures [5], dislocation-engineered silicon [6] and erbium doped SiO_2 [7], and nano-paterning of silicon [8]. However, these achievements are still far from the performance and quality needed for commercial applications such as telecommunication and optical interconnects. There have also been several efforts to integrate active materials heterogeneously on silicon substrates.
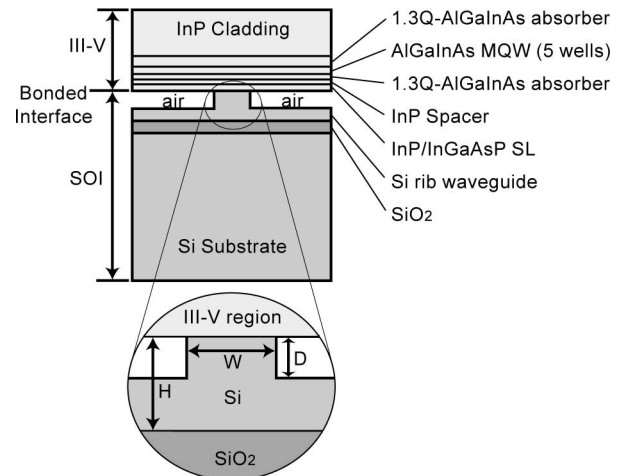
Fig. 1. Device structure.

Recently, we demonstrated a new approach, the hybrid silicon evanescent laser [9], employing a hybrid structure with AlGaInAs offset quantum wells (QWs) bonded to silicon rib waveguides. Modal confinement can be manipulated by changing the silicon waveguide dimensions, which enables easy coupling to other passive photonic devices. In this paper, we present the detailed design, fabrication, and the experimental characterization of optically pumped hybrid silicon evanescent lasers. In Section II, the device structure is introduced, and design issues focused on transverse confinement factors with various waveguide dimensions are also investigated. In Section III, the device fabrication process is described. Section IV presents the performance and characteristics of fabricated silicon evanescent lasers. Finally, future applications and modifying the device structure to electrically pumped active photonic devices are discussed in Section V.

II. DEVICE STRUCTURE AND DESIGN

A. Device Structure

The device structure is shown in Fig. 1. The device is divided into two regions: the silicon-on-insulator (SOI) passive-waveguide structure and the III–V active region that provides the optical gain. The SOI structure consists of a Si substrate, a SiO_2 lower cladding layer, and a Si rib waveguide with a height (H), rib-etch depth (D), and the waveguide width (W). The III–V region consists of an InP spacer/superlattice (SL), AlGaInAs QWs/separated confinement heterostructure (SCH), and InP upper cladding.

TABLE I
III–V Epitaxial Growth Layer Structure

Name	Composition	Thickness
Cladding	InP	4 μm
Absorber (SCH)	$Al_{0.131}Ga_{0.34}In_{0.528}As$, 1.3Q	500 nm
Quantum Wells	$Al_{0.089}Ga_{0.461}In_{0.45}As$, 1.3Q (6x)	10 nm
	$Al_{0.055}Ga_{0.292}In_{0.653}As$, 1.5Q (5x)	7 nm
Absorber (SCH)	$Al_{0.131}Ga_{0.34}In_{0.528}As$, 1.3Q	50 nm
Spacer	InP	110 nm
Super Lattice	$In_{0.85}Ga_{0.15}As_{0.327}P_{0.673}$, 1.1Q (2x)	7.5 nm
	InP (2x)	7.5 nm
Bonding Interface	InP, N type (10^{18} cm^{-3})	10 nm

B. Active Region Design

The epitaxial layer structure of the III–V region is summarized in Table I. The active region consists of five 7-nm-thick $Al_{0.055}$ $Ga_{0.292}$ $In_{0.653}$ As QWs under compressive strain (0.85%) and 10-nm-thick $Al_{0.089}$ $Ga_{0.461}$ $In_{0.45}$ As barriers under tensile strain (–0.55%). The barrier layers have a bandgap corresponding to a wavelength of 1.3 μm.

Unstrained 1.3-μm bandgap quaternary (1.3Q) $Al_{0.131}$ $Ga_{0.34}$ $In_{0.528}$ As SCH layers are placed on both sides of the QWs. The upper and lower SCH layer thicknesses are 0.5 and 0.05 μm, respectively. These layers increase pump power absorption and consequently increase the carrier flow into the QW region. An upper SCH thickness of 0.5 μm is chosen to be less than the diffusion length of 5 μm in AlGaInAs such that most of the generated carriers in this layer diffuse into the QWs before recombination. A two period InP/1.1Q $In_{0.85}$ $Ga_{0.327}$ $As_{0.673}$ P SL is employed below the 110-nm-thick InP spacer layer. The SL region has 7.5-nm-thick alternating layers of InP/InGaAsP to inhibit the propagation of defects from the bonded interface to the QW region [10]. Finally, a 10-nm-thick InP spacer is used as a bonding interface to silicon and is n-doped with a concentration of 10^{18} cm^{-3}. The band diagram is shown in the upper part of Fig. 2. It is calculated by Simwindows [11], a one-dimensional (1-D) drift-diffusion simulator. The bonded interface between the III–V and silicon materials is neglected in calculations, but would result in additional band bending or distortion near the interface in real situations depending on the thickness of the interfacial layer.

C. Hybrid Waveguide Design and Confinement Factors

The lower part of Fig. 2 shows the index profile of the hybrid waveguide. The index of each epi layer is calculated from the relative dielectric constants for strained layers [12] using material parameters of AlGaInAs that are interpolated by Vegard's law with binary material parameters of InAs, AlAs, and GaAs [13]. The index of the QW region and the absorber region is calculated to be 3.53 and 3.45, respectively, at 1550 nm. The index of the QW region is averaged using total length of barriers and QWs [14]. The index of SL region is assumed to be the same as InP index since InGaAsP layer is too thin to affect the optical mode property.

The confinement factors in the QW region (Γ_{QW}) and the silicon waveguide (Γ_{Si}) are calculated using the Beamprop mode solver. Γ_{QW} is a critical design parameter in order to achieve
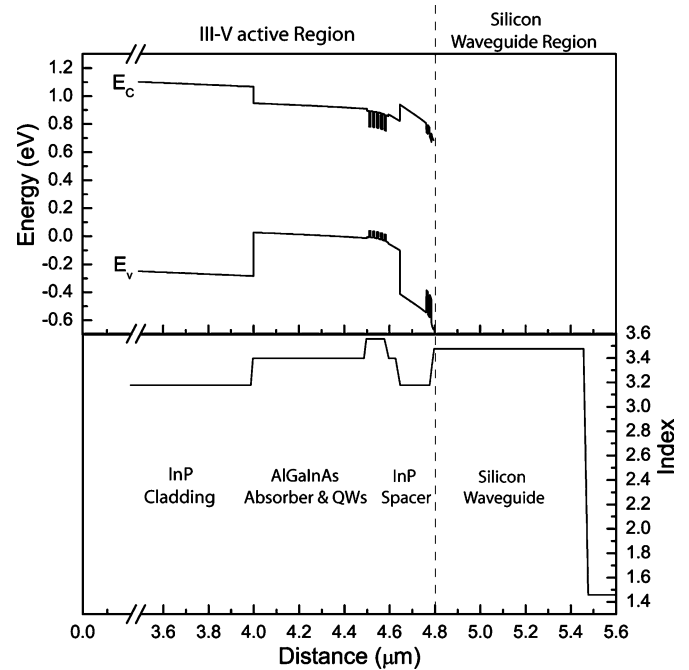

Fig. 2. III–V active region band diagram and index profile.

lasing threshold, which occurs when the modal gain is greater than the total losses. Fig. 3 shows the effect of rib waveguide width and height on Γ_{QW} and Γ_{Si}. In general, when W is small, most of the optical mode is in the III–V region. As W becomes larger the optical mode becomes more confined to the silicon waveguide. The behavior for the waveguide height follows the same trend, where smaller heights yield more optical mode in the III–V region and larger heights yield more optical mode in the silicon region.

Fig. 4 shows Γ_{Si} and Γ_{QW} for the fabricated device dimensions H and D of 0.7 and 0.6 μ m, respectively. Γ_{Si} is varied from 5% to 41% with waveguide width variation of 1–5 μm and correspondingly, the Γ_{QW} are varied from 5.1% to 4.1% for five QWs.

The calculated transverse mode profiles are shown in Fig. 5. It can be clearly seen that most of the optical mode is confined in the silicon region of the wider silicon waveguides [Fig. 5(d)], while it is confined in the III–V region of the narrower silicon waveguides [Fig. 5(a)] as mentioned before.

III. FABRICATION

The silicon rib waveguide is fabricated on the (1 0 0) surface of a lightly p-doped (doping concentration $< 2 \times 10^{15}$ cm^{-3}) SOI substrate by standard photolithography and reactive ion etching (RIE) plasma of Cl$_2$/HBr/Ar. A thin layer of SiO$_2$ is used as a hard mask. The SOI wafer and the III–V epitaxial wafer are treated by buffered HF and NH$_4$OH, respectively, after a thorough cleaning procedure using acetone, isopropanol, and deionized water. The two samples are bonded together via oxygen-plasma-assisted bonding. After a
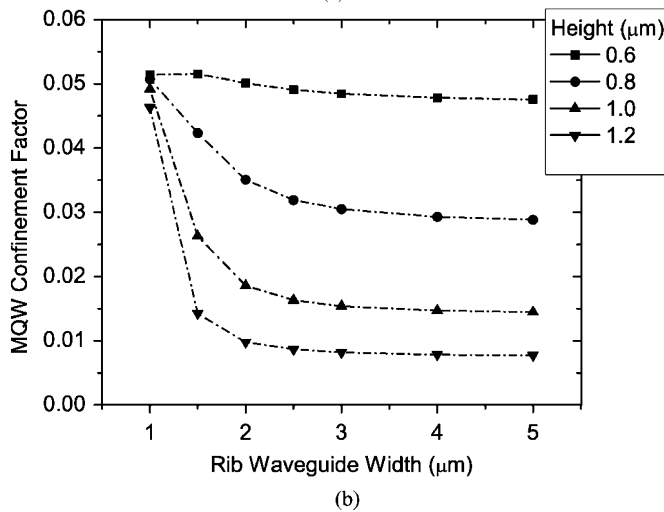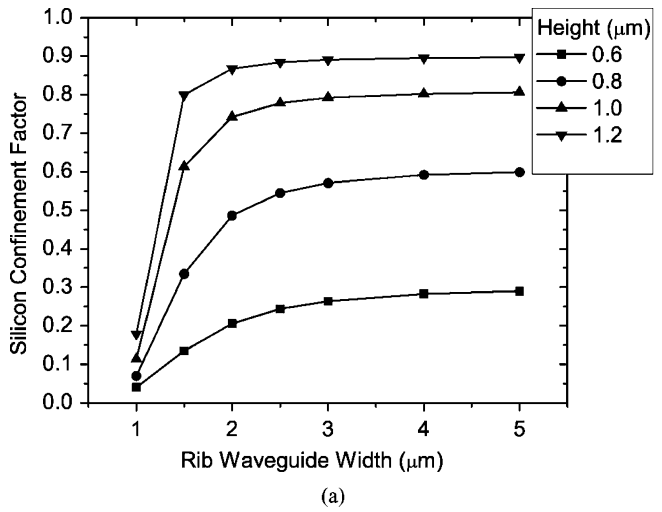
(a)

(b)

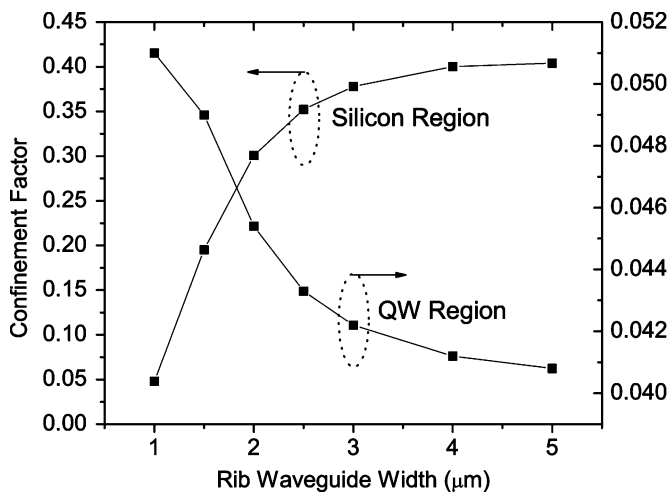Fig. 3. Calculated confinement factors. (a) Silicon waveguide region. (b) III–V QW region.

Fig. 4. Calculated confinement factors of fabricated devices.
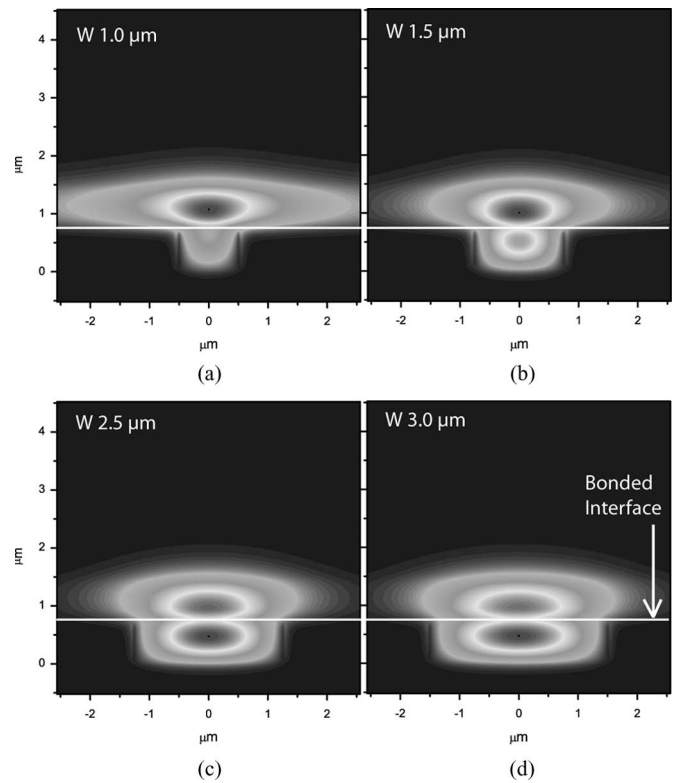

Fig. 5. Calculated mode profiles with several different waveguide widths of fabricated devices. The waveguide height (H) and rib-etch depth (D) are 0.7 and 0.6 μm, respectively, and the waveguide widths are (a) 1.0 μm, (b) 1.5 μm, (c) 2.5 μm, and (d) 3.0 μm.
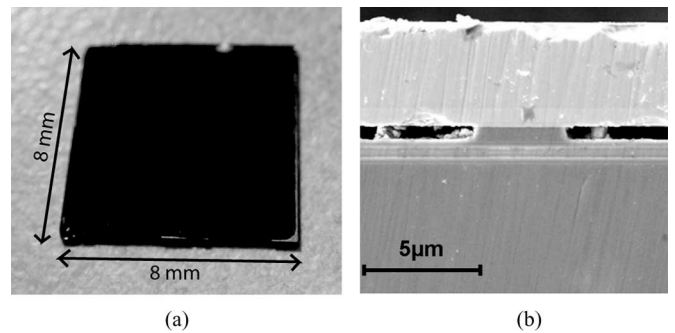

Fig. 6. (a) $8 \times 8 \text{mm}^2$ bonded section. (b) SEM image of device cross section.

the facets are coated with a broadband dielectric high reflectance (HR) coating consisting of three periods of $SiO_2/Ta2O_5$ with a reflectivity of approximately 80%. The final device length after dicing and polishing is 800 μm. An image of an 8×8 mm^2 bonded sample after InP substrate removal is shown in Fig. 6(a). The bonded layer is continuous across the entire sample and is robust enough to stand up to dicing and polishing of the facets. Fig. 6(b) shows a scanning electron microscope (SEM) image of the fabricated device cross section. The particles on the facet surface are due to the polishing process.

The thermal expansion coefficient mismatch between Si $(2.6 \times 10^{-6} \text{ K}^{-1})$ and InP $(4.8 \times 10^{-6} \text{ K}^{-1})$ can introduce cracks for temperatures above 300 °C for Si and InP substrate

low-temperature anneal (~ 300 °C), the InP substrate is removed with HCl, followed by the InGaAs etch stop layer removal with $H_2O:H_2O_2:H_3PO_4$ (1:1:38). The devices are diced, the facets are polished, and the devices are characterized. Finally,
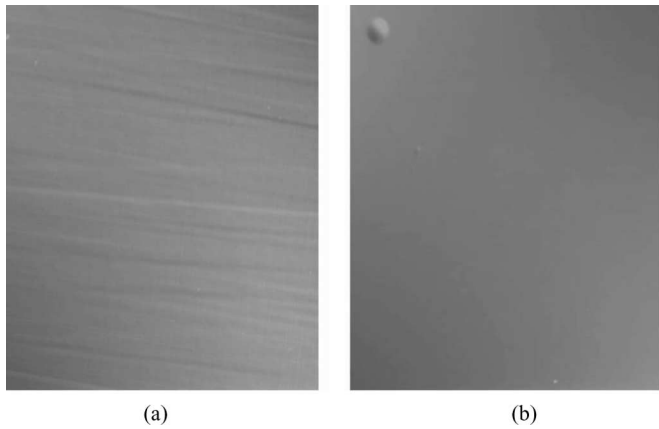
Fig. 7. Nomarski images of III–V epi-surface after bonding and subsequent InP substrate removal. (a) Annealed at $600\,°C$. (b) Annealed at $250\,°C$ after oxygen plasma treatment.

thicknesses of 500 and 350 μm, respectively. Fig. 7(a) shows the Nomarski microscope surface image of III–V epi layers bonded to a SOI substrate through direct wafer bonding at $600\,°C$. Surface deformation can be seen clearly in this picture, while low temperature oxide mediated bonded samples show smooth surfaces after the bonding [Fig. 7(b)]. The oxygen plasma treatment generates a thin oxide layer (<5 nm), whose surface is very smooth and highly chemically reactive [15]. As a result, this bonding process creates a thin oxide layer at the bonded interface; this does not significantly alter the optical mode because it is very thin and optically transparent.

IV. EXPERIMENTAL RESULTS

The devices are optically pumped perpendicular to the laser by a 1250-nm fiber laser. The light from the pump laser is focused by a cylindrical lens illuminating a 12 by 916 μm rectangular spot incident on the device through the top InP cladding layer. For the purpose of comparison, the incident pump power reaching the device is determined by factoring out the reflected pump power and calculating the overlap of the pump beam with the laser mode. The power reflectivity from the bonded wafer at 1250 nm is 40%, and the laser mode is calculated by the length of the cavity multiplied by the computed mode widths. The laser output is collected with a multimode fiber from the waveguide and subsequently characterized using a spectrum analyzer or photodetector. The fiber coupling efficiency is found to be –5 dB. The TE/TM near-field images of the output mode are recorded on an IR camera through a polarizing beam splitter and an $80\times$ lens at the opposite waveguide facet.

The devices are fabricated with a length of 800 μm. Uncoated devices are tested before HR coating and they lase continuous wave (CW) up to $35\,°C$. At $20\,°C$, the maximum power coupled into a single mode fiber is 11 mW. The performance of HR coated devices will be discussed through the rest of this section.

Fig. 8 shows the laser output power as a function of pump power and temperature for two different waveguide widths of 4 and 1 μm. In Fig. 8(a), a 4-μm-wide device is operating with a threshold pump power of 23 mW with a fiber-coupled maximum
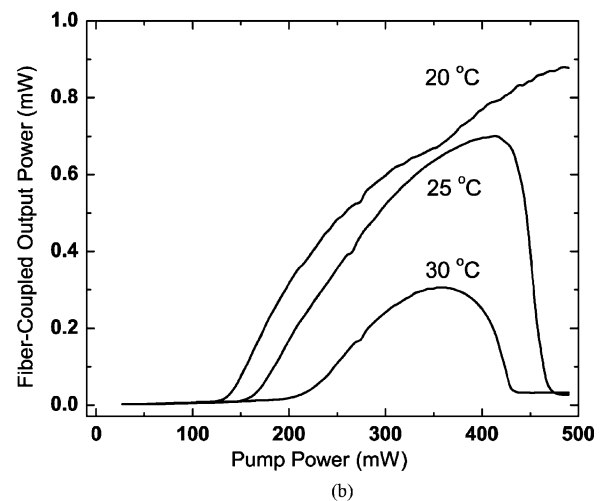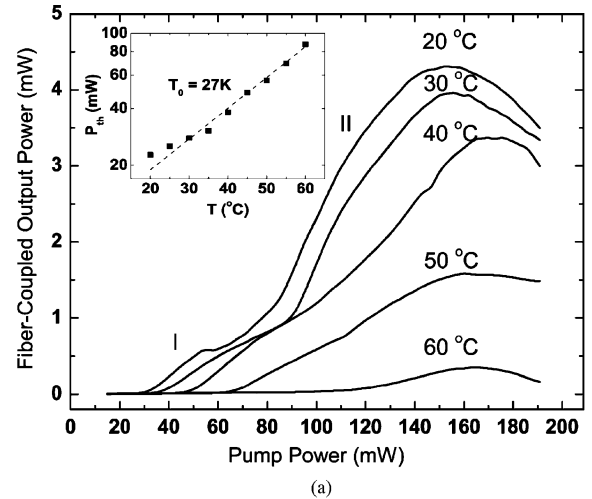

Fig. 8. LL curves. (a) 4-μm-wide, 800-μm-long device. (b) 1-μm-wide, 800-μm-long device.

output power of 4.5 mW and a slope efficiency of 3% at $20\,°C$. The total maximum output power, taking into account the light from both facets and the coupling losses of 5 dB, is approximately 28 mW and the corresponding slope efficiency is 16%. The threshold increases from 23 to 105 mW between $20\,°C$ and $60\,°C$, and the structure exhibits a temperature coefficient (T_0) of 27 K. The kinks in the light-in versus light-out (LL) curves are due to the multimode lasing with a wide waveguide dimension. It is observed that higher order modes are superimposed with a fundamental mode at the region II of the LL curve, while only a fundamental mode is lasing at the region I. Fig. 8(b) shows LL curves of a 1-μm-wide device with a threshold of 120 mW and a slope efficiency of 0.5% at $20\,°C$. Since this waveguide width is narrower, the fundamental mode is lasing without other higher order modes up to 0.6 mW. This device demonstrates a maximum fiber-coupled output power of 0.9 mW. The total maximum output power including the output from both facets and coupling losses is approximately of 5 mW with a slope efficiency of 2.8%.

In Fig. 9, the threshold pump power dependence on waveguide width is shown for different temperatures. This figure
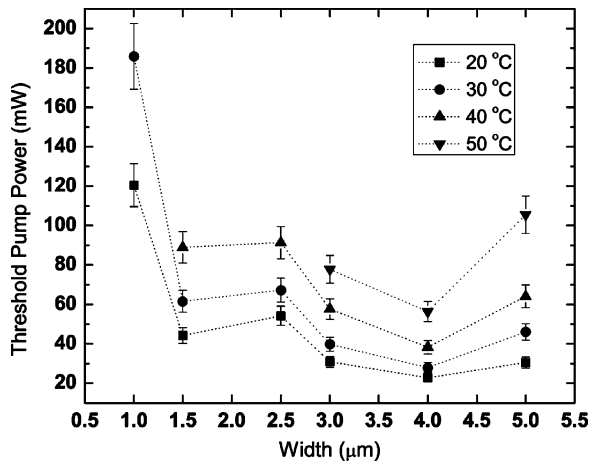
Fig. 9. Threshold variation with different waveguide widths for 800-μm-long devices.
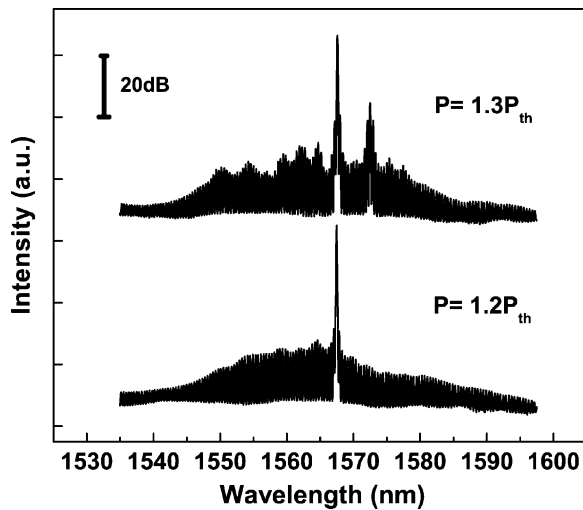

Fig. 10. Spectra for 4-μm-wide, 800-μm-long device. The y-axis is in log scale.

Fig. 11. Measured group indices from spectra for different waveguide widths.
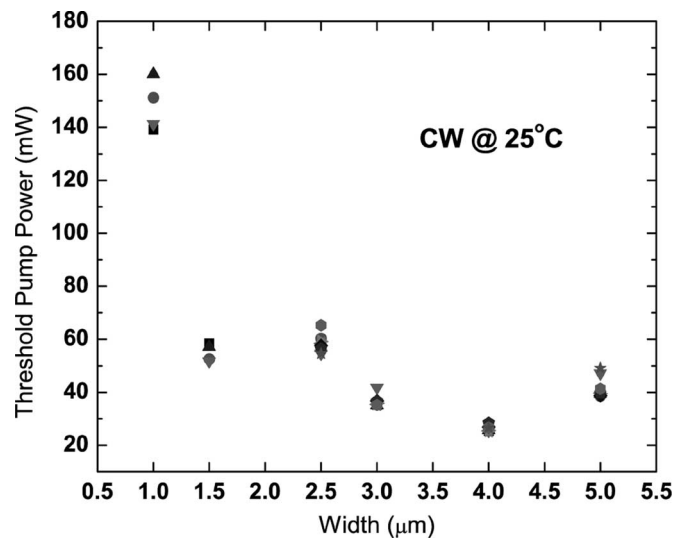
Fig. 12. Threshold variation for 800-μm-length device.

shows the competition between the modal gain and loss for the different stripe width lasers caused by the silicon material loss being an order of magnitude less than the III–V material loss at 1.5 μm. Narrow stripe lasers experience high overlap with the QW region and hence high gain combined with the high modal loss of that material. Wider waveguide widths overlap the silicon region more, reducing both the modal losses at the expense of modal gain. As can be seen, a waveguide width of 4 μm gives optimum performance in terms of the lowest achievable threshold of 23 mW.

Fig. 10 shows the lasing spectrum of a 4-μm-wide device with two pump powers, operating at 25 °C. The optical spectrum consists of the expected Fabry–Pérot response for the 800-μm-long cavity. The measured group indices from the spectra of different waveguide widths are shown in Fig. 11. The dotted line shows the calculated values taking into account the carrier induced index change in the active region. It can be seen from this figure that the waveguides of thinner widths exhibit greater wavelength dependence in modal index than the wider waveguides. This is
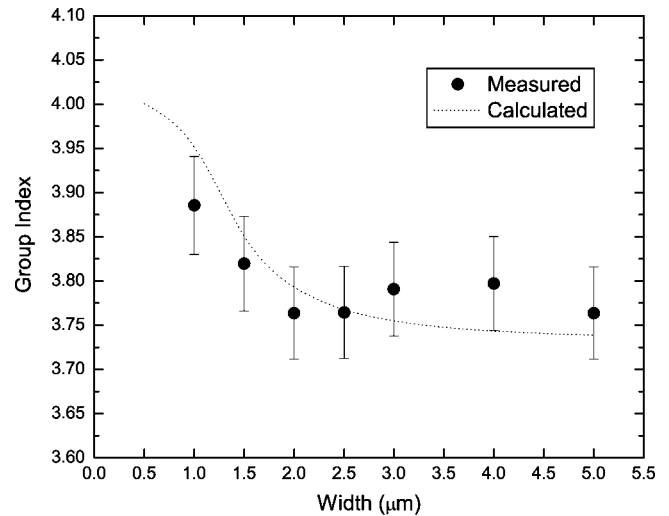
due to the higher mode overlap with the 1.3Q III–V region. The measured errors are limited by the resolution bandwidth of the spectrum analyzer.

Threshold variation and overall device yield are shown in Figs. 12 and 13, respectively. Sixty devices (ten devices at each of six widths) were characterized, out of which 47 devices are lasing as shown in Fig. 13. The yield of the four wider widths is 98%, but the yield is lower for the narrower stripe widths due to the damage during polishing. The devices show a variation of the threshold power for each waveguide width of less than $\pm 9\%$.

In Fig. 14, the measured optical modes imaged by the IR camera are shown for different waveguide widths. The transition of the optical mode from the III–V region to the silicon region can be seen as the waveguide width increases. The experimentally observed optical modes qualitatively match the calculated mode profiles in Fig. 5.

Modal loss is measured experimentally to be ~ 20 cm^{-1} by fabricating a second set of devices with lengths of 700 μm. The
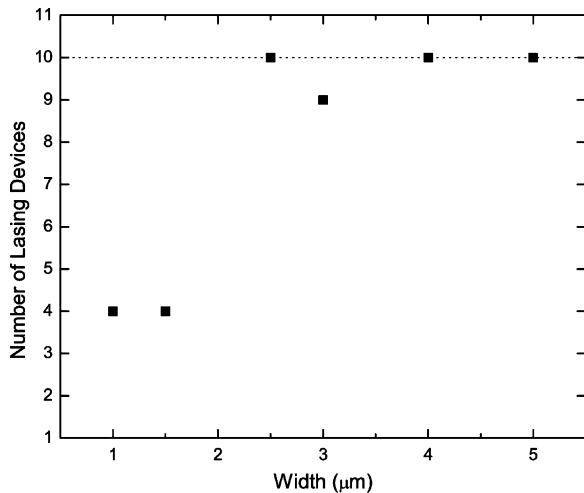
Fig. 13.　Device yield. The number at each width represents the number of lasing devices out of ten.
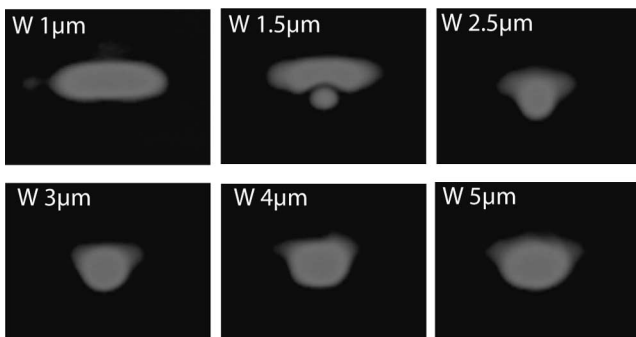

Fig. 14.　Measured mode profiles with different waveguide widths. Height (H) and rib-etch depth (D) of the fabricated waveguides are 0.7 and 0.6 μm, respectively.

modal loss measurement is confirmed by taking Hakki–Paoli measurements in the long wavelength limit. The 700 μm HR coated devices has a maximum output power of 2.7 mW at 20 °C and operate up to 60 °C for wider devices. They show high yield, low device-to-device variation, and threshold versus waveguide width behavior similar to that of the 800 μm devices.

V. Conclusion

Hybrid silicon evanescent lasers combine the standard processing and low loss of silicon waveguides with the high light-generation efficiency of III–V materials. This novel approach is realized by low temperature oxygen assisted wafer bonding, which enables the bonding of InP and silicon—two thermally mismatched materials—at temperatures much lower than that of conventional direct wafer bonding. The characteristic of transverse optical mode follows the general tendency of greater confinement in the silicon region with a wider or taller silicon waveguide. More of the mode is confined in the III–V region with a narrower or shorter silicon waveguide. This suggests that the waveguide dimensions must be chosen carefully depending on the application, considering the tradeoff between optical gain and coupling efficiency with silicon passive devices.

The fabricated hybrid silicon evanescent lasers are optically pumped CW lasers and operate at 1.5 μm. The devices wider than 4 μm have a maximum lasing temperature of 60 °C. The 4-μm-wide devices show the maximum fiber-coupled output power of 4.5 mW with a threshold pump power of 23 mW. The robust process has an yield of 78% and a low device-to-device threshold variation of 9%.

The next step for this new platform is the realization of electrically pumped lasers and other active devices such as amplifiers, modulators, and detectors. The design presented in this paper can be directly extended into electrically pumped active devices by providing proper doping layers to III–V materials and the development of backside processing on the bonded III–V layer for the manipulation of electrical properties. Another potential path of future development is photonic integration with electrical circuitry on SOI wafers. The low temperature bonding process should not contaminate or impair the CMOS circuits while preserving the quality of the III–V materials. General suggested processing steps for the integration can be broken into three major steps: 1) fabricating silicon CMOS circuits and passive optical devices on silicon substrates; 2) bonding silicon with III–V materials via low temperature plasma assisted wafer bonding; and 3) backside processing of the III–V region.

We have presented the design, fabrication, and performance of optically pumped hybrid silicon evanescent lasers. The demands of low-cost high-performance photonic devices and integrated circuits make this new approach promising for a wide range of applications in optical telecommunication systems and optical interconnects.

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