UNIVERSITY OF CALIFORNIA,
IRVINE

Analysis and Design of a Sub-THz > 100 Gbps CMOS RF-64QAM Transmitter with On-Chip Antenna for FutureG Wireless Links

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

Zisong Wang

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DEDICATION

To my father, Yongjia Wang

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ABSTRACT OF THE DISSERTATION

Analysis and Design of a Sub-THz > 100 Gbps CMOS RF-64QAM Transmitter with On-Chip Antenna for FutureG Wireless Links

By

Zisong Wang

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FutureG wireless communication aims for data transmission rates of hundreds of gigabits per second (Gbps), utilizing the extensive bandwidth within the sub-terahertz (sub-THz) spectrum and higher-order modulation schemes such as 64QAM to enhance spectral efficiency. Conventional transmitter (TX) architectures face significant challenges at these data rates, especially from power amplifier (PA) design issues like efficiency degradation and AM-PM distortion.

This research introduces a bits-to-antenna RF-64QAM TX that constructs the 64QAM constellation directly in the RF domain using three QPSK sub-TXs with weighted amplitude, effectively countering PA nonlinearity challenges. To this end, a sub-THz TX prototype fabricated in 45nm CMOS SOI is presented, showcasing a 40-GHz RF bandwidth, with a measured data rate of 120 Gbps, and an effective isotropic radiated power (EIRP) of 16 dBm, paving the way for next-generation wireless communication.

Chapter 1

Introduction

6G and FutureG ambitiously aim at achieving data rates in the realm of hundreds of gigabits per second (Gbps), setting the stage for a transformative leap in data transmission technologies[1]. This vision draws attention to the wide contiguous bandwidth residing within the (sub-)terahertz (THz) spectrum[2], and employs higher-order modulation schemes as key enablers for significantly higher data rates by enhancing spectral efficiency. However, the quest to surpass 100-Gbps data rate with traditional transmitters (TXs) encounters formidable challenges, particularly those associated with power amplifier (PA) design. The obstacles include degradation in power efficiency and error vector magnitude (EVM) stemming from PA nonlinearities, such as AM-AM and AM-PM distortion. These challenges become more pronounced with higher-order modulations (e.g., 64QAM) having higher peak-to-average power ratio (PAPR), where PA nonlinearity precludes full saturation operation, compromising the TX output power. Such constraints are particularly serious at mm-wave frequencies bounded by the device f_{max} and G_{max}. The RF power-digital-to-analog-converter (power-DAC) approach, aimed at resolving efficiency degradation by activating DAC segments associated with specific constellation points, leverages the discrete power-level nature of digital modulation to maintain high power efficiency [3]. However, attaining the necessary

signal-to-noise-and-distortion ratio (SNDR) for wideband, higher-order modulation at mm-wave frequencies remains a significant hurdle. The widely-adopted stack-up topology of RF power-DAC cells confronts challenges in its applicability for wideband design[4, 5]. Additionally, the issue of clock skew, which stems from the need to synchronize delays across DAC segments becomes more severe at sub-THz frequencies [3], casting doubts on its practical viability.

In addressing these complex issues, our recent analysis suggests that the power-backoff issue encountered in PAs when amplifying signals with high PAPR can be substantially alleviated through the concurrent execution of symbol generation/formation and upconversion in the analog/RF domain[6]. A case in point is the construction of a 64QAM signal using three QPSK signals with magnitude ratios of two, as demonstrated in Figure 2.1. This approach, enabling each PA to process a constant-envelope RF signal, not only circumvents AM-AM and AM-PM distortions but also fundamentally avoids power efficiency degradation due to power back-off of high-order modulation. Thus, the PA design complexity is reduced from a multidimensional problem to a more manageable three-dimensional focus on bandwidth, P_{sat}, and stability, enabling new PA design methodologies at sub-THz frequencies[7]. Furthermore, it is established that N QPSK signals with identical EVM will generate a 4^NQAM signal with the same EVM[8, 6].

Leveraging its notable advantages in output power, linearity, and EVM, the direct-RF modulation method, referred to as RF-64QAM, is utilized to generate 64QAM signals at sub-THz frequencies. Fabricated in 45nm CMOS SOI, the RF-64QAM prototype demonstrates the first fully integrated sub-THz TX integrating all critical stages of the digital/mixed-signal/analog/RF chain from bits and symbols generation circuits to the antenna, showcasing a wirelessly measured data rate of 120 Gbps. This paper offers a complete study of the RF-64QAM TX, covering design consideration and over-the-air measurement: Chapter 2 presents the system-level architecture and foundational design principles. Chapter 3

investigates the design considerations and implementation of critical circuit blocks. Chapter 4 details the measurement setups and presents results from the TX prototype. Finally, Chapter 5 summarizes key contributions of this work.

Chapter 2

System Architecture

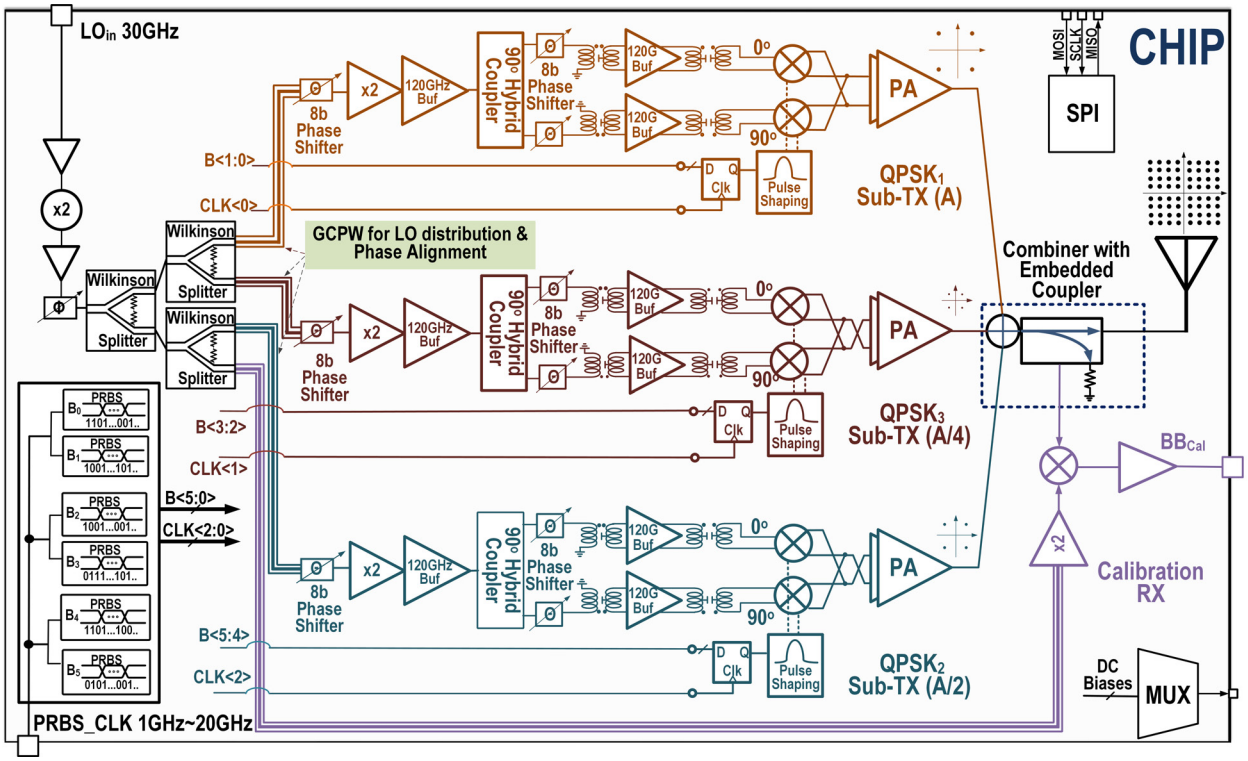


Figure 2.1: System Architecture of the Proposed RF-64QAM Transmitter.

From a system-level perspective, decomposing 4^NQAM into N QPSK sub-TXs relaxes the TX output power and linearity trade-off, while streamlining the overall design process. The TX power efficiency is maximized through minor adjustments in bias conditions and power

supply voltages for the circuit components. Additionally, this architecture significantly boosts the TX reconfigurability. Specifically, through the selective deactivation of sub-TXs, it facilitates a straightforward conversion of the RF-64QAM TX into either an RF-16QAM or a QPSK TX, while maintaining high power efficiency. This feature renders the TX highly adaptable to meet diverse communication needs.

The RF-64QAM TX architecture, as shown in Figure 2.1, revolves around three QPSK sub-TXs that share identical circuit blocks to ensure uniformity, scalability, while simplifying the design process. The output power is fine-controlled by adjusting the DC bias conditions of the three PAs, enabling distinct output saturation power (P_{sat}) levels with a 6 dB difference (Figure 2.1), while maintaining high power-added efficiency (PAE). A key aspect of the design is the carrier synchronization as well as baseband signals' phase alignments among the three sub-TXs, through a carefully laid-out transmission-line-based distribution network and a calibration receiver (RX) with detailed synchronization methods to be elaborated later in Section 2.1.

The on-chip local oscillator (LO) chain takes the external 30-GHz single tone and boosts its frequency to 60 GHz using an on-chip doubler whose output is then fed to Wilkinson power splitters for distribution (Figure 2.1). On the baseband side, the chip incorporates six $2^9 - 1$ pseudorandom binary sequence (PRBS) generators to integrate baseband signal generation and distribution. The DC biasing for all circuit blocks is handled by current-steering DACs under the digital control of an on-chip SPI controller. Fine-tuning the control parameters through SPI enables comprehensive monitoring of on-chip DC bias voltages via the output of an on-chip multiplexer available through one single pad. This configuration facilitates a one-time calibration to compensate for process, voltage, and temperature (PVT) variations.

Focusing on each QPSK sub-TX, the 60-GHz tone emerging from the Wilkinson splitter passes through an LO chain, wherein the first stage is a low-pass 8b phase shifter, with a tuning range of approximately ± 10 to compensate for PVT variations across the three

sub-TXs. The phase-shifter output is fed to a frequency doubler and buffer/amplifier before entering a miniaturized 90 branch-line coupler to produce IQ signals. A pair of 120-GHz buffers then counteract the losses of the coupler and routing, and further boost the LO signal prior to the Gilbert-cell-based QPSK modulator. A local D-flip flop on the baseband signal path compensates for the PRBS routing loss, ensuring adequate conversion gain, while switched-RC networks provide basic pulse shaping. The output of QPSK modulator is coupled via a transformer into a wideband PA with a single-ended output, which finally feeds a 3-way power combiner to form the 64QAM signal.

2.1 Phase Synchronization of QPSK Sub-TXs

Constructing a 64QAM constellation using three QPSK signals necessitates phase synchronization among these QPSK sub-TXs. The relationship between EVM and phase mismatch has been established, as follows[8]:

$$EVM_{RF-64QAM,\theta} = \sqrt{\frac{4[(2\sin\frac{\theta_2}{2} + \sin\frac{\theta_1-\theta_2}{2})^2 - 2\sin\frac{\theta_2}{2}\sin\frac{\theta_1-\theta_2}{2}]}{21}} \tag{2.1}$$

where θ_i for $i \in \{1, 2\}$ represents the phase difference between the largest QPSK signal ($QPSK_3$) and $QPSK_i$. From (2.1), it is deduced that for a -30 dB EVM floor, θ_i must be within ± 5. To meet this theoretical requirement, a three-step strategy is employed for LO and baseband phase synchronizations across the three sub-TXs.

The first step, conducted during the design phase, aligns phase offsets among I/Q carrier signals and synchronizes baseband signals across the QPSK sub-TXs. Variations in bias conditions across the three PAs lead to distinct phase responses for each sub-TX. The resulting phase differences are corrected by precise length adjustments of the grounded coplanar waveguides (GCPWs) that deliver the 60 GHz LO signal from the outputs of Wilkinson splitters to each sub-TX. Additionally, electromagnetic (EM) simulations of interconnects carrying

high-speed baseband signals from PRBS generators are undertaken to ensure modulator input phase alignment.

The second step employs an on-chip calibration RX at the TX output (Figure 2.1) to mitigate PVT variations post fabrication. The 60 GHz LO signal emerging from the splitter is fed to a doubler and is used to downconvert the signal coupled from the combiner's output. During the calibration phase, each sub-TX is activated one by one while the DC output BB_{Cal} of the calibration RX is measured. The 8b tunable 60-GHz phase shifter at each sub-TX input is tuned to calibrate BB_{Cal} to a 0-V DC voltage, achieving phase alignment.

The final step targets IQ phase-mismatch corrections within each QPSK sub-TX, employing a pair of 8b ± 10 phase shifters at 120 GHz placed after the 90° hybrid coupler (Figure 2.1). A one-time calibration for each sub-constellation mitigates process-induced discrepancies, ensuring precise 64QAM signal formation.

2.2 LO Leakage Suppression

Besides the outlined advantages regarding PA linearity, TX power efficiency, and noise reduction, as detailed in [6], the RF-4^NQAM architecture intrinsically enhances LO leakage suppression, leading to higher TX dynamic range and linearity. This is readily achieved by swapping the input connections to the PAs in lower-amplitude sub-TXs (Figure 2.2). Assuming uniform mismatches and parasitic couplings across the sub-TXs, this configuration enables a reduction in total LO leakage amplitude A_{lkg}, as expressed by:

$$A_{lkg} = Ae^{j\Phi}\left(1 - \sum_{i=1}^{N-1}\frac{1}{2^i}\right) \quad \text{for } N \geq 2 \tag{2.2}$$

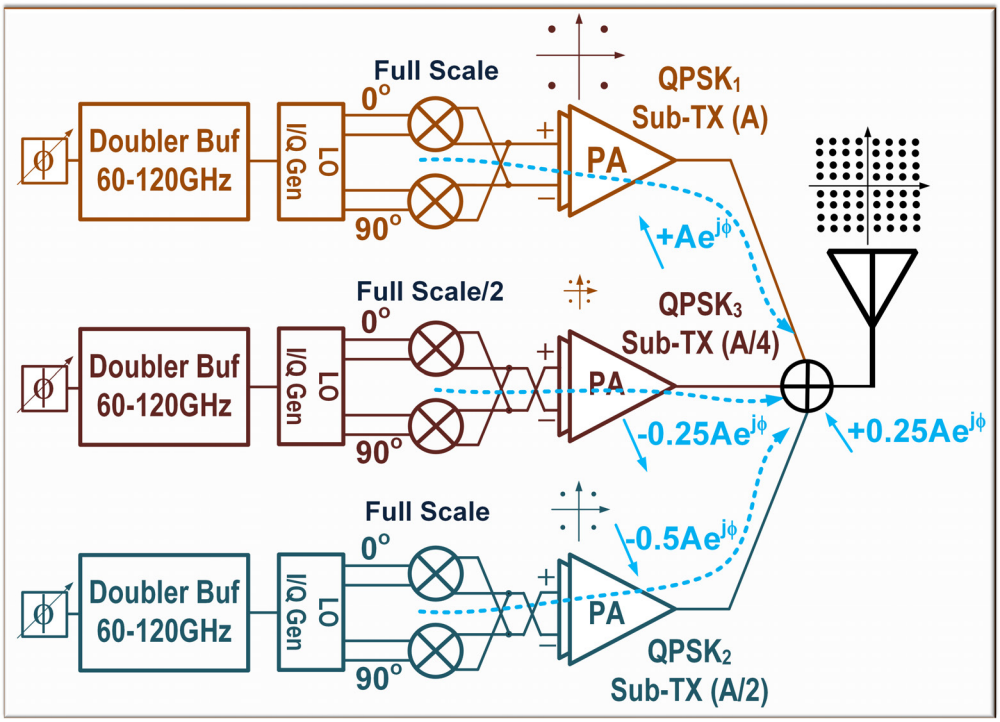


Figure 2.2: Proposed LO leakage suppression technique in RF-64QAM TX.

(2.2) reveals that the RF-QAM TX achieves greater LO leakage suppression with higher-order QAM. As N adopts very large values, we observe:

$$\lim_{N\to\infty} A_{lkg} = \lim_{N\to\infty} Ae^{j\Phi}\left(\frac{1}{2^{N-1}}\right) = 0 \tag{2.3}$$

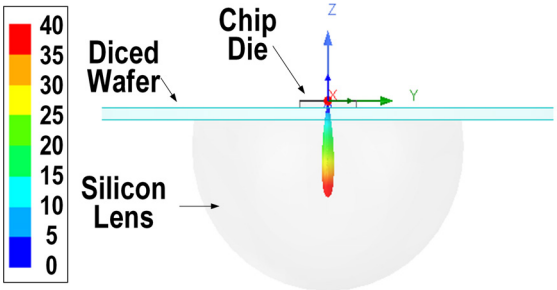
This indicates that, in theory, the RF-QAM TX architecture is capable of completely suppressing the LO leakage. In our specific case of the RF-64QAM TX, this simple architectural variation, as illustrated in Figure 2.2, results in a theoretical 75% (or 12 dB) reduction in LO leakage power.

Chapter 3

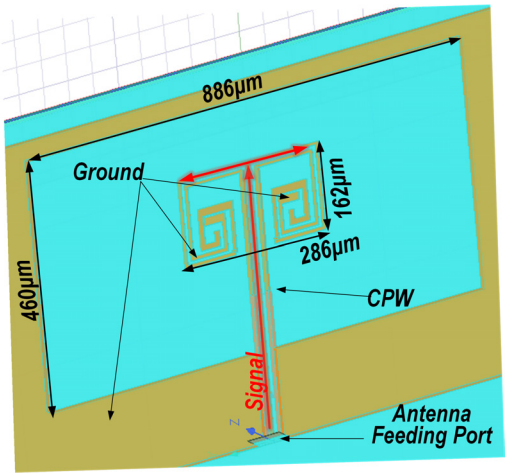
Block Level Design Consideration

3.1 On-chip Wideband Antenna

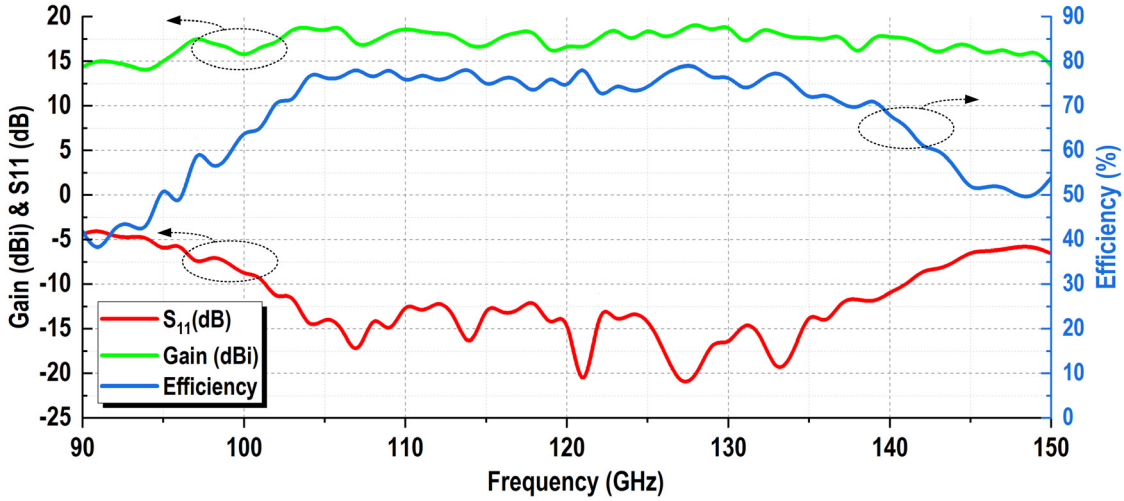
Transmitting a wideband sub-THz modulated signal directly from a chip while maintaining signal integrity poses considerable challenges. The use of wirebonding for an output port above 100 GHz is impractical due to the significant losses associated with bonding wires, which degrade signal integrity. The antenna-in-package (AiP) offers a viable pathway yet faces implementation obstacles[9, 10]. A wide variety of substrate technologies (in terms of materials and processes) have been used, such as high-density interconnect (HDI) PCB using materials with low relative permittivity and loss tangent, low temperature co-fired ceramic (LTCC), quartz-on-silicon, thin films on glass, wafer-level fan-out package, and multi-layer organic laminate [11]. These technologies offer enhanced fabrication precision concerning line width, spacing, and via size useful for optimal matching and high power efficiency in sub-THz antennas, but come with higher costs and longer turnaround. Feeding wideband high-frequency signals to antennas on interposers via copper pillars or C4 balls requires precise interface modeling to capture high-frequency impairments induced by routing



(a) On-chip antenna with backside radiation silicon lens with simulated radiation pattern.



(b) Zoomed-in view of on-chip antenna.



(c) Simulated results of antenna gain, matching, and total efficiency.

Figure 3.1: On-chip antenna design in HFSS.

and vias. In addition, low-loss wideband matching with 30% fractional bandwidth at sub-THz frequencies, as mandated in this work, through heterogeneous integration of multiple materials with different loss-tangent in an AiP structure is extremely challenging and still an open research problem.

Given these considerations, we opt for an on-chip antenna solution. An on-chip antenna with an underneath ground shield is, however, unsuitable for wideband applications due to the substantial interlayer capacitances resulting from dense metal stackup in CMOS process. Without a ground shield, the antenna primarily radiates about 97% of its power into the

silicon substrate due to the significant difference in dielectric constants between air and silicon[12]. Thus, we employ a back-side radiation technique utilizing a silicon lens.

For wideband design, a helical antenna is selected for its superior broadband characteristics compared to dipole antennas[13, 14, 15]. The thick metal layers are utilized to construct the helical antenna, spiraling down from M7 to M6. It is crucial for an on-chip antenna to have a well-defined ground plane to prevent the radiated wave from using the silicon substrate as a propagation medium, potentially jeopardizing the functionality of the IC. To this end, a ground routing that spirals down alongside the signal routing is implemented, as shown in Figure 3.1c. This design secures a well-defined ground path for the signal, while allowing for adjustment of multiple resonant frequencies of the helical antenna by varying the distance between the signal and ground routes to meet wideband design specifications. To enhance gain and ensure electrical field continuity at the ground strips of the CPW feed, the signal path is divided into two symmetrical sub-spirals, enabling effective spatial power combining. Modeled in HFSS with its diced wafer substrate and silicon lens, the simulated radiation pattern of this antenna is displayed in Figure 3.1a. The simulation results in Figure 3.1**??** also reveal ∼15 dBi antenna gain, ∼70% radiation efficiency across the 100-to-140-GHz range, and good input matching, as indicated by $S_{11} < -10$ dB.

3.2 Front-End Wideband Power Combining

3.2.1 Power Combining in RF-QAM Modulation

The power combining is a crucial part of the proposed RF-64QAM TX, serving a dual purpose, (1) it helps in the construction of the 64QAM constellation, and (2) it naturally combines the power from several PAs in their saturation and increases the equivalent TX saturation power, $P_{sat,eq}$, at the system level. To elucidate, consider the PA saturation power

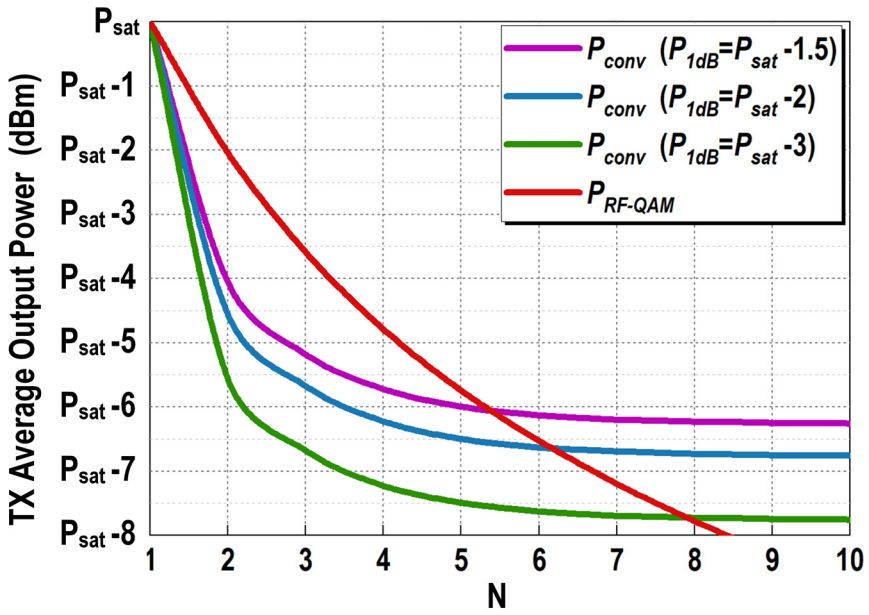


Figure 3.2: Comparison of average TX output power for 4^NQAM modulation between direct-RF modulation scheme and conventional approach.

of QPSK$_1$ to be P_{sat}, $P_{sat,eq}$ is derived, as follows:

$$P_{sat,eq} = \sum_{i=0}^{N-1} \frac{P_{sat}}{4^i} \tag{3.1}$$

where N denotes the number of sub-TXs contributing to the 4^NQAM generation. For $N = 3$, (3.1) yields $P_{sat,eq} = 1.3125 P_{sat}$, marking a 1.2 dB improvement in equivalent saturation power before any power back-off is applied. As N approaches infinity, $P_{sat,eq}$ asymptotically reaches:

$$P_{sat,eq} = \lim_{N\to\infty} \sum_{i=0}^{N-1} \frac{P_{sat}}{4^i} = \frac{4}{3} P_{sat} \tag{3.2}$$

As discussed below, this P_{sat} enhancement implies that the RF-QAM TX is capable of providing larger output power compared to the conventional counterpart even when accounting for $10\lg(N)$ dB power combining loss. This observation underscores the superiority of the proposed RF-QAM TX architecture.

The output power discrepancies between an RF-QAM TX and the conventional counterpart necessitates quantitative analysis of the average output power. For a conventional TX, the PA should handle an upconverted high-order modulated signal with a high PAPR. Notably, PAPR for a 4^NQAM signal is given by [6]:

$$PAPR = \frac{3 \times (2^N - 1)}{2^N + 1} \tag{3.3}$$

The PA is typically required to back-off from its 1 dB compression point P_{1dB} in a TX handling high-order QAM. This requirement shapes the average output power for the conventional TX, as follows:

$$\mathrm{P}_{conv}\ (dB) = \begin{cases} P_{sat} & \text{if } N = 1, \\ P_{1dB} - 10\lg\left[\frac{3(2^N-1)}{2^N+1}\right] & \text{otherwise.} \end{cases} \tag{3.4}$$

In the proposed RF-4^NQAM TX, the PA output power in each QPSK sub-transmitter can extend beyond P_{1dB} to P_{sat}. The power back-off in this architecture effectively becomes the insertion loss from the power combiner. Assuming the use of a classic N-way Wilkinson balanced power combiner[16], the insertion loss can be quantified as $10\lg(N)$ dB. Thus, the average output power for the RF-QAM scheme is derived as:

$$P_{RF-QAM}\ (dB) = P_{sat} + 10\lg\left[\frac{4}{3}\left(1 - \frac{1}{4^N}\right)\right] - 10\lg(N) \tag{3.5}$$

Figure 3.2 visually compares the average output power between RF-QAM TX and the conventional counterpart based on (3.4) and (3.5). Recognizing that the difference between P_{1dB} and P_{sat} is contingent upon the linearity of PA topology, this analysis uses benchmark examples of 1.5-, 2- and 3-dB differences. For the PA used in the QPSK sub-TX_1, the simulated difference is 2 dB. The majority of published CMOS PAs operating above 100 GHz

demonstrate a measured difference of $1.5 \sim 4$ dB[17, 18]. Figure 3.2 shows that the RF-QAM TX achieves higher average output power for modulation orders extending up to 1024-QAM ($N \leq 5$) even for a difference as small as 1.5 dB. This advantage extends to $16K$-QAM ($N \leq 7$) when the difference reaches 3 dB. Notably, our RF-64QAM TX design showcases a 2.1 dB advantage in average output power. Moreover, since the P_{1dB} point is often higher than the actual linear region boundary of the PA[19], mitigating the AM-to-AM and AM-to-PM effects on the EVM floor for conventional TX allows this advantage of RF-64QAM to be extended to even larger N values in practice. Additionally, considering 6G and FutureG may impose stringent requirements on the IM3 level, PAs may need to operate with a greater back-off from P_{1dB}, further highlighting the advantage of RF-QAM TX. To summarize, this analysis validates that by enabling the PA to work in its P_{sat} region for all 4^NQAM modulations, the RF-QAM architecture fundamentally improves the TX output power.

3.2.2 Miniaturized 3-Way On-Chip Combiner

Processing wideband uncorrelated signals simultaneously using three QPSK sub-TXs necessitates a 3-way combiner with exceptional isolation and large fractional bandwidth. Traditional 3-way Wilkinson combiners, although effective in theory, do not fit planar 2D designs due to their reliance on Δ-resistors or star-resistors[20]. This challenge compels a shift towards the adoption of a more sophisticated recombinant power combiner structure [21], designed in a 2D layout that combines 10 transmission lines each with one of 6 unique characteristic impedances, as shown in Figure 3.3. Adopting a Chebyshev transformation for synthesis,

these six impedances, Z_1 to Z_6 are derived:

$$\begin{cases} Z_1 = \mathcal{T}_1 & \text{(3.6a)} \\ Z_2 = 2\mathcal{T}_2 & \text{(3.6b)} \\ Z_3 = \dfrac{2\mathcal{T}_3 Z_4}{Z_4 - 2\mathcal{T}_3} & \text{(3.6c)} \\ Z_4 = \mathcal{T}_3 \left[2 + \dfrac{\sqrt{2}K}{\mathcal{T}_4}(Z_6 - \mathcal{T}_4) \right] & \text{(3.6d)} \\ Z_5 = \dfrac{2\mathcal{T}_4 Z_6}{Z_6 - \mathcal{T}_4} & \text{(3.6e)} \\ Z_6 = \dfrac{\mathcal{T}_1\mathcal{T}_3\mathcal{T}_4\left(\sqrt{2} - K\right)}{\mathcal{T}_2\mathcal{T}_4\sqrt{2K^2+2} - K\mathcal{T}_1\mathcal{T}_3} & \text{(3.6f)} \end{cases}$$

where $\mathcal{T}_1 = 0.91Z_0$, $\mathcal{T}_2 = 1.4Z_0$, $\mathcal{T}_3 = 0.48Z_0$, $\mathcal{T}_4 = 0.36Z_0$, and K^2 denotes the sum of the powers of Port 2 and Port 4 to that of Port 3[21, 22]. However, for $K^2 = 2$ these relationships turn singular, and the necessity for all ten transmission lines to be of quarter wavelength renders the structure unsuitable for on-chip integration.

Efforts were made to minimize transmission line lengths and reduce the number of lines on planar 3-way combiners at the PCB level[23], yet application to on-chip integration remains unexplored. To tackle these challenges and tailor the footprint of the combiner for silicon integration, we accommodate design flexibility by allowing the power combiner to make up for part of the 12-dB output power difference needed between QPSK_3 and QPSK_1 sub-TXs. This will allow flexibility in choosing K^2. Assuming -20dB return loss to be satisfactory in this design, Z_0 is selected such that Z_5 and Z_6 are sufficiently close to $50\,\Omega$. Pursuing this approach, $K = 1.2$, and $Z_0 = 40\,\Omega$, and from (3.6) this yields $Z_5 = 44\,\Omega$ and $Z_6 = 41.4\,\Omega$ for this design, which achieves a reflection loss of -19 dB and an insertion loss difference of about 1 dB between S_{31} and S_{21}. As Z_5 and Z_6 is close to $50\,\Omega$, this allows for the removal of the three input transmission lines—specifically TL_8, TL_9, and TL_{10}, as shown in Figure 3.3.

Apart from the issues related to footprint, another concern is the range of characteristic

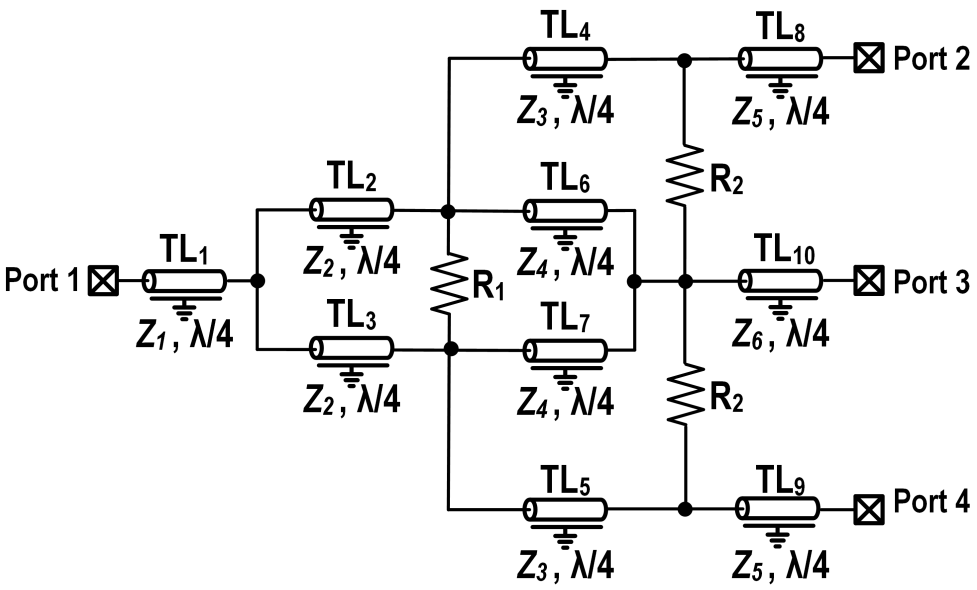


Figure 3.3: Schematic of a conventional recombinant, in-phase power combiner.

impedances realizable by on-chip transmission lines. Due to the complexity of the signal routings in this TX, the GCPW has been selected as the preferred transmission-line structure owing to its well-defined ground return path, while providing substantial isolation from any environmental noise that may disturb the TX output signal. However, the characteristic impedance range for on-chip GCPW is determined by the technology specifications of the foundry, which dictate the maximum and minimum widths for thick metal wire routing and the spacing to lower metal layers. This range typically spans from $30\,\Omega$ to $80\,\Omega$.

The recombinant combiner design, if followed by (3.6), often necessitates an impedance surpassing $80\,\Omega$. For instance, with $Z_0 = 40\,\Omega$ and $K = 1.2$ as selected parameters, Z_4 is calculated to be $99.5\,\Omega$. To address this issue, the use of serial inductances at the transmission line's ends is identified as an effective measure, which also aids in reducing the line's overall length, as shown in Figure 3.4 [24]. The diversity in characteristic impedances used within this combiner naturally results in the formation of T-junctions at each connection node, where GCPW discontinuities act as the required serial inductance [25]. (Figure 3.5). Furthermore, a capacitor introduced at the T-junction further shortens the length of $\mathrm{TL}_2/\mathrm{TL}_3$,

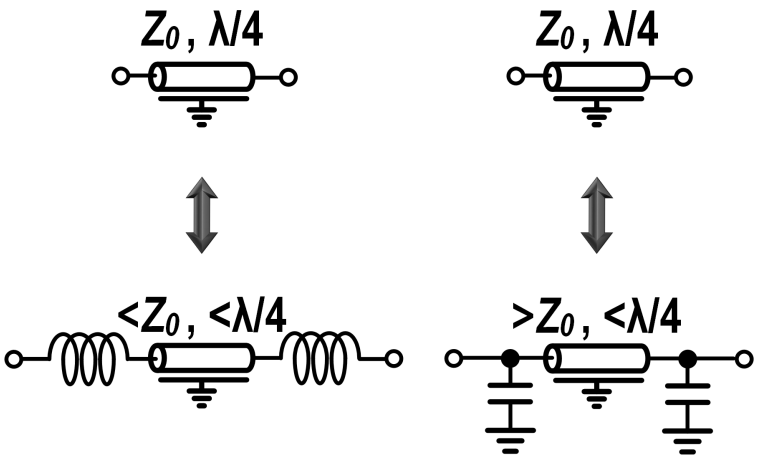


Figure 3.4: Strategies to shorten transmission line length: add serial inductors, reducing Z_0; or add parallel capacitors, increasing Z_0.

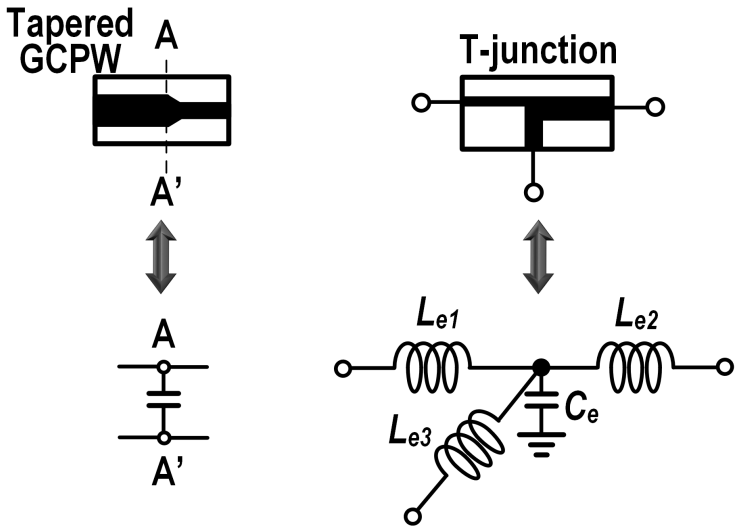


Figure 3.5: Equivalent circuits for GCPW discontinuities: Tapered GCPW, and T-junction.

while making characteristic impedance Z_2 to be more flexible. This adjustment enhances the design versatility of the combiner. and we were able to get $Z_2 = Z_3$ through this practice, simplifying the design process.

Finally, TL_1 in Figure 3.3 at the combiner output is replaced with a -14 dB coupler – comprising a 13-fF coupling capacitor, a 50 Ω isolation resistor, and an interstage matching circuit – to realize a coupler-embedded combiner (Figure 3.6). This embedded coupling network captures a portion of the TX output power and feeds the on-chip calibration RX, all while

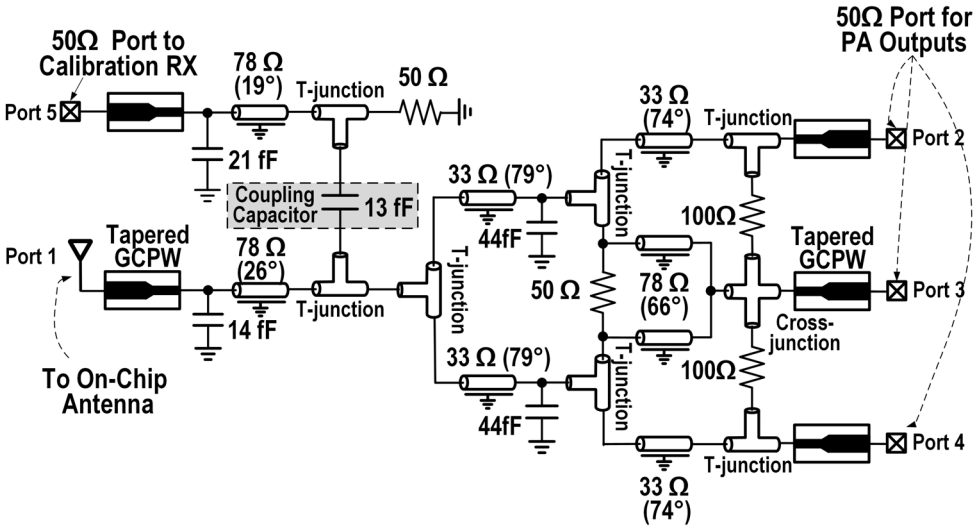


Figure 3.6: Schematic of coupler-embedded combiner.

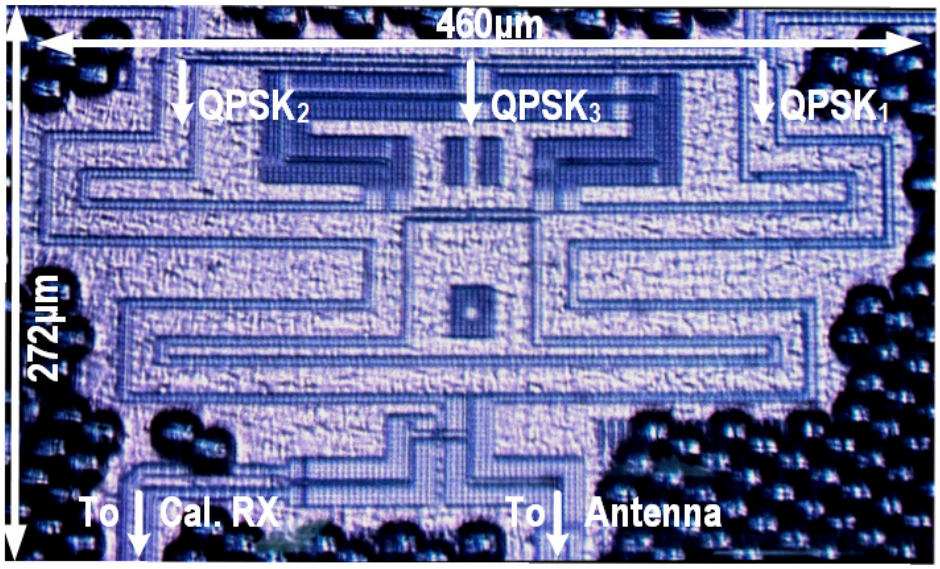
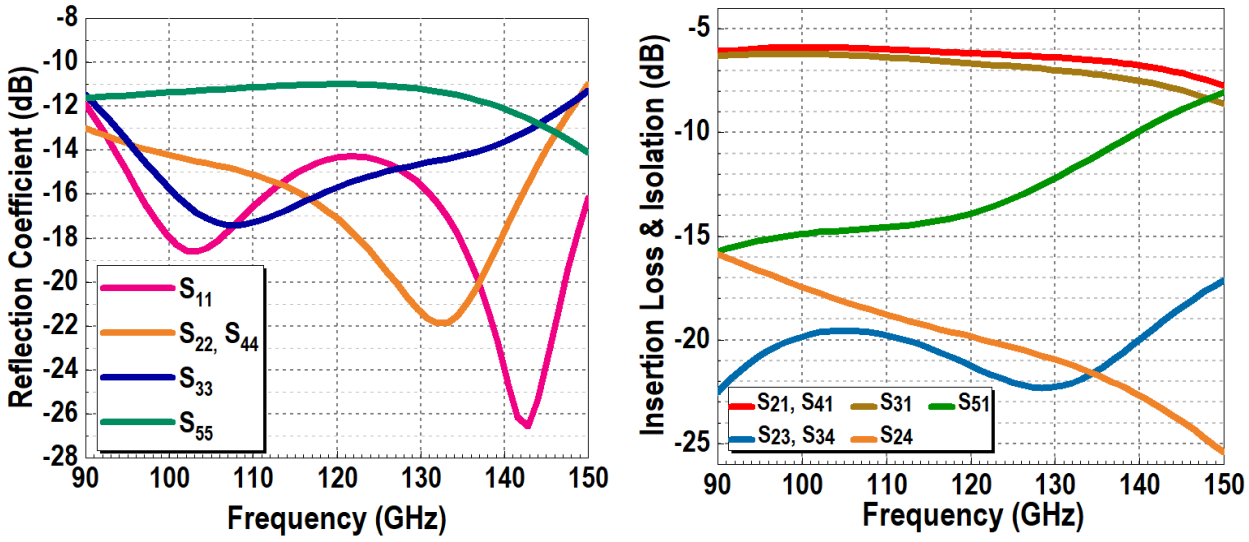


Figure 3.7: Micro-photograph of fabricated coupler-embedded combiner.

exerting a negligible impact on the TX performance. The loaded capacitor, together with the capacitive component resulting from the output tapered GCPW, are used to reduce the footprint of this transmission line network [26].

The final schematic of the miniaturized coupler-embedded combiner and its microphotograph are depicted in Figs. 3.6 and 3.7. This block occupies an area of $460\times272\mu m^2$. The simulated performance is summarized in Figs. 3.8a-3.8b, demonstrating <-10 dB input matching, <-



(a) Simulated matching performance.

(b) Simulated insertion loss, coupling, and isolation.

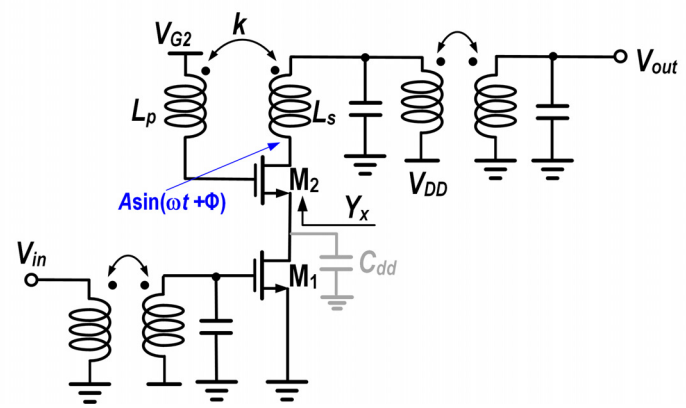
Figure 3.8: Simulated matching performance of proposed coupler-embedded combiner.

15 dB isolation, and 6 dB insertion loss across the entire F-band together with a -14 dB coupling at carrier frequency. This design presents the first 3-way combiner integrated in silicon.

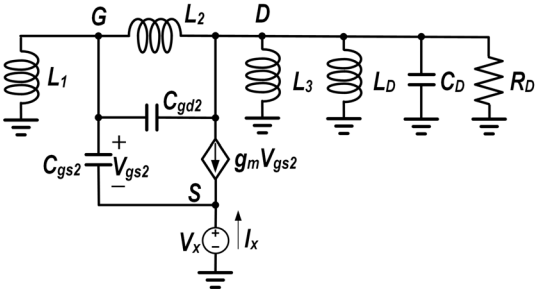
3.3 Wideband PA

Sub-THz PA design in CMOS faces a significant challenge in achieving high output power due to constraints imposed by the process intrinsic limitations on G_{max} and f_{max}. This work focuses on exploring a PA topology that can achieve maximum output power over a wide bandwidth. Along the way, we adopt a two-stage PA which is fed by up to 0-dBm output power from the QPSK modulator, sufficient for PA saturation. As outlined in Chapter 1, the PAs placed before the power combiner now handle QPSK signals, enabling us to focus on improving P_{sat} and bandwidth, while ensuring stability.

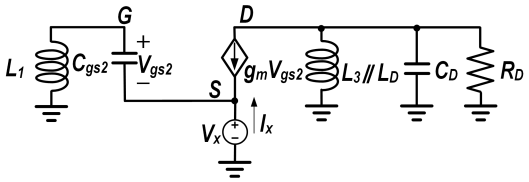
3.3.1 P_{sat} Enhancement



(a) Half circuits schematic of the PA output stage.



(b) Equivalent small-signal circuit for Y_x calculation



(c) Simplified Equivalent small-signal circuit at high corner frequency

Figure 3.9: Schematic of the PA output stage.

In CMOS PA design, the maximum output power is often constrained by the technology's breakdown voltage. To mitigate this limitation, we employ mutually coupled gate and drain inductors with a coupling factor $k \sim 0.2$ within the common-gate transistor of the PA's output cascode stage, as shown in Figure 3.9a. Assuming the drain signal emerging from the final stage is represented by $A\sin(\omega t + \Phi)$, this mutual coupling introduces a signal at the gate with a coupling factor of α, resulting in:

$$V_{DG2} = V_{DD} - V_{G2} + A(1-\alpha)\sin(\omega t + \Phi) \tag{3.7}$$

where V_{DD} is the supply voltage, and V_{G2} is the gate bias voltage. To avert voltage break-

down, the maximum amplitude A_{max} is derived to be:

$$A_{max} = \frac{V_{BO} - (V_{DD} - V_{G2})}{1 - \alpha} \tag{3.8}$$

with V_{BO} representing the gate-drain breakdown voltage. (3.8) shows that, given the same bias conditions, this coupling factor α can improve P_{sat} without endangering the transistor breakdown. Notably, biasing the gate at V_{DD} yields $A_{max} \simeq (1 + \alpha)V_{BO}$ for small α values, indicating the feasibility of achieving output voltage levels beyond breakdown-voltage constraints set by the CMOS process.

3.3.2 Bandwidth Enhancement

The PA bandwidth primarily determines the overall TX bandwidth, thereby influencing the achievable data rates. The mutually coupled gate and drain inductors L_p and L_s will contribute to PA's bandwidth enhancement, as will be proved using the small-signal analysis of the PA's output stage in Figure 3.9a.

We adopt the π model for the coupling inductances [27], while disregarding the intrinsic parasitics within the transformer. The investigation commences by deriving input admittance seen at the source node of the cascode device. This leads to the small-signal equivalent circuit of Figure 3.9b. The inductances L_1, L_2, and L_3 are derived to be[27]:

$$\begin{cases} L_1 = \dfrac{L_p L_s - M^2}{L_s - M} & \text{(3.9a)} \\ L_2 = \dfrac{L_p L_s - M^2}{M} = \dfrac{1 - k^2}{k}\sqrt{L_p L_s} & \text{(3.9b)} \\ L_3 = \dfrac{L_p L_s - M^2}{L_p - M} & \text{(3.9c)} \end{cases}$$

where $M = k\sqrt{L_p L_s}$ denotes the mutual inductance between L_p and L_s. The equivalent inductor L_2 in parallel with C_{gd} can either resonate out this parasitic capacitance - turning

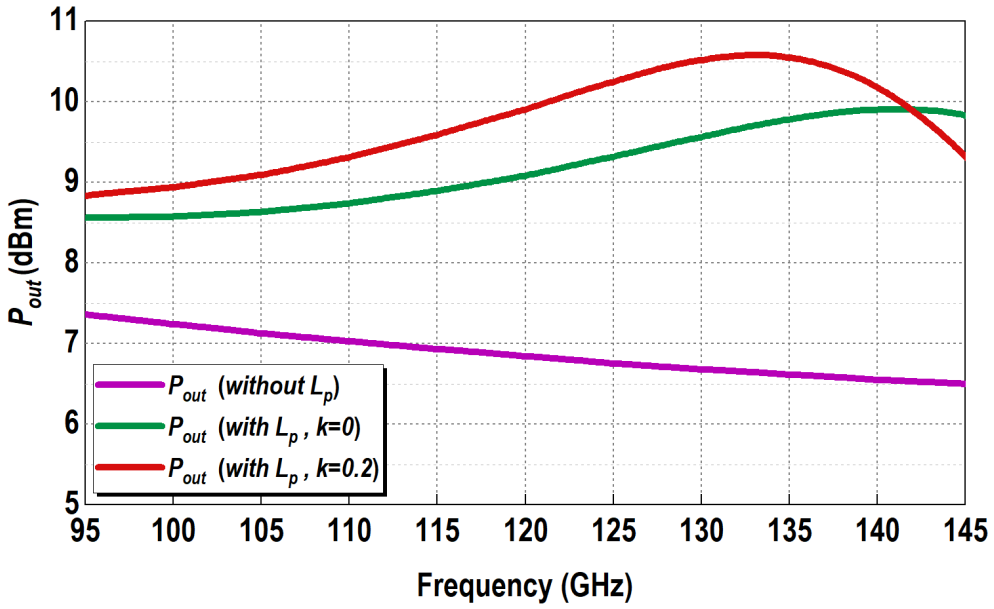


Figure 3.10: Simulated results comparison for P_{out} when cascade device has different gate inductance configurations.

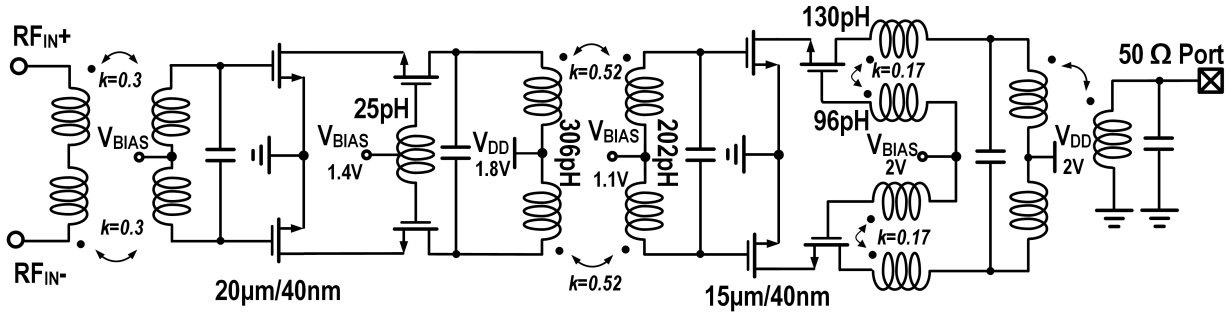


Figure 3.11: Schematic of wideband differential PA with single-end output balun.

the gate-drain connection as an open circuit - or render this parallel network as a negligibly small capacitance. This notion leads to the simplified equivalent circuit in Figure 3.9c. Applying KCL, the input admittance Y_x is derived, as follows:

$$Y_x(j\omega) \triangleq \frac{I_x}{V_x} = \underbrace{\frac{g_{m2}}{1-\omega^2 L_1 C_{gs2}}}_{G_x} + j\omega \underbrace{\frac{C_{gs2}}{1-\omega^2 L_1 C_{gs2}}}_{C_x} \tag{3.10}$$

Defining a reference resonant frequency $\omega_0 \triangleq 1/\sqrt{L_1 C_{gs2}}$, (3.10) reveals that

$$\begin{cases} G_x > 0,\ C_x > C_{gs2} > 0 & \text{if } \omega < \omega_0, \quad (3.11a) \\ G_x < 0,\ C_x = -\dfrac{C_{gs2}}{\left(\frac{\omega}{\omega_0}\right)^2 - 1} < 0 & \text{if } \omega > \omega_0. \quad (3.11b) \end{cases}$$

(3.11b) reveals unique admittance properties at high frequencies, notably the appearance of negative resistance and capacitance. From Figure 3.9a, we can see that this negative resistance can neutralize the effects of large drain resistance r_{o1} and the total capacitance C_{dd} seeing from the drain of M_1. For a special case of $C_x = -C_{dd}$, the effective capacitance seen at the intermediate node of the cascode stage is removed, thereby increasing the bandwidth.

The mutual coupling effect introduced between the gate and drain inductances offers distinct advantages over conventional gain-peaking inductor techniques for bandwidth enhancement[28]. Figure 3.10 presents large-signal simulation results comparing a standalone cascode PA operating at P_{sat} with the same output loading network at the drain but under three different configurations at the gate: without gate inductance L_p, with gate inductance L_p but no coupling factor, and with gate inductance L_p and a coupling factor of 0.2. The simulations clearly show that introducing a coupling factor helps in C_{gd2} neutralization, and results in additional peaking in output power at the high corner frequency to compensate for sharp roll-off, thus extending the bandwidth. Furthermore, this approach results in L_1 and L_2 values that are larger than those of L_p and L_s, enabling a more compact layout for inductances[1]. This compactness is beneficial for increasing the self-resonance frequency (SRF) of the transformer, an essential aspect for sub-THz applications.

Following our analysis in [7], we adopt a transformer-based interstage matching network for its superior bandwidth enhancement over transmission-line designs, further augmented by

[1]Proof is shown in Appendix A.

stagger tuning. Additionally, the gain-peaking inductor technique is also utilized at the PA's first stage, ensuring the wide bandwidth of the entire design.

3.3.3 Stability

To safeguard the output stage's stability while maximizing bandwidth, the negative resistance seen at the drain of the common-source device M_1 in Figure 3.9a (*cf.* Eq. (3.11b)) must be designed to be smaller than the output resistance viewed from drain node of M_1. Disregarding C_{gd1} for simplicity, this leads to:

$$r_{o1} > \left|\frac{1}{G_x}\right| = \frac{\left(\frac{\omega}{\omega_0}\right)^2 - 1}{g_{m2}} \tag{3.12}$$

Combining (3.11b) and (3.12) establishes a critical design constraint:

$$1 < \frac{\omega}{\omega_0} < \sqrt{g_{m2} r_{o1} + 1} \tag{3.13}$$

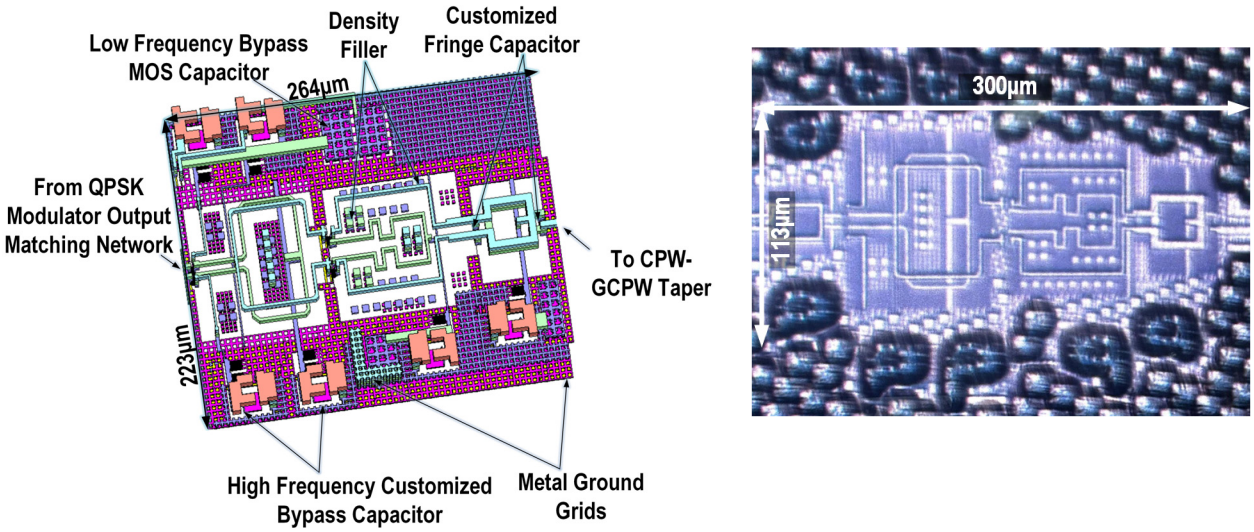
As $g_{m2} r_{o1}$ is usually a large number in amplifier design, the relationship in (3.13) can be easily satisfied.

If we consider C_{gd1} for M_1, the input impedance of M_1 can be expressed as:

$$Y_{in} = j\omega C_{gs1} + j\omega C_{gd1}\left(\frac{g_{m1} + Y_x}{Y_x + j\omega C_{gd1}}\right) \tag{3.14}$$

Here, Y_x is as defined in (3.10). Ensuring unconditional stability of the amplifier requires the real part of Y_{in} to be positive, leading to:

$$(C_x + C_{gd1})(g_{m1} + G_x) > G_x C_x \tag{3.15}$$



(a) Layout of wideband PA.

(b) Microphotograph of the fabricated PA.

Figure 3.12: PA layout and micro-photograph.

This condition introduces another design constraint:

$$\frac{\omega}{\omega_0} > \sqrt{1 + \frac{g_{m1}C_{gs1} + g_{m2}C_{gd1}}{g_{m1}C_{gd1}}} \tag{3.16}$$

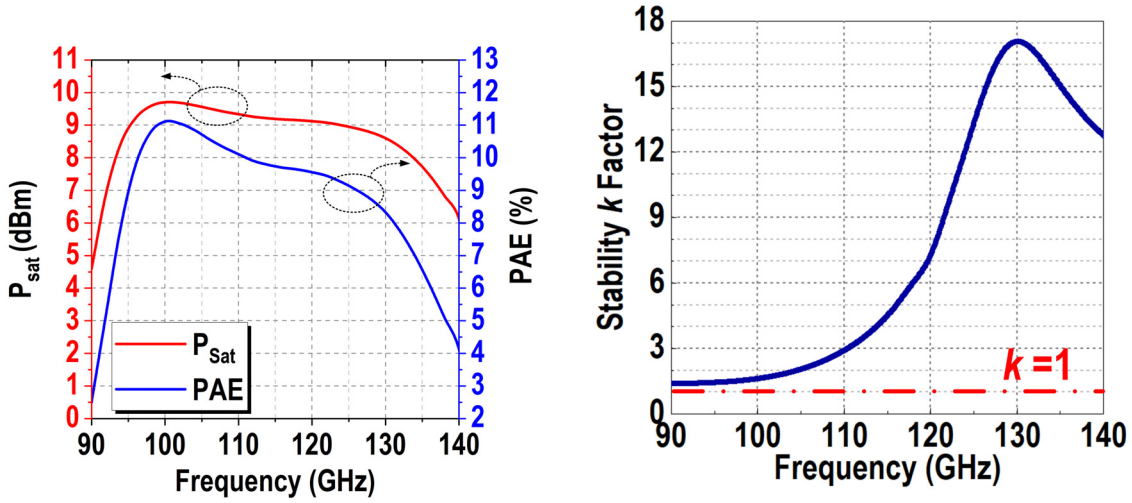
Combining with (3.13), we derive a comprehensive design guideline for PA stability:

$$\sqrt{1 + \frac{g_{m1}C_{gs1} + g_{m2}C_{gd1}}{g_{m1}C_{gd1}}} < \frac{\omega}{\omega_0} < \sqrt{g_{m2}r_{o1} + 1} \tag{3.17}$$

(3.17) outlines a more detailed constraint for ensuring the stability of the PA in the design process.

As part of the design process, we initially utilize the small-signal analysis described above to establish the foundation for our design parameters. We then conduct large-signal S-parameter (LSSP) simulations in Cadence Spectre to obtain all critical large-signal transistor parameters. These LSSP parameters are used to replace the values in the initial small-signal design equations. To ensure PA stability across all operational frequencies, further validations are conducted via large-signal harmonic balance and transient simulations at the

design stage.



(a) Simulated P_{sat}, PAE

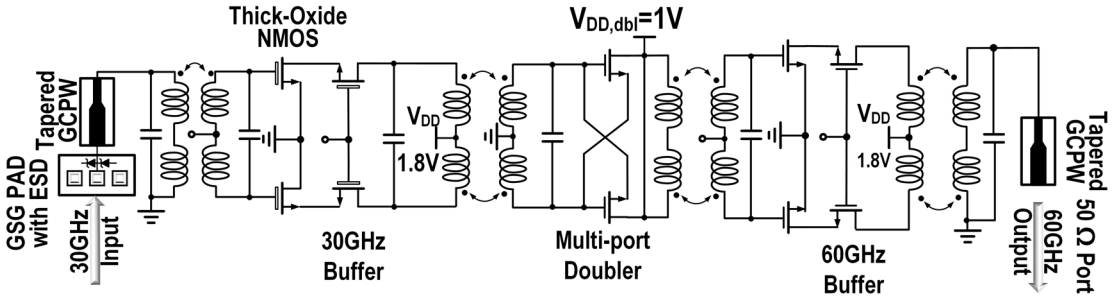
(b) Simulated k-factor for stability.

Figure 3.13: Simulated PA performance.

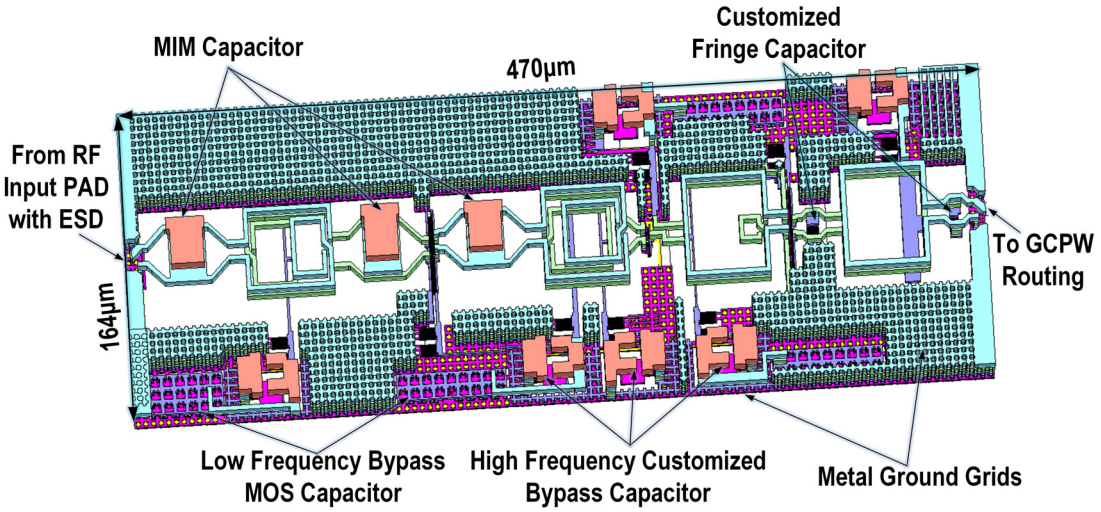
The final standalone layout of the PA, excluding the modulator output matching network, is depicted in Figure 3.12a. The micro-photograph of the entire fabricated PA, occupying an area of $300\times113\mu m^2$, is shown in Figure 3.12b. Post-layout simulation results indicate a saturation power (P_{sat}) exceeding 9 dBm and a 3-dB bandwidth surpassing 40 GHz, as shown in Figure 3.13a. Large-signal S-parameter simulation confirms $k > 1$ across F-band, as illustrated in Figure 3.13b, demonstrating unconditional stability of the PA.

3.4 Frequency doubler and LO chain

As described in Section 2, the TX utilizes an off-chip 30 GHz signal for the LO input, enabling on-chip generation of a 120 GHz signal via two doubler chains. Due to the topological similarities between these chains, only one is illustrated for the sake of brevity. As depicted in Figure 3.14a, the configuration includes a 30 GHz buffer, a doubler, and a 60 GHz buffer. The use of a cascode topology for each LO buffer ensures stability and sufficient output power, while the inclusion of thick-oxide NMOS transistors in the 30 GHz buffer stage enhances the

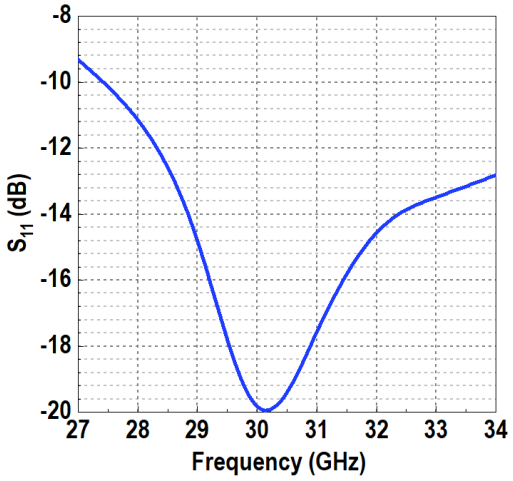


(a) Schematic.

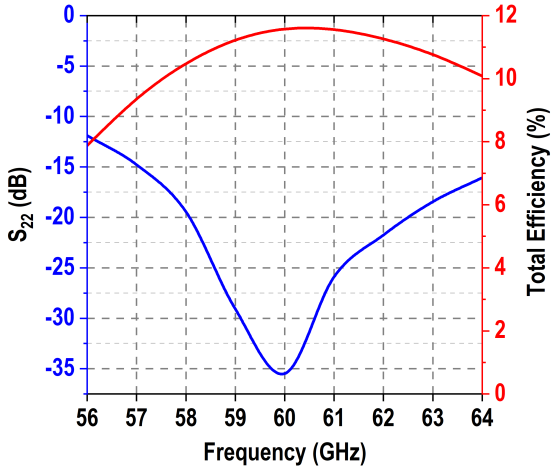


(b) Layout.

Figure 3.14: Schematic and layout of LO doubler and buffers.



(a) S_{11}.



(b) S_{22} and total efficiency.

Figure 3.15: Simulated performance for LO doubler chain.

design's durability.

The design reliability is further enhanced by a carefully designed matching network, which integrates 30 GHz ESD-protected input pads and utilizes tapered GCPW routing with a transformer matching network. This approach effectively mitigates capacitive effects of ESD diodes, ensuring robust transfer of the off-chip LO signal into the chip. The efficacy of the matching network is demonstrated by the simulated input matching shown in Figure 3.15a, where $S_{11} < -10$ dB is achieved across the 27.5-34 GHz range.

Given the power-hungry nature of the LO chain in the TX design, a multiport waveform shaping technique has been adopted to significantly improve power efficiency[29]. Shown in Figure 3.14a, this doubler achieves zero DC power by biasing the gate of a cross-coupled NMOS pair at DC 0 V (class-C operation regime [30]). This multiport doubler is then connected to an additional buffer stage to ensure a satisfactory output power level to be able to drive the subsequent stages. Figure 3.14b shows the detailed layout of the 30 GHz LO doubler chain, featuring ground grid distribution and localized bypass capacitors, and occupies an area of $470 \times 164\,\mu m^2$. The total efficiency[2] of this doubler chain, peaking at 11.5% at 60 GHz, is shown in Figure 3.15b. The 60 GHz LO output port exhibits $S_{22} < -10$ dB across the 56-64 GHz range, and provides a > 10 dBm power ready to be distributed to three QPSK sub-TXs through GCPW and Wilkinson-splitter network.

3.5 LO IQ Generation

The 120-GHz LO IQ generation circuit, detailed in Figure 3.16, is comprised of a 90 branch-line coupler followed by a phase shifter for IQ calibration and 120-GHz buffers. In conventional designs, IQ branch-line couplers necessitate quarter-wave length routing on each side,

[2]Total efficiency $\eta_{total} = \dfrac{P_{out}}{P_{DC} + P_{in}} \times 100\%$.

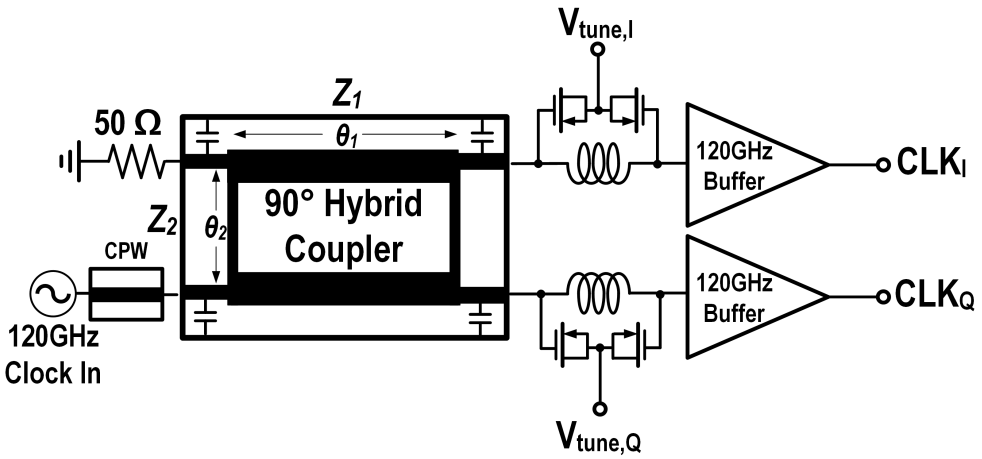
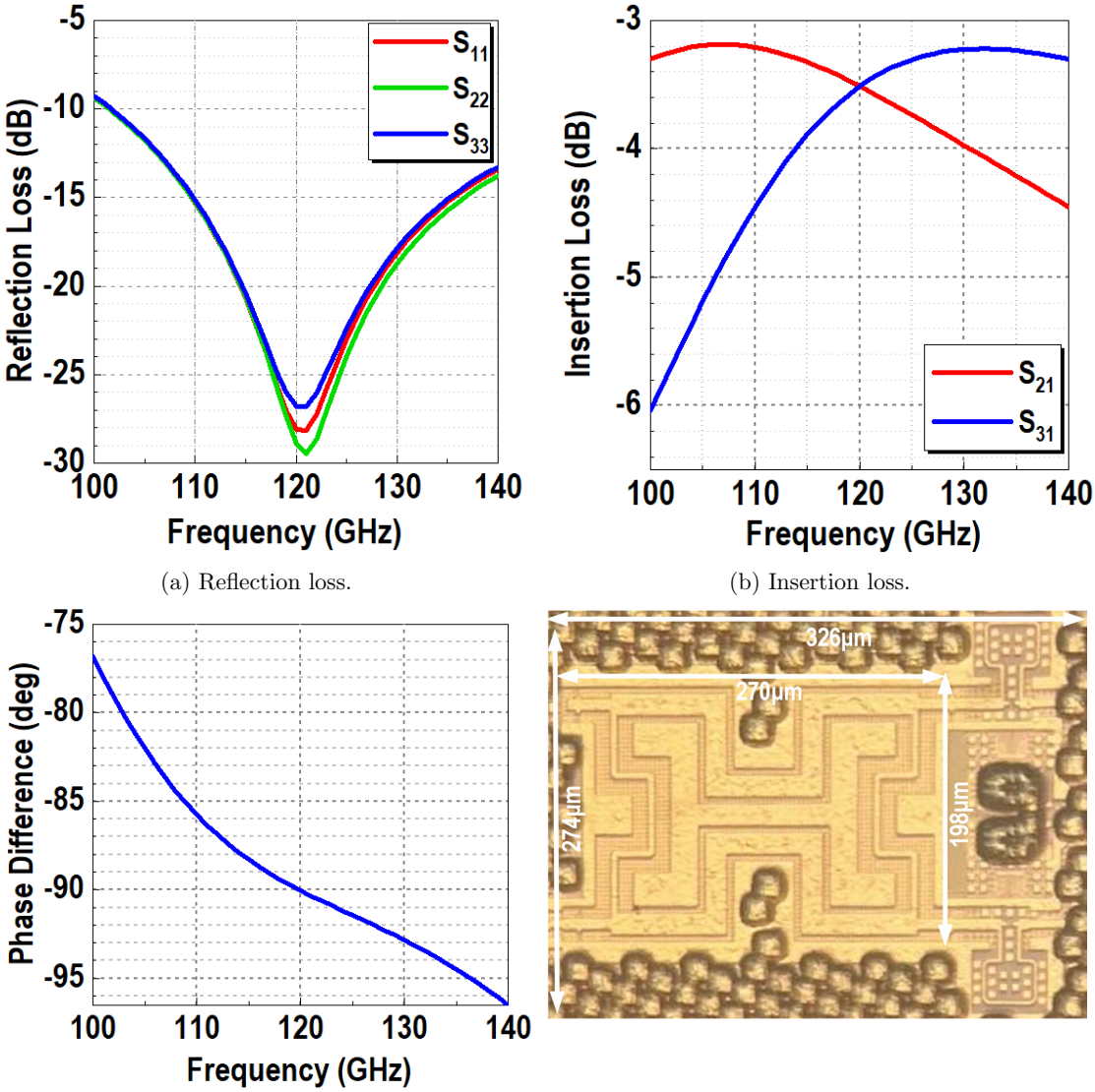


Figure 3.16: Schematic of IQ clock generation.

which poses challenges within our system-level architecture. The critical concern arises from the long transmission line length in the vertical direction, θ_2, which determines the vertical length of the entire QPSK sub-TX. This, in turn, directly influences the routing length from the PA output to the power combiner. The insertion loss incurred by this routing critically affects the total output power P_{out} of the TX. To address these constraints and optimize the system design, unequal line lengths in the couplers have been utilized[31], in which the vertical length is determined by $\theta_2 = \arcsin(Z_0/Z_2)$, where Z_2 is the characteristic impedance of the vertical branch line and Z_0 is the reference impedance which is normally $50\,\Omega$. Increasing Z_2 will reduce the routing length θ_2. A loaded capacitor at both ends of the transmission line is also introduced to further reduce the length while adding another degree of design freedom (Figure 3.4)[32].

To address PVT variations and IQ phase mismatches, a low pass phase shifter using a 60 pH inductor and a PMOS varactor was developed, offering a 10° tuning range. This grants phase alignment for the IQ calibration process mentioned in Section 2.1(Figure 3.16). Additionally, a 120 GHz buffer post-phase shifter balances LO amplitude across each IQ path at its saturation while providing ample power to drive the modulator. The microphotograph of the 90 branch-line coupler and the phase shifter is shown in Figure 3.17d which occupies



(a) Reflection loss.

(b) Insertion loss.

(c) Phase difference..

(d) Micro-photograph.

Figure 3.17: Simulated performance of the IQ branch-line coupler and micro-photograph of the fabricated IQ clock generation block.

an area of $326 \times 274\,\mu m^2$. The simulated performance of the branch-line coupler is shown in Figs. 3.17a-3.17c, demonstrating a matching of ¡-10 dB for 102-140GHz range, insertion loss of 3.6 dB and -90 phase difference at the carrier frequency of 120 GHz.

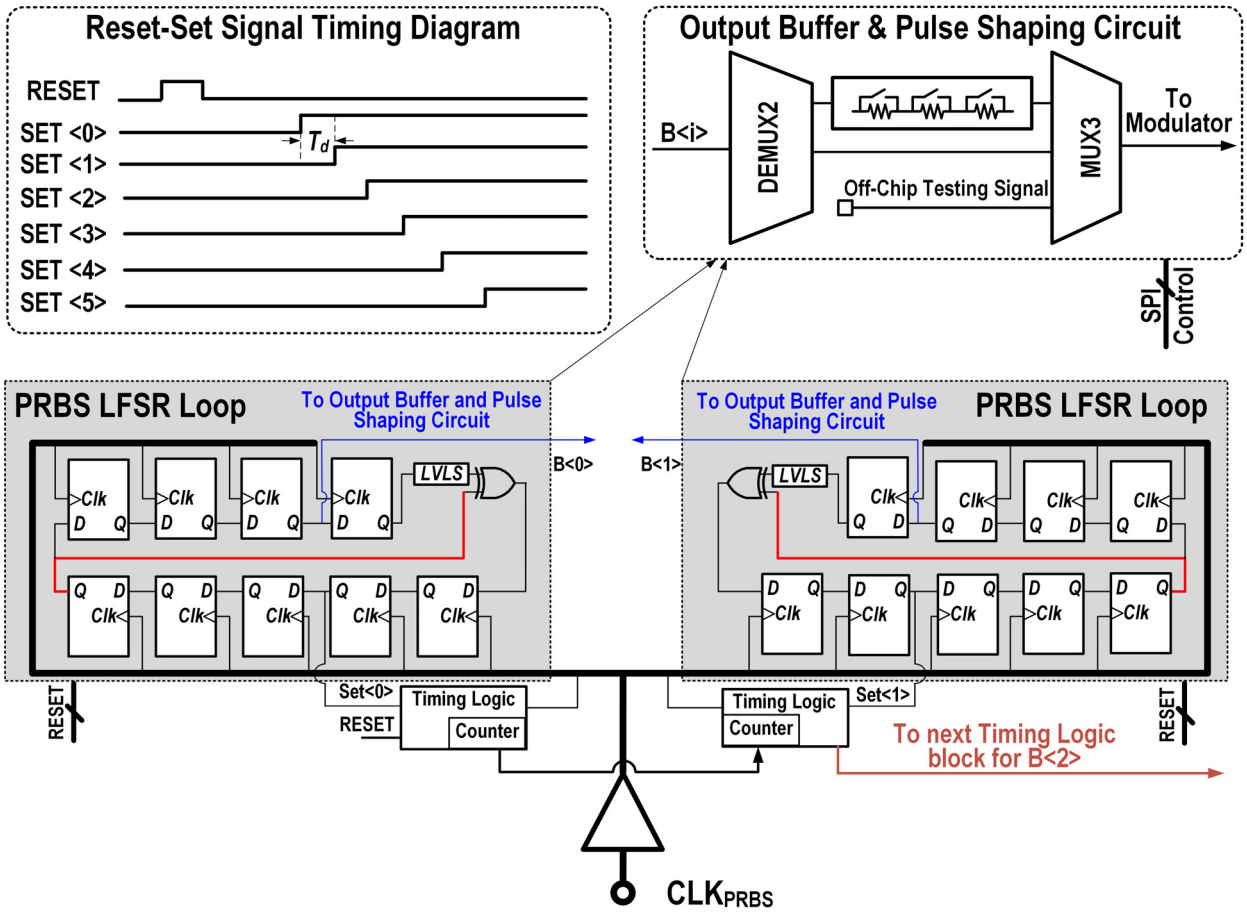


Figure 3.18: Proposed $2^9 - 1$ PRBS generation circuit diagram.

3.6 PRBS Generation

To fully exploit the capabilities of our TX and ensure a thorough evaluation of baseband signal distribution and upconversion, we designed an on-chip high-speed $2^9 - 1$ PRBS generator to maintain uniformity in constellation distribution while conserving hardware resource overhead. Each QPSK sub-TX employs a pair of PRBS blocks in its I and Q paths, necessitating six uncorrelated PRBS bit streams, namely $B\langle 0\rangle$ to $B\langle 5\rangle$. Traditional methods to generate uncorrelated PRBS sequences by modifying XOR input locations within the linear feedback shift register (LFSR) loop (red wires in Figure 3.18) are constrained by the number of registers, permitting a limited number of permutations in configuration. This limitation maintains a high correlation between adjacent bit streams, $B\langle i\rangle$ and $B\langle i+1\rangle$.

To address this challenge, we propose to delay the cyclic pattern by $T_d = \lfloor (2^M - 1)/K \rfloor \cdot T_{PRBS}$ bit periods to minimize the correlation between $B\langle 0 \rangle$ to $B\langle K-1 \rangle$, where M is the PRBS order, K is the total number of bit streams, T_{PRBS} is the PRBS clock period, and $\lfloor \cdot \rfloor$ denotes the floor function. Figure 3.18 demonstrates the proposed PRBS generator, where for clarity and simplicity, only $B\langle 0 \rangle$ and $B\langle 1 \rangle$ are shown. To start this PRBS generator, an off-chip $RESET$ signal brings all six LFSR loops to a synchronized logic zero state. Referring to Figure 3.18, this $RESET$ signal is processed by timing logic circuits to generate $SET\langle 0 \rangle$ to $SET\langle 5 \rangle$ to initiate six LFSR loops, where T_d is generated by a counter driven by $\mathrm{CLK_{PRBS}}$. Upon generation, $B\langle 0 \rangle$ to $B\langle 5 \rangle$ are routed through a transmission-line distribution network to each sub-TX in pairs, synchronized with the clock signal. The entire distribution network was modeled in Sonnet to guarantee the simultaneous arrival of all six bit-streams and synchronization of the three local PRBS clocks. Before integration into the modulator, each $B\langle i \rangle$ passes through a DEMUX-MUX network, which includes local D flip-flop buffers. Controlled by SPI, this network facilitates pulse shaping via a switched-RC mechanism and provides an off-chip testing pin, enabling quadrature upconversion sensing a single carrier for characterization of image-reject-ratio (IRR). This PRBS design method ensures the bit streams are highly uncorrelated, allowing for the reuse of the LFSR loops.

Chapter 4

Measurement Setup and Results

4.1 PCB Design and Chip Assembly

Fabricated in a 45-nm CMOS SOI process, the TX die photo is depicted in Figure 4.1, occupying an area of $4.5\times2.8\,\text{mm}^2$. To realize the backside radiation, careful consideration was given to both the PCB design and the assembly process. At the outset, a hyper-hemispherical high-resistivity float-zone silicon (HRFZ-Si) lens with a 12 mm diameter was selected to enhance backside radiation. A fused silica wafer was diced into square tiles of $1.5\times1.5\,\text{cm}^2$, where each tile served as the substrate for assembly. As depicted in Figure 4.2a, a three-dielectric-layer PCB was engineered to evaluate the chip's performance. The foundational dielectric layer employs a 1.6 mm thick FR-4, chosen for its durability and resistance to thermal deformation, thus minimizing warping during the PCB assembly and chip-bonding process. The incorporation of the chip, approximately 300 μm thick, introduced challenges in wire bonding due to the requirement for <0.2-mm height difference between the bonding interfaces[1]. To address this challenge, a Rogers RO4350B material of 0.1 mm thickness, featuring 0.5 oz copper on the top and bottom sides, was adopted as the top layer. This ar-

[1]This requirement may differ among various packaging companies.

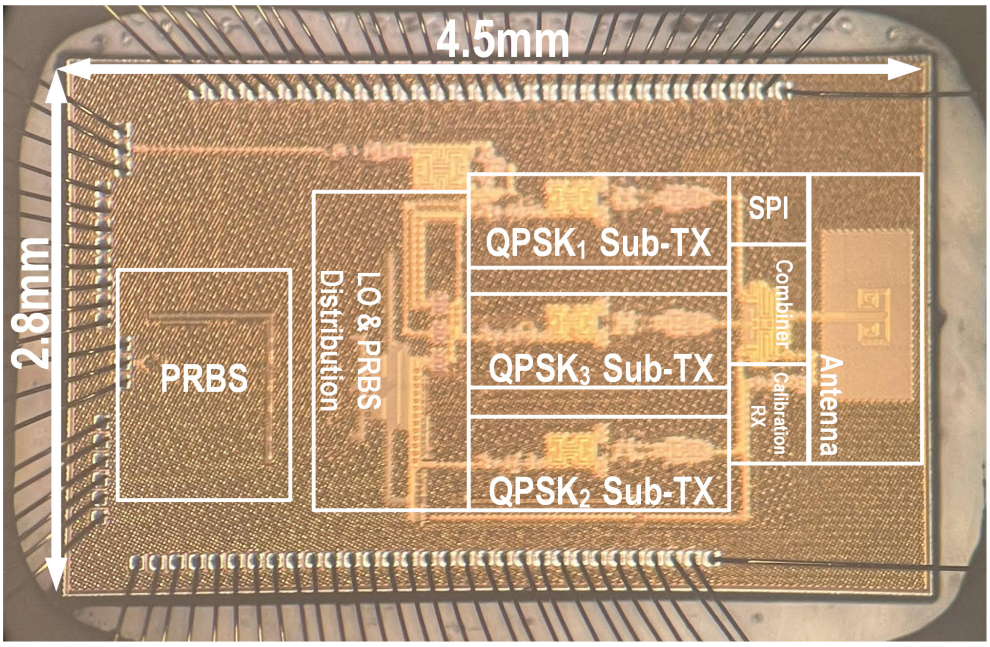
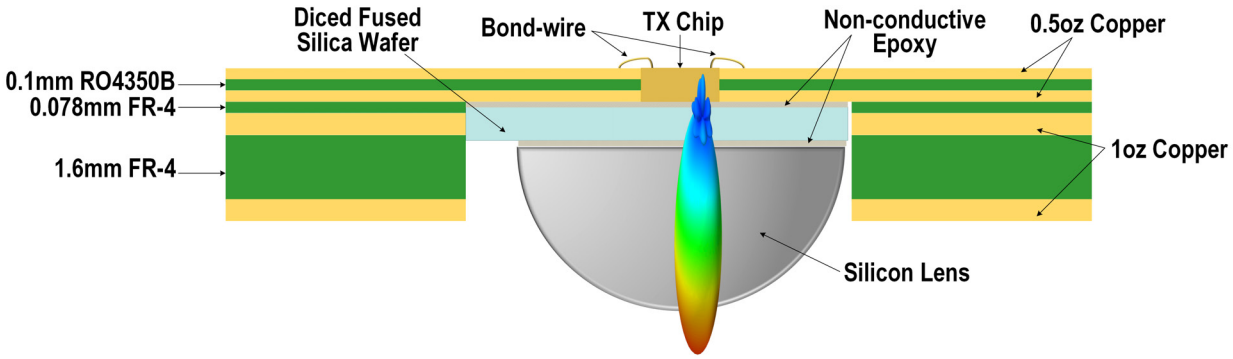
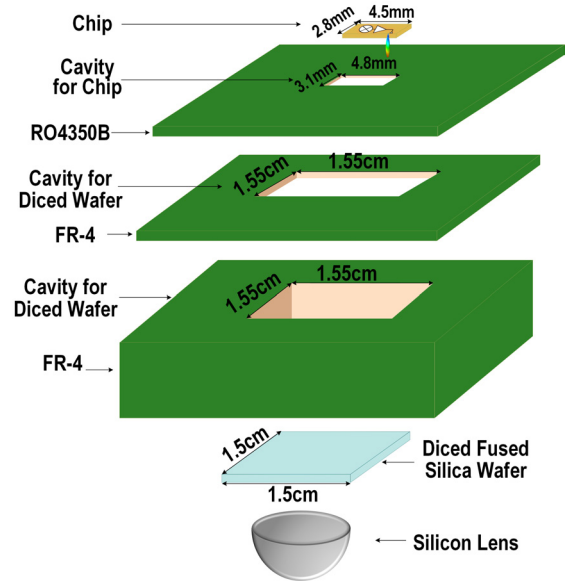


Figure 4.1: Micro-photograph of the bits-to-antenna RF-64QAM TX chip.

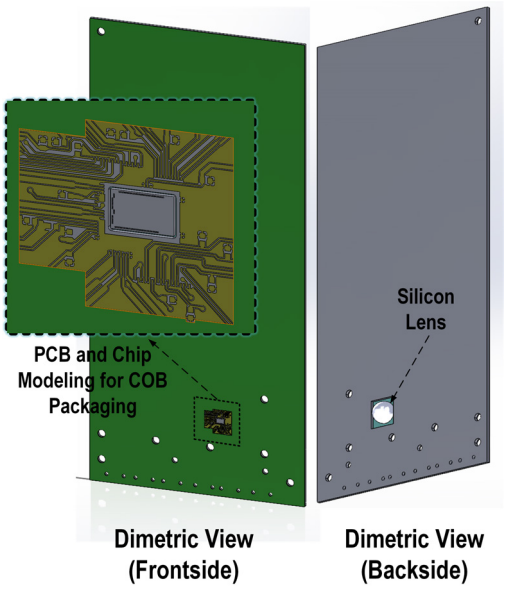
rangement, matching the chip's thickness and including a $4.8\times3.1\,\mathrm{mm}^2$ cavity (Figure 4.2b), ensures the chip can be positioned within the cavity, aligning with the electrical characteristics projected in simulations. The choice of RO4350B material, with its dielectric constant ϵ_r of approximately 3.6 at 30 GHz, supports good input impedance matching at mm-wave frequencies. An intermediate FR-4 layer enhances the PCB's layout flexibility for DC and low-frequency signal routings. The design's feasibility and structural integrity were verified through SolidWorks modeling, with dimetric views from both the front and back sides presented in Figure 4.2c. Non-conductive epoxy (EPO-TEK® 353ND) with an ϵ_r of about 3.2 was used to stick the silica wafer to the chip, PCB, and silicon lens. A cross-sectional view in Figure 4.2a demonstrates the complete assembly of the TX system.



(a) Cross-section diagram for final assembled chip and silicon lens.



(b) PCB stack-up and cavity openings diagram



(c) Dimetric views in SolidWorks for chip assembly.

Figure 4.2: TX chip assembly and PCB stack-up.

4.2 Measurement Setups and Results

4.2.1 Continuous-wave measurements

A continuous wave test was conducted on the chip, mounted on a 3D rotatable holder at a distance of 10 cm, to evaluate the TX radiation pattern at the carrier frequency of 120 GHz, as depicted in Figure 4.3. A Rohde & Schwarz® SMA100B sent a 30 GHz signal to the chip as the LO input. A Keysight® arbitrary waveform generator (AWG) generated a low-frequency

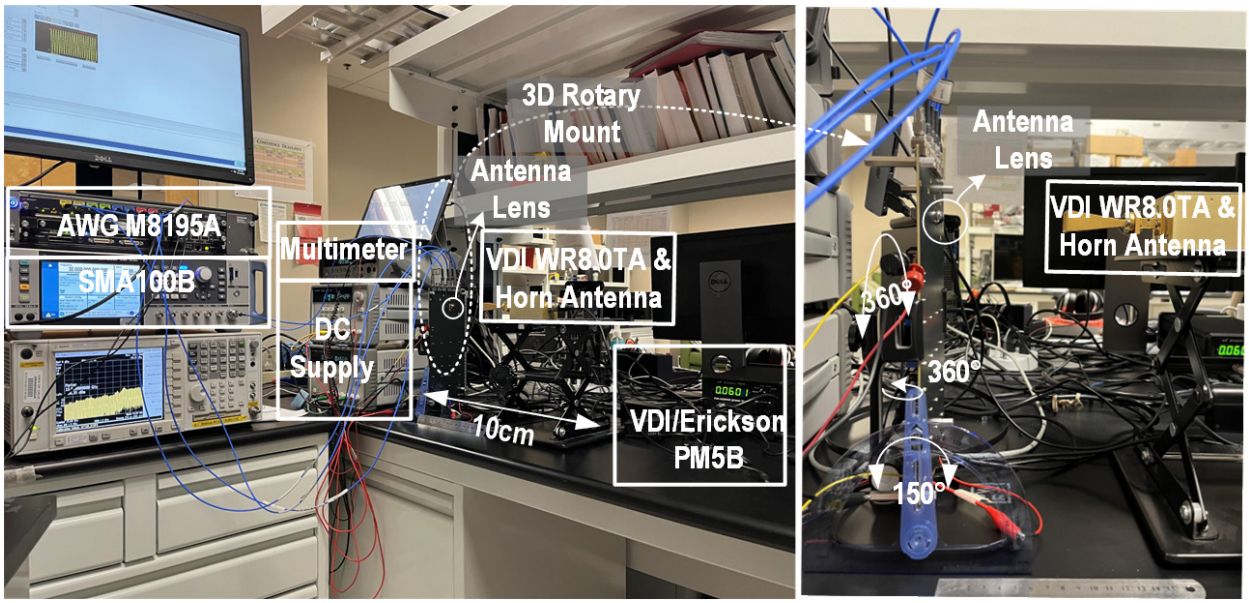


Figure 4.3: Setup for antenna radiation pattern measurement.

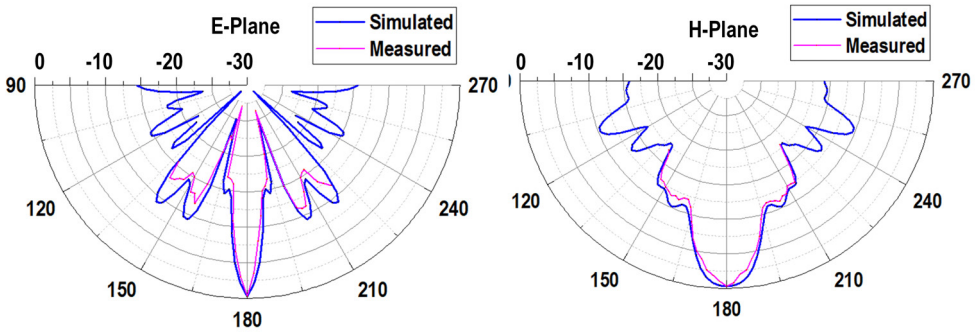


Figure 4.4: Normalized radiation pattern of TX prototype at carrier frequency.

single-tone signal to act as the on-chip baseband signal, bypassing the PRBS generator in all continuous wave tests. The received power was measured using a VDI/Erickson® PM5B power meter, connected through a waveguide taper from WR10 to WR8.0 (WR8.0TA). The free-space path loss (FSPL) was estimated by the Friis formula[33]:

$$FSPL\ (dB) = 20\lg(d) + 20\lg(f_c) + 20\lg(\frac{4\pi}{c}) \tag{4.1}$$

where d is the distance between TX and RX, f_c is the carrier frequency, and c is the speed of light. In this setup, the FSPL was calculated to be 54 dB at 120 GHz. The measured

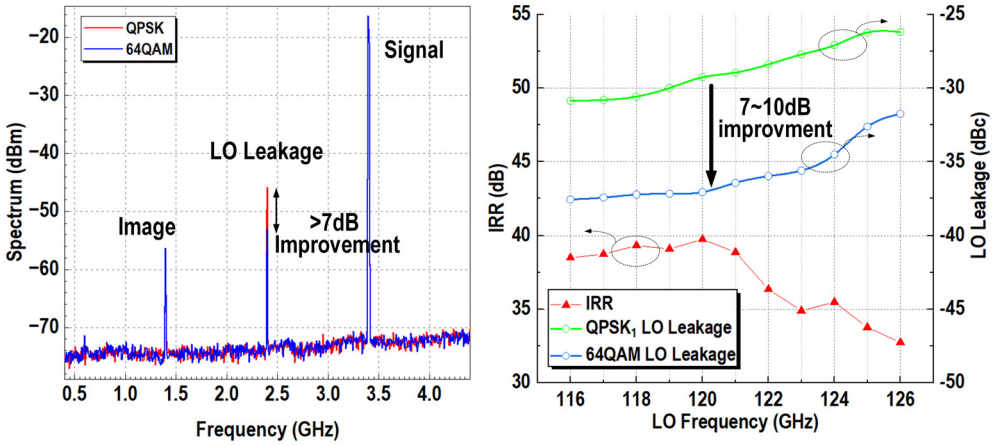


Figure 4.5: Measured LO leakage cancellation and IRR results

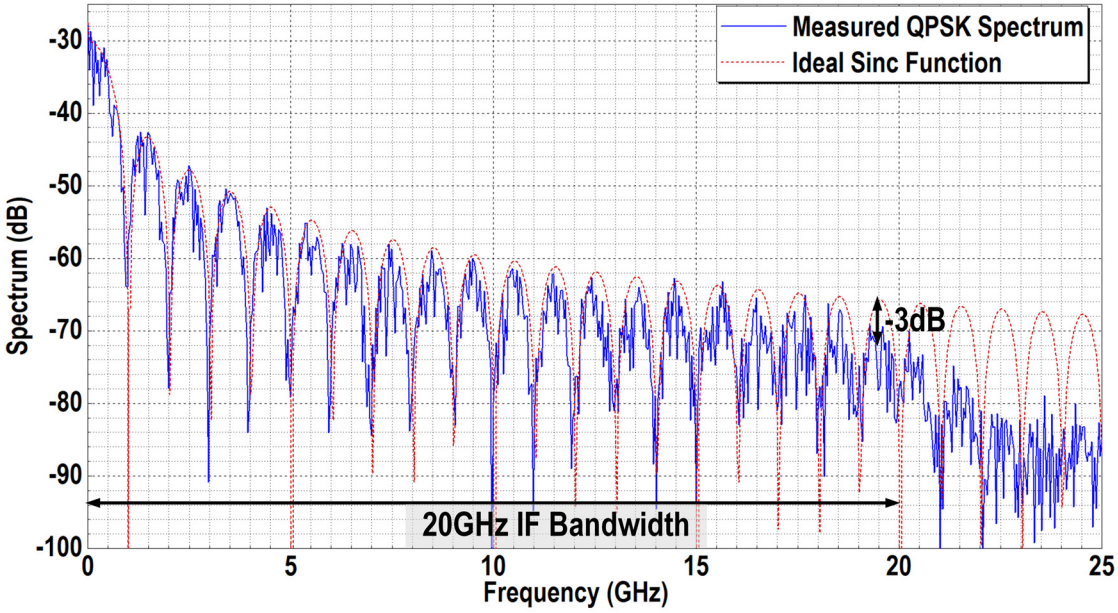


Figure 4.6: Downconverted zero-IF spectrum of 1 GBd QPSK signal.

power from PM5B varied between -14 dBm to -13 dBm in multiple test runs. Accounting for the 24 dBi standard gain of the horn antenna and the reported loss of 0.2 dB of WR8.0TA by VDI®, this translates to a worst-case measured EIRP of 16 dBm. A rotatable holder, shown in Figure 4.3, enabled 3D rotation of the TX for comprehensive radiation pattern measurement. The measured normalized radiation pattern results, displayed in Figure 4.4, closely follow the simulation results in HFSS.

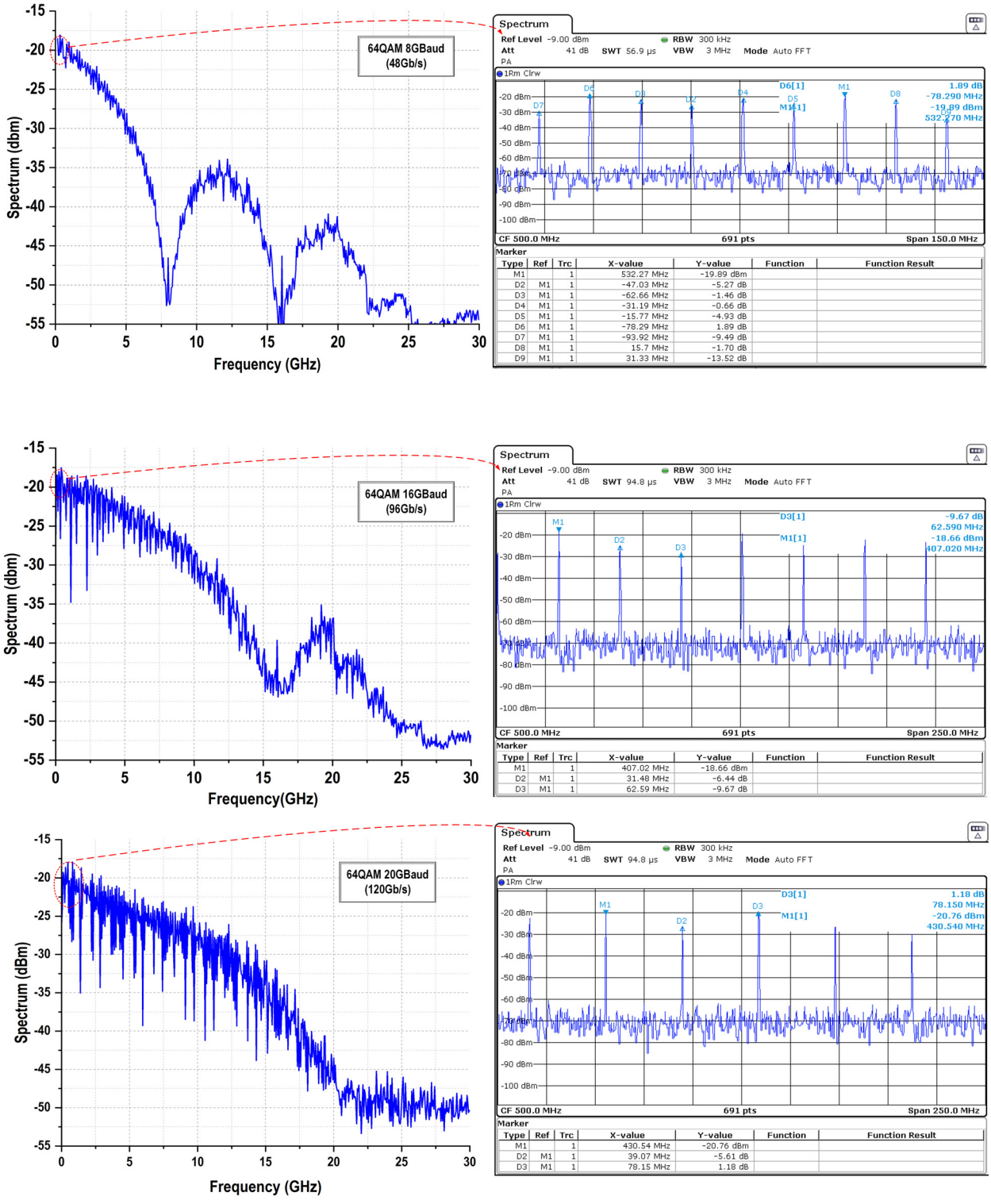


Figure 4.7: Downconverted 64QAM spectrum for 8 GBd, 16 GBd, and 20 GBd.

Hartley modulator tests were also performed on the TX by transmitting IQ single-tone signals from Keysight® M8195A AWG and bypassing the on-chip PRBS block. To verify

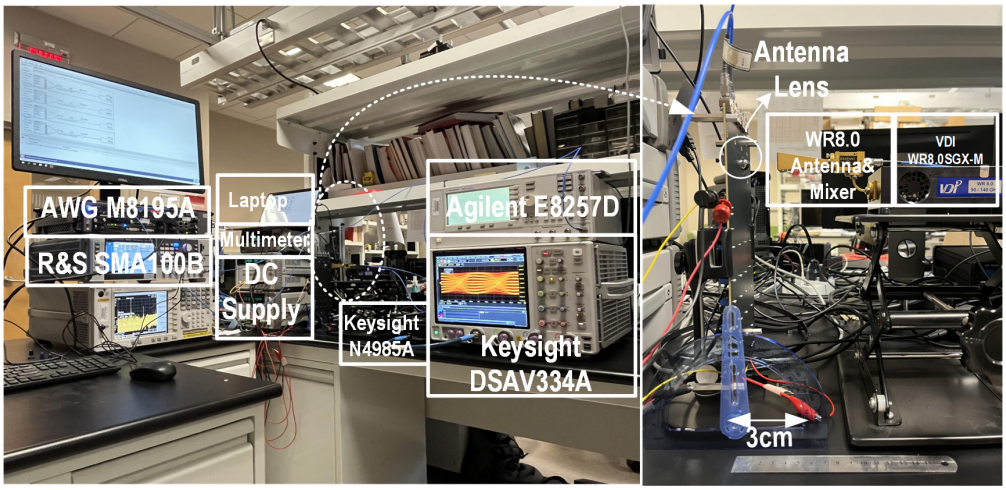
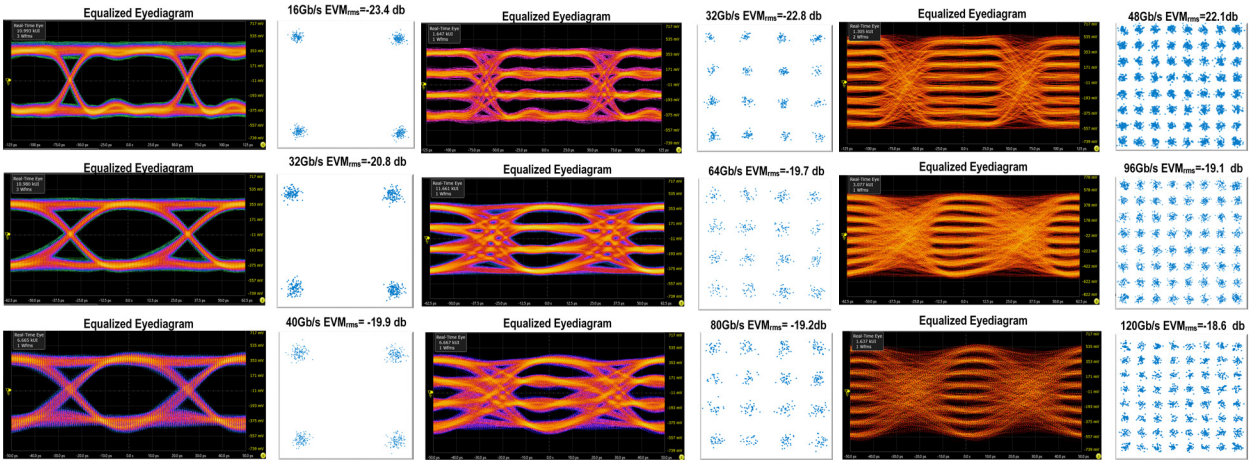


Figure 4.8: Setup for real-time oscilloscope measurement.



(a) QPSK. (b) 16QAM. (c) 64QAM.

Figure 4.9: Measured equalized eyediagrams and constellations.

our LO leakage suppression concept, Hartley tests were conducted on both the QPSK_1 sub-TX and the entire 64-QAM TX. The outcomes, including LO leakage and the 64-QAM TX IRR, are depicted in Figure 4.5. An exemplary down-converted spectrum[2] is shown on the left side of Figure 4.5. From the results in Figure 4.5, it is evident that the proposed LO leakage cancellation technique enhanced the overall LO feedthrough by $7 \sim 10\,\text{dB}$ in the RF-64QAM scheme in comparison to a single QPSK sub-TX. Moreover, the measured IRR for this prototype is $> 32\,\text{dB}$.

[2]A signal at $1 + 120 = 121\,\text{GHz}$ was down-converted by a signal of $9.8 \times 12 = 117.6\,\text{GHz}$ from the VDI signal generator frequency extender.

Table 4.1: Comparison of the prototype with state-of-the-art

	This Work	[34]	[35]	[8]	[36]	[37]	[38]	[39]
Technology	**45nm SOI**	28nm CMOS	22nm FinFET	180nm SiGe	45nm SOI	16nm FinFET	45nm SOI	22FD-SOI+InP HBT
Architecture	**Direct Mod.**	Direct Mod.	I/Q DAC	Direct Mod.	I/Q DAC	I/Q DAC	I/Q DAC	I/Q DAC
D/AInterface	**Integrated 1-bit**	Integrated 1-bit	Integrated 2-bit⋆	Integrated 1-bit	External AWG	External AWG	External AWG	External AWG
Modulation	**64QAM**	16QAM	16QAM	16QAM	64QAM	16QAM	64QAM	64QAM
Carrier Frequency (GHz)	**120**	135	140	115	149	109,135	143, 152	149
Antenna	**On-chip +Silicon Lens**	Off-chip	-	Off-chip	Off-chip	Off-chip	PCB +Flat Lens	LTCC
EIRP (dBm)	**16**	8	-	N.M.	8.3	N.M.	16.4	27.5
Pout (dBm)	**1.4**	0	0.8	1	0.1	-5	-9.6	20.5
DR (Gbps)	**120**	32	160†	20	84.48	120	57.6	30
Pdc (mW)	**880**	287	173	520	420	584.5	1580	760
Eff. (pJ/bit)	**7.33**	9	1.1	26	4.97	4.87	27.4	25.3

N.M.= Not mentioned. ⋆ Insufficient SQNR for practically attainable EVM and INL/DNL[6]. †No wireless meaurement.

4.2.2 Modulated-signal measurements

As discussed in Section 3.4 and illustrated in Figure 3.14b, our LO chain design prioritizes power efficiency over bandwidth expansion. This design choice precludes the possibility of evaluating our TX bandwidth by sweeping the LO signal across the entire RF spectrum. Instead, we adopted an alternative approach for bandwidth measurement, inspired by the methodology presented in [35]. By activating only a single sub-TX and transmitting a 1 GHz PRBS signal, we were able to assess the TX bandwidth. The measured QPSK spectrum in Figure 4.6 shows a 3 dB drop at 20 GHz from the ideal function, indicating a 40 GHz RF bandwidth. Figure 4.7 displays the measured spectrum at 30-cm TX-RX distance for the downconverted 64QAM signals at 8 GBd, 16 GBd and 20 GBd, captured using a Rohde & Schwarz® FSVA40 signal analyzer. For the proposed PRBS pattern of $2^9 - 1$, the beating frequency difference Δf_B is derived to be

$$\Delta f_B = \frac{f_{BD}}{2^9 - 1} \tag{4.2}$$

where f_{BD} represents the baud rate of the baseband signal. Accordingly, we anticipate Δf_B to be 15.66 MHz, 31.31 MHz, and 39.1 MHz for baud rates of 8 GBd, 16 GBd, and 20 GBd, respectively. The right side of Figure 4.7 provides a zoomed-in view of the spectrum, confirming our expectations. Additionally, a 3 cm wireless link measurement was performed by downconverting the signal through an F-band balanced mixer, followed by demodulation using a Keysight® DSAV334A 33-GHz real-time oscilloscope for eyediagrams and a Tektronix® DPO77002SX 70-GHz ATI performance oscilloscope for real-time data capture and processing for constellation and EVM analysis. The limited transmission distance is primarily due to significant path loss at this carrier frequency further exacerbated by the absence of a low-noise amplifier in the off-the-shelf RX, the integrated noise across a 40 GHz RF bandwidth, and the sensitivity constraints of the wideband oscilloscope. These factors are critical for achieving a discernible eye-opening for the 64QAM signal. The measured eye diagrams for QPSK (utilizing QPSK_1 sub-TX alone), 16QAM (employing both QPSK_1 and QPSK_2 sub-TXs), and 64QAM, obtained through the oscilloscope's internal continuous-time linear equalizers (CTLE) and decision feedback equalizers (DFE), are displayed in Figure 4.9. The distinct eye-openings at 48 Gbps and 120 Gbps affirm the performance of the proposed RF-64QAM TX. Furthermore, the equalized 64QAM constellation diagram at 120 Gbps exhibited an EVM_{rms} of -18.6 dB. A comprehensive performance summary of the RF-64QAM prototype alongside a comparison with state-of-the-art is presented in Table 4.1. This prototype represents a complete fully integrated bits-to-antenna 64QAM transmitter capable of ¿100 Gbps transmission, paving the way for next-generation wireless communication.

Chapter 5

Conclusion

A comprehensive CMOS single-chip solution for $> 100\,\text{Gbps}$ 64QAM tailored for 6G applications is presented. The F-band RF-64QAM TX prototype was fabricated in 45 nm CMOS SOI. The demonstrated performance showcased 120 Gbps wirelessly measured data rate with an EVM_{rms} of -18.6 dB. The measured EIRP was reported to be at approximately 16 dBm, coupled with a power efficiency of 7.3 pJ/b. Additionally, this TX successfully achieved an LO leakage cancellation of over 7 dB, further enhancing the overall performance of the system.

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Appendix A

The π-model inductances for weak coupling case

In this appendix, we aim to demonstrate that in a π-model of a transformer, all inductances exceed the original values of the two coils when these are weakly coupled. This insight is particularly valuable for designers working at sub-terahertz frequencies, where inductor size or self-resonance frequency could be design-limiting factors.

Given the π-model inductance values as outlined in equation (3.9), we define weak coupling as the condition where the mutual inductance $M < \min(L_s, L_p)$. Examining the difference between L_1 and L_p, we derive:

$$L_1 - L_p = \frac{M(L_p - M)}{L_s - M} > 0 \tag{A.0.1}$$

Similarly, for L_3 compared to L_s, we have:

$$L_3 - L_s = \frac{M(L_s - M)}{L_p - M} > 0 \tag{A.0.2}$$

(A.0.1) and (A.0.2) confirm that L_1 and L_3 in a π-model are invariably larger than the original values of the two coils, suggesting that by strategically tuning L_2, the inductor footprint can be made more compact and the self-resonance frequency of these inductances could be increased, which is beneficial for sub-terahertz designs.

To assess L_2, we examine the function $f(k) = (1 - k^2)/k$ and its first order derivative:

$$\frac{df}{dk} = -\frac{1}{k^2} - 1 < 0 \tag{A.0.3}$$

which holds true for all possible k values. And from (3.9b) we know that $L_2 = f(k)\sqrt{L_p L_s}$, will increase if k gets smaller. Given practical constraints at sub-THz frequencies, including skin and proximity effects as well as parasitics inherent to the technology, k generally remain below 0.6. This results in $L_2 > 1.067\sqrt{L_p L_s}$ across the board for sub-THz designs. Specifically, for our case that $k \simeq 0.2$, L_2 is roughly four times larger than the root average of individual inductances.