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Implantable Neural Recording Front-Ends for Closed-Loop Neuromodulation Systems

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy in Electrical Engineering

by

Hariprasad Chandrakumar

2018
ABSTRACT OF THE DISSERTATION

Implantable Neural Recording Front-Ends for Closed-Loop Neuromodulation Systems

by
Hariprasad Chandrakumar
Doctor of Philosophy in Electrical Engineering
University of California, Los Angeles, 2018
Professor Dejan Marković, Chair

The goal of neuromodulation is to alter neural activity through targeted delivery of a stimulus to specific sites in the body. A prominent example of neuromodulation is deep brain stimulation (DBS), which has proved effective in mitigating the effects of certain neurological conditions. However, existing neuromodulation treatments lack real-time feedback (simultaneous sensing) to adapt stimulation parameters in response to brain dynamics. Hence, neuroscientists and clinicians aim to perform closed-loop neuromodulation, where stimulation can be optimally controlled in real time for better treatment outcomes. In recent years, the community has emphasized closed-loop neuromodulation as a highly desirable tool for administering therapy in patients suffering from drug-resistant neurological ailments. A miniaturized autonomous implant would be instrumental in ensuring that neuromodulation achieves its full potential.

A key requirement for any closed-loop neuromodulation system is the ability to record neural signals while concurrently performing stimulation. However, neural stimulation generates large differential and common-mode artifacts at the recording sites, which easily saturate existing implantable recording front-ends due to their limited linear input range. To observe the neural
response during stimulation, the front-end must faithfully digitize neural signals in the presence of large stimulation artifacts. The front-end must also satisfy strict constraints on power consumption, noise and input impedance, while achieving a small form-factor. State-of-the-art neural recording front-ends do not meet these requirements.

This work presents a recording front-end that can digitize neural signals in the presence of 200mV\textsubscript{pp} differential artifacts and 700mV\textsubscript{pp} common-mode artifacts. The front-end consists of a chopper amplifier and a 15.2b-ENOB continuous-time delta-sigma ADC. In the design of the chopper amplifier, new techniques have been proposed that introduce immunity to common-mode interference, increase the DC input impedance (Z\textsubscript{in}) of the chopper amplifier to 1.5GΩ, and enable the realization of large resistances (90GΩ) on-chip in a small area for filtering electrode offsets. In the design of the delta-sigma ADC, a modified loop-filter is used along with new linearization techniques to significantly reduce power consumption in the ADC. These techniques enable our recording front-end to achieve a dynamic range of 90dB (14b ENOB) in 1Hz - 200Hz, and 81dB (12.7b ENOB) in 1Hz - 5kHz. Implemented in a 40nm CMOS process, the prototype occupies an area of 0.113mm\textsuperscript{2}/channel, consumes 7.3µW from a 1.2V supply, and can digitize neural signals from 1Hz to 5kHz. The input-referred noise is 1.8µV\textsubscript{rms} (1Hz - 200Hz) and 6.35µV\textsubscript{rms} (1Hz - 5kHz). The total harmonic distortion for a 200mV\textsubscript{pp} input at 1kHz is −81dB. Compared to state-of-the-art neural recording front-ends, this work improves Z\textsubscript{in} by 24.2x (for chopped front-ends), the linear-input range by 2x, the signal bandwidth (BW) by 10x, the dynamic range by 12.6dB, and tolerance to common-mode interferers by 6.5x, while maintaining comparable power and noise performance. The ADC alone consumes 4.5µW, has Z\textsubscript{in} of 20MΩ, BW of 5kHz, and achieves a peak SNDR of 93.5dB for a 1.77V\textsubscript{pp} differential input at 1kHz. The ADC’s Schreier FOM (using SNDR) is 184dB, which is 6dB higher than the state-of-the-art in high-resolution ADCs.
The dissertation of Hariprasad Chandrakumar is approved.

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2018
To Mom and Dad...
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CHAPTER 1

Introduction

1.1 Motivation for this work

The recordings of the electrical activity of neurons have been among the most important tools available in decoding the working of the brain [1]. The presence of “bio-markers” in neural recordings makes them indispensable for understanding brain function, in diagnosing neurological disorders like epileptic seizures, in the creation of brain-machine interfaces and for neuro-prosthetic technologies to aid paralyzed patients [2]-[4].

![Conventional neural recording systems](image)

Figure 1. Conventional neural recording systems.

However, most hardware solutions available for neural recordings are primarily wired or tethered setups with bulky rack-mounted electronics (Figure 1). The patient has wires coming out of their head or chest cavity through percutaneous connections. These wires carry the neural signals from the implanted electrodes to the external electronics that process these signals. Due to percutaneous connections, such a setup presents a significant risk of infection. Also, the mobility of the patient is severely limited, which may present problems in studies that need the patient to have normal mobility. This is also a major issue in animal studies that need the test animals to be socially active, freely moving about in an enriched environment with other animals. Hence, due to
the above constraints imposed by existing neural recording systems, the maximum duration of neural recordings is limited to about 30 minutes to at most a few hours. To overcome these constraints, we require a miniaturized, fully implantable, wireless neural recording system capable of recording from 100’s of channels. Such an implant will significantly reduce the risk of infection, not limit patient mobility, and increase the duration of neural recordings to several days or weeks as opposed to a few hours. Access to long-term neural recordings from the patient’s natural environment could lead to new insights in brain dynamics.

Figure 2. Simplified block-diagram of closed-loop stimulation.

1.2 Need for neural stimulation and closed-loop neural recording

Although neural recordings are invaluable, neural stimulation is necessary to administer therapy in patients suffering from neurological ailments that do not respond to pharmacological treatment [5]-[6]. Neural stimulation is performed by sending controlled current pulses into specific regions of the brain to modulate brain activity. Existing stimulation therapies rely on continuous open-
loop stimulation. Open-loop stimulation, though useful, can have detrimental side effects [7]-[8] while losing its efficacy over time due to plasticity and other changes in the brain. Hence, neuroscientists aim to perform closed-loop stimulation (Figure 2) where stimulation parameters are adapted in real time using recorded neural signals as feedback. This ensures that stimulation is applied only when necessary and with the required intensity, mitigating the undesirable effects of open-loop stimulation while maximizing the therapeutic benefits. Feedback also allows the stimulation parameters to track the dynamics of the brain, thus maintaining the therapeutic effects over time. Apart from therapy, a closed-loop neuromodulation system provides neuroscientists with an investigative tool to explore the workings of the brain. The next generation of neuromodulation systems requires implantable devices capable of closed-loop operation with 100s of recording channels.

1.3 Organization of this dissertation

Chapter 2 presents the characteristics of the desired neural signals along with the electrode-interface characteristics. This chapter also shows simple analyses to reveal the differential and common-mode nature of stimulation artifacts, along with estimates of their respective amplitudes. Chapter 3 discusses the comprehensive list of requirements for a closed-loop neural recording front-end. Chapter 4 presents design paradigms from state-of-the-art recording front-ends as seen in the published literature. This chapter reveals the strengths and pitfalls of the state-of-the-art, and compares their performance with the required performance for an implantable closed-loop neural recording front-end. In chapter 5, we discuss the architecture of the neural recording front-end proposed in this dissertation. Chapter 6 presents the high dynamic-range chopper amplifier that interfaces with the recording electrodes, along with new techniques that were developed to solve
several challenges in the design of this chopper amplifier. Chapter 7 presents a power-efficient high-resolution continuous-time delta-sigma ADC that was developed for the proposed neural recording front-end. This chapter presents power-reduction techniques and linearization techniques which result in the most power-efficient ADC proposed to date. Chapter 8 presents the performance of the complete front-end. Chapter 9 presents the conclusions drawn from this work, along with possible lines of future research. Finally, the appendix presents a direct-digitization sensing front-end using the proposed delta-sigma ADC, along with suitable modifications for various bio-signal recording applications.
CHAPTER 2

Neural signals and electrode-interface characteristics

2.1 Nature of stimulation artifacts

Figure 3. A closed-loop neural recording setup, leading to stimulation artifacts at the recording sites.

Figure 3 shows a typical setup for closed-loop neural recording. Due to direct conduction paths through the cerebro-spinal fluid (CSF), and capacitive coupling between traces from the electrodes to the recording electronics, large stimulation artifacts could appear at the recording sites. To estimate the amplitude of these stimulation artifacts, we use a simplified equivalent circuit (Figure 4) for simultaneous differential stimulation and recording. For peak stimulation current amplitudes of 3mA, and assuming that the tissue impedance between two local stimulation sites is about 600-800Ω (denoted by $2R_{\text{tissue}}$ in Figure 4) [9], the maximum voltage swing generated in the tissue ($V_1$ or $V_2$) is 0.9-1.2V. Note that the stimulator compliance voltage will be much higher to support the voltage drops across the electrode and trace impedances. These stimulation-induced tissue voltages will generate artifacts at the recording sites.
Figure 4. Simplified equivalent circuit to estimate artifact amplitudes at the recording sites.

However, since differential stimulation is employed (i.e. $V_1 = -V_2$), there will be partial cancellation of the artifacts appearing at the recording sites. Based on path mismatches due to electrode positions, tissue non-homogeneity etc, the residual artifact amplitude can be estimated. Assuming a maximum path-mismatch impedance of 50%, the residual artifact amplitude is 450-600mV$_{pp}$. Differential recording (or recording with respect to a local reference electrode) further attenuates artifact amplitudes in the sensing signal path. However, this attenuation is also limited to due to mismatches in the CSF and electrode impedances. If the worst-case attenuation of common-mode artifacts due to differential recording is about 15-20dB, then the maximum differential artifact amplitude ($V_3 - V_4$) is 75-100mV$_{pp}$.

Next, we consider the characteristics of the neural signals of interest.
Figure 5. Amplitude and frequency characteristics of recorded neural signals. The interferer denotes stimulation artifacts.

2.2 Signals of interest

From the analysis in the previous section, we see that the differential signal at the recording sites \((V_3-V_4)\) will contain large stimulation artifacts along with the neural signals of interest. This presents a significant challenge to the recording electronics, because the neural signals of interest also occupy the same frequency bands as the artifacts (Figure 5). The neural signals that are recorded by the electrodes occupy a frequency band from 1Hz to 5kHz. The various types of neural signals, along with their bandwidths and amplitudes are shown in Figure 5 [2], [8], [10]. The local field potentials (LFPs) occupy a frequency band from 1Hz to 200Hz, and the action potentials (APs) occupy a frequency band from 200Hz to 5kHz. The peak amplitude of LFPs is about 1mV,
and the peak amplitude of APs is about 100µV. The thermal and biological background noise picked up by the electrodes is about 10µVrms [11]. Thus, in the absence of stimulation artifacts, a recording front-end with a dynamic range of 45dB would suffice to faithfully digitize neural signals. However, the presence of in-band artifacts increases the required front-end dynamic range to 80dB. Since these artifacts occupy the same frequency band as the neural signals (Figure 5), conventional up-front filtering cannot be used to attenuate these artifacts. To ensure simultaneous recording during stimulation (which is necessary for closed-loop operation), the recording front-end must digitize neural signals to the required resolution of 7-8 bits in the presence of stimulation artifacts. Hence, the required signal to noise and distortion ratio (SNDR) for differential signals is >13 bits. Also, the recording front-end must achieve a 13-bit SNDR in the presence of 450-600mV common-mode artifacts. This is a non-trivial requirement, since front-ends are usually susceptible to large common-mode signals. This susceptibility is explained later in section 6.2.

2.3 Electrode-interface characteristics

Before designing a suitable neural recording system, the electrode-interface characteristics must be considered. The electrode can be modeled as a Thevenin equivalent circuit [12], as shown in Figure 6. The electrode-impedance is modeled by a parallel RC network (Re and Ce) in series with Rs. Re and Ce model the metal-electrolyte surface coupling, and Rs is the series resistance of the metal interconnect. The dominant components are Re and Ce, and their values vary widely depending on the electrode’s intended bandwidth, manufacturer, surface properties etc.

To get reasonable estimates of the electrode impedance, two types of electrodes (surface electrodes and depth electrodes) that are widely used were characterized for their impedance. Depth electrodes are very thin and are made to record individual cell activity. Their capacitance
(\(C_{el}\)) is about 1-10 nF and resistance (\(R_{el}\)) is about 200 M\(\Omega\). Surface electrodes are much larger, and they are designed to record the activity of groups of neurons. Their capacitance is about 3\(\mu\)F, and their resistance is about 10 k\(\Omega\). A common observation across various electrodes is that the electrode-impedance can be approximated as a capacitance (\(C_{el}\)) in the signal band of interest (Figure 6).

Figure 6. Equivalent model of a typical neural-recording electrode (left), and typical frequency characteristics of the electrode impedance (right).

Another observation is that the neural signal at the electrode is riding on top of a large DC offset voltage. This offset voltage develops at the electrode due to electro-chemical effects at the electrode-tissue interface. The value of this offset for differential recording from nominally identical electrodes can be up to 50-100mV [13]. These interface properties will inform our design choices in the recording front-end.

Based on the properties of neural signals, stimulation artifacts, and the electrode-interface characteristics, we consider the system requirements in the next section.
CHAPTER 3

System requirements

An implantable neural recording system needs to satisfy many design specifications to ensure functionality, patient safety, implantability and prolonged battery life. The requirement of a 13-bit SNDR in the presence of common-mode interferers has been explained in the previous section. The other requirements have been discussed in [14]-[16], which are summarized here. The power consumption of the neural recording front-end is limited by thermal dissipation constraints to prevent tissue damage [17], battery-life constraints, the number of recording channels used and the dissipation capabilities of the implant. Studies in [18]-[19] suggest that a dissipation of 10mW for a 6x6x2 mm$^3$ implant was low enough to avoid tissue damage. Assuming 50% power for stimulation and 50% power conversion efficiency, the power consumption of the neural recording front-end should be less than 10µW per channel for a few 100 recording channels. Since the background noise picked up by the electrodes in the AP band is about 10µV$_{rms}$, the input-referred noise of the recording front-end in the AP band should be 4-8µV$_{rms}$. LFPs are known to have amplitudes ranging from 10µV-1mV (cortical recordings), to 5-100µV (sub-cortical recordings) [13]. Given this range of amplitudes, and assuming a minimum SNR of 0dB, the front-end noise in the LFP band should be around 2-3µV$_{rms}$. Apart from neural signals and stimulation artifacts, a large DC offset (50-100mV) appears at the recording electrodes due to the electrochemical effects at the electrode-tissue interface [13]. This offset needs to be rejected to prevent saturation. Thus a high-pass filter with a corner frequency less than 1Hz is necessary to preserve the neural signals while attenuating the electrode offset. The electrode offset can create DC currents at the electrode due to the finite DC input-impedance of the recording front-end. Prolonged presence of DC
currents at the electrode can cause tissue damage. A DC input impedance $Z_{in}$ larger than $1\text{G}\Omega$ is required, since this limits the DC current to $50\text{pA}$ for an offset voltage of $50\text{mV}$, which is sufficiently low for most applications [20]. Also, the input-impedance in the frequency range of interest (1Hz – 5kHz) needs to be much larger than the Thevenin impedance of the electrode (~5nF) to prevent signal attenuation [12], [21]. Finally, the area per channel should be about $0.1\text{mm}^2$, so that ~100 recording channels can be packed in a reasonable area. These requirements are summarized in Table 1.

<table>
<thead>
<tr>
<th>Specification (per channel)</th>
<th>Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power ($\mu W$)</td>
<td>&lt; 10</td>
</tr>
<tr>
<td>BW (Hz)</td>
<td>1-5k</td>
</tr>
<tr>
<td>Noise ($\mu V_{rms}$)</td>
<td>4-8</td>
</tr>
<tr>
<td>DR (dB)</td>
<td>80</td>
</tr>
<tr>
<td>THD (dB)</td>
<td>$-80$</td>
</tr>
<tr>
<td>I/P swing ($\text{mV}_{pp}$)</td>
<td>&gt; 100</td>
</tr>
<tr>
<td>CM Tolerance ($\text{mV}_{pp}$)</td>
<td>&gt; 500</td>
</tr>
<tr>
<td>DC $Z_{in}$ (Ω)</td>
<td>&gt; $1\text{G}$</td>
</tr>
<tr>
<td>Area ($\text{mm}^2$)</td>
<td>&lt; 0.1</td>
</tr>
</tbody>
</table>

**Table 1.** Summary of requirements for an implantable neural recording front-end for closed-loop neuromodulation.
CHAPTER 4
Review of prior art

The most widely used topology for neural recording is shown in Figure 7. It consists of a low-noise high-gain amplifier to interface with the electrodes, followed by a moderate-resolution ADC. This topology is power-efficient, since the power consumption is limited by the LNA, which can be designed to optimize the power-noise tradeoff [11], [14], [22]-[24]. However, due to the high gain of the LNA (>40dB), the recording front-end saturates beyond an input amplitude of ~5mV, making them incapable of handling stimulation artifacts. “Blanking” has been proposed in [25], [26] to prevent saturation (Figure 8(a)). However, the neural signals of interest are lost during the presence of artifacts. Also, stimulation artifacts could last for several milliseconds or more when burst or periodic stimulation pulses are used, which would result in severe loss of neural data if blanking is used. Another technique [27] attempts to estimate the artifact using an adaptive filter in the digital domain, and cancel the artifact in the analog domain using mixed-signal feedback (Figure 8(b)). Artifact cancellation using feedback would significantly reduce the required dynamic range of the front-end. However, this technique was demonstrated for artifacts smaller than 3mV with long convergence times, which is insufficient for closed-loop recording.

Figure 7. Topology of a conventional neural recording front-end.
Figure 8. Techniques to prevent saturation in existing neural recording front-ends. (a) Blanking disconnects the front-end from the electrode during stimulation. (b) A coarse adaptive artifact estimation loop is employed to reduce the required front-end dynamic range.

Apart from the saturation problem due to high LNA gain, the LNAs demonstrated in the current state-of-the-art have several problems, which are discussed next.

The capacitively coupled inverting amplifier (Figure 9(a)) is among the most popular topologies used in neural recording front-ends [11], [14], [22]-[24]. Capacitive coupling ensures a large DC input-impedance, and sizing the input capacitance smaller than 100pF ensures negligible signal attenuation at the electrode. This topology has been optimized for power and noise, as
discussed in [14]. The input devices are sized to have a large area to minimize their flicker noise contribution. To achieve low-frequency high-pass corners, pseudo-resistors are used [14], as they are an area-efficient way to realize very-low frequency high-pass corners. However, pseudo-resistors are very nonlinear, and since they experience the full output swing $V_{out}$, they limit the linearity of the front-end to about 8 bits [23]. Pseudo-resistors are also very sensitive to process and temperature variation, as their resistance can vary by a factor of 100. In addition, any bulk leakage currents in the pseudo-resistor can create large DC bias shifts, leading to poor control of bias points in the front-end. These issues make the pseudo-resistor unreliable in a clinical setting [20].

The chopper-stabilized amplifier (Figure 9(b)) is another popular front-end topology for neural recording [13], [28]-[30], as chopping is an effective way to mitigate the low-frequency flicker noise of the opamp. A servo-loop is usually employed (Figure 10(a)) to attenuate the electrode offset at the output $V_{out}$, thus creating the required high-pass filter. However, chopping reduces the DC input impedance, since the passive mixer at the input along with the capacitance $C_{in}$ (Figure 10(a)) form a switched-capacitor resistance. For $C_{in}$ of 10pF and $f_{clk}$ of 20kHz (typical values for this application), the DC input impedance is limited to 2.5MΩ, which is significantly lower than the required 1GΩ. Off-chip coupling capacitors can be used to increase the DC input impedance [31], but they become impractical for a miniaturized implant with a large number of recording channels. To boost the input impedance, a positive-feedback loop (Figure 10(b)) has been used in [28]. The positive feedback path provides the required DC current to the switched-capacitor resistor at the input, which otherwise would have been supplied by the electrodes, thus boosting the DC input impedance to infinity. However, the positive feedback loop is sensitive to parasitic capacitance appearing at node n1 (denoted by $C_{bp}$ in Figure 10(b)), which limits the realized
impedance boost to a factor of 5 as opposed to the targeted boost of a factor of 100 in [28]. Another critical problem with this technique is that the positive feedback loop is driven by the output $V_{out}$. Any practical neural recording front-end would attenuate the DC signal at the output $V_{out}$. Thus the positive feedback loop is rendered inoperative at DC, where it is most needed.

Figure 9. Conventional neural recording amplifiers. (a) the capacitively coupled inverting amplifier. (b) the chopper-stabilized amplifier.
Figure 10. Techniques to enable chopper amplifiers for neural recording. (a) the DC-Servo loop to attenuate electrode-offsets. (b) the positive-feedback path to boost the input impedance.

Figure 11. A direct-digitization neural recording front-end [32], without a high-gain LNA.

Recently, a different front-end recording architecture was presented [32], where the LNA interfacing with the electrode was omitted, and a continuous-time (CT) ΔΣ-ADC was used to directly digitize the neural signals at the electrode (Figure 11). The absence of the high-gain LNA
resolved the problem of saturation in the recording architecture of Figure 7. However, the design in [32] had several problems. A multi-bit DAC was used in the feedback path of the ΔΣ-ADC, and no effort was made to mitigate the mismatch-induced nonlinearity of the DAC. Hence, the ENOB of this front-end was limited to 10.2b. Chopping was used to mitigate flicker noise, which reduced the DC input impedance to 30MΩ, while the required DC input impedance is >1GΩ. Finally, all the above-mentioned front-end topologies are susceptible to common-mode artifacts (discussed in section 6.2).

The current state-of-the-art in neural recording is summarized in Table 2. The state-of-the-art has successfully addressed power and noise. However, there are significant limitations in the linear input range, dynamic range, input impedance, tolerance to common-mode interferers and the signal bandwidth.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (µW)</td>
<td>2</td>
<td>7.6</td>
<td>1.8</td>
<td>2.3</td>
<td>8</td>
<td>&lt; 10</td>
<td></td>
</tr>
<tr>
<td>BW (Hz)</td>
<td>180</td>
<td>5.32k</td>
<td>700</td>
<td>300</td>
<td>500</td>
<td>1-5k</td>
<td></td>
</tr>
<tr>
<td>Noise (µV rms)</td>
<td>0.95</td>
<td>3.06</td>
<td>6.7</td>
<td>1.3</td>
<td>1.7</td>
<td>4-8</td>
<td></td>
</tr>
<tr>
<td>DR (dB)</td>
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<td>50</td>
<td>N.A.</td>
<td>50</td>
<td>73</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>I/P swing (mV pp)</td>
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<td>7.3</td>
<td>N.A.</td>
<td>1</td>
<td>23.2</td>
<td>&gt;100</td>
<td></td>
</tr>
<tr>
<td>CM Tolerance</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>DC Z in (Ω)</td>
<td>8M</td>
<td>∞</td>
<td>6M</td>
<td>28M</td>
<td>30M</td>
<td>&gt;1G</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Performance summary of current state-of-the-art neural recording front-ends.

The front-end topologies discussed above are candidate topologies for implantable neural recording front-ends. Commercial neural recording systems for clinical research are another category of recording hardware that can be considered. Examples of such systems can be seen in
Some of these devices do achieve the required large linear input signal range. However, these devices were not designed for implantable applications. Hence, these devices tend to be bulky, and their power consumption is far beyond the power budget of an implant. Figure 12 graphically depicts the contrast between state-of-the-art implantable recording front-ends and commercially available wall-powered devices. For a viable closed-loop implantable neural recording system, we need to achieve the large linear input range currently afforded by the wall-powered bulky devices, while keeping power consumption and device volume at the levels of current implantable systems.

**Figure 12.** Current landscape of neural recording front-ends, and comparison with our proposed recording system.
For the front-end topology shown in Figure 7, we have seen that a high-gain LNA leads to saturation of the front-end in the presence of stimulation artifacts, leading to a loss of signal information. We propose to use the same topology—however, the gain of the LNA is reduced by almost two orders of magnitude. By reducing the LNA gain, saturation is avoided at the output of the LNA (Figure 13) in the presence of artifacts. Hence, the neural signals of interest survive at the output of the LNA. If a suitable ADC is used to digitize the LNA output, the desired neural signal can be recovered in the digital domain by performing adaptive artifact rejection [99], [100].

**Figure 13.** Comparison of conventional neural recording topologies and the proposed front-end.

However, by reducing the gain of the LNA in Figure 13, the burden on the ADC has significantly increased in terms of achieving low noise and low distortion. Hence, the challenge
with the proposed approach is to realize the front-end within the same (or similar) power budget as the conventional front-end in Figure 7. The LNA is not removed completely, since the gain of the LNA eases the requirements of the ADC.

The proposed neural recording front-end is shown in Figure 14. It consists of a low-noise chopper amplifier with a gain of 8, followed by a 15.2b-ENOB continuous-time $\Delta\Sigma$-ADC. This front-end is capable of digitizing $2\text{mV}_{pp}$ neural signals in the presence of $200\text{mV}_{pp}$ differential artifacts, while remaining immune to $700\text{mV}_{pp}$ common-mode interferers. The signal at the output of the ADC consists of the sum of the desired neural signal and the differential artifact, and subsequent adaptive artifact rejection can recover the neural signal in the digital domain [99], [100].

The $\Delta\Sigma$-ADC proposed in this work can also be used as a stand-alone sensing front-end for bio-signal recording. This approach is discussed in the appendix.

**Figure 14.** A simplified diagram of the proposed neural recording front-end that is tolerant to large differential and common-mode artifacts.
This dissertation focuses on the design of the chopper amplifier and the ADC. Three prototype chips were fabricated and tested as shown in Figure 15. The first chip (Chip-1) consists of the initial version of the chopper amplifier. The second chip (Chip-2) consists of a substantially improved version of the chopper amplifier, which solved all the electrode-interface requirements. The final chip (Chip-3) presents the complete neural recording front-end, where a power-efficient continuous-time ΔΣ-ADC is introduced, along with a modified chopper amplifier (from Chip-2) to complete the front-end.

**Figure 15.** Fabricated prototypes of the neural recording front-ends in this work.

The next few chapters discuss the challenges and solutions proposed for the chopper-amplifier and the ΔΣ-ADC.
CHAPTER 6

A high dynamic-range, low-power, common-mode-artifact tolerant neural recording chopper amplifier

As mentioned in chapter 4, the chopper-stabilized amplifier (Figure 9(b)) is a widely used front-end amplifier for neural recording [13], [28]-[30], as chopping is an effective way to mitigate the low-frequency flicker noise of the opamp. However, the chopper amplifier has several limitations that make it unsuitable as a neural recording amplifier. Specific challenges include realizing very-low frequency high-pass corners for electrode-offset attenuation, preventing distortion due to large common-mode interferers, increasing the input-impedance and reducing output ripples. This chapter presents solutions for each of these problems. In the next section, we discuss the problem of realizing very-low frequency HP corners.

6.1 Realizing very-low frequency high-pass corners

As discussed in section 2, the neural signals at the electrodes (<2mV) are accompanied by electrode offsets as large as 100mV. Hence any amplification must be applied only to the neural signals while attenuating the offset to prevent saturation. Since the signals of interest occupy frequencies as low as 1Hz, a high-pass filter is necessary with a corner frequency less than 1Hz. Such low corner frequencies can be difficult to implement as they usually require very-large resistors and capacitors, making it prohibitively area expensive. Conventional capacitive-feedback amplifiers have been reported before [11], [14], [22]-[24], that use “pseudo-resistors” as large resistors to realize sub-Hz high-pass corners (Figure 9(a)). However, as discussed in chapter 4,
pseudo-resistors are unreliable due to its nonlinearity and sensitivity to process and temperature variations.

In chopper amplifiers, a DC-Servo loop can be used [28] to realize the required high-pass corner frequency. The DC servo-loop consists of a low-bandwidth integrator that is placed in a negative feedback loop around the chopper amplifier (Figure 10(a)). The high loop-gain of the servo-loop attenuates low-frequency signals at the output $V_{out}$, thus realizing the required high-pass corner. For frequencies beyond the unity-gain bandwidth of the servo-loop, the servo-loop is effectively broken. Hence, since the signal-band of interest lies beyond the servo-loop unity-gain bandwidth, the output noise of the servo-loop in the signal band will be amplified by $C_3/C_2$ and appear at $V_{out}$ (Figure 10(a)). The noise analysis of the servo-loop is presented in [13].

The capacitor $C_3$ is kept small to reduce the in-band noise contribution of the servo-loop integrator and $g_m$ [13]. The minimum value of $C_3$ is limited by the maximum electrode offset that needs to be attenuated [13], [28]. $C_3$ is chosen to be $C_1/10$ which is sufficient to attenuate differential electrode offsets up to ±50mV. For a high-pass corner frequency of $f_{HP}$ in the signal transfer function $V_{out}/V_{in}$, the unity-gain bandwidth of the servo-loop integrator is given by $f_{dwl,ugb} = f_{HP}(C_3/C_3)$. Hence for $f_{HP}$ of 1Hz, the servo-loop unity-gain bandwidth should be 0.5Hz. As discussed in chapter 4, pseudo-resistors are not viable in a closed-loop neural recording application. To realize such low corner frequencies in a reasonable chip area, switched-capacitor techniques [37] have been used in prior work [28]. However, switched-capacitor integrators significantly increase the noise of the recording front-end. When the servo-loop was enabled in [28], the measured input-referred noise increased from 0.7µV to 6.7µV in the band of 0.5Hz-100Hz. The wideband noise of the opamp and switches used in the switched-capacitor integrator gets aliased down to baseband, which results in a large in-band noise contribution from the servo-
loop integrator. Hence, switched-capacitor integrators, though an effective way to realize low-frequency corners in a small chip area, prove to be detrimental to the noise performance of the recording front-end.

![Diagram of duty-cycled resistor and its equivalent circuit](image)

Figure 16. (a) Concept of a duty-cycled resistor to realize a large resistance. (b) Low-pass filter using duty-cycled resistor. (c) Programmable pulse (1–15 ns) generator to drive duty-cycled resistor switches.

In this work, we propose to use duty-cycled resistors [38]-[43] to realize very-low bandwidth integrators. The following analysis shows that duty-cycled resistors are an effective way to realize large linear resistors in a small chip area. Since duty-cycled resistors are inherently time-varying, the analysis needs to account for frequency translations and aliasing effects. A duty-cycled resistor, shown in Figure 16(a), consists of a passive poly-resistor placed in series with a switch. When the switch is driven by a clock with a duty-cycle factor of D, then the average resistance observed across the terminals is given by R/D. This can be shown by analyzing the circuit in Figure 16(b).
If G(t) is the time-varying conductance of the duty-cycled resistor, then using KVL, the behavior of the circuit in Figure 16(b) can be described as

\[ V_{in}(t) \cdot G(t) = V_{out}(t) \cdot G(t) + C \frac{dV_{out}}{dt} \]  (1)

To get meaningful insight, we move to the frequency domain. The Fourier transform of G(t) is given by

\[ G(j\omega) = \sum_{k=-\infty}^{\infty} g_k \delta(\omega - k\omega_o) \]

where \( g_o = D/R \) and \( g_k = (2/Rk\pi)\sin(Dk\pi) \) are the Fourier coefficients corresponding to the waveform G(t). Hence, taking the Fourier transform of equation (1) leads to the following:

\[ g_o V_{in}(j\omega) + \sum_{k=-\infty}^{\infty} g_k V_{in}(j(\omega - k\omega_o)) = (g_o + j\omega C)V_{out}(j\omega) + \sum_{k=-\infty}^{\infty} g_k V_{out}(j(\omega - k\omega_o)) \]  (2)

We use two assumptions to simplify equation (2). If RC>>DT, where T is the period of the clock driving the switch in Figure 16(b), then \( V_{out}(\omega) \) is a low-frequency signal and the last term in equation (2) can be approximated to zero. Assuming that \( V_{in}(\omega) \) is a low-frequency signal, \( V_{in}(\omega - k\omega_o) \) can be neglected for \(|\omega| > \omega_o/2\). Since \( g_o = D/R \), equation (2) can be simplified to

\[ \frac{V_{out}(j\omega)}{V_{in}} = \frac{1}{1 + j\omega C \frac{R}{D}} \]  (3)

Equation (3) shows that if the two above-mentioned assumptions are true, then the circuit in Figure 16(b) is identical to a low-pass filter formed by a capacitor C and an equivalent resistor R/D. Thus, the resistance R is boosted by a factor of 1/D. A simple anti-aliasing filter can be used before the integrator to satisfy the assumption of \( V_{in}(\omega) \) being a low-frequency signal. With a pulse width of a few ns, and for a sampling clock frequency of 25kHz, it is possible to achieve duty-cycle factors
of 1/20,000 (as an example). Such small duty-cycle factors also ensure that the assumption of \( RC \gg DT \) is satisfied. Hence, a 1M\( \Omega \) poly-resistor can be boosted to 20G\( \Omega \). Poly-resistor resistance can vary by 25% across process corners. A pulse generator as shown in Figure 16(c) can be used to realize pulse widths of a few ns, with a pulse-width variation less than 10% across process corners. Thus, the overall variation of duty-cycled resistors is 35%, as compared to 100x variation for pseudo-resistors. Hence, duty-cycled resistors are a more reliable method to realize large resistors. Since the poly-resistor is inherently linear, the duty-cycled resistor achieves high linearity. By using variable capacitor loads in the pulse generator, the duty-cycle factor can be varied by a factor of 10, which translates to a 10x variation in the equivalent resistance, or a 10x variation in the corner frequency.

Since Figure 16(b) is a switched-capacitor circuit, it may suffer from the same noise degradation due to aliasing as seen in conventional switched-capacitor integrators. Hence it is essential to analyze the noise contribution of this circuit. The noise power spectral density (PSD) of the resistance \( R \) is given by \( 4kTR V^2/Hz \). Since the input \( V_{in} \) is now a wideband noise signal, equation (3) is not valid, and equation (2) can be written as

\[
\sum_{k=-\infty}^{\infty} g_k V_{in}(j(\omega - k\omega_o)) = (g_o + j\omega C)V_{out}(j\omega)
\]

(4)

The frequency-translated versions of \( V_{out}(\omega) \) are approximately zero if \( RC \gg DT \). The left-hand-side of equation (4) represents the resistor noise \( V_{in}(t) \) multiplied with \( G(t) \), and the right-hand-side represents the result of \( V_{out}(t) \) being passed through a filter with a frequency-response of \( g_o + j\omega C \). Hence, equation (4) can be simplified to the following:
\[ 4kTR \left( \sum_{k=-\infty}^{\infty} g_k^2 \right) = |g_o + j2\pi fC|^2 V_{out}^2(f) \]  

(5)

where \( V_{out}^2(f) \) is the output noise PSD. Since \( \sum g_k^2 = D/R^2 \), equation (5) further simplifies to:

\[ V_{out}^2(f) = \frac{4kT \frac{R}{D}}{1 + j\omega C \frac{R}{D}} \]

(6)

Thus, equation (6) shows that the output noise PSD of the circuit in Figure 16(b) is identical to an RC low-pass filter, with capacitance of C and resistance of R/D. The integrated noise \( \int V_{out}^2(f) df \) is equal to kT/C, which is similar to the noise of a switched-capacitor integrator. However, the noise PSD given by equation (6) is predominantly confined to frequencies below the corner frequency \( D/(2\pi RC) \). Thus, by setting the corner frequency 3-4 times lower than 1Hz, the noise contribution in the neural signal band (1Hz-5kHz) is negligible.

The duty-cycled resistor is used to realize a low unity-gain bandwidth integrator, as shown in Figure 17(a). Though the signal transfer function analysis and noise analysis were performed on the circuit shown in Figure 16(b), the results directly translate to the integrator shown in Figure 17(a). Thus, the integrator in Figure 17(a) behaves identical to an integrator with a resistor of R/D. The step response of the integrator is shown in Figure 17(b) when the duty-cycled resistor is driven with a DC signal and a clock, respectively. The slope of the step response is significantly lowered when the duty-cycled resistor is driven with a clock as compared to a DC signal, which shows the reduced unity-gain bandwidth as predicted by equation (3). The output thermal noise PSDs of low unity-gain bandwidth integrators are shown in Figure 17(c). The plot shows that an integrator
implemented with duty-cycled resistors has large noise contribution below the signal band of interest, but the in-band noise contribution is significantly lower than a conventional switched-capacitor integrator.

**Figure 17.** (a) Opamp-based low UGB integrator using the duty-cycled resistor. (b) Step response of the integrator shown in (a). (c) Typical output thermal noise PSD of low UGB integrators.
Figure 18. Electrode-referred noise PSD of the servo-loop integrator

From Figure 17(a), we see that by realizing a larger equivalent resistance $R_{eq}$, the value of $C_{int}$ can be reduced, thus reducing chip area. It can also be shown that the in-band noise contribution (when referred to the electrodes) of the DCR in the servo-loop can be reduced by realizing larger equivalent resistances $R/D$ (Figure 18). Similar arguments can also be used to show that the in-band noise of the DCR $R_B$ (shown later, in Figure 22) can be reduced by realizing larger equivalent resistances. However, the maximum resistance of the DCR is limited by the parasitic capacitance that appears in-between the passive resistor $R$ and the switch (Figure 19). This parasitic capacitance results in an equivalent switched-cap resistor $R_p$ that appears in parallel across the amplified resistance $R/D$, thus limiting the maximum equivalent resistance to $R_p$. The value of $R_p$ is given by $1/(f_1 C_p)$, where $C_p$ is the value of the parasitic capacitance and $f_1$ is the switching frequency of the DCR. As an example, for $C_p=5fF$ and $f_1=25kHz$ (both being typical values), $R_p$ is set to $8G\Omega$. To increase $R_p$, either $f_1$ or $C_p$ can be reduced. However, $C_p$ is limited by the substrate capacitance of the resistance $R$, while $f_1$ must be greater than twice the signal bandwidth to avoid aliasing. Thus it would seem that the maximum resistance is limited to $8G\Omega$. 
Figure 19. Equivalent circuit of a low-pass filter using a DCR.

Figure 20. A low-pass filter using the proposed MDCR to realize very-low corner frequencies, while overcoming the limitation due to parasitic capacitance.

We propose the Multi-rate Duty-Cycled Resistor (MDCR) to solve this problem [42]-[43]. The MDCR is shown in Figure 20. Let’s assume that we need to realize a 0.2Hz low-pass filter. Since such a low corner frequency would require an exceptionally large resistance (much larger than $R_p$ from Figure 19), we instead first realize a low-pass filter with a moderately low corner frequency of 10Hz. This low-pass filter, termed the anti-alias filter (AAF) in Figure 20, is realized by the DCR formed by $R_1$ switching at $f_1$, and the capacitor $C_1$. The AAF is followed by a second low-pass filter formed by the DCR $R_2$ switching at $f_2$, and the capacitor $C_2$. The AAF allows for a
significantly reduced switching frequency $f_2$, as the AAF reduces the bandwidth of the signal flowing into the second low-pass filter. The lower limit on the switching frequency $f_2$ is determined by the bandwidth $f_{aaf}$ of the AAF and the required attenuation of the aliased components. For this work, we chose to have $f_2/f_{aaf}$ to be greater than 64, which provides sufficient attenuation to the aliased components. Hence, in the second low-pass filter, we have circumvented the limitation of the minimum required switching frequency by using the AAF, thus increasing the maximum realizable resistance of the DCR (formed by $R_2$ switching at $f_2$) by a factor of $f_1/f_2$.

![Equivalent circuit](image1)

**Figure 21.** (a) Equivalent circuit of the low-pass filter shown in Figure 20. (b) Low-BW integrator using the proposed MDCR.

The equivalent circuit of this composite low-pass filter is shown in Figure 21(a). The ON duration of the switches $T_{ON}$ is 4.7ns, and $f_1$ was set to 25kHz. This results in a duty-cycle factor $D$ of $1/8530$ for the DCR formed by $R_1$ switching at $f_1$. $R_1$ and $R_2$ were set to 350kΩ, which leads to the equivalent resistance $R_{1,eq} = R_1/D = 3GΩ$. Thus, $R_{1,eq}$ along with $C_1 = 6pF$ leads to an anti-alias corner frequency $f_{aaf}$ of 10Hz. In the second low-pass filter, $f_2$ is set to be $f_1/32 = 781.25Hz$. 

\[
R_{eq} = 32 \cdot \frac{R_2}{D} \\
\]
This leads to the equivalent resistance \( R_{2,\text{eq}} = (R_2/D) \times 32 = 90 \Omega \). Hence, \( R_{2,\text{eq}} \) along with \( C_2 = 12 \text{pF} \) leads to the required low-pass corner frequency of 0.15Hz. Thus by using the MDCR, a 350k\( \Omega \) resistance has been amplified to 90G\( \Omega \).

Though the above example is a passive low-pass filter, the MDCR can also be used as a large resistor to realize low-bandwidth integrators, as shown in Figure 21(b). The transfer function and noise analysis of the conventional DCR have already been discussed, and the results directly translate to the MDCR. Hence, the noise contribution of the MDCR is nearly identical to the noise contributed by the equivalent amplified resistance. By using the MDCR, we have realized a much larger resistance than what was possible using the conventional DCR, leading to lower noise in the front-end. Also, the MDCR can be realized in a small chip area, and there’s no penalty on linearity unlike the pseudo-resistor.

Since the MDCR is equivalent to a cascade of two low-pass filters (Figure 21(a)), it could cause instability when used in a feedback-loop since it introduces two poles. The servo-loop unity-gain bandwidth sets the high-pass corner \( f_{\text{HP}} \) of the signal transfer function (Figure 10(a)). Let the servo-loop integrator have a unity-gain bandwidth of \( f_{\text{ugb,dsi}} \). Hence, from Figure 10(a), \( f_{\text{HP}} = f_{\text{ugb,dsi}}(C_3/C_2) \). To ensure stability, we must choose the AAF corner to be much larger than \( f_{\text{HP}} \). We return to this point in section 6.5.

Next, we consider the problem of distortion due to large common-mode interferers.
6.2 Reducing distortion due to common-mode interference

The susceptibility of conventional recording front-ends to common-mode interference is explained using a typical chopper amplifier as an example. The amplifier is implemented using capacitive feedback (Figure 22) in the “inverting” topology. Chopping is implemented using passive mixers at the input and feedback arms of the capacitive feedback network. The demodulation mixer is placed within the opamp $g_m$, usually in-between the 1$^{st}$ and 2$^{nd}$ stages of a 2-stage opamp.

![Figure 22. Response of a chopper amplifier to CM inputs.](image)

The signals appearing at the electrode inputs, as discussed before, consist of a differential signal with amplitudes <100mV, and a common-mode signal with amplitudes up to 500mV. Passive mixers allow the common-mode signal to pass unaltered. The opamp used in the chopper amplifier is usually designed to respond only to differential signals while having high common-mode rejection. This is accomplished by using a differential-pair with a high-impedance tail current source. Also, common-mode feedback (CMFB) loops are used to set the bias voltages at the outputs of $g_m$. Hence, for common-mode signals, the CMFB loops create low-impedance connections to ac-ground at the output of $g_m$. To set the common-mode DC bias at the input of the opamp, large resistors ($R_B$ in Figure 22) are used.
Figure 23. (a) Equivalent circuit of the chopper amplifier for CM signals. (b) Transfer function from \( E_{CM} \) to \( V_{in,CM} \) (refer Figure 22).

The equivalent common-mode circuit for the chopper amplifier is shown in Figure 23(a). The transfer function from the common-mode input at the electrode \( E_{CM} \) to the opamp input \( V_{in,CM} \) is found to be

\[
\frac{V_{in,CM}}{E_{CM}} = \frac{sC_{in}R_B}{1+s(C_{in}+C_f)R_B}
\]

The above transfer function is plotted in Figure 23(b). We see that \( V_{in,CM}/E_{CM} \) is a 1\(^{st}\) order high-pass filter, with the corner frequency set by the capacitance \( C_{in}+C_f \) and the resistor \( R_B \). To ensure proper functioning of the chopper amplifier, this corner frequency is usually set to \(<10\text{Hz} \) [44]. Hence, common-mode signals beyond 10Hz pass unattenuated to the input of the opamp, which could cause the differential response of a power-optimized amplifier to show significant departures from the expected response.
Consider the current-reuse differential pair as shown in Figure 24, which is the most common topology (due to its favorable power-noise trade-off) used for the 1st stage of the opamp $g_m$. To ensure sufficient headroom for the tail current sources, the gate bias $V_{\text{in,CM}}$ of the input transistors $M_{1-4}$ must be within the following range: $V_{ov6} + V_{GS3,4} < V_{\text{in,CM}} < V_{DD} - V_{ov5} - V_{GS1,2}$, where $V_{DD}$ is the supply voltage, $V_{ov5,6}$ are the overdrive voltages of the tail current sources and $V_{GS1-4}$ are the required gate-source voltages for transistors $M_{1-4}$ to carry a bias current of $I_B/2$. Assuming $V_{DD} = 1.2\,V$, $V_{ov5,6} = 0.1\,V$ and $V_{GS1-4} = 0.45\,V$ (typical values), the range for $V_{\text{in,CM}}$ is $0.55\,V < V_{\text{in,CM}} < 0.65\,V$. Hence the input common-mode range is limited to less than 100mV. This range is significantly lower than the common-mode swings (500mV) that are expected at the electrodes.

To estimate the distortion caused by common-mode artifacts, the chopper amplifier in Figure 22 was simulated with a differential input of $80\,mV_{pp}$ at 1kHz, along with a common-mode interferer of $500\,mV_{pp}$ amplitude at 900Hz. The total harmonic distortion (THD) degraded from $-74\,dB$ to $-43\,dB$ when the common-mode interferer was enabled, thus exposing the severity of the problem.
A simple solution to the CM-interferer problem would be to use an opamp with a large input common-mode range (ICMR), like a folded-cascode topology. Although the folded-cascode would consume more than twice the power as compared to the current-reuse opamp (for the same noise), immunity to CM interference could be worth the power penalty. However, it must be noted that these CM interferers are not “slow” signals. Since the CM interferers have the same BW as the differential signals of interest, large CM swings at the input of opamps could lead to distortion. This is particularly significant when the opamp is designed for low-noise and low-power operation, i.e. the input devices (and possibly others) are biased in weak inversion, where they are most nonlinear. To verify this, we simulated a folded-cascode opamp (similar to [11]) with an n-MOS input diff-pair, from a 1.2V supply with an ICMR of 0.7V. We set up a similar scenario as before-differential input of 40mV\(_{pp}\) at 1kHz, along with a common-mode interferer of 500mV\(_{pp}\) amplitude at 900Hz. Since the CM interferer (0.5V) is smaller than the ICMR (0.7V), the linearity of the front-end could be preserved in the presence of the CM interferer. However, the total harmonic distortion (THD) degraded from −78dB to −62dB when the CM interferer was enabled. Thus we see that a simple folded-cascode with its large ICMR is insufficient.
From the previous discussion, we see that the presence of large common-mode swings at the opamp input $V_{in,CM}$ leads to distorted outputs. We propose a feed-forward common-mode cancellation (CMC) path to attenuate the common-mode swings at $V_{in,CM}$, which would restore the linear operation of the front-end for differential signals [42]-[43]. The concept of the CMC path is shown in Figure 25. The common-mode signal at the electrodes is sensed and amplified by the opamp $g_{ma}$ and capacitors $C_a$ and $C_b$. This amplified common-mode signal is then subtracted from $V_{in,CM}$ through capacitors $C_{cm}$. The gain in the CMC path is set by the capacitor ratio $A_{cm} = 2C_a/C_b$. If $C_{cm}$ is sized to be $C_{in}/A_{cm}$, then the common-mode signals at the input of the opamp $V_{in,CM}$ are ideally cancelled to zero. Any mismatches in the ratio of $C_{in}/C_{cm}$ would lead to residual common-mode swings at $V_{in,CM}$. However, since $g_m$ is immune to small common-mode swings (<20mV), a cancellation accuracy of 2% is sufficient. This can be easily achieved by matching the capacitors.
C<sub>in</sub> and C<sub>cm</sub>. However, the presence of the capacitors C<sub>cm</sub> leads to an increase in the input-referred noise of the front-end, as shown by the following equation:

\[
\nu_{n,in} = \nu_n \left[ \frac{C_{in} + C_f + C_{cm}}{C_{in}} \right]
\]  

(8)

Here, \( \nu_n \) is the input-referred noise of the opamp \( g_{ma} \). To minimize the increase in the input-referred noise, \( C_{cm} \) should be sized smaller than \( C_{in} \). This requirement leads to a larger gain \( A_{cm} \) in the CMC path. However, increasing \( A_{cm} \) results in larger signal swings at the output of \( g_{ma} \), which will cause saturation due to limited headroom at the output of \( g_{ma} \). This will prevent the CMC path from cancelling the common-mode swings at \( V_{in,CM} \). To increase the headroom at the output of \( g_{ma} \), we integrate a 50%-efficient charge-pump on-chip [45]-[46] to generate a local 1.8V supply for \( g_{ma} \) from the available 1.2V supply. Thus, with the CMC gain \( A_{cm}=2 \), common-mode signals as large as 650mV<sub>pp</sub> can be easily cancelled at \( V_{in,CM} \), while the noise contribution of \( g_m \) is kept low. To ensure accurate cancellation, the bandwidth of the CMC path must be well beyond the expected bandwidth of the common-mode artifacts. Since we expect common-mode artifacts in the entire neural signal band up to 5kHz, the CMC-path bandwidth is set to 30kHz. This sets the requirement of \( g_{ma} \) as follows:

\[
g_{ma} \left( \frac{C_b}{C_b + 2C_a} \right) \frac{1}{2\pi(C_b + 2C_{cm})} > 30kHz
\]  

(9)

Hence, for \( C_a=C_b=1pF \) and \( C_{cm}=0.5pF \), \( g_{ma} \) should be larger than 1.13µA/V. The schematic of the opamp used to realize \( g_{ma} \) is shown in Figure 26. A current of 120nA was sufficient to achieve the required \( g_{ma} \), which is a small fraction of the overall power budget. Hence a relatively low
efficiency (50%) charge-pump design was chosen for simplicity and reducing design time, since the power overhead is negligible.

**Figure 26.** Schematic of the opamp $g_{ma}$ used in the CMC path (refer Figure 25).

Although the CMC path attenuates common-mode swings at $V_{in,cm}$, mismatches in $C_{cm}$ could degrade CMRR. However, since $C_{cm}$ is large (0.5pF), good matching (<0.1%) between $C_{cm}$ can be achieved by using common-centroid layout techniques. Any residual mismatches in $C_{cm}$ would indeed convert a common-mode signal at the electrode into a differential signal flowing out of the CMC path. However, note that there is no chopping at the output of the CMC path. Hence, the CM-to-DM signal at the CMC output remains at baseband, as compared to the up-modulated differential signal of the electrode. Thus, the CM-to-DM component remains separate (in frequency) from the desired differential signal, which ensures negligible impact to CMRR.

Next, we consider the problem of reduced input-impedance in chopper amplifiers.
6.3 Boosting the input impedance of chopper amplifiers

The input branch of the chopper amplifier is redrawn in Figure 27(a). For a DC input $V_{in}$, the current supplied by the input voltage source is shown in Figure 27(b). The charge supplied in one period of the chopping clock $f_{clk}$ is $Q = 2C_{in}V_{in}$. Hence, the DC input impedance is given by $Z_0 = 1/(2C_{in}f_{clk})$. For $C_{in}$ of 1pF, and a chopping clock frequency $f_{clk}$ of 25kHz, the DC input impedance $Z_0$ is 20MΩ.

$$Q = C_{in}V_{in}$$

Figure 27. (a) Input branch of the chopper amplifier. (b) Waveform of the current $I_{in}$ provided by a DC input $V_{in}$ in (a).

Figure 27(b) shows that the input voltage source $V_{in}$ provides charge in a narrow region of time, labeled as $\Delta t$. If an alternate reservoir of charge could be used to supply charge to the input capacitors $C_{in}$ for the duration $\Delta t$, then the DC current provided by $V_{in}$ is reduced to zero, boosting the DC input impedance to infinity. This concept [47]-[48] is realized as a circuit in Figure 28(a), [39], [41], with the control waveforms shown in Figure 28(b).
Figure 28. (a) Auxiliary path precharge technique to boost the input impedance of a chopper amplifier. (b) Control signal waveforms for the auxiliary path technique.
At the beginning of every chopping phase, denoted as the pre-charge phase $\varphi_{1,2}$, the input capacitors are pre-charged to the input voltage $V_{\text{in}}$ through buffers in an auxiliary path. At the end of the pre-charge phase, the input capacitors are reconnected back to the input port. Since the capacitors $C_{\text{in}}$ have been charged to $V_{\text{in}}$, there is no charge flow when the capacitors are reconnected to the input port. Thus, the DC current provided by $V_{\text{in}}$ is reduced to zero, boosting the DC input impedance to infinity. However, due to finite gain and finite bandwidth of the auxiliary buffer, a non-zero error is made during the pre-charge phase. If the auxiliary buffer bandwidth is $\tau^{-1}$ rad/sec, and the pre-charge duration is $T_1$ sec, then the error made in the pre-charge phase $\Delta V$ is given by

$$
\Delta V \approx 2V_{\text{in,DC}} \cdot \left[ \alpha + \exp \left( - \frac{T_1}{\tau} \right) \right] 
$$

(10)

where $\alpha$ is the gain error of the auxiliary path buffer. Hence at the end of the pre-charge phase, due to the error $\Delta V$, the input $V_{\text{in}}$ has to provide some residual charge required by $C_{\text{in}}$. The input impedance is now given by

$$
Z_{\text{in,DC}} = \frac{1}{2C_{\text{in}}f_{\text{clk}}} \left( \frac{1}{\alpha + \exp \left( - \frac{T_1}{\tau} \right)} \right) = Z_o \cdot \frac{\exp \left( \frac{T_1}{\tau} \right)}{1 + \alpha \exp \left( \frac{T_1}{\tau} \right)}
$$

(11)

As an example, assuming that $T_1$ is large enough for 1% settling, and if the DC gain of the opamp used in the auxiliary buffer is 30dB (both being reasonable assumptions), then from equation (11), the DC input impedance is boosted by a factor of 25. Thus, the DC input impedance of 20M$\Omega$ can be boosted to 500M$\Omega$ by employing the auxiliary path.
The power consumption of the auxiliary buffers (Figure 28(a)) and the pre-charge time $T_1$ can be determined as follows. Let the auxiliary path duty-cycle factor $T_1/(0.5T_{clk})$ be denoted by $d_{aux}$. Also, let the bandwidth of the auxiliary buffers allow for $k$ time constants of settling in the pre-charge phase. Thus, the bandwidth of the auxiliary buffers $\tau^{-1}$ is given by $k/T_1$. Let $I_{aux}$ be the current consumed by each buffer during the pre-charge phase. To reduce power consumption, the auxiliary buffer bias currents are disabled in-between pre-charge phases. Assuming that the input devices of the auxiliary buffers are biased in weak inversion, i.e. $g_{m,aux}/I_{aux} \approx 25$, then the total DC current consumed by both auxiliary buffers is given by

$$I_{aux,DC} = \frac{8kC_{in}}{25T_{clk}} \quad (12)$$

For $C_{in}=1\text{pF}$, $f_{clk}=25\text{kHz}$ and $6\tau$ settling, equation (12) gives $I_{aux,DC} = 48\text{nA}$, which is negligible.

![Figure 29. Input-referred noise contribution of the auxiliary-path buffers.](image)

The noise contribution of the auxiliary buffers is determined as follows. The noise PSD of the auxiliary buffers in the pre-charge phase is denoted by $v_{n,aux}^2 = \sqrt{2} \cdot v_{n,buf}^2$, as shown in Figure 29. Since the auxiliary buffer noise is duty-cycled when referred to the input as shown in Figure 29, the contribution to the input-referred noise PSD is given by $v_{in,aux}^2 = d_{aux} \left( v_{n,aux}^2 \right)$. By ensuring that
\( v_{in,aux}^2 \) is 10 times lower than the noise PSD of the 1\textsuperscript{st} opamp stage \( g_{m1} \), the auxiliary path noise contribution can be made negligible. This leads to the following duty-cycle requirement:

\[
d^2 \approx \frac{kC_m}{(25T_{clk})(5I_B)}
\]  \( (13) \)

where \( I_B \) is the bias current of \( g_{m1} \). Equation (13) assumes that the input devices of \( g_{m1} \) were biased in weak inversion, which is required for a power-optimized design. From equation (13), for \( I_B=1\mu A \), \( d_{aux} = 1/28 \). For ease of digital implementation, \( d_{aux} \) is set to 1/16. Hence, the auxiliary path consumes very low power as compared to the 1\textsuperscript{st} stage of the chopper opamp, while its noise contribution is also kept small. However, from Figure 29, \( v_{in,aux}^2 \) has power at multiples of 2\( f_{clk} \), leading to output ripples at 2\( f_{clk} \). These ripples are expected to be small due to the limited bandwidth of the front-end.

The auxiliary-path impedance-boosting technique has two critical advantages over the positive feedback loop employed in [28]. As discussed in chapter 4, the positive-feedback loop is rendered inoperative at DC if a servo loop is used. This is because the positive-feedback loop is driven by the output \( V_{out} \), and the servo loop attenuates the DC signal at \( V_{out} \). In contrast, the auxiliary path is driven by the voltage appearing at the input \( V_{in} \). Hence the auxiliary-path technique can be employed simultaneously with a DC servo loop, which is necessary in a practical neural recording front-end. Another key advantage of the auxiliary-path technique is its insensitivity to parasitic capacitance. The positive-feedback technique is very sensitive to parasitic capacitance appearing at the bottom plate of \( C_{in} \), as discussed in [28]. When the auxiliary-path technique is used, any parasitic capacitance appearing at the bottom-plate of \( C_{in} \) reduces the bandwidth of the auxiliary path buffer, which increases the error \( \Delta V \) (equation (10)) due to insufficient settling time in the
pre-charge phase. For a typical bottom-plate capacitance of $C_{in}/5$, increasing the bandwidth of the auxiliary path buffer by 20% compensates for the bottom-plate capacitance. Since the power consumed by the auxiliary buffers is very low compared to $g_{m1}$, increasing the bandwidth of the buffers by 20% results in negligible additional power consumption. Hence this technique can be made insensitive to parasitic capacitance.

In the above analysis of the auxiliary path, the electrode impedance has been assumed to be zero. However, as discussed in section 2.3, the electrode impedance consists of a parallel RC circuit. Due to the non-zero electrode impedance, a positive feedback loop forms around the auxiliary path (not to be confused with the positive feedback loop discussed in [28]). It can be shown that this positive feedback will cause the DC offset and flicker noise of the auxiliary-path buffers to be amplified and appear at the electrodes [43]. Thus, the amplified offset could cause saturation, and the amplified flicker noise will degrade the performance of the front-end since it adds directly at the input of the front-end.

**Figure 30.** Half-circuit of the auxiliary path to analyze positive feedback.

The positive feedback in the auxiliary path is analyzed below. The differential half-circuit of the auxiliary path along with the input arm of the chopper amplifier is shown in Figure 30. The offset and flicker noise of the buffer is modeled as a voltage source $V_{off}$, while the electrode
impedance is modeled by the impedance $R_{el}||C_{el}$. For simplicity, we assume $R_{el}$ is infinite. In the pre-charge phase, the buffer charges the capacitor $C_{in}$ to $V_{el} + V_{off}$. At the end of the pre-charge phase, $C_{in}$ is re-connected back to $V_{el}$, and the electrode voltage is given by

$$V_{el}(n+1) = V_{el}(n) + \left( \frac{C_{in}}{C_{in} + C_{el}} \right) \cdot V_{off}(n)$$  (14)

From the above equation, we see that the transfer function from $V_{off}$ to $V_{el}$ is identical to that of an ideal first-order integrator. Hence for a non-zero DC value of $V_{off}$, $V_{el}$ will go to infinity.

To get a more accurate description of the positive feedback, the effect of a finite $R_{el}$ is considered next. From Figure 30, the capacitance $C_1$ is periodically switched between the buffer output and the electrode. Hence, this switching capacitance forms an equivalent resistance (Figure 31(a)) with a value of $R_a = T_c/(2C_{in})$, where $T_c$ is the chopping period. Thus the buffer output $V_a = V_{el} + V_{off}$, and $V_{el} = V_a \cdot Z_{el}/(Z_{el} + R_a)$. Using these 2 equations, the transfer function $V_{el}/V_{off}$ is determined to be

$$\frac{V_{el}(s)}{V_{off}} = \frac{2R_{el}C_{in}}{T_c(1 + sR_{el}C_{el})}$$  (15)

The above transfer function is shown in Figure 31(b). The DC gain is given by $2R_{el}C_{in}/T_c$. Assuming $R_{el}=200\text{M}\Omega$, $C_{in}=1\text{pF}$, $C_{el}=1\text{nF}$ and $T_c=40\mu\text{s}$ (all typical values), the DC gain from $V_{off}$ to $V_{el}$ is 10. Hence, a 5mV auxiliary-buffer offset is amplified to a 50mV DC voltage by the positive feedback in the auxiliary path, and this voltage appears at the electrodes. Also, from the transfer function in Figure 31(b), we see that low-frequency components of $V_{off}$, for example the flicker noise of the auxiliary-buffers, will also be amplified and appear at the electrodes, thus degrading the low-frequency noise performance of the front-end.
Figure 31. (a) Equivalent circuit of the auxiliary-path half circuit in Figure 30. (b) Transfer function from $V_{off}$ to $V_{el}$ due to positive feedback, leading to amplified buffer offset and flicker noise appearing at $V_{el}$.

A solution to this problem can be determined by taking a closer look at the transfer function in Figure 31(b). The unity-gain bandwidth (UGB) of this transfer function is given by $\alpha f_c/\pi$, where $\alpha$ is the ratio given by $C_{in}/C_{el}$. For the above-chosen typical values of $C_{in}$ and $C_{el}$, the UGB of $V_{el}/V_{off}$ is approximately given by $f_c/3000$. Thus, if $V_{off}$ can be up-modulated to a frequency that is much larger than $f_c/3000$, then $V_{off}$ will appear as tiny ripples at the electrode instead of a large DC
voltage. This is realized by introducing passive mixers $M_{1,2}$ in the auxiliary path (Figure 32) [42]-[43].

![Figure 32. Proposed auxiliary-path chopping using mixers $M_{1,2}$ to mitigate the effect of positive feedback.](image)

The frequency of the ripple at the electrodes will be equal to the clock frequency $f_{aux}$ used in the mixers $M_{1,2}$. To ensure that these ripples remain outside the frequency band of interest, $f_{aux}$ should be larger than 5kHz. The amplitude of the ripples can be determined to be

$$V_{ripple} \approx V_{off} \left( \frac{4}{\pi^2} \right) \frac{C_f}{f_{aux}}$$  \hspace{1cm} (16)

Although introducing mixers $M_{1,2}$ can mitigate the amplification of $V_{off}$, it will reduce the input impedance of the front-end. This is because the gate capacitance of the auxiliary-path buffers along with the mixer $M_1$ will appear as a switched-cap resistance $Z_{in,aux}$ at the input of the front-end. Hence the input impedance of the front-end is now given by $Z_{in,boost} \parallel Z_{in,aux}$, where $Z_{in,boost}$ is the boosted input impedance achieved by the auxiliary path (Figure 32). To achieve the required 1GΩ
DC input impedance, $Z_{\text{in,aux}}$ must be significantly larger than $1\,\Omega$. $Z_{\text{in,aux}}$ is given by $1/(2C_{\text{auxbuf}} f_{\text{aux}})$, where $C_{\text{auxbuf}}$ is the gate capacitance of each auxiliary-path buffer. Since $f_{\text{aux}}$ has a minimum value of 5kHz, $C_{\text{auxbuf}}$ must be reduced to achieve the required value of $Z_{\text{in,aux}}$. However, reducing $C_{\text{auxbuf}}$ is achieved by reducing the area of the input transistors of the auxiliary buffers, which will lead to a larger value of $V_{\text{off}}$ due to increased mismatch. This will cause larger ripples at the electrode (from equation 16) which is undesirable. Hence while sizing the input transistors of the auxiliary-buffers, the trade-offs for the input impedance and the ripple amplitudes at the electrode must be considered together. $V_{\text{off}}$ is proportional to $1/\sqrt{C_{\text{auxbuf}}}$ and the ripple amplitude is proportional to $V_{\text{off}}/f_{\text{aux}}$. Thus, accounting for all trade-offs, the ripple amplitude $V_{\text{ripple}}$ is proportional to $Z_{\text{in,aux}} \sqrt{C_{\text{auxbuf}}}$. Hence for a given $Z_{\text{in,aux}}$, $C_{\text{auxbuf}}$ must be minimized to reduce ripple amplitudes at the electrodes. This corresponds to using minimum-sized devices for the input transistors of the auxiliary-buffers. $C_{\text{auxbuf}}$ will ultimately be limited by routing capacitance. Hence a practical solution would be to reduce the gate capacitance of the input devices of the auxiliary buffers to match the routing capacitance between the gate and the mixer $M_1$. The mixers $M_{1,2}$ are driven with a clock frequency of $f_c/4$, where $f_c=25\,\text{kHz}$ is the chopping frequency of the chopper amplifier. The input transistors of the auxiliary buffers are sized such that $C_{\text{auxbuf}}$ (including routing capacitance) is about $15\,\text{fF}$, which sets $Z_{\text{in,aux}}$ to be about $6\,\Omega$. Hence $Z_{\text{in,aux}}$ is sufficiently large to achieve the required input impedance of the front-end.

The auxiliary path, as shown in Figure 28, was implemented in the first prototype of the chopper amplifier (Chip-1 in Figure 15). From measurements \cite{41}, we found that $Z_{\text{in}}$ was indeed boosted, however the increase in $Z_{\text{in}}$ was not sufficient to meet our requirement of $Z_{\text{in}}>1\,\Omega$ (measured $Z_{\text{in}} = 300\,\text{M}\,\Omega$). This insufficient boost to $Z_{\text{in}}$ was due to the limited bandwidth of the auxiliary-buffers, which caused a non-zero settling error in the pre-charge phase. The finite gain
of the opamp used in the auxiliary-buffers also leads to a non-zero settling error in the pre-charge phase [41]. This is illustrated in Figure 33 (with reference to Figure 28).

**Figure 33.** Settling errors in the precharge phase (referring to Figure 28) leading to limited $Z_{\text{in}}$-boost using the auxiliary path.

The input-impedance at DC was derived earlier (equation 11). In equation 11, $\alpha = 1/A_{\text{DC}}$, where $A_{\text{DC}}$ is the open-loop DC gain of the buffer, which is usually around 40dB. This implies that the maximum achievable boost to $Z_{\text{in}}$ is limited to a factor of 100. To ensure we get most of this impedance boost, the settling error due to the finite bandwidth of the auxiliary-buffer must be minimized. This can be done by increasing the transconductance of the auxiliary-buffers, which would increase power consumption. A simple alternative is to use storage capacitors $C_{\text{aux}}$ (Figure 34) to assist the auxiliary-buffers [43].
Figure 34. Implementation of auxiliary-buffer assistance using storage caps $C_{aux}$ to achieve additional $Z_{in}$-boost.

At the beginning of the pre-charge phase (as shown in the timing diagram in Figure 34), $C_{aux}$ is allowed to charge-share with $C_{in}$. If $C_{aux}$ is sized to be significantly larger than $C_{in}$, then most of the pre-charging of $C_{in}$ (labeled as $\Delta V_{assist}$ in Figure 33) is complete in this charge-sharing phase. Hence the auxiliary-buffers now only need to complete the remainder of the pre-charging of $C_{in}$. This reduces the settling error in the pre-charge phase, leading to a larger $Z_{in}$ without increasing power consumption. $C_{aux}$ was set to 8-$C_{in}$, and the DC current in the auxiliary-buffers was 150nA. This was sufficient to provide an impedance boost by 2.5x, as we shall see in section 6.6. From Figure 34, when $\phi_{1,2} = 0$, the auxiliary-buffer bias currents are reduced to 25nA to save power while ensuring that $C_{aux}$ tracks $V_{el}$ till the next pre-charge phase.

In the next section, we consider the problem of chopper ripples.
6.4 Ripple rejection in chopper amplifiers

The up-modulated DC offset and flicker noise of the 1st opamp stage $g_{m1}$ can appear as large ripples at the amplifier output (Figure 35). These ripples can significantly reduce the available linear swing at the output, as discussed in [28] and [44], thus reducing the dynamic range of the front-end.

![Figure 35](image)

Figure 35. A simplified block-diagram of a 2-stage chopper amplifier, along with frequency components at various nodes.

By placing a DC-blocking impedance after $g_{m1}$, as shown in Figure 36, the chopper ripples at the output $V_{out}$ can be attenuated without additional power consumption. A DC-feedback loop is necessary to establish a stable input bias voltage for the first opamp stage. This ripple-rejection technique is discussed in [44]. Referring to Fig. 2 in [44], the ripple attenuation is given by $g_{m1}R$. However, in this work, there is no path for DC current to flow from $g_{m1}$ to $g_{m2}$ (Figure 36), or referring to Fig. 3 in [44], the resistance $R$ is infinite. Thus, the expected attenuation of ripples caused by the DC offset of $g_{m1}$ is infinite. To attenuate ripples caused by the flicker noise of $g_{m1}$, the unity-gain frequency (referring to Fig. 3 of [44]) of the transfer function $\left[ \frac{V_{out}(f_{clk} + f)}{V_{in}(f)} \right]/A_0$, where $A_0$ is the gain of the opamp, can be used.
which is given by $\omega_{ugbf} = \left[ A_o \omega_{ch} C_C \left( \frac{1}{R_f (C_{in} + C_f + C_{dil})} \right) \right]^{1/2}$, should ideally be larger than the flicker-noise corner frequency of $g_{m1}$. Here, $A_o = C_{in}/C_f$ is the closed-loop gain. For $C_C = 2\text{pF}$, $R_f = 20\text{G}\Omega$ and $C = 10\text{pF}$, $f_{ugbf}$ is 830Hz, while the simulated flicker-noise corner of $g_{m1}$ was 3.4kHz. Either $R_f$ or $C$ can be reduced to increase $f_{ugbf}$, but reducing $R_f$ would increase its in-band noise contribution, while reducing $C$ would increase signal swings at the output of $g_{m1}$. Due to these considerations, $f_{ugbf}$ was kept at 830Hz, since this is sufficient to attenuate the majority of the flicker-noise of $g_{m1}$.

![Diagram](image)

**Figure 36.** Ripple-rejection implementation without using additional active elements [44].
6.5 Experimental results from a fabricated prototype of the chopper amplifier

The proposed chopper amplifier is shown in Figure 37, and the schematics for \( g_{m1} \) and \( g_{m2} \) are shown in Figure 38. The amplifier was implemented in a 40-nm CMOS technology. Figure 39 shows the chip micrograph, and Figure 40 shows the measurement setup with provisions to emulate the electrode impedance. The amplifier occupies an area of 0.06mm\(^2\)/ch and the total power consumed from a 1.2V supply is 2.8\( \mu \)W. The trans-conductances \( g_{m1} \) and \( g_{m2} \) consume 1.2 and 0.25 \( \mu \)W respectively. The servo-loop, aux-path buffers and the CMC path consume 0.36, 0.2 and 0.3 \( \mu \)W respectively. Biasing and control-signal generation consumes 0.45\( \mu \)W.

**Figure 37.** Complete implementation of the proposed chopper amplifier.
Figure 38. Schematics of opamps used in the chopper amplifier.

Figure 39. Micrograph of the fabricated prototype showing eight chopper amplifiers, implemented in 40-nm CMOS.
Figure 40. Bench-top test setup for characterizing the fabricated chopper amplifier.

The measured signal transfer function is shown in Figure 41. The mid-band gain was 17.9dB and the low-pass corner was 5kHz. The servo-loop unity-gain bandwidth sets the high-pass corner of the signal transfer function. From Figure 37, we see that $f_{HP} = 2f_{ugb,dsl}$. The AAF corner frequency in the MDCR was chosen to be 10Hz (section 6.1). Hence, the pole associated with the AAF will be a non-dominant pole since it is far away from the unity-gain frequency $f_{HP}$ of the servo-loop, and the phase margin of the servo-loop will be close to 90° ensuring stability.
The input-referred noise was measured to be $1.8\mu V_{\text{rms}}$ in the LFP band (1Hz – 200Hz), and $5.3\mu V_{\text{rms}}$ in the AP band (200Hz – 5kHz), as shown in Figure 42.

The measured input impedance of the front-end is shown in Figure 43. When the auxiliary path was disabled, $Z_{\text{in}}$ was 20MΩ. When the auxiliary path was enabled, $Z_{\text{in}}$ was boosted to 570Ω,
which further increased to $1.52 \text{G} \Omega$ when the auxiliary-buffer assistance was enabled. Hence $Z_{\text{in}}$ has been boosted by a factor of 76, with the storage capacitors $C_{\text{aux}}$ providing a $2.67 \times$ boost.

![Input Impedance Graph](image)

**Figure 43.** Measured input-impedance of the chopper amplifier using different impedance boost techniques.

![Input Impedance Graph](image)

**Figure 44.** Measured input-impedance of the chopper amplifier using the positive-feedback technique (Chip-1).
As discussed in section 6.3, a significant advantage of the auxiliary path technique over the positive feedback technique ([28]) is that the auxiliary path can be used simultaneously with the DC-Servo loop. To verify this claim, the positive feedback technique to boost the input impedance was implemented on the first prototype of the chopper amplifier (Chip-1). The measured $Z_{in}$ is shown in Figure 44, and we see that the positive feedback path has been rendered ineffective at DC.

To show the benefits of chopping in the auxiliary path, the offset appearing at the electrode was measured. When chopping in the auxiliary path (mixers M1,2 in Figure 34) was disabled, large offsets were observed at the electrode (Figure 45(a)), and the worst-case offset was 45mV. When the auxiliary-path chopping was enabled, the 45mV offset reduced to zero and a 5.4$\mu$V ripple was observed at $f_c/4$ (Figure 45(b)). This is expected from the discussions in section 6.3.

<table>
<thead>
<tr>
<th>Channel #</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured electrode offset (mV)</td>
<td>7.5</td>
<td>9.1</td>
<td>36</td>
<td><strong>45</strong></td>
<td>6.1</td>
<td>7.6</td>
<td>5.7</td>
<td>21.4</td>
<td>2.8</td>
<td>12.6</td>
<td>3.6</td>
<td>18</td>
</tr>
</tbody>
</table>

(a)

(b)

45mV DC offset up-modulated to 5.4$\mu$V ripple at $f_c/4 = 5.86kHz$

Residual DC offset ≈ 0
Figure 45. Benefits of auxiliary-path chopping. (a) Large offsets observed at the electrode when aux-path chopping is disabled. (b) Measured electrode input when aux-path chopping was enabled. (c) Measured input-referred noise showing reduced aux-buffer flicker noise when auxiliary-chopping is enabled.

The input-referred noise in the 1Hz – 200Hz band also reduced from $4.5\mu V_{\text{rms}}$ to $1.8\mu V_{\text{rms}}$ when the auxiliary-path chopping was enabled (Figure 45(c)), since the flicker noise of the auxiliary buffers have been removed.

The linearity measurements of the chopper amplifier are shown in Figure 46. For a differential input sinusoid of $100mV_p$ (or $200mV_{pp}$) at 1kHz with no common-mode interferer, the measured THD was $-85$ dB. The THD was also measured for varying frequencies (Figure 47).
Figure 46. Measured total harmonic distortion of the chopper amplifier for a 200mV\textsubscript{pp} input at 1kHz.

HD\textsubscript{3} = −86.5dB  
THD = −85dB

Figure 47. Measured THD vs frequency of the CCIA, for an input tone of 200mV\textsubscript{pp}.

To measure the front-end performance in the presence of common-mode interference, we performed two-tone tests. Realistic stimulation artifacts have significant power at multiple harmonics of the stimulation frequency due to their pulse-like nature [31]. Hence, immunity to common-mode interference must be measured for frequencies up to several harmonics of the
stimulation frequency. Stimulation is usually performed at frequencies below 150Hz. Hence, we measure performance with CM interference up to 900Hz. The two-tone test is conducted as follows. The differential input to the front-end consists of the sum of a 100mV$_p$ sinusoid at 900Hz and a 2mV$_p$ sinusoid at 1kHz. A common-mode interferer of 650mV$_{pp}$ is also applied at 900Hz. The 900Hz tones represent the stimulation artifacts, while the 1kHz tone represents the neural signal of interest.

The two-tone test is conducted as follows. The differential input to the front-end consists of the sum of a 100mV$_p$ sinusoid at 900Hz and a 2mV$_p$ sinusoid at 1kHz. A common-mode interferer of 650mV$_{pp}$ is also applied at 900Hz. The 900Hz tones represent the stimulation artifacts, while the 1kHz tone represents the neural signal of interest.

Figure 48. Response of the front-end to two-tone tests with a large CM interferer, showing the severity of distortion (without CMC), and the efficacy of the CMC path in reducing distortion.

Figure 48 shows the measured results of the two-tone tests. When the CMC path was disabled, we see significant distortion components at the output. We define the Signal-to-Interferer ratio (SIR) as the power of the desired signal (in this case, at 1kHz) divided by the power of the harmonics created by distortion. The SIR was only 6.6dB when the CMC path was disabled.
However, when the CMC path was enabled, there is significant suppression of the distortion components and the SIR improves to 42.8dB. We also measure SIR for varying amplitudes of common-mode interference, and the results are shown in Figure 49. When the CMC path is disabled, the SIR degrades rapidly as the CM interferer amplitude is increased. However, when the CMC path is enabled, the SIR remains large, and degrades by only 6dB for a CM interferer amplitude of 700mV_{pp}. Hence, if a 1-bit degradation in the SIR is acceptable, then the proposed chopper amplifier can tolerate CM interference as large as 700mV_{pp}.

![Graph showing SIR vs CM Interferer Amplitude](image)

**Figure 49.** Performance of the CMC path for varying amplitudes of CM interference.

These measurements show the efficacy of the CMC path in maintaining linearity in the presence of large CM interferers. The CMRR and PSRR were also measured, and the results are shown in Figure 50. The CMRR and PSRR are better than −78dB and −76dB respectively in the signal band (1Hz – 5kHz).
The various contributors to the total power consumption of the chopper amplifier (2.8µW) are shown in Figure 51. The proposed techniques consume about 31% of the total power.

<table>
<thead>
<tr>
<th>Block</th>
<th>Power (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-stage opamp</td>
<td>1.45</td>
</tr>
<tr>
<td>Servo-loop</td>
<td>0.36</td>
</tr>
<tr>
<td>Aux-path</td>
<td>0.2</td>
</tr>
<tr>
<td>CMC + Charge-Pump</td>
<td>0.3</td>
</tr>
<tr>
<td>Bias + Control</td>
<td>0.45</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>2.8</strong></td>
</tr>
</tbody>
</table>

**Figure 50.** Measured CMRR and PSRR of the chopper amplifier.

**Figure 51.** Contributions to the total power consumption of the chopper amplifier.
6.6 In-vitro measurements using a fabricated prototype of the chopper amplifier

In-vitro measurements were performed using the prototype of the chopper amplifier to record signals from electrodes dipped in phosphate-buffered saline (PBS). Figure 52 shows the measurement setup.

![In-vitro measurement setup diagram](image)

**Figure 52.** In-vitro measurement setup.

A pair of electrodes (Stim₁ and Stim₂) was used to deliver stimulation into the PBS solution, while another pair of electrodes (V_{in,p} and V_{in,n}) were used as sensing electrodes connected to our front-end. A separate electrode was used to inject neural signals into the PBS solution. Figure 53 shows the measured output of the CCIA when pre-recorded human neural signals were injected while stimulation was disabled.

To assess the magnitude of differential and common-mode artifacts due to stimulation, stimulation waveforms (Figure 54) were injected into the PBS solution without neural signals, and the measured waveforms are shown in Figure 55.
Figure 53. In-vitro measurements using pre-recorded human neural recordings (no stimulation).

Figure 54. Stimulation waveforms used for in-vitro measurements.

The common-mode artifact at the recording site is $342\text{mV}_{pp}$ (Figure 55(a)), while the differential artifact is $8.6\text{mV}_{pp}$ (Figure 55(b)). The measured output of the CCIA matches the differential artifact at the recording site as expected (Figure 55(c)).
Figure 55. Measured waveforms when differential stimulation is enabled without injecting pre-recorded neural signals. (a) Waveforms at recording sites. (b) Differential signal at recording site. (c) Measured output using CCIA (gain normalized to unity).
Next, a 25Hz sinusoid (representing a neural signal) was injected into the PBS solution along with the stimulation waveforms. The measured output of the CCIA, after LP filtering up to 50Hz, shows a 25Hz signal (Figure 56).

![Graph showing measured output of CCIA](image)

**Figure 56.** Measured output (LP filtered up to 50Hz) of CCIA during stimulation. A 25Hz sinusoid was injected to represent a neural signal.

The injected sinusoid frequency was changed to 1kHz, and the corresponding measurements, after HP filtering from 800Hz, are shown in Figure 57. The differential signal at the recording site (Figure 57(a)) matches the output of the CCIA (Figure 57(b)). Since the stimulation waveform has power at the harmonics of 110Hz, the HP-filtered outputs show residual stimulation artifacts.
Figure 57. Measured waveforms (HP filtered from 800Hz) during stimulation. (a) Recording site. (b) CCIA output; A 1kHz sinusoid was injected to represent a neural signal.

Finally, the injected sinusoid is replaced with a pre-recorded human neural signal, and stimulation remains enabled. The measured waveforms (LP filtered up to 50Hz) are shown in Figure 58. The differential signal at the recording site (Figure 58(a)) matches the CCIA output (Figure 58(b)). These measurements show that the proposed CCIA is capable of recording neural signals in the presence of stimulation artifacts.
Figure 58. Measured waveforms (LP filtered up to 50Hz) during stimulation. (a) Recording site. (b) CCIA output; Pre-recorded human neural recordings were injected to emulate a neural signal.
6.7 Comparison of proposed neural recording CCIA with state-of-the-art neural amplifiers

Table 3 compares this work with the current state-of-the-art. Our work improves $Z_{in}$ by 54x for chopped front-ends, the maximum resistance of DCRs by 32x, the linear-input range by 20x, the dynamic range by 23-38dB, and introduces tolerance to 700mV$_{pp}$ common-mode interferers. These improvements are achieved while maintaining comparable power, noise, signal BW and chip area. Also, since the chopper amplifier meets the DC $Z_{in}$ requirement of 1GΩ, we do not need off-chip coupling capacitors, ensuring that this front-end is implantable.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power/Ch</td>
<td>2 µW</td>
<td>1.8 µW</td>
<td>4.8 µW</td>
<td>2.3 µW</td>
<td>3.28 µW</td>
<td>2.8 µW</td>
</tr>
<tr>
<td>Supply</td>
<td>1.8 V</td>
<td>1 V</td>
<td>0.5 V</td>
<td>0.5 V</td>
<td>1 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Signal BW</td>
<td>0.05Hz – 120Hz</td>
<td>0.5Hz – 700Hz</td>
<td>10kHz</td>
<td>1Hz – 400Hz</td>
<td>1Hz – 8.2kHz</td>
<td>1Hz – 5kHz</td>
</tr>
<tr>
<td>Peak Input</td>
<td>5 mV$_p$</td>
<td>N/A</td>
<td>N/A</td>
<td>0.5 mV$_p$</td>
<td>0.7mV$_p$</td>
<td>100 mV$_p$</td>
</tr>
<tr>
<td>Input-referred noise (V$_{rms}$)</td>
<td>LFP: 1 µV</td>
<td>LFP: 6.7 µV</td>
<td>AP: 4.7 µV</td>
<td>LFP: 4.3 µV</td>
<td>LFP: 1.3 µV</td>
<td>4.13 µV</td>
</tr>
<tr>
<td>NEF</td>
<td>LFP: 4.6</td>
<td>LFP: 14</td>
<td>AP: 5.99</td>
<td>LFP: 30</td>
<td>LFP: 4.76</td>
<td>3.19</td>
</tr>
<tr>
<td>DC Input-impedance</td>
<td>8 MΩ</td>
<td>6 MΩ</td>
<td>∞</td>
<td>28 MΩ</td>
<td>∞</td>
<td>1.52 GΩ</td>
</tr>
<tr>
<td>Off-chip caps</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Dynamic Range $^b$</td>
<td>67 dB (LFP)</td>
<td>N/A</td>
<td>~35 dB</td>
<td>50 dB (LFP)</td>
<td>44.6 dB</td>
<td>83 dB (AP)</td>
</tr>
<tr>
<td>Total Harmonic Distortion</td>
<td>~60 dB</td>
<td>N/A</td>
<td>~37 dB</td>
<td>~48 dB</td>
<td>~40 dB</td>
<td>~85 dB</td>
</tr>
<tr>
<td>Tolerance to large-signal CM</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Up to 700 mV$_{pp}$</td>
</tr>
<tr>
<td>Area/ch</td>
<td>1.7 mm$^2$</td>
<td>0.2 mm$^2$</td>
<td>0.013 mm$^2$</td>
<td>0.025 mm$^2$</td>
<td>0.042 mm$^2$</td>
<td>0.06 mm$^2$</td>
</tr>
<tr>
<td>Technology</td>
<td>0.8µm</td>
<td>65nm</td>
<td>65nm</td>
<td>65nm</td>
<td>65 nm</td>
<td>40nm</td>
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</table>

Table 3. Comparison of the proposed chopper amplifier with state-of-the-art neural recording amplifiers.
CHAPTER 7

A power-efficient high-resolution continuous-time ΔΣ-ADC for neural recording front-ends

7.1 ADC requirements

Before embarking on the design of the ADC, we must determine the key performance requirements of the ADC, like power consumption, ENOB, signal BW etc. To digitize the local-field potentials and action potentials, the ADC signal bandwidth must be 5kHz. As discussed in section 3, the power consumption of the neural recording front-end should be less than 10µW/channel. The CCIA presented in the previous chapter consumes 2.8µW. After digitization, some signal processing (eg: filtering) may need to be performed on the recorded data. Hence, we set the ADC power consumption to be less than 5µW/channel, which allows for an additional 2µW for digital processing. The ADC ENOB requirement is determined as follows. The peak differential input to the ADC is 0.8Vp, corresponding to the maximum output signal of the CCIA. The CCIA’s input-referred noise is 5.6µVRms (1Hz – 5kHz), which along with a 100mVP input signal range, leads to a peak SNR of 82dB. The ADC’s input-referred noise is set to 16µVRms. Since the CCIA gain is 8, the electrode-referred noise contribution of the ADC is 2µVRms. Hence, the input-referred noise of the recording front-end is 5.95µVRms, leading to a peak SNR of 81.5dB. This provides some margin from the required SNR of 80dB. Note that distortion power will also need to be kept low to ensure that the dynamic range of 80dB is achieved. Thus, the peak SNR of the ADC is 91dB for a 0.8Vp input signal. Assuming the noise budget of 16µVRms includes distortion, the ADC ENOB requirement is 15b.
The reference voltage for the ADC is usually set to the peak input signal amplitude, which is 0.8V. However, we keep additional margin on this to allow for a graceful degradation of SNDR above the peak input signal. The 1.2V supply can be used as a reference; however, the supply noise would degrade the SNR of the ADC. A low-noise reference voltage is necessary, which after a suitable analog buffer, can be used as the ADC reference. Hence, the ADC reference voltage is chosen to be 1.1V, so that an analog buffer operating from 1.2V can be designed with 100mV headroom for the output PMOS device. The ADC reference is expected to drive switching loads, which should be considered while designing the reference buffer.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>&lt; 5 µW per channel</td>
</tr>
<tr>
<td>ENOB</td>
<td>15 bits</td>
</tr>
<tr>
<td>Signal BW</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Input Signal Range</td>
<td>1V_p</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>High ( &gt;2MΩ)</td>
</tr>
</tbody>
</table>

Table 4. Summary of performance requirements for the ADC.

The ADC performance requirements are summarized in Table 4. An input-impedance requirement is also included, without explicitly quantifying the requirement. A low input-impedance would demand higher power consumption from the previous stage (in this case, the CCIA) to drive the ADC. To ensure that the overall front-end power consumption is kept low, the ADC’s input impedance should be large. Assuming an input impedance of 2MΩ, the power consumed in driving the ADC input for a 1V_p signal swing is 0.25µW, which is a small fraction (5%) of the available power budget. Hence, we target a minimum input impedance of 2MΩ.
7.2 ADC Architecture Exploration

Based on the bandwidth and ENOB requirements of the ADC, we see from Figure 59 that the SAR and Delta-Sigma topologies have been widely used in prior work, since they are the most power efficient for this range of bandwidth and ENOB [50]-[52]. We consider both architectures next, and see which one may suit our needs.

![Design space for closed-loop neural recording](image)

**Figure 59.** A plot showing the ENOB-frequency range of various ADC architectures.

### 7.2.1 SAR ADCs

SAR ADCs have proved to be the most power-efficient ADCs for ENOB < 12b [53]-[64]. This is primarily because SAR ADCs have almost no constant power drain (or analog power), as shown in Figure 60. Their power consumption is dominated by switching power, which scales very well with technology nodes.
Figure 60. Block diagram of a typical SAR ADC.

However, SAR ADCs have the following limitations for ENOB > 12b.

a) The CDAC and comparator power consumption increases by 4x for every additional bit of resolution (assuming a fixed reference voltage). Hence, even if we can design a very-low power SAR ADC with an ENOB of 10b, the power consumption would increase by a factor of $10^3$ when scaled to an ENOB of 15b. For example, the work in [56] shows a 10.1b-ENOB SAR ADC in 65nm-CMOS, consuming 50nW for a sampling rate of 20kHz. Scaling this ADC to 15b-ENOB would increase the power consumption to 50µW, which is 10x larger than our requirement.

b) Capacitor matching in the CDAC of the SAR-ADC is difficult to achieve on-chip beyond and ENOB of 10b. These mismatches will cause nonlinearity in the CDAC, which will limit the ENOB of the ADC. Calibration and mismatch-shaping techniques can be used, which would increase power consumption.

c) The power consumption of the sample-and-hold (S/H) block (Figure 60) is often ignored while reporting ADC performance in publications [53]-[64]. However, the power consumption of the S/H block is comparable, and sometimes greater than the ADC power consumption. This is because the sampling capacitance in the S/H block must be large enough to keep the kT/C noise associated with sampling lower than the available noise budget.
For the above-mentioned reasons, a SAR-ADC implementation would exceed the power consumption requirements of our neural recording front-end. Next, we consider the delta-sigma ADC.

### 7.2.2 Delta-Sigma ADCs

The delta-sigma ADC [65]-[68], shown in Figure 61(a), is formed by a coarse quantizer which is placed in a negative feedback loop along with a feedback-DAC and a loop-filter. The quantizer can be approximated as an additive noise source, where the noise samples are uncorrelated. This approximation is not true since the quantization noise is a function of the input signal. However, this approximation of uncorrelated additive noise works well for quantization levels beyond 10, and we use this approximation to simplify analysis. The quantization noise spectral density is shown in Figure 61(b). The loop-filter is a low-pass filter, with a large gain at low frequencies. Hence, the quantization-noise spectrum at the output of the ΔΣ-ADC is high-pass shaped, as shown in Figure 61(b). For a narrow signal-band at low frequencies, the quantization-noise at the output of the ΔΣ-ADC is significantly lower than the noise of the coarse quantizer. Thus, through a combination of oversampling and noise-shaping, the ΔΣ-ADC achieves a much higher resolution as compared to the coarse quantizer. Hence, only modest demands are made on the accuracy of the analog components, as opposed to other ADC architectures.
ΔΣ-ADCs can be broadly classified as discrete-time (DT) or continuous-time (CT) ΔΣ-ADCs, corresponding to a discrete-time or continuous-time loop-filter. The continuous-time implementation has several advantages [69]. Due to the reduced settling requirements as compared to a DT loop-filter, the opamps in the CT loop-filter have reduced BW requirements, potentially reducing power consumption. The CT ΔΣ-ADC has inherent anti-aliasing, since sampling happens
after the loop-filter (Figure 62). Any wide-band noise that would alias to baseband is indistinguishable from the quantization noise of the quantizer. Hence, the aliased components are attenuated by the same baseband noise-shaping transfer function that keeps the in-band quantization noise low. Thus, an explicit anti-alias filter preceding the ADC is not required. Another advantage of the CT ΔΣ-ADC is that there is no sampling of the input signal in the loop-filter. Thus, there are no impedance requirements that need to be satisfied, unlike DT implementations where the minimum sampling cap is limited by kT/C requirements. In principle, the driving point impedance for all the opamps in the loop filter (except the last stage that drives the coarse quantizer) and the feedback-DAC reference buffer can be made arbitrarily large, which leads to reduced power consumption.

**Figure 62.** Block diagram of a continuous-time ΔΣ-ADC.

The disadvantages of CT ΔΣ-ADCs over DT ΔΣ-ADCs are as follows [65]. The loop-filter coefficients can be made immune to process and temperature variations in DT implementations, as the DT loop filter can be implemented using switched-capacitor circuits. However, in CT loop filters, the coefficients are usually a function of resistance and capacitance values, making them
sensitive to process and temperature variations. The CT ΔΣ-ADC is also more sensitive to clock-jitter as compared to the DT implementation [85].

The loop-filter coefficient variations in CT implementations can be countered through appropriate calibration techniques (eg: [70]) while consuming very low power. The clock-jitter sensitivity can be reduced by using multi-bit feedback DACs [69]. Also, clock-jitter sensitivity is reduced for lower sampling frequencies. Since our bandwidth requirements are rather small (5kHz), it can be shown that a clock generated from a standard crystal oscillator is more than sufficient for our requirements. The jitter requirements of the sampling clock are discussed in [85] and [89]. From the analysis in [89], and from simulations, it was determined that a clock-jitter of 150ps_{rms} would limit the SQNR of our modulator to about 115dB. A jitter of 150ps_{rms} is a relaxed requirement, since most commercially available crystal oscillators have a clock jitter less than 10ps_{rms}.

Hence, for the above-mentioned reasons, we chose a CT ΔΣ architecture over the DT counterpart to lower power consumption.
7.2.3 Review of state-of-the-art ΔΣ ADCs

ΔΣ ADCs have been widely researched over the last two decades, and a brief collection of the current state-of-the-art designs can be found in [69] and [72]-[82]. A rich body of literature exists that discuss various aspects of the design and analysis of ΔΣ ADCs. The unfamiliar reader interested in ΔΣ ADCs is referred to [65]-[69], [71] and [83]-[84] to gain a good understanding of the subject.

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<td>800</td>
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<td>280</td>
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<tr>
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<tr>
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<td>24k</td>
<td>25k</td>
<td>20k</td>
<td>20k</td>
<td>24k</td>
</tr>
<tr>
<td>Peak SNDR (dB)</td>
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<td>98.5</td>
<td>95.2</td>
<td>91.3</td>
<td>103</td>
<td>98.5</td>
</tr>
<tr>
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<td>100.6</td>
<td>100.1</td>
<td>N.A.</td>
<td>106</td>
<td>99.3</td>
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<td>SFDR (dB)</td>
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<td>100</td>
<td>98.4</td>
<td>107.4</td>
<td>107.6</td>
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<tr>
<td>DR (dB)</td>
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<td>100.6</td>
<td>103</td>
<td>103.1</td>
<td>109</td>
<td>103.6</td>
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<tr>
<td>FOMS,DR (dB)</td>
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<td>FOMS,SNDR (dB)</td>
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<td>65</td>
<td>160</td>
<td>160</td>
<td>180</td>
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</table>

Table 5. Performance summary of the current state-of-the-art ΔΣ-ADCs.

The state-of-the-art ADC performance is summarized in Table 5. The Figure of Merit (FOM) is often used to compare ADC performance [90]. The FOM is defined as \( FOM = SNDR + 10\log(BW/Pwr) \), and it captures the tradeoffs between noise, linearity, power consumption and signal bandwidth. To the best of our knowledge, the work in [77] reports the highest FOM to date.
for ADCs with ENOB>14b, with an FOM of 177.8dB. When scaled for our bandwidth and SNDR requirements, the design in [77] would consume 2.6x more power than our requirement. Also, [77] used a 1.8V supply, which is larger than the 1.2V supply that we are constrained to use due to system-level requirements. A larger supply voltage allows for a proportionally larger lsb value, increasing the available noise budget. For example, a 2x larger supply results in a 2x larger lsb. Hence the input-referred noise power of the ADC can be increased by 4x, equivalent to a 4x reduction in current consumption. The increased supply results in 2x higher power consumption (assuming a constant current consumption). Thus, overall, we see a 2x reduction in the ADC power for a 2x higher supply voltage. We ignored power consumption of digital blocks in this analysis, since the digital blocks usually consume a small portion of the ADC power (<30%). However, greater supply scaling will see more influence from the digital power consumption. Hence, when scaling [77] for our requirement, the power consumption using a 1.2V supply would be ~25µW, which is 5x higher than our requirement.

The prior art in Table 5 are stand-alone ADC designs, and they use an externally driven reference voltage for the ADC. The power consumption of this external buffer (and the decoupling-capacitor area) are seldom considered when reporting the performance of the ADC. In many applications (like audio etc), an external voltage reference, or an internal reference with a large off-chip decoupling capacitance, is permissible. However, as discussed in chapter 3, a neural implant can only support a very small number of off-chip components. Thus, we cannot rely on off-chip components, and all blocks need to be integrated on-chip in a reasonably small area. Also, the ADC power consumption requirement of 5µW includes all reference buffers.

Hence, from the above discussions, we see that to meet our requirements, the ADC power consumption needs to be reduced by a factor of 5 as compared to the state-of-the-art. Before
delving into ways of reducing power consumption, we first consider the various design choices in a CT $\Delta\Sigma$-ADC, like the order of the loop-filter, loop-filter topology, number of coarse quantization levels, oversampling rate etc.

### 7.2.4 Summary of design choices and tradeoffs in CT $\Delta\Sigma$-ADCs

The work in [69] and [83] discuss the various design choices and trade-offs for a CT $\Delta\Sigma$-ADC, and we give a brief overview here for completeness. A higher order loop-filter leads to greater attenuation of in-band quantization noise, enabling a reduced oversampling rate. However, increasing the loop-filter order reduces stability due to a larger number of poles in the loop. The loop-filter can be implemented in a CIFF or CIFB configuration. The CIFF loop-filter requires a single feedback DAC, instead of multiple feedback DACs in the CIFB loop-filter. To satisfy stability requirements, the unity-gain bandwidth (UGB) of the first integrator in the CIFF loop-filter must be larger than the UGB of the proceeding integrators. This leads to higher power consumption in the 1st integrator, which is also required for lowering noise. However, a CIFB loop-filter requires the last integrator to have the highest UGB for stability. Thus, CIFB loop-filters need to burn sufficient power in the last integrator to satisfy stability, but also need to burn sufficient power in the first integrator to satisfy noise. Hence a CIFF loop-filter optimally uses the available power consumption by satisfying both noise and stability requirements simultaneously.

The out-of-band (OOB) gain of the noise transfer function (NTF) needs to be appropriately set depending on the design requirements. A larger OOB gain enables a more aggressive NTF, but reduces the maximum stable amplitude (MSA) due to the saturation of the coarse quantizer. A larger number of quantizer levels enables a relaxed NTF, reduces the slewing requirements of opamps in the loop-filter, and reduces the sensitivity of the CT $\Delta\Sigma$-ADC to clock-jitter (assuming
a Non-Return-to-Zero (NRZ) DAC pulse). However, a larger number of quantizer levels requires a higher-resolution feedback DAC, and the unit-element mismatches in the DAC need to be addressed to mitigate DAC nonlinearity. Mismatch-shaping algorithms can be used [91]-[92] that shape the DAC errors out of the signal band. However, the power consumption of these algorithms increases with increasing number of DAC levels. Any excess loop-delay (ELD) introduced by mismatch-shaping in the feedback path needs to be compensated.

![Figure 63. Architecture of the proposed CT ΔΣ-ADC.](image)

The reference voltage used for the feedback DAC and the coarse quantizer should be as large as possible to relax the noise requirement of the ADC, or increase the lsb value. The available 1.2V supply can be used as the reference voltage; however, supply-noise will increase the feedback-DAC noise and degrade the ADC performance. A low-noise reference voltage can be generated on-chip and shared among all ADCs. However, the reference must be buffered since it must drive
switching loads. A reference of 1.1V is chosen, since this allows for a 100mV headroom (given that the supply is 1.2V) for the analog buffer that drives the feedback DAC.

The CT ΔΣ-ADC used in this work is shown in Figure 63. A 3rd order CIFF loop-filter was chosen along with an OSR of 40. The OOB gain of the NTF was 2.5, and a 6b-SAR ADC was used as the coarse quantizer. The reasons for these specific design choices are explained next.

There are several advantages when using a multi-bit quantizer in the ΔΣ-ADC, as discussed in [69]. However, a larger number of quantizer levels increases the implementation complexity and power consumption of the quantizer. A multi-bit quantizer also requires a multi-bit DAC in the feedback path, which necessitates the use of DAC error correction/shaping algorithms. This is because mismatches among the unit-elements of the DAC are inevitable, which causes nonlinearity in the DAC. The power consumption of the mismatch-shaping logic increases with increasing number of DAC levels. Hence, as a compromise, a 6b-quantizer was chosen. The quantizer was implemented as a 6b Asynchronous SAR-ADC, since it is the most power-efficient ADC for low ENOBs. A SAR-ADC is also easier to implement, as opposed to a flash-ADC, which would require 64 comparators. The convergence time of the SAR-ADC and the mismatch-shaping logic would add excess loop-delay, which will be compensated in the loop-filter.

Since a 6b-SAR ADC is used as the coarse quantizer, a 6b-DAC is needed in the feedback path. The unit-element mismatch in the feedback DAC was assumed to be 1%, which is achievable using careful layout [93], [94]. This results in an inherent DAC SNDR of 62dB (Figure 64). Data-weighted averaging (DWA) can be used to provide 1st order high-pass shaping to the feedback-DAC errors. More complex mismatch-shaping algorithms are available to provide higher-order
shaping to the DAC errors, but their implementation would consume significantly higher power as compared to 1st order DWA.

Hence to keep digital power consumption low, we chose the simple 1st order DWA. Since the raw SNDR of the DAC is 62dB, we need an additional 40-45dB improvement in the DAC SNDR to exceed the overall ADC SNDR requirement of 92dB. An OSR of $2^5 = 32$ would ideally improve the DAC SNDR by an additional $(1.5) \times 5 = 7.5b$, resulting in an effective DAC SNDR of 107dB. Hence, an OSR of 40 was chosen to provide sufficient margin on the minimum-required OSR of 32.

![Figure 64. Simulations of a 6b-DAC with 1% unit-element mismatch.](image)

An ideal DAC with unit-element mismatch of 1% was simulated by providing a clean sinusoid as the digital input sequence. The input sequence was generated using an ideal 3rd order digital ΔΣ ADC with an OSR of 40, with an input SNDR of 112dB in the signal band. The simulated outputs of the DAC are shown in Figure 64. We see that by using an OSR of 40 and 1st order DWA, the
in-band SNDR is improved from 62dB to 101.5dB. This verifies our choice of OSR to ensure sufficient DAC performance.

Since the OSR is 40 (from the previous discussion), from simulations using the delta-sigma toolbox [88], and using custom routines in Matlab, it was determined that a minimum loop-filter order of 3 was necessary to achieve the required SNDR.

![Output spectrum of a simulated CT ΔΣ-ADC (100 trials).](image)

**Figure 65.** Output spectrum of a simulated CT ΔΣ-ADC (100 trials).

The simulated output spectrum for 100 trials is shown in Figure 65. These simulations include DAC nonlinearity and 1st order DWA, clock-jitter of 150ps rms, SAR comparator noise (0.25 lsb), quantizer nonlinearity (1% unit-mismatch), integrator finite-gain and integrator non-dominant poles. The loop-filter coefficients were chosen while accounting for dynamic-range scaling to ensure that the integrator output swings were well within the supply.
Figure 66. Histograms of SNDR and SFDR, corresponding to the CT ΔΣ-ADC simulations in Figure 65.

The histograms of SNDR and SFDR for the 100 trials are shown in Figure 66, which shows a minimum SNDR of 97.4dB and minimum SFDR of 98.7dB. These simulations only include quantization noise; the thermal and flicker noise contributions are not included for now. Once the transistor-level implementations of the various blocks are determined, the thermal and flicker noise can be included in simulations. Now that a suitable CT ΔΣ-ADC architecture has been determined, we investigate the dominant power contributors, and how to reduce power consumption.
**Figure 67.** A typical CT ΔΣ-ADC. The errors introduced by the 1st integrator and feedback DAC are added directly at the input.

The power consumption in CT ΔΣ-ADCs is dominated by the 1st integrator and the feedback-DAC, since these blocks determine the overall noise and linearity performance of the ADC (Figure 67). The digital blocks (quantizer and DWA logic) usually account for about 25% of the total power consumption. The designs in [72] and [77] were implemented in 180nm-CMOS, and moving to an advanced technology node (in our case, 40nm-CMOS) will help to keep digital power consumption low. However, the power consumption of the analog blocks (1st integrator and feedback-DAC), which dominates the overall ADC power (~75%) does not scale with technology nodes. Hence, we focus on reducing power consumption in the analog blocks, with the aim of reducing the overall ADC power consumption.
7.3 Comparison of loop-filter/DAC architectures in CT ΔΣ-ADCs

Since the 1st integrator and feedback-DAC are the dominant power contributors, we review how these blocks have been implemented in state-of-the-art CT ΔΣ-ADCs.

7.3.1 Gm-C Integrators

The Gm-C integrator is a common implementation of the 1st integrator in the loop-filter (Figure 68). The Gm-C integrator consumes significantly lower power as compared to the Active-RC integrator, since there is no local feedback in the Gm-C integrator. However, due to its open-loop nature, the linearity of the Gm-C integrator is limited, and linearization techniques need to be adopted to meet the ADC linearity requirements [95].

![Gm-C integrator diagram](image)

**Figure 68.** A CT ΔΣ-ADC using a Gm-C integrator.

Source-degeneration has been successfully used to improve linearity [95]. However, source-degeneration results in significantly higher input-referred noise as shown in Figure 69. This increase in noise translates to higher power consumption. Hence, the low-power advantage of the Gm-C integrator is negated by employing source-degeneration. Note that the equation in Figure 69 does not include the noise contribution from the tail-current sources. By using source-
degeneration, the noise contribution of the tail-current sources is no longer common-mode, which would further degrade the input-referred noise.

\[ v_{n,in}^2 = \frac{8kT\gamma}{g_m} \left[ 1 + \frac{g_m R_D}{\gamma} \right] \]

**Figure 69.** Source degeneration to improve linearity of a diff-pair (left) leads to increased input-referred noise (right).
7.3.2 Active-RC integrators

The active-RC integrator is a widely used topology for the 1st integrator in the loop filter. Due to the local feedback around the integrator opamp, the active-RC integrator provides excellent linearity. However, the local feedback loop increases the power consumption of the integrator opamp, since stability must be guaranteed in unity-gain feedback by having sufficient phase margin. The RC feedback network also loads the output of the opamp, leading to larger bias current requirements (assuming class-A operation).

![Active-RC integrator](image)

**Figure 70.** (a) A CT ΔΣ-ADC using an active-RC integrator. (b) The active-RC integrator and feedback-DAC (right).

Apart from the above-mentioned sources of higher power consumption, it can be shown that the power required to drive the input and DAC resistance is much larger than the power consumption of the opamp itself. We refer to Figure 70(b) for this analysis. If a current-reuse fully-differential opamp is used, the input-referred noise is given by equation 17.

\[ V_{n, in}^2 \approx 4 \left( \frac{4kTg}{g_{m1}} \right) + 8kTR_{in} \]  

(17)
For the active-RC integrator in Figure 70(b), the total power consumption consists of the opamp power and the power required to drive the input and DAC resistances ($R_{in}$, $R_{DAC}$). Equation (18) shows the total power consumption.

$$P_{WR} = (I_{amp} + I_{DAC} + I_{Driver}) \cdot V_{DD}$$

(18)

The input devices of the integrator opamp are biased in weak inversion to reduce power. Hence, we assume that $g_{m1}/I_d = 20$, where $g_{m1}$ is the transconductance of the input device, and $I_d$ is the bias current flowing through the input device. Also, we assume that the peak input swing is $V_{dd}$. By making these substitutions in equation (18), the power consumption is now given by equation (19).

$$P_{WR} \approx \left( \frac{g_{m1}}{10} + \frac{2V_{DD}}{R_{in}} \right) \cdot V_{DD}$$

(19)

For the active-RC integrator in Figure 70(b), it can be shown that for a given noise budget, the power consumption is minimized when $g_{m1}R_{in} \approx 5.65$. Hence, we can compare the power consumed in the opamp and the power consumed in driving $R_{in}$ and $R_{DAC}$, as shown in equation (20).

$$\frac{I_{amp}}{I_{DAC} + I_{Driver}} = \frac{g_{m1}R_{in}}{20} \approx \frac{1}{3.53}$$

(20)

From the above equation, we see that far more power is burnt in the input and DAC resistors than in the opamp itself! Publications of stand-alone ADCs usually do not report the power consumed by the stage driving the ADC input and the feedback-DAC reference buffer. However,
we have a constraint on the power consumption of the complete recording front-end, hence all relevant power contributors need to be considered.

The above analysis assumed that the input signal to the ADC was the peak value of the input, which is $V_{dd}$. This is a pessimistic assumption, since it is unlikely the input will be near the peak value for all time. However, for class-A implementations of the ADC driving stage and the DAC reference buffer, the peak value of the load current sets the bias currents, leading to large power consumption as predicted by equation (20). Class-B or higher implementations can be used; however, they can be difficult to implement due to the high linearity requirement (>100dB) of the ADC. Also, even with Class-B implementations, the power consumption during stimulation artifacts will be similar to the predictions of equation (20), making the front-end power consumption a function of the activity at the recording sites. This complicates system-level power management (LDO design, battery discharge-time estimation etc).
### 7.4 Proposed loop-filter for a low-power CT ΔΣ-ADC

A possible approach to reduce power is to either increase the value of $R_{in}$ and $R_{DAC}$ without degrading noise, or modify the integrator topology to remove the resistances altogether. A simple implementation of this approach is shown in Figure 71, where a small gain-stage is added before the 1st integrator.

![Proposed loop-filter for a CT ΔΣ-ADC](image)

**Figure 71.** Proposed loop-filter for a CT ΔΣ-ADC, with a gain-stage preceding the 1st integrator.

Let’s assume that a gain of 4 is added before the 1st integrator, implemented as a capacitive-feedback inverting amplifier (Figure 71). Hence, $R_{in}$ can be increased by 16x for the same noise contribution as before, which significantly reduces the power required to drive $R_{in}$. Also, the signal appearing across $R_{in}$ now consists of the error signal ($V_{in} - V_{fb}$) amplified by 4, which is significantly smaller than the peak input signal ($V_{in}$), assuming a coarse quantizer resolution larger than 3b. The input and DAC resistance ($R_{in}$, $R_{DAC}$) from Figure 70(b) are now replaced by capacitors $C_{in}$ and $C_{DAC}$. These capacitances can be made arbitrarily small since there is no $kT/C$ requirement for CT loop-filters. Hence, the power burnt by the ADC driving stage and the DAC reference buffer can be significantly reduced. The power burnt in this composite integrator (Figure 71) is now dominated by the opamp used in the gain-stage, which can be optimally designed. The
gain preceding the 1st integrator is limited to 4 to limit the signal swings at the output of the gain stage. A larger value of the gain would further reduce noise from the 1st integrator; however, this would result in larger swings at the output of the gain stage, leading to increased distortion.

The power reduction by using the 4x gain-stage can be quantified as follows. The PowerXNoise product for the active-RC integrator and the capacitive-feedback inverting gain stage is shown in Figure 72. Here, the noise is integrated only in the signal-band, due to the inherent anti-aliasing property of the CT ΔΣ-ADC.

\[
[Pwr \times Noise]_1 \approx 29.35kT
\]

\[
[Pwr \times Noise]_2 \approx 1.62kT
\]

**Figure 72.** Comparison of the Power x Noise product, for the active-RC integrator and the capacitive-feedback inverting amplifier. The noise in the signal-band is considered.

Hence, we see that for the same noise budget, the capacitive gain stage consumes 18.1x lower power. This comparison is not complete, since the power and noise contributions of the integrator after the gain stage is not included in [Pwr X Noise]_2. However, even after accounting for the integrator after the gain stage, the power is reduced by a factor of ~10.

Thus, we show that a simple modification to the 1st integrator (Figure 71) significantly reduces the power consumption of the integrator, the reference DAC buffer and the ADC-driving stage.
However, by using the gain-stage as shown in Figure 71, the noise and linearity performance of the ADC are now limited by the gain stage. We have addressed *thermal noise* in this section. Next, we consider the nonlinearity of the gain stage.

### 7.5 Loop-filter impairments and techniques to mitigate them

#### 7.5.1 Gain-stage nonlinearity

The signal flowing through the gain-stage in Figure 71 is the difference between the ADC input $V_{in}$ and the feedback-DAC output $V_{fb}$. This is shown in Figure 73(a). The error signal, $V_{er} = V_{in} - V_{fb}$, is dominated by shaped quantization noise, as shown in Figure 73(b). Thus, the output of the gain-stage is ideally a scaled version of the shaped quantization noise. However, if the gain-stage is nonlinear, we see spectral broadening at the output of the gain stage. Figure 73(c) shows an example where the gain-stage transfer characteristic is approximated by a 3rd order polynomial. The presence of the non-zero cubic term in the transfer characteristic leads to a raised in-band quantization noise floor. The increased in-band noise shown in Figure 73(c), when referred to the input of the ADC, is attenuated by 4. This attenuation is rather small, and the increased in-band noise could significantly degrade the ADC performance.
Figure 73. (a) A diagram showing the error signal $V_{er}$ seen at the input of the gain-stage shown in Figure 71. (b) Spectrum of the error signal $V_{er}$. (c) Spectrum of $V_{o1}$, for a linear gain-stage (black) and a nonlinear gain-stage (red).

An appropriate transistor-level gain-stage was simulated to verify this problem, and the in-band SQNR degraded from 104dB to 87dB. The source of the nonlinearity was traced to the input devices of the opamp used in the gain stage. The gain-stage is redrawn in Figure 74. When the feedback-DAC updates its output, there is a sudden change in $V_{fb}$. This step-input to the gain-stage
results in an exponentially decaying error signal $V_{er}$ at the virtual ground (Figure 74). $V_{er}$ decays to near-zero rather quickly, since the time-constant of the gain-stage is much smaller than the oversampling period of the ADC to maintain stability. However, the large glitches in $V_{er}$ push the input devices of $g_m$ from their linear region of operation, leading to distortion. Since the input devices would be biased in weak inversion to minimize their [Pwr X Noise] product, their linear performance is even more sensitive to the large excursions in $V_{er}$.

![Figure 74.](image)

**Figure 74.** The capacitive-feedback gain stage, showing large glitches at $V_{er}$ during transitions in the feedback-DAC.

To improve gain-stage linearity, the opamp linearity under large $V_{er}$ must be improved. As discussed in section 7.3.1, source-degeneration improves the linearity of the diff-pair opamp, but leads to increased noise. However, from Figure 74, we see that the gain-stage needs to be linearized only for a small duration immediately after the feedback-DAC updates its output. This observation leads us to the following solution. We use time-varying source-degeneration to improve linearity, as shown in Figure 75. Source-degeneration is enabled at the beginning of every DAC transition for a period of $T_s/12$, which linearizes the gain-stage during the large excursions in $V_{er}$. Here, $T_s$ is the oversampling period. Source-degeneration is disabled for the rest of the clock period by shorting the resistor $R_D$ (Figure 75), since $V_{er}$ returns to a small value within $T_s/12$. This ensures that for the rest of the clock period ($T_s \cdot 11/12$), the degeneration-induced noise is not added in the
gain stage. Hence, the gain-stage linearity is improved, while the noise due to degeneration is substantially reduced. Note that by using source-degeneration, the duration of the glitch in $V_{er}$ is increased due to the reduced transconductance of the diff-pair in Figure 75. This increased duration is accounted for by appropriately increasing the OFF-duration of $\phi_D$.

**Figure 75.** Proposed duty-cycled source-degeneration technique to improve linearity without degrading noise (left), and control waveforms (right).

![Proposed duty-cycled source-degeneration technique to improve linearity without degrading noise](image)

**Figure 76.** Output spectrum of the gain-stage, when the gain-stage is used in an otherwise ideal CT $\Delta\Sigma$-ADC. The spectrum shows reduced in-band noise due to improved linearity when time-varying source-degeneration is used.

The time-varying source-degeneration was verified in simulations by using a suitable transistor-level implementation of the gain stage. The output spectrum of the gain stage is shown
in Figure 76. The in-band SQNR of the ADC has been restored from 87dB to 104dB by using the proposed technique, while the thermal noise of the gain-stage increased by only 0.7dB.

Next, we consider the flicker noise of the gain stage.

### 7.5.2 Flicker noise of the gain stage

It was mentioned in section 7.4 that the input and DAC capacitance ($C_{in}$ and $C_{DAC}$) of the gain-stage can be made arbitrarily small, since there are no $kT/C$ limitations. Reducing the capacitance reduces the loading on all the stages that drive these caps, thus reducing power consumption. However, due to the non-zero gate-capacitance $C_g$ of the opamp in the gain-stage (Figure 77), the input-referred noise increases if $C_{in}$ and $C_{DAC}$ are made smaller, as shown in equation (21).

$$\nu_{n,in} = \nu_n \left[ \frac{2C_{in} + C_f + C_g}{C_{in}} \right]$$  \hspace{1cm} (21)

**Figure 77.** The capacitive gain-stage, along with the gate-capacitance $C_g$ of the opamp. A larger value of $C_g$ increases the input-referred noise of the opamp.
To ensure that $C_{in}$ and $C_{DAC}$ can be made small, the gate capacitance $C_g$ must be small. This requires reducing the area of the input devices of the opamp used in the gain stage. However, smaller input devices lead to higher flicker noise. Since the neural signals of interest occupy a frequency band starting from 1Hz, the flicker noise of the gain-stage would degrade the low-frequency performance of the ADC. The ADC flicker noise may not be a concern in conventional neural recording front-ends where a large gain is used in the electrode-interface amplifier. However, the CCIA gain is limited to 8 to accommodate the large stimulation artifacts appearing at the recording sites. Hence, the ADC’s flicker noise would not be sufficiently attenuated when referred to the electrodes.

Chopping can be used to mitigate the flicker noise of the gain stage, just as it was used in the CCIA. However, chopping causes an aliasing problem [77], which we discuss next.

Let’s assume that we need to filter out the flicker noise of an amplifier labeled as A in Figure 78. This can be done by using chopping around the amplifier: placing an up-modulation mixer before the stage A, and using a de-modulation mixer after the stage A to restore the signal of interest to baseband. The mixers are implemented using commutating switches, thus implementing multiplication with a 50%-duty-cycled square wave transitioning between ±1. If the stage A is ideal, i.e. A has infinite bandwidth, then the output $V_{out}$ is identical to $V_{in}$. However, all practical implementations of A will have a limited bandwidth. Hence at the beginning of every chopping phase, the output $V_{out}$ will have a glitch, since A requires some time to acquire the new value of $V_1$ (Figure 78). Thus, $V_{out}$ consists of the sum of the input $V_{in}$ and an error signal corresponding to the glitches. This error signal $V_{er}(t)$ (not the virtual ground voltage in Figure 77) is shown in Figure 78. We can approximate $V_{er}(t)$ as a train of impulses, where the area of each impulse is
equal to the area under each decaying glitch. Hence, \( V_{er}(t) \) can be approximated by the following digital sequence

\[
V_{er}(n) = (2\tau) \cdot V_{in}(nT/2)
\]

(22)

where \( \tau \) is the time-constant of the stage A. We assume that A is a first-order system, since it simplifies the analysis while providing sufficient intuition.

**Figure 78.** A simple analysis to determine how the finite-BW of stage-A leads to aliasing when chopping is employed.

Hence, since \( V_{er} \) consists of \( V_{in} \) sampled at \( 2f_{chop} \), chopping leads to aliasing from multiples of \( 2f_{chop} \). The gain term associated with this aliasing \( (2\tau) \) is usually much smaller than 1. Hence, if there are no large OOB signals present at \( V_{in} \), the aliased components at \( V_{out} \) are very small, and can be ignored. This is the case for the CCIA that was discussed in chapter 6. However, the signal flowing through the capacitive gain-stage shown in Figure 71 is shaped quantization noise (Figure 79), which has a much larger noise density at OOB frequencies as compared to in-band.
frequencies. Hence, any aliased components from higher frequencies can significantly increase the in-band noise. An example of aliasing due to chopping is shown in Figure 79. The chopping frequency $f_{ch}$ is set to be $f_s/8$, where $f_s$ is the oversampling frequency of the ΔΣ-ADC. The noise density at $2f_{ch}$ and $4f_{ch}$ are about 65dB higher than the average noise density in the signal band. Simulations using a suitable transistor-level gain stage show that the in-band quantization noise increased by 20dB when chopping was enabled. Thus, chopping would reduce flicker noise, but would degrade the SNR of the ADC due to aliasing.

**Figure 79.** A typical spectrum of the error signal seen by the gain stage, showing high-pass-shaped quantization noise. Due to the large OOB noise density, aliasing due to chopping will degrade in-band noise. In this example, $f_s = 8f_{ch}$.

From equation (22), we see that to reduce the magnitude of the aliased components by 20dB, the bandwidth of the gain-stage should be increased by a factor of 10. However, this would significantly increase the power consumption of the gain-stage.
Figure 80. Typical spectral characteristics of shaped quantization noise at the output of the feedback-DAC. The spectrum has nulls at multiples of the oversampling frequency \( f_s \).

The above-mentioned chopping-induced noise aliasing occurs when an analog chopping operation is performed on shaped quantization noise. However, this can be avoided by performing the demodulation operation (corresponding to mixer \( M_2 \) in Figure 78) in the digital domain. However, this would lead to an increased signal bandwidth and a reduction in SNR, resulting in a significant increase in the power consumption of the ADC. This idea is discussed further in Appendix A.1.

Another alternative is found by realizing that the shaped quantization noise has naturally occurring spectral nulls at multiples of \( f_s \) (Figure 80). These nulls are the combined effect of the high-pass shaping NTF (repeated at multiples of \( f_s \)) and the sinc filtering due to the NRZ shape of the DAC pulse. Hence, if \( 2f_{ch} \) is set to \( f_s \), then aliasing due to chopping is mitigated, since the noise density at multiples of \( f_s \) is significantly smaller than at other frequencies. The additional attenuation provided by the aliasing gain (2\( \tau \)) is sufficient to keep the aliased noise much smaller than the in-band quantization noise (before chopping).
The above-mentioned choice of chopping frequency solves the aliasing problem. However, the restriction of using $f_{ch} = 0.5f_s$ presents another problem. The signal bandwidth is 5kHz. Hence, a chopping frequency of $\sim 25$kHz is more than sufficient to keep the signal of interest and the flicker noise far apart in the frequency domain, such that the up-converted flicker noise can be easily filtered out. Therefore, in the CCIA, the chopping frequency was chosen to be 25kHz. However, to mitigate the aliasing problem in chopping, we are restricted to use a chopping frequency of $0.5f_s$ in the $\Delta\Sigma$-ADC. As discussed in section 7.2.4, the ADC oversampling frequency $f_s$ is 400kHz, which implies that $f_{ch}$ must be 200kHz. This is 8x higher than the required chopping frequency. Such a large chopping frequency leads to frequent switching transients in the gain-stage, which can cause nonlinearity, as discussed in the next section.

7.5.3 Chopping-induced nonlinearity in the loop-filter

The feedback path of the CT $\Delta\Sigma$-ADC (Figure 81) consists of the reference buffer, an up-modulating passive mixer, and a bank of capacitors that form the feedback DAC. At every transition of the chopping clock, a large transient appears at the buffered reference, as shown in Figure 81. This is because the buffer has a non-zero output impedance, and the switching CDAC demands an impulse current at every chopping transition which the buffer is unable to provide. The large transient at $V_{\text{ref,buf}}$ propagates into the buffer, pushing devices from their linear region of operation. The transient also propagates to $V+/V-$, which is the virtual ground of the capacitive-feedback gain stage. As discussed in section 7.5.1, large excursions in the virtual-ground voltage will cause nonlinearity. Since these transients at $V_{\text{ref,buf}}$ occur at twice the chopping frequency, a higher chopping frequency leads to more frequent transients, which increases distortion. To verify this, we performed simulations of the CT $\Delta\Sigma$-ADC using a suitable transistor-level implementation of the reference-buffer and the chopped capacitive-feedback gain stage. The
The output spectrum of the ADC (Figure 82) shows large distortion components, which were absent when chopping was not used (Figure 65). The in-band SNR has degraded from 104dB to 54.9dB. The reference buffer was designed to minimize its power consumption while meeting the thermal and flicker-noise constraints of the ADC.

**Figure 81.** A diagram showing the reference buffer and the feedback DAC of the CT ΔΣ-ADC shown in Figure 71. Chopping leads to large glitches at the output of the buffer, which cause nonlinearity.

**Figure 82.** The simulated output spectrum of a CT ΔΣ-ADC with chopping. The spectrum shows large distortion components due to chopping-induced nonlinearity.
Since the reference-buffer is designed to minimize power consumption, its output impedance is not very low. Hence the glitch amplitudes can be reduced by reducing the output impedance of the buffer, which requires increased power consumption. An alternate solution is to use a large decoupling capacitor at \( V_{\text{ref, buf}} \), which provides the switching currents demanded by the CDAC during chopper-clock transitions, thus reducing the glitch amplitudes. However, the value of the decoupling capacitance necessary to restore linearity is rather large (~100pF). Such a large decoupling capacitance will occupy a large area on silicon. State-of-the-art ΔΣ-ADCs use off-chip decoupling capacitors to maintain a clean reference voltage. However, as discussed in chapter 3, off-chip components are not an option since our recording front-end must be implantable.

**Figure 83.** Proposed storage-capacitance based assistance for the reference buffer, and the corresponding control waveforms. The storage-capacitance \( C_s \) provides the instantaneous charge required by the switching CDAC load, thus reducing glitches.

We propose the following 2-step solution to the above-mentioned problem of reference glitches leading to distortion. The first step of the proposed solution is shown in Figure 83. By
recognizing that the CDAC requires an impulse current at every chopping-clock transition, we use a storage capacitor ($C_S$ in Figure 83) as follows. At the beginning of every chopping phase, the reference-buffer is disconnected from the CDAC, and the storage capacitor (pre-charged to $V_{\text{ref}}$) is connected to the CDAC. Hence the storage capacitor, which is significantly larger than the total CDAC capacitance, provides most of the charge required by the CDAC. At the end of this charge-sharing phase ($\phi_1$), $C_S$ is shifted back to the reference $V_{\text{ref}}$, while the reference-buffer now drives the CDAC to provide the required residual charge. Using this approach, the reference-buffer is assisted in providing impulse-currents to the CDAC, while the storage capacitance $C_S$ does not load the reference-buffer, thus maximizing the buffer’s bandwidth. The larger buffer-bandwidth enables $V_{\text{ref,buf}}$ to recover faster after the charge-sharing phase. Thus, the glitch amplitudes at $V_{\text{ref,buf}}$ are significantly reduced, and the capacitance $C_S$ can be made about 7x smaller than a stand-alone decoupling capacitance. From simulations, we determined that a 14pF storage capacitance was sufficient for $C_S$, which can be implemented in a reasonably small silicon area.

In the above-mentioned reference-buffer assistance (Figure 83), it was assumed that the reference $V_{\text{ref}}$ is generated by a single low-noise reference generator, with a high output impedance. Hence, when the storage capacitance $C_S$ is being pre-charged (phase $\phi_2$), the reference generator may have insufficient bandwidth. Thus, the benefit of reduced loading on the reference buffer during $\phi_2$ is negated. A simple solution to this problem is to add an additional buffer between $V_{\text{ref}}$ and $C_S$; hence $V_{\text{ref}}$ remains isolated from $C_S$. The power and noise requirements of this buffer would be minimal (~0.2µW), due to the long time-period available to pre-charge $C_S$. 
Figure 84. The capacitive-feedback gain stage with chopping, showing the reference-buffer assistance, dead-band switches and control waveforms to attenuate glitches at the input of $g_m$.

Though the above-mentioned reference-buffer assistance reduced the glitch amplitudes at $V_{\text{ref,buf}}$, the additional switching introduced by $\varphi_{1,2}$ in Figure 83 causes residual glitches at $V_{+/-}$. From simulations, it was observed that these residual glitches at the virtual ground of the capacitive-feedback gain stage were sufficiently large to degrade linearity. To shield the input devices of $g_m$ from these residual glitches, we added dead-band switches as shown in Figure 84. This is the second part of the 2-step solution to restore linearity with chopping. A dead-band duration ($\varphi_{db}$) of 12ns was sufficient, since the residual glitches created by the reference-buffer assistance decay to a small value beyond 12ns. Since every chopping phase is 2.5$\mu$s, the 12ns
dead-time is small enough to ensure minimal noise contribution from the sampled-noise on the gate capacitance of $g_{in}$.

**Figure 85.** The simulated output spectrum of a CT ΔΣ-ADC with chopping (red), and including proposed reference-buffer assistance and dead-band switches (blue).

The reference-buffer assistance and the dead-band switches were included in the transistor-level simulation of the CT ΔΣ-ADC with a chopped capacitive-feedback gain stage. The output spectrum of the ADC is shown in Figure 85, super-imposed on the spectrum without the proposed 2-step solution. The spectrum shows significant reduction in the distortion components, and the in-band SNR has been restored from 54.9dB to 102.3dB. This shows the efficacy of the proposed linearization techniques. Note that these simulations only include quantization noise; they do not include thermal and flicker noise. The SNR including thermal noise is about 95dB.
7.6 Complete implementation of the proposed CT ΔΣ-ADC

The complete implementation of the proposed CT ΔΣ-ADC is shown in Figure 86. For simplicity, Figure 86 shows the single-ended version of the ADC, while the fully-differential version was implemented. The CT ΔΣ-ADC was implemented in TSMC’s 40nm-CMOS technology (Figure 88), and the single-channel area is 0.053mm². The chopped capacitive-feedback gain-stage implements a mid-band gain of $C_{in}/C_f = 4$, where $C_{in}$ is 128fF and $C_f$ is 32fF. The multi-rate duty-cycled resistor $R_f$, implemented as a 3-stage resistor (with $R_f \approx 50\Omega$), sets the gate bias for the input devices in the gain-stage. The 6b feedback DAC is implemented as a bank of capacitors, with a unit capacitance of 2fF. To achieve a raw DAC SNDR of >60dB, the unit-element mismatch in the DAC must be less than 1%, as discussed in section 7.2.4. This mismatch requirement would set the minimum value of $C_u$. However, no mismatch data was available for TSMC’s 40nm technology for capacitors on the order of a few fF. Hence, to determine the minimum value of $C_u$, we relied on data reported in [93]-[94]. From these publications, we see that $C_u = 0.5fF$ provides the required 1% mismatch if $C_u$ occupies an area of ~4µm². However, the works in [93] and [94] were in 180nm and 65nm respectively; hence there could be some deviation in the mismatch. We kept sufficient margin in the design by using a unit capacitance of $C_u = 2fF$, which is 4x larger than the estimates from [93]-[94].
The loop-filter integrators are implemented as active-RC integrators. Since the gain-stage provides a gain of 4, the flicker noise of the 1\textsuperscript{st} integrator would be attenuated by only a factor of 4 when referred to the input of the ADC. Hence, we implement chopping in the 1\textsuperscript{st} integrator along with the gain-stage. For subsequent loop-filter stages, we do not require chopping due to the high gain of the 1\textsuperscript{st} integrator. The feedforward paths of the CIFF loop-filter are combined with the 3\textsuperscript{rd} integrator using capacitors $C_{11}$-$C_{31}$, where the loop-filter coefficients are implemented as the ratio of capacitors $C_{11}$-$C_{31}$/$C_{3}$. Excess loop-delay compensation (ELDC) is implemented by the capacitor $C_{11}$, which provides a feedforward path around the 3 integrators. The R-C component values in the loop-filter integrators are: $R_{1} = 3\,\text{M}\Omega$, $R_{2} = 25\,\text{M}\Omega$, $R_{3} = 60\,\text{M}\Omega$, $C_{1} = 1\,\text{pF}$, $C_{2} = 300\,\text{fF}$, $C_{3} = 200\,\text{fF}$.

**Figure 86.** Simplified single-ended implementation of the proposed CT $\Delta\Sigma$-ADC. The fully-differential version was fabricated. Single-ended version shown here for simplicity.
200fF. The impedances of the integrator’s feedback-network components were kept large to minimize the loading on the respective driving stages. Since $R_{2,3}$ are rather large (25MΩ and 60MΩ), we implement them as conventional duty-cycled resistors using a 1MΩ passive resistance. The switching frequency for the duty-cycled resistors $R_{2,3}$ are a multiple of $f_s$, to avoid aliasing OOB shaped quantization noise. The 6b-SAR ADC was used as the coarse quantizer, and the design was based on the concepts in [61] and [94]. Data weighted averaging (DWA) was used to shape the feedback-DAC errors [69]. The feedback-DAC reference buffer was implemented as a flipped voltage-follower, which provided >35dB suppression from the noise in the power supply. The reference voltage for the DAC was $V_{\text{ref}} = 1.1\,\text{V}$. The opamps used in the loop-filter integrators were implemented as 2-stage opamps with Miller compensation. The opamp schematics are shown in Figure 87.

**Figure 87.** Schematics of loop-filter opamps used in the proposed CT ΔΣ-ADC
Figure 88. Chip micrograph of the proposed CT ΔΣ-ADC (along with the CCIA proposed in chapter 6) in 40-nm CMOS.

7.7 ADC measurements

The measurement setup for the ADC is shown in Figure 89. The IC includes both the ADC and the CCIA shown in chapter 6. Provisions were made to test the ADC and the CCIA separately, and as a combined recording front-end. The 1.1V reference was generated off-chip on the PCB, and it was provided to the IC, where it was internally buffered by the DAC reference buffer. The available system clock was 12MHz. This rather high clock frequency is required for the digital control block (not implemented in this work) that will receive the ADC output data (after decimation to 25kHz) from several (~100) channels, serialize and packetize the data, and send it
to the low-power transceiver to stream the data out of the implant. To ensure that the digital controller could process the large data-rate of the implant, the frequency of the system clock (12MHz) was chosen to be much larger than the sampling rate of a single recording channel.

**Figure 89.** Measurement setup (top) and the bench-top test-PCB (bottom) for the fabricated front-end IC.

The measured output spectrum of the ADC for the peak SNDR is shown in Figure 90. For an input sinusoid with an amplitude of $-1.9$dBFS at 1kHz, the measured SNDR was 93.5dB. The full-scale amplitude corresponds to $V_{\text{ref}} = 1.1V$. A 512k-point Blackman-Harris window was used to reduce spectral leakage.
Figure 90. Measured output spectrum (corresponding to peak SNDR) of the CT ΔΣ-ADC.

When the proposed techniques (duty-cycled source degeneration, reference-buffer assistance, and dead-band switches) were disabled, the SNDR for a −1.9dBFS input degraded from 93.5dB to 47.2dB (Figure 91). We also had the option to disable the proposed techniques individually to measure the sensitivity of the SNDR to each technique. These measurements are shown in Figure 92, and the SNDR degrades to 91.2dB, 74.2dB and 49.2dB when the duty-cycled degeneration, dead-band time, and the reference-buffer assistance are disabled, respectively. These measurements show the efficacy of the proposed techniques in maintaining the low in-band noise and distortion in the CT ΔΣ-ADC. The measurements in Figure 92 also reveal that the ADC is most sensitive to disabling the reference-buffer assistance.
**Figure 91.** Measured output spectrum of the CT ΔΣ-ADC, with and without the proposed linearization techniques.

**Figure 92.** Measured output spectrum of the CT ΔΣ-ADC, with linearization techniques disabled.
The SNDR of the ADC was measured as a function of the input signal amplitude, as shown in Figure 93. This measurement was made for an input sinusoid frequency of 1kHz. The measurement shows that the peak SNDR of 93.5dB is achieved for an input amplitude of −1.9dBFS. We also measured the peak SNDR across the signal band, up to the maximum frequency of $f_{BW}/3$. The measurement shows that the worst-case peak-SNDR (93.5dB) is achieved at 1kHz. For this reason, we report all performance metrics at 1kHz.

![SNDR vs input amplitude and peak SNDR vs input frequency](image)

**Figure 93.** SNDR vs input amplitude (top), and peak SNDR vs input frequency (bottom).

The ADC response was also measured for a zero input to check for the presence of idle tones. The measured output spectrum is shown in Figure 94. The spectrum reveals tones at 253Hz and its harmonics. These idle tones are about 10dB smaller than the HD3 and HD5 components shown in Figure 90. The source of these tones is unclear, since there is no explicit clock/signal in the chip.
at these frequencies. During the design of the ADC, we estimated that it would be very unlikely for idle tones to appear, since a 6b coarse quantizer is used along with a 3\textsuperscript{rd} order loop filter. However, since these tones are quite small, they are inconsequential for our application.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure94.png}
\caption{Measured output spectrum of the CT ΔΣ-ADC for zero-input, revealing idle tones at 253 Hz and its harmonics. The power of the idle tones is lower than the in-band noise.}
\end{figure}

The anti-aliasing property of the CT ΔΣ-ADC is well known, and we measure this property for our fabricated prototype. The ADC was driven with tones at various frequency offsets from the oversampling frequency of $f_S = 400$kHz, and the measured response is shown in Figure 95. The measurement shows a minimum attenuation of 34dB in the signal band. Ideally, the attenuation would be greater than the attenuation provided by the NTF to quantization noise. However, the 2\textsuperscript{nd} and 3\textsuperscript{rd} integrators are not continuous-time, since we have used the duty-cycled resistor to implement the resistances $R_{2,3}$ (Figure 86). This duty-cycling to amplify the resistance leads to sampling at the input of the 2\textsuperscript{nd} and 3\textsuperscript{rd} integrators. Hence, the anti-aliasing attenuation corresponds to the attenuation provided by the 1\textsuperscript{st} integrator only. Also, the dead-band switches implemented
in the gain-stage (Figure 84) would cause some aliasing, due to the momentary sampling operation during the dead-time. This explains the reduced attenuation observed in Figure 95. However, an attenuation of 34dB is sufficient to filter out any OOB noise, since there are no large OOB interferers in closed-loop neural recording applications.

![Graph showing Gain vs Frequency Offset](image)

**Figure 95.** Measured anti-aliasing property of the CT ΔΣ-ADC for input frequencies around $f_s$.

The proposed ADC consumes a total power of 4.5µW from a 1.2V supply. The contributions to the power consumption are shown in Figure 96. The capacitive-feedback gain stage and the 1st integrator consume 48.4% of the total power. The rest of the loop-filter and the DAC reference buffer consume 26.9% of the total power, and all digital blocks (SAR-ADC, DWA logic, control signal generation) consume 24.7% of the total power.
Based on the measured performance of the proposed CT ΔΣ-ADC, the FOM can be calculated. Two widely used versions of the FOM are shown below [90]-

\[
FOM_1 = SNDR_{max} + 10 \log \left( \frac{BW}{PWR} \right)
\]

(23)

\[
FOM_2 = DR_{max} + 10 \log \left( \frac{BW}{PWR} \right)
\]

(24)

These FOMs capture the tradeoffs between power consumption, signal bandwidth, noise and distortion. From the measurements presented earlier, \( FOM_1 = 184 \text{dB} \) and \( FOM_2 = 187 \text{dB} \).
7.8 Comparison of proposed CT ΔΣ-ADC with current state-of-the-art ADCs

Table 6 compares the performance of our CT ΔΣ-ADC with the current state-of-the-art ADCs with ENOB>14b. Although we couldn’t find high-resolution ADCs for neural recording applications, a large body of work has been published in the field of high-resolution audio ADCs. Audio applications require a signal band of 20Hz - 20kHz and a peak SNDR of 90-100dB. Since these requirements are similar to our needs, we compare the FOM of our ADC to published audio ADCs.

<table>
<thead>
<tr>
<th>Spec</th>
<th>[72] JSSC’14</th>
<th>[73] JSSC’15</th>
<th>[74] JSSC’16</th>
<th>[75] JSSC’16</th>
<th>[76] JSSC’17</th>
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Table 6. Comparison of the proposed CT ΔΣ-ADC with state-of-the-art high-resolution ADCs.

From Table 6, we see that this work achieves >6dB higher FOM\(_1\) as compared to the state-of-the-art, which corresponds to a 4x reduction in power consumption for the same BW and peak SNDR. We also see that the requirements outlined in Table 4 have been achieved. It should be noted that we include the power and area of all blocks when reporting our performance in Table
6, including the feedback-DAC reference buffer and the reference decoupling capacitance. However, many of the other designs do not include these contributions. Also, the power required to drive the ADC input is not included in the comparison shown in Table 6. The input-impedance of the proposed ADC is a switched-capacitor resistance of $20\text{M}\Omega$, which is much higher than the input-impedance reported in [72]-[77]. This ensures that minimal additional power is required to drive the ADC input, further reducing the power consumption of the complete recording front-end.

![Figure 97](image.png)

**Figure 97.** A plot showing competitive ADC FOMs vs $f_{s,\text{Nyquist}}$, with data taken from the proceedings of the past 21 years of ISSCC and VLSI [96].

In Table 6, we compared the proposed ADC with state-of-the-art high-resolution ADCs (ENOB>14b). We can also compare this work with ADCs across all ENOBs, by comparing the respective FOMs. A repository of competitive ADC FOMs from the past 21 years of ISSCC and VLSI publications has been compiled in [96]. We use Figure 97 from this reference, and include
the performance of our ADC for comparison. Hence to the best of the author’s knowledge, from the comparisons shown in Table 6 and Figure 97, we report the highest FOM to date.

In this chapter, we have proposed a power-efficient CT ΔΣ-ADC, that can digitize the amplified electrode signals appearing at the output of the CCIA. The proposed ADC can also be used as a stand-alone recording front-end, by directly connecting the electrodes to the input of the ADC. For this direct digitization approach, the benefits offered by the CCIA (very-high input impedance, immunity to large in-band common-mode interference, electrode-offset filtering) would be lost. However, the stand-alone performance of the ADC would be sufficient for many sensing applications. Additional discussion on this approach is provided in the appendix.

So far, we have measured the individual performance of the CCIA and the CT ΔΣ-ADC. In the following chapter, we present the measured performance of the complete recording front-end.
CHAPTER 8

A front-end capable of closed-loop neural recording

8.1 Experimental results using a prototype of the complete neural recording front-end

The proposed neural recording front-end, which consists of the CCIA with gain = 8 (shown in chapter 6) and the CT ΔΣ-ADC (shown in chapter 7), is shown in Figure 98. The measured signal transfer function (STF) of the front-end is also shown in Figure 98. The STF is set by the CCIA, with a mid-band gain of 17.9dB, and a high-pass corner of 0.1Hz to filter ±100mV electrode offsets. The low-pass corner (not shown in Figure 98) is about 12kHz, although the signal band of interest is up to 5kHz. In the STF measurement for the CCIA (chapter 6, Figure 41), the low-pass corner was set by the passive low-pass filter formed by $R_L$ and $C_L$ in Figure 37. However, for the measurement in Figure 98, the resistance $R_L$ is reduced to 50kΩ, since the LPF is not required. This is because the CT ΔΣ-ADC provides inherent anti-aliasing, as discussed in chapter 7.

The input-referred noise measurement of the front-end is also shown in Figure 98. The input-referred noise in the LFP band is $1.8\mu V_{rms}$, and in the full signal band (1Hz - 5kHz) is $6.35\mu V_{rms}$. The input-referred noise is dominated by the noise contribution from the CCIA, which is about $6\mu V_{rms}$. The ADC’s noise contribution (referred to the electrode) is about $1.54\mu V_{rms}$. 

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Figure 98. The complete recording front-end (top) consisting of the CCIA from chapter 6, and the ADC from chapter 7. Measured signal transfer function and input-referred noise of the complete front-end (bottom).

Figure 99. Measured total harmonic distortion of the complete neural recording front-end.
The linearity measurement of the front-end is shown in Figure 99, and the THD is \(-81\)dB for a 200mV\(_{pp}\) sinusoid at 1kHz.

**8.2 In-vitro measurements using a prototype of the complete neural recording front-end**

In-vitro measurements were performed using a prototype of the proposed neural recording front-end to sense neural signals from electrodes dipped in Phosphate-Buffered Saline (PBS). These measurements follow the same procedure as shown in chapter 6 (section 6.6). The measured results are summarized in Figure 100, which show that the proposed front-end can indeed record neural signals in the presence of in-band differential and common-mode stimulation artifacts.

**Figure 100.** Summary of in-vitro measurements using the fabricated prototype of the proposed neural recording front-end (CCIA + ADC).
8.3 Comparison of the proposed neural recording front-end with state-of-the-art front-ends

Now that the complete front-end has been characterized, we can compare the proposed front-end with state-of-the-art front-ends intended for closed-loop neural recording. Table 7 presents the performance comparison.

<table>
<thead>
<tr>
<th>Spec</th>
<th>[97] TBCAS’16</th>
<th>[98] TBCAS’17</th>
<th>[32] VLSI’17</th>
<th>[40] JSSC’17</th>
<th>This work CCIA+ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power(µW) / Sup(V)</td>
<td>5.5 / 1.5</td>
<td>9.5 / 1.8, 0.9</td>
<td>8 / 1</td>
<td>7 / 1.2, 0.45</td>
<td>7.3 / 1.2</td>
</tr>
<tr>
<td>BW(Hz)</td>
<td>0.25 to 250</td>
<td>0.3 to 7k</td>
<td>DC to 500</td>
<td>0.1 to 200</td>
<td>0.1 to 5k</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>58.5</td>
<td>56</td>
<td>70.6</td>
<td>LFP: 75</td>
<td>Full BW: 78 LFP: 86</td>
</tr>
<tr>
<td>SNR / SFDR (dB)</td>
<td>N.A. / 74</td>
<td>57.6 / 61</td>
<td>N.A.</td>
<td>77.6 / 79</td>
<td>81 / 82</td>
</tr>
<tr>
<td>DR (dB)</td>
<td>60.5</td>
<td>59</td>
<td>73.6</td>
<td>LFP: 77.4</td>
<td>Full BW: 81 LFP: 90</td>
</tr>
<tr>
<td>FOM_{S,SNDR} (dB)</td>
<td>135.1</td>
<td>144.7</td>
<td>148.5</td>
<td>149.6</td>
<td>166.4</td>
</tr>
<tr>
<td>Area (mm²) / Tech (nm)</td>
<td>0.11 / 180</td>
<td>N.A. / 180</td>
<td>N.A. / 180HV</td>
<td>0.135 / 40</td>
<td>0.113 / 40</td>
</tr>
<tr>
<td>Peak Inp (V_{pp})</td>
<td>4m</td>
<td>10m</td>
<td>23.2m</td>
<td>100m</td>
<td>200m</td>
</tr>
<tr>
<td>THD @ peak inp (dB)</td>
<td>−72.4</td>
<td>−61</td>
<td>−73.6</td>
<td>−79</td>
<td>−81</td>
</tr>
<tr>
<td>Inp. ref. noise (µV_{rms})</td>
<td>1.58</td>
<td>4.57</td>
<td>1.7</td>
<td>LFP: 5.2</td>
<td>Full BW: 6.35 LFP: 1.8</td>
</tr>
<tr>
<td>Z_{in,DC} (MΩ)</td>
<td>62</td>
<td>∞</td>
<td>30</td>
<td>∞</td>
<td>1520</td>
</tr>
<tr>
<td>Large signal CM tolerance</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 7. Comparison of the proposed front-end (CCIA+ADC) with state-of-the-art front-ends intended for closed-loop neural recording.

Our front-end has comparable performance in terms of power consumption, noise and chip area. However, we show the following significant improvements over the state-of-the-art. The input-impedance (at DC) is 24.2x higher than other chopped front-ends. Since our front-end meets
the DC input-impedance requirement of 1GΩ, we do not need off-chip ac-coupling capacitors, ensuring that our front-end is implantable. The linear input-range is extended by 2x, and the signal bandwidth is extended by 10x over the state-of-the-art, ensuring that the full neural signal spectrum (single units and LFPs) is captured. The dynamic range is improved by atleast 12.6dB, and our front-end introduces tolerance to 700mV_{pp} common-mode interferers. From Table 7, we also see that the requirements for a closed-loop neural recording front-end outlined in chapter 3 (Table 1) have been achieved.

From Table 7, we see that due to the large number of performance specifications, it is difficult to make fair comparisons of various front-end implementations. This is because researchers customize the performance of their recording front-ends based on their unique requirements, leading to different specifications. However, a normalized comparison can be made to evaluate the performance of the front-ends. We use FOM₁, as defined in chapter 7 (equation (23)), which combines the trade-offs between power consumption, bandwidth, noise and distortion. Table 7 compares the FOMs of the state-of-the-art recording front-ends. Our proposed front-end achieves an FOM of 166.4dB, which is atleast 16.8dB higher than the state-of-the-art. From equation (23), we see that a 16.8dB higher FOM corresponds to a 48x reduction in power consumption, if all other performance specifications are identical.

The front-end presented above consists of the CCIA and the CT ΔΣ-ADC. As mentioned before, the proposed ADC could also be used as a stand-alone sensing front-end for many applications. This approach is discussed in the appendix.
CHAPTER 9

Conclusion

In this work, a neural recording front-end is presented that can faithfully digitize the (small) neural signals of interest in the presence of large in-band differential and common-mode stimulation artifacts. Apart from immunity to artifacts, this work also presents solutions to several challenges encountered in the design of neural recording front-ends: boosting the input-impedance of chopper amplifiers, realizing reliable very-low frequency high-pass corners in a small silicon area, attenuating the output ripples in chopper amplifiers, and realizing a very-low power high-resolution ADC with minimal loading on the ADC driver. By addressing all these problems in a single unified design, this work stands apart from other neural recording front-ends by meeting all the requirements outlined in Table 2 (Chapter 4). Extensive measurements using fabricated prototypes of the neural recording front-end, along with accompanying analyses that predict the measured results, are offered as evidence to support our claims. In-vitro measurements using electrodes dipped in Phosphate-Buffered Saline (PBS) are also shown to mimic the environment and the interface of realistic neural recording applications.

The specific contributions of this work are summarized below.

9.1 Research contributions

- A new input impedance boosting technique is presented for chopper amplifiers: the *chopped auxiliary path*. This technique enables our front-end to achieve a DC input impedance of 1.5GΩ, which is 24.2x higher than state-of-the-art chopped front-ends. Unlike the “positive-
feedback” technique, the auxiliary path has no stability problems and it can be used simultaneously with the DC-Servo loop. The power consumption and noise contribution of the chopped auxiliary path are shown to be a small fraction of the power and noise of the complete front-end, respectively. Also, the large DC input-impedance of 1.5GΩ was achieved for a relatively high chopping frequency (compared to prior art) of 25kHz without using any off-chip components, which ensures that the front-end can process the complete neural signal spectrum (up to 5kHz).

- A new technique is presented for the reliable realization of analog filters with very-low corner frequencies in a small silicon area without using nonlinear elements: The Multi-rate Duty-Cycled Resistor (MDCR). In this work, the MDCR realizes an equivalent resistance of 90GΩ by using a 350kΩ passive poly-resistor, which corresponds to a resistance amplification of 2.57x10^5. This equivalent resistance is used in the DC-Servo Loop integrator to realize the required high-pass signal transfer function (0.1Hz HP corner) in the recording front-end, enabling the attenuation of large electrode-offsets. The large resistance amplification also leads to a compact area. Apart from the Servo-Loop integrator, the MDCR is also used as a biasing resistor to set the DC bias at various nodes in the recording front-end, with minimal contribution to the input-referred noise. Since the MDCR uses linear elements (passive resistors, MOM capacitors and switches), it does not degrade the linearity of the recording front-end, unlike the “pseudo-resistor” used in prior art. Also, the equivalent resistance realized by the MDCR is significantly less sensitive to process and temperature variations (~ ±35%) as compared to the “pseudo-resistor” (~ 100x).
• A simple technique is presented to increase the recording front-end’s tolerance to large in-band common-mode artifacts: The Common-Mode Cancellation (CMC) path. This technique significantly reduces the distortion of the recording front-end for large common-mode inputs (up to 700mV<sub>pp</sub>), thus enabling the recording of neural signals in the presence of stimulation artifacts. A design methodology has been presented to minimize the noise degradation due to the CMC path.

• A simple ripple-rejection technique for chopper amplifiers is presented in this work. This technique only requires a small ac-coupling capacitance and an MDCR, as compared to conventional ripple-rejection loops that require complicated active blocks like switched-capacitor integrators.

• A modified loop-filter is shown to reduce power consumption in CT-ΔΣ ADCs. This loop-filter also reduces the loading seen by the ADC-driver and the reference-buffer in the feedback DAC, further reducing power consumption in the recording front-end. A linearization technique, duty-cycled source-degeneration, is also presented to linearize the loop-filter without degrading the noise performance.

• Linearization techniques are presented for chopped CT-ΔΣ ADCs: the feedback-DAC reference buffer assistance using an on-chip storage capacitance, and dead-band switches at the input of the 1<sup>st</sup> stage in the loop-filter. These techniques reduce the signal swings at the reference-buffer output and the virtual ground of the 1<sup>st</sup> stage in the loop-filter, ensuring that these blocks operate in their linear regions of operation. Using the above two techniques, the
ADC proposed in this work achieves a Schreier FOM that is 6dB higher than the state-of-the-art, which corresponds to a 4x reduction in power consumption.

9.2 Future work

This dissertation presents a viable neural recording front-end that satisfies all requirements for a human-quality implant capable of recording neural signals in the presence of stimulation artifacts. However, additional work is necessary before this front-end is qualified for pre-clinical trials. Also, during the course of this research, it has been suggested by experts in the field that further miniaturization of the front-end is desirable to implement a larger number of recording channels in a small silicon area. Hence, the following areas of research and development are suggested to further advance this work.

- In-vivo measurements should be performed using the fabricated prototype of the 8-channel CCIA. These measurements would reveal (if any) concerns that need to be addressed in future iterations of this work.

- Explore the possibility of time-multiplexing the complete front-end for area-reduction; also consider the general problem of time-interleaving a CT-ΔΣ ADC and the associated inter-symbol interference (ISI). Can the ΔΣ ADC be modified to reduce ISI? Could the ISI be removed by performing equalization in the digital domain? Can this equalizer be realized with low power consumption and area? Could the equalizer be combined with the decimation filter for lower area?
• Although this dissertation has addressed the difficult problem of realizing a high dynamic-range front-end while meeting the strict power constraints, a significant number of neural recording applications do not require a high dynamic-range. Even in closed-loop recording applications, where the recorded signal is contaminated by large stimulation artifacts, stimulation may be performed only for short periods of time. Hence, over the course of recording, the high dynamic-range requirement is only necessary for the short durations when stimulation is enabled. Thus, power consumption could be reduced by reducing the dynamic-range of the front-end when stimulation is disabled. This requires that the front-end be programmable to trade off dynamic-range for power. The proposed front-end already contains all the necessary building blocks for a lower dynamic-range front-end. Hence for future iterations, the front-end should have the flexibility to alternate between a high dynamic-range and a low dynamic-range for greater power efficiency.

• Explore options for artifact rejection in the digital domain, including considerations for efficient and low-power IC implementations for real-time artifact rejection.

• Could artifact cancellation be performed in the analog domain to reduce the ENOB requirement of the ADC? Would this approach reduce the power consumption of the front-end? Consider the convergence times of any adaptive cancellation loops.

• In a future iteration of this work, a larger number of recording channels (eg: 32) should be implemented on a single IC, along with auxiliary blocks (LDOs, XO circuitry etc). A 32-channel neural sensing IC can be easily integrated on to a palm-sized PCB along with an FPGA
and a USB controller, which can be used to perform in-vivo measurements to verify performance. Such a system could be used to validate this work in a clinical setting, before committing to the development of the implant.
APPENDIX

In chapter 5, we proposed an architecture for an implantable neural recording front-end, consisting of a low-gain (8x) electrode-interfacing amplifier (the CCIA), and a high-resolution CT ΔΣ-ADC. The CCIA provided signal amplification to ease the requirements of subsequent stages, while meeting all the necessary electrode-interface requirements for a human-quality artifact-tolerant implantable neural recording system. Specifically, the CCIA realizes a 1.5GΩ input impedance, rejects ±100mV electrode offsets, achieves a linear input range of 200mV_{pp} and provides immunity to 700mV_{pp} in-band common-mode interference.

However, there are many signal-sensing applications that have relaxed requirements for the input impedance and tolerance to large CM interference. For such applications, the CT ΔΣ-ADC proposed in chapter 7 can be used as a stand-alone recording front-end, as shown in Figure A1. In this section, we present performance comparisons when the proposed CT ΔΣ-ADC is used as a sensing front-end. Suitable modifications to the ADC are also suggested to compensate for the performance limitations due to the omission of the CCIA.

Figure A1. A direct-digitization front-end using the CT ΔΣ-ADC proposed in chapter 7.
A.1 Direct-digitization using the proposed CT-ΔΣ ADC

Table A1 presents the performance of the CT ΔΣ-ADC proposed in chapter 7, when used as a direct-digitization front-end. Comparisons are made to state-of-the-art high dynamic-range sensing front-ends. The proposed ADC, when used as a sensing front-end, provides substantial improvements to the dynamic range for comparable power consumption, noise and area. The linear input range is improved to $1.77V_{pp}$, which is 25dB larger than the state-of-the-art. The SNDR is improved by 31dB, which corresponds to an additional 4.9 bits compared to the state-of-the-art. The FOM (using peak SNDR) is improved by 32.9dB compared to the state-of-the-art.

<table>
<thead>
<tr>
<th>Spec</th>
<th>[97] TBCAS’16</th>
<th>[98] TBCAS’17</th>
<th>[32] VLSI’17</th>
<th>[40] JSSC’17</th>
<th>This work CT ΔΣ-ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power(µW) / Sup(V)</td>
<td>5.5 / 1.5</td>
<td>9.5 / 1.8, 0.9</td>
<td>8 / 1</td>
<td>7 / 1.2, 0.45</td>
<td>4.5 / 1.2</td>
</tr>
<tr>
<td>Peak Input ($V_{pp}$)</td>
<td>4m</td>
<td>10m</td>
<td>23.2m</td>
<td>100m</td>
<td>1.77</td>
</tr>
<tr>
<td>THD @ peak input (dB)</td>
<td>-72.4</td>
<td>-61</td>
<td>-73.6</td>
<td>-79</td>
<td>-104 (1kHz input)</td>
</tr>
<tr>
<td>BW(Hz)</td>
<td>0.25 to 250</td>
<td>0.3 to 7k</td>
<td>DC to 500</td>
<td>0.1 to 200</td>
<td>0.1 to 200</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>58.5</td>
<td>56</td>
<td>70.6</td>
<td>LFP: 75</td>
<td>106</td>
</tr>
<tr>
<td>Inp. ref. noise (µV rms)</td>
<td>1.58</td>
<td>4.57</td>
<td>1.7</td>
<td>LFP: 5.2</td>
<td>2.4</td>
</tr>
<tr>
<td>FOM S, SNDR (dB)</td>
<td>135.1</td>
<td>144.7</td>
<td>148.5</td>
<td>149.6</td>
<td>182.5</td>
</tr>
<tr>
<td>Area (mm²) / Tech (nm)</td>
<td>0.11 / 180</td>
<td>N.A. / 180</td>
<td>N.A. / 180HV</td>
<td>0.135 / 40</td>
<td>0.053 / 40</td>
</tr>
<tr>
<td>$Z_{in, DC}$ (MΩ)</td>
<td>62</td>
<td>∞</td>
<td>30</td>
<td>∞</td>
<td>20</td>
</tr>
</tbody>
</table>

Table A1. Comparison of sensing front-ends with the proposed CT ΔΣ-ADC as a direct-digitization front-end.

The above-mentioned front-end has the following limitations. The input impedance is limited to 20MΩ, due to the switched-capacitor resistance presented by the chopped input-stage of the ADC. The input-referred noise of the ADC in the full signal band (0.1Hz to 5kHz) is 12µVrms,
which may be too large for some recording applications. Also, there is no explicit offset-filtering implemented in the proposed ADC, since the electrode-offset was filtered out by the CCIA (Figure 98). However, since the linear input range of the ADC is 1.77V_{pp}, an input offset of 100-200mV can be easily absorbed by the ADC, obviating the need for an explicit offset cancellation in the ADC. Alternately, the offset-cancellation can be implemented as a digital servo-loop, similar to the analog servo-loop shown in Figure 10(a). The servo-loop integrator can be implemented as a digital IIR filter, and the integrator’s output can be subtracted from the virtual-ground of the capacitive-feedback gain-stage through the feedback-DAC of the CT ΔΣ-ADC.

The input impedance can be improved by employing the chopped auxiliary-path, as discussed in section 6.3. However, since the peak signal swing at the input of the ADC is large (1.77V_{pp}), the buffers used in the auxiliary-path would create significant distortion components, degrading the performance of the ADC. An alternative would be to use a lower chopping frequency in the first stage of the ADC. As discussed in section 7.5.3, the chopping frequency in the CT ΔΣ-ADC must be a multiple of 0.5f_s to avoid aliasing of quantization noise, where f_s is the sampling frequency of the CT ΔΣ-ADC. This constraint limits the minimum chopping frequency to 0.5f_s. However, a lower chopping frequency can be used by modifying the implementation of chopping in the CT ΔΣ-ADC. This approach, along with the corresponding penalty in power consumption, is discussed in the next section.
A.2 Digital demodulation for higher $Z_{in}$ and to avoid noise-aliasing in chopped CT-$\Delta \Sigma$ ADCs

Since the neural signals of interest occupy very-low frequency bands (1Hz to 5kHz), the flicker noise of the ADC must be addressed. As discussed in section 7.5.2, chopping could provide a viable solution to mitigate flicker noise. The problem of chopping-induced noise aliasing is also discussed in section 7.5.2. It was determined [77] that chopping the shaped quantization noise in the analog domain leads to noise-aliasing, as shown in Figure 78. To avoid this problem, the demodulation operation (corresponding to mixer $M_2$ in Figure 78) can be performed in the digital domain. This idea is shown in Figure A2.

![Figure A2](image_url)

**Figure A2.** An alternate implementation of chopping in $\Delta \Sigma$-ADCs.

Since chopping-induced noise-aliasing is prevented, $f_{ch}$ can be much smaller than $0.5f_S$. Hence, the problems associated with a high chopping frequency (reduced input impedance, and other issues discussed in section 7.5.3) could be avoided. However, the following analysis shows that
the ADC implementation shown in Figure A2 would require a significant increase in power consumption compared to the ADC shown in chapter 7.

When chopping is implemented as shown in Figure 78, the mixer conversion gain is very close to unity due to the high bandwidth of the stage “A”. This ensures that there is no SNR degradation due to a conversion loss in the mixer.

**Figure A3.** Frequency-domain analysis of the signal and noise paths (refer to Figure A1).

However, when chopping is implemented as shown in Figure A2, the decimation filter (LPF₁) attenuates the signal power at the harmonics of f\(_{ch}\). Hence, when demodulation is performed in the digital domain, the signal power only around f\(_{ch}\) is restored to baseband. This leads to a conversion
gain of $G_C = 2(2/\pi)^2 \approx 0.8$. Figure A3 illustrates this problem. The signal is assumed to have an r.m.s. value of $A_0$, and the in-band noise spectral density of the ADC is $N_0$. Hence, the SNR at the output of the ADC (after demodulation) is given by

$$\text{SNR} = \frac{(G_C A_0)^2}{N_0 G_C} = G_C \left( \frac{A_0^2}{N_0} \right)$$

By performing filtering before demodulation, the SNR has scaled by $G_C \approx 0.8$. The in-band noise of the ADC is dominated by thermal noise of the loop-filter and feedback-DAC reference buffer. Hence, to compensate for the reduced SNR, the power consumption of the ADC’s analog blocks must increase by $1/G_C \approx 1.23$.

**Figure A4.** Signal bandwidth requirements for chopping (here, $f_{ch} = 3f_{bw}$).

Another drawback of implementing chopping as shown in Figure A2 is the requirement of higher signal bandwidth. Referring to Figure A4, the ADC is now digitizing the up-modulated version of $V_{in}$. To ensure sufficient separation of the signal of interest and the ADC’s flicker noise, the chopping frequency $f_{ch}$ should be $3f_{bw}$, where $f_{bw}$ is the bandwidth of $V_{in}$. Thus, from Figure
A4, the signal bandwidth requirement has increased by a factor of 4. This requires a 4x increase in the ADC sampling frequency $f_S$, to ensure that the noise transfer function (NTF_1 in Figure A4) provides sufficient attenuation to the coarse quantizer’s noise. However, by optimally placing the zeros of the NTF, a better NTF (labeled NTF_2 in Figure A4) can be realized. Hence by using NTF_2, the ADC sampling frequency needs to be increase by 2x instead of 4x. Thus, all the digital blocks of the ADC must operate at twice the frequency, requiring double the power consumption.

Hence, from the above analysis, we determine that if chopping is implemented as shown in Figure A2, then the analog power consumption of the ADC increases by 1.23x, and the digital power consumption of the ADC increases by 2x. The contributions to the ADC power consumption (proposed in chapter 7) are shown in Figure 96. Applying the above-mentioned penalties, the analog power increases from 3.36µW to 4.13µW, and the digital power increases from 1.1µW to 2.2µW. Thus, the total power consumption of the ADC increases by 41% from 4.5µW to 6.33µW.

In contrast, the techniques introduced in section 7.5.3 to improve the linearity of the ADC have a negligible contribution to the ADC power. The additional power consumption corresponds to the driving power of the dead-band switches and the switches used in the reference-buffer assistance. This additional power would be about 50-100nW, which is much smaller than the additional 1.83µW that is required to implement chopping as shown in Figure A2.

Hence, for a 41% increase in the ADC power consumption, the chopping frequency can be reduced from $0.5f_S = 200kHz$, to $3f_{bw} = 15kHz$. This corresponds to a 13.3x reduction in the chopping frequency, which results in an increase in the ADC’s input impedance from $20M\Omega$ to $267M\Omega$. Such a high input impedance would be sufficient for many sensing applications.
The proposed CT $\Delta \Sigma$-ADC, with a reduced chopping frequency of 15kHz, is compared with state-of-the-art sensing front-ends in Table A2. Using the measured performance of the ADC (Table 6 and Table A1), and the power penalties associated with digital demodulation (Figure A2), the performance of the proposed CT $\Delta \Sigma$-ADC with a reduced chopping frequency of 15kHz can be accurately extrapolated. Table A2 shows that the proposed CT $\Delta \Sigma$-ADC (with reduced $f_{ch}$) achieves 25dB higher linear input range, 31dB higher SNDR, and 31.4dB higher FOM as compared to the current state-of-the-art. By reducing the chopping frequency, the input impedance of the proposed ADC is 267M$\Omega$, which would suffice for many sensing applications. Thus, in this section, modifications to the CT $\Delta \Sigma$-ADC are presented, that enable a higher input impedance for a reasonable increase in power consumption.

<table>
<thead>
<tr>
<th>Spec</th>
<th>[97] TBCAS’16</th>
<th>[98] TBCAS’17</th>
<th>[32] VLSI’17</th>
<th>[40] JSSC’17</th>
<th>This work CT $\Delta \Sigma$-ADC, reduced $f_{ch}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power(µW) / Sup(V)</td>
<td>5.5 / 1.5</td>
<td>9.5 / 1.8, 0.9</td>
<td>8 / 1</td>
<td>7 / 1.2, 0.45</td>
<td>6.33 / 1.2</td>
</tr>
<tr>
<td>Peak Input ($V_{pp}$)</td>
<td>4m</td>
<td>10m</td>
<td>23.2m</td>
<td>100m</td>
<td>1.77</td>
</tr>
<tr>
<td>THD @ peak input (dB)</td>
<td>−72.4</td>
<td>−61</td>
<td>−73.6</td>
<td>−79</td>
<td>−104 (1kHz input)</td>
</tr>
<tr>
<td>BW(Hz)</td>
<td>0.25 to 250</td>
<td>0.3 to 7k</td>
<td>DC to 500</td>
<td>0.1 to 200</td>
<td>0.1 to 200 / 0.1 to 5k</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>58.5</td>
<td>56</td>
<td>70.6</td>
<td>LFP: 75</td>
<td>106</td>
</tr>
<tr>
<td>Inp. ref. noise ($\mu V_{rm}$)</td>
<td>1.58</td>
<td>4.57</td>
<td>1.7</td>
<td>LFP: 5.2</td>
<td>2.4</td>
</tr>
<tr>
<td>FOM$_{SNDR}$ (dB)</td>
<td>135.1</td>
<td>144.7</td>
<td>148.5</td>
<td>149.6</td>
<td>181</td>
</tr>
<tr>
<td>Area (mm$^2$) / Tech (nm)</td>
<td>0.11 / 180</td>
<td>N.A. / 180</td>
<td>N.A. / 180HV</td>
<td>0.135 / 40</td>
<td>0.053 / 40</td>
</tr>
<tr>
<td>$Z_{m,DC}$ ($M\Omega$)</td>
<td>62</td>
<td>∞</td>
<td>30</td>
<td>∞</td>
<td>267</td>
</tr>
</tbody>
</table>

**Table A2.** Comparison of sensing front-ends with the proposed CT $\Delta \Sigma$-ADC as a direct-digitization front-end, with a reduced chopping frequency of 15kHz.
From Table A2, we see that the proposed CT ΔΣ-ADC with reduced $f_{ch}$, when used as a direct-digitization front-end, significantly outperforms the current-state-of-the-art. However, the input-referred noise in 0.1Hz to 5kHz is 12μVrms, which may be too large for certain sensing applications. In the next section, a simple modification to the proposed CT ΔΣ-ADC is suggested, which reduces the input-referred noise while also reducing the linear input range.

**A.3 Direct-digitization using the proposed CT-ΔΣ ADC, with reduced input-referred noise**

The input-referred noise of the CT ΔΣ-ADC proposed in chapter 7 is dominated by the thermal noise of the capacitive-feedback gain stage and the feedback-DAC reference buffer (Figure 86). The noise contribution can be reduced by reducing the size of the unit-cap, $C_u$, used in the feedback-DAC (Figure 84). The total capacitance of the feedback-DAC loads the feedback network in the gain-stage, thus reducing the feedback factor. Reducing $C_u$ leads to reduced loading of the feedback network, thus reducing the input-referred noise. This analysis is discussed in detail in [13] and [28]. If $C_u$ is reduced from 2fF to 0.5fF, the input-referred noise of the ADC reduces by 3.5dB. However, this also reduces the linear input range by a factor of 4. The modified gain-stage, along with a reduced chopping frequency (discussed in section A.2), is shown in Figure A5.

Table A3 presents the performance of the CT ΔΣ-ADC as a direct-digitization front-end, with reduced noise and a reduced chopping frequency of 15kHz. Using the measured performance of the ADC (Table 6 and Table A1), and the power penalties associated with digital demodulation (Figure A2), the performance of the proposed CT ΔΣ-ADC with a reduced chopping frequency of
15kHz can be accurately extrapolated. The table also makes comparisons with the state-of-the-art in sensing front-ends.

The proposed ADC achieves 12.9dB higher linear input range, 24.7dB higher SNDR, and 25.1dB higher FOM as compared to the state-of-the-art. The input-referred noise in 0.1Hz to 5kHz is 8µVrms, and the input impedance is 267MΩ, which would suffice for many sensing applications.
Thus, in this section, we presented a simple modification to the CT ΔΣ-ADC, that traded off linear input range for a lower input-referred noise.

| Spec | [97] TBCAS'16 | [98] TBCAS'17 | [32] VLSI'17 | [40] JSSC'17 | This work
| CT ΔΣ-ADC Reduced noise and $f_{ch}$ |
|---|---|---|---|---|---|
| Power(µW) / Sup(V) | 5.5 / 1.5 | 9.5 / 1.8, 0.9 | 8 / 1 | 7 / 1.2, 0.45 | 6.33 / 1.2 |
| Peak Input ($V_{pp}$) | 4m | 10m | 23.2m | 100m | 440m |
| THD @ peak input (dB) | -72.4 | -61 | -73.6 | -79 | < -104 (1kHz input) |
| BW(Hz) | 0.25 to 250 | 0.3 to 7k | DC to 500 | 0.1 to 200 | 0.1 to 200 |
| Peak SNDR | 58.5 | 56 | 70.6 | LFP: 75 | 99.7 |
| Inp. ref. noise ($µV_{rms}$) | 1.58 | 4.57 | 1.7 | LFP: 5.2 | 1.6 |
| $FOM_{S,SNDR}$ (dB) | 135.1 | 144.7 | 148.5 | 149.6 | 174.7 |
| Area (mm²) / Tech (nm) | 0.11 / 180 | N.A. / 180 | N.A. / 180HV | 0.135 / 40 | 0.053 / 40 |
| $Z_{in,DC}$ (MΩ) | 62 | ∞ | 30 | ∞ | 267 |

**Table A3.** Comparison of sensing front-ends with the proposed CT ΔΣ-ADC as a direct-digitization front-end, with reduced noise and a reduced chopping frequency of 15kHz.

To improve tolerance to large in-band common-mode interference, the Common-Mode Cancellation (CMC) path, presented in section 6.2, can be employed in the capacitive-feedback gain stage shown in Figure A5. However, the performance of the ADC with the CMC path cannot be easily extrapolated; hence CM tolerance is excluded from Table A3.

The auxiliary-path can also be used in the capacitive-feedback gain stage to boost the input impedance of the ADC. However, the auxiliary path would increase distortion, and requires
additional power. Since this was not implemented in the fabricated prototype, we refrain from making comparisons in Table A4.

In the above sections, simple modifications have been proposed to the CT ΔΣ-ADC presented in chapter 7. Using these modifications, the proposed CT ΔΣ-ADC can be used as a direct-digitization front-end in applications that do not require a very-high (~GΩ) input impedance. Tables A1-A3 compare the proposed CT ΔΣ-ADCs with the state-of-the-art sensing front-ends, and we see substantial improvements in the linear input range, peak SNDR and the FOM. Based on the requirements of a specific sensing application, an appropriate combination of techniques can be used along with the proposed CT ΔΣ-ADC.
REFERENCES


[71] S. Pawan, “VLSI Data Conversion Circuits,” VLSI group, Indian Institute of Technology, Madras, video lectures (http://nptel.ac.in/courses/117106034/).


