Impact of Transport Anisotropy on the Performance of van der Waals Materials-Based Electron Devices

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***Abstract*— Layered van der Waals (vdW) semiconductors have emerged as preferred materials for building next-generation electronic devices, such as diodes and field-effect transistors (FETs), because of their capability of providing high mobility at the nanometer-scale thickness, as well as their flexibility and pristine interfaces. However, the inherent "vdW gaps" in these materials lead to much larger cross-plane resistivity, with respect to in-plane resistivity, thereby forming intriguing transport anisotropy. In this article, using extensive numerical simulations, it is found that this anisotropy introduces anomalous current transport behavior in vdW-based electron devices in which the current conducts in both the in-plane and cross-plane directions, including stacked heterojunction diodes and thin-film transistors (TFTs). Our study reveals for the first time that transport anisotropy degrades the performance of these devices, especially when devices are scaled (<0.6 μm) and/or relatively thicker materials (>4 nm) are used. Potential solutions to alleviate degradation are discussed as well.**

***Index Terms*— 2-D materials, diode, display electronics, edge-contact, field-effect transistors (FETs), intercalation doping, mobility, thin-film transistors (TFTs), transport anisotropy, van der Waals (vdW) materials.**

I. Introduction

THE discovery of 2-D van der Waals (vdW) materials [1] in 2004/2005 opened a new world not only to physicists, but also to semiconductor device engineers who are seeking new materials for improving the performance of existing device concepts, such as MOSFETs [2]–[4], thin-film transistors (TFTs) [5], or enabling new devices that are not feasible with conventional semiconductors, such as stacked heterojunction diodes (SH-Diodes) [6]–[8], vdW-channel tunnel field-effect transistors (FETs) [9], and so on. The strong hexagonal lattice, pristine surface, and atomic-scale thinness offer 2-D vdW materials interesting physical properties [10] that are desired in many electron device applications, and have received extensive studies [11]. In fact, the unique feature of vdW semiconductors, with respect to conventional semiconductors, is the transport anisotropy induced by the vdW gap between adjacent layers. This transport anisotropy in bulk vdW materials (such as graphite) has been known and characterized half a century ago [12], [13]. Specifically, the cross-plane resistivity ($\rho_{\perp}$) is much larger than the in-plane resistivity ($\rho_{//}$), as illustrated in Fig. 1(a). Density-functional-theory (DFT) calculations (using QuantumWise-ATK) show that the electron density in the vdW gaps is very low [Fig. 1(b)], and moreover, the energy dispersion ($E-k$ relation) along the cross-plane direction is very "flat" [Fig. 1(c)], indicating an extremely low cross-plane carrier velocity ($v = \hbar^{-1} dE/dk$), which explains the physical origin of this anisotropy. Fig. 1(d) collects the in-plane and cross-plane resistivities for several typical vdW semiconductors from the literature [12], [13]. As shown, the anisotropy can be as large as 200 for MoS_2 at room temperature. Apparently, such a large anisotropy will very likely change the device behavior, and thus, needs extensive investigation. Das and Appenzeller [14] performed an experimental study, aided by a simple resistor network model, to roughly estimate the current path in vdW material-based back-gated transistors (a common structure for TFTs), which provides valuable insights and preliminary information, but remains far from delivering the full picture of this effect correctly and accurately. In this article, rigorous numerical simulations are performed to quantitatively capture the effect of transport anisotropy on the performance of typical electronic devices that employ multilayer vdW materials, including TFTs and novel SH-Diodes, in a comprehensive manner. The obtained results are beneficial in elucidating the misunderstandings on the behavior and design of multilayer vdW material-based electron devices in the 2-D electronics community, as well as providing promising solutions for alleviating the harmful effects of transport anisotropy, thereby leading to optimal 2-D electronics design.

Manuscript received October 26, 2019; revised December 29, 2019; accepted January 15, 2020. Date of current version February 26, 2020. This work was supported in part by the Army Research Office (ARO) under Grant W911NF1810366, in part by the Japan Science and Technology Agency (JST) Core Research for Evolutional Science and Technology (CREST) Program under Grant SB180064, in part by the University of California (UC) Lab Fees Research Program under Grant LFR17-477237, and in part by the Mentor Graphics Corporation. The review of this article was arranged by Editor R. Wang. *(Corresponding author: Kaustav Banerjee.)*

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Digital Object Identifier 10.1109/TED.2020.2970394

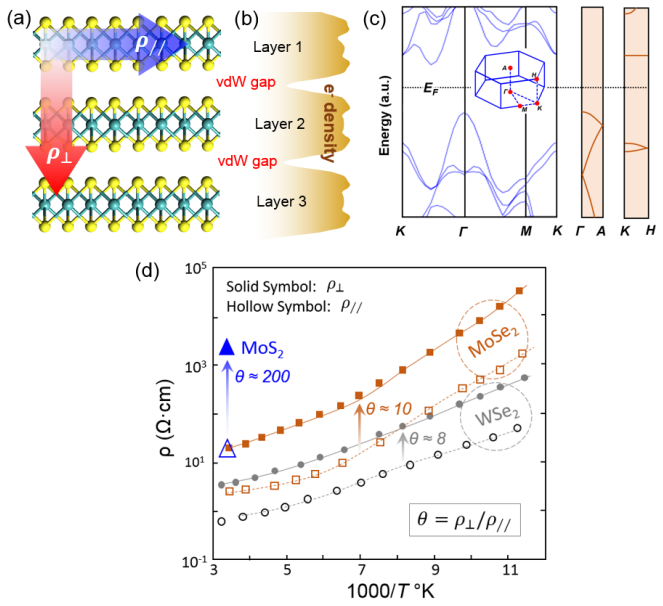

Fig. 1. (a) Appearance of vdW gap between adjacent layers leads to large transport anisotropy, i.e., the large cross-plane resistivity ($\rho_\perp$) with respect to the in-plane resistivity ($\rho_{//}$) in vdW materials. (b) Electron density distribution (DFT results) along the the cross-plane direction. (c) Band structure along cross-plane direction ($\Gamma \leftrightarrow A$ and $K \leftrightarrow H$) is nearly dispersion-less ("flat" E–k curves with energy closest to Fermi level E_F) compared to those along in-plane directions. (d) Experimentally measured resistivity (adapted from [12], [13]) for MoS_2, $MoSe_2$, and WSe_2 shows that the transport anisotropy factor θ (defined to be $\rho_\perp/\rho_{//}$ in isolated and intrinsic vdW materials) has a large range, depending on the material sources and synthesis approach.

II. Methodology

Since the feature sizes of 2-D vdW SH-Diodes and TFTs are relatively large (micrometer level), and the bandgap changes negligibly with the number of 2-D layers in the cases of tri-layer and above [15], drift-diffusion model can adequately capture the carrier transport dynamics, such as carrier velocity/momentum and scattering, and so on. Thus, the drift-diffusion equation and Poisson's equation are solved iteratively to obtain the carrier density and electrostatic potential, respectively, until convergence is reached (see [15] for details). The Schottky barrier width is dependent on bias condition and doping concentration and is obtained from self-consistent simulation. Once the Schottky barrier height and width are known, thermionic and tunneling current can be calculated. The Schottky barrier tunneling current at the metal-to-semiconductor contacts is calculated with the Wentzel–Kramers–Brillouin (WKB) theory [16]. The edge- and top- contacts have only a geometric difference, and no fundamental difference in this simulation.

According to the definition of resistivity, $\rho = (qn\mu)^{-1}$, the anisotropy of resistivity, or resistance, in a biased active device is contributed by two components, the carrier concentration (n) and mobility (μ). It is worth noting that nonuniform carrier concentration induced anisotropy in resistivity is common to all types of semiconductors under biased conditions. Only the anisotropy of mobility is unique and intrinsic to vdW semiconductors. Thus, an anisotropic mobility, instead of a lumped anisotropic resistor [14] that neglects the details of carrier distribution, and thereby introduces a large error, is employed in the simulations in this article. This excludes the contribution of nonuniform carrier concentration, allowing us to accurately study the intrinsic anisotropic transport behavior in vdW devices. More specifically, the transport anisotropy factor θ is defined to be $\theta = \mu_{//}/\mu_\perp$, in our device simulations. Note that the anomalous vertical quantum interference effects, such as the magic angle [17] or Moire's pattern [18], are only observable at extremely low temperatures, which is irrelevant to the normal electron device operation condition. Therefore, such effects are not considered in this article.

III. Analysis of SH-Diodes

An SH-Diode can be made by stacking two oppositely doped vdW semiconductors, e.g., n-doped MoS_2 and p-doped WSe_2, forming a geometrically vertical heterojunction p-n diode, as schematically illustrated in Fig. 2(a). It is worth mentioning that the top contact structure is found to be much worse than the existing edge-contact structure for SH-Diode, and hence, will not be discussed here because of space limitation. Such vertical devices have generated broad interest and have been extensively fabricated with a combination of different n-side and p-side materials, as recently reviewed by Frisenda *et al.* [8]. However, the device physics of such diodes, especially in terms of transport behavior, remains ambiguous. Thus, a comprehensive theoretical investigation is desirable in order to understand and optimize such devices. In the simulations, both n-region and p-region are set to be 4 nm thick and 70 nm long, with 40-nm-long stacking or overlapping region between each other. A Schottky barrier height of 0.2 eV (to account for possible Fermi level pinning between metal and 2-D materials) [19] and [20], and transport anisotropy factor θ of 100 are used in all the simulations if not specified otherwise. The doping level in each vdW layer is set to be 6.5×10^{11} cm^{-2} at both n- and p-sides, which can be achieved through the intercalation doping technique that was introduced to the 2-D materials community by Xu *et al.* [21], [22], and subsequently demonstrated by various groups [23]–[27], and is above the normal doping range of unintentionally doped (defect induced doping only) vdW materials. Fig. 2(b) shows the simulated electrostatic potential in this device at a reverse bias of −0.5 V. It is found that the potential drops primarily in the lateral direction, and the expected vertical potential drop in this vertical p-n diode is negligible. This observation can be explained by the formula of depletion width in a p-n junction [28], versus doping level

$$W_{\text{dep}} = \sqrt{\frac{2\varepsilon_s kT}{q^2}\left(\frac{1}{N_A}+\frac{1}{N_D}\right) ln\left(\frac{N_A N_D}{n_i^2}\right)} \qquad (1)$$

where ε_s, k, T, q, N_A, N_D, and n_i are permittivity of semiconductor, Planck's constant, temperature, elementary charge, acceptor concentration, donor concentration, and intrinsic carrier density, respectively. Assuming $N_A = N_D = N_d$, for the simplicity in the discussion, this formula is reduced to $W_{\text{dep}} \propto (\ln(N_d)/N_d)^{1/2}$, indicating that W_{dep} increases as N_d decreases. For thin-body vdW SH-Diodes, when the N_d is not sufficiently high, W_{dep} will be much larger than the film

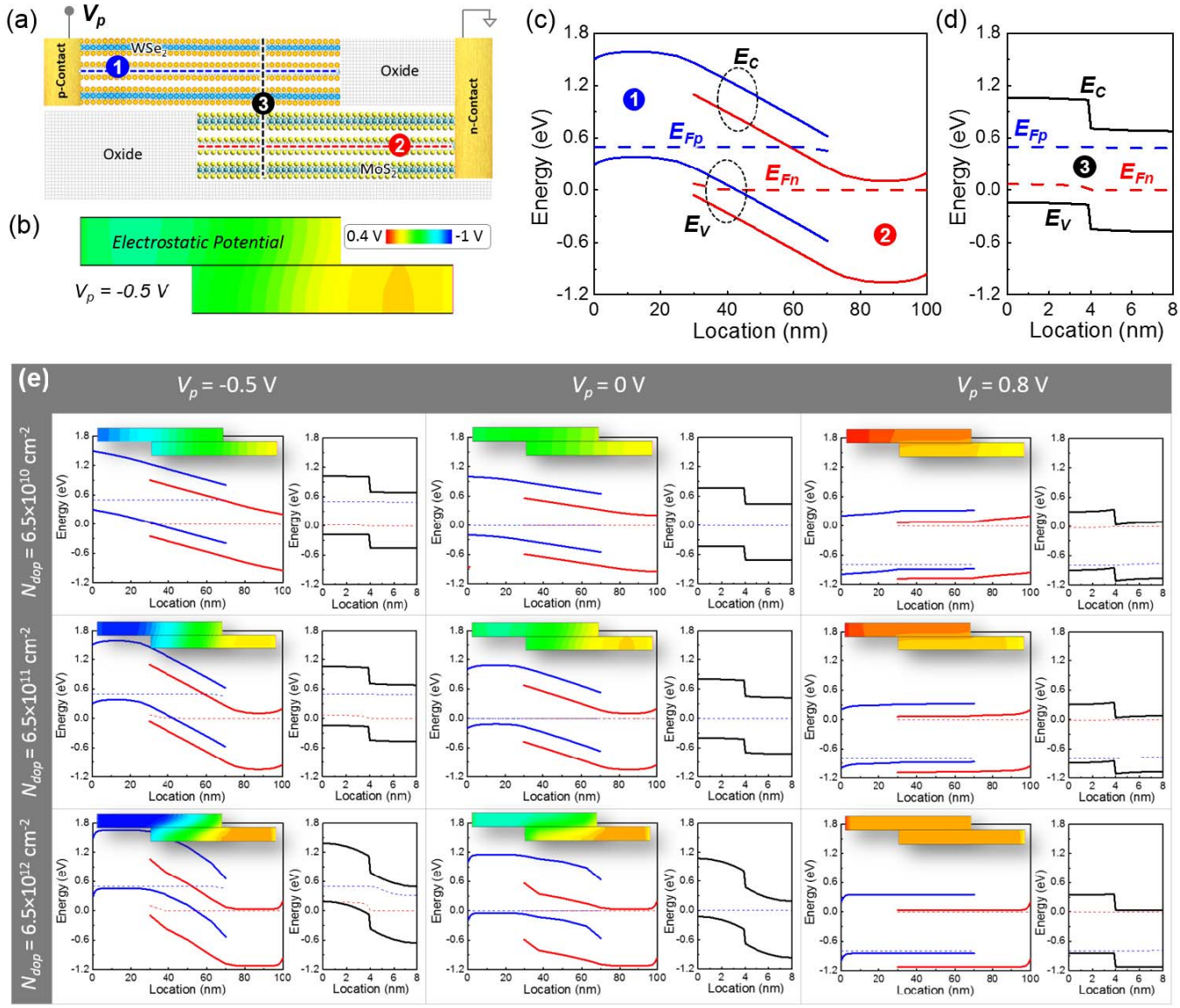

Fig. 2. (a) Schematic of a stacked heterojunction vdW diode with proper n(p)-contacts. The thickness of each material is set to be a typical value of 4 nm or roughly six layers. (b) Simulated electrostatic potential for a doping level of $N_{\text{dop}} = 6.5 \times 10^{11}$ cm^{-2} in each vdW layer. Extracted band diagrams along (c) two in-plane paths #1 and #2 in (a) and along (d) cross-plane path #3 in (a). All the symbols in this figure have their nominal meanings. A Schottky barrier of 0.2 eV is used in the simulation. (e) Band diagrams along the three paths marked in (a) at different doping level N_{dop} and bias V_p. The inset in each subplot (to the left) is the corresponding electrostatic potential contour. The magnitude scale is referenced to the one in (b). The dashed red and blue lines represent the E_{Fn} and E_{Fp}, respectively.

thickness, which makes the potential profile in the vertical direction look very "flat." Fig. 2(c) and (d) shows the band diagrams along the path # 1 and # 2, and path # 3 in Fig. 2(a), respectively. Note that the discontinuities of conduction band minima (E_C) and valence band maxima (E_V) stem from the band offset between MoS_2 and WSe_2. The band diagrams in the stacking region uncover that both n- and p-sides are fully depleted. In other words, this geometrically vertical p-n diode functions as a lateral p-i-n diode at the doping level of 6.5×10^{11} cm^{-2}. To fully understand the device operation mechanism, as well as the role of doping level, band diagrams and electrostatic potentials are studied at various doping levels and applied biases, as shown in Fig. 2(e). At a very low doping level of 6.5×10^{10} cm^{-2} [the first row of Fig. 2(e)], which can represent the condition of undoped good-quality vdW materials, the entire device, including the underlapped region, is fully depleted, as reflected by the nearly linear potential drop (because of low doping and charge carrier concentration, similar to a p-i-n diode [28]) in the lateral direction, ending up with a resistor-like device, instead of an effective p-n diode. It is worth noting that such low-doped resistor-like devices may still provide rectified current–voltage ($I-V$) characteristics, which has been observed in many experiments, as well as in our simulation [see the blue solid line in Fig. 3(a)]. However, the rectified $I-V$ in such devices stems from the Schottky junction at the two asymmetric contacts [see the lateral band diagrams in the turn-on and turn-off conditions in Fig. 2(e)] [29], leading

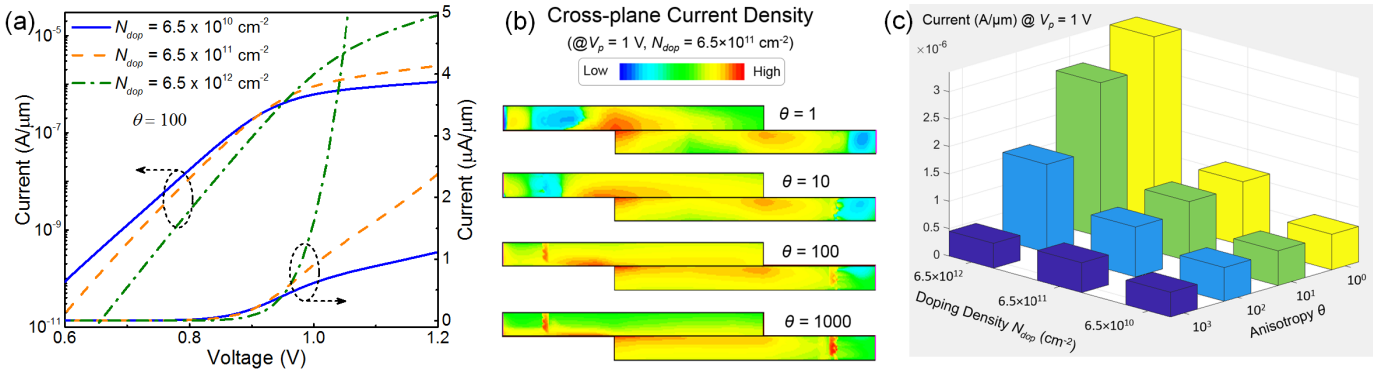

Fig. 3. (a) Simulated current–voltage characteristics of a vdW materials-based SH-Diode at different doping levels. Higher doping increases threshold voltage, but increases the steepness of the turn-on curve and drive current. Low doping suffers from voltage loss in the lateral direction, resulting in inefficient rectifying characteristics. (b) Simulated cross-plane current density versus the anisotropy θ. With low anisotropy, the current injects primarily at the edge, while with high anisotropy, current tends to spread to the overlapped region for more injection area. (c) Drive current (at $V_p = 1$ V, in the above-threshold regime) versus doping density and anisotropy θ.

to poor rectifying efficiency compared to the highly doped devices [see Fig. 3(a)]. When the doping level increases to 6.5×10^{11} cm^{-2} [the second row of Fig. 2(e)], although the overlapped region is still fully depleted, underlapped regions can stay neutral, i.e., forming a p-i-n diode, which shows much better rectifying efficiency with respect to the resistor-like case in the low doping of 6.5×10^{10} cm^{-2}. When the doping level in vdW materials can increase, if possible, to 6.5×10^{12} cm^{-2} [the third row of Fig. 2(e)], depletion width is significantly reduced, allowing the neutral region to extend to part of the overlapped region, and noticeable potential to drop across the vertical junction. It can be observed that the potential quadratically drops, indicating a trend back to normal diode behavior as the doping level is increased, which is consistent with the improved rectifying efficiency, as shown in Fig. 3(a). However, it is worth noting that even at such a high doping level, part of the overlapped region is still fully depleted, and a noticeable portion of the potential still drops laterally, indicating that these geometrically vertical SH-Diodes are extremely difficult to be made physically "vertical."

As shown in Fig. 1(d), θ has a broad range for different vdW materials, and hence, may lead to different transport behavior. Fig. 3(b) shows the current density distribution in an SH-diode at forward bias condition for different θ. Interestingly, with low anisotropy, the current injects primarily at the edge of the overlapped region, while with high anisotropy, current tends to spread into the overlapped region for more injection area. Fig. 3(c) shows the drive current (at a forward bias of 1 V) versus different doping levels and anisotropy factors. At low doping density (an inefficient resistor-like diode), the effect of θ on drive current is small because the low doping induced large lateral resistance, and hence, lateral voltage loss dominates the performance degradation. However, when doping increases to a very high degree, lateral resistance is significantly reduced, and vertical resistance in the overlapped region dominates the device performance. In other words, the device becomes more like a proper vertical diode, and the effect of transport anisotropy begins to degrade the current appreciably.

IV. Analysis of TFTs

TFTs are widely employed in display electronics because of their simple structure and low manufacturing cost, as well as the much less urgent need in display electronics for ultrascaled devices, compared to very large-scale integration (VLSI) application. Main-stream channel materials of TFTs include amorphous silicon (a-Si), polycrystalline silicon (poly-Si), organic semiconductors, and a metal oxide, such as indium gallium zinc oxide (IGZO), and so on [30]. All these technologies have great challenges or limitations. For example, amorphous silicon (a-Si) and organic semiconductors suffer from low carrier mobility that degrades device performance; the polycrystalline nature of poly-Si introduces device performance variation that is a serious problem for displays; IGZO lacks p-type device that is required to construct complementary periphery circuits for energy-efficient displays. The discovery of the vdW material family provides a new promising option to the TFT community [11], because of their intrinsic thinness, crystalline structure, high mobility, and feasible n-type and p-type operation. Most importantly, TFTs prefer high mobility and low contact resistance, compared to ultimate scalability. Thus multilayer vdW is a much more practical option compared to monolayer vdW. As a result, transport anisotropy is expected to play an important role in such devices. Fig. 4(a) shows the schematic of a typical vdW semiconductor-based TFT with a 70-nm-long, 4-nm-thick channel, and 30-nm-long source/drain top contacts. As shown in Fig. 4(b), the current flows from drain, through the channel surface near the bottom gate dielectric, BOX, (due to the larger carrier concentration there compared to that away from the gate), and then to source, as expected in a normal TFT. Simulated transfer characteristics, i.e., I_d–V_g curves with different anisotropy θ in Fig. 4(c), show that large anisotropy does not affect the subthreshold characteristics, but degrades the ON-current considerably. Fig. 4(d) shows the electron Fermi energy distribution in the channel (other parts not shown) in the turn-on condition for different anisotropy. In the case of large anisotropy θ, a clear Fermi level (or voltage) drop can be observed along the vertical direction under the source electrode, indicating the existence of a large vertical resistance

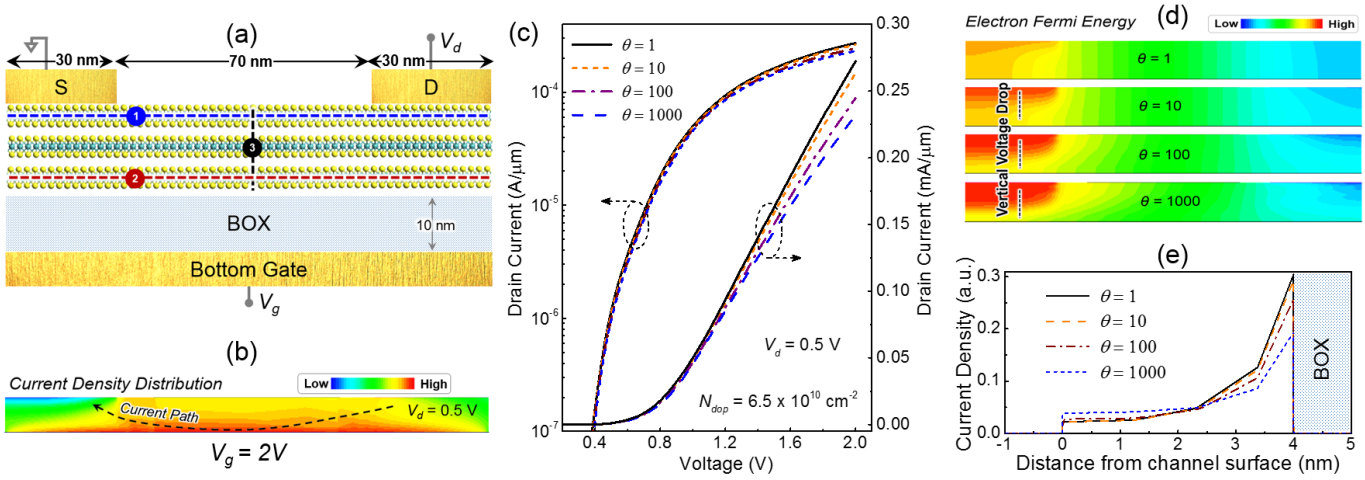

Fig. 4. (a) Device schematic of a typical TFT with a 4-nm-thick and 70-nm-long vdW semiconductor channel. The contact length is set to be 30 nm. A Schottky barrier of 0.2 eV is used in the simulation. (b) Injected current conducts primarily near the bottom gate, i.e., along the path #2 in (a). (c) Simulated transfer characteristics, i.e., I_d–V_g curves with different anisotropy θ. (d) Electron Fermi energy distribution in the channel (other parts of the device are not shown) in the turn-on condition. For the case of large anisotropy θ, a clear Fermi energy drop can be observed under the source electrode, indicating the existence of a large vertical resistance compared to horizontal resistance. (e) Current density distribution at the channel center [at each point of the line #3 in (a)] for different anisotropy θ. Large θ tends to prevent the current from accumulating near the bottom gate.

at least comparable to the lateral resistance. Fig. 4(e) shows the current density distribution at the channel center [at each point of the line #3 in Fig. 4(a)] for different anisotropy. It can be observed that large θ tends to reduce the current density near the bottom gate, and increase the current density away from the gate, which can be attributed to the fact that large θ induced large vertical resistance prevents current being injected from the source toward the bottom gate. The current degradation induced by anisotropy is studied for different channel length and channel thickness, as shown in Fig. 5(a) and (b), respectively. All the currents have been normalized by the maximum current obtained at zero anisotropy, i.e., $\theta = 1$. For the longer channel, e.g., 1.3 μm, 96% of the maximum current can be preserved (for $\theta = 1000$). However, if channel length is reduced to 0.13 μm, the current degradation can reach 15%. This trend presents a serious problem if vdW semiconductors are targeted for the TFTs in the micro-LED technology in which TFTs are expected to be made small (<200 nm). Channel thickness plays an equally important role. In the simulation results in Fig. 5(b), the channel length is fixed to be 0.13 μm. As shown, thicker channels accelerate the anisotropy induced current degradation, which can reach ~50% when channel thickness increases to 16 nm (for $\theta =$ 100). These observations can be explained with a simple lumped resistor network model, as schematically illustrated in Fig. 5(c). The vertical resistance ($R_\perp$) induced by vdW gaps is primarily determined by the channel thickness, while the lateral resistance ($R_{//}$) is roughly proportional to the channel length. At fixed channel thickness (length), reducing channel length (increasing channel thickness) increases the ratio of $R_\perp$ and $R_{//}$, leading to more severe current degradation for large θ.

Fig. 5(d) shows the current density distribution in the channel (other parts not shown) for different channel thicknesses (T_{Ch}). θ is set to be 100. Interestingly, when the channel thickness increases to 12 and 16 nm, additional current path

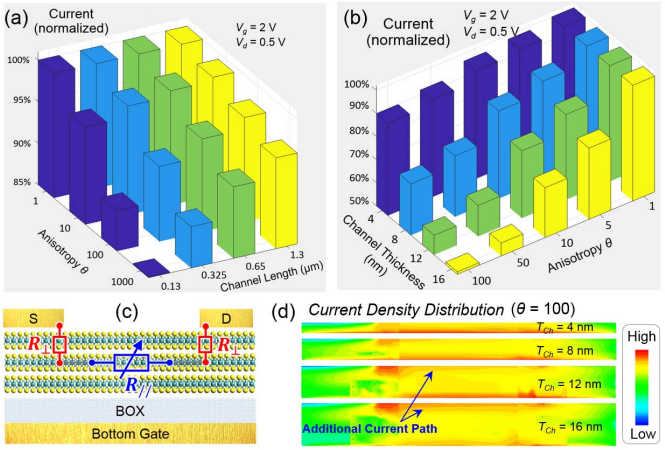

Fig. 5. (a) Current degradation induced by anisotropy θ for different channel lengths. (b) Current degradation induced by anisotropy θ for different channel thicknesses. Note that here the in-plane mobility and contact resistance are assumed to be the same for different channel thicknesses in order to isolate and study the effect of transport anisotropy on the current. These observations can be explained with a simple resistor network, as schematically illustrated in (c). (d) $R_\perp$ in thick channel can be so large that current begins to conduct along the channel top surface, in addition to the normal path near the gate dielectric.

forms near the top surface of the channel, in parallel with the one near the bottom gate. Such an anomalous phenomenon, which should not be expected in a single-gate transistor simply from the band bending perspective, is actually consistent with the results in Fig. 4(e). Briefly speaking, although the carrier concentration near the gate is larger than that at the channel top surface, the large vertical resistance consumes too much drain voltage (V_d) that should have been used to accelerate the carrier along the channel for current conduction. In other words, the carriers at the channel top surface do not suffer from vertical resistance induced large drain voltage loss, and hence, can gain higher velocity compared to that near the gate, thereby forming a comparable current flow near the top

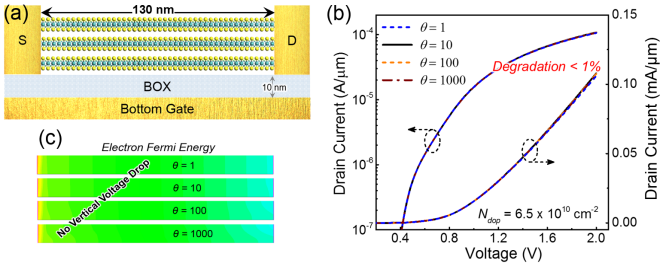

Fig. 6. (a) Schematic of a vdW material-based TFT with edge-contacts. (b) Simulated transfer characteristics show negligible (<1%) performance degradation induced by the transport anisotropy (V_d = 0.5 V). (c) Electron Fermi energy distribution in the channel (other parts not shown) in the turn-on condition. The voltage drop is primarily along lateral direction, indicating that the vertical resistance does not play a major role in this device.

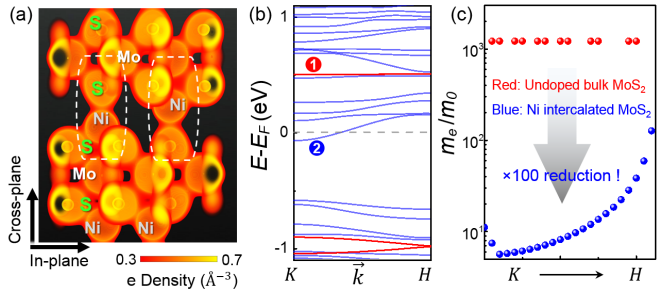

Fig. 7. (a) Side-view of electron density in bulk MoS_2 with Ni intercalants. (b) Band structures of intercalated MoS_2(blue) with respect to undoped MoS_2 (red) along the cross-plane direction. (c) Extracted effective mass of the band closest to the Fermi level [marked with symbol 1 and 2 in (b)], shows that the Ni intercalation reduces the electron effective mass of MoS_2 by 100-folds, indicating a 100-fold increase in carrier velocity in the vertical direction, and hence, significantly reduced transport anisotropy.

surface. Note that the previous resistor network model [14] did not capture this dual-path conduction behavior, primarily due to its over-simplification of carrier distribution in the device.

Based on the mechanism of such transport anisotropy induced current degradation, we propose two potential solutions to suppress this degradation.

The first is edge-contact [31]–[34], as schematically illustrated in Fig. 6(a). In this TFT structure, the current can be laterally injected into the channel near the gate, and hence, large vertical resistance has limited influence on the current flowing path. This postulation is verified by the indistinguishable I_d–V_g curves in Fig. 6(b) and the nearly lateral electron Fermi energy gradient [Fig. 6(c)] in the channel (other parts not shown), in contrast to Fig. 4(c) and (d), respectively.

The other solution could be intercalation doping, which is essentially a process of inserting some foreign molecules in the vdW gap. This approach not only effectively increases the charge carrier density in vdW materials, but can also reduce the vertical resistivity significantly if proper intercalants are selected, and hence, reduce the transport anisotropy, which has been verified in a graphitic system [35]. We performed a DFT simulation (Synopsys QuantumATK) [36] to extract the electron density and band structure along the cross-plane direction. In the simulation, Perdew–Burke–Ernzerhof (PBE) variant of generalized gradient approximation (GGA) is used as the exchange-correlation functional; the DFT-D3 model is activated to include the effect of vdW force; k-point sampling, density mesh cutoff, and maximum force for geometry optimization are set to be 11 × 11 × 3, 180 Rydberg, and 0.05 eV/Å, respectively. It is found that the vdW gap in bulk MoS_2 can be effectively bridged by the additional electrons introduced by Nickel (Ni) intercalants [Fig. 7(a)]. The simulated band structure [Fig. 7(b)] of Ni intercalated MoS_2 (blue lines) along the across-plane direction (K–H), is much more dispersive with respect to that of undoped bulk MoS_2 (red lines). Extracted effective mass [Fig. 7(c)] from the band closest to the Fermi level in Ni-doped MoS_2 is 100-folds lower with respect to that in undoped bulk MoS_2, indicating a ∼100-fold increase in carrier velocity in the cross-plane direction, and hence, leads to 100-folds reduction in transport anisotropy.

It is worth mentioning that simply reducing the layer thickness is not an option. The purpose of Fig. 5(b) is to only illustrate the effect of transport anisotropy and thus neglects several thin channel-related issues such as higher contact resistance, lower density of states (DOS), and lower in-plane mobility. Although thinner channel suffers less from transport anisotropy induced current degradation, the higher contact resistance, lower DOS, and increased scattering that degrade charge carrier mobility can override the benefit of lower transport anisotropy effect and result in a poor current drive. Therefore, there should be an optimal channel thickness for intrinsic van der Waals materials-based semiconductors, as experimentally observed with multilayer MoS_2 FETs [2].

V. Conclusion

This article comprehensively studied the effect of transport anisotropy of vdW semiconductors in commonly employed display electronic devices, such as SH-Diodes and TFTs, which uncovers the unexpected transport behavior in these devices, as well as the degraded device performance. Potential solutions, including intercalation doping with the right intercalates (for both SH-Diodes and TFTs) and edge-contacts (for TFTs), are suggested to alleviate these issues. The methodology developed and analyses presented are equally applicable to a wider range of electron devices that employ multilayer vdW materials.

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