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# Low-Temperature Wafer Bonding for Three-Dimensional Wafer-Scale Integration

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***Abstract*—In this paper, we will report a low-temperature wafer-to-wafer fusion bonding process, whose maximum processing temperature is 300C, and can potentially be further reduced to 250C. This low-temperature process would enhance the compatibility of the three-dimensional wafer-scale integration technology with the devices that might suffer from high-temperature FBEOL processes. Preliminary experiments are done with blanket 300mm wafers, and characterization results from SAM imaging and mechanical shear test are reported to evaluate the feasibility of the low-temperature fusion bonding process.**

***Keywords—wafer bonding, fusion bonding, wafer bond characterization, three-dimensional-wafer-scale-integration.***

## I. Introduction

Three-dimensional wafer-scale integration (3D-WSI) technology [1,2] based on fusion bonding has been studied to enable high-throughput 3D integration. This method uses a via-last process to make very fine-pitch (~1um) vertical interconnect vias for very large-scale systems requiring massive interconnectivity, such as brain-scale cognitive systems [3,4]. Since wafer-level integration technology uses fabricated wafers, one of the challenges is to reduce the thermal budget of the process flow to prevent degradation to the existing devices on the wafers [5]. In addition, high-temperature process will limit the choice of the temporary adhesive to use between the wafer and the handler.

In this work, new process flow is designed to reduce the maximum processing temperature during the fusion bonding process from 400C high-temperature (HT) to 300C low-temperature (LT). Different experimental recipes are used to reduce the temperature of certain processes in the flow, such as oxide deposition and ultraviolet (UV) activation. The experiments are conducted on blanket wafers as a preliminary study to the feasibility of the LT fusion bonding process for the 3D-WSI and other 3D integration technologies.

## II. Low-Temperature Fusion Bonding

This study focuses on the fusion bonding process in the 3D-WSI process flow, which uses a 2-layer CVD-based oxide as the bonding interface (Fig. 1), similar to the previous art [2]. For a fabricated wafer, low-k dielectric (Oxide #1) is deposited, followed by a CMP. The deposited Oxide #1 is then activated by UV curing. On top of the Oxide #1 layer, an adhesion oxide (Oxide #2) layer is deposited, followed UV

Table. 1: processing temperatures of steps in the high-temperature (HT) and low-temperature (LT) wafer bonding process flow

| Process Step (in order) | HT | LT |
|---|---|---|
| Oxide #1 deposition | 400C | 250C |
| 1st UV cure | 385C | 250C |
| Oxide #2 deposition | 200C | 200C |
| 2nd UV cure | 385C | 250C |
| Annealing | 300C | 300C |

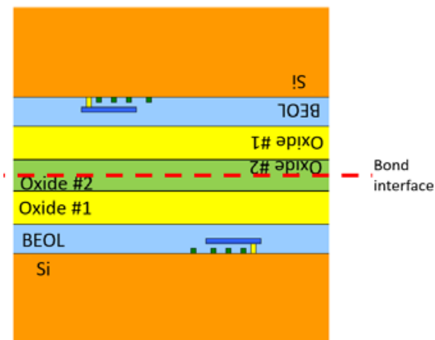


Fig. 1: structure of the fusion bond used in this work (drawing not to scale).

activation. The activated Oxide #2 is then polished by CMP. Fusion bonding uses the Oxide #2 layer as the interface. Depending on which side the adhesion layer is on, face-to-face, face-to-back and back-to-back bonding can be achieved. The bonded wafer stack is then annealed. The key processing temperatures of the HT process (gated by the Oxide #1 deposition temperature) and the LT process (gated by annealing temperature) are listed in Table 1.

From the fusion bond analysis in [2], the Oxide #2 interface contributes to the strong bond strength (i.e. high bond energy from Maszara method [6]), while the Oxide #1 layer serves as the planarizing layer between the Oxide #2 and the Si wafer (with BEOL layers). Therefore, the temperature reduction in the fusion bonding process could affect the bond strength by the following factors:

1. Lowering the processing temperature of Oxide #1 deposition reduces the density of the deposited Oxide #1 layer (checked by wet etch rate from HF dip, see Table 2).

Therefore, the LT Oxide #1 is easier to be planarized during the CMP process, and more flexible during the mechanical deformation of the bonding contact. However, the weaker mechanical strength of the less dense Oxide #1 itself could undermine the mechanical strength of the bond.

2. Lowering the processing temperature for 1st UV cure reduces the cross-linking in the Oxide #1, which has similar effect as reducing the Oxide #1 deposition temperature.

3. Lowering the processing temperature for 2nd UV cure reduces the cross-linking in the Oxide #2 layer, which has similar effect as reducing the Oxide #1 deposition temperature. In addition, the defect regions in the Oxide #2 make it a better bonding interface than Oxide #1 since those defect regions can accommodate the water molecules generated during the interfacial condensation reaction ($\mathrm{Si-OH+Si-OH \rightarrow Si-O-Si+H_2O}$) which forms the bond between the silanol molecules of the top wafer and the bottom wafer. Furthermore, due to the existence of the Oxide #1 below the Oxide #2, reducing the 2nd UV cure temperature will drive fewer volatiles to the Oxide #1/Oxide #2 interface, which might strengthen the bond if the Oxide #1/Oxide #2 interface is the weakest segment of the bond.

Table 2: wet etch rate (WER) of the Oxide #1 layer using the same HF dip (DHF) recipe.

| Oxide #1 deposition temperature | 250C | 280C | 400C |
|---|---|---|---|
| WER (same DHF recipe) | 12.67nm | 8.43nm | 4.26nm |

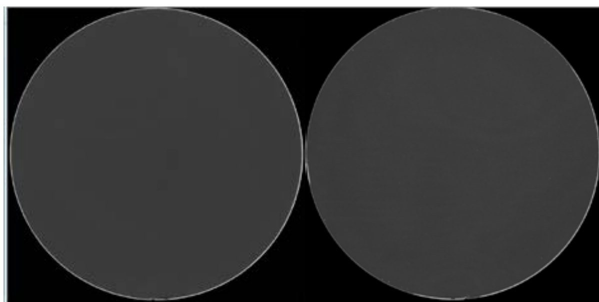

Fig. 2: SAM image of the bonded 300mm wafer using HT process (left) and LT process (right). No significant void is shown in both processes.

## III. Results and Discussion

SAM imaging is done for all bonded samples as a fast and non-destructive method to check for significant bond voids. Fig. 2 shows the typical SAM image of the HT process and the LT process (250C Oxide #1 deposition and both UV cure processes). No significant void is observed in both cases.

To quantitatively measure the strength of the wafer bond from the process, mechanical (destructive) shear test is used. In contrast to the popular Maszara method (blade test), shear test uses dices from the bonded wafer for testing, whose sample can come from any location of the wafer, while blade testing can only be applied at the edge of the wafer.

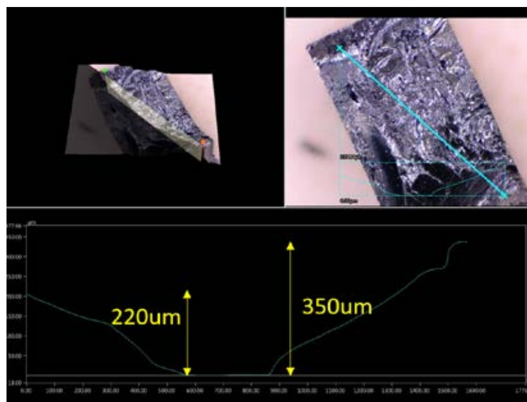


Fig. 3: the cross section profile of the bond sample fractured during the shear test. The fracture (>100um) is much deeper than the thickness of the bond interface (~1um), and therefore the fracture is into the Si.

Destructive Shear Test on (1.75mm)$^2$ Sample

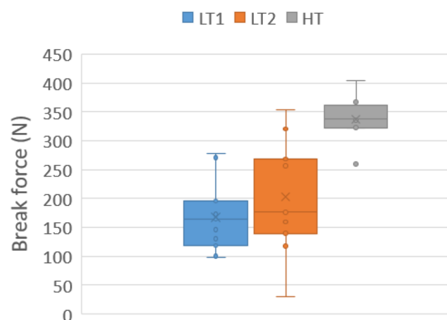


Fig. 4: the break force of the destructive shear test on the 1.75mm x 1.75mm dies from the bonded wafers. HT process shows higher bond strength.

During the shear test on the (1.75mm)$^2$ dies, all samples are broken. However, the samples do not break clearly at the bonding interface (1um oxide layers), and show fractures into the Si as shown in Fig. 3. The force at which the sample is broken is recorded as the break force of the sample for the comparison. As the preliminary result showed in Fig. 4, the samples from two different LT processes (LT1 and LT2) show lower bond strength than the sample from HT process. However, more tests are needed to be done to study the bond strength variation at the different locations of the wafer, and the variation across different lots.

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