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Analysis and Implementation of a Series-Capacitor Zero-Bias Trans-Inductor Voltage Regulator

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***Abstract*—This paper proposes and demonstrates a series-capacitor zero-bias trans-inductor voltage regulator (SC-ZB-TLVR) for data center power delivery applications, along with its i_{L_c}-based control strategy. Compared to conventional series-capacitor buck converters, the interphase magnetic coupling enhances the load-transient response while maintaining small inductor current ripple. DC flux bias in the indirect-coupled inductor cores is canceled through flux injection from the last phase compensation inductor current, enabling reduced core size and improved power density. In this work, we show how the inherent current balancing among phases may not hold under non-ideal magnetic coupling. A phase-shift modulation strategy is proposed to fully remove the DC flux imbalance. The i_{L_c}-based control strategy is proposed and validated in simulation, enabling the use of the current sensing output of DrMOS and greatly reduces the system complexity. Finally, the proposed topology is verified on a 24 V-to-1 V, four-phase, 120 A experimental prototype.**

I. Introduction

Series-capacitor buck (SCB) converters [1] offer significant performance improvements compared to conventional multiphase buck converters due to reduced voltage stress on switches, reduced inductor current ripple, and automatic current sharing [2], making it an appealing choice for high-frequency, high-step-down-ratio applications [3]. Recently, multiple SCB-based topologies have been proposed for point-of-load (PoL) converters in data centers and achieved promising efficiency and power density [4]–[7].

However, both academia and industry have raised concerns regarding the load transient performance of SCB converters. Data center power supplies must respond rapidly to demanding load transients (e.g., over $1\ \mathrm{A/ns}$) while keeping the output voltage overshoot and undershoot within stringent specifications. Due to the duty cycle limit of SCB converters, the output current cannot slew up as fast as conventional solutions such as multiphase buck converters, where the PWM of each phase is overlapped during the transients. The load step-up transient response is therefore sacrificed in SCB converters. Meanwhile, the prevalent control strategy scheme of data center point-of-load converters is current mode constant on-time control (CMCOT) [8], where the high-frequency current ripple signal is a necessity in the current loop control. State-of-the-art integrated power module (e.g., DrMOS) solutions typically offer integrated current sensors. However, it is not possible to adopt off-the-shelf DrMOS in SCB converters due to its lack of half-bridge structure at the output stage. This makes high-bandwidth current sensing extremely difficult for SCB converters, either being lossy, bulky, or costly.

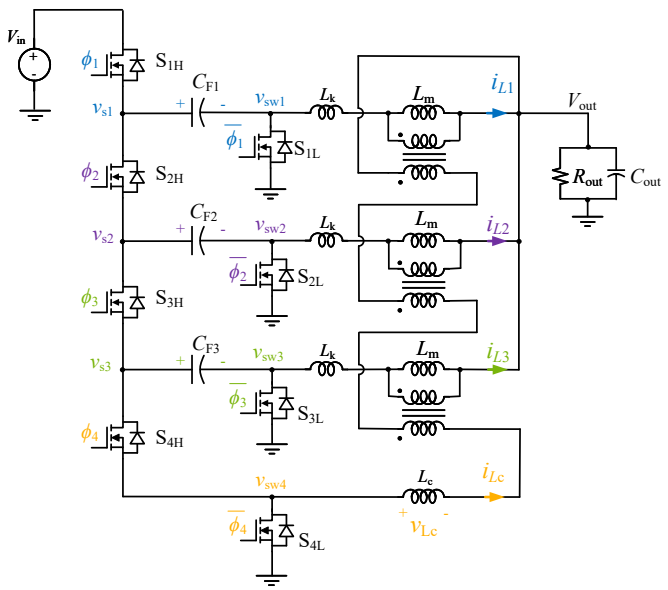


Fig. 1: Proposed series-capacitor zero-bias TLVR topology (four-phase version as an example).

To address these concerns, this paper proposes a series-capacitor zero-bias trans-inductor voltage regulator (SC-ZB-TLVR). The transient performance is improved by the indirect magnetic coupling [9] using TLVR inductors [10]. The interphase coupling results in different equivalent inductances for steady-state and transient operations, enabling faster transient response while preserving the same inductor current ripple to maintain high efficiency [11]. Meanwhile, zero DC flux bias in the TLVR inductors is achieved by injecting the flux generated by the last phase into the remainder of the TLVR cores [12], which can reduce the required core volume by flux cancellation, thereby greatly improving the power density compared to conventional indirect-coupled inductor with floating L_c winding [13]. The half bridge of the last phase can be implemented by DrMOS to achieve higher efficiency and enhanced power density. The i_{L_c}-based control scheme [14] enables the use of the current sensing output of the DrMOS, which greatly simplifies the sensing architecture of CMCOT.

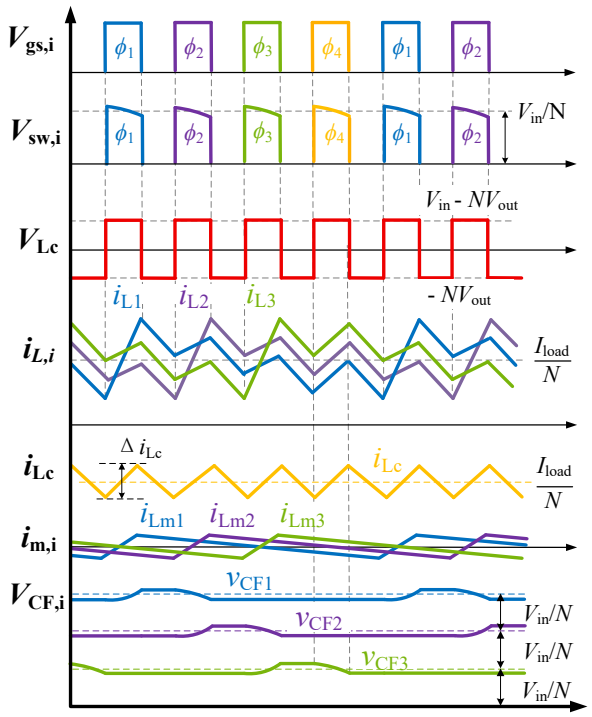


Fig. 2: Steady-state operation waveform of the proposed SC-ZB-TLVR (four-phase, 1-2-3-4 interleave sequence as an example).

It has been well studied that SCB converters have inherent automatic current balancing, which naturally eliminates the need for active balancing control [2]. However, this paper reveals that in SC-ZB-TLVRs, automatic current balancing only holds when adopting TLVR inductors with high coupling coefficients (e.g., $\alpha \approx 1$). Although TLVR inductors are designed with strong coupling to maximize the dynamic response due to strong interphase coupling, low-profile designs with larger leakage inductance [15] and loosely-coupled designs [16] have also been demonstrated in recent years. To the best of our knowledge, the effect of leakage inductance on the performance of ZB-TLVRs has not previously been studied thoroughly. This paper analyzes the unbalanced operating mode due to loose coupling, and a PWM phase-shift balancing strategy is proposed and simulated to fully achieve zero-bias for this converter.

Finally, the proposed converter topology is validated on a 24 V-to-1 V, four-phase, 120 A prototype.

II. Operation Principles of SC-ZB-TLVR

A. Operation waveforms

Fig. 1 shows the schematic drawing of a SC-ZB-TLVR, with four phases as an example. It contains N complementary switch pairs S_{iH} and S_{iL}, $i = 1, 2 ... N$. Except for the last phase, a series capacitor is connected between every switch pair, blocking a voltage of

$$V_{\mathrm{C_{Fi}}} = \frac{(N-i)V_{\mathrm{in}}}{N} \tag{1}$$

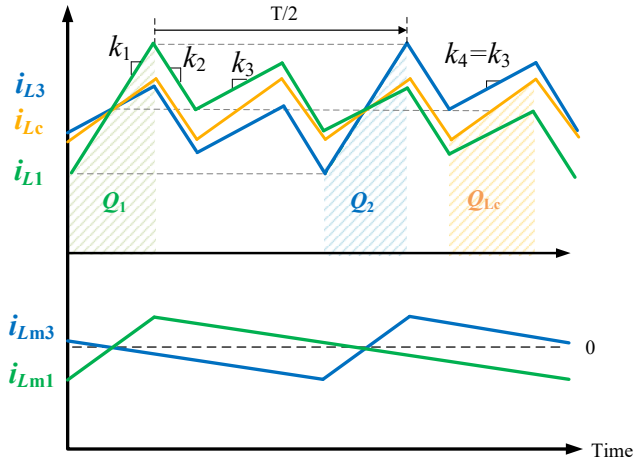
From phase 1 to phase $N-1$, the switch node is connected with a TLVR transformer to V_{out}. Unlike in conventional TLVR [10], where a floating winding in series with the compensation inductor L_{c} links all the secondary windings of each phase together, SC-ZB-TLVR puts L_{c} at phase N, connected in series with the secondary winding of all other phases, then delivers power to V_{out}.

Fig. 2 shows steady-state operation waveform of a four-phase SC-ZB-TLVR. It uses the "1-2-3-4" switching pattern, though any sequence is feasible as long as adjacent upper switches are not turned on at the same time [17]. The series capacitor C_{Fi} charges when S_{iH} is on and discharges when $S_{(i+1)\mathrm{H}}$ is on, regulating the inductor currents between phases. The last phase current $i_{L_{\mathrm{c}}}$ has the same DC bias as the other phase currents. As a result, the series connection of TLVR windings cancels DC flux in the core from phase 1 to $N-1$. Unlike conventional TLVRs, where each core carries a magnetizing current bias of I_{load}/N, the magnetizing currents $i_{L_{\mathrm{m,i}}}$ in SC-ZB-TLVR is much smaller due to DC flux cancellation. This allows the use of smaller cores with the same saturation current, thereby improving power density.

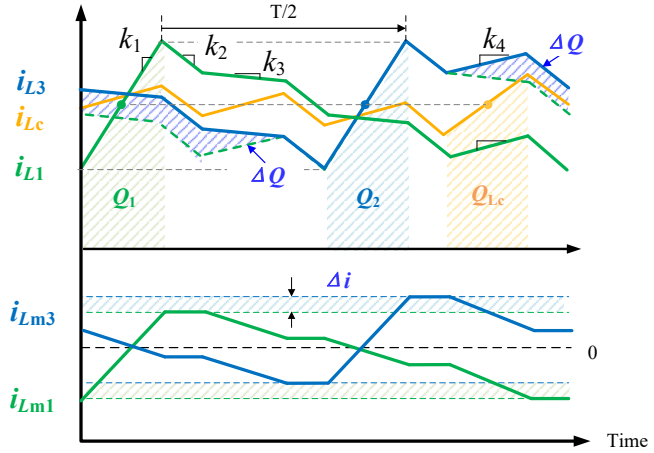
B. Analysis of the current dynamics and steady-state current balancing

Prior works have shown that under the same per-phase duty cycle, series-capacitor buck converters implemented with discrete inductors have inherent automatic current balancing when the flying capacitors are operating in the continuous voltage mode [2]. This balance is achieved by the inherent negative feedback provided by the flying capacitors, and it is still valid under asymmetric per-phase inductance value. In the case of SCB converters with symmetrical two-phase coupling [18], prior work has also proven that the per-phase average inductor currents automatically damp to become balanced after a deviation. In SC-ZB-TLVR, however, the steady-state automatic current balancing does not necessarily hold due to its asymmetric structure, even if all the TLVR inductors are identical. The unbalanced operation comes from the leakage inductance of TLVR inductors. Fig. 3 shows the waveform of a four-phase SC-ZB-TLVR considering ideal and non-ideal coupling. For simplicity, we only demonstrate the case without interphase PWM overlaps. The slope k_1 denotes the inductor current slew rate when the corresponding high-side switch is on, and the rest of the switches are off. Slope k_2 is the current slope when all the high-side switches are off, and k_3 is when other phases except for the L_c phase are on. Finally, k_4 is the slope when the L_c phase is on. The rising slope k_1 determines the steady-state peak-to-peak inductor current ripple, which decides the L_{ss}, while the transient equivalent inductance L_{tr} is determined by k_2 [19]. The detailed derivation of L_{ss} and L_{tr}, k_{1-4} are included in Appendix. A.

In periodic steady state, for i = 1,2 ... $N-1$, the charge



(a) Ideal coupling ($\alpha \to 1$) and balanced operation



(b) Non-ideal coupling case that leads to unbalanced operation

Fig. 3: Phase currents, i_{L_c}, and magnetizing currents of a four-phase SC-ZB-TLVR considering ideal and non-ideal coupling.

balance in the flying capacitors yields

$$\int_0^T i_{C_{Fi}}(t)\, dt = 0 \tag{2}$$

Therefore the converter satisfies

$$Q_1 = Q_2 = ...Q_{N-1} \tag{3}$$

where Q_i denotes the charge delivered into the i_{th} flying capacitor, which is also the charge taken from the $(i+1)_{th}$ capacitor during each turn-on interval, as is shown in Fig. 3.

In SC-ZB-TLVR, the automatic balance holds true when the coupling coefficient $\alpha = \frac{L_k}{L_m + L_k} \to 1$. In this case, (13) shows that k_3 = k_4 when the coupling coefficient is 1, which results in a current waveform like non-ZB TLVRs as in Fig. 3-(a). In this case, i_{L_c} features a triangular wave of $N \times f_{sw}$ frequency. The magnetizing current from phase 1 to $N-1$

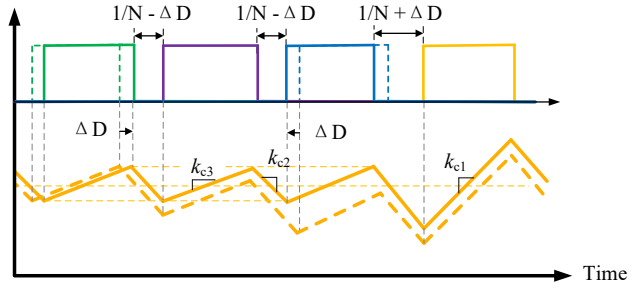


Fig. 4: Proposed phase-shift modulation to correct the current balancing

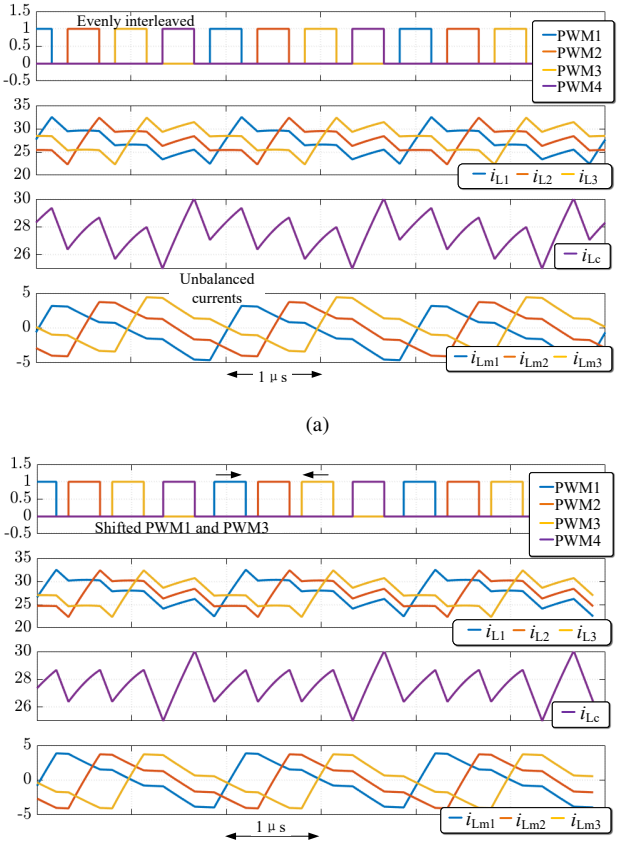


Fig. 5: Simulation verification of the proposed phase-shift correction technique. Simultation setup: four phase, switching frequency $f_{sw} = 500$ kHz, $V_{\text{in}} = 24$ V, $V_{\text{out}} = 1$ V, $L_{\text{m}} = 150$ nH, $L_{\text{k}} = 50$ nH, $L_c = 70$ nH, $\alpha = 0.75$, $C_F = 16$ μF. (a) Unbalanced current waveforms with symmetrically interleaved PWMs. (b) Balanced currnt waveform with ϕ_1 and ϕ_3 shifted by ΔD.

are all zero-bias, which means full DC flux cancellation is achieved.

When $\alpha < 1$, however, the current slope k_4 is larger than k_3 due to non-ideal coupling. This leads to asymmetrical per-phase current waveforms. As is shown in Fig. 3-(b), the slope k_4 occurs at different relative locations to the k_1 slope in

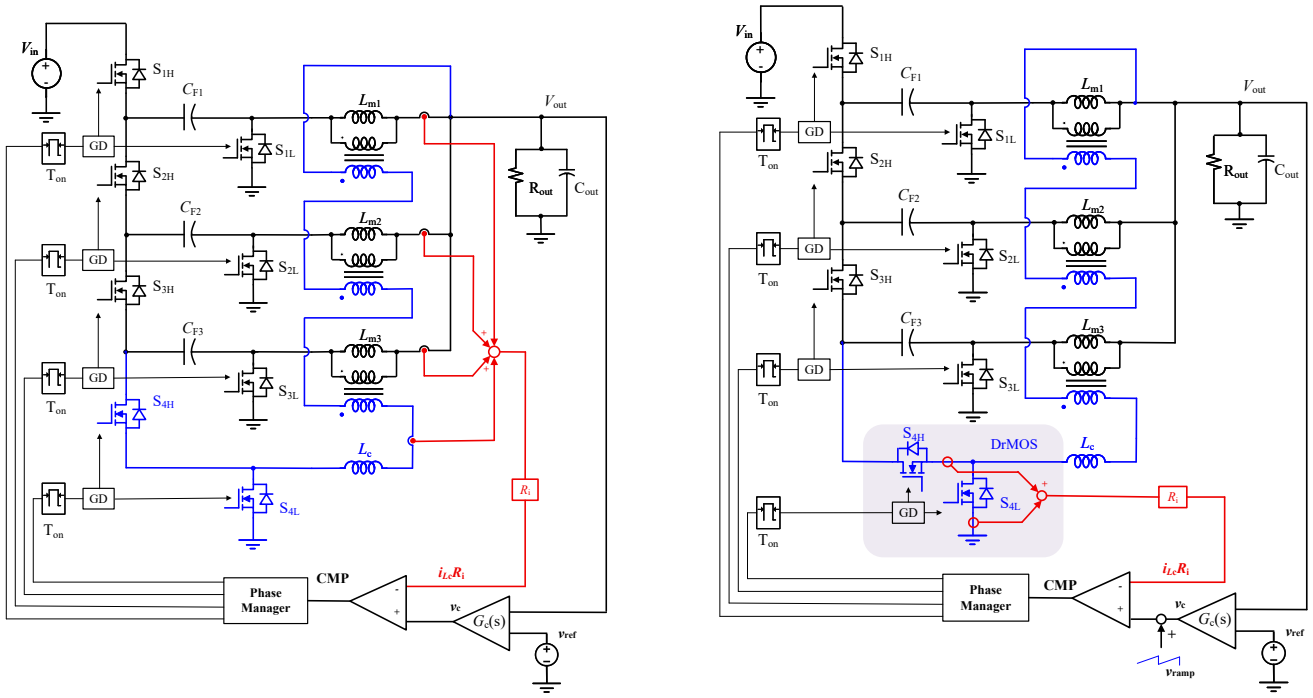


Fig. 6: (a) Conventional CMCOT control scheme implemented in SC-ZB-TLVR. (b) i_{L_c}-based control.

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different phases, but (3) must be maintained. A resulted charge imbalance ΔQ leads to the per-phase DC current deviating from the average current. The waveform of $i_{L_{\mathrm{m1,3}}}$ shows that the magnetizing currents are no longer zero-bias due to the non-ideal coupling.

C. Proposed phase-shift correction to achieve current balancing

Either duty cycle adjustment or PWM phase shift can correct the unbalanced DC bias currents. This section introduces a phase shift strategy to correct the unbalanced current.

Similar to TLVR inductor currents, i_{L_c} in ZB-TLVRs has three different slopes under non-ideal coupling. k_{c1} is the current slope when the high-side switch of the L_c phase is on, k_{c2} is the slope when all the high-side switches are off, k_{c3} is the slope when one of the other phases is on. The derivation of k_{c1-3} can be found by (12) in Appendix. A. As is shown in Fig. 4, the way to correct the per-phase current balancing is to make the peak and valley of i_{L_c} at each subinterval symmetric about the DC current bias. Maintaining the duty cycle D unchanged, we can add lagging phase to PWM1 and add leading phase to PWM3. The shifted duty cycles are both ΔD, which can be calculated by

$$\Delta D = -\frac{Dk_{c1} + Dk_{c3} + 2k_{c2}(1/N - D)}{2k_{c2}} \tag{4}$$

Fig. 5 shows the PLECS simulation of the proposed phase shift scheme. Fig. 5-(a) is the current waveforms with symmetrically interleaved PWMs. It is clear that due to non-ideal coupling, the magnetizing current of phase 1 and phase 3 are no longer zero, which introduces additional flux bias, thereby increasing the required magnetic core volume. In Fig. 5-(b), the PWM signals of phase 1 and 3 are shifted by ΔD according to (4). The i_{L_c} waveform is corrected to be symmetric, and the per-phase magnetizing currents become zero-bias.

D. i_{L_c}-based CMCOT control scheme

In this section, a SC-ZB-TLVR with current-mode constant on-time control (CMCOT) [20] is validated in simulation. Fig. 6-(a) shows the conventional control scheme of CMCOT [21]. A voltage compensator with $G_c(\mathrm{s})$ is included to provide the valley current reference v_c. Inductor currents at each phase are sensed and summed by a gain R_i, then compared with the valley reference. Once i_{sum} falls below the valley reference, the comparator sends the CMP pulse to the controller. A phase manager decides the interleaving sequence, and the high-side switch in the corresponding phase is triggered on for a time of T_{on}.

Fig. 6-(b) shows a proposed i_{L_c}-based control strategy [14] that takes advantage of the current ripple in the L_c winding, streamlining the current sensing scheme and reducing the system complexity. As is shown in Fig. 7, instead of using the summed inductor current in the current loop, i_{L_c}-based control senses only i_{L_c}. If the last phase is used for DC flux injection, the inherent half bridge structure enables the use of

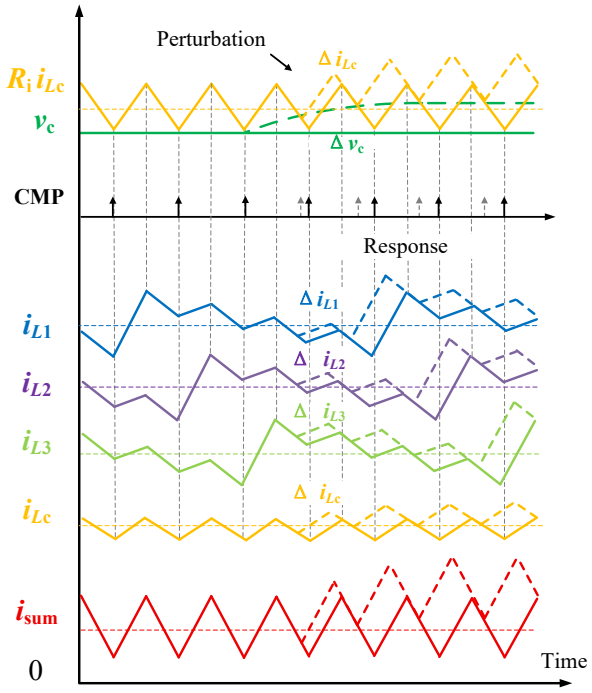


Fig. 7: Proposed i_{L_c}-based COT control

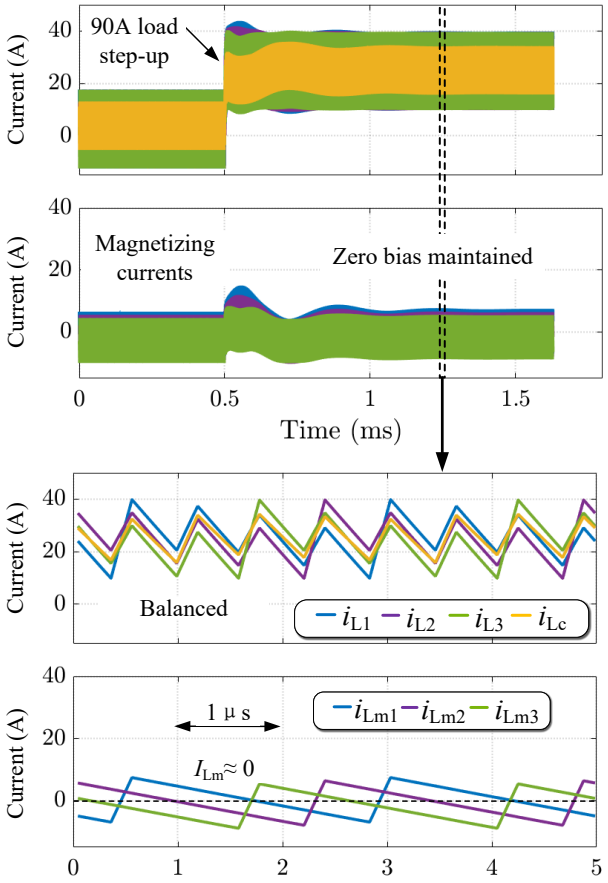


Fig. 8: Simulation result of the proposed i_{L_c}-based control of SC-ZB-TLVR under a load step-up transient

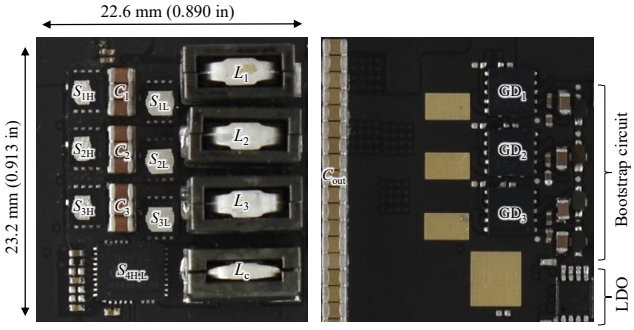


Fig. 9: Top view and bottom view of the hardware prototype. Converter dimensions: 0.89 × 0.91 × 0.55 in^3 (22.6 × 23.2 × 13.9 mm^3).

DrMOS with integrated high-bandwidth, low-cost, and lossless current sensing.

Fig. 8 demonstrates the i_{L_c}-based CMCOT, where the per-phase inductor currents of the proposed SC-ZB-TLVR can balance well without active current balancing, and zero DC-flux bias is maintained under different output load conditions.

III. Experimental Validation

The proposed topology is validated on a 24V-to-1V, 120 A, 500 kHz SC-ZB-TLVR prototype. The component selection of this prototype is summarized in Table. I. Fig. 9 shows the top and the bottom view photographs of the hardware prototype. The switches, flying capacitors, and inductors are on the top side of the PCB. The cascaded bootstrap circuit like [22] and the gate drivers are on the bottom side. Fig. 10 shows the efficiency curves measured under 24V-to-1V and 24V-to-0.8V. The proposed converter is tested up to 120 A output current, achieving an area current density of 0.229 A/mm^2. The performance of this prototype is summarized as in Table. II.

IV. Conclusions

This paper proposes and demonstrates a SC-ZB-TLVR, adopting magnetic coupling to enhance the transient response of SCB converters. In this topology, the flux generated by the last phase is injected to the rest of the phases, thereby decreasing the required core size and improving power density. This work also reveals that in SC-ZB-TLVRs, automatic current balancing degrades under loosely coupled conditions, and additional phase shift can be implemented to re-balance the current, which provides guideline on low-profile TLVR designs. The use of a DrMOS on the half-bridge in the last phase, together with an i_{L_c}-based control scheme, further improves the power density and simplifies current sensing for current-mode constant on-time control. A four-phase 24V-to-sub 1V, 120A SC-ZB-TLVR hardware prototype is built to validate the proposed topology. The prototype achieves a peak efficiency of 92.67% and a full-load efficiency of 86.92% at $f_{\text{sw}} = 500$ kHz, 24V-to-1V.

TABLE I: Component List of the Hardware Prototype

Component	Part Number	Parameters
S_{1-3H}	Infineon IQEH80NE2LM7UCGSCATMA1	25 V, 1 mΩ @ $V_{GS} = 4.5$V
S_{1-3L}	Infineon IQE004NE1LM7CGSCATMA1	15 V, 0.37 mΩ @ $V_{GS} = 7$V
S_{4H},S_{4L}	Infineon TDA21590AUMA1	16 V, 90 A
L_c	Pulse PGL6395.700HLT	70 nH, DCR = 0.23 mΩ
TLVR inductors	BOURNS TLVR1005T-R15K	L_{self} = 150 nH, DCR_{pri} = 0.125 mΩ, DCR_{sec} =0.45 mΩ
C_{F1-3}	Murata GRM21BZ71E106KE15L	10 μF 25V X7R 0805* × 3
Output capacitors C_{out}	Murata GRM21BC80G107ME15L	100 μF 4V X6S 0805* × 20
	TDK C1608X6S0G226M080AC	22 μF 4V X6S 0603* × 40
Gate drivers for $S_{1-3H,L}$	TI UCC27212DPRT	4 A, 120 V
Bootstrap diodes	Nexperia PMEG2020AEA	20 V, 2 A

* The capacitance listed is nominal value before DC derating.

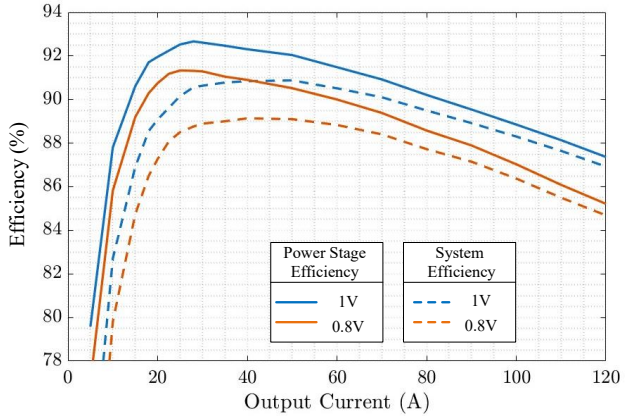


Fig. 10: Measured power stage efficiency (excluding the gate drive loss) and and system efficiency (including the gate drive loss) of the hardware prototype at $V_{in} = 24$ V, $f_{sw} = 500$ kHz.

TABLE II: Measured performance of the hardware prototype

Output Voltage	Power Stage Efficiency	System Efficiency†
1 V	Peak efficiency: 92.67% Full-load efficiency: 87.37%	90.88% 86.92%
0.8 V	Peak efficiency: 91.33% Full-load efficiency: 85.22%	89.14% 84.69%

† Gate drive loss is included in the calculation of system efficiency.

V. Acknowledgements

The authors would like to acknowledge the financial support from the Berkeley Power and Energy Center (BPEC).

Appendix A
Derivation of the Inductor Current Dynamics and Equivalent Inductances for ZB-TLVR

This section presents the derivation of the current dynamics and the equivalent inductances of an N phase ZB-TLVR, taking non-ideal coupling into consideration. The conclusions of this section apply to all the ZB-TLVR topologies using single-secondary 1:1 turns ratio TLVR inductors.

Define the summed inductor current as

$$i_{\text{sum}} = \sum_{i=1}^{N-1} i_i + i_{Lc}. \tag{5}$$

Applying KVL to each phase gives

$$v_{\text{sw},i} - V_o = L_{\text{k}} \frac{di_i}{dt} + L_m \frac{di_{L_{\text{m}}}}{dt}. \tag{6}$$

From KCL at each phase,

$$i_i = i_{L_{\text{m}}} + i_{L_{\text{c}}}. \tag{7}$$

Substituting (7) into (6) and summing from $i = 1$ to $N-1$ yields

$$\sum_{i=1}^{N-1} v_{\text{sw},i} - (N-1)V_o = (L_m + L_k)\frac{di_{\text{sum}}}{dt} - (NL_m + L_k)\frac{di_{Lc}}{dt}. \tag{8}$$

Next, applying KVL around the L_c loop gives

$$v_{\text{sw},N} - V_o + L_m \sum_{i=1}^{N-1} \frac{di_{L_{\text{m,i}}}}{dt} = L_c \frac{di_{L_c}}{dt}. \tag{9}$$

Using (7) to eliminate i_{Lm} in (9), we obtain

$$v_{\text{sw},N} - V_o + L_m \frac{di_{\text{sum}}}{dt} = (NL_{\text{m}} + L_{\text{c}})\frac{di_{L_c}}{dt}. \tag{10}$$

Combining (8) and (10) to eliminate $\frac{di_{\text{sum}}}{dt}$, define

$$\beta = \frac{L_{\text{m}} + L_{\text{k}}}{(N-1)L_{\text{k}} + \frac{L_{\text{k}}L_{\text{c}}}{L_{\text{m}}} + L_{\text{c}}}, \qquad \alpha = \frac{L_{\text{m}}}{L_{\text{m}} + L_{\text{k}}}. \tag{11}$$

The dynamics of the compensation inductor current are obtained as

$$\frac{di_{Lc}}{dt} = \frac{\beta}{L_{\text{m}}} \left[\alpha \sum_{i=1}^{N} v_{\text{sw},i} + v_{\text{sw},N} - \big(1 + \alpha(N-1)\big)V_o \right]. \tag{12}$$

Substituting the expression for $\frac{di_{Lc}}{dt}$ into the phase current

dynamics yields

$$\frac{di_i}{dt} = \frac{1}{L_{\text{self}}}\Bigg[v_{\text{sw},i} - V_o + \beta\Bigg[\alpha \sum_{i=1}^{N-1} v_{\text{sw},i} + v_{\text{sw},N} - \big(\alpha(N-1)+1\big)V_o\Bigg]\Bigg] \tag{13}$$

where $L_{\text{self}} = L_{\text{m}} + L_{\text{k}}$. The per-phase inductor current slopes k_{1-4} can be derived from (13). The i_{L_c} current slopes k_{c1-4} can be derived from (12).

For series-capacitor buck topologies, the output voltage $V_o = DV_{\text{bus}} = NDV_{\text{in}}$. The steady-state equivalent inductance L_{ss} is,

$$\frac{V_{\text{bus}} - V_o}{L_{ss}} = k_1. \tag{14}$$

Solving for L_{ss} gives

$$L_{ss} = L_{\text{self}} \frac{1-D}{(1-D) + \beta\Big(\alpha - \big(\alpha(N-1)+1\big)D\Big)}. \tag{15}$$

The transient equivalent inductance L_{tr} is defined from the falling current slope k_2 as

$$-\frac{V_o}{L_{\text{tr}}} = k_2. \tag{16}$$

Therefore, the transient equivalent inductance is

$$L_{\text{tr}} = \frac{L_{\text{self}}}{1 + \beta\big(\alpha(N-1)+1\big)} \tag{17}$$

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