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Journal

IEEE Transactions on Power Electronics, PP(99)

ISSN

0885-8993

Authors

Ellis, Nathan M
Brooks, Nathan C
Blackwell, Margaret E
et al.

Publication Date

2023

DOI

10.1109/tpel.2023.3285745

IEEE Transactions on Power Electronics, 2023

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N. M. Ellis
N. C. Brooks
M. E. Blackwell
R. A. Abramson
S. Coday
R. C. N. Pilawa-Podgurski

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Nathan M. Ellis, *Member, IEEE,* Nathan C. Brooks, *Student Member, IEEE,* Margaret E. Blackwell, *Student Member, IEEE,* Rose A. Abramson, *Student Member, IEEE,* Samantha Coday, *Member, IEEE,* Robert C. N. Pilawa-Podgurski, *Senior Member, IEEE*

***Abstract*—This work presents a general analytical framework enabling large-signal characterization of resonant switched-capacitor (ReSC) power converters that accounts for passive component voltage and current ripple, for operation at and above resonance. From this, appropriate phase durations for minimized rms currents are derived, in addition to expressions for total passive component volume using an intuitive peak energy method. An example hardware prototype validates both the derived waveforms and timings—as well as total passive volume—through three comparable hardware configurations, one of which minimizes passive component volume. In addition, the proposed technique formulates analytical expressions for both rms currents and peak blocking voltages, facilitating refined loss estimation and component selection. Subsequent calculation of the large-signal Volt–Amp (VA) switch stress metric allows a more accurately quantified trade-off between active and passive components compared to prior work, which has not fully accounted for ripple. Four common ReSC topologies are exemplified throughout, with topology specific parameters documented for reference.**

***Index Terms*—DC-DC converters, hybrid switched capacitor, resonant power conversion.**

I. Introduction

RESONANT switched capacitor (ReSC) power converters (e.g., Fig. 1) are a relatively new class of converter topology primarily relying on capacitors as energy transfer elements, leveraging their superior energy density over magnetics [1]. However, to mitigate the well-known slow-switching limit (SSL) impedance [2] and associated pulse inrush currents in pure switched capacitor (SC) converters, some small inductance is introduced to enable "soft-charging" of the flying capacitors [3]–[5]. When soft-charged, capacitor voltage ripple may be greatly increased without incurring large SSL losses. This allows for more effective energy density utilization of the capacitors which perform most of the voltage conversion [6], while the added magnetics are subjected to reduced volt-seconds. Recent demonstrations [7]–[12] have considered these benefits and illustrate dramatic net reductions in overall ReSC converter volume as compared with more traditional architectures (e.g. buck/boost).

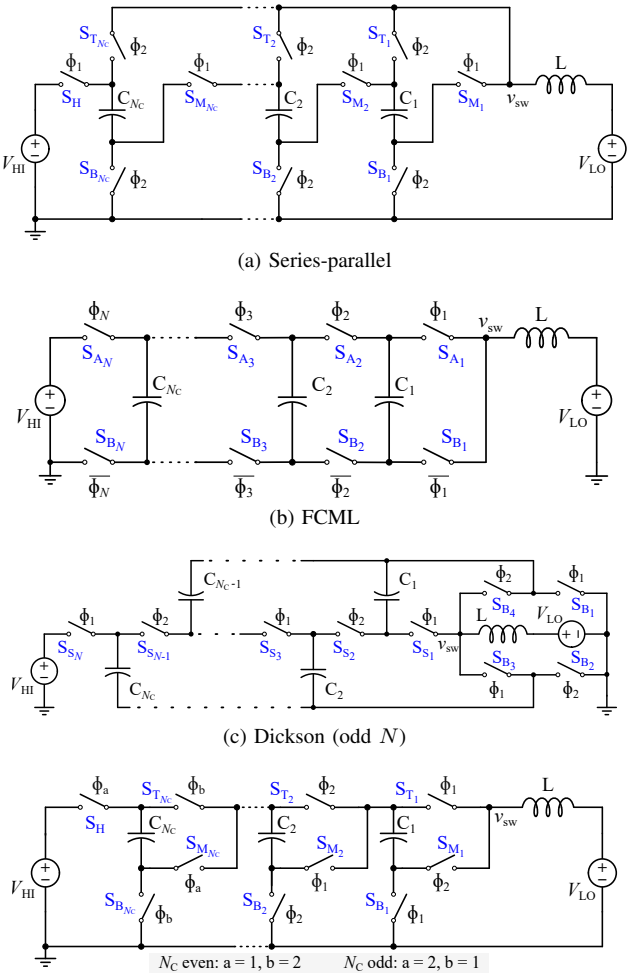

Fig. 1. Four common N:1 ReSC converters with "inductor-at-the-output": (a) series-parallel, (b) flying capacitor multilevel (FCML), (c) Dickson (odd N), and (d) Fibonacci. Here N refers to the conversion ratio and N_C refers to the total number of capacitors.

Prior literature has presented analytical methods to calculate both the minimum achievable passive component volume and output impedance for these types of converter; however, these analyses are often limited to ReSC converters operating

Manuscript received XXXXXXX; accepted XXXXXXXX. Parts of the analysis in Section III of this paper were presented at the 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL) [DOI: 10.1109/COMPEL53829.2022.9830004]. *(Corresponding author: Robert Carl Nikolai Pilawa-Podgurski.)*

The authors are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: nathanmilesellis@berkeley.edu; nathanbrooks@berkeley.edu; blackwell@berkeley.edu; rose_abramson@berkeley.edu; scoday@berkeley.edu; pilawa@berkeley.edu).

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exactly at resonance (e.g., [12], [13]). While this operating point facilitates zero current switching (ZCS) for reduced switching loss, other work in [14]–[21] has established that operating some ReSC converters above resonance can significantly improve overall converter efficiency through a reduction in rms currents and associated conduction losses, despite increases in relative switching loss. Although above resonance operation has been demonstrated in practice, a characteristic analysis has been lacking. The framework presented in [12] is not applicable, while a provision (parameter β) in [13], [22] characterizing the ratio of rms to dc current allows the analysis therein to be extended to above-resonance operation without being explicitly derived.

This work therefore contributes a generalized analytical technique enabling complete characterization of ReSC operation while operating both at and above resonance. No small-ripple approximations are made, resulting in an accurate large-signal solution accounting for both voltage and current ripple on capacitors and inductors, respectively. In addition, the presented analysis is simplified with respect to [12] (which required instantaneous power integrals to be evaluated) and only requires the use of inherent topology characteristics, such as the number of components and phases, and standard charge flow vectors, similar to those described by the analytical method for pure SC converters presented in [2].

While the methodology presented here can be extended and applied to any ReSC converter topology, this work restricts its application to a subset of ReSC converters capable of operating effectively above resonance. Specifically, this work considers fixed-ratio (N:1) ReSC converter topologies with a single inductor placed in series with the low-side port, as is the case for several common example topologies depicted in Fig. 1. Termed "direct" in [22], [23], "inductor-at-the-output" in [19], and here as "inductor-at-the-low-side-port" (to accommodate step-up 1:N variants), these structures are capable of operating both at or significantly above their nominal resonant switching frequency. When operated above resonance, the inductor enters a forward continuous conduction mode where the converter exhibits a lower sensitivity to component or timing mismatch, in addition to the aforementioned reduction in rms current.

In contrast, LC-tank type ReSC structures (e.g. [10], [24]–[28]), termed "indirect" in [23], are constrained to at- or near- resonant operation since they either incur excessive circulating currents when operated above resonance, or hard-charging losses when operated below resonance without the introduction of discontinuous conduction states or dynamic off-time modulation [27], [29], [30]. Consequently, tank-based topologies have a susceptibility to component and timing mismatch and require either active auto-tuning control [31], [32], or accurate component tolerance and stability with aging, temperature, and bias—disqualifying Class II multi-layer ceramic capacitors (MLCCs) [33] and soft-saturating magnetics. Conversely, the switches within tank topologies generally experience favorable constant blocking voltages that are independent of load since voltage ripple is hidden within LC-tank elements [17], [28]—serving to simplify design. Both "direct" and "indirect" topology variations exhibit theoretically identical total passive component volume when operated at resonance, irrespective of inductor count, when inductance is distributed accordingly [12]. However, unless a common core can be used in indirect multi-inductor designs, the magnetics of direct single inductor ReSC designs scale more favorably [34], lending further preference to direct variants. Moreover, the LC tanks within indirect topologies require bi-directional inductor current, necessitating a $2\times$ increase in flux density ripple, ΔB, as compared to the uni-polar current observed in equivalent direct converters, where much of the spectral power is concentrated at dc, having implications for magnetic losses [35], [36].

TABLE I
SURVEY OF ANALYTICAL METHODS FOR SWITCHED-CAPACITOR CONVERTERS

	Work	Type	Above Resonance	Analyzes Ripple		Calculates Loss
				Passives	Switches	
Pure SC	Seeman [2]	–	–	Δv_C	None	Yes
	McRae [39]	–	–	Δv_{out}	Δv_{out}	Yes
ReSC	Pasternak [22]	Direct	Yes	Δi_L*	Δi_L*	Yes
	He [27]	Indirect	–	Δv_C, Δv_{out}, Δi_L	None	Yes
	McLaughlin [13]	Both	No	Δi_L	Δi_L	Yes
	Ye [12]	Both	No	Δv_C, Δi_L	None	No
	This Work	Direct	Yes	Δv_C, Δi_L	Δv_C, Δi_L	No

*explicit derivation of rms current provided for at-resonance operation only.

Following this reasoning, the subset of ReSC converters evaluated in this work (single inductor "direct" topologies) are simultaneously highly attractive and challenging to fully analyze. Analytical expressions for peak ratings are derived for both the capacitor voltages and inductor current, aiding the practicing engineer in component selection. These expressions also permit a derivation of the minimum passive component volume, both at- and arbitrarily above- resonance. The general expressions derived herein collapse into the results presented in [12] when constrained to resonant operation, further validating this general approach. In addition, this framework is used to improve the fidelity of calculated switch stress metrics. Prior switch stress computations typically use simplified voltage and current calculations to characterize the switches, such as neglecting the effects of capacitor voltage ripple on switch voltage [2], [12], [20], [37] or neglecting the effects of inductor current ripple on switch current [2], [12]. Here we calculate the precise peak switch voltages and rms currents and demonstrate that prior simplifying assumptions can lead to significant under-sizing of switches for high-ripple designs. Moreover, while minimized passive component volume is emphasized, the presented framework assists with global optimization efforts (e.g., [38]) by providing the large-signal values and waveforms needed for accurate loss estimation.

Table I summarizes, categorizes, and highlights the limitations of several analytical approaches to SC and ReSC analysis presented in the literature. For example when assessing passive volume, [12] addresses both capacitor voltage ripple, Δv_C, and inductor current ripple, Δi_L, for both direct and indirect

topologies, strictly at resonance. However, the impact of ripple on switch stress is not considered.

Furthermore, since this article constrains consideration to steady-state fixed-ratio converter operation, several important additional aspects are not discussed here, but have been investigated in prior work. These include: start-up, shut-down and transient response [40]–[46]; capacitor voltage and inductor current balancing [47]–[53]; lossless regulation [54], [55] and droop control [2], [56]; zero voltage switching (ZVS) capability [19]; and reliability [57].

This work is organized as follows. Section II presents the base assumptions and analytical framework necessary to characterize the operation of a general (lossless) fixed-ratio ReSC topology. Section III introduces closed-form expressions for phase timings both at and arbitrarily above resonance. A direct energy-based approach for quantifying total passive component volume/mass through assessment of per-component peak energy storage requirements is proposed in Section IV, along with an optimization method to minimize total passive volume. Generalized results are presented for several common ReSC topologies. Section V presents a hardware example illustrating the described analysis. Switch stress including full capacitor voltage and inductor current ripples is assessed in Section VI. Section VII summarizes and discusses the results obtained in Sections III–VI, and contextualizes the trade-offs between different ReSC topologies. Finally, Section VIII concludes this work.

II. Framework Definition

The proposed framework stems from conventional vectorized descriptions of switched capacitor converters in [2], [5], [22], [58] and is derived from fundamental charge-balance and zero volt-second principles. In addition, we assume periodic steady-state operation, with dynamic response beyond the scope of this work. Ideal circuit elements are also assumed, with no ohmic losses or parasitic effects. This assumption is valid for moderate- to heavy-load operation and where ohmic losses have minimal impact on the large-signal dynamics of a converter designed for high efficiency (e.g. $\eta \geq 95\%$). Phase durations are chosen so each phase begins and ends with the same inductor current, implying zero inductor volt-seconds within each phase. This constraint is justified in Appendix A, and validated with hardware in Section V. Lastly, input and output bypass capacitance is assumed large with respect to the flying capacitors, thus the input and output sources can be considered ideal as is done in many existing models and analyses [2], [5], [9], [17], [22], [56]. Finite input/output bypass capacitors may be included as part of a comprehensive analysis that facilitates port voltage ripple constraints [59], [60], however, this adds significant analytical complexity and is omitted here for conciseness. This framework applies not only to two-phase ReSC, but also to multi-phase/multi-resonant converters—more than two phases in a switching period—such as the flying capacitor multi-level (FCML) converter in Fig. 1b.

To begin, several topologically-defining vectors are obtained through careful analysis and deduction for each ReSC structure under consideration. These are summarized in Table II and listed in order of appearance throughout the following sections. General matrices are defined in addition to example values for the series-parallel topology depicted in Fig. 1a.

TABLE II
Definition of Characteristic Terms

N	Conversion ratio, N:1 for $N \in \mathbb{N} \geq 2$
N_{C}	Total number of flying capacitors
N_{P}	Total number of phases within a switching period
N_{S}	Total number of switching devices
$a_{\text{X},ji}$	Net charge through the ith element of type X (C, L, or S), during phase j, normalized to high-side charge quantity q_{HI}
v_i	Mid-range dc voltage on ith capacitor, normalized to high-side voltage V_{HI}
c_i	Capacitance of ith capacitor, normalized to arbitrary scaling capacitance C_0
κ_j	Equivalent capacitance seen by the inductor during phase j, normalized to capacitance C_0
$\omega_{0,j}$	Natural angular frequency of the equivalent LC network during phase j
t_j	Time duration of phase j
τ_j	Time duration of phase j normalized to the full switching period T_{sw}

A. Charge Flow Matrices: $\boldsymbol{a_x}$

As is typical for purely capacitor-based converters [2], periodic steady-state analysis of ReSC structures also begins by assessing charge flow through the converter. To do so, charge flow quantities through all circuit elements are normalized to the amount of charge periodically conducted by the high-side port, q_{HI}, as

$$q_{\text{X},ji} = q_{\text{HI}}\, a_{\text{X},ji} \tag{1}$$

where X is the circuit element type (e.g., capacitor, C; inductor, L; or switch, S), j is the phase index, and i is the element index. The charge quantity q_{HI} is itself an operating parameter defined as

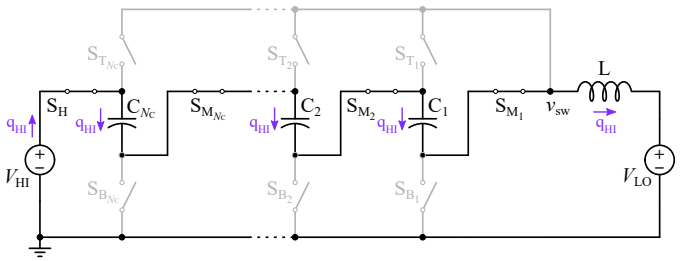
$$q_{\text{HI}} = \frac{I_{\text{HI}}}{f_{\text{sw}}} = I_{\text{HI}} T_{\text{sw}} \tag{2}$$

where I_{HI} is the average high-side port current and f_{sw} is the periodic switching frequency (with associated switching period T_{sw}). Subsequently the normalized charge flow matrix, $\boldsymbol{a_x}$, is comprised of topologically-dependent entries which are invariant of operating point (i.e., power level, voltage, and switching frequency) whereas q_{HI} scales the charge conducted through all elements in unison, while preserving their relative relationships.

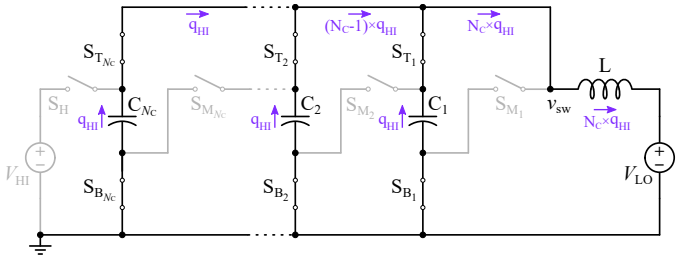
Periodic steady-state requires the capacitors conduct zero net charge per full switching period, as described by

$$\sum_{j=1}^{N_{\text{P}}} a_{\text{C},ji} = 0, \tag{3}$$

where N_{P} is the number of operating phases. Utilizing this



(a) Phase 1: Series connection



(b) Phase 2: Parallel connection

Fig. 2. Charge flow in an N:1 Series-Parallel converter.

characteristic, values for $\boldsymbol{a}_{\mathrm{C}}$, and subsequently $\boldsymbol{a}_{\mathrm{L}}$ and $\boldsymbol{a}_{\mathrm{S}}$, can then be obtained by inspection.

For example, Fig. 2 depicts the periodic steady-state charge flow through an N:1 series-parallel step-down converter operating with two switching phases ($N_{\mathrm{P}} = 2$) and with $N_{\mathrm{C}} = N - 1$ flying capacitors. During phase 1, charge q_{HI} is provided by the high-side source V_{HI}, and is admitted by all series-connected flying capacitors. In adherence with (3), each flying capacitor must then release charge q_{HI} during phase 2. Subsequently, the normalized capacitor charge values, $a_{\mathrm{C},ji}$, for the series-parallel topology are

$$\boldsymbol{a}_{\mathrm{C}_{[N_{\mathrm{P}} \times N_{\mathrm{C}}]}} = \begin{bmatrix} \frac{q_{\mathrm{C},11}}{q_{\mathrm{HI}}} & \frac{q_{\mathrm{C},12}}{q_{\mathrm{HI}}} & \cdots & \frac{q_{\mathrm{C},1N_{\mathrm{C}}}}{q_{\mathrm{HI}}} \\ \frac{q_{\mathrm{C},21}}{q_{\mathrm{HI}}} & \frac{q_{\mathrm{C},22}}{q_{\mathrm{HI}}} & \cdots & \frac{q_{\mathrm{C},2N_{\mathrm{C}}}}{q_{\mathrm{HI}}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & \cdots & 1 \\ -1 & -1 & \cdots & -1 \end{bmatrix} \tag{4}$$

where the first row's entries correspond to phase 1 and the second row's entries correspond to phase 2. The charge matrices $\boldsymbol{a}_{\mathrm{L}}$ and $\boldsymbol{a}_{\mathrm{S}}$ are similarly determined.

Also apparent from Fig. 2, the charge admitted by V_{LO} over both phases is equal to $q_{\mathrm{LO}} = (N_{\mathrm{C}} + 1)\, q_{\mathrm{HI}}$, yielding the converter's voltage conversion ratio:

$$\frac{V_{\mathrm{HI}}}{V_{\mathrm{LO}}} = \frac{I_{\mathrm{LO}}}{I_{\mathrm{HI}}} = \frac{q_{\mathrm{LO}} f_{\mathrm{sw}}}{q_{\mathrm{HI}} f_{\mathrm{sw}}} = \frac{(N_{\mathrm{C}} + 1)\, q_{\mathrm{HI}}}{q_{\mathrm{HI}}} = N. \tag{5}$$

Moreover, converter power throughput, P_{HI}, may be expressed in terms of the average high-side charge q_{HI} as

$$P_{\mathrm{HI}} = I_{\mathrm{HI}} V_{\mathrm{HI}} = \frac{q_{\mathrm{HI}}}{T_{\mathrm{sw}}} V_{\mathrm{HI}}. \tag{6}$$

Table VIII records the charge flow matrices for the flying capacitors, $\boldsymbol{a}_{\mathrm{C}}$, the low-side inductor, $\boldsymbol{a}_{\mathrm{L}}$, and the switches, $\boldsymbol{a}_{\mathrm{S}}$, for the four common ReSC topologies depicted in Fig. 1.

B. Mid-Range Flying Capacitor Voltage Vector: $\boldsymbol{v}$

Each flying capacitor's mid-range voltage is defined as the dc value symmetrically centered between the maximum and minimum voltage, as dictated by ripple. This value is distinct from the time-averaged dc voltage which can deviate significantly in multi-phase converters. Here the mid-range voltages can be derived from an assumption of zero average voltage across the inductor (i.e., zero volt-seconds) within each phase. Under this assumption, the inductor may be treated as a short circuit when applying average KVL loops to each phase. Subsequently the absolute mid-range voltages of each flying capacitor, V_{C_i}, may be expressed with respect to the high-side voltage, V_{HI}, as

$$V_{\mathrm{C}_i} = V_{\mathrm{HI}}\, v_i, \tag{7}$$

where v_i represents the normalized (to V_{HI}) mid-range voltage. By applying per-phase *average* KVL to the N:1 series-parallel depicted in Fig. 2, during phase 2 each flying capacitor is connected in parallel with—and thus holds a voltage equal to—V_{LO}. Using the conversion ratio relationship established in (5), the normalized capacitor voltage vector, $\boldsymbol{v}$, is defined as

$$\boldsymbol{v}_{[1 \times N_{\mathrm{C}}]} = \begin{bmatrix} \frac{V_{\mathrm{C}_1}}{V_{\mathrm{HI}}} & \frac{V_{\mathrm{C}_2}}{V_{\mathrm{HI}}} & \cdots & \frac{V_{\mathrm{C}_{N_{\mathrm{C}}}}}{V_{\mathrm{HI}}} \end{bmatrix} = \begin{bmatrix} \frac{1}{N} & \frac{1}{N} & \cdots & \frac{1}{N} \end{bmatrix}. \tag{8}$$

Although beyond the scope of this work, certain multi-resonant topologies—e.g., the multi-resonant doubler [61] and the cascaded series-parallel [62]—or switching schemes—e.g., split-phase switching [63], [64]—have mid-range voltages dependent on load [58], adding significant analytical complexity.

C. Capacitance Vector: $\boldsymbol{c}$

While some topologies have no strict constraints on capacitance sizing (e.g. FCML converter), others require specific relative sizing to prevent hard-charging and retain simplified clocking schemes, as derived in [5], [58], [65], [66] for example. The absolute capacitance of each flying capacitor, C_i, is normalized to a single capacitance value, C_0, as

$$C_i = C_0\, c_i \tag{9}$$

and by doing so, the required relative capacitor relationships are preserved as the single value C_0 changes—a useful feature for the analytical passive component volume minimization performed in Section IV.

Considering the exemplar series-parallel topology, all capacitors conduct equal charge in each phase, and must express identical voltage ripple characteristics when connected in parallel during phase 2. Thus, by $Q = CV$ (and to ensure soft-charging behavior) each capacitor must be equal in value, yielding

$$\boldsymbol{c}_{[1 \times N_{\mathrm{C}}]} = \begin{bmatrix} \frac{C_1}{C_0} & \frac{C_2}{C_0} & \cdots & \frac{C_{N_{\mathrm{C}}}}{C_0} \end{bmatrix} = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}. \tag{10}$$

The normalized capacitance vector, $\boldsymbol{c}$, is documented in Table VIII for the series-parallel, Dickson, and Fibonacci

topologies; and for the FCML topology, all capacitances are chosen to be equal for simplicity.

D. Lumped Equivalent Capacitance Vector; $\boldsymbol{\kappa}$

During each switching phase j, the inductor forms a second-order resonant impedance network with the connected flying capacitors, which have an equivalent lumped capacitance, $C_{\mathrm{e},j}$. This value is then normalized with respect to C_0, yielding $\boldsymbol{\kappa}$:

$$C_{\mathrm{e},j} = C_0\,\kappa_j. \tag{11}$$

In phase 1 of the example series-parallel converter (Fig. 2), all capacitors are connected in series and the equivalent capacitance seen by the inductor is

$$C_{\mathrm{e},1} = C_1||C_2||\cdots||C_{N_\mathrm{C}} = \frac{1}{N_\mathrm{C}}\,C_0 \tag{12}$$

whereas in phase 2 all capacitors are connected in parallel relative to the inductor and the equivalent capacitance is

$$C_{\mathrm{e},2} = C_1 + C_2 + \cdots + C_{N_\mathrm{C}} = N_\mathrm{C}\,C_0. \tag{13}$$

More generally, the normalized equivalent capacitance vector, $\boldsymbol{\kappa}$, is defined and shown for the series-parallel topology as

$$\boldsymbol{\kappa}_{[N_\mathrm{P}\times 1]} = \begin{bmatrix} \frac{C_{\mathrm{e},1}}{C_0} \\ \frac{C_{\mathrm{e},2}}{C_0} \end{bmatrix} = \begin{bmatrix} \frac{1}{N_\mathrm{C}} \\ N_\mathrm{C} \end{bmatrix} \tag{14}$$

and is tabulated for additional topologies in Table VIII.

This section has obtained fundamental topology-dependent parameters. However, in order to fully characterize the large signal behaviour of a ReSC converter, including passive volume and switch stress both at and above resonance (discussed in Sections IV-VII), switching-frequency dependencies must also be derived. The following Section III explores how phase timings and current waveforms depend on switching frequency.

III. Phase Timings

A "direct" ReSC converter can be switched at its natural resonant switching frequency, $f_{\mathrm{sw},0}$, to achieve zero current switching (ZCS) at each phase transition. However, dissimilar to "indirect" or LC-tank topologies, the switching frequency of a direct topology may also be increased without incurring increased circulating currents [16]. Subsequently, we define a free parameter, Γ, as the ratio of the actual switching frequency, f_sw, to the natural resonant switching frequency

$$\Gamma = \frac{f_\mathrm{sw}}{f_{\mathrm{sw},0}} = \frac{T_{\mathrm{sw},0}}{T_\mathrm{sw}}. \tag{15}$$

Resonant ZCS is obtainable at $\Gamma = 1$ (i.e., at-resonance operation), while for $\Gamma > 1$ (i.e., above-resonance operation) the inductor enters continuous conduction mode (CCM). In practice, values of $\Gamma < 1$ (i.e., below-resonance operation) would only be implemented with a modified discontinuous conduction mode (DCM) or dynamic off-time modulation (DOTM) [29], [30], otherwise SSL losses would reemerge.

The motivation for operation above resonance operation has been explored in [14]–[18], [20], [21] as a method for reducing conduction losses and improving overall efficiency. However, for several topologies—including the FCML converter and resonant N-phase implementations of Cockcroft-Walton and Dickson converters [67], [68]—the phase durations depend heavily on the relationship between the natural resonant switching frequency and the implemented f_sw. Given that a rigorous proof of the necessary phase timings for above resonance operation has not been demonstrated in the literature, [16], [17] instead relied on closed-loop control to converge on appropriate phase durations.

Therefore, this section expands on an earlier version of this work in [21] to explicitly derive the required relative phase durations for any given switching frequency at or above resonance ($\Gamma \geq 1$). Continuous closed-form expressions are derived for phase-timing durations which minimize the peak, peak-to-peak, and rms inductor current both at resonance and for arbitrary frequencies above resonance. The presented analysis yields a robust method for explicitly determining the phase durations as well as the inductor current waveform used for the switch stress analysis in Section VI.

A. Phase Duration Vector: $\boldsymbol{\tau}$

Each phase duration, t_j, can be defined in terms of the full switching period, T_sw, using a normalization parameter, τ_j,

$$t_j = T_\mathrm{sw}\,\tau_j \tag{16}$$

where T_sw defines the sum of all N_P phase durations

$$T_\mathrm{sw} = \sum_{j=1}^{N_\mathrm{P}} t_j. \tag{17}$$

The normalized phase duration vector, $\boldsymbol{\tau}$, is deduced from the resonance of the inductor current $i_L(t)$ for each topology and as a function of Γ.

When operating at the resonant switching frequency, $f_{\mathrm{sw},0}$ (i.e., $\Gamma = 1$), each phase is half-wave resonant with $i_\mathrm{L}(t)$ starting and ending at 0 A. Thus the phase duration, t_j, equals half the duration of the natural resonant period, $T_{0,j}$, of the lumped LC resonant tank in the jth phase or

$$t_j|_{\Gamma=1} = T_{\mathrm{sw},0}\cdot\tau_j|_{\Gamma=1} = \frac{T_{0,j}}{2} \tag{18}$$

as per (16).

The natural angular frequency, $\omega_{0,j}$, associated with $T_{0,j}$ can be expressed as

$$\omega_{0,j} = \frac{1}{\sqrt{L\cdot C_0\kappa_j}} = \frac{2\pi}{T_{0,j}} = \frac{\pi}{t_j|_{\Gamma=1}} \tag{19}$$

since parameter κ_j defines the lumped equivalent capacitance.

Calculating the phase durations, t_j, for operation above resonance (i.e., $\Gamma > 1$) requires further analysis. Within each phase j, if the inductor is subjected to zero volt-seconds, then it forms a symmetrically centered sinusoidal segment[1], as depicted in Fig. 3. Continuity in $i_\mathrm{L}(t)$ between adjacent

[1]Appendix A demonstrates timings calculated under this assumption always satisfy both charge balance and inductor current continuity in periodic steady-state.

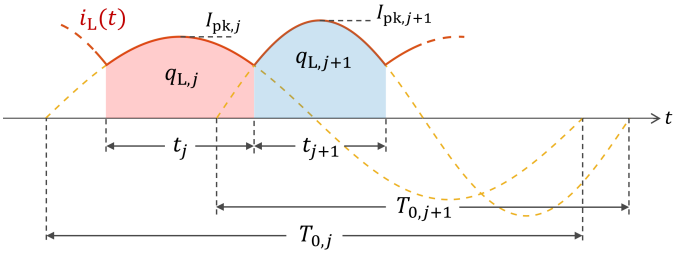


Fig. 3. Two adjacent phases of the inductor current waveform, $i_L(t)$, operating above resonance. Each phase constitutes a symmetrically centered sinusoidal segment with angular frequency governed by (19).

phases (including $j = N_P$ and $j = 1$) can be expressed mathematically as

$$I_{pk,j} \cos\left(\omega_{0,j} \frac{t_j}{2}\right) = I_{pk,j+1} \cos\left(\omega_{0,j+1} \frac{-t_{j+1}}{2}\right), \quad \forall j \leq N_P \tag{20}$$

where $I_{pk,j}$ is the peak current in phase j.

Furthermore during phase j, the inductor conducts charge $q_{L,j}$, where

$$\begin{aligned} q_{L,j} &= \int_{-\frac{t_j}{2}}^{\frac{t_j}{2}} I_{pk,j} \cos(\omega_{0,j}\, t)\, dt \\ &= \frac{2I_{pk,j}}{\omega_{0,j}} \sin\left(\omega_{0,j} \frac{t_j}{2}\right) = q_{HI}\, a_{L,j}, \quad \forall j \leq N_P \end{aligned} \tag{21}$$

which relates to the known normalized charge flow matrix, $\boldsymbol{a}_L$, and can be rearranged with respect to $I_{pk,j}$ as

$$I_{pk,j} = \frac{q_{HI}\, a_{L,j}\, \omega_{0,j}}{2 \sin\left(\omega_{0,j} \frac{t_j}{2}\right)}, \quad \forall j \leq N_P. \tag{22}$$

Combining the phase-to-phase current continuity (20) and per-phase charge flow (22) yields

$$\frac{a_{L,j}\, \omega_{0,j}}{\tan\left(\omega_{0,j} \frac{t_j}{2}\right)} = \frac{a_{L,j+1}\, \omega_{0,j+1}}{\tan\left(\omega_{0,j+1} \frac{t_{j+1}}{2}\right)}, \quad \forall j \leq N_P. \tag{23}$$

Equation (23) can be solved using (19) and (16), to determine appropriate normalized phase durations, τ_j, for each phase. The resultant vector, $\boldsymbol{\tau}$, is documented for the four topologies in Table VIII. For all two-phase converters, τ_j is notably independent of Γ, as will be demonstrated for the series-parallel converter in Example 1. However, as detailed in [21], phase durations for the FCML converter vary with Γ. This derivation, documented as Example 2, is more complex, yielding an implicit transcendental equation with an approximated numerical solution.

Example 1: Series-Parallel Converter

Consider the two-phase series-parallel topology with arbitrary conversion ratio N in Fig. 2 as an example. Substituting the normalized equivalent capacitance vector, κ_j, (from Table VIII) into the natural angular frequency, $\omega_{0,j}$, during each phase in (19) yields

$$\omega_{0,1} = \sqrt{N-1} \cdot \frac{1}{\sqrt{LC_0}} \tag{24}$$

and

$$\omega_{0,2} = \frac{1}{\sqrt{N-1}} \cdot \frac{1}{\sqrt{LC_0}} \tag{25}$$

with the corresponding relationship between these two frequencies as

$$\omega_{0,1} = (N-1)\, \omega_{0,2}. \tag{26}$$

Next, (26) and values for normalized inductor charge flow, $a_{L,j}$, (recorded in Table VIII) are substituted into the steady-state charge flow and inductor continuity constraint given by (23), yielding

$$\tan\left(\omega_{0,1} \frac{t_1}{2}\right) = \tan\left(\frac{\omega_{0,1}}{N-1} \cdot \frac{t_2}{2}\right). \tag{27}$$

The argument of each tangent is then equated to find a relationship between the two phase time durations

$$t_1 = \frac{1}{N-1}\, t_2. \tag{28}$$

For this two-phase topology

$$T_{sw} = t_1 + t_2, \tag{29}$$

and therefore the normalized phase durations, τ_j, become

$$\begin{aligned} \boldsymbol{\tau}_{[N_P \times 1]} &= \begin{bmatrix} \frac{t_1}{T_{sw}} \\ \frac{t_2}{T_{sw}} \end{bmatrix} \\ &= \begin{bmatrix} \frac{1}{N} \\ \frac{N-1}{N} \end{bmatrix} \end{aligned} \tag{30}$$

where $\boldsymbol{\tau}$ only varies with conversion ratio and not Γ. This result is also recorded in Table VIII.

In addition, substituting (26) and (28) into (20) reveals $I_{pk,1} = I_{pk,2}$—a consistent result for all two-phase converters considered in this work.

Example 2: Flying Capacitor Multi-Level (FCML) Converter

While Example 1 exhibits consistent phase durations at- and above-resonance, the phase durations are more complex for the higher order ($N \geq 3$) resonant FCML converter. Extensive literature explores the dynamic behavior of the PWM regulating FCML converter, both using time domain [47], [48], [50], [52], [53], [69] and frequency domain [70]–[72] methods. However less discussion surrounds the resonant, fixed-ratio variation capable of achieving smaller magnetic volume. In regulating mode, conventional symmetric phase-shifted PWM dictates identical phase durations. However in resonant mode, phase durations deviate to accommodate the differing natural resonant frequencies within each phase. This adjustment improves capacitor balancing and overall converter efficiency [16], [17], [21]. While [16], [17] explored above-resonance operation of $N = 3$ and $N = 6$ FCML converters, these works expanded on the valley current control scheme in [73] to converge on optimal phase durations through active feedback without providing an analytical solution. Here we provide an accurate closed form solution for appropriate phase timings, accounting for all $\Gamma \geq 1$.

Fig. 4 depicts the phase progression for an exemplar FCML converter with $N = 5$. Using this same nomenclature, (31)

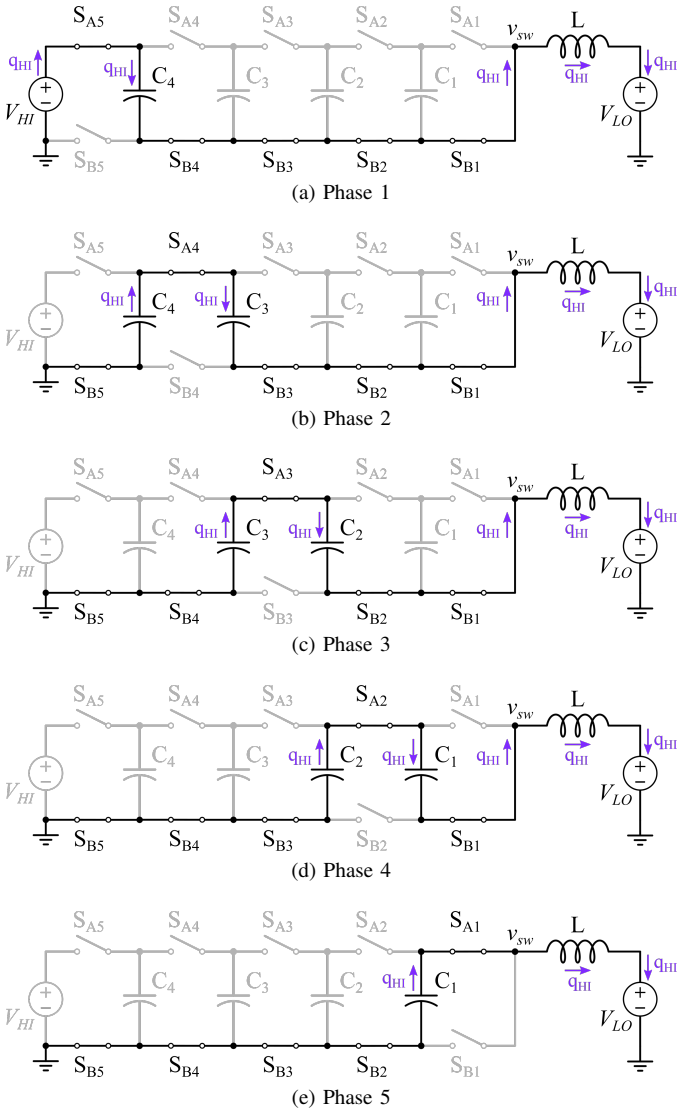


Fig. 4. Schematics for the phase progression of a 5:1 FCML converter ($N = 5$), highlighting the charge flow during each phase. Charge flow is normalized with respect to the high-side input charge quantity q_{HI}.

describes the normalized lumped capacitance presented to the inductor during each phase, κ, in terms of arbitrary integer conversion ratio N.

$$\kappa_j = \begin{cases} 1 & \text{for } \; j \in \{1, N\} \\ \frac{1}{2} & \text{for } \; j \in 2 \leq \mathbb{N} \leq (N-1) \end{cases} \tag{31}$$

Consequently the first and last phases have identical durations, while all phases in between have a different (but equal) duration. Thereby, we can limit consideration to the first and second phase intervals only, where the full switching period may be expressed as

$$T_{\text{sw}} = \sum_{j=1}^{N} t_j = 2t_1 + (N-2)\, t_2. \tag{32}$$

Evaluating (19) with (31)

$$\sqrt{2}\,\omega_{0,1} = \omega_{0,2} \tag{33}$$

and substituting into (23) produces an implicit equation for t_1

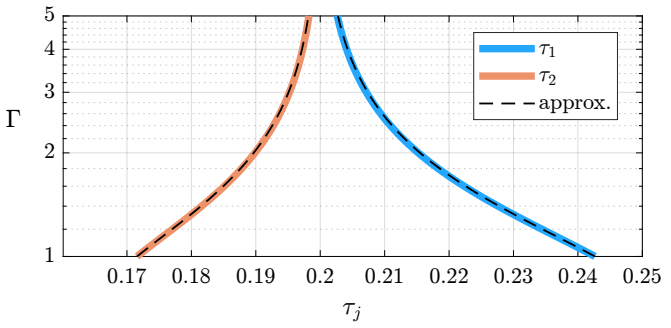


Fig. 5. Numerical solution of relative phase durations τ_1 and τ_2 for a 5:1 FCML converter across Γ. The closed-form approximations are superimposed with dashed lines and differ by less than 0.03% of the switching period.

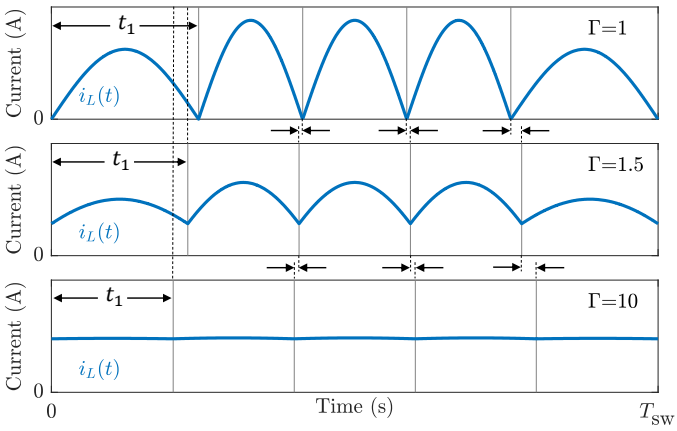


Fig. 6. Simulated inductor current waveforms $i_{\text{L}}(t)$ for a 5:1 resonant FCML converter, demonstrating the required change in phase durations as a function of Γ.

and t_2,

$$\sqrt{2}\,\tan\!\left(\omega_{0,1}\frac{t_1}{2}\right) = \tan\!\left(\sqrt{2}\,\omega_{0,1}\frac{t_2}{2}\right). \tag{34}$$

This implicit equation of phase durations does not reduce analytically, but it can be solved numerically using (32) as a constraint. From inspection of the numerical solution, an accurate closed-form expression for the relative phase durations is approximated as a function of N and Γ as

$$\tau_1 = \frac{t_1}{T_{\text{sw}}} \approx \left(\frac{1}{N} - \frac{\sqrt{2}}{2\sqrt{2}+N-2}\right)\cdot\frac{\Gamma}{\pi}\sin\left(\frac{\pi}{\Gamma}\right) + \frac{\sqrt{2}}{2\sqrt{2}+N-2} \tag{35}$$

$$\tau_2 = \frac{t_2}{T_{\text{sw}}} \approx \left(\frac{1}{N} - \frac{1}{2\sqrt{2}+N-2}\right)\cdot\frac{\Gamma}{\pi}\sin\left(\frac{\pi}{\Gamma}\right) + \frac{1}{2\sqrt{2}+N-2}. \tag{36}$$

Fig. 5 shows both the numerical and analytical approximations for τ_1 and τ_2 for an $N = 5$, FCML converter example. The error between the numerical and analytical results is negligible, validating the accuracy of (35) and (36). Finally, Fig. 6 depicts simulated inductor current waveforms for various Γ, highlighting the change required in t_1 (and correspondingly t_2) to ensure zero volt-second per phase.

IV. Passive Component Volume/Mass

To characterize passive component volume/mass, and subsequently enable converter size/weight minimization, expressions are derived for both total flying capacitor and inductor volume/mass, as dictated by their peak energy storage requirements.

A direct energy method is demonstrated here, expanding on the flying capacitor analysis in [58], and using the phase timings derived in Section III to further obtain expressions for peak inductor energy. Dissimilar to [12], this approach circumvents the need to analytically generalize and integrate instantaneous power waveforms (i.e., $p(t) = v(t) \cdot i(t)$) for every passive component.

While the results of the proposed method and [12] are equivalent for operation at resonance, the proposed method generalizes the passive component requirements for arbitrary switching frequencies *above* resonance (i.e., $\Gamma > 1$) where both the peak flying capacitor voltage and inductor current are diminished.

A. Total Peak Flying Capacitor Energy Storage

To calculate the total flying capacitor energy storage requirement, consider the peak voltage expressed on each flying capacitor, as a function of load, while noting these events may not occur simultaneously in time for each flying capacitor. Moreover, since a flying capacitor may admit charge over multiple phases before achieving its peak voltage—as is the case for the multi-resonant doubler [61] and cascaded series-parallel [62] topologies—a modified charge flow quantity $\hat{a}_{\mathrm{C},i}$ is defined describing the maximum deviation in stored charge on the ith flying capacitor throughout a full switching cycle[2]. For converters in which each flying capacitor only admits charge during a single phase (e.g., Fig. 1), $\hat{a}_{\mathrm{C},i}$ is defined as

$$\hat{a}_{\mathrm{C},i} = \max_{j \in [N_{\mathrm{P}}]} a_{\mathrm{C},ji}, \tag{37}$$

which for two-phase converters may be simplified to

$$\hat{a}_{\mathrm{C},i} = |a_{\mathrm{C},ji}| \qquad \forall j \in \{1, 2\} \tag{38}$$

since each capacitor must admit and release the same quantity of charge across both phases in periodic steady-state.

Subsequently the peak-to-peak voltage ripple, $\Delta v_{\mathrm{pp},i}$, on each flying capacitor, i, may be described as

$$\Delta v_{\mathrm{pp},i} = \frac{\hat{q}_{\mathrm{C},i}}{C_i} = \frac{q_{\mathrm{HI}}\, \hat{a}_{\mathrm{C},i}}{C_0 c_i} \tag{39}$$

The peak energy storage requirement follows for the ith capacitor across all phases as

$$\begin{aligned} E_{\mathrm{C,pk},i} &= \max_{j \in [N_{\mathrm{P}}]} \left\{ \frac{1}{2} C_i\, V_{\mathrm{pk,C}_i}^2 \right\} \\ &= \frac{1}{2} C_0 c_i \cdot \left(V_{\mathrm{HI}} v_i + \frac{1}{2} \Delta v_{\mathrm{pp},i} \right)^2 \end{aligned} \tag{40}$$

where the peak capacitor voltage is the mid-range voltage plus half the peak-to-peak voltage ripple, or $V_{\mathrm{pk,C}_i} = V_{\mathrm{C}_i} + \frac{1}{2}\Delta v_{\mathrm{pp},i}$.

[2]Appendix B describes the general form of the modified charge flow quantity $\hat{a}_{\mathrm{C},i}$ for any ReSC converter with any sequence of capacitor charging/discharging.

The total peak flying capacitor energy over all N_{C} capacitors is then

$$E_{\mathrm{C,tot}} = \sum_{i=1}^{N_C} E_{\mathrm{C,pk},i}. \tag{41}$$

Substituting (6), (39) and (40) into (41) yields

$$E_{\mathrm{C,tot}} = \frac{C_0 V_{\mathrm{HI}}^2}{2} A_1 + \frac{V_{\mathrm{HI}} q_{\mathrm{HI}}}{2} A_2 + \frac{q_{\mathrm{HI}}^2}{8 C_0} A_3 \tag{42}$$

where

$$A_1 = \sum_{i=1}^{N_{\mathrm{C}}} c_i v_i^2 \tag{43}$$

$$A_2 = \sum_{i=1}^{N_{\mathrm{C}}} v_i \hat{a}_{\mathrm{C},i} \tag{44}$$

$$A_3 = \sum_{i=1}^{N_{\mathrm{C}}} \frac{\hat{a}_{\mathrm{C},i}^2}{c_i} \tag{45}$$

This result is similar to that described in [58] where notation α, β, θ is used in place of A_1, A_2, and A_3. Furthermore, the impact of switching frequency on capacitor ripple, and therefore peak storage, is subsumed within q_{HI}, recalling (2) and (15).

The total volume of the capacitive elements can then be computed as

$$\mathrm{Vol}_{\mathrm{C,tot}} = \frac{E_{\mathrm{C,tot}}}{\rho_{\mathrm{C}}} \tag{46}$$

where ρ_{C} is the volumetric energy density ($\mathrm{J/m^3}$) of the chosen capacitor technology. Alternatively, total mass (kg) may be defined using each components' specific density [1]. Similarly, a cost density metric defining stored Joules per unit cost (J/$) may be used.

B. Peak Inductor Energy Storage

Next, peak inductor energy storage is calculated, accounting for converter operation above resonance (i.e., $\Gamma > 1$). For simplicity, the inductor is assumed to have a constant inductance with applied current bias and to be saturation limited, as is often the case for low-loss ferrite materials. Consequently, the minimum inductor volume is proportional to the peak energy stored therein.

First, the per-phase resonance equation (19) is rearranged to give

$$L = \frac{1}{\omega_{0,j}^2 \kappa_j C_0} \tag{47}$$

and (15), (16), (18), and (19) are substituted into the peak inductor current in (22)

$$I_{\mathrm{pk},j} = \frac{q_{\mathrm{HI}}\, a_{\mathrm{L},j}\, \omega_{0,j}}{2 \sin\left(\omega_{0,j} \frac{t_j}{2}\right)} = \frac{q_{\mathrm{HI}}\, a_{\mathrm{L},j}\, \omega_{0,j}}{2 \sin\left(\frac{\pi}{2\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}. \tag{48}$$

Using (47) and (48), the peak inductor energy over all phases, j, can then be expressed as

$$E_{\mathrm{L,pk}} = \max_{j \in [N_{\mathrm{P}}]} \left\{ \frac{1}{2} L\, I_{\mathrm{pk},j}^2 \right\} = \frac{q_{\mathrm{HI}}^2}{2 C_0} B_1 \tag{49}$$

where

$$B_1 = \max_{j\in[N_P]} \left\{ \frac{a_{L,j}^2}{4\kappa_j} \cdot \frac{1}{\sin^2\left(\frac{\pi}{2\Gamma} \cdot \frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)} \right\}. \tag{50}$$

For converters with τ_j independent of Γ, B_1 is simplified since $\tau_j = \tau_j|_{\Gamma=1}$. Furthermore, for all converters operating in resonant ZCS mode (i.e., $\Gamma = 1$), (50) reduces to

$$B_1\big|_{\Gamma=1} = \max_{j\in[N_P]} \left\{ \frac{a_{L,j}^2}{4\kappa_j} \right\} \tag{51}$$

The total inductor volume can then be computed as

$$\mathrm{Vol_L} = \frac{E_{L,pk}}{\rho_L} = \frac{q_{HI}^2}{2\rho_L C_0} B_1 \tag{52}$$

where ρ_L is the volumetric energy density ($\mathrm{J/m^3}$) of the inductor. Again, specific density (J/kg) or cost density (J/$) may alternatively be used in mass or cost constrained applications, respectively.

C. Minimization of Passive Components

Passive components typically comprise the large majority of a converter's volume (or mass). Thus, a converter's volume may be approximately minimized by considering only the volume of the passive components. To do so, an expression for total passive volume—as defined by peak energy storage requirements—is constructed using (46) and (52).

$$\begin{aligned}\mathrm{Vol_{tot}} &= \mathrm{Vol_C} + \mathrm{Vol_L} \\ &= \left(\frac{C_0 V_{HI}^2}{2\rho_C} A_1 + \frac{V_{HI} q_{HI}}{2\rho_C} A_2 + \frac{q_{HI}^2}{8\rho_C C_0} A_3\right) + \frac{q_{HI}^2}{2\rho_L C_0} B_1.\end{aligned} \tag{53}$$

Total passive volume is then minimized by differentiating with respect to the normalized capacitance C_0

$$\left.\frac{\partial \mathrm{Vol_{tot}}}{\partial C_0}\right|_{C_0=C_0^*} = 0 = \frac{V_{HI}^2}{2\rho_C} A_1 - \frac{q_{HI}^2}{8\rho_C C_0^{*2}} A_3 - \frac{q_{HI}^2}{2\rho_L C_0^{*2}} B_1 \tag{54}$$

which is solved explicitly for the minimizing normalized capacitance C_0^* as

$$C_0^* = \frac{q_{HI}}{V_{HI}} \sqrt{\frac{\frac{1}{4}A_3 + \frac{\rho_C}{\rho_L} B_1}{A_1}} \tag{55}$$

for a given Γ, V_{HI}, q_{HI}, and passive energy density ratio ρ_C/ρ_L. The composite terms A_1, A_3, and B_1 are all known functions of topology and a given choice of switching frequency (i.e., Γ). By then substituting C_0^* into (47), we obtain the corresponding inductance value, L^*, that maintains $f_{sw,0}$ while minimizing passive volume.

Back substituting (55) into (53) and replacing q_{HI} using (2) yields the minimal achievable total passive component volume,

$$\mathrm{Vol_{tot}^*} = \frac{P_{HI}}{f_{sw}\,\rho_C} \left(\frac{A_2}{2} + \sqrt{A_1\left(\frac{1}{4}A_3 + \frac{\rho_C}{\rho_L} B_1\right)}\right). \tag{56}$$

Furthermore, (56) can be normalized with respect to power throughput, natural resonant switching frequency $f_{sw,0}$ (as per (15)), and capacitor energy density ρ_C. The resulting normalized minimum total passive component volume, M_{vol}^*, may be used to directly compare different topologies and is solely a function of the above-resonance parameter, Γ; the ratio of passive densities, ρ_C/ρ_L; and invariant topological parameters:

$$M_{vol}^* = \frac{\mathrm{Vol_{tot}^*}}{\left(\frac{P_{HI}}{f_{sw,0}\,\rho_C}\right)} = \frac{1}{\Gamma}\left(\frac{A_2}{2} + \sqrt{A_1\left(\frac{1}{4}A_3 + \frac{\rho_C}{\rho_L} B_1\right)}\right). \tag{57}$$

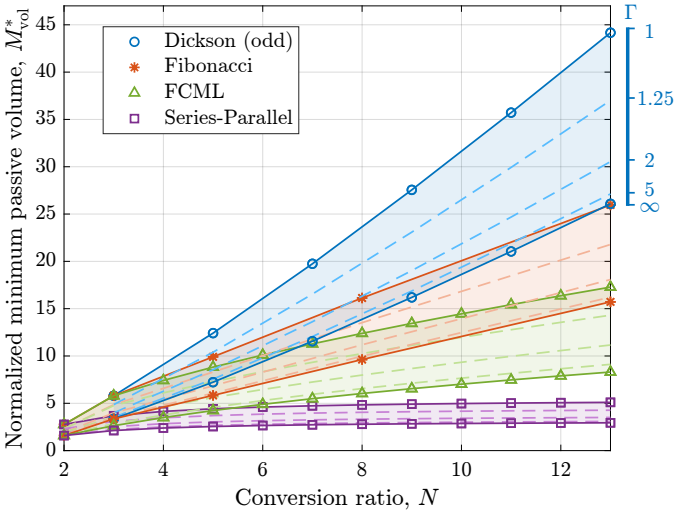


Fig. 7. Normalized minimum total passive volume versus conversion ratio for $\rho_C/\rho_L = 100$, and $1 \le \Gamma < \infty$. The range of Γ is annotated for the Dickson topology only, but applies similarly for all topologies plotted. For $\Gamma > 5$, diminishing ripple reductions result in minimal reductions in volume.

This is a similar normalized passive volume metric as obtained in [12], but now includes terms accounting for above resonance operation. The normalized minimum passive volume is visualized across a range of conversion ratios, N, in Fig. 7 for the Dickson (odd), Fibonnaci, FCML, and series-parallel topologies depicted in Fig. 1. The relative energy density ratio of capacitors to inductors in this plot is chosen as $\rho_C/\rho_L = 100$, following the empirical scaling trends analyzed in [1]. As the switching frequency is increased above resonance, the minimum passive volume also decreases due to a reduction in peak voltage and current ripple. However, as Γ is increased further the reduction in minimum passive volume becomes relatively small as ripple becomes negligible relative to dc values.

One additional consideration not captured in the preceding analysis is capacitor-ripple-induced clamping—operation where capacitor voltage ripple imposes a reverse voltage bias on inactive switches. This condition leads to reverse conduction in practice, resulting in unintended converter operation and significant losses. Detailed in [58] for the Dickson topology, here we record similar power limitations for the three remaining topologies in Table III. These limits are obtained by setting the flying capacitor voltage ripple—as related to load via (39) and (2)—equal to the maximum allowable ripple condition, i.e., the point at which unintended reverse conduction begins to occur. As expected, this constraint scales with input voltage, switching frequency, and C_0. Therefore, it could be beneficial to design with volume sub-optimal $C_0 > C_0^*$, so as to extend the load range in lower voltage

TABLE III
MAXIMUM POWER (VOLTAGE RIPPLE CONSTRAINED)

Topology	Maximum Power (P_{MAX})
Series-Parallel	$V_{\text{HI}}^2 C_0 f_{\text{sw}} \cdot \dfrac{2}{N(N-1)}$
FCML	$V_{\text{HI}}^2 C_0 f_{\text{sw}} \cdot \dfrac{1}{N}$
Dickson	$V_{\text{HI}}^2 C_0 f_{\text{sw}} \cdot \dfrac{2(N-1)}{N(N+1)}$
Fibonacci	$V_{\text{HI}}^2 C_0 f_{\text{sw}} \cdot \dfrac{2}{N F_{N_C+1}}$

applications subject to strict switching frequency constraints.

V. HARDWARE VALIDATION

The preceding analysis is applied to the design of a 5:1 (i.e., $N = 5$) FCML converter hardware prototype, whose schematic is depicted in Fig. 1b. The PCB, switches, and gate driving circuitry—depicted in Fig. 8 and listed in Table IV—are identical to the hardware demonstration in [21], while the passive components are replaced with values minimizing total passive volume. Switch operation is controlled in accordance with the clocking scheme depicted in Fig. 4. Table V defines this design example's chosen operating point. The target output power of $P_{\text{HI}} = V_{\text{HI}} \cdot I_{\text{HI}} = 77\,\text{W}$ corresponds to the demonstrated peak efficiency point in [21] when using the same switching devices at the same input voltage of $V_{\text{HI}} = 200\,\text{V}$. Similarly, $\Gamma = 1.25$ was selected, having demonstrated a good balance between switching and conduction losses in [21]. To emphasize achievable passive volume reductions, a modestly high switching frequency of $f_{\text{sw}} = 250\,\text{kHz}$ is chosen here, implying $f_{\text{sw,0}} = f_{\text{sw}}/\Gamma = 200\,\text{kHz}$.

We note that the choice of Γ, f_{sw} and the selected switch sizings largely dictate converter efficiency. Section VI presents a method to derive both peak blocking voltage, $V_{\text{ds,max}}$, and rms current, I_{rms}, for each switch as a function of Γ, which facilitates conventional loss estimation and optimization across frequency, with the effects of lage ripple behavior now fully modeled. However, a detailed loss assessment is beyond the scope of this work, with the following design example focusing on passive component volume only. In practice, the described design flow may be iterated in conjunction with complimentary large ripple enhanced loss calculations, allowing for comprehensive converter optimization that accurately captures the well known trade-off between passive component volume and converter efficiency.

Having specified an operating point in Table V, passive component volume is now calculated in accordance with Section IV. First, the high-side average charge $q_{\text{HI}} = 1.54\,\mu\text{C}$—as per (2), (6), and the relative phase durations are evaluated as $\tau_1 = 0.233$ and $\tau_2 = 0.178$ using (35) and (36). Temporarily setting $\Gamma = 1$ gives $\tau_1|_{\Gamma=1} = 0.243$ and $\tau_2|_{\Gamma=1} = 0.172$. Values for $\hat{\boldsymbol{a}}_{\text{C}}$, $\boldsymbol{c}$, $\boldsymbol{v}$, $\boldsymbol{a}_{\text{L}}$, and $\boldsymbol{\kappa}$ are retrieved from Table VIII. Subsequently, the requisite coefficients necessary to compute total

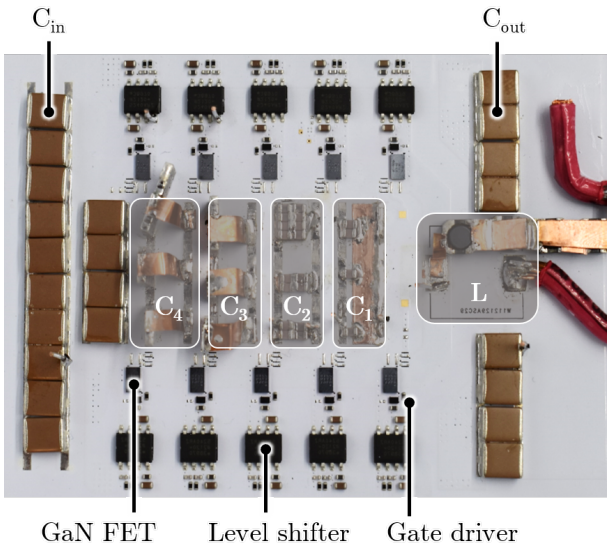


Fig. 8. Annotated photograph of the FCML converter used to validate the passive volume calculations. Constructed on a white soldermask, the hardware presented in [21] is modified to include the passive component cases depicted in Fig. 9.

TABLE IV
SWITCHING COMPONENT DETAILS

Component	Description	Part Name
$S_{\text{A}_{1-5}}$, $S_{\text{B}_{1-5}}$	100 V, 3.2 mΩ GaN-FET	EPC2218
Gate Driver	5 V, 7 A / 5 A	LMG1020
Isolator	Power and Signal	ADUM5240

passive volume using (53) are evaluated as $A_1 = 1.2$, $A_2 = 2$, $A_3 = 4$, and $B_1 = 0.537$. The only remaining unknowns are technology dependent passive energy densities, ρ_C and ρ_L, and the choice of C_0—whose minimizing expression C_0^* is given in (55).

To demonstrate that $C_0 = C_0^*$ results in minimized total passive component volume, three sets of passive components—depicted as Cases 1-3 in Fig. 9—were implemented in hardware. To ensure consistent energy densities ρ_{C} and ρ_{L} across all instances of the same passive type, regardless of value or applied bias, each passive component is constructed using series and/or parallel combinations of either a small unit capacitor or unit inductor. These unit elements, summarized in Table VI, both have competitive energy densities representative of their respective technologies [1]. A Class I MLCC capacitor (e.g., C0G/NP0) with $\rho_{\text{C}} = 8800\,\text{J/m}^3$ is used, given the stability, low loss, and achievable tolerances of these dielectrics in tuned ReSC designs [10]. Likewise, the unit inductance is a low loss stable ferrite with $\rho_{\text{L}} = 123\,\text{J/m}^3$. Using these densities, the prescribed operating parameters, and (55), the normalizing capacitance value minimizing total passive component volume is found to be $C_0^* = 44\,\text{nF}$, with associated inductance $L^* = 3.4\,\mu\text{H}$ using (47). Last, having obtained C_0^*, Table III is consulted to ensure that the target power of 77 W does not exceed the capacitor ripple limitation.

TABLE V
SPECIFIED 5:1 FCML CONVERTER OPERATING POINT

Description	Parameter	Value
High-Side Voltage	V_{HI}	200 V
Power Level	P_{HI}	77 W
Switching Frequency	f_{sw}	250 kHz
Above Resonance	Γ	1.25

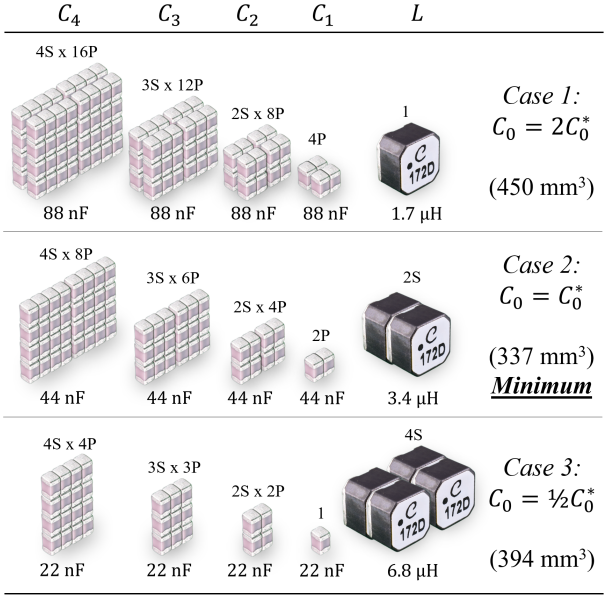


Fig. 9. The total passive component volume for three different 5:1 FCML converter solutions with identical resonant switching frequency. $P_{\text{HI}} = 77\,\text{W}$, $\Gamma = 1.25$, $f_{\text{sw}} = 250\,\text{kHz}$, $V_{\text{HI}} = 200\,\text{V}$. All components are depicted to relative scale. For Case 2, $C_0 = C_0^* = 44\,\text{nF}$, resulting in approximately minimal total component volume.

TABLE VI
UNIT PASSIVE COMPONENT DETAILS

Component	C	L
Description	C0G, 0805	Ferrite
Part Name	C2012C0G1H223J125AA	LPS5030-172
Ratings	22 nF, 50 V	1.7 µH, 3.3 A
Dimensions (mm)	2.00 × 1.25 × 1.25	5.00 × 5.00 × 3.00
Volume (mm³)	3.13	75.0
Density (J/m³)	8800	123

In this case, $P_{\text{MAX}} = 88\,\text{W}$ ensuring correct operation with a 10 % margin.

For each of the three cases in Fig. 9, values for both C_0 and L differ, but all cases express an identical natural resonant frequency, $f_{\text{sw},0}$, leading to the same switching frequency, f_{sw}, for a given Γ. Case 1 uses a capacitance C_0 twice as large as the minimizing value (i.e., $C_0 > C_0^*$), Case 2 uses the optimal design choice (i.e., $C_0 = C_0^*$), and Case 3 uses a capacitance C_0 half the minimizing value (i.e., $C_0 < C_0^*$).

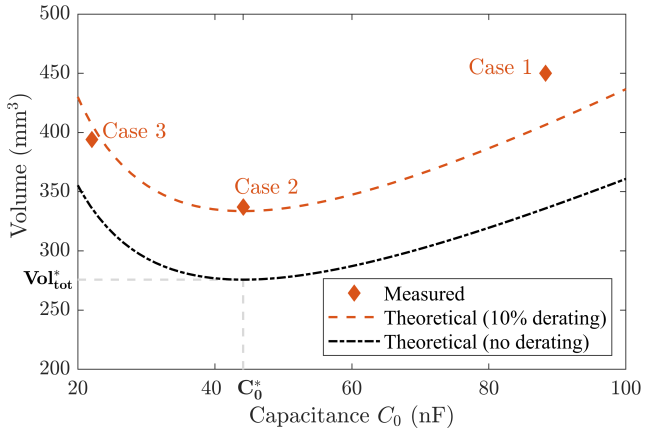


Fig. 10. Total measured passive volume versus C_0^* for three constructed cases, along with theoretically derived continuous functions of (53) with and without a 10% passive component derating. The error between measured and theoretical datapoints results from practical component rating availability. Minimizing capacitance C_0^* is highlighted, illustrating that even with imperfect component selection, a minimized result is still achieved.

Fig. 10 compares the resulting total passive volumes with the theoretically calculated volume using (53). The theoretical volume assumes all passives are rated at their precise maximum energy storage requirement, with no voltage or current derating, and a continuum of part availability. Conversely, the chosen unit inductor has a practical current derating of 2.9 A (instead of 3.3 A) to avoid saturation and ensure a stable inductance value. Similarly, while the flying capacitors nominally experience dc voltages in multiples of 40 V, a 50 V dielectric is chosen to accommodate each element's voltage ripple. Similar approximations are expected for practical design constraints and, as demonstrated in Fig. 10, lead to a realized passive volume inflated from the theoretical. However, the applied deratings do not significantly alter the optimal value of C_0^* and L^*, provided a similar degree of voltage/current margin is applied to both capacitors and inductors. To illustrate this, a 10 % derating is applied to each passive's voltage or current, which when squared in (40) and (49) gives a 21 % increase in expected volume. This modified theoretical result is also plotted in Fig. 10, showing closer agreement with volumes measured in practice.

Fig. 11 depicts measured flying capacitor voltage and inductor current waveforms at the described operating point with $C_0 = C_0^* = 44\,\text{nF}$ and $L = L^* = 3.4\,\mu\text{H}$. Taking measured peak inductor current, peak flying capacitors voltages, and applying $\frac{1}{2}LI_{\text{pk}}^2$ and $\frac{1}{2}C_0V_{\text{pk}}^2$ reveals total peak inductor and capacitor energies of $14.3\,\mu\text{J}$ and $1.4\,\text{mJ}$, respectively. Dividing by passive energy densities ρ_{L} and ρ_{C} yields the theoretically expected minimum volume of $\text{Vol}_{\text{tot}}^* = 275\,\text{mm}^3$, as predicted by (56) and plotted in Fig. 10, further validating the preceding analysis.

VI. SWITCH STRESS

Section IV and Section V aim to minimize total passive component volume of capacitors and inductors while assuming in practice these elements comprise the large majority of a converter's overall volume. However, this minimization may incur increased voltage and current ripple, which would

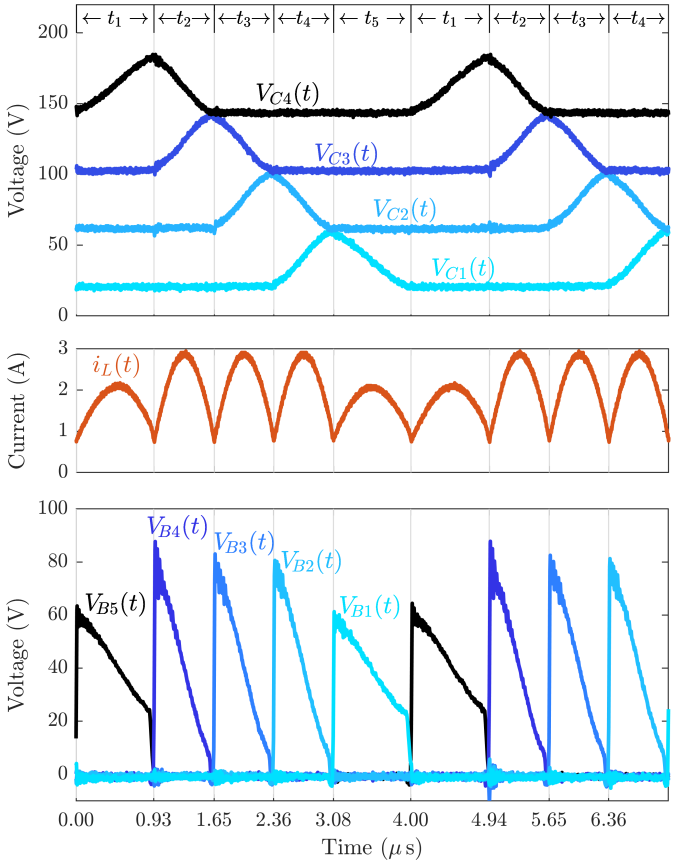


Fig. 11. Measured flying capacitor voltage waveforms (top), inductor current (middle), and switch voltages, V_{ds}, (bottom) for minimized volume Case 2, where $V_{\text{HI}} = 200\,\text{V}$, $P_{\text{HI}} = 77\,\text{W}$, $f_{\text{sw}} = 250\,\text{kHz}$, and $\Gamma = 1.25$. Switches are controlled in accordance with the clocking scheme depicted in Fig. 4 with phase timing durations calculated using (35) and (36). For each phase the inductor current waveform is a centered symmetric sinusoidal segment, further validating the zero volt-seconds per phase assumption.

subsequently be imposed on the adjacent switching devices. This in turn may lead to increased switch stress, resulting in volume/loss increases within the active devices. One conventional metric characterizing switch stress is the volt-amp (VA) product [2], [12], [22], [74]. This metric assumes linear device scaling and commonly serves as a proxy for total switching device area and/or loss in a given converter when summed across all switching devices. That is, an improved VA rating translates to a smaller and/or more efficient power converter. In this work, we propose a VA metric that takes into account the full effect of the inductor current and capacitor voltage ripples, improving upon calculations presented in past literature by providing a metric with greatly increased fidelity.

A. Current Stress

Rather than using average current for the total VA rating, as in [2], [12], here we calculate the rms current through each switch—for both at- and above-resonance operation—using the inductor current waveform derived in Section III. Utilizing rms current is similar to the analysis performed in [20], [37] and captures conduction losses, thermal requirements, and the effects of operating frequency on switch current ripple.

The normalized charge flow, $a_{\text{s},ji}$, through the ith switching device is obtained using the procedure described in Section II-A and the results for four topologies are recorded in Table VIII where switches adhere to the naming convention depicted in Fig. 1. In phase j, the ratio of the peak current through switch S_i relative to the peak inductor current, as defined in (48), is equivalent to the ratio of respective charge flow, or

$$\frac{I_{\text{pk,s}_i,j}}{I_{\text{pk},j}} = \frac{a_{\text{s},ji}}{a_{\text{L},j}}. \tag{58}$$

For each switch, S_i, the total rms current in a switching period is constructed from a squared sum of per-phase rms currents as

$$\begin{aligned} I_{\text{rms,s}_i} &= \sqrt{\frac{1}{T_{\text{sw}}}\int_0^{T_{\text{sw}}} i_{\text{s}_i}^2(t)\,dt} \\ &= \sqrt{\frac{1}{T_{\text{sw}}}\sum_{j=1}^{N_{\text{P}}}\int_{-\frac{t_j}{2}}^{\frac{t_j}{2}} \left(I_{\text{pk,s}_i,j}\cos(\omega_{0,j}\,t)\right)^2\,dt} \\ &= \frac{I_{\text{HI}}}{2}\sqrt{\frac{\pi}{\Gamma}\sum_{j=1}^{N_{\text{P}}}\frac{a_{\text{s},ji}^2}{\tau_j|_{\Gamma=1}}\cdot\left(\frac{\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}+\sin\left(\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}{1-\cos\left(\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}\right)} \end{aligned} \tag{59}$$

where (16) and (19) are substituted for t_j and $\omega_{0,j}$, respectively, and q_{HI} is substituted for the high-side input current, I_{HI}, using (2). A similar analytical expression for the inductor current rms may be derived as

$$I_{\text{rms,L}} = \frac{I_{\text{HI}}}{2}\sqrt{\frac{\pi}{\Gamma}\sum_{j=1}^{N_{\text{P}}}\frac{a_{\text{L},j}^2}{\tau_j|_{\Gamma=1}}\cdot\left(\frac{\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}+\sin\left(\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}{1-\cos\left(\frac{\pi}{\Gamma}\cdot\frac{\tau_j}{\tau_j|_{\Gamma=1}}\right)}\right)}. \tag{60}$$

Interestingly, both the switch and inductor rms currents are independent of both C_0 and f_{sw}, varying only with Γ and I_{HI}. For all two-phase converters, the normalized phase durations are invariant to Γ (i.e., $\tau_j = \tau_j|_{\Gamma=1}$) leading to further simplification of (59) and (60). In all cases an increase in Γ results in reduced rms currents, as expected.

The results in (59) and (60) have been validated using the measured inductor current waveforms presented in Fig. 11, where switch current waveforms can be extracted from $i_{\text{L}}(t)$ on a phase-by-phase basis.

B. Voltage Stress

Prior work in [2], [12], [20], [37], only calculated switch voltage stresses based on the mid-range capacitor voltages, thereby neglecting the effects of capacitor voltage ripple. In this analysis, the peak voltage indicates switch stress, and more fairly characterizes the performance of switches under the large ripple conditions typical in converters designed for minimized passive volume.

When a switch is disabled, its blocking voltage, $V_{\text{ds},i}$, is dictated by proximal flying capacitors. In every phase, large-signal KVL is applied to obtain expressions for the voltage imposed upon each switch, inclusive of flying capacitor voltage ripple. However the phase and time of occurrence for the peak blocking voltage in each switch is not immediately obvious by inspection. For the ReSC topologies presented in

this work, the maximum (or minimum) of V_{ds} in each phase occurs either at its beginning, j_{start}, or end, j_{end}. Therefore the instantaneous blocking voltage immediately before and after each phase transition must be investigated, after which the maximum value is recognized.

Using the 5:1 FCML converter depicted in Fig. 4 as an example, at the start of phase 1 switch S_{B5} experiences a blocking voltage of

$$V_{\text{ds,B}_5}\Big|_{(j=1)_{\text{start}}} = V_{\text{HI}} - \left(V_{\text{HI}} v_4 - \frac{1}{2}\Delta v_{\text{pp},4}\right) \tag{61}$$

whereas at the end of phase 1 switch S_{B5} experiences

$$V_{\text{ds,B}_5}\Big|_{(j=1)_{\text{end}}} = V_{\text{HI}} - \left(V_{\text{HI}} v_4 + \frac{1}{2}\Delta v_{\text{pp},4}\right) \tag{62}$$

where v_4 is the normalized mid-range voltage of capacitor C_4 and its voltage ripple $\Delta v_{\text{pp},i}$ is defined by (39). In this case (61) clearly expresses the peak blocking voltage condition in phase 1. Continuing the analysis for every phase shows (61) is also the maximum switch voltage stress, $V_{\text{ds,max,B}_5}$, for switch B_5 over the entire switching period.

This search is expanded to all switches, where phases in which a switch is turned on may be ignored since these switches will have 0 V across them. For convenience, Table VII documents the generalized result for peak voltage stress on each switching element for four common topologies. The calculated peak blocking voltage for the FCML topology is validated against the measured V_{ds} waveforms depicted in Fig. 11 for switches $S_{\text{B},1-5}$.

C. Total VA Switch Rating

To compute a converter's total VA rating, the rms current of each switch is multiplied by its corresponding peak voltage, before summing across all elements:

$$\text{VA}_{\text{tot}} = \sum_{i=1}^{N_{\text{S}}} V_{\text{ds,max},i} \cdot I_{\text{rms},i}. \tag{63}$$

In choosing C_0 to minimize the total passive volume (i.e. $C_0 = C_0^*$), (55) can be substituted into the $V_{\text{ds,max}}$ expressions listed in Table VII. Here it becomes apparent V_{HI} can be factored out of all $V_{\text{ds,max}}$ expressions. Similarly, the high-side current, I_{HI}, is a factor of I_{rms}, as per (59). Subsequently, the VA rating in (63) can be normalized with respect to input power, $P_{\text{HI}} = V_{\text{HI}} I_{\text{HI}}$, yielding a metric, M_{VA}^*, independent of power level or switching frequency

$$M_{\text{VA}}^* = \frac{\text{VA}_{\text{tot}}}{V_{\text{HI}} I_{\text{HI}}} \tag{64}$$

and can be used to directly compare the switch utilization of different ReSC topologies. Trade-offs between this normalized switch stress metric and the normalized minimimum passive volume, M_{vol}^* are visualized in Section VII.

TABLE VII
MAXIMUM SWITCH VOLTAGE STRESS

	$V_{\text{ds,max},i}$	
Series-Parallel		
S_{T_i}	$\frac{i}{N}V_{\text{HI}} + \frac{i}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le N_{\text{C}}\}$
S_{B_i}	$\frac{i}{N}V_{\text{HI}} + \frac{N-i}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le N_{\text{C}}\}$
S_{M_i}	$\frac{1}{N}V_{\text{HI}} + \frac{1}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le N_{\text{C}}\}$
S_{H}	$\frac{N-1}{N}V_{\text{HI}} + \frac{1}{2}\frac{q_{\text{HI}}}{C_0}$	
FCML		
S_{A_i}	$\frac{1}{N}V_{\text{HI}} + \frac{q_{\text{HI}}}{C_0}$	$i \in \{2 \le \mathbb{N} \le N-1\}$
	$\frac{1}{N}V_{\text{HI}} + \frac{1}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1, N\}$
S_{B_i}	$\frac{1}{N}V_{\text{HI}} + \frac{q_{\text{HI}}}{C_0}$	$i \in \{2 \le \mathbb{N} \le N-1\}$
	$\frac{1}{N}V_{\text{HI}} + \frac{1}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1, N\}$
Dickson		
S_{B_i}	$\frac{1}{N}V_{\text{HI}} + \frac{1}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le 4\}$
S_{S_i}	$\frac{2}{N}V_{\text{HI}} + \frac{1}{N-1}\frac{q_{\text{HI}}}{C_0}$	$i \in \{2 \le \mathbb{N} \le N-1\}$
	$\frac{1}{N}V_{\text{HI}} + \frac{1}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1, N\}$
Fibonacci		
S_{T_i}	$\frac{F_{(i+1)}}{N}V_{\text{HI}} + \frac{F_{(N_{\text{C}}-i+1)}}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le N_{\text{C}}\}$
S_{B_i}	$\frac{F_i}{N}V_{\text{HI}} + \frac{F_{(N_{\text{C}}-i+2)}}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le N_{\text{C}}\}$
S_{M_i}	$\frac{F_{(i+1)}}{N}V_{\text{HI}} + \frac{F_{(N_{\text{C}}-i+1)}}{2}\frac{q_{\text{HI}}}{C_0}$	$i \in \{1 \le \mathbb{N} \le N_{\text{C}}\}$
S_{H}	$\frac{F_{N_{\text{C}}}}{N}V_{\text{HI}} + \frac{F_1}{2}\frac{q_{\text{HI}}}{C_0}$	

VII. DISCUSSION

The previous sections describe a comprehensive large-signal assessment of ReSC converters when operating in periodic steady-state, either at or above resonance. Section IV derived a normalized minimum total passive volume metric, M_{vol}^*, in (57), while Section VI derived a normalized total switch stress, M_{VA}^*, in (64). These normalized metrics at the minimum volume are evaluated in Fig. 12 for an example $N = 5$ conversion ratio and $\rho_{\text{C}}/\rho_{\text{L}} = 100$—a conservative representation of the peak capabilities of Class I ceramic capacitors (e.g., C0G) and ferrite inductors. Here each topology can be compared across the full range of possible switching frequencies, from resonant to above resonant operation ($1 \le \Gamma < \infty$). For a decided Γ, converters with smaller M_{vol}^* and M_{VA}^* are expected to offer improved performance, with both a reduced minimum passive volume and VA rating.

In Fig. 12, each topology is visibly differentiated when considering its M_{vol}^* versus M_{VA}^*, indicating a quantitative measure of design trade-offs. For example, the Dickson topology exhibits the lowest M_{VA}^*, suggesting improved efficiency when total switch volume/area is constrained. Viewed differently, for the same conversion efficiency across all four topologies, the Dickson converter's switches are expected to realize a smaller total footprint area/volume. Conversely, the Dickson requires a greater total passive volume than the other topologies when operated at the same power level. The series-parallel topology exists on the opposite extreme: trading worsened total switch stress for superior total passive volume.

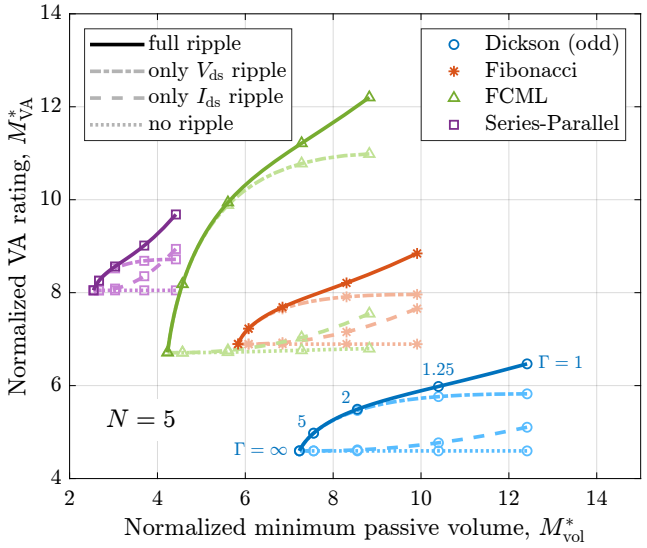


Fig. 12. Normalized switch VA rating versus normalized minimum total passive volume, using $\rho_C/\rho_L = 100$. Each curve describes a sweep of $1 \leq \Gamma < \infty$ where the rightmost point on each curve is $\Gamma = 1$. Also plotted is the result when inductor current ripple and/or capacitor voltage ripple are neglected from the switch stress calculations (dashed), as per conventional analysis using small ripple approximations.

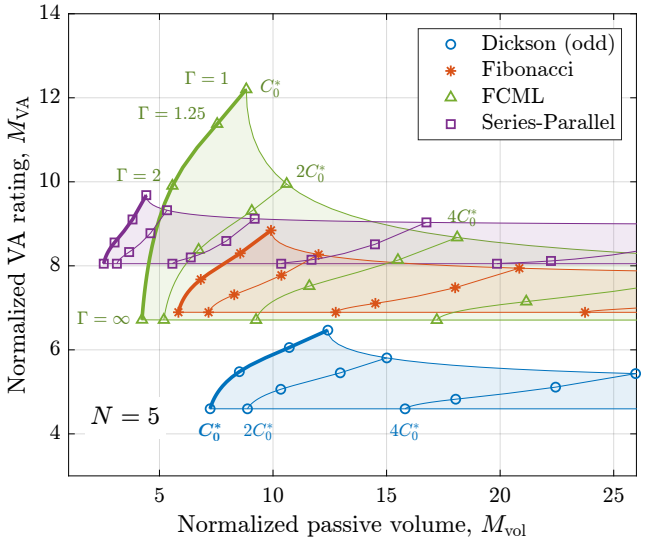


Fig. 13. Normalized switch VA rating versus normalized total passive volume with relative energy density ratio $\rho_C/\rho_L = 100$. Full ripple is assumed on all passives for improved accuracy. Added curves demonstrate a reduction in total switch stress with increasing passive volume within a given converter solution.

The FCML and Fibonacci converters lie between these two extremes. For all converters, both VA rating and passive volume decrease with increasing Γ, due to reduced inductor current and capacitor voltage ripple. However, while the VA rating provides a correlative proxy for the relative switching losses between a set of converter topologies at a given switching frequency, it does not include a frequency dependent term and thus increasing Γ does not directly translate to both a smaller and more efficient converter design. Instead, the VA rating in Fig. 12 should be viewed as informing the *relative* loss dissipation between topologies at a specified switching frequency, where total loss estimates are calculated separately. The choice of a specific switching frequency is dictated by conventional loss calculations (e.g., [13], [22]), which can now be augmented with the rms of complete current waveforms and ripple enhanced blocking voltages, as derived in Section VI.

To further emphasize the improved fidelity of the presented analysis, Fig. 12 also depicts the resulting curves if either capacitor voltage ripple, inductor current ripple, or both are neglected in the calculation of M^*_{VA}. In the "no ripple" case, the switch voltage is calculated using the mid-range capacitor voltages only, neglecting capacitor and therefore switch voltage ripple. Likewise, the switch rms current is calculated assuming a constant current through the inductor, equal to the low-side current. The "only V_{ds} ripple" case calculates switch voltage including the peak voltage across the switches, while the "only I_{ds} ripple" case calculates the rms of the switch current including the sinusoidal ripple on the inductor current. The "full ripple" case includes the effects of capacitor voltage and inductor current ripples on both the switch voltage and rms current, giving the highest accuracy. The inclusion of voltage ripple in the switch stress calculation is significant, with the FCML converter seeing almost double the switch stress when at resonance (i.e., $\Gamma = 1$) compared to the calculated result when large-signal ripple is neglected. This reveals fully resonant FCML converters may not offer the best trade-off between passive volume and VA rating, motivating further investigation of the Fibonacci converter where applicable.

While Fig. 12 depicts solutions for the minimized total passive volume, it may be preferable to deliberately increase this volume to alleviate switch stress (volume versus efficiency trade-off) or to extend the power range as per Table III. This expanded degree of design is illustrated in Fig. 13 where added C_0 contours in multiples of $2^n\, C_0^*$ demonstrate alternative valid operating solutions, with their corresponding switch stress and passive volume. For all topologies and provided a constant Γ, increasing the normalized capacitance above the minimizing value of C_0^* results in reduced VA rating as capacitor voltage ripple is reduced, albeit with diminishing returns for $C_0 > 2C_0^*$. Furthermore, although not shown, operating with a normalized capacitance less than the minimizing value C_0^* has no theoretical benefit as it results in an increased passive volume, an increased VA rating, and a reduction in the achievable power throughput as a result of switch voltage clamping. Therefore, the value of C_0^* minimizing the passive volume also represents a minimum desirable choice of C_0.

As can be observed from Fig. 13, different topologies experience varied reductions in normalized VA rating for the same relative increase in the chosen C_0. For example, of the four topologies, the FCML sees the most dramatic reduction in VA rating, given a doubling of C_0, whereas the series-parallel sees a much more modest decrease in VA for the same increase in capacitance.

Additionally, while an energy density ratio of $\rho_C/\rho_L = 100$ was chosen for these comparisons, this ratio can vary for different capacitor and inductor technologies, as described in [1]. For example, Class II ceramic capacitors (e.g., X5R) can exhibit a much higher energy density ratio of $\rho_C/\rho_L = 1000$ relative to ferrite or powder iron inductors, and therefore may be desirable in applications that priortize power density, provided their worsened dielectric tolerances are addressed.

Finally, the optimal topology choice for a given application is dependent on available component technologies and the desired trade-off between power density and efficiency—a classic design trade-off. Assisting this design effort, the discussed framework provides a set of foundational analytical tools required for comprehensive large-signal design.

VIII. Conclusion

The metrics of VA switch stress and minimized passive component volume are highly informative to the designer when making a topology selection and designing a high-density power converter. However, with more phases and components, determining these metrics for ReSC converters becomes increasingly tedious. This work presents a concise and direct framework based on component peak energy for analyzing ReSC converters both at and above resonance, with generalized topology dependent vectors recorded in Table VIII for convenience. In addition to providing appropriate phase durations for minimized rms currents, Section III further describes a simple method to realize the complete inductor current waveform, allowing not only accurate peak required energies to be calculated, but also more accurate core losses to be calculated. In addition, Table III documents each converter's maximum allowable power throughput as dictated by unintended reverse conduction in switches with increased flying capacitor voltage ripple. Section VI calculates each switch's rms current, which can be further applied to estimation of switch-induced conduction loss; and the peak switch voltages, accounting for large voltage ripple, which can be used to accurately calculate C_{OSS}-related switching loss. Furthermore, the presented framework significantly increases the calculation fidelity of large signal operating points, while also offering the steps necessary for further improved loss calculation.

Appendix A

Throughout this work, the inductor is assumed to experience zero volt-seconds within each phase, implying the inductor current follows a centered, symmetric sinusoidal segment, beginning and ending each phase with the same current, and with the peak current occurring at the exact center of each phase. Subsequently the relative phase durations, $\boldsymbol{\tau}$, resulting from this assumption were calculated in a simplified manner, as shown in (20)-(23) and tabulated in Table VIII.

However, if the assumption of per-phase zero volt-seconds is relaxed, then the inductor current waveform is not necessarily per-phase symmetric. Equations (20)-(23) must then be re-derived in a more generalized form to account for the possibility of some non-zero arbitrary phase shift, θ_j, in each phase j.

Consider a generic resonant current waveform during phase j with peak $I_{\text{pk},j}$ and arbitrary phase shift θ_j

$$i_{\text{L},j}(t) = I_{\text{pk},j}\cos\left(\omega_{0,j}t + \theta_j\right). \tag{65}$$

The charge accumulated throughout this phase j of duration t_j is then

$$\begin{aligned} q_{\text{L},j} &= \int_{-\frac{t_j}{2}}^{\frac{t_j}{2}} I_{\text{pk},j}\cos(\omega_{0,j}t + \theta_j)\ dt \\ &= \frac{2I_{\text{pk},j}}{\omega_{0,j}}\sin\left(\omega_{0,j}\frac{t_j}{2}\right)\cos(\theta_j). \end{aligned} \tag{66}$$

The phase-to-phase continuity equation at the transition between phase j and phase $j+1$ previously presented in (20) can now also be updated to include θ_j, and is given by

$$I_{\text{pk},j}\cos\left(\omega_{0,j}\frac{t_j}{2} + \theta_j\right) = I_{\text{pk},j+1}\cos\left(\omega_{0,j+1}\frac{-t_{j+1}}{2} + \theta_{j+1}\right). \tag{67}$$

Substituting (66) into (67) as before gives the same form as (23), but this expression now accounts for arbitrary phase shifts:

$$\begin{aligned} &\frac{q_{\text{L},j}\,\omega_{0,j}\cos\left(\omega_{0,j}\frac{t_j}{2} + \theta_j\right)}{2\cos(\theta_j)\sin\left(\frac{\omega_{0,j}t_j}{2}\right)} \\ =&\frac{q_{\text{L},j+1}\,\omega_{0,j+1}\cos\left(\omega_{0,j+1}\frac{-t_{j+1}}{2} + \theta_{j+1}\right)}{2\cos(\theta_{j+1})\sin\left(\frac{\omega_{0,j+1}t_{j+1}}{2}\right)}, \quad \forall j \le N_{\text{P}}. \end{aligned} \tag{68}$$

Applying this equation to all pairs of adjacent phases ensures both inductor charge balance and current continuity. Therefore, any values of θ_j satisfying this system of equations represent possible valid inductor current waveshapes for a ReSC converter.

Next, we determine whether any non-zero solutions for θ_j exist when implementing the phase timings derived under the assumption that all $\theta_j = 0$; in other words, t_j and t_{j+1} are known inputs, derived as per Section III and recorded as $\boldsymbol{\tau}$ in Table VIII (normalized with respect to T_{sw}). For two-phase ReSC converters, substituting tabulated values for $\boldsymbol{a}_{\text{L}}$ and $\boldsymbol{\kappa}$ into (1) and (19), respectively, and multiplying the result of both, reveals that

$$q_{\text{L},1}\,\omega_{0,1} = q_{\text{L},2}\,\omega_{0,2}. \tag{69}$$

Similarly, substituting recorded values for $\boldsymbol{\tau}$ and $\boldsymbol{\kappa}$ into (16) and (19), respectively, gives

$$\omega_{0,1}\,t_1 = \omega_{0,2}\,t_2. \tag{70}$$

Substituting (69) and (70) into (68) reveals the solution

$$\theta_1 = -\theta_2 \tag{71}$$

where both the phase 1 / phase 2 and phase 2 / phase 1 transitions are considered. Thus the relative phase timings, $\boldsymbol{\tau}$, recorded in Table VIII correctly maintain both charge balance and inductor continuity. However, there exists a continuum of non-zero θ_j for which these conditions are satisfied. Moreover, unless $\theta_1 = 0$, zero volt-seconds per phase is not achieved.

However, knowing $\cos(\theta_1) = \cos(|\theta_2|)$ and substituting (71) into (66) reveals that the peak per-phase currents $I_{\text{pk},j}$ and $I_{\text{pk},j+1}$ scale with non-zero θ_j, suggesting the zero-phase solution, $\theta_j = 0$, represents a point of convergence in the presence of any real loss. To see this, the per-phase charge

TABLE VIII
CHARACTERISTIC VECTORS FOR FOUR COMMON RESC TOPOLOGIES

Topology	**Series-Parallel** $N \in \{\mathbb{N} \geq 2\}$	**FCML** $N \in \{\mathbb{N} \geq 2\}$	**Dickson** $N \in \{\text{odd } \mathbb{N} \geq 3\}$	**Fibonacci** $N \in \{F_m \,:\, m \in \mathbb{N} \geq 3\}$, $F_x = (1, 1, 2, 3, 5, 8, 13, ...)$
N_P	2	N	2	2
N_C	$N-1$	$N-1$	$N-1$	$m-2$
N_S	$3N-2$ $N_{\text{S}_\text{B}} = N_{\text{S}_\text{M}} = N_{\text{S}_\text{T}} = N_\text{C}$ $N_{\text{S}_\text{I}} = 1$	$2N$ $N_{\text{S}_\text{M}} = N_{\text{S}_\text{T}} = N$	$N+4$ $N_{\text{S}_\text{S}} = N$ $N_{\text{S}_\text{B}} = 4$	$3N_\text{C}+1$ $N_{\text{S}_\text{B}} = N_{\text{S}_\text{M}} = N_{\text{S}_\text{T}} = N_\text{C}$ $N_{\text{S}_\text{H}} = 1$
$\boldsymbol{a}_{\text{C}\,[N_\text{P}\times N_\text{C}]}$	$\begin{bmatrix} 1 & 1 & \cdots & 1 \\ -1 & -1 & \cdots & -1 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ -1 & 1 & \ddots & 0 & 0 \\ 0 & -1 & \ddots & 0 & 0 \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & \ddots & -1 & 1 \\ 0 & 0 & \cdots & 0 & -1 \end{bmatrix}$	$\begin{bmatrix} -1 & 1 & -1 & \cdots & 1 & -1 \\ 1 & -1 & 1 & \cdots & -1 & 1 \end{bmatrix}$	$\begin{bmatrix} -F_{N_\text{C}} & F_{(N_\text{C}-1)} & \cdots & \pm F_2 & \mp F_1 \\ F_{N_\text{C}} & -F_{(N_\text{C}-1)} & \cdots & \mp F_2 & \pm F_1 \end{bmatrix}$
$\boldsymbol{a}_{\text{L}\,[N_\text{P}\times 1]}$	$\begin{bmatrix} 1 \\ N_\text{C} \end{bmatrix}$	$\begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}$	$\begin{bmatrix} \frac{N+1}{2} \\ \frac{N-1}{2} \end{bmatrix}$	$\begin{bmatrix} F_{(N_\text{C}+1)} \\ F_{N_\text{C}} \end{bmatrix}$
$\boldsymbol{a}_{\text{S}_\boldsymbol{x}\,[N_\text{P}\times N_{\text{S}_\boldsymbol{x}}]}$	$\boldsymbol{a}_{\text{S}_\text{B}}: \begin{bmatrix} 0 & \cdots & 0 \\ 1 & \cdots & 1 \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{M}}: \begin{bmatrix} 1 & \cdots & 1 \\ 0 & \cdots & 0 \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{T}}: \begin{bmatrix} 0 & \cdots & 0 \\ 1 & \cdots & 1 \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{H}}: \begin{bmatrix} 1 \\ 0 \end{bmatrix}$	$\boldsymbol{a}_{\text{S}_\text{A}}: \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & 1 \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{B}}: \begin{bmatrix} 0 & 1 & \cdots & 1 \\ 1 & 0 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 1 \\ 1 & \cdots & 1 & 0 \end{bmatrix}$	$\boldsymbol{a}_{\text{S}_\text{S}}: \begin{bmatrix} 1 & 0 & 1 & \cdots & 0 & 1 \\ 0 & 1 & 0 & \cdots & 1 & 0 \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{B}}: \begin{bmatrix} \frac{N_\text{C}}{2} & 0 & \frac{N_\text{C}}{2} & 0 \\ 0 & \frac{N_\text{C}}{2} & 0 & \frac{N_\text{C}}{2} \end{bmatrix}$	$\boldsymbol{a}_{\text{S}_\text{B}}: \begin{bmatrix} F_{(N_\text{C}+1-i)} & 0 & F_{(N_\text{C}+1-i)} & \cdots \\ 0 & F_{(N_\text{C}+1-i)} & 0 & \cdots \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{M}}: \begin{bmatrix} 0 & F_{(N_\text{C}+1-i)} & 0 & \cdots \\ F_{(N_\text{C}+1-i)} & 0 & F_{(N_\text{C}+1-i)} & \cdots \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{T}}: \begin{bmatrix} F_{(N_\text{C}+2-i)} & 0 & F_{(N_\text{C}+2-i)} & \cdots \\ 0 & F_{(N_\text{C}+2-i)} & 0 & \cdots \end{bmatrix}$ $\boldsymbol{a}_{\text{S}_\text{H}}: \begin{bmatrix} F_1 \\ 0 \end{bmatrix}_{N_\text{C}\text{ is even}}$ or $\begin{bmatrix} 0 \\ F_1 \end{bmatrix}_{N_\text{C}\text{ is odd}}$
$\boldsymbol{v}_{[1\times N_\text{C}]}$	$\frac{1}{N}\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$	$\frac{1}{N}\begin{bmatrix} 1, & 2, & \cdots, & N_\text{C} \end{bmatrix}$	$\frac{1}{N}\begin{bmatrix} 1, & 2, & \cdots, & N_\text{C} \end{bmatrix}$	$\frac{1}{N}\begin{bmatrix} F_2, & F_3, & \cdots, & F_{(N_\text{C}+1)} \end{bmatrix}$
$\boldsymbol{c}_{[1\times N_\text{C}]}$	$\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$	$\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$	$\begin{bmatrix} \frac{N_\text{C}}{N_\text{C}}, & \frac{N_\text{C}}{2}, & \frac{N_\text{C}}{N_\text{C}-2}, & \frac{N_\text{C}}{4}, & \cdots, & \frac{N_\text{C}}{2}, & \frac{N_\text{C}}{N_\text{C}} \end{bmatrix}$	$\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$
$\boldsymbol{\kappa}_{[N_\text{P}\times 1]}$	$\begin{bmatrix} \frac{1}{N_\text{C}} \\ N_\text{C} \end{bmatrix}$	$\begin{bmatrix} 1 \\ 1/2 \\ 1/2 \\ \vdots \\ 1/2 \\ 1 \end{bmatrix}$	$\begin{bmatrix} \frac{N+1}{2} \\ \frac{(N-1)^2}{2(N+1)} \end{bmatrix}$	$\begin{bmatrix} \frac{F_{(N_\text{C}+1)}}{F_{N_\text{C}}} \\ \frac{F_{N_\text{C}}}{F_{(N_\text{C}+1)}} \end{bmatrix}$
$\boldsymbol{\tau}_{[N_\text{P}\times 1]}$	$\begin{bmatrix} \frac{1}{N} \\ \frac{N_\text{C}}{N} \end{bmatrix}$	$\begin{bmatrix} \text{Eqn. (35)} \\ \text{Eqn. (36)} \\ \text{Eqn. (36)} \\ \vdots \\ \text{Eqn. (36)} \\ \text{Eqn. (35)} \end{bmatrix}$	$\begin{bmatrix} \frac{N+1}{2N} \\ \frac{N-1}{2N} \end{bmatrix}$	$\begin{bmatrix} \frac{F_{(N_\text{C}+1)}}{F_{(N_\text{C}+2)}} \\ \frac{F_{N_\text{C}}}{F_{(N_\text{C}+2)}} \end{bmatrix}$
$\hat{\boldsymbol{a}}_{\text{C}\,[1\times N_\text{C}]}$	$\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$	$\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$	$\begin{bmatrix} 1, & 1, & \cdots, & 1 \end{bmatrix}$	$\begin{bmatrix} F_{N_\text{C}} & F_{(N_\text{C}-1)} & \cdots & F_2 & F_1 \end{bmatrix}$
A_1	$\frac{N-1}{N^2}$	$\frac{(N-1)(2N-1)}{6N}$	$\frac{N-1}{N^2}\left(\frac{N^2-1}{4} + \sum_{x=1}^{\frac{N-1}{2}} \frac{(2x-1)^2}{N+1-2x}\right)$	$\frac{1}{N^2}\left(F_{N_\text{C}+2}\,F_{N_\text{C}+1} - 1\right)$
A_2	$\frac{N-1}{N}$	$\frac{N-1}{2}$	$\frac{N-1}{2}$	$\frac{N_\text{C}+1}{5N}F_{N_\text{C}} + \frac{3N_\text{C}}{5N}F_{N_\text{C}+1}$
A_3	$N-1$	$N-1$	$\frac{N+1}{2}$	$F_{N_\text{C}}F_{N_\text{C}+1}$
B_1	$\frac{N-1}{4}\cdot\frac{1}{\sin^2\left(\frac{\pi}{2\Gamma}\right)}$	$\frac{1}{2}\cdot\frac{1}{\sin^2\left(\frac{\sqrt{2}-1}{N}\sin\left(\frac{\pi}{\Gamma}\right)+\frac{\pi}{2\Gamma}\right)}$	$\frac{N+1}{8}\cdot\frac{1}{\sin^2\left(\frac{\pi}{2\Gamma}\right)}$	$\frac{F_{N_\text{C}+1}F_{N_\text{C}}}{4}\cdot\frac{1}{\sin^2\left(\frac{\pi}{2\Gamma}\right)}$

in (66) is rearranged to provide an expression for the peak current

$$I_{\text{pk},j} = \frac{q_{\text{L},j}\,\omega_{0,j}}{2\cos(\theta_j)\sin\left(\frac{\omega_{0,j}t_j}{2}\right)}. \tag{72}$$

Here peak current is minimized when $\cos(\theta_j)$ is at its maximum value (i.e., when $\theta_j = 0$). This is visualized in Fig. 14a for an $N = 2$ FCML both at $\theta_j = 0$ and $\theta_j = \pi/8$ rad, where both waveforms satisfy charge balance and current continuity. From inspection, $\theta_j = 0$ minimizes the peak, peak-to-peak, and rms current. Therefore, similar to the conclusions in [72], we conjecture that parasitic loss mechanisms will minimize the circuit losses by ensuring that any inductor current initialized with some non-zero values of θ_j will converge to the zero phase shift condition ($\theta_j = 0$) in steady-state, implying a symmetrically centered current waveform in each phase and adherence to the per-phase zero volt-seconds assumption applied throughout the paper.

Finally, while zero inductor volt-seconds per phase (i.e., $\theta_j = 0$) is merely assumed for a general ReSC converter, for odd-N FCML converters this condition is necessary and corresponds to the only valid operating state where both steady-state charge balance and inductor current continuity are satisfied. To illustrate this, Fig. 14 plots steady-state inductor current waveforms for three conversion ratios, a) $N = 2$, b) $N = 3$, and c) $N = 4$, where for the FCML converter the conversion ratio also equals the number of phases, N_{P}. As is apparent in Fig. 14b for an odd value of N, non-zero values of θ_j will result in a current discontinuity, thus violating periodic steady-state. Therefore, for FCML converters with odd N, non-zero values of θ_j do not result in valid operating conditions, implying the inductor must experience zero volt-seconds within each phase in steady-state. This outcome further supports the conclusions made in [52], [75] and is observed experimentally in Section V where measured inductor current waveforms for $N = 5$ express near perfect zero volt-second per phase behaviour.

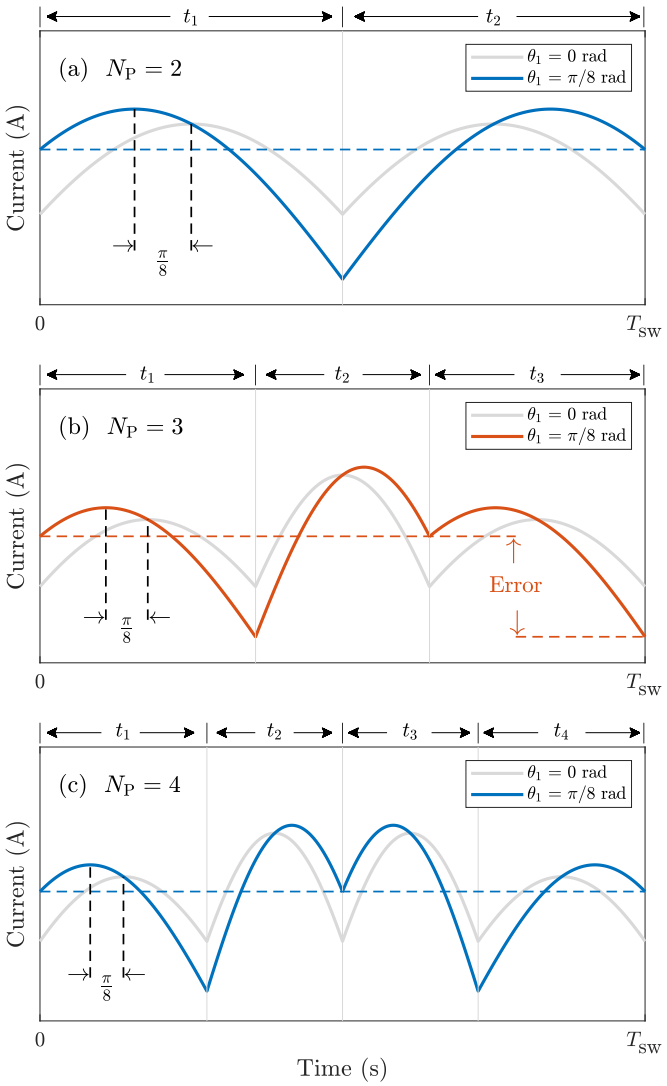


Fig. 14. Inductor current waveforms at $\Gamma = 1.5$ for an FCML converter with varied conversion ratio N and corresponding number of phases $N_{\text{P}} = N$. Sweeping phase angle θ between 0 rad and $\pi/8$ rad while constraining constant charge q_{L}—i.e., keeping the accumulated area in each phase fixed—demonstrates the peak, peak-to-peak, and rms currents are all minimized when $\theta_j = 0$. For *odd* N, inductor continuity cannot be satisfied for $\theta_j \neq 0$.

Appendix B

Section IV-A introduces a modified charge flow quantity, $\hat{a}_{\text{C},i}$, defined as the maximum deviation in stored charge on the i^{th} flying capacitor throughout a full switching cycle. This quantity is simplified for the ReSC cases presented in this work, however, a more generalized expression

$$\hat{a}_{\text{C},i} = \max_{x\in[N_{\text{P}}]}\left(\sum_{j=1}^{x} a_{\text{C},ji}\right) - \min_{x\in[N_{\text{P}}]}\left(\sum_{j=1}^{x} a_{\text{C},ji}\right) \tag{73}$$

is applicable to any charge flow vector, a_{C}, so long as it satisfies the periodic steady state condition in (3). The first term determines the peak positive (maximum) accumulated charge, while the second term determines the peak negative (minimum) accumulated charge. The difference between these values is the peak-to-peak charge ripple experienced by the capacitor.

Consider an example calculation of $\hat{a}_{\text{C},1}$ for a capacitor C_1 that experiences some arbitrary normalized capacitor charge flow vector

$$a_{\text{C},1} = \frac{q_{\text{C},1}}{q_{\text{HI}}} = \begin{bmatrix} 1 & -1 & -1 & 1 \end{bmatrix}. \tag{74}$$

A possible capacitor current waveform, $i_{\text{C},1}(t)$, corresponding to this charge vector, and its associated voltage waveform, $v_{\text{C},1}(t)$, are shown in Fig. 15, where a constant current during each phase is assumed for simplicity. The capacitor voltage ripple is centered around the mid-range voltage, V_{C_1}, while the capacitor current is centered around zero to satisfy periodic steady-state conditions. The charge expelled or received per phase corresponds to the area under the current waveform during that phase, and has a magnitude of q_{HI} as per (1).

By inspecting Fig. 15 or evaluating (73), we can determine that the peak positive accumulated charge occurs at the end of phase $j = 1$, and the peak negative accumulated charge occurs

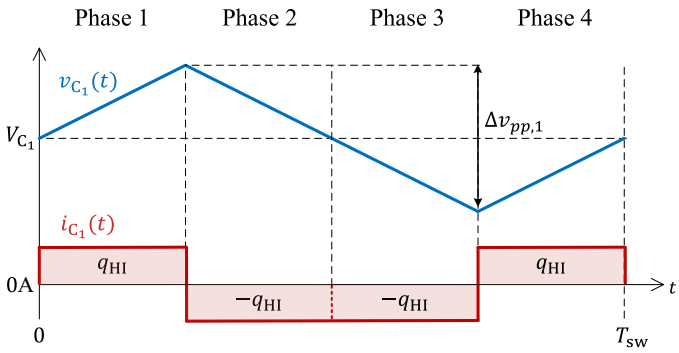


Fig. 15. Exemplar capacitor voltage and current waveforms for the given normalized charge flow vector $a_{C,1}$ in (74). The capacitor is charged by quantity q_{HI} in phases 1 and 4, and discharged by quantity $-q_{HI}$ in Phases 2 and 3. For simplicity, constant capacitor current and linear capacitor voltage are shown.

at the end of phase $j = 3$.

$$\max_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right) = \sum_{j=1}^{1} a_{C,ji} = 1 \tag{75}$$

$$\min_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right) = \sum_{j=1}^{3} a_{C,ji} = -1. \tag{76}$$

Therefore, the modified charge quantity for this example evaluates to

$$\begin{aligned}\hat{a}_{C,1} &= \max_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right) - \min_{x\in[N_P]}\left(\sum_{j=1}^{x} a_{C,ji}\right)\\ &= 1-(-1) = 2.\end{aligned}$$

This value can then be substituted into (39) to find the peak-to-peak voltage ripple, $\Delta v_{pp,1}$, for capacitor C_1 (also depicted in Fig. 15).

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Nathan Miles Ellis (Member, IEEE) was born in Cork, Ireland. He received the B.S. degree in Electrical and Electronic Engineering from the University College Cork, Ireland, in 2013, and the M.S. and Ph.D degrees in Electrical and Computer Engineering from the University of California, Davis in 2017 and 2020 respectively. During this time he was funded in part by both Texas Instruments and the U.S. Dept. of Education in recognition of research excellence in areas of national need.

Dr. Ellis is currently a Post-Doctoral Researcher at the University of California, Berkeley within the Department of Electrical Engineering and Computer Sciences. His primary area of research is power electronics. His interests include vehicle electrification, renewable energy integration, datacenter power delivery, biomedical devices, energy harvesting, mixed signal integrated circuit design, control and circuit techniques. Dr. Ellis was named Best Graduate Researcher by UC Davis' Industrial Affiliates in 2017, before receiving the title of Analog Devices Outstanding Student Designer at the International Solid-State Circuits Conference (ISSCC) in 2020. He has received an IEEE best paper award.

Nathan Charles Brooks (Student Member, IEEE) received the B.S. degree in electrical engineering from the Rose-Hulman Institute of Technology, Terre Haute, IN, USA, in 2016, and the M.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign, IL, USA, in 2018. He is currently working toward the Ph.D. degree in electrical engineering at the University of California at Berkeley, CA, USA. His research interests include dynamic modeling of switched circuits, high-performance circuit layout, passive component characterization, and high-density design of single-phase and multilevel power converters.

Margaret E. Blackwell (Student Member, IEEE) received the B.S. degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 2017 and the M.S. degree in electrical engineering and computer sciences in 2019 from the University of California, Berkeley, CA, USA, where she is currently working toward the Ph.D. degree in electrical engineering. Her research interests include hybrid switched-capacitor circuits focusing on the modeling and implementation of resonance operation, soft-switching techniques, and EMI mitigation strategies. Ms. Blackwell is a 2019 NSF Graduate Research Fellow.

Rose A. Abramson Rose A. Abramson (Student Member, IEEE) received the B.S. and M.Eng. degrees in electrical engineering in 2015 and 2016, respectively, from the Massachusetts Institute of Technology, Cambridge, MA, USA. Since 2018, she has been working towards the Ph.D. degree in electrical engineering with the University of California, Berkeley, Berkeley, CA, USA. In between receiving her M.Eng. and starting her Ph.D., she worked at an electric vehicle startup and then later with Lutron Electronics, Inc. developing offline LED drivers. Her current research focus includes hybrid and resonant switched-capacitor circuits and high performance dc–dc power conversion. Ms. Abramson is a 2019 NDSEG Fellow, and is also the recipient of the 2021 IEEE Joseph John Suozzi INTELEC Fellowship Award in Power Electronics.

Samantha Coday (Student Member, IEEE) received the B.S. degree in electrical engineering and mathematics from Southern Methodist University, TX, USA, in 2017. She received the M.S. and Ph.D degrees in electrical engineering and computer sciences from the University of California, Berkeley in 2019 and 2023 respectively. Her research interests include hybrid switched-capacitor circuits focusing on the design and implementation of converters in harsh aerospace environments. Dr. Coday has received the Outstanding Graduate Student Instructor Award at University of California, Berkeley, the Cadence Women in Technology Scholarship and the ThinkSwiss Research Scholarship.

Robert C. N. Pilawa-Podgurski (Senior Member, IEEE) (S'06–M'11–SM'19) was born in Hedemora, Sweden. He is currently an Associate Professor in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley. Previously, he was an Associate Professor in Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. He received dual B.S. degrees in physics and electrical engineering and computer science in 2005, the M.Eng. degree in electrical engineering and computer science in 2007, and the Ph.D. degree in electrical engineering in 2012, all from the Massachusetts Institute of Technology. He performs research in the area of power electronics, and enjoys snowboarding. His research interests include renewable energy applications, electric vehicles, CMOS power management, high density and high efficiency power converters, datacenter power delivery, and advanced control of power converters.

Dr. Pilawa-Podgurski served as the Student Activities Chair for IEEE Energy Conversion Congress and Exposition 2016 and 2017, and as the Technical Co-Chair for the 4th IEEE Workshop on Wide Bandgap Power Devices and Applications, 2016. From 2014 to 2022, he served the PELS Technical Committee 6 – Emerging Power Electronics Technologies as Awards Chair, Secretary, Vice Chair, and Chair. From 2016-2019 he served as Chair of PELS Technical Committee 2—Power Conversion Systems and Components. From 2014-2019, he served as Associate Editor for IEEE Transactions on Power Electronics, and for IEEE Journal of Emerging and Selected Topics in Power Electronics. From 2018-2023, he was a member of the IEEE ISSCC Power Management Committee.

Dr. Pilawa-Podgurski received the Chorafas Award for outstanding MIT EECS Master's thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. In 2015, he received the Air Force Office of Scientific Research Young Investigator Award, the UIUC Dean's Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, and the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017. He was the 2018 recipient of the IEEE Education Society Mac E. Van Valkenburg Award given for outstanding contributions to teaching unusually early in his career. In 2023, he received the UC Berkeley EECS department Electrical Engineering Outstanding Teaching Award. He is co-author of fourteen IEEE prize papers.