Reconfigurable Hybrid-Switched-Capacitor-Resonant LED Driver for Multiple Mains Voltages

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***Abstract*— This paper presents a hybrid-switched-capacitor-resonant (HSCR) light-emitting diode (LED) driver based on a stackable switched-capacitor (SC) converter IC rated for 15–20-W applications. Bulky transformers have been replaced with an SC ladder to perform high-efficiency voltage step-down conversion; an *LC*-resonant output network provides almost lossless current regulation and demonstrates the potential of capacitive galvanic isolation. The integrated SC modules can be stacked in the voltage domain to handle a large range of input voltage ranges that largely exceed the voltage limitation of the medium-voltage-rated 120-V silicon technology. The LED driver demonstrates >91% efficiency over a rectified input dc voltage range from 160 to 180 V_{dc} with two stacked ICs; using a stack of four ICs >89.6% efficiency is demonstrated over an input range from 320 to 360 V_{dc}. The LED driver can dim its output power to around 10% of the rated power while maintaining >70% efficiency with a pulsewidth modulation-controlled clock gating circuit.**

***Index Terms*— dc-dc power converters, light emitting diodes (LED), power integrated circuits, switched capacitor (SC) circuits, zero voltage switching (ZVS).**

I. Introduction

SOLID-STATE lighting has shown great promise as an efficient, environmentally friendly, and affordable alternative to incandescent and fluorescent lights. The engineering-economic analysis suggests light-emitting diode (LED) lighting is more cost-effective due to its high luminous efficacy and long life span, which significantly saves electric energy and reduces replacement cost. Thanks to their small form factor, LED bulbs with a small LED driver can be combined in many shapes in various applications to provide fantastic lighting effects.

Since an LED is a current-driven device whose light emission intensity is proportional to its forward conduction current, LED drivers are necessary to provide current regulation over a range of input and load conditions. A simple way to drive LEDs is to use a linear regulator. Compared with other topologies, linear regulators are often smaller in size without bulky magnetics, easier to design, and they emit little electromagnetic interference. However, the efficiency of linear regulators is inversely proportional to the conversion ratio and thus too low for most applications requiring high energy efficiency. Fig. 1(a) shows a linear LED driver that efficiently performs current regulation and power factor correction (PFC) by alternating the average load impedance with switches and multichannel LED strings [1]. Disadvantages of such a topology include difficulties in performing LED dimming and adapting to applications with various input or output specifications. Switched-mode LED drivers can achieve much higher power transfer efficiency than linear regulators by using passive energy storage devices and keeping the switch transistors in full-ON and full-OFF states most of the time. The buck-based LED driver, as shown in Fig. 1(b), is a widely used topology that can achieve higher efficiency (>90 %) and handle a wide range of input and loading conditions with a simple architecture. In [2], with a 5.5-mH inductor and a peak current-controlled pulsewidth modulation (PWM) method, the driver achieves >80 % efficiency and >0.9 power factor with large input and LED load variations. Despite its simple topology and good performance, the buck-based driver is not isolated from the ac mains, which can be a safety hazard in certain applications. In addition, the 5.5-mH inductor is large in size. To provide galvanic isolation, the most common solution is to use transformers. Fig. 1(c) shows the flyback-converter-based LED driver that is popular in low-to-moderate power applications [3]. The major drawback of the transformer-based LED driver is relatively large size and high cost due to the transformer, whose power handling capability is related to its volume. One example of the commercial flyback LED driver is shown in Fig. 2 [4], where the magnetic transformer takes up significant space onboard and cost around $2.

Switched-capacitor (SC) dc/dc converters provide another solution for high performance and highly integrated LED drivers. In comparison to magnetic-based converters, the SC topologies have a few fundamental advantages. As concluded in [5], any dc/dc converter must have at least two time-varying and/or nonlinear resistors (e.g., switches) and one reactance. The effectiveness of utilizing these two kinds of basic elements in a power converter decides its intrinsic performance-to-cost ratio. For integrated switching transistors, the cost of a device is proportional to its voltage–current (V–A) product. Larger transistors are typically required in order to stand

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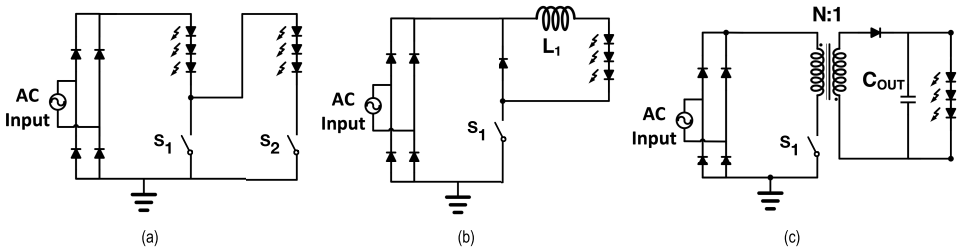

Fig. 1. Schematics of LED drivers. (a) Simplified circuit of an ac/dc converterfree LED driver. (b) Simplified circuit of a conventional buck LED driver. (c) Simplified circuit of a conventional off-line flyback LED driver.

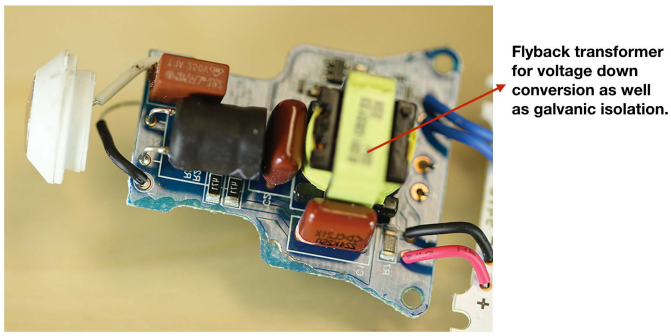

Fig. 2. Dissembled commercial flyback LED driver circuit.

higher voltage stress or to handle larger current while keeping resistive loss small. Likewise, in order to reduce the size of reactive components, one must minimize their required energy storage or V–A stress. Thus, switching converters should be designed in a way that reduces the total V–A stress over the components. Reference [5] gives two fundamental limits on the minimal V–A stress of the switches and reactive parts of a converter. Through a detailed first-order analysis in [6], it is concluded that SC converters can be superior to the inductor-based buck converter in terms of switch and reactive element utilization, approaching the given fundamental limits.

One of the noted advantages of the SC converter topologies is that their main reactive components are capacitors, which exhibit a substantially higher energy and power density than magnetics. Such is true for both integrated and discrete components. Typical surface mount capacitors can easily have an energy density three orders of magnitude larger than that of inductors [7]. The significantly higher energy density of capacitors allows for greater potential for integration. In addition, since most of the SC converter topologies (e.g., the ladder type or series–parallel type) arrange the power elements in series to interface the high input/output voltage level, the voltage stress on each individual component is only a fraction of the total rating. This allows the SC converters to use devices with lower voltage rating for "high" voltage applications. In magnetic-based converters, the main switches and reactive elements usually need to stand the whole input voltage or even higher.

However, SC dc/dc converters typically have a fixed input to output–voltage ratio. This behavior can be a disadvantage since LED devices are more conveniently controlled by a regulated forward current. Because of the process, voltage and temperature variation in an LED's I–V characteristic, it is impractical to control the LED's output by voltage regulation. A highly efficient current regulation scheme is required to take advantage of the SC converter topology for use in an LED driver. To achieve this goal, a hybrid-switched-capacitor-resonant (HSCR) strategy has been developed to combine the SC ladder topology with the series-resonant converter [8]. The proposed HSCR converter leverages the advantages of the SC topology while offering nearly lossless regulation of the output current and a soft-switching configuration to handle the parasitic capacitance of the switching transistors. The series-resonant stage can potentially provide a capacitive galvanic isolation barrier for the LED driver application as well.

We improved the HSCR architecture and implemented a highly integrated LED driver for a wide range of mains voltage standards [9]. To assist in integration, our design takes advantage of the multilevel architecture of the SC ladder topology and the lowered individual device stress. As such, we use a medium-voltage-rated analog-bipolar-CMOS-DMOS (ABCD) technology to integrate the power transistors, gate drivers, level shifters, and internal dc–dc converters into a standard SC module. These modules can then be stacked in the voltage domain to interface with various mains voltages. This paper analyzes the proposed HSCR dc/dc converter topology [9] and describes the modularized IC implementation in detail. This paper also provides the detailed analysis of the power loss of the SC ladder, the design of the resonant network, and the performance of the HSCR converter under two different output stage configurations. The measurement results of both two-chip stacking and four-chip stacking HSCR converters are reported. This paper is organized as follows. Section II introduces the proposed HSCR dc/dc converter. Section III describes the implementation details of the HSCR converter module IC, and Section IV discusses the measurement results. Finally, Section V concludes this paper.

II. Hybrid-Switched-Capacitor-Resonant DC–DC Converter

A. System Architecture

Fig. 3 shows the simplified system architecture of the proposed HSCR LED driver [9]. A PFC rectifier interfaces the 120-V_{AC} line voltage to the input of the HSCR converter, converting the ac source voltage to about 170 V_{dc}. One example of the PFC rectifier front-end implementation

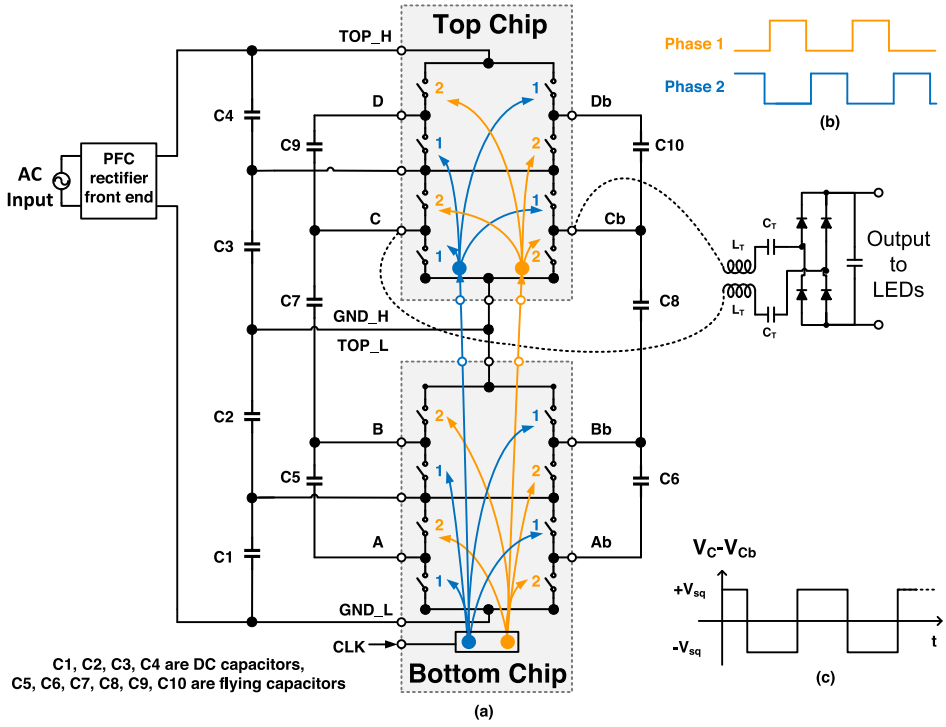

Fig. 3. (a) System architecture of the chip-stacking HSCR LED driver. (b) Two-phase nonoverlapping gate-drive signals. (c) Differential output signal between nodes C and C_b of the SC ladder.

that works with the proposed HSCR converter can be found in [10]. The HSCR converter consists of two main building blocks: a two-phase balanced 4:1 step-down power train and an LC-resonant output stage. Capacitors C_1, C_2, C_3, and C_4 in the power train are dc capacitors, which ideally distribute the input dc link voltage evenly. In order to balance the charge across each capacitor, flying capacitors C_5–C_{10} are switched in a pair of nonoverlapping phases with 50% duty cycle, as shown in Fig. 3(b). All of the switches and their driving circuits are integrated on-chip. As described in Section I, a chip-stacking configuration is implemented in order to overcome the breakdown voltage limit of the silicon technology. The SC ladder shown in Fig. 3 is split into two identical parts each with two dc voltage levels and eight main switches. This eight-switch part is designed as a standard SC module which can be stacked in series in the voltage domain and configured to stand a range of input dc voltage levels. The balanced topology of the SC ladder creates a differential ac square waveform across any two of the symmetrical flying nodes [e.g., node C and Cb in Fig. 3(a)]. This differential ac signal is then fed through the LC-resonant tank and rectified to drive the output LEDs. The differential topology helps in minimizing the common-mode signal feedthrough to the output. With high-voltage (e.g., 5 kV) multi-layer ceramic capacitor capacitors, the resonant bridge can provide dc galvanic isolation between the LED heat spreader assembly and the power train. Since the resonant capacitors are rated for high voltage, the input of the LC bridge can be attached to any of the symmetrical flying nodes. By varying the switching frequency of the SC ladder, the imaginary impedance of the LC tank can be altered, thus allowing for output current regulation. Another LC output network that utilizes all the differential nodes in the SC ladder is shown in Fig. 4 and will be analyzed in Section II-B. The modified topology reduces the required capacitance of the dc and flying capacitors and boosts the power efficiency.

B. Power Loss of the SC Ladder

A proper design of the HSCR dc–dc converter requires insights in analyzing and minimizing its power loss. There are three major contributions of power loss from the SC ladder in steady state: 1) charge sharing loss between the power capacitors during the two-phase operation; 2) resistive conduction loss due to the resonant output current flowing through the power switches; and 3) gate drive loss. The other switching losses, shoot-through current losses, and other parasitic losses are relatively small and thus are not discussed in this paper. The efficiency of the output resonant stage and the overall converter will be discussed in Section II-D. We can model the steady-state behavior of the SC ladder as an ideal transformer with a series output impedance R_S [11], which represents the power losses and the requisite output voltage drop to transfer charge from input to the load.

The charge sharing loss of traditional SC converters has been well studied, and given the complexity of the multiphase and many-element RC network, the concept of slow switching limit (SSL) and fast switching limit (FSL) have been used to approximate R_S [11]–[13]. The SSL and FSL operation conditions are based on the maximum time constant τ of the SC ladder with respect to the switching clock period $T_{\rm sw}$. If $\tau \ll T_{\rm sw}$, which is the SSL condition, all the charge sharing between the capacitors or voltage sources is completed within one clock phase. Thus, the total loss is $\sum_i (1/2) C_i \Delta v_i^2$, where

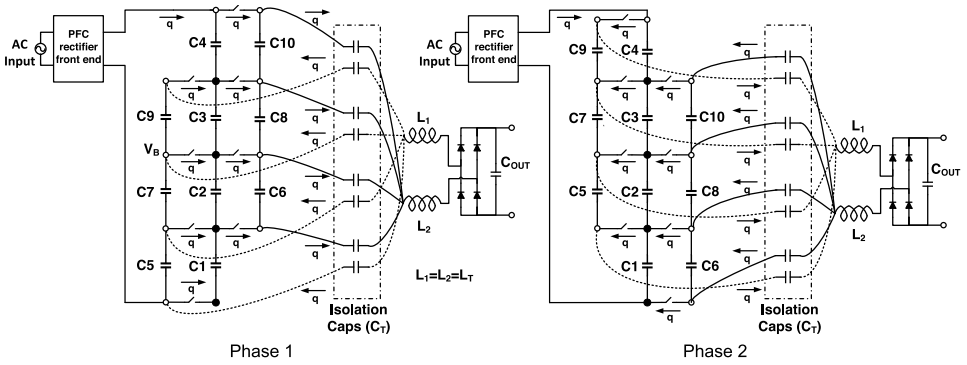

Fig. 4. Charge flow in the SC ladder when the LC-resonant bridge is attached to all four pairs of differential notes.

the ripple voltage Δv_i across each capacitor C_i is irrelevant to the resistances in the SC network. The corresponding output impedance can be expressed as $R_{\rm SSL} = \gamma\,(1/C_{sc}f)$, where γ is a constant factor derived from the SC ladder topology, C_{sc} is the total capacitance of the SC ladder, and f is the switching frequency. If $\tau \gg T_{\rm sw}$, Δv_i is very small and the charging and discharging current $i_{r,i}$ through each conduction path resistance R_i can be viewed as constant. In this case, which is called the FSL condition, the total loss can be calculated as $\sum_i i_{r,i}^2\ R_i$, and the output impedance is $R_{\rm FSL} = \delta R_{on}$, where δ is another constant factor derived from the SC ladder structure. If τ is comparable with $T_{\rm sw}$, the loss is a function of the two [13].

The resistive conduction loss caused by the resonant output current of the SC ladder can be written as $I_{\rm rms}^2 \cdot \sigma R_{on}$, where $I_{\rm rms}$ is the rms value of the resonant output current and σ is a constant factor. Thus, the equivalent output impedance is similar to the FSL condition: $R_C = \sigma R_{on}$.

The gate drive power of the primary power switches is another major source of loss. For an n:1 HSCR dc–dc converter, the number of high power switches is $2n$. Thus, the total gate drive loss is given by

$$P_G = 2nfC_{gg}V_g^2 = p_1 \cdot fnWV_g^2 \tag{1}$$

where C_{gg} is the parasitic gate capacitance of the switch transistors, which is proportional to the transistor width W, and V_g is the gate drive voltage. p_1 is a constant derived from transistor characteristics as follows:

$$p_1 = 2 \cdot \frac{C_{gg}}{W} = 2C_0 \tag{2}$$

where C_0 is the parasitic gate capacitance of the transistor per unit width. It is a common process characteristic of MOSFETs. Similarly, R_{on} of transistors in the linear region can be written as

$$R_{\rm on} \approx \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_g - V_{\rm th})} = p_2 \cdot \frac{1}{W \cdot (V_g - V_{\rm th})} \tag{3}$$

where p_2 is also a constant derived as follows:

$$p_2 = \frac{L}{\mu_n C_{ox}} \tag{4}$$

where μ_n and C_{ox} are also process characteristics of MOSFETs. Combining the power loss of charge sharing, resistive conduction, and gate driving, the minimum value of the total power loss from the SC ladder is limited by the following three terms: $(k_1/C_{sc}f)$, $(k_2/nW(V_g - V_{\rm th}))$, and $k_3 \cdot fnWV_g^2$, where $k_{1,2,3}$ are constant parameters. Since we use off-chip ceramic dc and flying capacitors, C_{sc} is mainly limited by the component cost and printed circuit board (PCB) area. Parameters f, $(n \cdot W)$, and V_g need to be traded off to optimize the power efficiency.

C. Multilevel-Resonant Output Network

An alternative HSCR converter topology using a multilevel-resonant LC output stage is proposed and shown in Fig. 4. As mentioned in Section II-A, the isolation capacitors in the resonant tank are rated for high voltage (e.g., 5 kV) and can be attached to any of the output differential nodes of the SC ladder. Thus, in the multilevel output network, we make use of every level of the SC ladder. Fig. 4 shows the charge flow of the modified HSCR converter in both phases of operation. Since each level of the SC ladder contributes equally to the output power in this modified topology, the converter is effectively a series–parallel circuit, but with zero charge variations of the dc and flying capacitors. As a result, the ideal circuit is free of capacitor charging and discharging loss and the current flows in the power train are purely resonant currents. From Fig. 4, the equivalent R_S can be written as

$$R_S = \frac{2\ R_{\rm on}}{n} = \frac{R_{\rm on}}{2} \tag{5}$$

since $n = 4$. Thus, the total power loss can be expressed as

$$P_{\rm loss\_SC} = I_{\rm rms}^2 \cdot R_S + P_G = \frac{k_2'}{nW(V_g - V_{\rm th})} + k_3' \cdot fnWV_g^2. \tag{6}$$

Here, we extract the conversion ratio n from the constants to indicate its impact on the power loss. The absence of the $R_{\rm SSL}$ term $(k_1/C_{\rm fly}f)$ enables us to reduce the capacitance of the dc and flying capacitors by at least three orders of magnitude. However, the capacitors should still exist to handle the output current mismatch in the different branches of the LC network, as well as provide enough dc supply for the gate drive channels in the SC converter IC. The absence of the $R_{\rm SSL}$ term also allows the switching frequency to be reduced even with scarce capacitance resources, thereby reducing gate drive loss. However, f is still limited by the passive components'

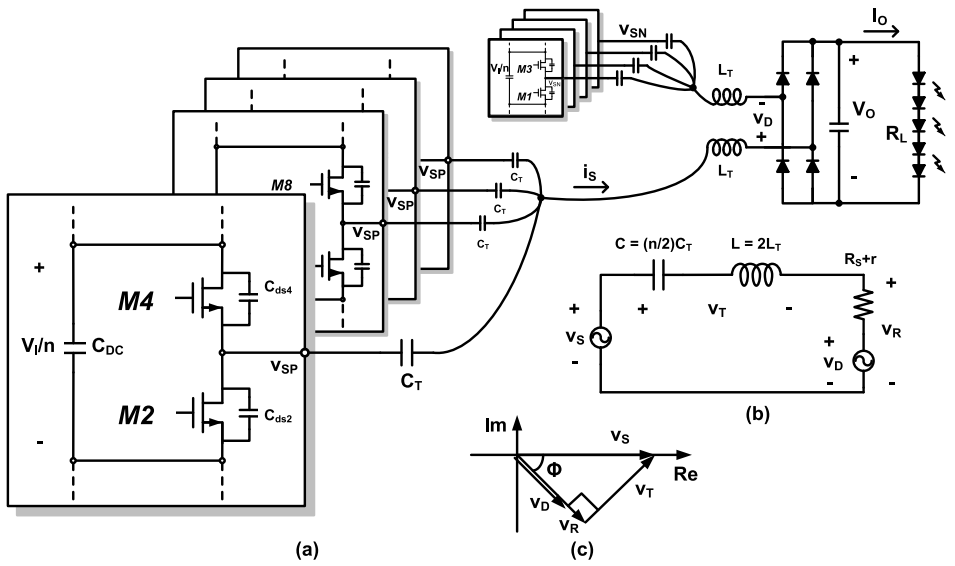

Fig. 5. (a) Equivalent circuit of the HSCR converter for ac analysis. (b) Simplified single-end equivalent circuit of the HSCR dc–dc converter. (c) Phase diagram used to design the resonant tank.

sizes in the resonant network, which will be analyzed in Section II-D. The performance of this topology is reported in Section IV.

D. Design of the Resonant Tank

The analysis in this section is based on the improved multilevel-resonant architecture, as discussed in II-C. As shown in Fig. 4, the converter is differentially symmetric. The output stage consists of a split-wound coupled inductor, two isolation capacitors for each SC level (eight in total), and a bridge rectifier. The equivalent inductance on each side is L_T and the capacitance is C_T for each isolation capacitor. Fig. 5(a) shows the equivalent circuit for the ac components of the output stage. By removing the dc components, we can now look at the multilevel SC ladder stacked in the voltage domain as multiple basic switching cells aligned in parallel. Assuming that the devices are perfectly matched, the parallel ac output signals from each side of the balanced SC ladder are equal and $v_{SP} = -v_{SN}$. The resonant output stage is attached to the SC ladder to provide low-loss current regulation and achieve zero voltage switching (ZVS) operation. In addition, it has the potential to serve as a galvanic isolation barrier [8]. In order to properly design the LC tank, a frequency-domain analysis is introduced in the following.

1) Circuit Analysis: The output stage is studied under the following assumptions: 1) the rectification diodes are ideal devices with fixed forward dc drop V_F and linear on resistance R_F; 2) the passive elements have no reactive parasitic elements; and 3) the loaded quality factor Q_L of the resonant output stage is sufficiently high so that the current through the resonant tank is sinusoidal. Fig. 5(b) shows the simplified equivalent circuit of the LC-resonant stage. v_S and i_S are the fundamental components of the differential square-wave output voltage and current from the SC ladder. Voltage v_D is the fundamental component of the input square-wave signal to the diode rectifier with ideal rectification diodes. Voltage v_T is the voltage across the LC tank, and v_R is the voltage across the resistive components in the output stage. Symbols V_S, I_S, V_D, V_T, and V_R are the amplitudes of the sinusoidal signals. P_O, V_O, and I_O are the dc output power, voltage, and current of the LED driver. $R_S = 2R_{on}/n$ is derived from the ON-resistance of the switch transistors. r represents the equivalent series resistances of the inductors. R_L is the LED load resistance and is equivalent of a resistance $R'_L = (8R_L/\pi^2)$ looking into the diode rectifier bridge from the resonant tank's output.[1] The total input resistance of the rectifier bridge can now be derived as $R_i = R'_L + 2R_F + (2V_F R'_L/V_O)$, where R_F and V_F are the ON-resistance and the forward voltage of the diodes. R_L and V_O can be derived from the output power specification P_O and the I–V characteristics of the LED load. As an example, twelve 1.2-W LED diodes with a 3.2-V operation voltage give $R_L \approx 100\ \Omega$ and $R'_L \approx 81\ \Omega$. Together with $R_F = 0.025\ \Omega$ and $V_F = 0.5$ V, we have $R_i \approx 85\ \Omega$. Thus, the power path efficiency of the HSCR converter excluding the gate drive power is given by

$$\eta_r = \frac{R'_L}{R_i + R_S + r} = \frac{R'_L}{R_i + 2R_{\rm on}/n + \omega L/Q_i} \tag{7}$$

where $L = 2L_T$ is the total inductance of the resonant tank and Q_i is the quality factor of the inductor. Using (1), (3), and (7), the overall conversion efficiency can be simplified as

$$\eta = \frac{P_O}{P_G + P_O/\eta_r} = \frac{1}{\frac{P_G}{P_O} + \frac{2R_{\rm on}}{nR'_L} + \frac{\omega L}{R'_L Q_i} + \frac{R_i}{R'_L}} = \frac{1}{c1 \cdot (nW) f + c2 \cdot (nW)^{-1} + c3 \cdot fL + c4} \tag{8}$$

where $c1$, $c2$, $c3$, and $c4$ are constants derived from the output specifications and device characteristics: $c_1 = (2C_0\ V_g^2/P_O)$, $c_2 = (L/\mu_n C_{ox}(V_g - V_{\rm th})) \cdot (2/R_L)$, $c_3 = (2\pi/R'_L Q_i)$, and $c_4 = (R_i/R'_L)$. The values of the design parameters f, W,

[1] $I_S = (\pi/2)I_O$, $V_D = (4/\pi)V_O$, and $R'_L = (V_D/I_S) = (8V_O/\pi^2 I_O) = (8R_L/\pi^2)$

and L need to be optimized for highest efficiency. Besides (8), we can derive another limit on the value of $f \cdot L$. Fig. 5(c) plots the phasor diagram of the resonant stage. As stated in assumption 3), v_S, v_T, v_R, and i_s are sinusoidal signals. The phase angle between v_S and i_s is given by

$$\tan\psi = \frac{\omega L - \frac{1}{\omega C}}{R} = \frac{\sqrt{V_S^2 - v_R^2}}{V_R} \approx \frac{\sqrt{V_S^2 - V_D^2}}{V_D} \tag{9}$$

where $C = (n/2)C_T$, $R = R_i + R_S + r$, $V_S = (4/\pi)V_I/n$, and $V_D = (4/\pi)V_O$. V_I is the dc input voltage of the SC ladder. From (9), we derive

$$f \cdot L = \frac{1}{2\pi}\left(\tan\psi \cdot R + \frac{1}{2\pi f C}\right) \approx \frac{\tan\psi R_i}{2\pi} + \frac{1}{4\pi^2 f C}. \tag{10}$$

The first term in (10) is constant. Combining (8) and (10), we obtain

$$\eta \approx \frac{1}{c1 \cdot Wf + c2 \cdot W^{-1} + c3' \cdot (fC)^{-1} + c4'} \tag{11}$$

where $c3'$ and $c4'$ are constant parameters. The denominator can be minimized by optimizing the transistor width W and switching frequency f once the tank capacitance C is given. From (11), larger capacitance within the design specifications should be used. However, the capacitance value is often safety-limited due to the common-mode impedance requirements for galvanic isolation. The usual upper bound is about 10 nF. Thus, in order to meet the safety standards, each isolation capacitor C_T in the HSCR converter should be $\leq$ (5 nF/n_{stage}), where n_{stage} is the number of stages of the converter.

2) Zero Voltage Switching: The parasitic capacitor C_{ds} of each switch transistor needs to be charged to V_I/n when the transistor is OFF and discharged to zero when it is ON, resulting in a significant energy loss at high frequencies and voltages. In order to minimize this loss, a ZVS condition should be enforced. This is achieved by providing a resonant switching transition during the dead time of the two-phase gate drive signals. Fig. 5(a) shows the parasitic C_{ds} of the switch transistors. When switch M_2 is turned ON, C_{ds2} discharges from V_I/n to zero, while C_{ds4} is charged from zero to V_I/n. By keeping the switching frequency of the SC ladder above resonance, the tank current can displace the charge across all the C_{ds} capacitors. Fig. 6 shows one example of the ideal waveforms of the differential output voltage of the SC ladder and the resonant tank current together with the two-phase gate drive signals. The total charge that needs to be displaced from C_{ds} of n stages is $Q_{\text{ds}} = C_{\text{ds}}V_I$. Q_{ds} should be smaller than the maximum charge $Q_{\max}$ that the tank current can displace. As depicted by the shaded region in Fig. 6, $Q_{\max}$ can be found by integrating the tank current between the falling edge of the gate drive signal and the tank current's zero crossing. Thus, $Q_{\max}$ and the switching frequency range for ZVS are

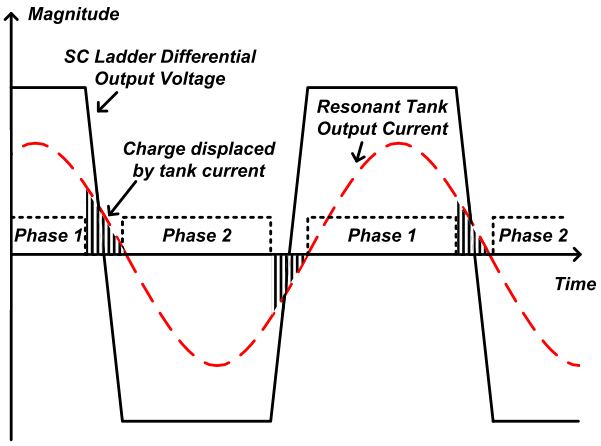

Fig. 6. Example of ideal ZVS waveforms. Solid line: SC ladder differential output voltage. Dashed line: resonant tank current. Dotted line: two-phase gate-drive voltages.

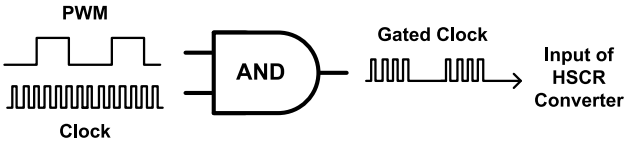

Fig. 7. PWM dimming of the LED driver.

given by

$$Q_{\max} = \frac{1}{\omega}\int_{\frac{\pi}{2}}^{\frac{\pi}{2}+\psi} |i_s|\cos\theta \; d\theta = \frac{|i_s|}{\omega}(1-\cos\psi) \tag{12}$$

$$f \leq \frac{|i_s|}{2\pi C_{\text{ds}} V_I}(1-\cos\psi) = \frac{I_O}{4C_{\text{ds}}V_I}(1-\cos\psi). \tag{13}$$

E. LED Dimming

The HSCR converter can be efficiently dimmed by gating the input clock with a low-frequency PWM signal, as shown in Fig. 7. The PWM signal activates and deactivates the HSCR converter at around 2 kHz with a tunable pulsewidth to control the average power delivered to the LED diodes. When the HSCR converter is activated, it operates with high efficiency as discussed previously. When it is completely deactivated, it consumes no power. However, the converter suffers extra power loss during the start-up and shutdown transitional phases, which reduces its average efficiency in the heavily dimmed situations.

III. Stackable DC–DC Converter IC Implementation

A. Chip-Stacking Topology

The prototype HSCR dc–dc converter is designed to handle multiple mains voltage standards, such as 120 and 240 V_{ac}, which, respectively, become 170 and 340 V_{dc} after rectification. The characteristics and availability of industrial high voltage silicon processes can limit the application and performance of off-line power converter ICs. Taking advantage of the multilevel structure of the proposed HSCR topology,

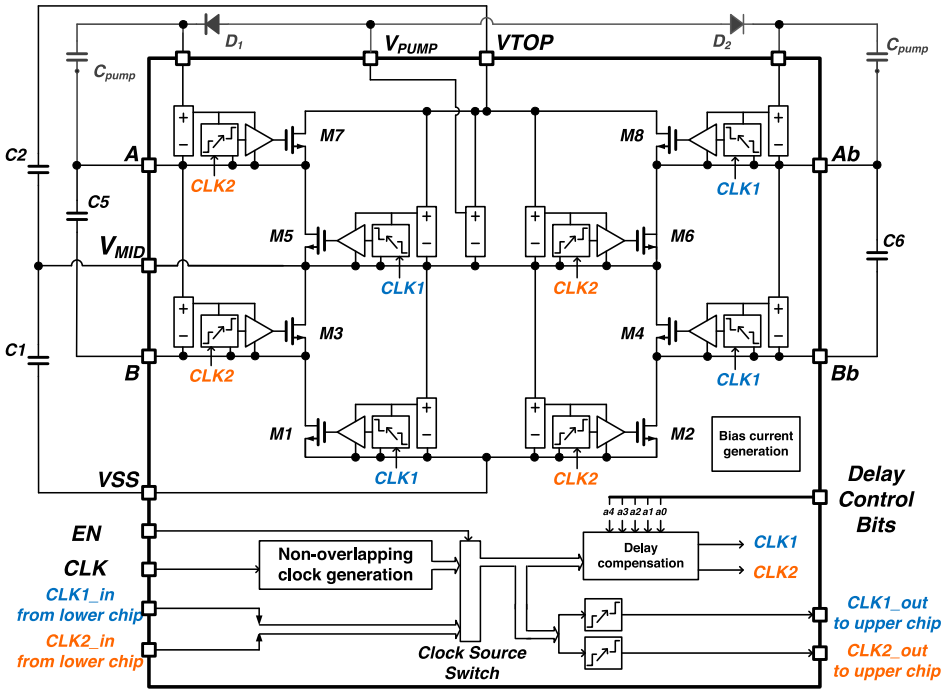

Fig. 8. Architecture of the SC converter IC.

a chip-stackable dc–dc converter is implemented in a 120-V rated technology. By stacking multiple chips, we can exceed the breakdown voltage limit of the silicon process and handle a range of input voltage levels.

1) Overall Architecture: The overall architecture of the stackable SC converter IC is shown in Fig. 8, which in this example represents the bottom chip of Fig. 3(a). The eight main switches, M_1–M_8, with their gate drive circuits are integrated onto the IC. Here, we represent each main switch and its driving circuits as a single channel, as shown in Fig. 10. The main switches are implemented with n-type laterally diffused metal–oxide–semiconductor (nLDMOS) transistors. Each transistor only needs to block a voltage drop of $V_{\rm IN}/n$, where n is the conversion ratio of the converter. Since the off-chip capacitors $C_{1,2,5,6}$ are large (>200 nF), they can be used as dc voltage supplies for the gate drive channels. The static capacitors C_1 and C_2 supply the gate drive channels for M_1, M_2, M_5, and M_6. Similarly, the flying capacitors C_5 and C_6 supply the channels for M_3 and M_4. Two small capacitors $C_{\rm pump}$, a voltage supply generator for $V_{\rm pump}$, along with diodes D_1 and D_2 form a charge pump that provides the supply voltage for the channels of the top switches M_7 and M_8. Note that the voltage on the positive plate of $C_{\rm pump}$ exceeds $V_{\rm TOP}$ by $V_{\rm pump}$ when the switches are turned ON. $V_{\rm pump}$ should be large enough to supply the top channels while keeping $V_{\rm TOP} + V_{\rm pump}$ smaller than the breakdown voltage of the silicon process. $C_{\rm pump}$ can be as small as a few pF and can be integrated on chip with D_1 and D_2. The operation of the main switches is controlled by a pair of nonoverlapping clock signals CLK1 and CLK2. These signals are generated in the 0–5-V voltage domain and are level-shifted to the voltage domain of each gate drive channel.

2) Signal Path and Delay Compensation: The stacked chips in the SC ladder can be configured to pass and synchronize the gate drive clock signals for each switch channel. By activating the control bit EN, the bottom chip selects CLK as the input, from which a pair a nonoverlapping gate drive signals with the same frequency as CLK are generated. These clock signals are simultaneously sent in two directions. In one direction, the signals are fed through a delay chain and level-shifted to the gate drive channels within the chip, as shown in Fig. 9(a). In the other direction, the clock signals are level-shifted to above $V_{\rm TOP}$ and sent to the upper chip. The upper chip can then utilize the synchronized clock signals in the same way. As discussed in Section II-B, in order to have optimal efficiency, the capacitor charge variation per clock phase Δq should be minimized and balanced across capacitors. However, mismatched gate drive signals lead to unbalanced charge transfer and additional loss. In the worst case, gating mismatch can cause shoot-through current, which can burn a large amount of energy and destroy the switches. For these reasons, the delay compensation block is introduced to compensate for the delay in the clock signal path between chips. In general, the delay is a product of the level shifters, buffers, and signal path parasitics. The delay compensation ultimately allows for the gate drive signals to arrive at the main switches in all the chips with a negligible timing mismatch (<6 nS). The delay chain is implemented with 31 inverter-based delay elements and a 32:1 MUX, controlled by a 5-bit control signal. Each element can generate 580 ps of delay, allowing for a maximum delay of around 18 ns. The simulation shows that as long as the mismatch is within 6 nS between chips, its effect on efficiency is negligible.

B. Gate-Driving Circuits Implementation

The schematic of a gate drive channel is shown in Fig. 10. The channel consists of a channel-supply generator, a level shifter, and a gate driver.

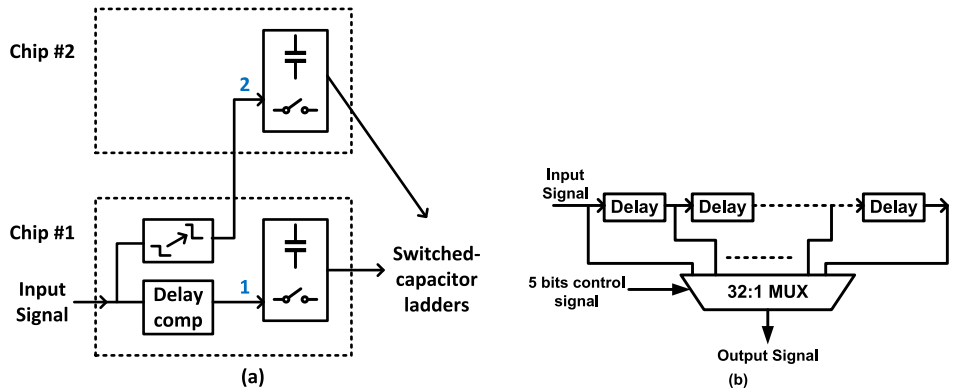

Fig. 9. Block diagram of (a) delay compensation system and (b) digital-controlled delay generation chain.

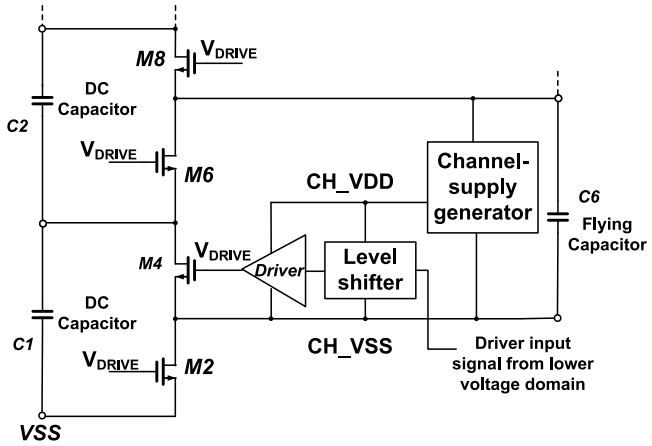

Fig. 10. Block diagram of the gate driver.

1) Channel-Supply Generator: A channel-supply generator is required to generate a 5-V dc supply above the source voltage of the nLDMOS switching transistor in order to drive it. A 5-V supply voltage is selected based on $V_{\mathrm{GS,\ MAX}}$ of the nLDMOS device. The supply generator is implemented as a simple linear regulator due to the restrictions on the silicon area and the self-start-up requirements of the converter. Conveniently, the regulator can be built with the 5-V Zener diode provided by the technology, as shown in Fig. 11(a). A reference voltage V_{REF} is generated from a bias current I_{bias} flowing through a Zener diode and a diode-connected pLDMOS device. This reference voltage is held constant at $V_{\mathrm{REF}} = V_{\mathrm{ch\_vss}} + V_{\mathrm{GS2}} + V_Z$, where V_Z is the Zener voltage. Transistor $M1$ acts as an amplifier whose output voltage is $V_{\mathrm{ch\_vdd}} = V_{\mathrm{REF}} - V_{\mathrm{GS1}} \approx V_Z + (I_{\mathrm{BIAS}}/K_2)^{1/2} - (I_{\mathrm{LOAD}}/K_1)^{1/2}$, where K_1 and K_2 are the $(1/2)\mu_n C_{ox}(W/L)$ constants of devices M_1 and M_2. C_1 is the output decoupling capacitor.

In the case where the regulator is in parallel with a flying capacitor, node ch_vss has a voltage swing of around 42.5 V. Due to the parasitics between the devices and the substrate, $V_{\mathrm{REF}} - V_{ch\_vss}$ and V_{GS2} can change drastically during the switching period. Thus, capacitor C_2 is needed to stabilize the reference node and protect devices from voltage breakdown. Ideally, we would like to reduce I_{bias} to save power. On the other hand, when a large pulse current is drawn from ch_vdd, e.g., while the gate driver is turning ON the main switch by charging the C_{GS} of the large nLDMOS, the pulse current can be coupled through C_{GS1} to the reference node V_{REF} and generate a significant ΔV across C_2. The rising slope of V_{REF} to its set value influences the voltage at the gate of the main switch, which ultimately affects the switch's average R_{on}. In order to reduce the voltage variation on V_{REF}, the size of M_1 needs to be limited and the value of I_{bias} should be optimized to balance power consumption and V_{REF} variation.

2) Level Shifter: The schematic of the level shifter circuit is shown in Fig. 11(b). The input clock signals Clk and Clk_b are in the low voltage domain between V_{DD} and V_{SS}, while the shifted output signal $\mathrm{Clk_{out}}$ is between $\mathrm{Ch_{VDD}}$ and $\mathrm{Ch_{VSS}}$. The voltage drop from $\mathrm{Ch_{VSS}}$ to V_{SS} can be up to 100 V. Transistors M_1 and M_2 form a differential pair with a regenerative-connected load M_7 and M_8. M_1 and M_2 are high-voltage devices that isolate the two voltage domains to protect the low-voltage transistors. The swing of the upshifted signal V_A and V_B is limited by diode-connected transistors M_5 and M_6, so they stay above V_{Ch_VSS}. To speed up the transition of the differential pair, a positive feedback loop is added to the level shifter. V_A and V_B are downshifted with another differential pair to the low voltage domain and are compared with Clk and Clk_b. In the transition interval, Clk and Clk_b will switch first and become opposite in phase to the downshifted signals. Once the difference is detected, a large current I_{PULSE} will be injected into the differential pair to speed up the flipping of the output signals. I_{PULSE} is only injected during the transition interval and a small bias current I_{BIAS} is left in the rest of the time to keep the operation point, which is more energy efficient.

3) Converter Start-Up: The HSCR dc–dc converter can self-start-up. As shown in Fig. 12, the charge flow during the start-up phase is marked with the red arrows. DC capacitors C_1 and C_2 are charged up once the input voltage V_{TOP} rises. The bias current generator is connected directly to the input node TOP and provides a 5-V supply voltage for the digital blocks. It also generates the bias current for all the channel-supply generators and level shifters. C_5 and C_6 are charged from node V_{MID} through the reverse diodes in the nLDMOS transistors M_5 and M_6. The charge pump capacitors C_{PUMP} are charged by the charge-pump-supply generator,

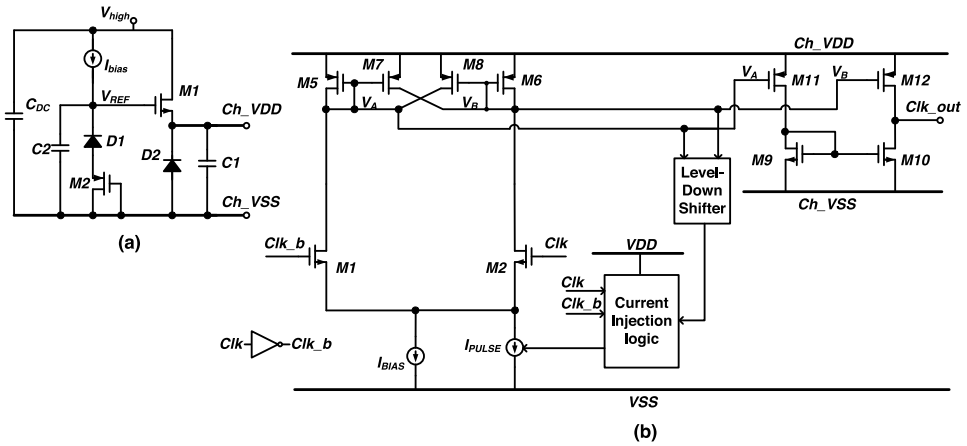

Fig. 11. Schematic of (a) channel-supply generator and (b) level shifter.

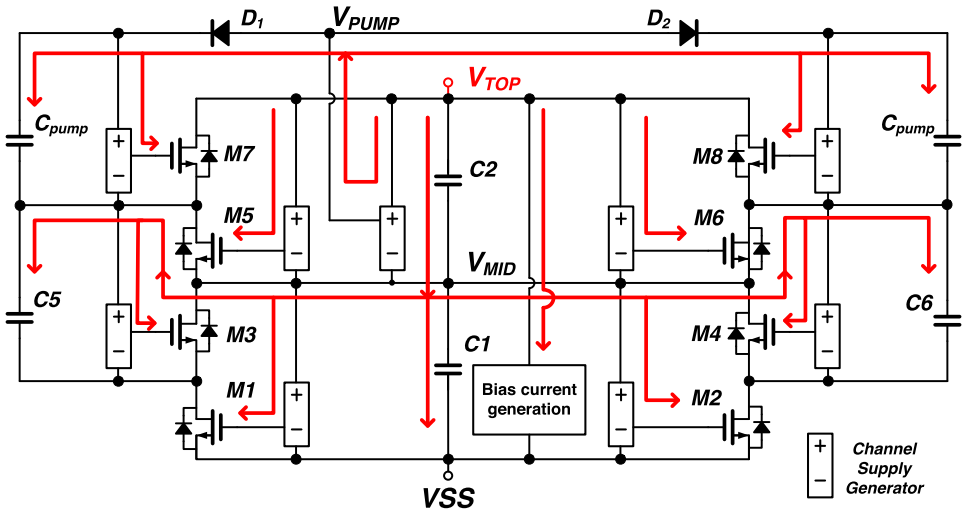

Fig. 12. Charge flow in the start-up phase of the converter.

which converts ($V_{\rm TOP} - V_{\rm MID}$) to $V_{\rm PUMP}$. As shown in 11(a), each channel-supply generator has a reference current path through a Zener diode across its dc input. In the start-up phase, the channel-supply generators stack in series and create a reference current path from $V_{\rm TOP}$ to $V_{\rm SS}$. This guarantees that all the channel-supply voltages can be generated during the start-up phase. The current path is also a resistive divider that sets the value of $V_{\rm MID}$. In order to protect the transistors from the unbalanced voltage drop across the dc capacitors, $V_{\rm TOP}$ should be ramped up with the clock signal applied.

IV. Experimental Results

A. Measurement Setup

The HSCR dc–dc converter IC is fabricated in an ABCD process with maximum 120-V voltage tolerance on silicon. The die shown in Fig. 13 measures 14.1 mm^2, which includes the eight main switch channels, the bias generation circuitry, the delay compensation block, and all the other supporting digital circuits. The converter is packaged in a 40-pin Leadless Leadframe Package for testing. Fig. 14 shows the test board of a two-chip-stacking HSCR dc–dc converter driving a string of 12 1-W white LEDs. The test board is implemented with a two-layer PCB and requires an input clock signal around 1 MHz to convert the input dc voltage to the specified output current. LED dimming is achieved by using a PWM control signal to gate the clock signal before it enters the test board. The digital configuration bits are manually set by jumper switches. Discrete 1 μF ceramic capacitors are used as the dc and flying capacitors in the SC ladder. The HSCR converter test board uses a split-wound coupled inductor with the total differential inductance 6.7 μH and two 10-nF 3-kV capacitors as the LC-resonant tank. Isolation capacitors with higher voltage ratings can be used based on the safety standards. The inductor is built from Micrometal's T50-6 iron powder toroidal core, with a height of 0.5 cm and an outer diameter of 1.3 cm. The discrete components used to implement the two-chip-stacking HSCR dc–dc converter is summarized in Table I.

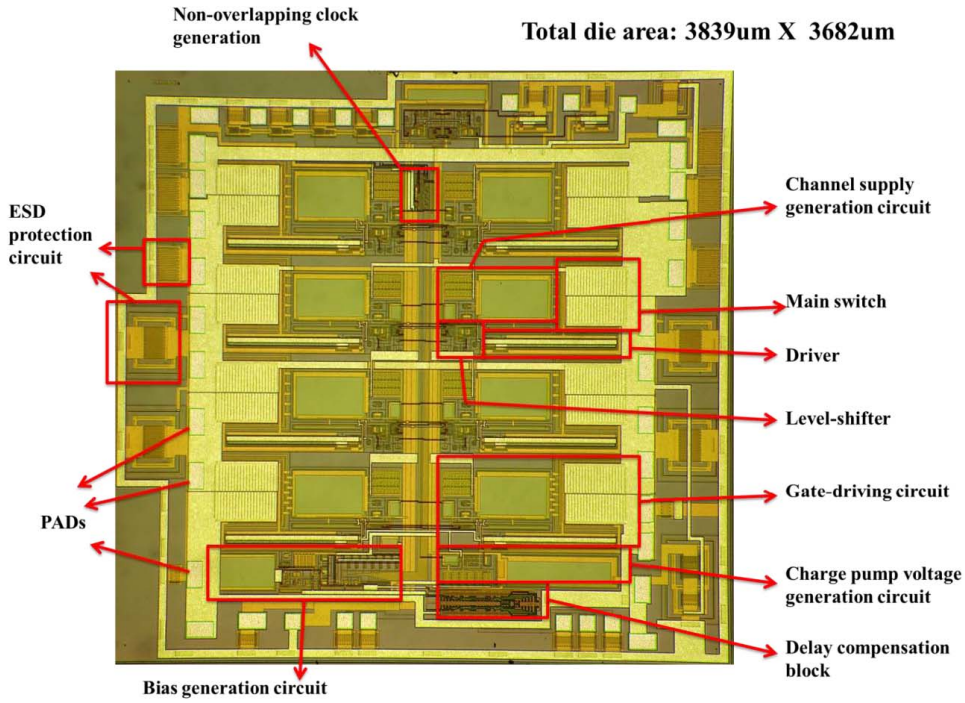

Fig. 13. SC converter die photograph.

TABLE I
COMPONENTS USED IN PROTOTYPE DC–DC CONVERTER FOR LED DRIVER

COMPONENT	Symbol in Fig. 3	MPN	DESC.	QTY
DC capacitor	C1 ~ C10	C3216X7R	1 µF, 50 V	10
Isolation capacitor	C_T	2220HC	10 nF, 3 kV	2
Resonant inductor	L_T	T50-6	26 AWG, 6.7 µH	1
Rectifier diode		PD3S160-7	60v, 1A	4

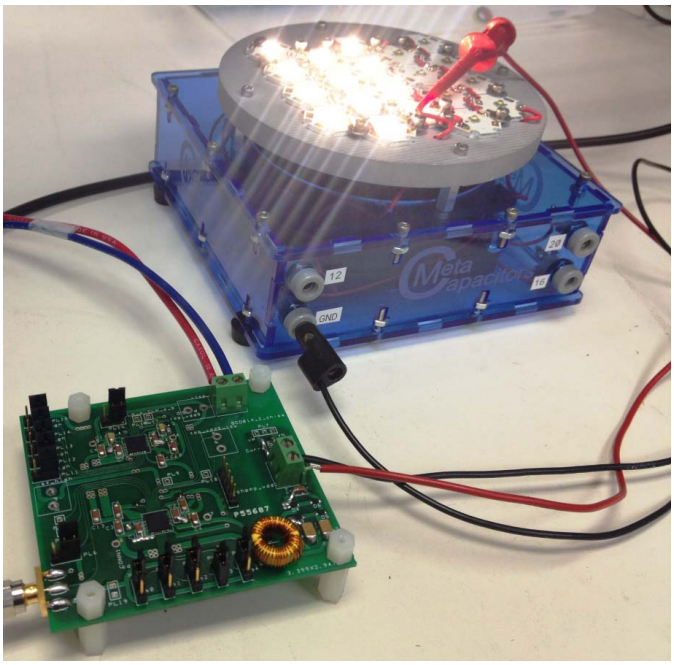

Fig. 14. Two-chip-stacking dc/dc converter for LED driver.

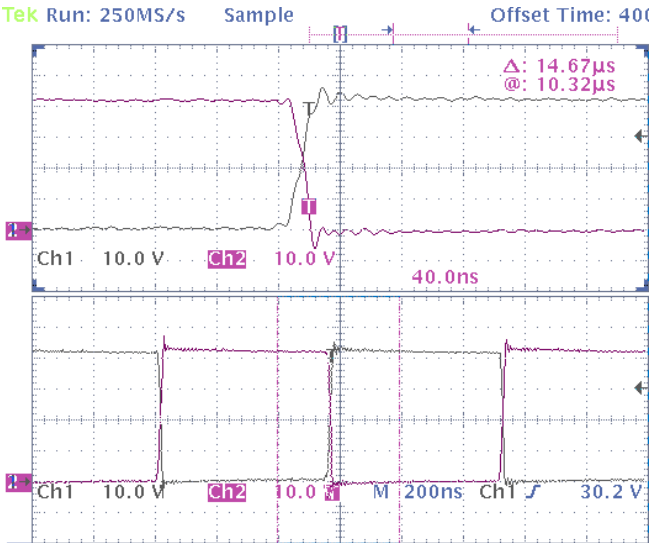

Fig. 15. Voltage waveforms of the differential output nodes of the SC ladder (nodes A and Ab in Fig. 3). The waveform on top (Ch1) is a zoomed-in view of the switching edge of the signals.

Fig. 15 shows the differential output voltage of a single stage of the SC ladder, which is the voltage of node A and Ab in Fig. 3. ZVS is achieved since the voltage transition across the parasitic C_{ds} of switch transistors finishes within the 25-ns nonoverlapping period of the two-phase gate-drive signals. The voltage of the flying nodes on one side of the balanced SC ladder (nodes A–D in Fig. 3) is shown in Fig. 16. The peak voltage stress on the switch transistor is around 45 V. The

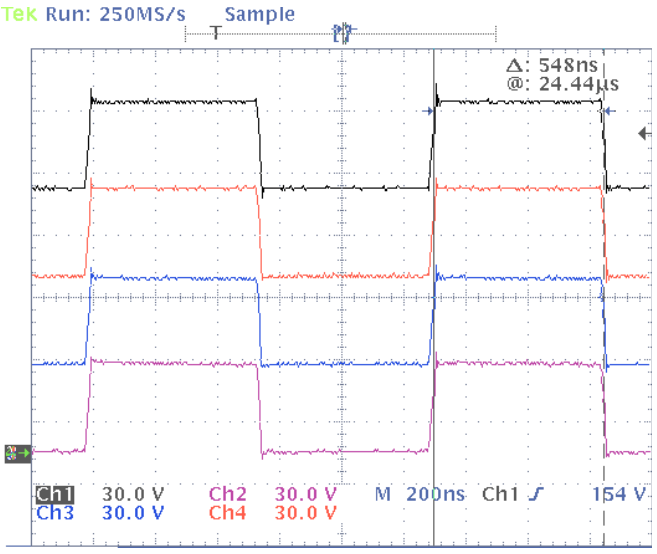

Fig. 16. Voltage waveforms the flying nodes on one side of the SC ladder (nodes A–D in Fig. 3).

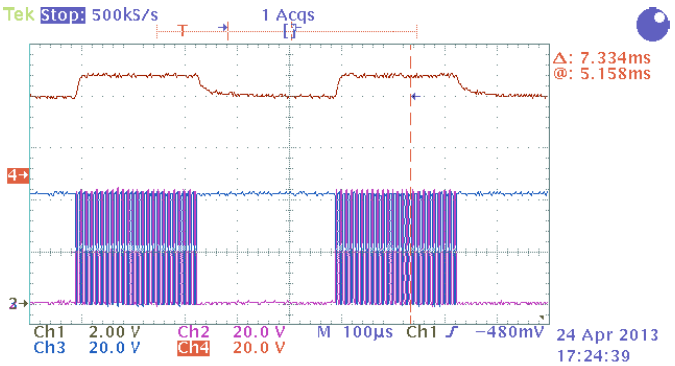

Fig. 17. Voltage across the LED string during dimming (upper waveform) and the voltage of the differential output nodes A and Ab in Fig. 3 (lower waveform).

well-aligned gate drive signals on chip, and between chips, enables the nearly ideally aligned waveforms of the flying nodes. Fig. 17 shows the output voltage across the LED string and the differential voltage of nodes A and Ab in Fig. 3 when the LEDs are dimmed. The start-up time of the output LEDs is 17 μs and shutdown time is about 60 μs.

B. Converter Performance With Different LC Output Stages

Two prototypes of the two-chip-stacking HSCR converter have been realized with single-level and multilevel LC output stages, respectively. Measurements of their power efficiencies are carried out over an input voltage variation from 160 to 180 V_{dc}. The output currents are regulated to constant values by controlling the switching frequencies. The targeted current levels are set to show the maximum efficiencies of the converters. The measured efficiencies and switching frequencies are shown in Fig. 18. With the single-level LC stage, the converter's efficiency varies between 85.6% and 90% for a 372-mA output current. The switching frequency is tuned from 870 kHz to 1.14 MHz. The prototype with the multilevel LC stage achieves higher efficiency between 91.5%

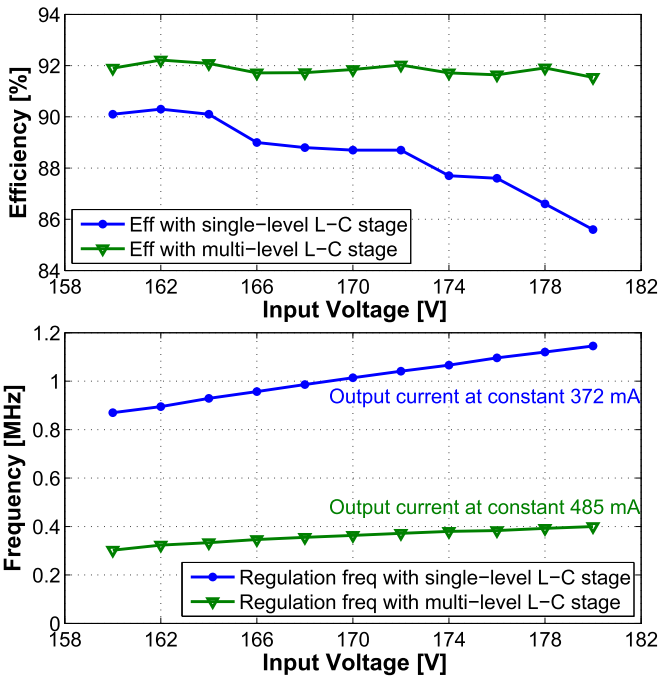

Fig. 18. Measured switching frequencies, output currents, and efficiencies versus input voltage variation of the proposed LED driver with the single-level and multilevel output LC stages connected.

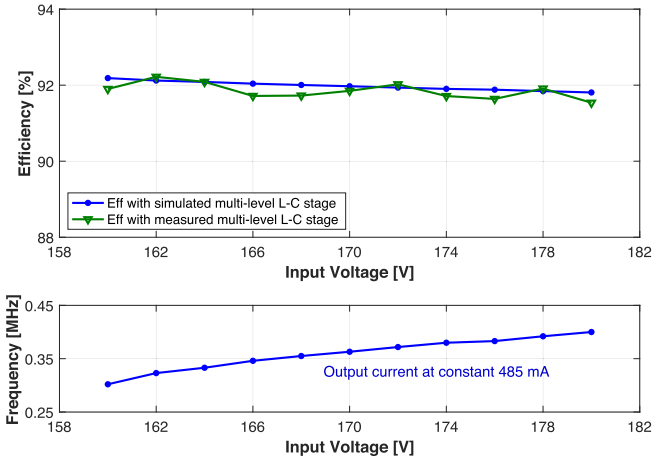

Fig. 19. Theoretically calculated and measured efficiencies versus input voltage variation of the proposed LED driver with the multilevel output LC stages.

and 92.2% while delivering a larger output current of 485 mA. As discussed in Section II-C, with limited capacitance in the SC ladder, the multilevel LC stage allows us to lower the switching frequency of the SC ladder from around 1 MHz to between 300 and 400 kHz. The improved efficiency of the multilevel-resonant topology is the result of the minimized capacitive charge sharing load and loss, as well as lowered gate-drive power consumption. To validate 11, we plotted the calculated versus measured efficiency of the HSCR converter with the multilevel LC stage in Fig. 19. The two results match closely.

Fig. 20 shows the dimming performance of the converter with the single-level and multilevel LC output stages. With duty-cycle control of the PWM dimming signal, the converter's output power can be dimmed from 100% to as low as 3%.

TABLE II
COMPARISON TO STATE-OF-THE-ART LED DRIVER DESIGNS

	ISSCC_12 [14]	ISSCC_11 [15]	JSSC_16 [17]	JSSC_18 [16]	ISSCC_11 [2]	JSSC_12 [3]	This Work
Converter Topology	Buck-Boost (DC-DC)	Buck-Boost (DC-DC)	Synchronous Inverted Buck (DC-DC)	Quasi-Resonant Inverted Buck (AC-DC)	Buck-Boost (AC-DC)	Flyback (AC-DC)	Hybrid_Switched-Capacitor-Resonant (DC-DC)
Technology	0.18µm CMOS	0.5µm CMOS	0.5µm 120V CMOS	Off-chip 600V GaN FETs & 0.35µm 120V CMOS	0.5µm 500V BCDMOS	0.35 um BCDMOS + 800V off-chip MOSFET	2.5µm 100V BCDMOS
Input Voltage Range (V)	**2.7 - 5.5**	**3-5.5**	**5 - 115**	**100 - 120 V_{AC}**	**50 - 320 V_{AC} or 450V_{DC}**	**180 - 260 V_{AC}**	**80 - 90, 160 - 180, 240 - 270, 320 - 360**
Output Current (A)	0.1 - 2	0.6 - 1.2	± 6.2% of 0.35	~ 0.5	~ 0.2	~ 0.36	0.485
Output Power (W)	0.5 - 10	~ 2.2 - 4.3	< 25	20 - 25	2.5 - 7	6 - 12	1.1 - 22
Efficiency vs Vin Range	80% - 91%	78% - 90.7%, 60% - 86%	77% to 94.4%	Peak 91.4% at 100V_{AC}	peak 86% at 110V_{AC}, peak 89% at 220V_{AC}	Peak 85.2% at 220V_{AC}	91% - 92.2% (160V - 180V), 89.6% - 91.2% (320V - 360V)
Switching Frequency (MHz)	2.5	1 - 2	< 2.2	1.7 - 5.7	0.086	2	0.3 - 0.4
Isolation	No	No	No	No	No	Yes	Yes
PFC Included	No	No	No	Yes	Yes	Yes	No
Magnetic Component for Peak Efficiency (uH)	**1**	**2.2**	**39**	**6.6**	**5500**	**2143**	**20**
Dimming Method	Amplitude	Amplitude	PWM	No	No	Firing angle controlled TRIAC dimming	PWM
Dimming Range (%)	5% - 100%	50% - 100%	10% - 100%	N/A	N/A	20% - 100 %	7.4% - 100%
Active Area (mm²)	4.125	5	9.4	3.3	3.132	0.76	14.1

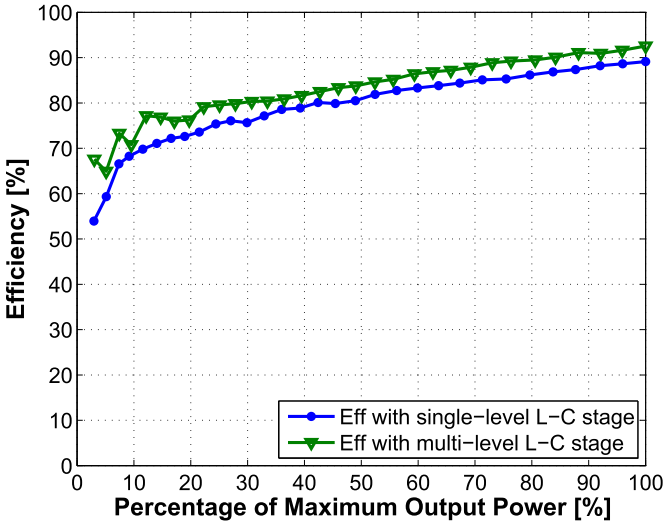

Fig. 20. Measured efficiency versus dimmed output power of the proposed LED driver with the single-level and multilevel output *LC* stages connected. The input voltage is 170 V_{dc}.

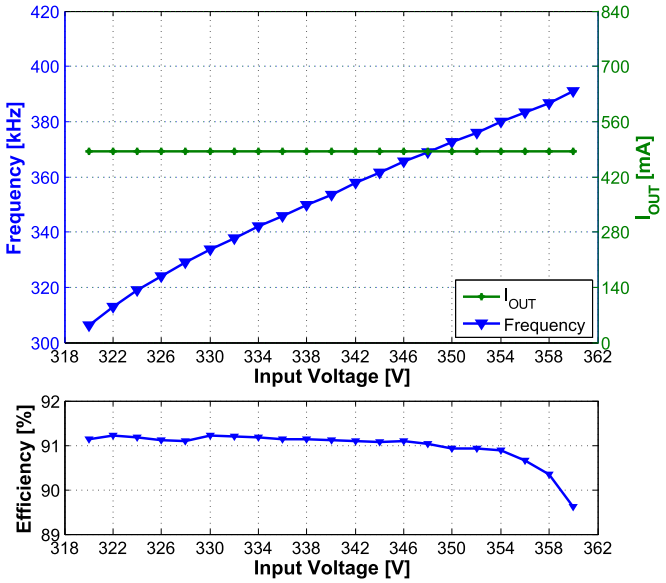

Fig. 21. Measured switching frequency, output current, and efficiency versus input voltage variation of the proposed LED driver with the rectified 240-V_{ac} (340-V_{dc}) input.

When the dimming ratio is higher than 10%, the power efficiency is kept above 70% with the single-level *LC* stage; 2%–3% improvement in efficiency can be observed with the multilevel *LC* stage.

C. Four-Chip-Stacking DC–DC Converter

As discussed in Section I, the proposed dc–dc converter IC can be stacked to interface with a range of input voltage levels. A four-chip-stacking converter with the multilevel *LC* output network has been implemented and measured for applications with around 240 V_{ac} (rectified 339 V_{dc}) input voltage. Fig. 21 shows the efficiency and current regulation performance of the converter with an input voltage range from 320 to 360 V_{dc}. The conversion efficiency stays above 89.6% when the current is regulated to be constant at 485 mA by tuning the switching frequency from 306 to 391 kHz. The output power can be dimmed to 27.3% with >75 % efficiency, as shown in Fig. 22. Based on (11), the transistor width, nW, has an optimized value for maximum efficiency. However, as we change the conversion ratio n of the SC ladder by stacking a different number of chips, the switch transistor width W cannot be modified after fabrication. Since the circuit is optimized for the two-chip-stacking converter operation by design, the efficiency of the four-chip-stacking LED driver is slightly lower.

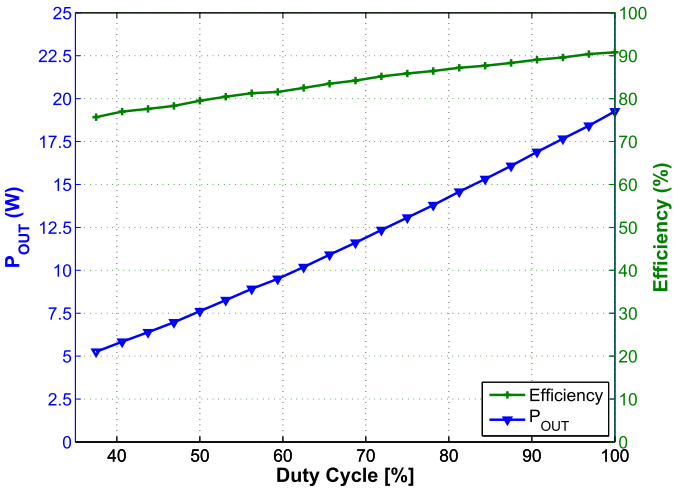

Fig. 22. Measured output power and efficiency versus dimming duty cycle of the proposed LED driver with the rectified 240-V_{ac} (340-V_{dc}) input.

D. Performance Comparison

A comparison of this paper with six other state-of-the-art LED drivers is given in Table II. The performance of this paper is based on the prototypes with multilevel *LC* output networks. Table II shows that the proposed LED driver achieves higher efficiency compared with the designs in [2], [3], and [14]–[16], much wider input voltage range than the designs in [14]–[16], and can achieve much higher input voltage level than [17]. This paper provides a wide output power and dimming ranges as well. Compared with the higher voltage designs in [2], [3], and [17], the proposed design has a smaller magnetic component size while providing a certain degree of isolation protection. With silicon technologies that allow higher frequency operation, the size of the isolation capacitance in the resonant stage can be further reduced, resulting in larger common-mode impedance for galvanic isolation. Furthermore, the proposed IC can be conveniently stacked for various input voltage levels or connected in parallel for heavier output load.

V. Conclusion

This paper presents a stackable SC dc–dc converter IC for an HSCR LED driver. The topology combines the advantages of the SC converter and the series-resonant converter, achieving an optimized use of reactive elements and switches. By developing a chip-stackable integrated SC module and a multilevel *LC*-resonant output network, the converter can be reconfigured and extended to handle a wide range of input voltage levels with relatively constant efficiency while requiring only an IC process that is rated for a half or a quarter of the input voltage. The HSCR converter also offers nearly lossless regulation and dimming functionality with small reactive components. The *LC* stage further has the potential to serve as a galvanic isolation barrier for safety concerns. The converter prototype achieves >91 % efficiency while delivering up to 22 W to an LED string for inputs from 160 to 180 V_{dc} and >89 % efficiency for inputs from 320 to 360 V_{dc}. This sets it apart as one of the highest power SC converters with an IC power train compared with the current state of the art.

Acknowledgment

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