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High Efficiency and High Linearity Doherty Amplifiers for Portable Wireless Communications

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electrical circuits and systems)

by

Yu Zhao

Committee in charge:

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2006

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Chair

University of California, San Diego
2006

To my parents and my Ruoheng, whose unconditional supports

have always been my greatest inspirations.

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Y. Zhao, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, "Linearity improvement of HBT-based Doherty amplifiers based on a simple analytical model," *IEEE Trans. Microwave Theory Tech.*, vol. 54, Dec. 2006.

Y. Zhao, M. Iwamoto, L.E. Larson, and P.M. Asbeck, "Doherty Amplifier with DSP Control to Improve Performance in CDMA Operation," *IEEE MTT-S International Microwave Symposium*, June 2003.

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A. Conway, Y. Zhao, P. M. Asbeck, M. Micovic, and J. Moon, "Dynamic gate biasing technique for improved linearity of GaN HFET power amplifier," *IEEE MTT-S International Microwave Symposium*, June 2005.

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Y. Zhao, M. Iwamoto, L.E. Larson, and P.M. Asbeck, "Using DSP to improve the performance of a Doherty Amplifier," *IEEE Topical Workshop on Power Amplifiers*, Sep. 2002.

Y. Zhao, M. Iwamoto, L.E. Larson, and P.M. Asbeck, "A 900MHz Doherty Amplifier implemented with lumped elements," *IEEE Topical Workshop on Power Amplifiers*, Sep. 2003.

Y. Zhao, M. Iwamoto, L.E. Larson, and P.M. Asbeck, "An analytical model of distortion in Doherty Amplifiers implemented with HBTs," *IEEE Topical Workshop on Power Amplifiers*, Sep. 2005.

ABSTRACT OF THE DISSERTATION

High Efficiency and High Linearity Doherty Amplifiers for Portable Wireless Communications

by

Yu Zhao

Doctor of Philosophy in Electrical Engineering (Electrical circuit and systems)

University of California, San Diego, 2006

Professor Peter M. Asbeck, Chair

The design of power amplifiers for wireless systems has become a challenging task due to increasingly stringent requirements placed upon transmitters using spectrum efficient modulation techniques. The Doherty amplifier is an important candidate for this type of application due to its feature of high efficiency over an extended power range. However, Doherty amplifiers in practice have often failed to exhibit the superb efficiency predicted by theory and their linearity is not always adequate to meet strict specifications of systems with high Peak-to-Average Ratio (PAR) signals such as CDMA systems. The objective of this dissertation is to provide a path for Doherty amplifiers that leads to a simultaneous high efficiency and high linearity performance.

First, based on detailed understanding of Doherty amplifier theory and careful investigation of behavior of Doherty amplifiers, a series of guidelines for designing a Doherty amplifier was created. A Doherty amplifier based on GaAs FET devices was accordingly designed in simulation and then fabricated. Simulation and measurement

results were compared to provide a description of performance issues of the Doherty amplifier.

Following the studies on characteristics of the Doherty amplifier, a new digital signal processing (DSP) control strategy was developed, which involves control of the gate bias voltage of the auxiliary amplifier. DSP was utilized to mitigate gain variations through this bias control and to eliminate phase distortion through baseband phase predistortion. The strategy was shown to significantly improve linearity of the Doherty amplifier, enabling it to meet ACPR specifications with IS-95 signals. The Doherty amplifier also maintained its high efficiency performance. Advantages of analog component based predistortion were also studied and demonstrated by experiments.

Finally, in an effort to find a circuit solution for high linearity Doherty amplifiers, nonlinear behavior in Doherty amplifiers was investigated. A simple analytical model was developed based on full transistor models. The model enables nonlinearity analysis associated with each nonlinear component in the transistor. This results in accurate distortion prediction for a Doherty amplifier implemented with InGaP/GaAs HBTs. The model provides detailed diagnosis of nonlinearity in the Doherty amplifier. Accordingly, simple circuit modifications were made to significantly enhance linearity. Experimental results demonstrate the efficacy of this analytical model.

Chapter 1

Introduction

1.1 Power Amplifier Background

The power amplifier is the final active device before the antenna in a wireless transmitter. From its name, the function of a power amplifier is to amplify the output signal. Because of the large amplitude of signals in it, the power amplifier is considered a critical component of the transceiver and the signal integrity of power amplifier significantly influences the performance of the entire system. Furthermore, due to its often dominant DC power requirements compared to the other components of the transceiver, the efficiency of the power amplifier has a major impact on the overall efficiency of the system. Fig. 1.1 is a typical RF transceiver architecture, in which the power amplifier is highlighted at the end of the transmitter chain.

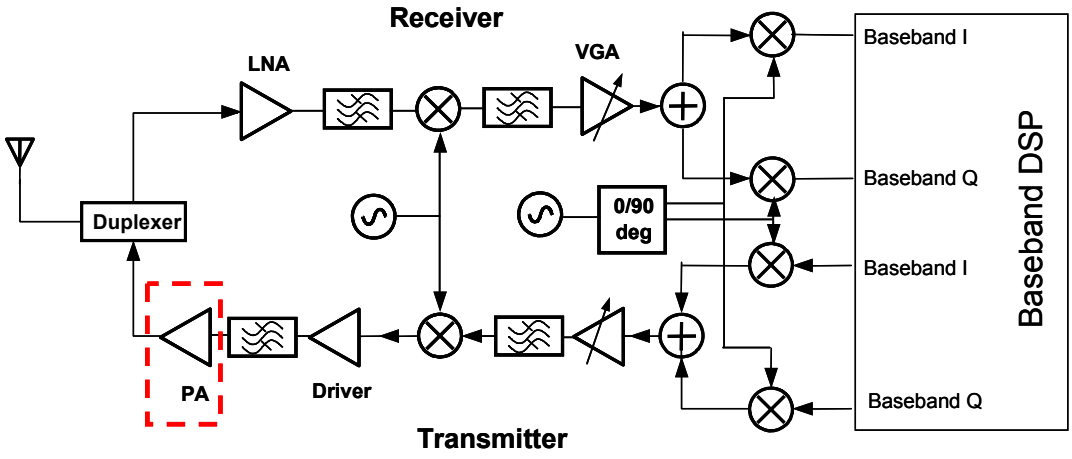


Figure 1.1: A typical wireless transceiver architecture with the power amplifier highlighted

Today, there are many commercial or military wireless standards that co-exist in a limited frequency spectrum. The most often used frequency range for a wireless transceiver is from 400MHz to 6GHz. For example, Fig. 1.2 shows a frequency allocation spectrum from 1.7GHz to 2.7GHz by the National Telecommunications and Information Administration of the United States. As the figure shows, there are numerous applications where radio transceivers, and the power amplifiers within, can be potentially implemented. In many commercial applications, there exist needs to switch from one application (frequency) to another within one portable device. In military applications, a wideband transceiver is often desired inside intelligent front-ends. All these needs can be accommodated by designing multi-mode multi-band transceivers and power amplifiers. Consequently, tunable power amplifiers which can be tuned into different frequency bands have attracted great interest recently [1], [2].

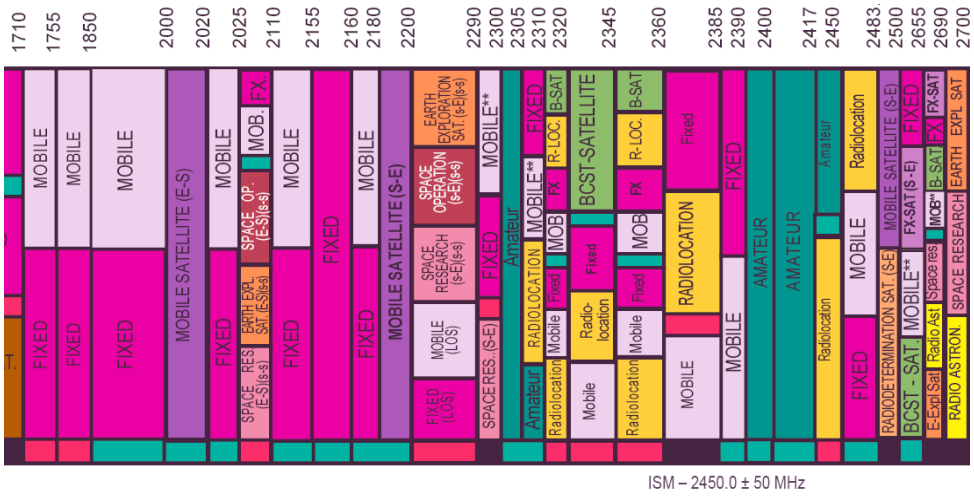


Figure 1.2: Frequency allocation spectrum from 1.7-2.7GHz in the U.S (circa 2003) http://www.ntia.doc.gov/osmhome/allochrt.pdf

Popular transistors used in power amplifier designs in portable transceivers are MESFETs, PHEMTs, and the HBT device family, which includs InGaP/GaAs HBT, SiGe HBT and InP HBT. Although the last one is most often used for millimeter wave amplifier designs, there are some efforts to use it to achieve high performance in lower frequency applications. Fig. 1.3 is a photograph of an InGaP/GaAs HBT based power amplifier (packaged) mounted on an evaluation PCB board (courtesy of Skyworks Solutions Inc).

CMOS technology was traditionally considered not suitable for power amplifiers with more than 20dBm output power, however, there have been strong efforts recently to prove that CMOS can provide far greater powers. In base-station power amplifiers, MESFETs, LDMOS, GaN are suitable devices.

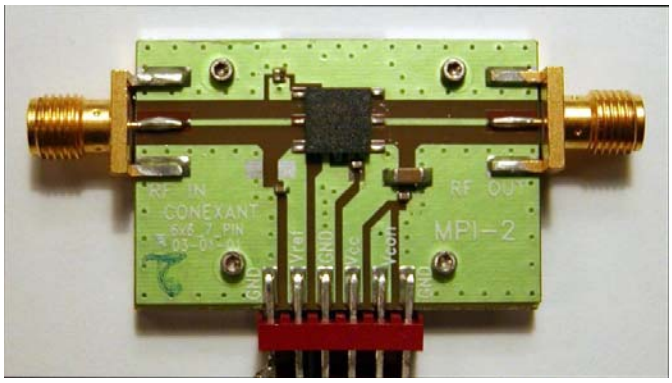


Figure 1.3: An InGaP/GaAs HBT power amplifier mounted on module (Skyworks)

1.2 Categorizing Power Amplifiers

A classic way to categorize power amplifiers is based on the time domain waveforms appeared in a power amplifier. With different conduction angles of their time domain current waveforms, Class A, Class B and Class C amplifiers are defined.

Class A amplifier has the full 360º conduction angle but the lowest peak efficiency among the three at 50%. Class B amplifier has 180º conduction angle and a peak efficiency of 78.5%. Class C can achieve a higher peak efficiency than that of Class B but also has an even smaller conduction angle. Extensions of these basic types of amplifiers, Class D, Class E and Class F amplifiers have come into being to use waveform engineering mainly to achieve higher peak efficiency. Since they have square waveforms in current or voltage and the transistors are acting as switches, Class D, E, and F amplifiers are called switching-mode amplifiers. They can theoretically achieve 100% efficiency. However, in practice, all face different design challenges depending on specific requirements of applications.

In most power amplifier applications, it is desirable to have the highest possible output power with the least device area consumed. In case of base-station power amplifiers, higher breakdown voltage devices are being developed to enhance the power performance of the amplifier. In handset power amplifier case, especially amplifiers designed with short-channel CMOS process, thick oxide device or stacked transistor structures are used to achieve higher power drain to source breakdown voltage and hence a more favorable load impedance matching.

In applications where high linearity is required, linearization techniques are introduced to improve linearity of amplifiers. For better efficiency and linearity tradeoff, methods to improve average efficiency have been actively investigated. In the following part of this section, a brief survey is conducted to cover and sort out all the amplifier categories mentioned above.

1.2.1 Basic Types of Power Amplifiers

In some low frequency analog amplifier designs, Class A amplifier is the typical choice as the power efficiency is not of particular concern. In situations such as the final stage of a wireless handset, power amplifier needs to be more efficient than a Class A amplifier to cut down the overall DC consumption. Nonetheless, class A amplifier is the very basic type of amplifier to begin with in any study.

Class A amplifier is always on, and thus has a constant conduction angle of 360º as shown in Fig. 1.4. Its peak efficiency is only 50%. It is inefficient because the DC current is wasted in the bias even with zero input power. But the class A amplifier is very linear. There's no waveform clipping introduced before the amplifier saturates.

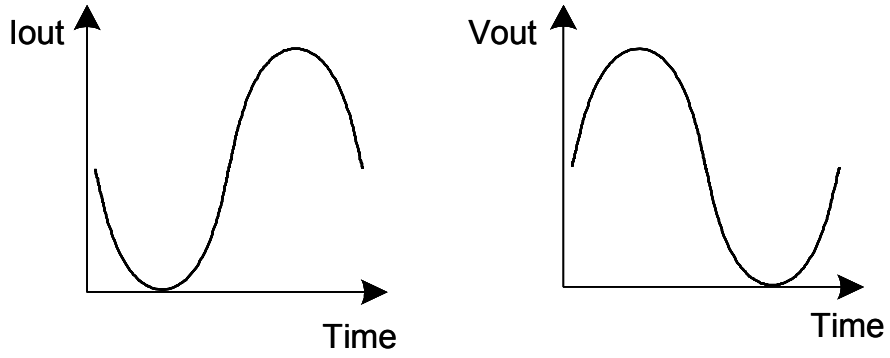


Figure 1.4: Voltage and current waveforms in a Class A amplifier

A Class B amplifier has a 180º conduction angle. A class B with push-pull structure can have a 360º conduction angle and 78.5% peak efficiency at the same time, however it requires more complex circuit. A further problem is that the requirement of a high speed P-type device makes it difficult to realize in RF frequency. There are alternative ways to use all N-type devices, but they require smart design of combiners, which still pose challenges for compact circuit designs in RF frequency. A

stand alone Class B amplifier is a good choice for efficiency but not for gain or linearity. For a best trade off between efficiency and linearity, most power amplifiers in mobile systems are biased between Class A and Class B, and called Class AB amplifier.

A Class C amplifier is even more efficient than a Class B amplifier and can theoretically achieve 100% efficiency [3]. However, the conduction angle in a class C amplifier is small and only a small portion of the input signal is utilized and amplified as shown in Fig. 1.5. Subsequently, its gain is low and that necessitates a very large input to achieve a desired output power level. A true class C amplifier was considered not very suitable for wireless portable transmitters. Nonetheless, Class C amplifier was actually explored to in a wireless Communication scenario by researchers in U.C. Berkeley [4], [5]. The schematic of their design is shown in Fig. 1.6. In this case, the amplifier is biased with zero quiescent current. When input power increases, the bias point will shift away from the quiescent point with self-bias effect, which results from nonlinearity of the amplifier transistor and the bias circuit. So the amplifier is operating similarly to a Class AB amplifier at high input power, thus provides enough gain and output power. This class C amplifier can reach 1.2W output power and 40% drain efficiency using 0.35um CMOS technology. However, large gain expansion in class C amplifier can cause large nonlinearity when amplitude modulated signal is used, making it only a good fit for systems with constant envelop signals like GSM.

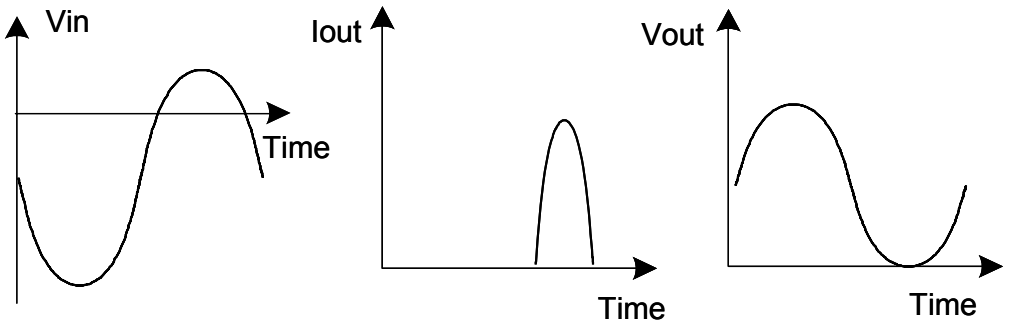


Figure 1.5: Voltage and current waveforms in a Class C amplifier

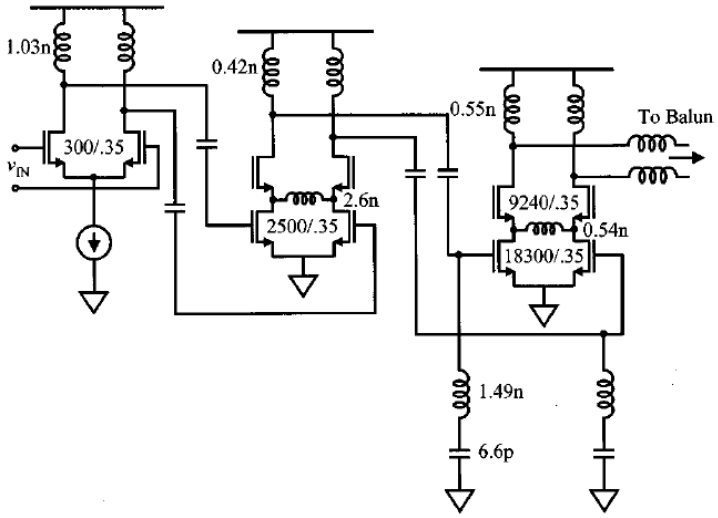


Figure 1.6: An example of Class C amplifier design (U.C. Berkeley)

1.2.2 Switching Mode Amplifiers for Peak Efficiency Enhancement

In a switching mode amplifier, the transistor operates as a switch rather than a voltage dependent current source. It achieves high efficiency by meeting the condition of non-overlapping current and voltage waveforms. In order to achieve that, transitions from on to off in the switch need to be made rapidly. Output harmonics need to be properly terminated to shape either the current or the voltage waveform into square

waves. Traditionally considered a drawback for the switch mode amplifier is the need for a DC-DC converter for power control. There is no other way to power control without controlling the supply voltage. However, this actually is becoming the strength of the switch mode amplifier with the growing popularity of the polar loop modulation, where the switch mode PA can naturally fit in.

Class D, E, F amplifiers are the most popular switch mode amplifiers. In a Class D amplifier, the amplifier is made to act like a switch. In a Class D amplifier, switch current and switch voltage do not have any overlapping non-zero instance. Hence, there is no loss in the switch. Depends on whether the voltage is a square wave or the current is, the Class D is classified into voltage mode Class D or current mode Class D. Assuming all reactive components have infinite Q, 100% efficiency can be achieved. In a practical voltage mode Class D amplifier, the presence of parasitic capacitance of the active device prevents voltage on switch from changing abruptly, causing the voltage and current waveforms to overlap. This results in power loss in the switch, and therefore drives efficiency below 100%.

A possible solution is current mode class D amplifier as shown in Fig. 1.7. The series LC tank forces the load voltage, V1, to be sinusoidal. Since parasitic capacitors can be absorbed into the tank capacitor C, the current mode Class D amplifier can significantly reduce the capacitive loss and improve the efficiency of the Class D amplifier [6], [7].

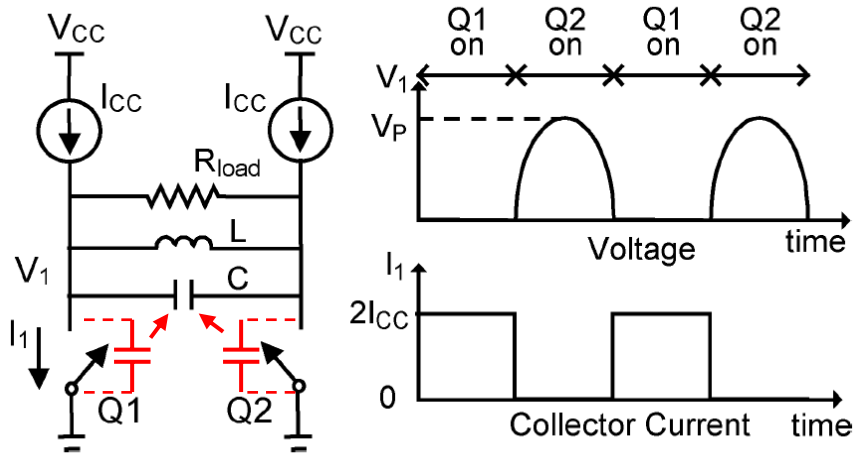


Figure 1.7: Current mode Class D amplifier and its waveforms (UCSD)

Class E amplifier was introduced to solve the parasitic capacitor problem of a transistor by using extra tuning components to resonate it out and thus ensure a zero voltage switch (ZVS) in the amplifier. A schematic of Class E amplifier and waveforms in it are shown in Fig. 1.8. Class E amplifier was first defined by N. O. Sokal and A. D. Sokal in their famous paper [8]. It is believed to be able to achieve a efficiency closer to 100% than a Class D amplifier. However, it requires sharp change in the time domain waveform and can impose a few times higher peak voltage, making it difficult to realize using modern low breakdown voltage CMOS devices. Decent work has been done by varies research groups to show promising usage of class E amplifier in portable transceiver scenarios [9].

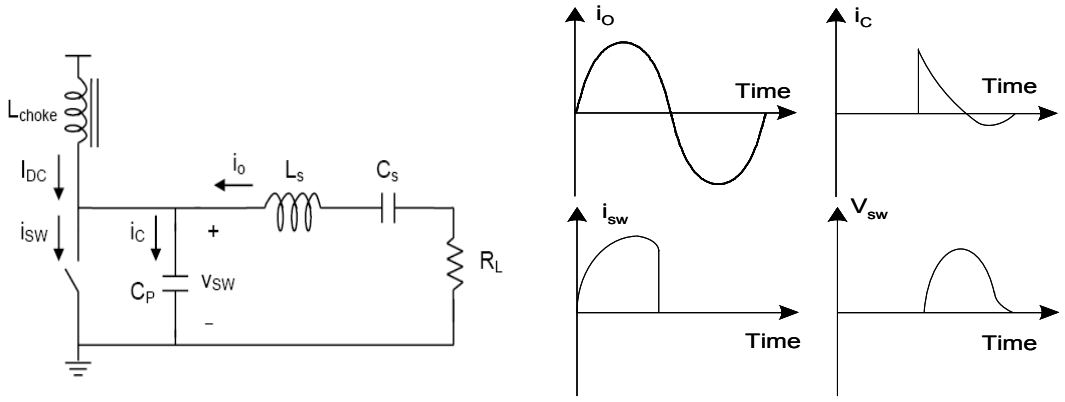


Figure 1.8: Class E amplifier and its waveforms

Class F amplifier uses harmonic terminations at the output of the amplifier to shape the time domain wave form of the voltage by adding 3rd order harmonics and other odd order harmonics [10]. That makes the voltage waveform more square-like, helps to reduce voltage and current overlapping and thus increases the efficiency. Just like current mode Class D amplifier, one can also try to make the current wave square-like in a Class F amplifier, which makes it an 'inverse class F amplifier' [11].

Class E and F amplifiers are considered closely related with differences made in the load tuning. A work done Scott Kee and colleagues in Caltech shows a family of Class E/F amplifiers having the feature of ZVS of Class E. These amplfiers also have different tuning in harmonics to make additional adjustment of current waveforms compared with standard Class E amplifier and subsequently achieve small difference in efficiency and gain tradeoffs [12].

1.2.3 Techniques for Output Power Enhancement

The first and foremost requirement of the power amplifier is the ability to deliver power. Also, cost of a power amplifier is heavily related to the output power per unit area.

For basestation applications, with no limitation on the supply voltage, increase of breakdown voltage in the amplifier devices can help improve many things. First, it enhances the output power by sustaining higher supply voltage; second it increases efficiency because increase of supply voltage can lead to higher optimum load impedance and thus enables low loss output matching. Si LDMOS has been a popular transistor choice for base-station high-power amplifiers since LDMOS technology can provide reliable and cost-effective solutions [13]. However, in order to obtain better linearity and efficiency for third-generation (3G) wireless base stations, intense research on high-voltage GaAs heterojunction bipolar transistors (HBTs) [14] and field-effect transistors (FETs), as well as GaN heterostructure field-effect transistors (HFETs) has been carried out. GaN HFETs can provide higher voltage operation and higher power density at microwave frequencies than other high power devices and thus are attractive for application to commercial high-power base stations [15].

For handsets, GaAs HBTs have been dominant. Although thought about for a long time, only in recent years, CMOS based power amplifiers have been considered seriously. The reason is that contemporary CMOS processes have been scale down to deep sub-micron gate length and breakdown voltage (V_{ds}) of CMOS devices has shrunk to below 2 Volts. With that small voltage, in order to put out large amount of power, one needs to parallel so many devices that would dramatically lower the

optimum load impedance. This causes a big problem because the low impedance matching can not be achieved without significant loss by using low quality on chip passive components, especially low quality factor inductors. One of the significant works to solve the above problem is done by Caltech, in which distributed active transformers (schematic shown in Fig. 1.9) were used to achieve low loss output impedance matching network. As reported, 1.9W output power and 41% efficiency are achieved with a supply voltage of 2V at 2.4GHz [16].

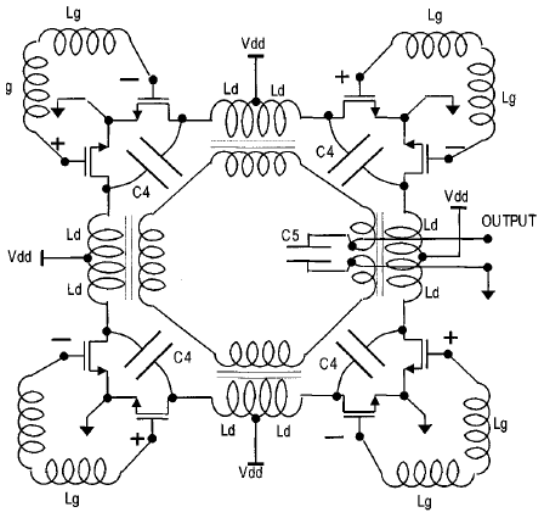


Figure 1.9: CMOS based Distributive Active Transformer (DAT) structure (Caltech)

Alternative ways to design CMOS power amplifiers are to use either thick oxide gated CMOS device for final stage of a power amplifier[17] or to use stacked transistor structure [18]. Both are used to help the CMOS device to sustain higher supply voltage and thus improve power performance just like the case of using higher breakdown voltage devices for basestation amplifiers. Examples are shown in Fig. 1.10 and 1.11.

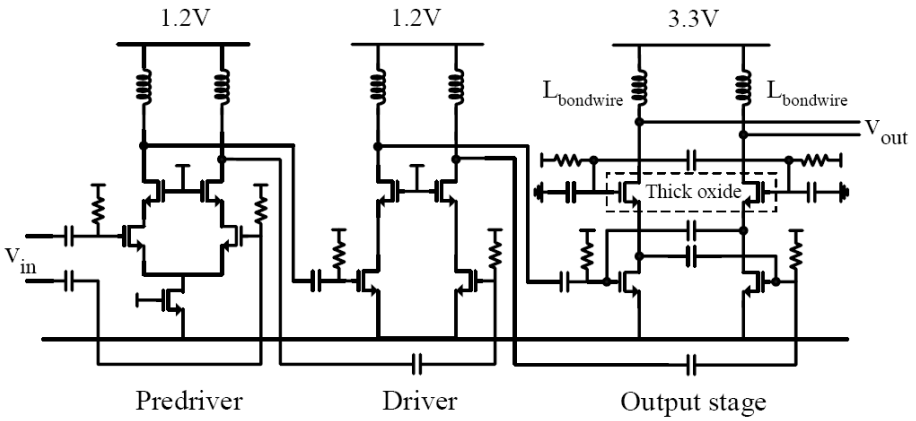


Figure 1.10: A CMOS amplifier using thick oxide and cascode structure (U.C. Berkeley)

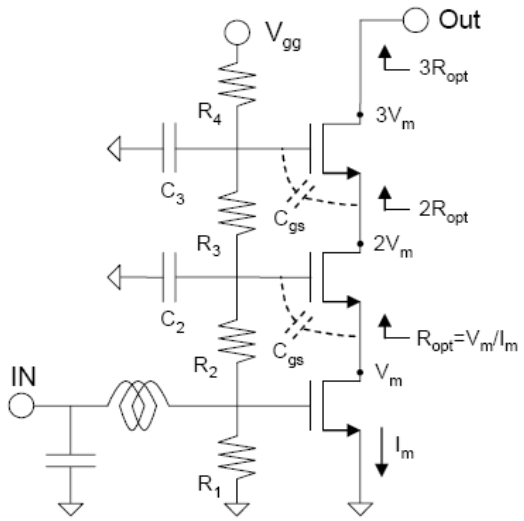


Figure 1.11: A stacked transistor structure using SOS (silicon-on-sapphire) MOSFETs (UCSD)

1.2.4 Architectures for Linearity Improvement

Linearity is always a key issue in designing a power amplifier. Most of today's communication systems can't afford to lose spectrum efficiency by not utilizing amplitude modulation. With amplitude modulation, nonlinearity in amplitude introduced by an amplifier can result in spectrum regrowth and cause interference with

adjacent channels. Certain linearity requirements need to be met by the amplifier to avoid this from happening. The amplitude modulation also introduces peak to average ratio (PAR) for the signal. For an amplifier to meet linearity requirement, input power typically has to be backed off according to the signal PAR. The larger the PAR is, the more the amplifier needs to be backed off. With power backed off, efficiency of the amplifier drops significantly. This is not a satisfying solution. Linearization techniques are needed to improve linearity with less power back-off. Traditional ways to improve linearity of a power amplifier include feedback, feedforward, predistortion and post-distortion.

1.2.4.1 Feedback

While good in principle, direct RF signal feedback is hard to achieve in reality because it requires a fast feedback loop to maintain loop stability. In contrast, envelop-rate feedback is a popular practice in base station amplifier designs. Cartesian feedback is an old concept and was popular in base-station amplifier design for some time. However, there are only a handful of successful examples in which it is implemented for a compact integrated amplifier. J. L. Dawson demonstrated method with a novel phase alignment loop [19]. In that work, a special phase alignment circuit block using a nonlinear regulator concept is introduced to ensure a good performance of the feedback loop and the resultant linearity enhancement for the power amplifier system. The whole thing is integrated on CMOS chip.

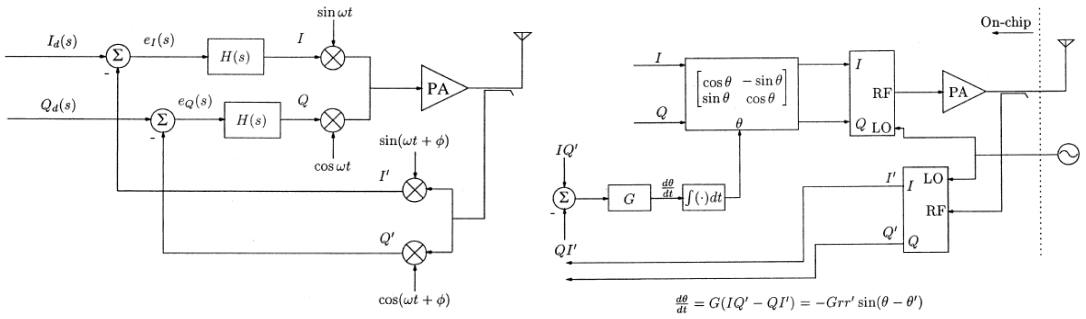


Figure 1.12: A standard Cartesian feedback loop Topology and a phase alignment feedback loop (Stanford)

1.2.4.2 Feedforward

Feedforward was the most powerful way to linearize a power amplifier over 10 years ago, and is still dominant for broad bandwidths. An example of feedforward schematic is shown in Fig. 1.13. By using first loop carrier cancellation and second loop distortion cancellation, it can easily achieve more than 40dB improvement of linearity, whether in terms of ACPR or IMD3. However, since the two loop structure and the strict requirements on circuit components matching for an accurate cancellation, the feedforwad system is definitely not a good choice for a compact amplifier system. Moreover, the use of a linear error amplifier in the second loop for cancellation of output distortions reduces overall efficiency of the system to the 7-15% range, unacceptable for some systems. Even by using advanced amplifier structures like Doherty amplifiers to improve efficiency at the main amplifier in the feedforward system, overall efficiency is still limited by the drawbacks inherent in the feedforward structure [20].

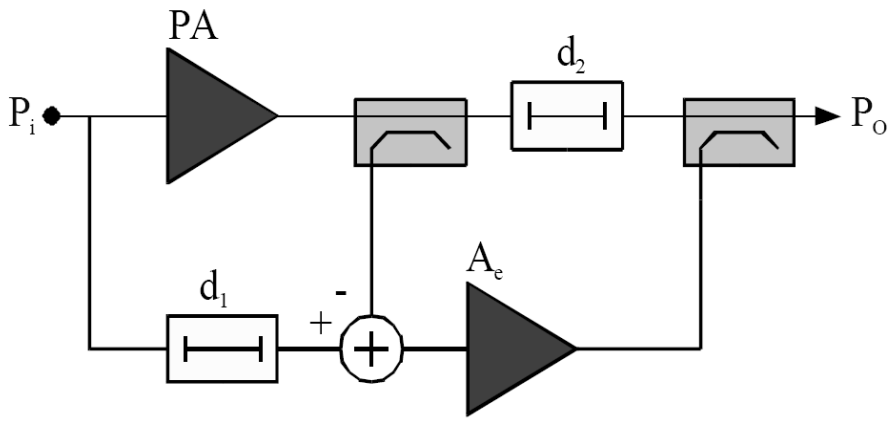


Figure 1.13: A simplified feedforward amplifier linearization topology

1.2.4.3 Predistortion

Digital predistortion is a dominant choice in contemporary base station amplifier designs. It provides very good performance and great flexibility by using an adaptive digital closed-loop control [21]. Advanced algorithms such as the genetic algorithm can be used to improve computation efficiency in the digital domain. However, using digital predistortion for handset amplifiers is still not popular due to the concerns of circuit complexity and cost. A typical block diagram of digital predistortion is shown in Fig. 1.14. It employs an auxiliary down converter to feedback the complex envelope of the output signal back into digital domain. This is compared with original data in look-up and to achieve adaptive adjustment.

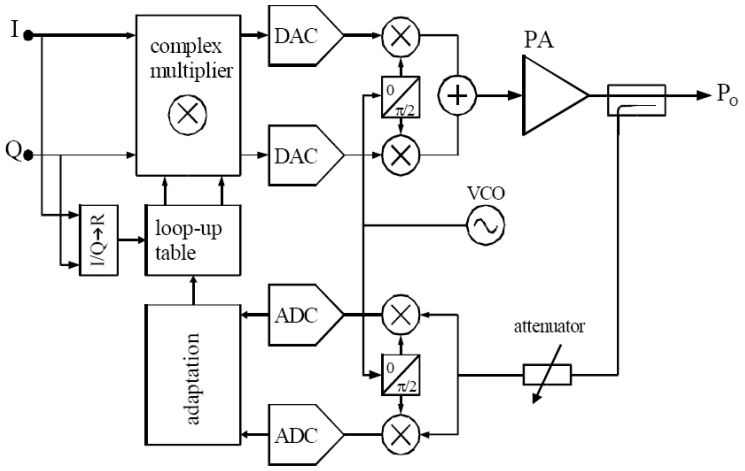


Figure 1.14: A typical block diagram of digital predistortion

Analog predistortion is by far one of the only viable ways to achieve linearity improvement in a compact handset power amplifier, although it only achieves moderate linearity improvement and usually can not adapt over a wide dynamic power range or a wide temperature change. A diode based analog predistortor was presented in [22] and its structure is shown in Fig. 1.15. If the nonlinear gain and phase transfer functions introduced the diode are inverse to those of the power amplifier following it, the input signal can be properly predistorted. This method is really popular in practice because of its simplicity and its ability to enhance maximum output power by 1-2 dB, where the efficiency and linearity of the amplifier matter the most. In fact, with the goal of same output power, having a 1-2dB enhancement from the predistortor translates to 25-50% saving of active device area. With that, either cost can be saved or additional functionality can be added without additional cost.

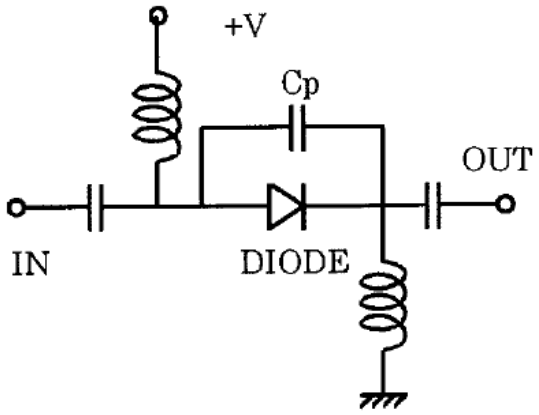


Figure 1.15 A diode based analog predistortor (Sharp Corp.)

Apart from what is considered a linearizer such as a simple diode, one can use a digital controller to control analog components to achieve 'analog component based predistortion'. Research done at Intel gives a good example [23], with the schematic shown in Fig. 1.16. Even though it has the same level of complexity as a digital predistortion scheme, an 'analog component based predistortion' has advantages in requiring less bandwidth on DACs and filters.

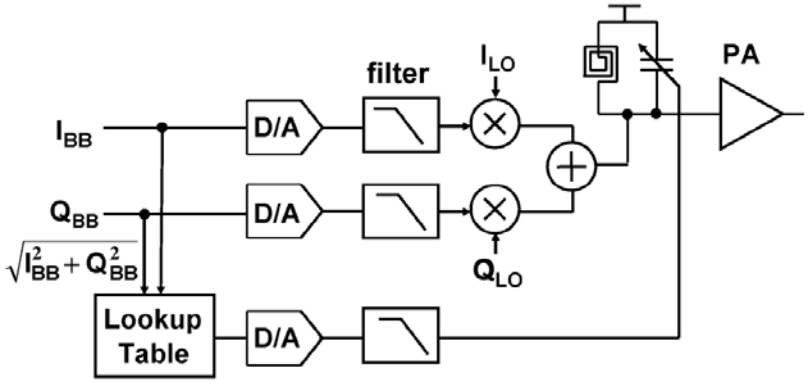


Figure 1.16: An example of 'analog component based predistortion' topology (Intel)

Another linearization technique is post-distortion, but in case of a power amplifier, doing anything after the amplifier introduces concerns about loss and

efficiency. Post-distortion is more suitable for LNA applications with lower output power requirements [24].

1.2.5 Advanced Amplifier Schemes for Average Efficiency Improvement

Recent advances in amplifier research have been mostly focused on improving the efficiency of the amplifier. Improvement of peak efficiency by means of a switching mode amplifier is only one side of the story. Improvement of average efficiency is often of more importance. Previously, designers paid the most attention to power added efficiency at the maximum output power. But focusing on average power efficiency instead of peak efficiency may make more sense, because average efficiency takes into account the power consumption in low output power range, it determines the talk time and battery life. Maximum output power will be achieved only when handsets are very far away from the base station, which occurs rarely in reality. It is nice to have high peak efficiency by using a Class D or a Class E amplifier. However, that does not necessarily improve average efficiency of an amplifier by much. Moreover, switching mode amplifiers are nonlinear and not suitable for systems with high linearity requirements. In the following, we discuss three directions to improve average efficiency of an amplifier.

1.2.5.1 Reduce Bias Current

One direction is to save DC power consumption by reducing quiescent bias current which may be minimized when the input power is small. However, since the quiescent bias current in a typical Class AB amplifier is already low, the saving by further cutting it can only provide limited improvement on overall efficiency. To

further help with the issue, work has been done by J. Deng and his colleagues in UCSD to switch off part of the transistor in low power levels to further reduce unnecessary DC power consumption [25].

1.2.5.2 Reduce Supply Voltage

This is now called Envelope Elimination and Restoration (EER). A similar technique is the Envelope Tracking (ET). But the story started with the Kahn modulation [26] [27]. It was further explored by D. Su with DC-DC converter implemented to modulate supply voltage of the power amplifier and thus reduce DC power consumption at low input power [28]. The scheme is so popular recently because it can utilize the high efficiency performance of the switch mode amplifiers very well. The amplitude modulation is carried out by modulating the supply voltage of the amplifier, leaving the main amplifier with only a phase modulated signal with constant amplitude. This enables high efficiency operation of the main amplifier since the device can always work in saturation. A nonlinear switch mode amplifier can be effectively used and its high peak efficiency can now transform to high average efficiency of the system. The use of switch mode amplifier is also very suitable for the push of CMOS or SiGe power amplifiers, which can potentially lead to a complete integration of the EER transmitter [29].

Polar loop modulation generally has a broader meaning than the EER. In a polar loop transmitter, the amplitude and phase modulation is also carried separately, but the amplitude modulation is not necessarily realized by supply voltage modulation. Many research papers have been published on this topic. [30]-[33]. An interesting

further step is the polar modulation approach proposed by Texas Instrument [34]. In their work, the amplitude modulation was realized by switching on and off transistors in the amplifier transistor array. The amplitude input is digitally modulated, so is the phase input, which is fed directly into the amplifier. The schematic of the method is shown in Fig. 1.17. The method is claimed to be the first suitable structure for an all digital polar loop transmitter.

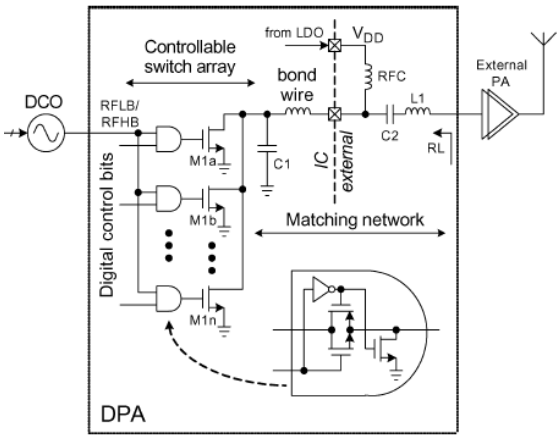


Figure 1.17: Digital modulated polar loop amplifier scheme by Texas Instrument

1.2.5.3 Increase Load Impedance

There are some proposed amplifier structures with tuned load impedance, changed by switches and capacitors. However, these approaches are usually too lossy with on chip passive components at the output of the amplifier, and the tuning can not be done automatically for all the power ranges. A more attractive way is to use an active device as a tuning component. The most important example of this is the Doherty amplifier, which is the main focus of this dissertation. Its origins date back to 1930s [35], but regained interest recently in wireless applications [36]-[55]. It uses an auxiliary amplifier to actively load the main amplifier. At low power, only the main

amplifier operates, and it is configured to have a high load impedance, thus saturates at a relatively low input power and achieves high efficiency at low power. The auxiliary amplifier is biased in Class C and turns on after the main amplifier saturates. It pulls the main amplifier out of saturation by changing its load impedance to a lower value. Overall, the Doherty PA can achieve extended high efficiency.

It is worthwhile to point out that there is no fundamental limitation that stops simultaneous use of multiple methods, but most often the system gets too complicated and does not provide much more improvement than using one method.

1.3 Performance Metrics for Power Amplifiers

Listed in table 1.1 is a range of performance parameters available in amplifiers designed for portable systems.

Table 1.1: Typical PA performance parameters in wireless communications

Frequency Range	0.4 to 6GHZ
Output Power	0.1 to 2W
Efficiency	30 to 60%
IMD3	-30 to -40dBc
Supply Voltage	1.5 to 3.4V
Gain	10 to 20dB
Output Spurs and Harmonics	< -30 dBc
Thermal noise floor at receiver band	< -130dBm/Hz

1.3.1 Power

The Output power of a power amplifier (P_{out}) is defined in watts or in dBm. P_{1dB} is the point at which P_{out} is 1dB less than its linearly projected value. Related to

P_{1dB} by the linear projection of power is 3rd order Output Intercept Point --- OIP_3. It is defined in a two tone test. It is the point where the extrapolated line of 3rd order inter-modulation product intersects with the linear projection line of fundament output power. OIP_3 is roughly 10dB higher than P_{1dB}. P_{max} (or P_{sat}) is the maximum power the amplifier can reach. It can be estimated by using output I-V curve of the transistor as explained in Fig. 1.18. P_{max} is roughly 2-3 dB higher than P_{1dB}. All these definitions of output power are illustrated and compared in Fig. 1.19.

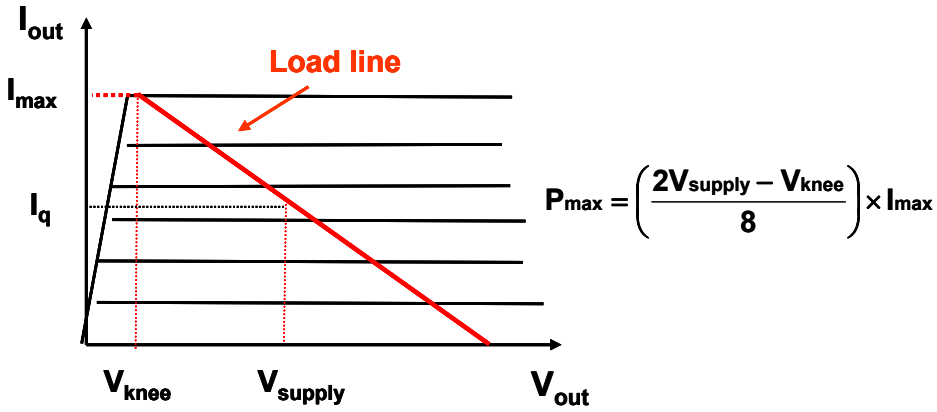


Figure 1.18: Estimation of P_{max} based on transistor I-V curve

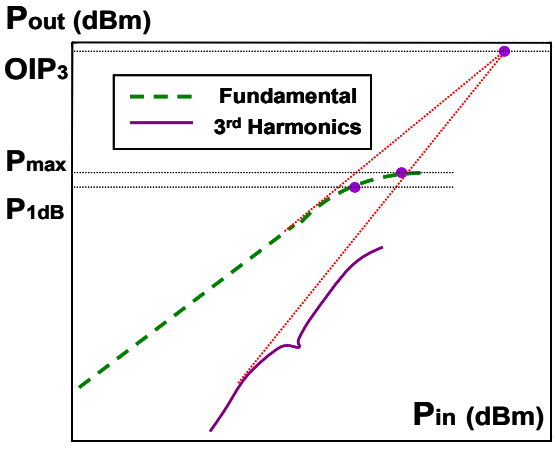


Figure 1.19: Different definitions of power P_{1dB}, OIP_3 and P_{max}

1.3.2 Efficiency

Drain (or collector) efficiency of the amplifier is defined as:

$$DE\,(\%) = \left(\frac{P_{out}}{P_{DC}}\right) \times 100 \tag{1-1}$$

Power added efficiency (PAE) is often a better measure of efficiency than drain efficiency because it takes into account efficiency of the circuits needed to drive the amplifier. It is defined as:

$$PAE\,(\%) = \left(\frac{P_{out} - P_{in}}{P_{DC}}\right) \times 100 \tag{1-2}$$

The average power added efficiency is a measure of the ratio of the total energy transmitted to the output, to the total energy drawn from the battery. It is a better measure of efficiency in systems with a dynamic signal probability distribution function (PDF) because it takes into account DC energy dissipated with varies level of input power. It is defined as:

$$\langle PAE \rangle = \frac{\langle P_{out} \rangle}{\langle P_{DC} \rangle} \times 100 = \frac{\int P_{out}\, p(P_{out})\, dP_{out}}{\int \frac{P_{out}\, p(P_{out})\, dP_{out}}{\eta(P_{out})}} \times 100 \tag{1-3}$$

Here P_{out} is the output power, $p(P_{out})$ is probability of a certain output power $P_{out,}$ and $\eta(P_{out})$ is the power-added efficiency at P_{out}. A representative data of $p(P_{out})$ for CDMA signal is shown in Fig. 1.20. Also plotted in Fig. 1.20 is a PAE curve for a typical Class AB power amplifier.

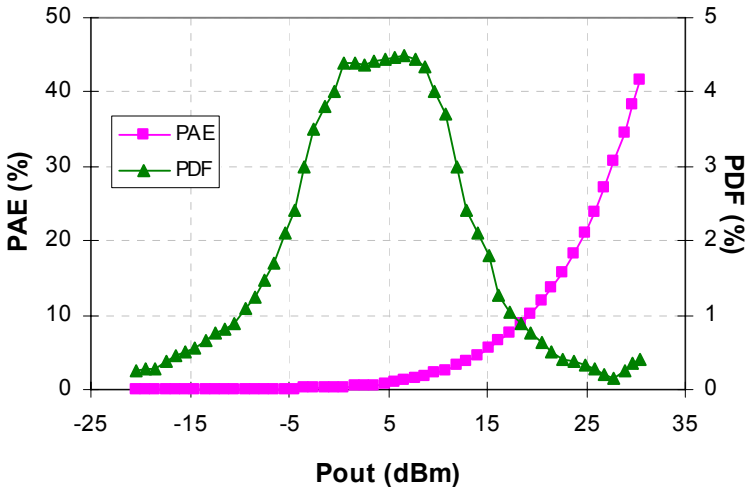


Figure 1.20: Representative CDMA PDF data and PAE data of a Class AB PA

The average output power of a CDMA handset is well below the peak output power, where efficiency is a maximum, so it is very desirable to improve the PAE of the amplifier at lower output powers. The typical CDMA/WCDMA power amplifiers average efficiency is rather low, at less than 5%. So, on average, well over 90% of the energy used for driving the power amplifier is turned into waste heat.

1.3.3 Linearity

Although they are not accurate measures of linearity, the gain and output phase vs. power of a power amplifier are the first things to check for a rough estimation of linearity. Sometimes when gain and phase are plotted versus input power, they are referred to as AM-AM and AM-PM distortion characteristics. If gain or phase variation is large, especially when the derivative of the variation is large, linearity of the PA is bad. For a first order representation of the PA, one can use the following equation:

$$V_{out}(P_{in}) = V_{in}\, G(P_{in}) e^{j2\pi\Psi(P_{in})} \qquad (1\text{-}4)$$

Here $G(P_{in})$ is the gain and $\Psi(P_{in})$ is the phase. A more complete PA nonlinearity model will be needed to include memory effect and in general out of band load impedance effects for all harmonics.

Measures of linearity are IMD3, ACPR, ACLR and EVM. IMD3 is the difference between fundamental output power and 3rd order inter-modulation product power when the input is a two tone signal. ACPR is the adjacent channel power ratio and ACLR is the adjacent channel leakage ratio. The definitions of ACPR and ACLR are explained in Fig. 1.21. $P_{channel}$ is defined as the integrated power over the desired signal bandwidth. $P_{adjacent}$ is defined as the integrated power over the adjacent channel. P_{offset} is the accumulated power over a 30KHz bandwidth (in the case of IS-95 and CDMA2000) at a designated offset frequency from center. ACPR = $P_{channel}$ -P_{offset} and ACLR = $P_{channel}$ - $P_{adjacent}$. Channel bandwidth and offset frequency can vary in different standards.

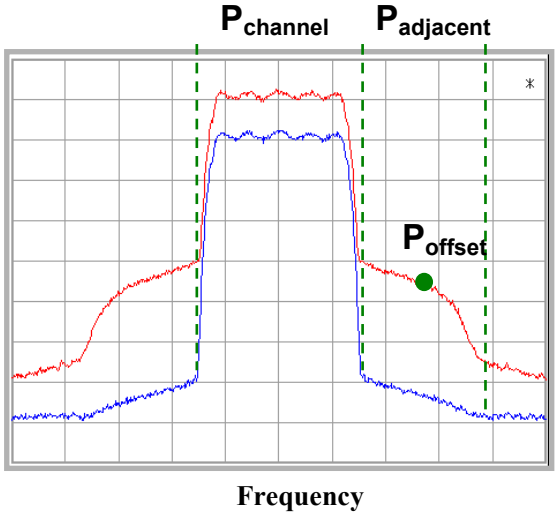
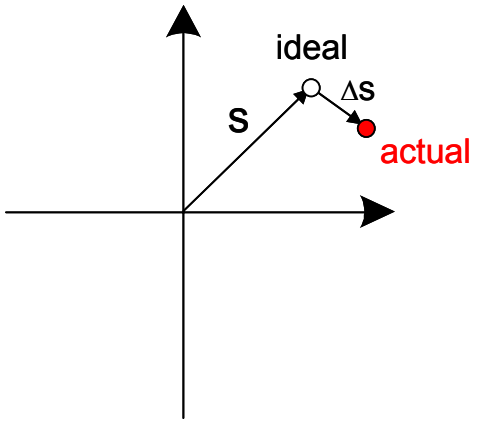


Figure 1.21: Definition of ACPR and ACLR in CDMA system

EVM is error vector magnitude. When the output signal is distorted, there is difference in the I-Q plane, between the actual signal and the ideal output. The difference between them is defined as error vector. EVM is subsequently defined as ratio of magnitude of error vector to that of the ideal signal vector as illustrated in Fig. 1.22.



$$EVM = \frac{\Sigma|\Delta s|}{\Sigma|s|}$$

or

$$EVM = \Sigma\frac{|\Delta s|}{|s|}$$

Figure 1.22: Error vector magnitude (EVM) definition

1.4 Scope of Dissertation

The Doherty amplifier structure has been focus of many research papers. However, more research needs to be done to improve the efficiency and the linearity performance of Doherty amplifiers. The objective of this dissertation is to analyze practical design issues for a Doherty amplifier and to provide solutions that lead to a simultaneous high efficiency and high linearity performance. By carefully investigating characteristics of Doherty amplifiers in simulations and experiments, a new digital signal processor (DSP) control strategy was developed and shown to significantly improve the linearity of a Doherty amplifier based on GaAs FETs while

maintaining its original high efficiency performance. Furthermore, with a developed analytical model, the nonlinear behavior of a Doherty amplifier based on InGaP/GaAs HBTs can be examined in detail which leads to improved linearity through simple circuit modifications.

The structure of this dissertation is as follows:

Chapter1 surveys power amplifier back ground. It describes different type of amplifiers including Class A, B, C, D, E, and F amplifiers. Techniques for output power, linearity and average efficiency enhancement are also discussed and examples are given. A range of performance parameters for the power amplifier is given and described in detail.

Chapter 2 gives an overview of the operation of Doherty amplifier based on simplified current source transistor model. It also examines the practical circuit design considerations for a Doherty amplifier, including load impedances, device size, input uneven splitting, bias of the auxiliary amplifier, and harmonic terminations. Simulation and measurement results of a Doherty amplifier implemented with GaAs FET devices are then discussed. This provides a description of performance issues of a Doherty amplifier. For the purpose of demonstrating the possibility of an integrated Doherty amplifier, a lumped element based Doherty amplifier was built and its performance investigated.

Chapter 3 discusses Doherty amplifier linearization techniques based on DSP control. Special characteristics of Doherty amplifiers are shown to justify controlling the input bias voltage of the auxiliary amplifier. DSP was utilized to mitigate variations in gain through input bias control and to eliminate phase distortion through

baseband phase predistortion. It is shown that, with IS-95 as input signal, the DSP controlled Doherty amplifier can achieve high PAE performance while satisfying the linearity requirements. Advantages of analog component based predistortion were studied and demonstrated by experiments.

Chapter 4 delves into nonlinear behaviors in Doherty amplifiers implemented with HBTs. An analytical model is developed based on full device model. The simplicity of the model enables nonlinearity analysis associated with each nonlinear component in the transistor. This results in accurate distortion prediction for both single-ended amplifiers and Doherty amplifiers. The model helps the diagnosis of nonlinearity in a InGaP/GaAs HBT based Doherty amplifier. As a result, circuit modifications were made and shown to significantly improve linearity of the Doherty amplifier. Furthermore, the new analytical model will be useful for circuit designs where the detailed distortion characteristics of the device are important.

Finally, Chapter 5 summarizes the work presented in this dissertation and suggests future work areas of research.

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Chapter 2

Doherty Amplifier Circuit Design

2.1 Doherty Amplifier Introduction

As briefly introduced in chapter 1, the Doherty amplifier is a type of power amplifier that can achieve high efficiency over a wide range of power levels. A Doherty amplifier comprises a main and an auxiliary amplifier. For a Doherty amplifier to operate properly, the main amplifier needs to see a high load impedance (R_{main} in Fig. 2.1) before the auxiliary amplifier turns on, and thus it saturates and reaches its peak efficiency at a relatively low power level. A correct value of R_{main} is ensured by inserting a quarter-wave transmission-line impedance inverter (with characteristic impedance Zc) between the output nodes of the main and the auxiliary amplifier. As the power level increases, the auxiliary amplifier turns on and the load impedance seen by the main amplifier decreases gradually due to active load-pulling from the auxiliary amplifier. Meanwhile, the combined efficiency of the Doherty amplifier also drops, but then rises again and reaches a second peak when the auxiliary amplifier also goes into saturation. Consequently, the Doherty amplifier can achieve high efficiency over an extended power range by the active load-pulling effect from the auxiliary amplifier.

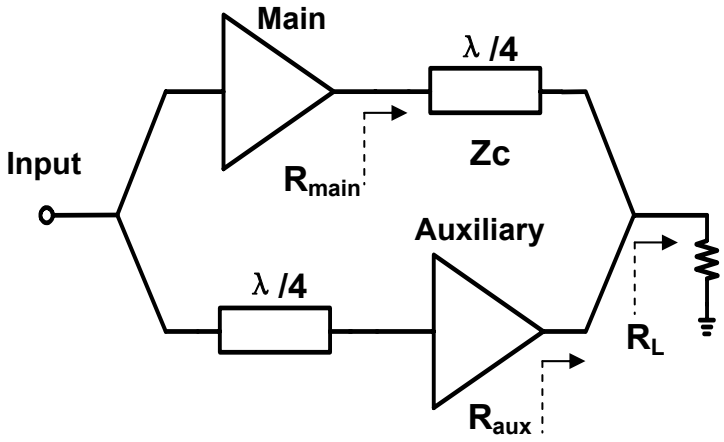


Figure 2.1: A schematic of Doherty amplifier

2.2 Operational Theory of the Doherty Amplifier

2.2.1 Ideal Current Source Based Analysis

If the active transistors in Doherty are simply modeled as ideal current sources (as shown in Fig. 2.2), the operational theory of Doherty amplifier can be simply derived. The analysis is very useful to understand behavior in a Doherty amplifier, although the treatment is ideal.

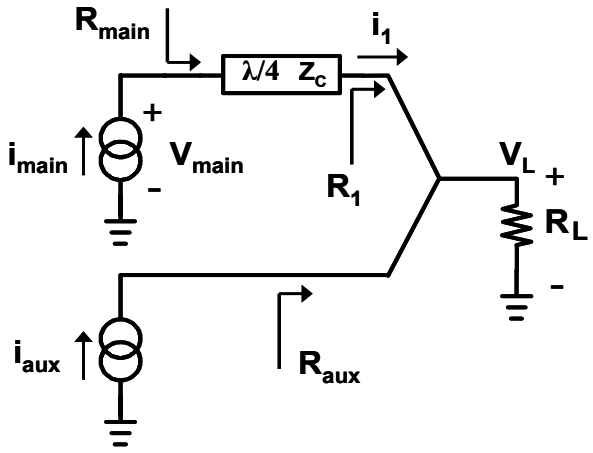


Figure 2.2: Simplified Doherty circuit based on ideal current sources

In this analysis, phasors are used to represent the values of voltages and currents at the fundamental frequency. i_{main} is assumed to be linearly proportional to the input signal voltage. The nodal current relation at the output node provides:

$$\mathbf{i_1 = \frac{V_L}{R_L} + i_{aux}} \tag{2-1}$$

Impedance inversion function of the quarter-wave line and power conservation give the following:

$$\mathbf{\frac{V_{main}}{i_{main}} = \frac{Z_C^{\,2}}{R_1} = \frac{Z_C^{\,2} i_1}{V_L}} \tag{2-2}$$

$$\mathbf{\left|\frac{V_{main} i_{main}}{2}\right| = \left|\frac{V_L i_1}{2}\right|} \tag{2-3}$$

Considering the physical constraints of the quarter-wave line, voltage V_L and current i_1 should both experience a quarter wavelength delay from V_{main} and i_{main}, which can be expressed as an additional –j factor in phasor expressions. This adds a -1 or 180 º phase factor to the product of V_L i_1, thus (2-3) becomes:

$$\mathbf{V_{main} i_{main} = -V_L i_1} \tag{2-4}$$

Combining (2-1) and (2-4):

$$\mathbf{V_L^{\,2} = -i_{main}^{\,2} Z_C^{\,2}} \tag{2-5}$$

Again, considering the 90º phase delay (or –j factor) imposed by the quarter-wave line, the correct solution of V_L to (2-5) is chosen:

$$\mathbf{V_L = -j i_{main} Z_C} \tag{2-6}$$

With (2-6) and (2-1), voltage on the output node of the main amplifier is solved as:

$$\mathbf{V_{main}} = \frac{\mathbf{Z_C}^2}{\mathbf{R_L}}\mathbf{i_{main}} - \mathbf{jZ_C i_{aux}} \tag{2-7}$$

To avoid nonlinearity and to achieve high efficiency, the output voltage swing of main amplifier needs to remain at a constant value (near the supply voltage V_{DD}) after it saturates. This can be achieved by turning on the auxiliary amplifier properly and setting the Z_C value correctly. As M. Iwamoto pointed out in [1], I_{aux} is designed to be:

$$\mathbf{i_{aux}} = \begin{cases} \mathbf{0} & i_{main} < i_{m_peak1} \\ \mathbf{-j\gamma\left(i_{main} - i_{m_peak1}\right)} & i_{main} \geq i_{m_peak1} \end{cases} \tag{2-8}$$

where γ is a design parameter that determines the value of i_{m_peak1} in relation to i_{m_peak2}, the maximum value of i_{main}. i_{m_peak1} is the point where the main amplifier begin to saturate and the Doherty amplifier reaches its first peak of efficiency. i_{m_peak2} is the point where the auxiliary amplifier goes into saturation and the Doherty amplifier reaches its second peak of efficiency.

To ensure a constant $V_{main} = V_{DD}$ after the main amplifier saturates, a necessary condition is that:

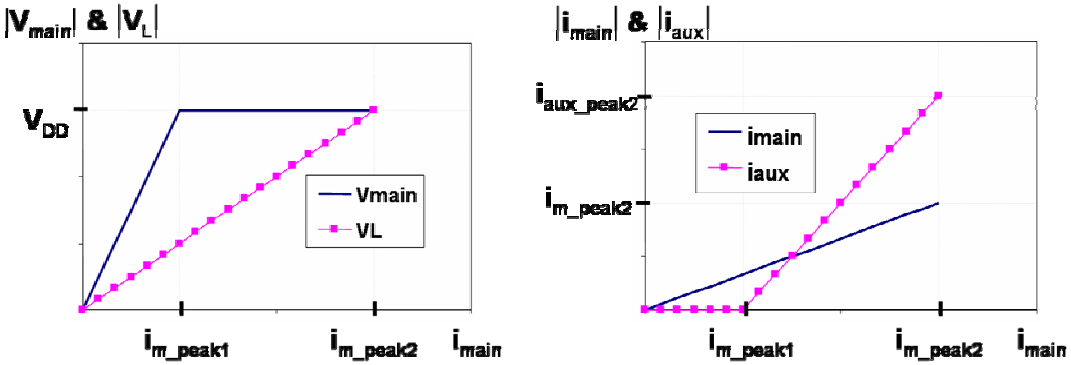
$$\mathbf{Z_C} = \gamma\mathbf{R_L} \tag{2-9}$$

That suggests:

$$\mathbf{V_{DD}} = \gamma^2\mathbf{R_L i_{m_peak1}} \tag{2-10}$$

2.2.2 Voltage and Current Relations

Based on the previous analyses, with i_{aux} defined from (2-8), all the voltages and currents in main and aux PA are derived and can be accordingly plotted in Fig. 2.3 with i_{main} as the independent variable.



(a) **(b)**

Figure 2.3: (a) voltage and (b) current characteristics as a function of i_{main}

A summary of voltages is:

$$V_{main} = \begin{cases} \frac{Z_C^2}{R_L} i_{main} & i_{main} \le i_{m_peak1} \\ \frac{Z_C^2}{R_L} i_{m_peak1} = V_{DD} & i_{main} > i_{m_peak1} \end{cases} \quad (2\text{-}11)$$

$$V_L = -j i_{main} Z_C$$

Some notable relations at the points of i_{m_peak1} and i_{m_peak2} are:

$$\begin{cases} i_{m_peak1} = \dfrac{1}{\gamma} i_{main_peak2} \\ V_L = \dfrac{V_{DD}}{\gamma} \end{cases} \qquad i_{main} = i_{m_peak1} \quad (2\text{-}12)$$

$$\begin{cases} i_{aux_peak2} = -j(\gamma - 1) i_{m_peak2} \\ V_L = V_{DD} \end{cases} \qquad i_{main} = i_{m_peak2} \quad (2\text{-}13)$$

(2-13) indicates that if the same peak current density is desired for both devices, then the size of the auxiliary amplifier should be γ-1 times that of the main amplifier.

2.2.3 Impedance

If the effective load impedances seen by the main and auxiliary amplifiers are defined as $R_{main} = V_{main}/i_{main}$ and $R_{aux} = V_L/i_{aux}$, then they can be derived based on known voltages and currents. It is worthwhile to point out that the equivalent impedance seen by either the main or the auxiliary amplifier is a combined result of the passive load impedances and the active load-pulling effect by the other transistor in the Doherty amplifier.

$$R_{main} = \frac{Z_C^{\,2}}{R_L} = \gamma^2 R_L \qquad i_{main} \le i_{m_peak1} \quad (2\text{-}14)$$

Since I_{aux} is zero when $i_{main} \le i_{m_peak1}$, R_{aux} is infinity.

$$\left.\begin{aligned} R_{main} &= \frac{V_{DD}}{i_{main}} = \frac{\gamma^2 R_L i_{m_peak1}}{i_{main}} \\ R_{aux} &= \frac{V_L}{i_{aux}} = \frac{R_o i_{main}}{\gamma(i_{main} - i_{m_peak1})} \end{aligned}\right\} \qquad i_{main} > i_{m_peak1} \quad (2\text{-}15)$$

Notable impedances at the point of i_{m_peak2} are:

$$\left.\begin{aligned} R_{main} &= \gamma R_L \\ R_{aux} &= \frac{\gamma}{\gamma - 1} R_L \end{aligned}\right\} \qquad i_{main}=i_{m_peak2} \qquad (2\text{-}16)$$

With that, we can plot impedances seen by the main and the auxiliary amplifiers in a Doherty amplifier in Fig. 2.4.

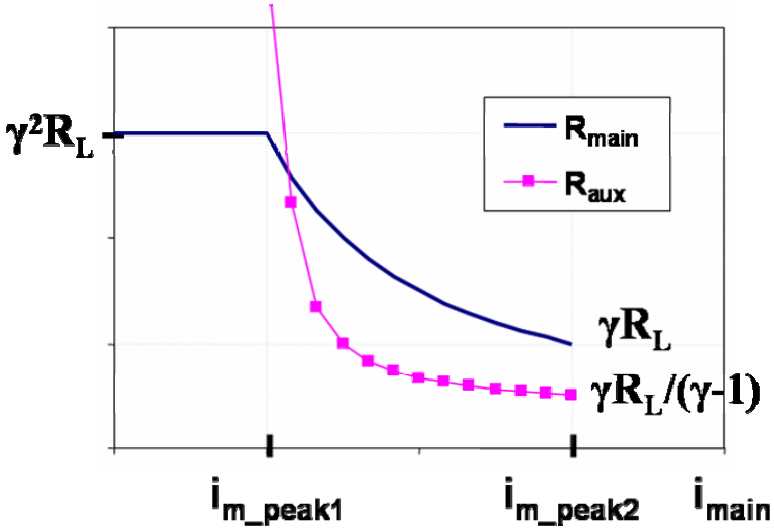


Figure 2.4: Equivalent load impedances in Doherty as a function of i_{main}

2.2.4 Output Power and Efficiency

For the idealized analyses here, it is assumed that the main amplifier is biased in Class B. In real circuits, it can often be biased in Class AB. It is worthwhile to note that the voltages and currents used in the analyses represent values at the fundamental frequency. Consequently, DC current, power consumption and RF output power can be derived accordingly.

In general:

$$\begin{cases} P_{DC} = \frac{2}{\pi}(|i_{main}| + |i_{aux}|)V_{DD} \\ P_{RF} = P_{RF_m} + P_{RF_aux} = \left|\frac{V_{main} i_{main}}{2}\right| + \left|\frac{V_L i_{aux}}{2}\right| \\ \eta = \frac{P_{RF}}{P_{DC}} \end{cases} \quad (2\text{-}17)$$

For input levels before the main amplifier goes into saturation:

$$\begin{cases} P_{DC} = \frac{2}{\pi}(V_{DD} i_{main}) \\ P_{RF} = \frac{V_{main} i_{main}}{2} = \frac{Z_C^{\,2}}{2R_L} i_{main}^{\,2} = \frac{\gamma^2 R_L i_{main}^{\,2}}{2} \\ \eta = \frac{\pi \gamma^2 R_L i_{main}^{\,2}}{4 V_{DD} i_{main}} = \frac{\pi}{4}\frac{i_{main}}{i_{m_peak1}} \end{cases} \quad i_{main} < i_{m_peak1} \quad (2\text{-}18)$$

For input level after main amplifier goes into saturation:

$$\begin{cases} P_{DC} = \frac{2}{\pi}(i_{main} + \gamma(i_{main} - i_{m_peak1}))V_{DD} \\ P_{RF} = \frac{V_{DD} i_{main}}{2} + \frac{i_{main} Z_C \gamma (i_{main} - i_{m_peak1})}{2} = \frac{\gamma^2 R_L i_{main}^{\,2}}{2} \\ \eta = \frac{\pi}{4}\frac{\gamma^2 R_L i_{main}^{\,2}}{(i_{main} + \gamma(i_{main} - i_{m_peak1}))V_{DD}} \end{cases} \quad i_{main} > i_{m_peak} \quad (2\text{-}19)$$

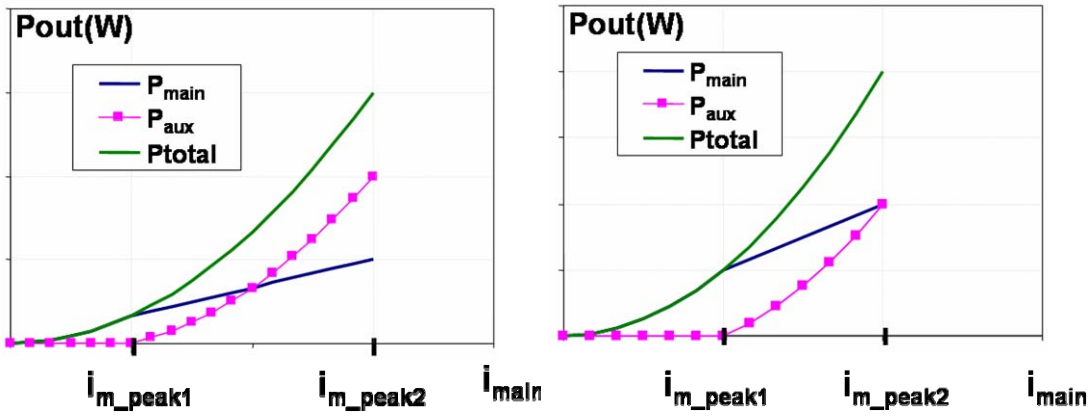
Notable relations at the point $i_{main} = i_{m_peak1}$ are:

$$\begin{cases} P_{RF_m} = \frac{V_{main} i_{main}}{2} = \frac{\gamma^2 R_L i_{m_peak1}^{\,2}}{2} \\ P_{RF_aux} = 0 \\ \eta = \frac{\pi}{4}\frac{i_{m_peak1}}{i_{m_peak1}} = \frac{\pi}{4} \end{cases} \quad i_{main} = i_{m_peak1} \quad (2\text{-}20)$$

Notable relations at the point of $i_{main} = i_{m_peak2}$ are:

$$\begin{cases} P_{RF_m} = \dfrac{V_{DD} i_{m_peak2}}{2} = \dfrac{V_{DD}\gamma i_{m_peak1}}{2} \\ P_{RF_aux} = \dfrac{V_{DD} i_{aux_peak2}}{2} = \dfrac{V_{DD}\gamma(\gamma-1) i_{m_peak1}}{2} \\ \eta = \dfrac{\pi}{4} \dfrac{\gamma^2 R_L (\gamma i_{m_peak1})^2}{(\gamma i_{m_peak1} + \gamma(\gamma i_{m_peak1} - i_{m_peak1}))V_{DD}} = \dfrac{\pi}{4} \end{cases} \qquad i_{main}=i_{m_peak2} \quad (2\text{-}21)$$

With (2-17) to (2-21), the RF output power of the main, the auxiliary and the overall Doherty amplifier (which is the sum of the aforementioned two) can be plotted, as shown in Fig. 2.5. Fig. 2.5(a) is for an extended Doherty case with $\gamma>2$, while Fig. 2.5(b) is the $\gamma=2$ classic Doherty case for comparison purpose. One notable difference between the two cases is that P_{aux} exceeds P_{main} at the maximum input level in the extended Doherty case.



(a) Extended Doherty ($\gamma>2$) **(b) Classic Doherty ($\gamma=2$)**

Figure 2.5: RF output power in the Doherty amplifier

Based on analyses here, the efficiency of the Doherty amplifier can be plotted in Fig. 2.6. The Doherty amplifier has two efficiency peaks at input levels of i_{m_peak1}

and i_{m_peak2}. Both of the peak efficiencies are 78.5%, which is the theoretical maximum efficiency a Class B biased amplifier can reach. Since $i_{m_peak2} = \gamma\, i_{m_peak1}$, the two efficiency peaks are separate in input power by 20log γ (dB). When γ=2, the separation is 6 dB. When γ=3 or 4, the separation is 9 or 12 dB, respectively.

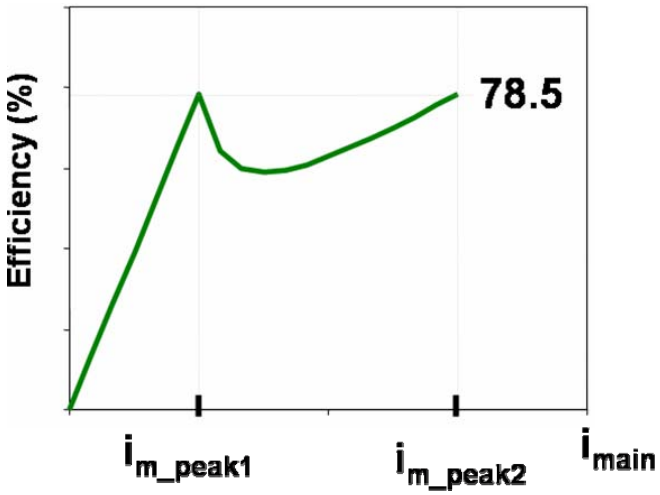


Figure 2.6: Efficiency of the Doherty amplifier

2.2.5 Current Sources with Finite Output Impedance

A more complete model with finite output impedances added to the current source based transistor model can be used to analyze the Doherty amplifier. Detailed analysis can be found in [2]. A conclusion can be drawn from this analysis that even with this relatively simple model, performance of a Doherty amplifier in terms of linearity of output voltage, maximum output power and in most cares efficiency can be degraded by the infinite output impedance associated with the real transistors.

2.3 Practical Design Issues of Doherty Amplifier Circuits

In section 2.2, the operational theory of a Doherty amplifier is presented. However, the theory is only developed for ideal conditions with transistors modeled as ideal current sources. To design a high efficiency Doherty amplifier that is suitable for CDMA handset applications, many practical issues must be understood. The completed design of a Doherty amplifier should exhibit significant efficiency improvement over a traditional Class AB biased amplifier at 6dB, 9dB and 12dB backed-off power levels when tested with CW signals and also show extended high PAE performance with CDMA signals applied at the input. In this chapter, our priority is to achieve high efficiency in a Doherty circuit design; design for linearity performance will be discussed in chapter 3 and chapter 4.

The practical design issues covered in this chapter are: design of ***load impedances*** for the main amplifier; choice of ***device sizes*** for the auxiliary amplifier; the need for ***uneven power split*** at the inputs; ***bias voltage optimization*** for the auxiliary amplifier; and implementation of ***harmonic terminations***. With understanding of these issues, a Doherty amplifier based on GaAs MESFETs is designed in simulation and also fabricated on a PCB board. Simulation results are discussed in this chapter. Following that, measurement results of PAE, gain, phase and linearity of the fabricated Doherty amplifier are also discussed. A lumped element based Doherty amplifier design is also shown to demonstrate that the entire Doherty amplifier can be potentially integrated on chip.

2.3.1 Design of Impedance Levels

The load impedances seen at the output of the main are among the very basic design parameters in a Doherty amplifier design. As can be seen in Fig. 2.4 of section 2.2.3, the impedance seen by the main amplifier is $R_{main}= \gamma^2 * R_L$ when i_{main} is low. With increase of i_{main}, R_{main} needs to decrease gradually to γR_L at the peak input level. This is guaranteed by using $Z_C= \gamma R_L$ for the quarter-wave transmission line.

In a single-ended amplifier design, with supply voltage usually fixed by device technology, load impedance R_L is the main design parameter for the amplifier to meet output power requirement. For example, output I-V curve can be used to estimate the output power as mentioned in chapter 1: $P_{max}= I_{max}(2V_{DD}-V_{knee})/8$, where I_{max} is the maximum current allowed in a transistor, V_{DD} is DC supply voltage and V_{knee} is the knee voltage of the transistor. It can be easily found that:

$$I_{max}=8\ P_{max}\ /(2V_{DD}-V_{knee})$$

$$R_L=(2V_{DD}-V_{knee})/\ I_{max} = (2V_{DD}-V_{knee})^2/(8\ P_{max}) \qquad (2\text{-}22)$$

(2-22) should apply to a Doherty amplifier since it can be viewed as a single PA with R_L as its load impedance, for this purpose. I_{max} also sets the requirement for transistor sizes. For the Doherty amplifier, according to its operational theory discussed in section 2.2, $I_{max} = i_{m_peak2}+i_{aux_peak2}$, and $i_{m_peak2} = I_{max} / \gamma$, $i_{aux_peak2} = (\gamma - 1)I_{max} / \gamma$.

With R_L determined, Z_C of the quarter-wave line can be calculated as $Z_C= \gamma R_L= \gamma (2V_{DD}-V_{knee})/ I_{max}$. With R_L, Z_C fixed, all the major relations in a Doherty

amplifier can be determined quantitatively. For example, the main amplifier reaches saturation and the Doherty amplifier reaches its first efficiency peak at Pout= P_{max}/γ^2. When the Doherty amplifier reaches its second efficiency peak at Pout= P_{max}, the main amplifier contributes $P_{main}= P_{max}/\gamma$ to the output, while the auxiliary amplifier contributes the rest, which is $P_{aux}= (\gamma -1) P_{max}/\gamma$. As pointed out in section 2.2, γ decides the width of the high efficiency range of the Doherty amplifier. However, in practice, $\gamma >4$ is not a good choice due to the low efficiency between the two peaks and other potential performance discontinuities.

2.3.2 Transistor Sizes

Transistor size for a power amplifier is usually determined by its current density limit J_{c_max}. J_{c_max} is often set to be the value where ft (unit current gain frequency) of the transistor reaches its peak in a ft vs. Jc plot. Reliability considerations and thermal issues may also determine the choice of J_{c_max}. J_{c_max} typically ranges from 0.1 to 1mA/um^2, depending on the device technology. When the power and hence maximum current delivery requirement on the main and the auxiliary amplifier in a Doherty amplifier is determined following section 2.3.1, transistor sizes for the main and the auxiliary amplifier can be subsequently determined. According to Fig. 2.3(b), since current ratio between the two amplifier at i_{m_peak2} is 1:(γ-1), their transistor size ratio should also be 1:(γ-1). For the γ=2 case, the size ratio is 1:1. But for the γ=3, the size ratio is 1:2.

For a Class C and a Class B biased amplifier to deliver a current with the same component at the fundamental frequency, the Class C amplifier needs a higher peak current due to its smaller conduction angle. So, it is plausible that the auxiliary PA potentially needs a higher I_{max} and thus a larger device size than the main PA even for a classic Doherty amplifier with γ=2. However, in reality, with increase of the input power level, the bias level in the Class C amplifier increases by a self-bias effect resulting from the nonlinearity of the amplifier and its bias circuit. Conduction angle of the initially Class C biased amplifier can increase from below to over 180º with a large input power, and into Class AB operation. As a result, the potential need of a larger device size for Class C biased auxiliary amplifier is not necessary. In the case of γ=2, the same device sizes can be used for both the main and the auxiliary amplifier. With the result, the auxiliary amplifier is pushed slightly harder than the main amplifier at peak power in terms of current density. In general, the ratio between transistor sizes of the main and the auxiliary amplifier is still 1: (γ -1), even the two are initially biased differently.

2.3.3 Uneven Input Splitting

For the discussion in section 2.3.2, it was decided that a 1: (γ -1) size ratio between the main and the auxiliary amplifier is enough for the auxiliary amplifier even it is initially biased in Class C. However, can the auxiliary amplifier generate the desired current $i_{aux_peak2}=\gamma i_{m_peak2}$ (or power) at the maximum input level? Looking back to i_{aux} in (2-8) for an ideal case, $i_{aux} = \gamma(i_{main}-i_{m_peak1})$ was designed. The slope of

i_{aux} is γ with i_{main} the independent variable. Can this i_{aux} actually be realized by the auxiliary amplifier? If i_{aux} has a slope lower than γ, the ideal performance of a Doherty amplifier shown in Fig. 2.3 will be affected. Such a case is shown Fig. 2.7. With a lower slope of i_{aux} after i_{main} increases to a value higher than i_{m_peak1}, the load-pulling effect from the auxiliary amplifier on the main amplifier is less strong. As a result, V_{main} keeps increasing in the ideal model, although at a slower pace. In reality, V_{main} can not be higher than V_{DD} and will be clipped. Consequently, output power of the Doherty amplifier will drop. More over, linearity and efficiency performance for the Doherty amplifier can be significantly degraded.

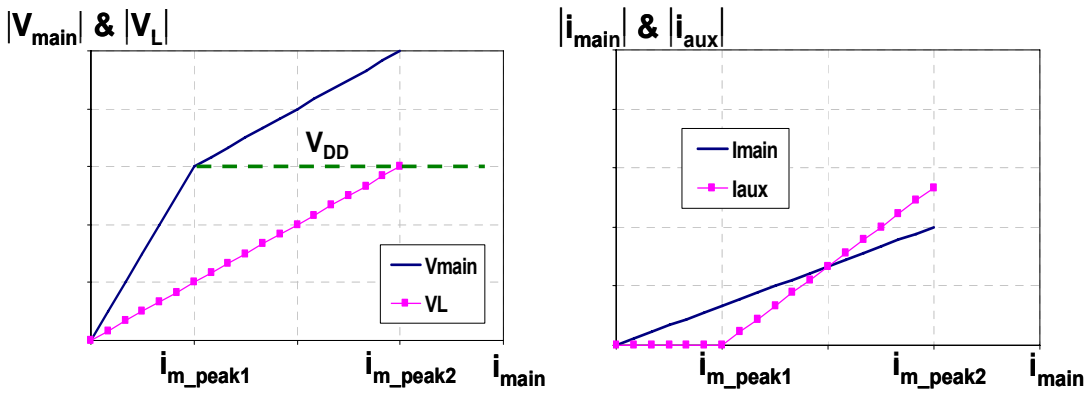


Figure 2.7: Voltage and current characteristics in a Doherty with lower slope of current i_{aux}

Based on idealized conduction angle θ of an amplifier in different bias conditions, its fundamental component of current can be calculated using a Fourier Transform of the output current waveform. The result is shown in equation (2-23), in which I_{max} is the peak value of the current excursion. Assuming I_{max} increases linearly with input current, then conduction angle of a Class C biased amplifier increases with input level, and so does the I_{fund}. I_{fund} vs. I_{input} can be calculated, and is plotted in Fig.

2.8. Also shown is the fundamental component of current for a Class B biased amplifier calculated based on (2-23). This result shows that the current slope for a Class C amplifier is not higher than that for a Class B amplifier.

$$I_{fund} = \frac{I_{max}(\theta - \sin\theta)}{2\pi(1 - \cos(\theta/2))} \tag{2-23}$$

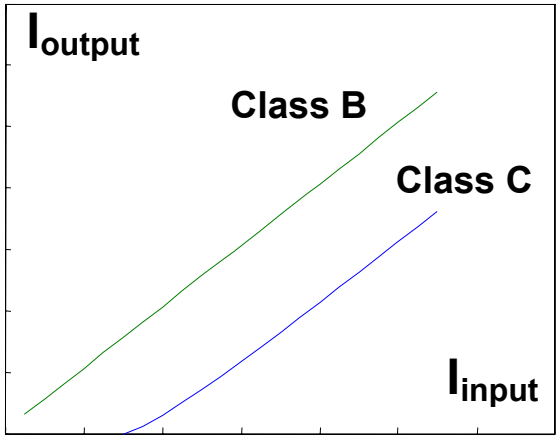


Figure 2.8: Slope of current in Class C and Class B biased amplifier based on conduction angle change

However, in real device simulation results shown in Fig. 2.10 (a), it is found that the current slope of a Class C biased auxiliary amplifier in a Doherty circuit can be approximately twice that of a Class B bias main amplifier. Self bias effect and other nonlinear effects in the Class C biased auxiliary amplifier probably play an important role in this. With increase of the input power level, bias current of the amplifier can be increased and the trans-conductance g_m of the Class C amplifier can also increase. This could have helped to increase the slope of its current. Another important factor is the effect of load impedance changes. From the ideal Doherty analysis, the load impedance the auxiliary sees in a Doherty change dramatically,

which can affect its output current. Fig. 2.9 shows a simple transistor model with a finite output impedance Zout. Zout will by pass output current from the transistor to the load R_L. When the RL value decreases, the bypass effect becomes smaller and hence I_2 increases. Simulation can be done using a stand-alone Class C amplifier with the same configurations as the auxiliary amplifier in the Doherty. This is shown in Fig. 2.10 (b), where the current slope of the stand-alone Class C amplifier gain increases with its load impedance statically tuned to lower values (green curves). For the auxiliary amplifier in a Doherty, its impedance drops gradually with increase of input power. At a designated input level, if the auxiliary amplifier sees R_L at its load, a point can be found in one of these green curves corresponding to the same R_L. Thus the current of this point should also be the current that of auxiliary amplifier in a Doherty operation. When such points are connected for the entire range of power levels, the current of auxiliary PA in Doherty operation can be drawn as shown in Fig. 2.10(b). This explains why impedance change in a Doherty amplifier can change the slope of i_{aux} higher than that of i_{main}.

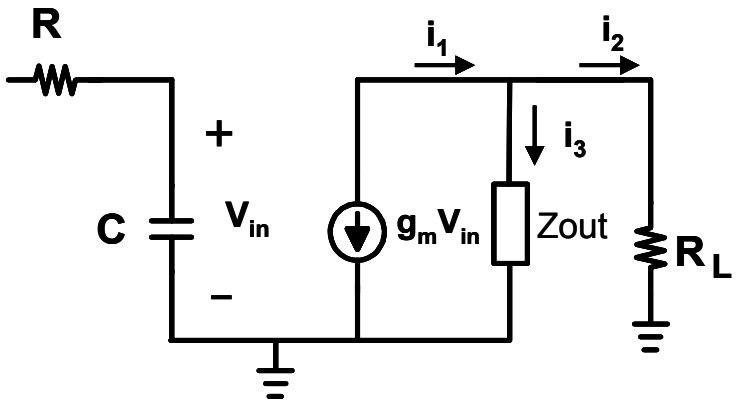


Figure 2.9: Effect of impedance change on current slope in Doherty PA

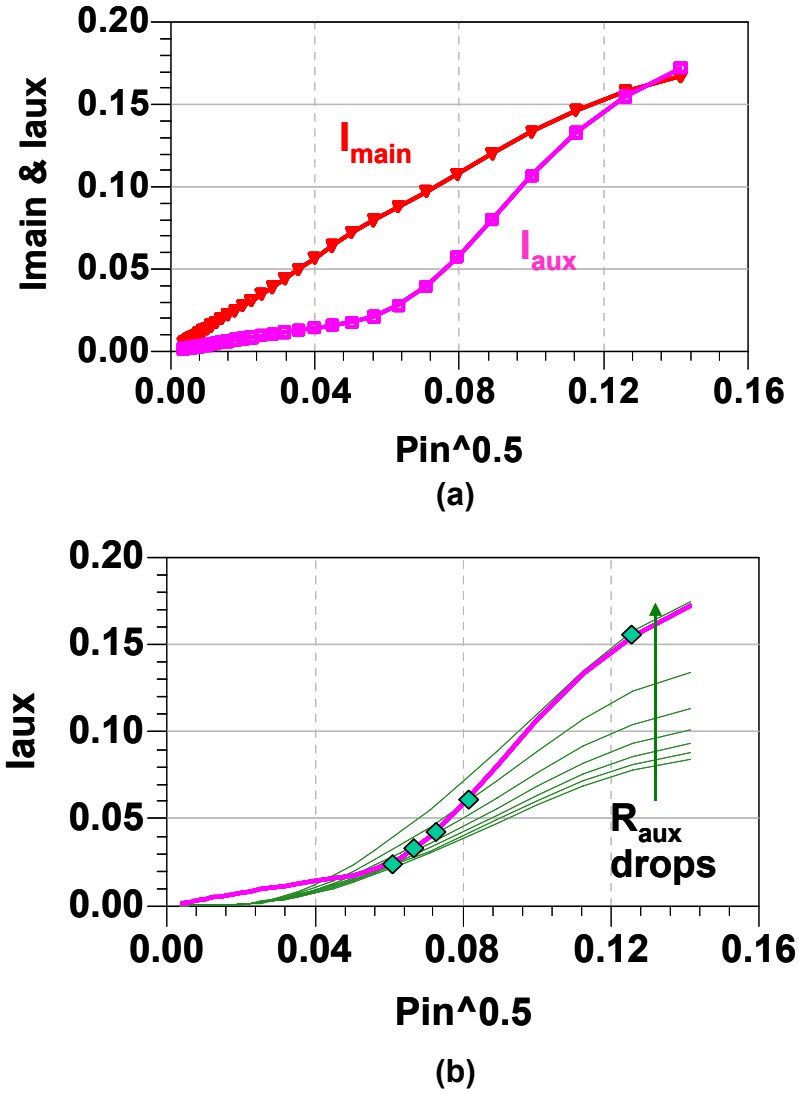


Figure 2.10: Effect of load impedance change on current slope of the auxiliary amplifier in a Doherty amplifier

The current slope gain of i_{aux} described above can be twice the slope of i_{main} , which is enough for a Classic Doherty operation. However, for an extended Doherty with $\gamma>2$, a slope (γ -1) is needed for i_{aux}. The Doherty circuit itself may not be able to provide that. Additional help can be found by using an uneven power split at the input of the Doherty amplifier. It increases the relative gain of the auxiliary amplifier to the

main amplifier and also increases the slope of i_{aux} [3]. An empirical value for the uneven split ratio between the main and the auxiliary amplifier is 1: (γ -1). The traditional Wilkinson divider can be modified to be an uneven splitter with changes made to the characteristic impedances. The method to calculate these impedances is given in reference [4].

It is worthwhile to point out that change of quiescent bias does not change the slope of current. It only results in change of turn on point and thus changes the efficiency of the Doherty amplifier.

2.3.4 Optimum Bias Condition for the Auxiliary Amplifier

The bias voltage (gate or base) of an amplifier is often a place where tradeoff can be made between efficiency and linearity. Lower bias can lead to lower quiescent current and higher efficiency but usually worse linearity. The main amplifier in a Doherty amplifier is biased in a proper level to make the main amplifier achieve adequate linearity while getting as high as possible efficiency when the auxiliary amplifier is off. Of more importance in a Doherty structure is the bias of the auxiliary amplifier. The Class C biased auxiliary amplifier is a key design feature for the Doherty amplifier.

Careful tuning on the bias of the auxiliary amplifier is necessary to ensure that the auxiliary amplifier turns on right at the point where main amplifier goes into saturation. This determines whether a continuous performance with constant gain vs.

power can be achieved for the overall Doherty amplifier. Higher bias on the auxiliary amplifier will turn it on early and can cause gain expansion. On the other hand, low bias can introduce gain compression for the Doherty amplifier. These are illustrated in Fig. 2.11, which contains representative measured gain data of a Doherty amplifier (whose detailed configuration is described in section 2.4) when the bias voltage on the gate of its auxiliary amplifier is varied. It is noticeable that gain of the Doherty amplifier remains relatively invariant to bias voltage change in low power. However, gain increase significantly with bias in high power where the auxiliary amplifier plays an important role.

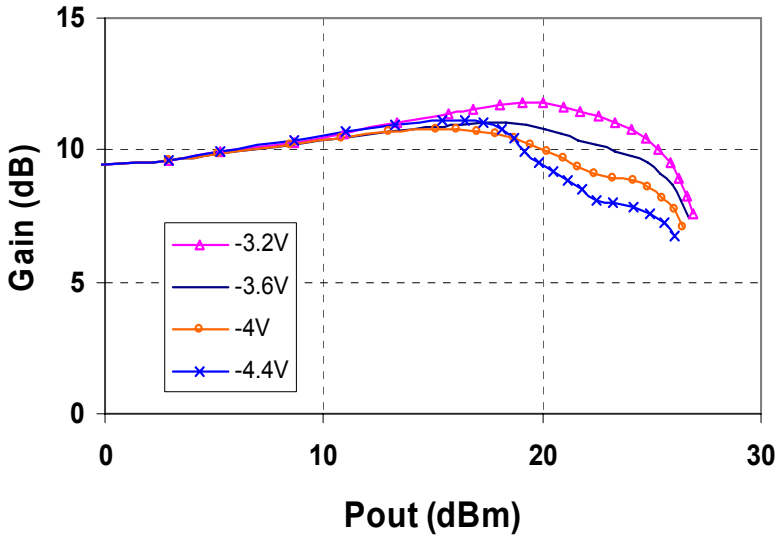
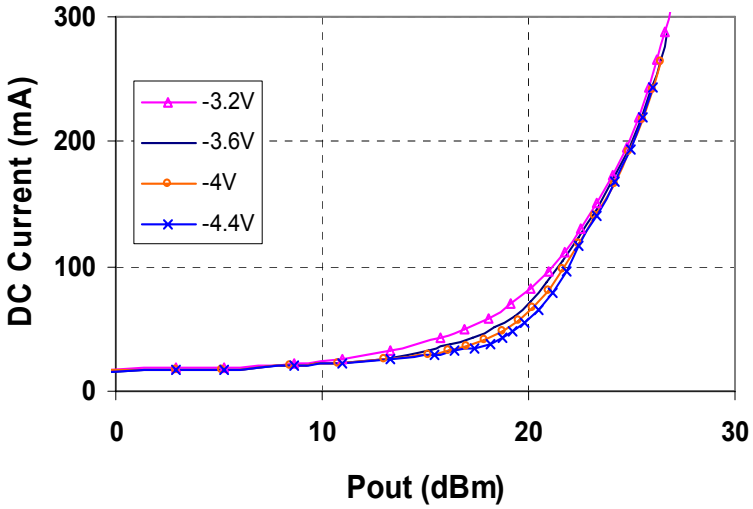


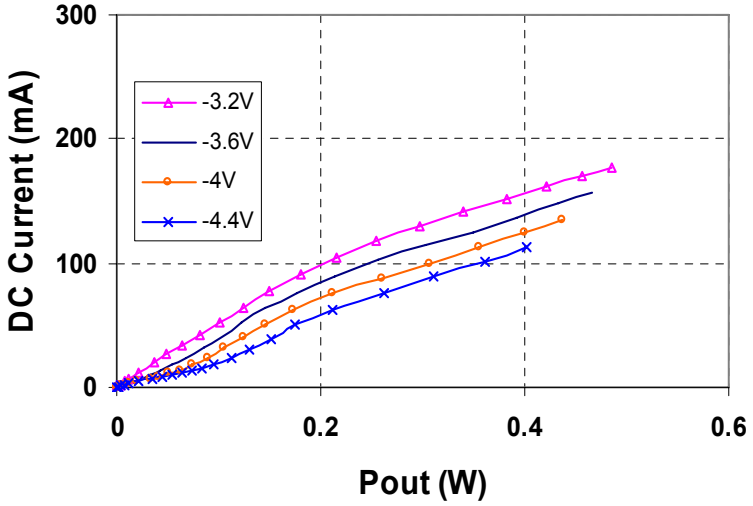
Figure 2.11: Change of gain in Doherty when gate bias voltage of the auxiliary amplifier changes

The bias point of the auxiliary amplifier is also critical to the overall current consumption and the efficiency performance in the Doherty. Changes of the bias of the auxiliary amplifier can lead to changes in DC current levels. Fig. 2.12(a) shows

how the total DC current of the same Doherty amplifier (as in Fig. 2.11) increases with the increase of the gate bias voltage of the auxiliary amplifier. This is especially evident when the current of the auxiliary amplifier is plotted versus power on a linear scale in Fig. 2.12(b). With higher bias, the turn on point of the auxiliary amplifier is shifted to lower input power, its DC current is shifted up and so is the DC current of the Doherty amplifier. As a result of these considerations, the efficiency of the Doherty (shown in Fig. 2.13) around the first efficiency peak of Doherty will drop and the first efficiency peak can disappear entirely with the auxiliary amplifier biased too high. It is beneficial for efficiency to bias the auxiliary amplifier as low as possible. However, if the bias of auxiliary amplifier is too low, current contribution from the auxiliary amplifier will not be enough to keep the main PA out of saturation when input power is high and linearity would suffer. More about the tradeoff involved in the gate bias voltage of the auxiliary amplifier will be discussed in Chapter 3. It will be shown that there is no single optimum bias point for both efficiency and linearity over the entire power range. Dynamic bias control is needed to achieve the best tradeoff when input signal has a non-constant envelope.



(a)



(b)

Figure 2.12: (a) Change of total DC current in Doherty and (b) change of DC current in the auxiliary amplifier when bias of the auxiliary PA changes

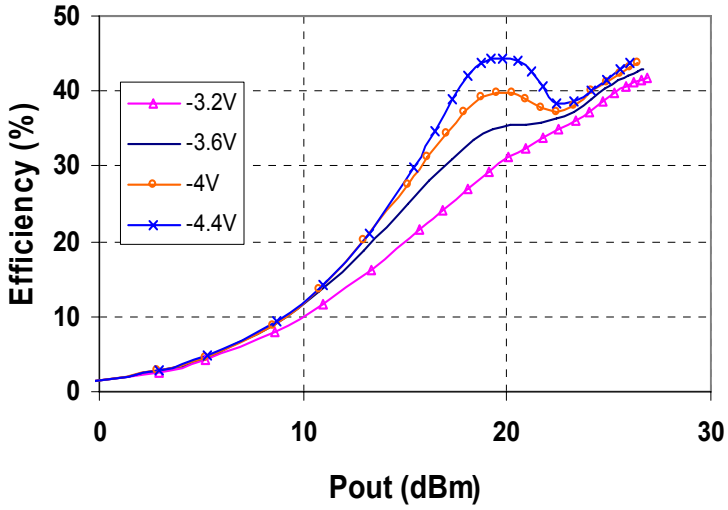


Figure 2.13: Change of efficiency in Doherty amplifier when bias of the auxiliary amplifier changes

2.3.5 Harmonic Terminations

To design an amplifier to meet practical performance requirements, it is always important to provide proper harmonic terminations, since these can help optimize both linearity and efficiency performance. For linearity concerns, a short load at the 2nd harmonic frequency is usually desired. This approach can increase IIP2 significantly [5]. For efficiency concerns, it is often desirable to have an open load at the 3rd harmonic frequency. This provides opportunity for voltage waveform shaping on the output node, which helps to reduce DC power dissipated inside the amplifier. Unfortunately, in a Doherty PA, since it is necessary to have the quarter-wave transmission line as impedance inverter, to have short load for 2nd harmonic and open for 3rd harmonic at the output of both the main and the auxiliary amplifier is not possible. A short for 2nd harmonic still looks like a short from the other end of the λ/4

line, but an open for 3rd harmonic looks like a short from the other end of the λ/4 line. Choice was made to have short for 2nd harmonic and open for 3rd harmonic at the output of the main amplifier (see Fig. 2.14). At the same time, the auxiliary amplifier sees a short for 2nd harmonic and a short for 3rd harmonic as well. As a result, the main amplifier, which is configured analogous to a Class F amplifier, can achieve higher efficiency and thus make the first peak of efficiency in the Doherty more pronounced. This is especially important because in many previous publications on Doherty amplifiers, the first efficiency peak was often not evident. In general, proper harmonic terminations at the 2nd and 3rd harmonic frequencies have the effect of improving efficiency by a few percent without significant changes to the fundamental output power.

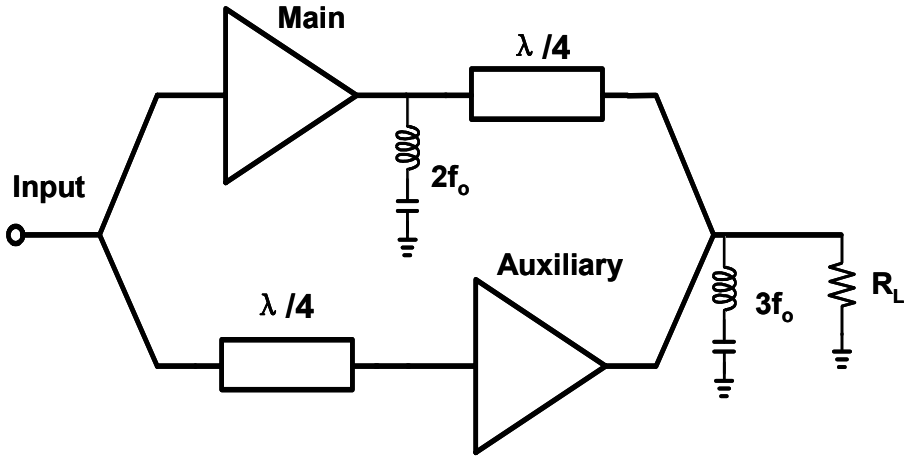


Figure 2.14: Harmonic terminations in a Doherty amplifier circuit

2.4 Simulation Results of a Doherty Amplifier

In this section, a GaAs MESFET based Doherty amplifier will be designed and simulation results will be discussed. In Fig. 2.15, the schematic of this Doherty amplifier is shown. The device model used in the simulation is a packaged model for MWT 871, which is a commercial available GaAs MESFET device. It has a 0.3um gate length and 1200um gate width. Its typical saturated drain current I_{DSS} is 400mA, gate-to-drain breakdown voltage BV_{GDO} is -12V. In the circuit design, quarter-wave impedance inverter and the quarter-wave delay line are implemented as microstrip lines. Other matching circuits are also implemented as microstrip lines. The circuit is designed to work at a center frequency of 840MHz.

Design of the circuit is based on the practical design issues discussed in section 2.3:

- $\gamma = 3$ is chosen.
- Impedances: $R_L=(2V_{DD}-V_{knee})^2/(8\,P_{max}) = 5\ \Omega$ (V_{DD} set to 3.4V, and knee voltage of the device is estimated to be 0.5V. The output power requirement P_{max} is 1Watt); $Z_C=15\ \Omega$, $R_{main}=45\ \Omega$.
- Transistor size ratio: $1:(\gamma -1) = 1:2$ (main to auxiliary). In simulation, two parallel MWT871 devices are used for the auxiliary amplifier.
- Uneven input power splitter ratio: $1:(\gamma -1) = 1:2$ (main to auxiliary).
- Gate bias voltage of the auxiliary amplifier: *-4.8V* (selected for high efficiency performance).
- Harmonic terminations are configured as mentioned in section 2.3.5.

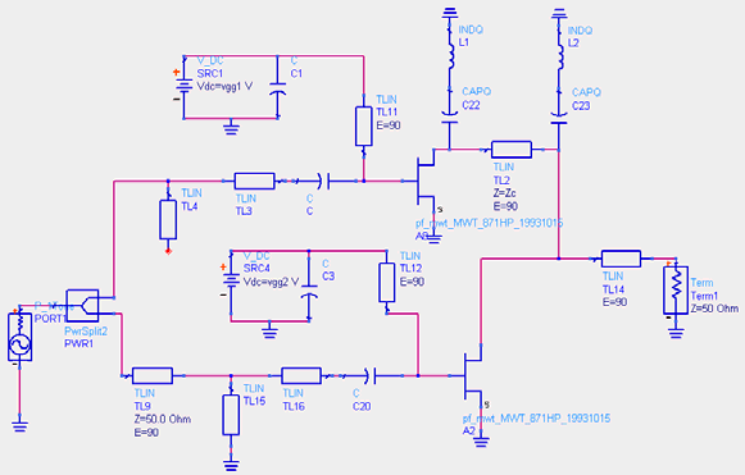


Figure 2.15: Schematic of the Doherty amplifier used in simulation

2.4.1 Voltages and Currents

Plotted in Fig. 2.16(a), (b) are simulated results of output voltages and currents of the main and the auxiliary amplifier at fundamental frequency. Compared to an ideal case as in Fig. 2.3, this simulated Doherty amplifier behaves well, although there is an undesired small leakage current I_{aux} in low power region where the auxiliary amplifier should be off. The reason is believed to be the current incurred on the finite output impedance of the auxiliary amplifier by voltage on the output node.

Compared with Fig. 2.3, I_{m_peak1} is estimated to be 75mA with I_{m_peak2}=220mA ~ γ I_{m_peak1} (γ=3). Also I_{aux_peak2}=440mA ~ (γ-1) I_{m_peak2}. V_{main} reaches 3.1V and saturates at I_{main}= I_{m_peak1}, although increases slightly to 3.5 after that. V_L increases almost linearly with I_{main}, but only reaches 3.2V, a little lower than the supply voltage V_{DD} of 3.4V.

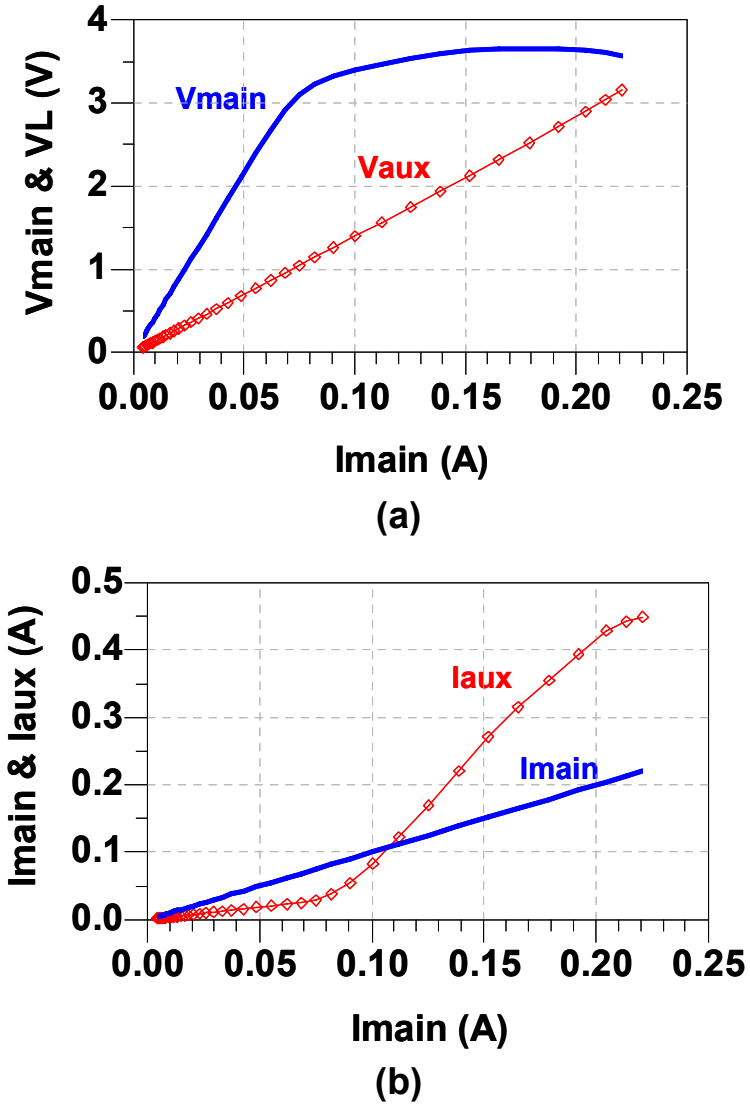


Figure 2.16: Voltages and currents in the simulated Doherty amplifier

2.4.2 Gain, Phase and PAE

Shown in Fig. 2.17 are simulated gain and phase of the Doherty amplifier vs. output power. Gain rolls off slightly in high power, a common problem in Doherty PA even with an uneven power splitter at input. Due to combined effect of nonlinear voltage output and parasitic complex output impedances (usually capacitive) of the

transistors, phase variation is as large as 30º here. Both gain and phase variation in high power region will cause linearity issues in Doherty.

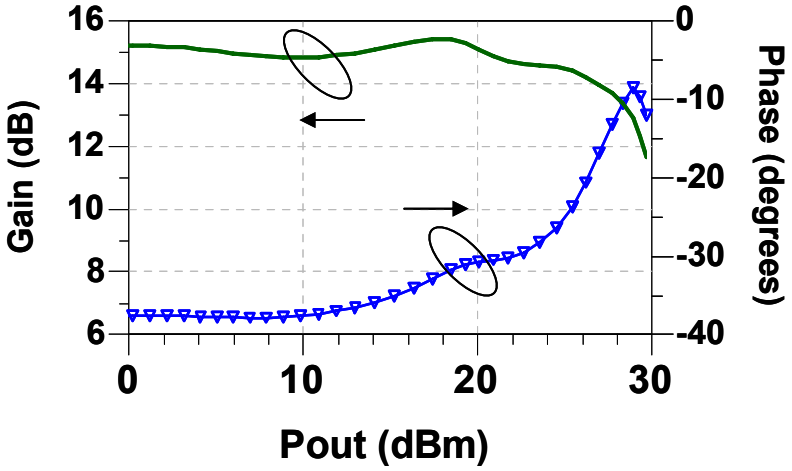


Figure 2.17: Gain and phase in the simulated Doherty amplifier

In Fig. 2.18, the efficiency of the simulated Doherty is shown. It has two visible efficiency peaks at Pout of 20 and 29dBm, in between, an extended range where efficiency higher than 40% is achieved. This is consistent with the 9dB range predicted by the ideal Doherty model for γ=3. The PAE is lower than in the ideal case due to parasitic loss that exists in circuit components and the device model used in simulation.

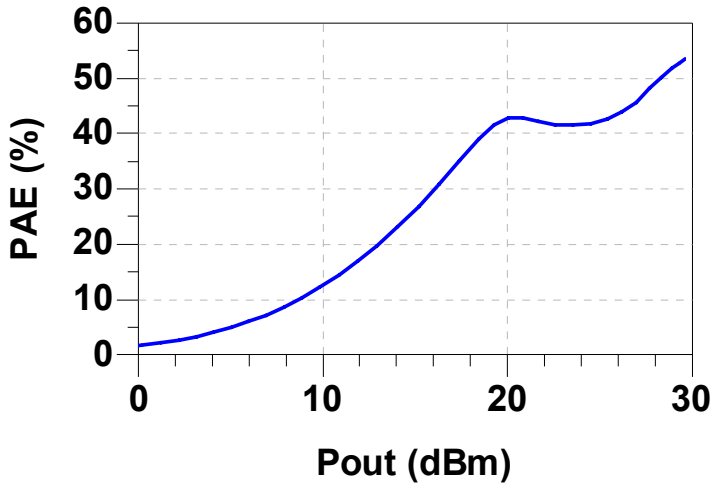


Figure 2.18: PAE in the simulated Doherty amplifier

2.4.3 Gain and Load Impedance of the Main and the Auxiliary Amplifier

The gain that the main and auxiliary amplifier experienced respectively within a Doherty amplifier operation can be easily measured in simulation, although it is difficult to measure in an experiment [6]. It is plotted in Fig. 2.19. It helps to show the behavior of each individual amplifier and their contributions to the overall Doherty amplifier. It can be seen in Fig. 2.19 that after main amplifier reaches saturation at around 20dBm Pout, its gain drops gradually instead of sharply as the case of a stand-alone amplifier with fixed load impedance (as indicated by dotted line in Fig. 2.19). Meanwhile, gain of the Class C biased auxiliary amplifier peaks up and compensates the gain drop of the main amplifier.

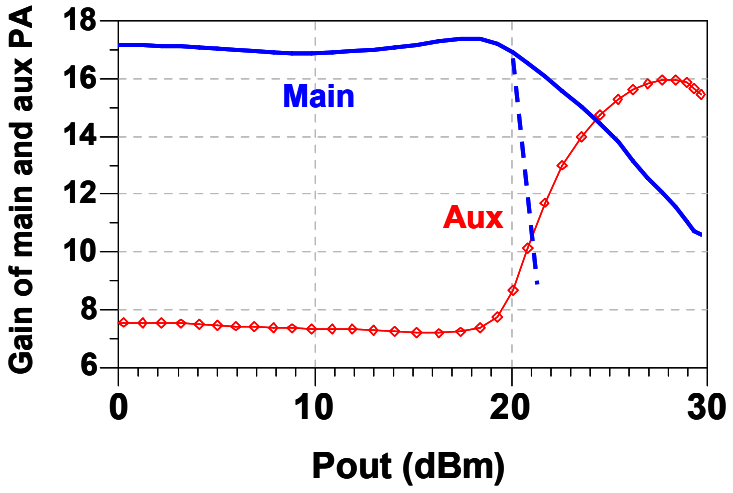


Figure 2.19: Gain of the main and the auxiliary amplifier individually within the simulated Doherty

The load impedances seen at the output of main and auxiliary amplifier are plotted in Fig. 2.20. In Fig. 2.20, the magnitude of Z_{main} starts with a value of 43Ω at low input level which is close to $\gamma^2 R_L$= 45Ω. It drops gradually to around γR_L= 15 Ω at maximum Pout. Z_{aux} is predicted to be infinity in low power in an ideal Doherty case (Fig. 2.4), but with the existence of leakage current I_{aux} in low power and the effect from the parasitic output impedance of the main amplifier transistor, Z_{aux} becomes smaller than Z_{main}. With I_{main} increases, the magnitude of Z_{aux} eventually drops to around to $\gamma R_L /(\gamma-1)$ = 7.5 Ω, matching accurately with predictions by an ideal case. However, in simulation, real device model was used instead of ideal current sources. As a result of that, Z_{main} and Z_{aux} are complex impedances. Fig. 2.21 shows the complex impedances in a smith chart.

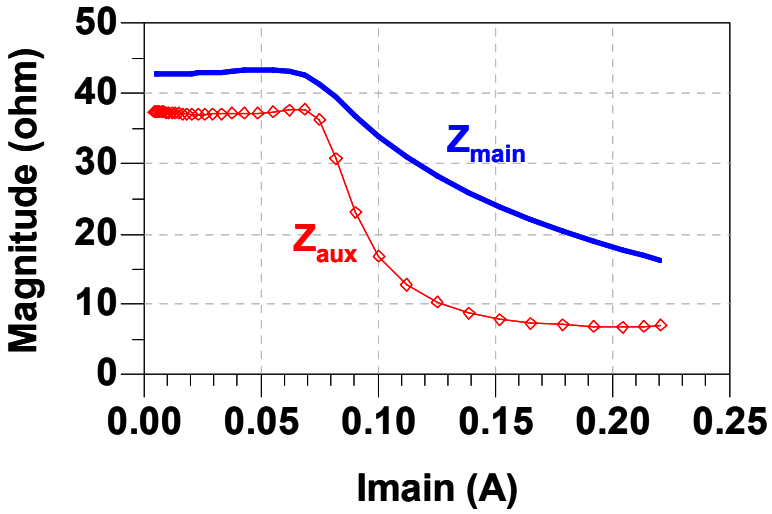


Figure 2.20: Load impedances for the main and the auxiliary amplifier

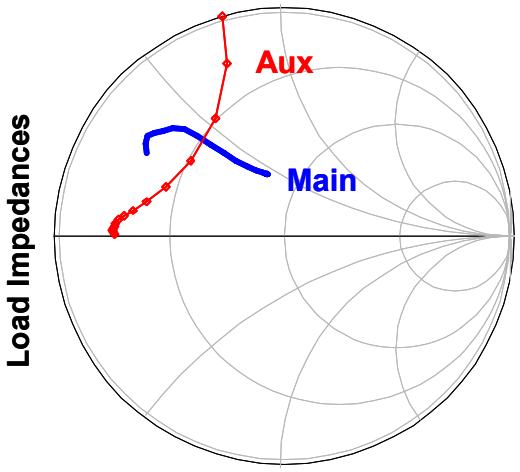


Figure 2.21: Load impedances for the main and the auxiliary amplifier

2.5 Measurement Results of a GaAs FET Based Doherty Amplifier

Following the design of the Doherty amplifier based on GaAs MESFETs in simulation in section 2.4, a Doherty amplifier was fabricated and tested. The circuit was designed to operate at a center frequency of 840MHZ. The test circuit was

constructed on a Roger4350 printed circuit board with thickness of 30 mils and dielectric constant $\varepsilon_\gamma = 3.48$. The quarter-wave impedance inverter and the quarter-wave delay line were implemented as microstrip transmission lines. Other matching circuits were designed with surface mount components and microstrip transmission lines. The experimental data of this Doherty amplifier will be discussed in this section.

Compared with the simulation design, major design parameters of this experimental Doherty amplifier are the same except that a CLY5 GaAs FET is used for the auxiliary amplifier. Also gate bias voltage of the auxiliary amplifier is changed slightly.

- $\gamma = 3$ is chosen.
- Impedances: $R_L = 5\ \Omega$ (V_{DD} = 3.4V, output power target is 1W); $Z_C = 15\ \Omega$.
- A CLY5 GaAs FET is used for the auxiliary amplifier (parallel two packaged MWT871 is not feasible in experiment). It has a typical 800mA I_{DSS}, twice that of MWT871. And transistor size ratio: $1:(\gamma - 1) = 1:2$ (main to auxiliary). BV_{GDO}= -12V, BV_{DSO}=9V. Other parameters are comparable to MWT871.
- Uneven input power splitter ratio: $1: (\gamma - 1) = 1:2$ (main to auxiliary). In experiment, a separate uneven Wilkinson power divider was designed with power split ratio 1 to 2.
- With amplifier characteristics measured, the gate bias voltage of the auxiliary amplifier is set to **-4.5V**, slightly different to -4.8V in simulation.
- Harmonic terminations are configured as mentioned in section 2.3.5.

A photograph of the fabricated Doherty amplifier installed on PCB board can be found in Fig. 2.34 in a later part of this chapter.

2.5.1 Output Power

Measured output power is shown in Fig. 2.22. Output power increases linearly with input power in low power (P_{in}<5 dBm), and experiences a slight gain expansion around P_{in}=10 dBm. In high power (P_{in}>15 dBm), output power begins to compress and reaches saturation at a maximum output power of 28.7 dBm. This maximum Pout is smaller than the designed 30dBm. The reason is believed to be due to impact of the large capacitive output impedances from the GaAs MESFETs devices. Employing larger transistors should help to increase the maximum output power in the Doherty amplifier. However in this work, the devices used were the only available ones.

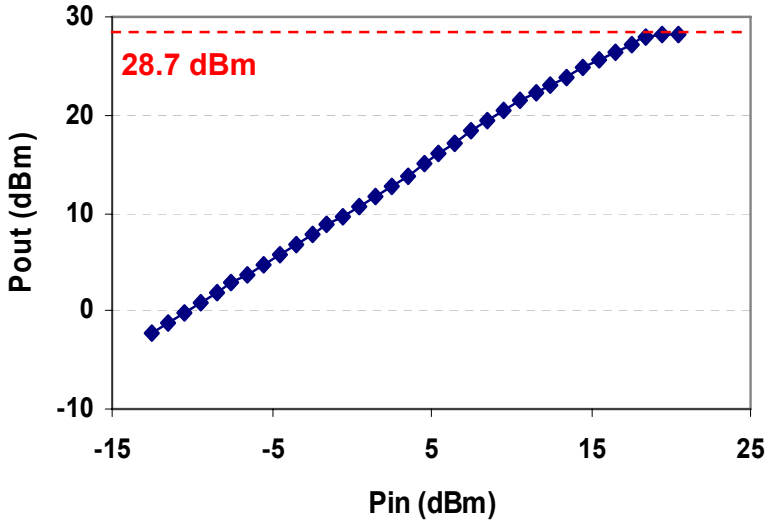


Figure 2.22: Measured output power of the Doherty amplifier with CW signal input

2.5.2 PAE and Average PAE

Fig. 2.23 shows the measured PAE of the Doherty amplifier, obtained with CW tones. The figure also includes, for comparison, the simulated PAE of a class AB amplifier constructed with the MwT-971 FET (and having similar output power and quiescent bias). This Doherty amplifier can achieve two efficiency peaks and high efficiency between the peaks. The first efficiency peak occurs at 22dBm output power, which is close to the designed 21dBm. The second efficiency peak happens at 28dBm, where output power saturates. When power is backed-off 6dB from the peak power at 28dBm to 22dBm, 48% PAE is achieved. That PAE of the Doherty amplifier is two times that of the Class AB at the same power level. When power is backed-off 12dB to 16dBm, 32% PAE is achieved, which is four times that of the Class AB at the same power level. Overall, high PAE (>40%) is obtained over an approximately 9dB wide region for the Doherty amplifier, and a significant efficiency improvement is obtained over a wide power range. The wide power range of high efficiency is achieved by designing γ=3. It experimentally demonstrates that by using higher impedance ratio γ, the high efficiency range can be widened.

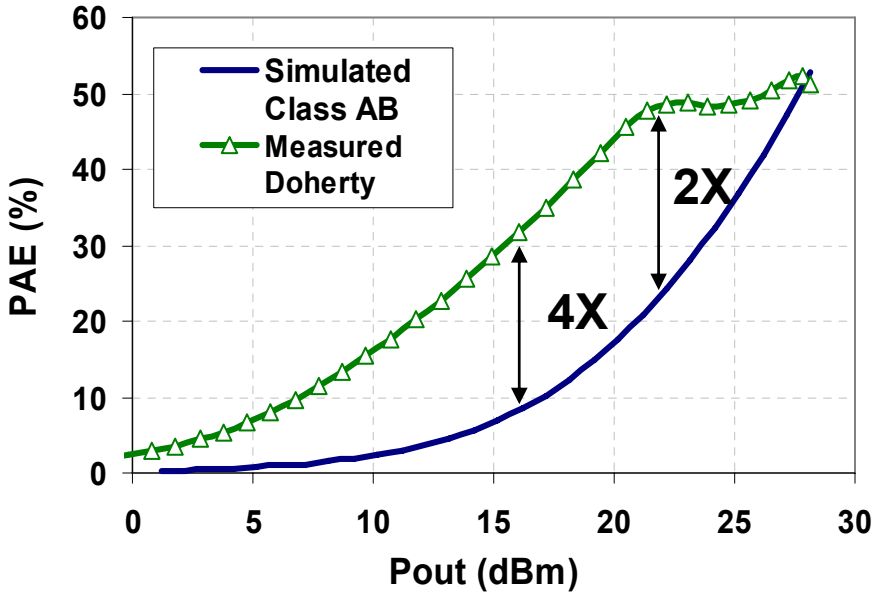


Figure 2.23: Measured PAE of Doherty amplifier and a simulated Class AB amplifier with CW signal input

Average efficiency or average PAE is a more accurate measure of true efficiency of an amplifier when it is used in a system with high signal dynamic range, such as CDMA. The average efficiency is defined in equation (1-3) in chapter1. The average efficiency of the Doherty amplifier can be calculated based on an assumed probability distribution function (PDF) for the output power with IS-95 signals. The PDFs can differ according to the environment of the cellular network. A probability distribution that is intermediate between urban and suburban environments is chosen and shown in Fig. 2.24. The PAE data of the Doherty and the Class AB amplifier are also shown together with the PDF. The figure clearly shows that probability peak happens in the low power region where PAE is very low (<5%). However, reducing DC power in this region is still very important to overall PAE due to the high signal probability in that region. The average PAE calculated based on this PDF for the

Doherty is 18.1%, it is more than 3 times the average PAE for the Class AB PA, which is 5%.

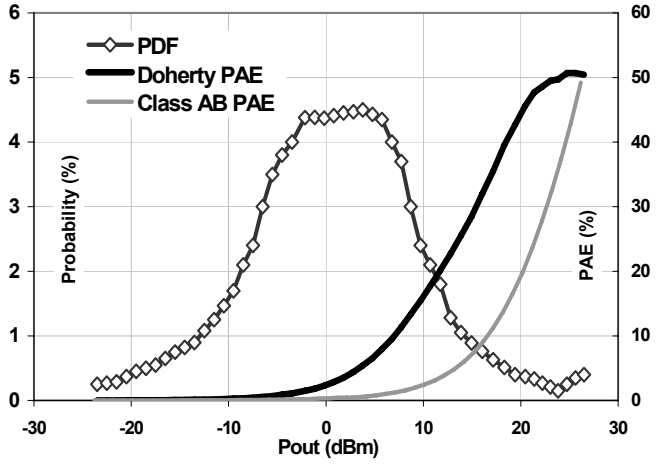


Figure 2.24: Representative PDF data and PAE curves of the Doherty and the Class AB amplifier with IS-95 input

To further illustrate the efficiency enhancement achieved by the Doherty PA, a CDG4 CDMA signal probability distribution function (PDF) was used to calculate the average efficiency. The CDG4 PDF includes both urban and suburban cases separately. Shown in Fig. 2.25 are the CDG4 PDF vs. output power and, also shown are the efficiency curves for the Doherty amplifier and for two commercial available PA modules from Skyworks Inc (first a standard PA, second an advanced PA with bias control to improve efficiency). The calculated average PAEs for all three PAs are compared in Table 2.1 with Doherty PA showing dramatic improvement of average PAE over the commercial amplifiers. It is worthwhile to point out that due to their different maximum output power levels, average PAE of these amplifiers are calculated with their maximum power normalized to a same value.

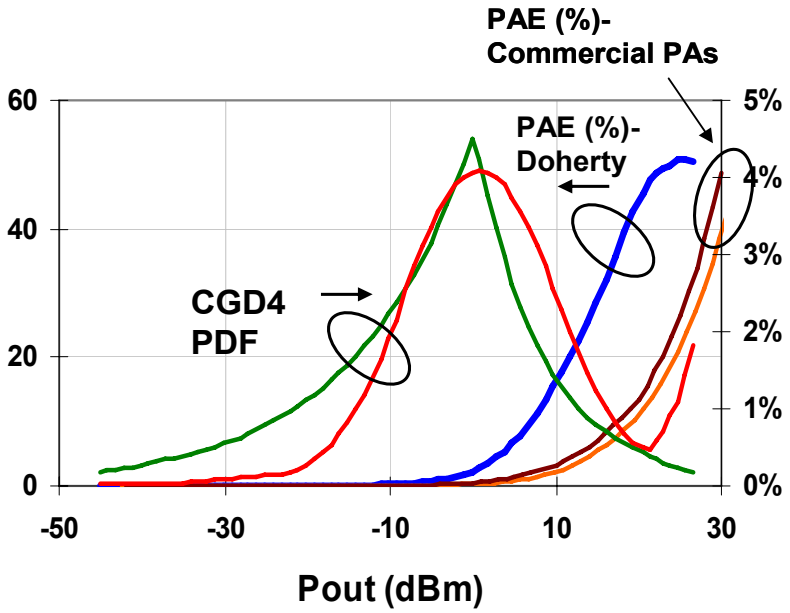


Figure 2.25: PDF of CDG4 signals and PAE of the Doherty and two commercial amplifiers

Table 2.1: Calculated average PAE for the Doherty and two commercial amplifiers

Average efficiency	Skyworks PA I	Skyworks PA II	Doherty PA
Urban	4.65%	6.37%	15.02%
Suburban	12.06%	15.15%	29.35%

2.5.3 Gain and Phase

Shown in Fig. 2.26 are the measured gain and phase of the Doherty amplifier. The gain is relatively flat at low power before the auxiliary amplifier turns on. The

circuit was optimized mainly for efficiency; a low bias voltage of -4.5 on the gate of the auxiliary is applied. A minor roll off of gain at high power still happens even with a 1:2 split ratio at the input of the two amplifiers. Phase variation is as large as 25º at its peak. The non-flat gain and phase leads to linearity degradation in the Doherty amplifier, which will be clearly seen in the measurement data of ACPR.

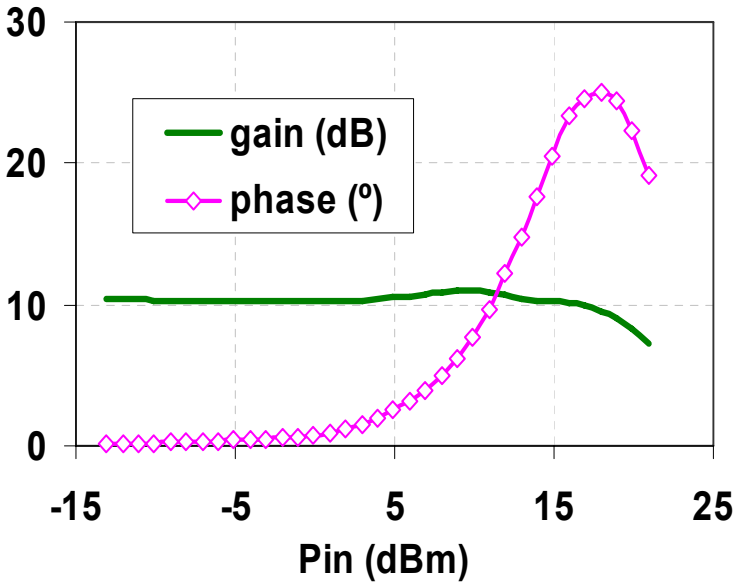


Figure 2.26: Measured gain and phase of the Doherty amplifier with CW signal input

2.5.4 Linearity

Fig. 2.27 shows measured ACPR and PAE vs output power with CDMA IS-95 signal input. In the figure, it can be seen that although PAE with CDMA signal input is still high, ACPR fails to meet the IS-95 specification of -42dBc at about 17dBm output power. This is not satisfactory for system applications. A general reason for this is that the Doherty amplifier needs the main and the auxiliary amplifier to work

accurately in conjunction with another. However, due to nonlinearity inside devices and other parasitics in the circuit, it is difficult to achieve that, especially in the transition region where the main amplifier begins to saturate and the auxiliary amplifier begins to turn on. The bias voltage on the gate of the auxiliary amplifier in this Doherty amplifier was set low to maximize its PAE performance. That contributes to the unsatisfactory linearity performance as well. The nonlinearity in Doherty amplifier is a problem and need to be corrected. The solutions for that will be extensively discussed in chapter 3 and chapter 4 of this dissertation.

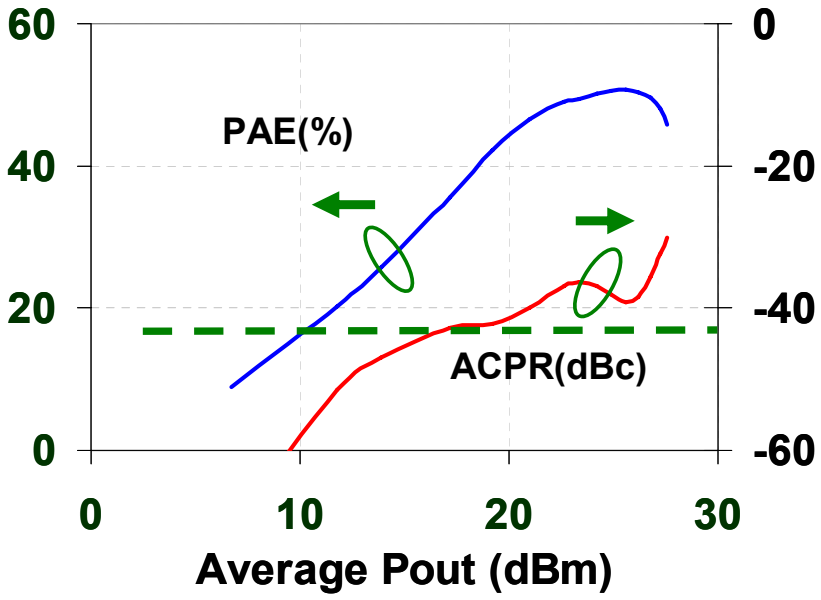


Figure 2.27: Measured PAE and ACPR with IS-95 signal input

2.5.5 Behavioral Modeling

Behavioral model simulation can be used to calculate gain and phase contributions to ACPR separately, which helps to identify major nonlinearity sources

in a Doherty amplifier (and in general, any nonlinear amplifier). The gain and phase data measured with CW signals shown in Fig. 2.26 are used as input to a behavioral model similar to the one mentioned in [7]. Nonlinearity of the PA is represented by AM-AM and AM-PM distortion characteristics in the model. With CDMA IS-95 input signal whose spectrum shown in Fig. 2.28(a), the model can generate the distorted output spectrum which is shown in Fig. 2.28(b).

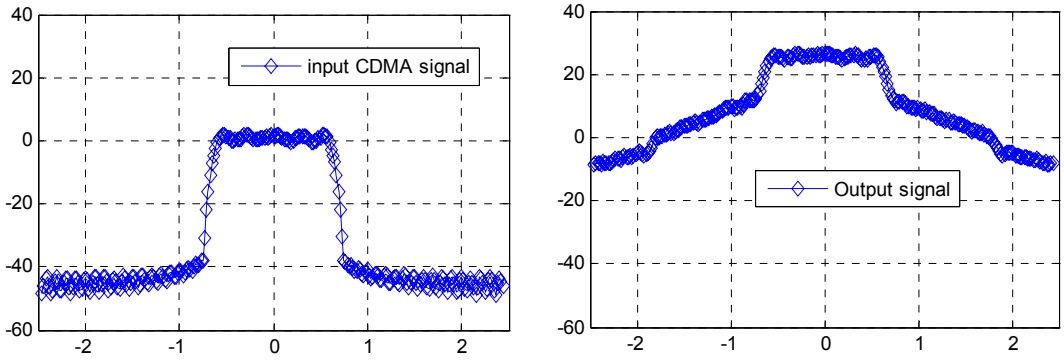


Figure 2.28: Spectrum of IS-95 signal and its distorted output by the Doherty amplifier based on behavioral modeling

The simulated ACPR of the Doherty PA is shown in Fig. 2.29 and is compared with the measured result together with ACPRs calculated with only gain or only phase distortion contribution (that is, ACPR calculated using ideal flat phase or flat gain in the behavioral model). It can be seen that phase variation with power (AM-PM distortion) is a major source of ACPR in the amplifier from low to medium power levels, and cannot be neglected in the linearization approach chosen. However, at high power levels, AM-AM distortion dominates as gain is heavily compressed. That is not surprising according to Fig. 2.26 because although absolute phase variation from low

power to peak power is large, the phase is rather stationary at high power, and thus its derivative, which is more directly related to nonlinearity, is small.

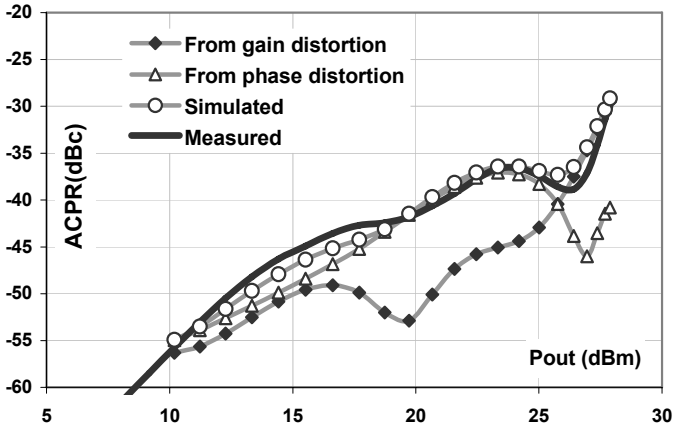


Figure 2.29: Measured and simulated ACPR results of the Doherty amplifier

Further use of the behavioral model can give us simulated results of EVM (Error Vector Magnitude, defined in chapter 1) in Fig. 2.30. The EVM results have similarity to ACPR results, not surprisingly. EVM requirement in CDMA systems is not very strict, for example, a WCDMA mobile transmitter only requires EVM to be less than 17%. In general, CDMA and WCDMA standards have strict requirements about spectrum regrowth induced-interference in adjacent channel and relatively less in-band signal accuracy requirements. But in an 802.11a/g WLAN system, which uses OFDM modulation schemes, EVM specification for the transmitter can be as low as 5%. This requires a very small in band signal degradation. Nonlinearity in the power amplifier is a major source of EVM degradation and thus need to be minimized.

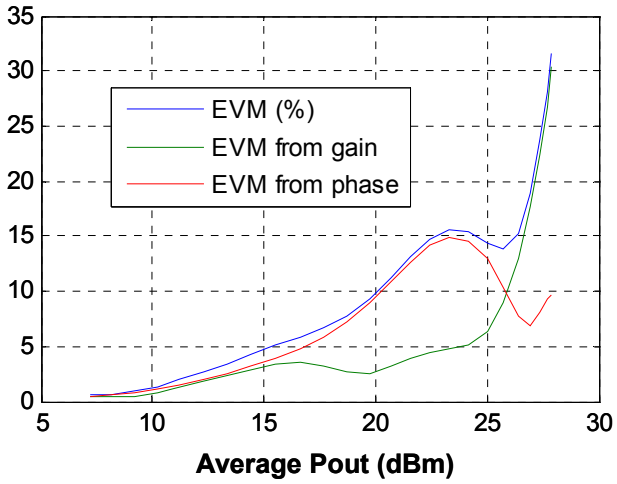


Figure 2.30: Simulated EVM of the Doherty amplifier

IMD3 performance in a two-tone input can also be simulated based on the behavioral model using the measured gain and phase data as input. Simulation results in Fig. 2.31 show that IMD3 becomes worse than -30dBc when Pout reaches 16dBm. This agrees reasonably with the power level where the ACPR fails the -42 dBc specification in CDMA case, although the two cases have different types of signal inputs and the average output power can not be compared point by point directly. In general, there is significant but not explicit correlation between the IMD3 and ACPR results for numerous nonlinear amplifiers.

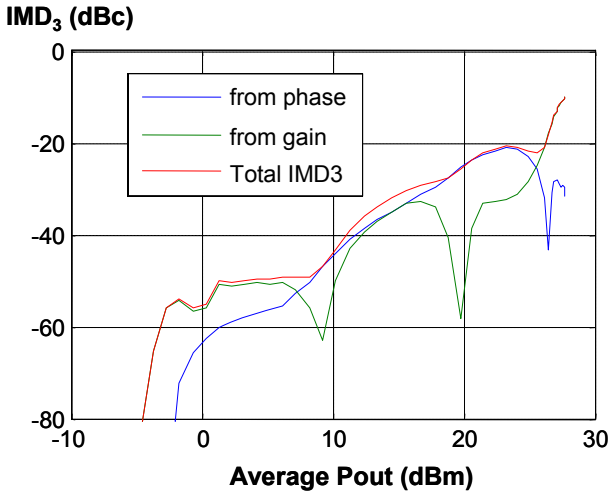


Figure 2.31: IMD3 of Doherty output in simulation

2.6 Lumped Element Doherty Amplifier

A traditional Doherty amplifier needs two quarter-wave lines, one for impedance transformation and one for phase compensation. Those two microstrip lines are physically the largest components in a Doherty structure, and they make it difficult to integrate the amplifier into small modules, since $\lambda \approx 48$mm at 900MHz using common dielectric materials. In this section, we demonstrate a Doherty amplifier with all lumped LC components for 900MHz operation. The quarter-wave lines are replaced with C-L-C and L-C-networks (Fig. 2.32). It is known that if $\omega L = 1/\omega C = Z_0$, then the C-L-C network can achieve the same function $Z_{in} = Z_0^2/Z_L$ as the quarter wave transmission line. The same rule applies for the L-C-L network. Consequently, the circuit area consumed by a Doherty amplifier with this replacement will be dramatically reduced while its high efficiency performance can be maintained.

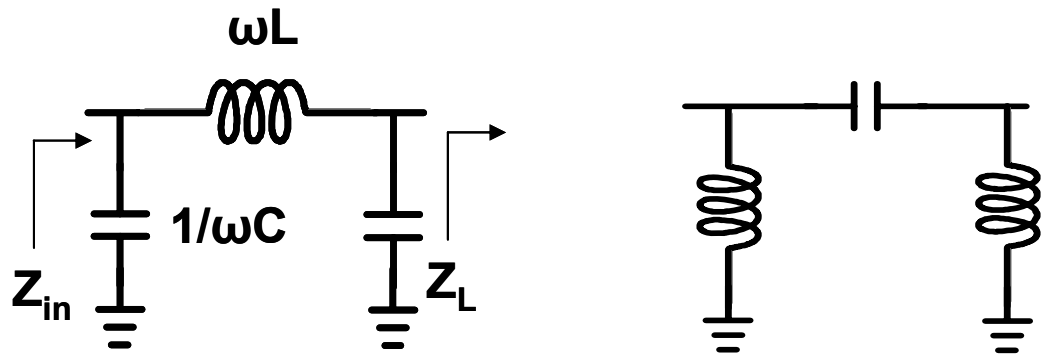


Figure 2.32: Lumped element replacement of quarter-wave transmission line

Shown in Fig. 2.33 is a block diagram of the Doherty amplifier with lumped element reactances. Instead of a quarter-wave microstrip line, a C-L-C (9.1pF, 2.7nH) Pi network impedance transformer is put between the main and auxiliary PAs, which also delays the output from the main PA by 90 degrees. To compensate that phase shift, another L-C-L Pi network 90-degree phase shifter is put before the matching network of the auxiliary PA. Another L-match is used at the output of the Doherty PA to match an ~ 5 Ohm load impedance of the Doherty amplifier to 50 Ohm.

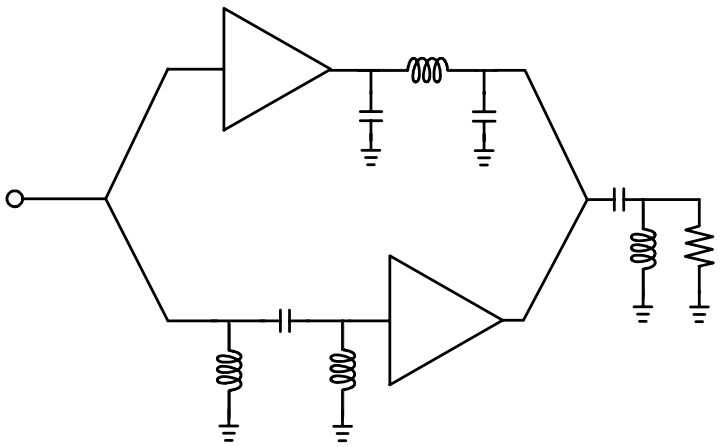


Figure 2.33: Schematic of the lumped element based Doherty amplifier

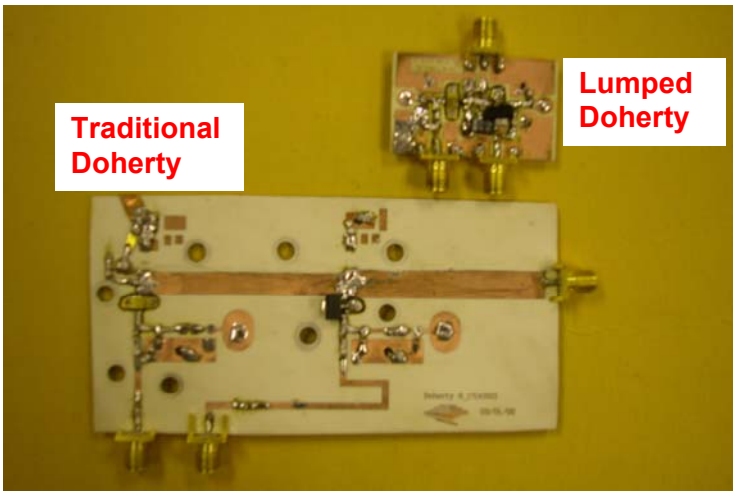


Figure 2.34: Photograph of a transmission line based Doherty amplifier compared with the lumped element based Doherty

For measurement, a lumped element based Doherty amplifier circuit was fabricated on PCB board using the same MWT871 and CLY5 GaAs MESFETs devices as the transmission line based Doherty amplifier (traditional Doherty) discussed in section 2.5. A photograph in Fig. 2.34 shows both of the circuit boards. The circuit area of the lumped element based Doherty amplifier is significantly smaller than the transmission line based Doherty amplifier. At the same time, high efficiency of a Doherty amplifier is maintained for the lumped element based Doherty amplifier as shown in Fig. 2.35, which shows high PAE (>40%) is obtained over an approximately 6dB wide region, similar performance to that of a traditional Doherty PA. This PAE performance is also compared with a simulated Class AB biased amplifier with similar configurations in Fig 2.36.

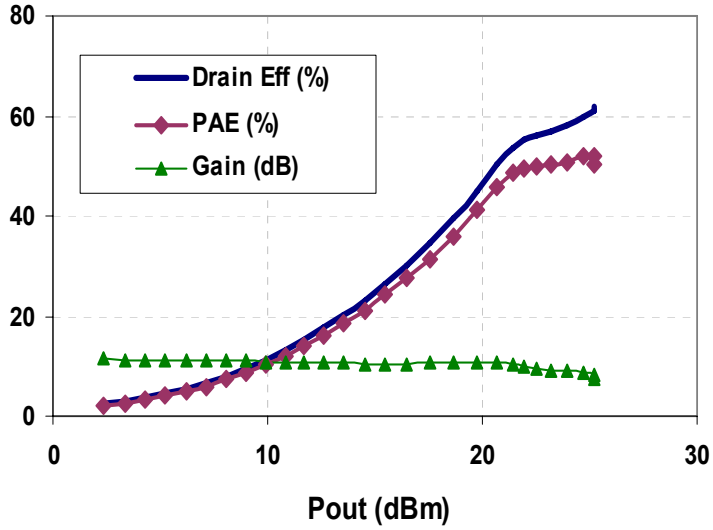


Figure 2.35: Measured Efficiency and gain of the lumped element based Doherty amplifier

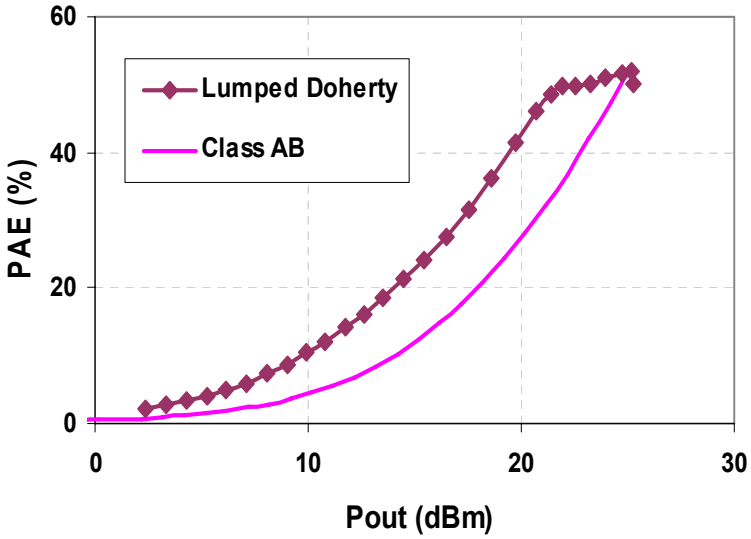


Figure 2.36: Measured PAE of the lumped element based Doherty amplifier compared with PAE of a simulated Class AB amplifier

In addition to efficiency performance, the lumped Doherty PA shows a 1dB bandwidth of about 110MHz (in terms of measured S21 vs. frequency) as can be seen in Fig. 2.37. This bandwidth is only slightly narrower than the bandwidth of the previous distributed Doherty PA from simulation and the bandwidth is adequate for

CDMA applications. One more issue of the lumped element networks is that it can have considerable resistive loss resulting from the use of inductors. This needs to be carefully dealt with when the lumped network is integrated on chip due to typical low Q on chip inductors [8].

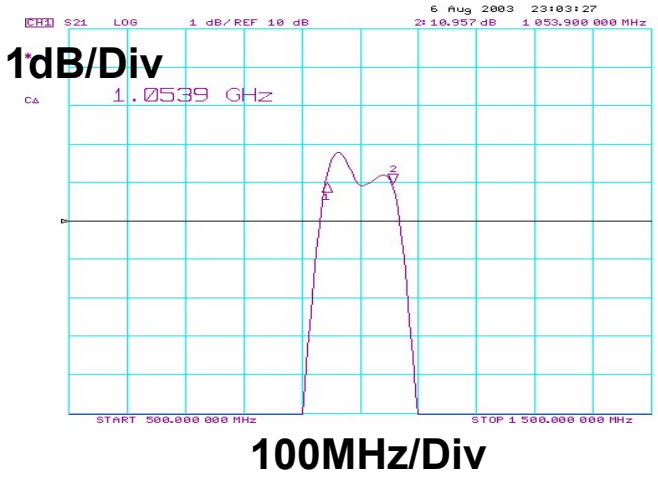


Figure 2.37: Measured bandwidth of the lumped element based Doherty amplifier

The results of the lumped element based Doherty amplifier further demonstrates that the Doherty amplifier structure is a very promising technique for wireless portable transmitters. Matching networks with lumped elements make the whole Doherty circuit ready to be integrated into a single chip or a small module.

2.7 Summary

In this chapter, the operational theory for a current source based Doherty amplifier was developed. Understanding of ideal behaviors in a Doherty amplifier can thus be achieved. Following that, practical design issues such as ***load impedances***,

transistor sizes, ***input split ratio***, ***optimum bias voltage*** for the auxiliary amplifier and ***harmonic terminations*** were all discussed. A GaAs MESFET Doherty amplifier was first designed in simulation and then fabricated on PCB board with the quarter-wave line impedance inverter implemented by microstrip lines. Simulation and measurement results were both discussed. The measurement results of the Doherty amplifier show high PAE (>40%) extended over a 9 dB output power range. Measured linearity results were also discussed and behavioral modeling was used to further analyze the observed linearity. At the end of this chapter, measurement results of a lumped element based Doherty amplifier were discussed. This demonstrates the possibility of an integrated Doherty amplifier.

2.8 Acknowledgements

The author of this dissertation wants to thank Masaya Iwamoto for providing background material for the Doherty amplifier research described here. Dr. Iwamoto also published the theory of the extended Doherty amplifier.

2.9 Reference

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Chapter 3
DSP Linearization of Doherty Amplifier

3.1 Introduction

In chapter 2, measured results of the GaAs FETs based Doherty amplifier clearly show that Doherty amplifier is capable of achieving high efficiency over a wide range of output power. This feature is highly advantageous in mobile phone applications where the output power can vary over a very wide range. Another highly desired feature in mobile systems using amplitude modulated signals for sake of spectrum efficiency is linearity. However, the measured GaAs FETs based Doherty amplifier reveals non-constant gain and phase behaviors as function of power. That is not uncommon in Doherty amplifiers and is detrimental to linearity of the system.

An invaluable technique to improve the performance of the power amplifiers is to incorporate digital signal processing (DSP). DSP has been widely applied to base station amplifiers to improve linearity [1]. In most instances, DSP is used as means of providing digital predistortion at the baseband. Alternatively, DSP can be used to monitor and control other aspects of the amplifier such as the amplifier power supply voltage [2]. In this chapter, we will show that the use of DSP for gate bias control combined with digital phase predistortion is highly beneficial in correcting the gain and phase characteristics of the Doherty amplifier and thereby improving its linearity.

In this chapter, a power amplifier system for CDMA applications which consists of a Doherty amplifier and a digital signal processing (DSP) controller will be presented. The 840MHz GaAs MESFETs based Doherty amplifier discussed in Chapter 2 is used in the system. DSP is used to dynamically adjust the gate bias of the auxiliary (peaking) amplifier at the rate of the signal envelope to obtain gain flatness (i.e. AM-AM distortion correction). Furthermore, DSP is used as a digital predistortor to adjust the phase at baseband (i.e. AM-PM distortion correction). In this work, the DSP was implemented externally with a board controlled by a personal computer. It is shown that by utilizing these DSP techniques, the overall linearity and efficiency characteristics of the Doherty amplifier can be significantly improved. To complete the performance evaluation of the system, issues such as bandwidth (digital predistortion vs. analog component based predistortion) and synchronization (between input signal envelop and control signal) will also be covered in this chapter.

3.2 The Need for Digital Control

It is a well proven conclusion that DSP can be used to dynamically change a variety of parameters to improve performance of numerous types of power amplifiers. This practice is especially widespread for base station power amplifier applications. But the Doherty amplifier has some special characteristics that make DSP a particular effective tool to improve its performance. The gate bias of the auxiliary amplifier (V_{gg2}) plays an important role in the performance of the Doherty amplifier. As already shown in Fig. 2.11 and Fig. 2.13 in chapter 2, changes of V_{gg2} can result in different gain and PAE vs. power characteristics for the Doherty amplifier.

Here we summarize measured and simulation data of the GaAs FETs based Doherty amplifier from chapter 2 in Fig. 3.1 and Fig. 3.2. Fig. 3.1 shows the measured gain and phase and the resultant ACPR of the Doherty amplifier tested with a CDMA IS-95 signal. Because the circuit was solely optimized for efficiency, the gain and phase were found to vary significantly with change of power levels, especially when output power is high. Correspondingly the ACPR behavior of the Doherty amplifier increases above the -42dBc specification in the same power levels. The gain drop at high input power can be corrected by increasing the bias voltage of the auxiliary amplifier with DSP control as implied by Fig. 2.11. This can correct the nonlinearity from gain distortion in the Doherty amplifier.

In Fig. 3.2, calculated ACPR based on the behavioral model is shown. Also shown in Fig. 3.2 are calculated ACPR with only gain or only phase distortion contributions (that is, calculated using ideal flat phase or flat gain in the behavioral model). It can be seen that phase variation with power (AM-PM distortion) is a major source of ACPR in the amplifier. More careful inspection of Fig. 3.2 tells us that gain variation induced distortion is dominant only in the last a few dB of power levels, at lower power levels, the phase variation induced distortion is dominant. While this may not be true for all Doherty amplifiers, phase distortion is clearly a very important part of the story and should not be neglected as done in some previous papers. The mechanism of phase distortion will be discussed in detail for GaAs HBT based single ended and Doherty amplifiers in chapter 4. But in this chapter, DSP based baseband

phase predistortion will be shown to be effective in correcting phase distortions in a Doherty amplifier.

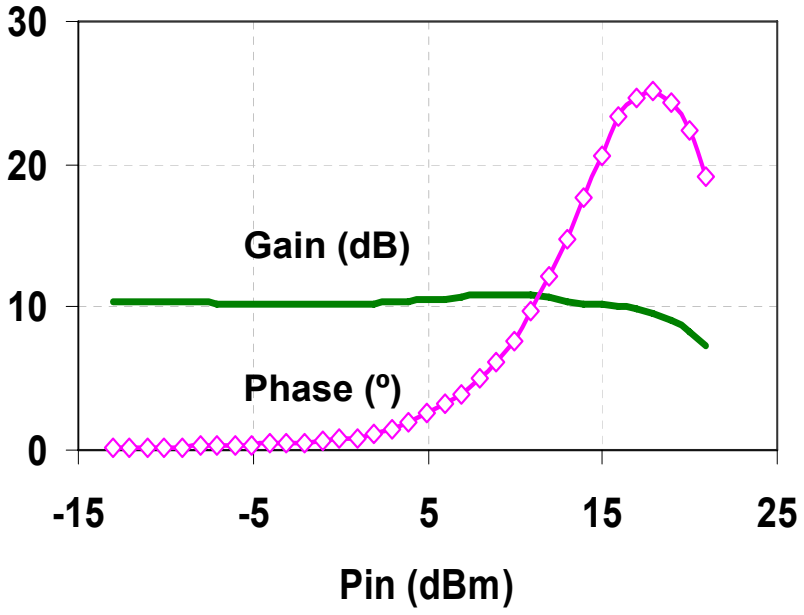


Figure 3.1: Measured results of gain, phase and ACPR under single tone testing for a MESFET-based Doherty amplifier

Fig. 2.13 tells us that the efficiency characteristics can be tailored by adjusting the value of the gate bias, where lower gate bias (i.e. lower drain current) results in higher efficiencies in the low power region. While from an efficiency point of view, a lower gate voltage is desired, the consequence of not supplying enough current from the auxiliary amplifier (i.e. lowering the gate voltage) is a decrease in the overall gain, which can be seen in Fig. 3.1. DSP control can alleviate this problem by dynamically changing the bias voltage of the auxiliary amplifier according to the instantaneous envelope of the input signal. The DSP control will enable the optimum low bias for

efficiency in the low power region and the increased bias for linearity improvement at high power. More detail will be shown in the following section.

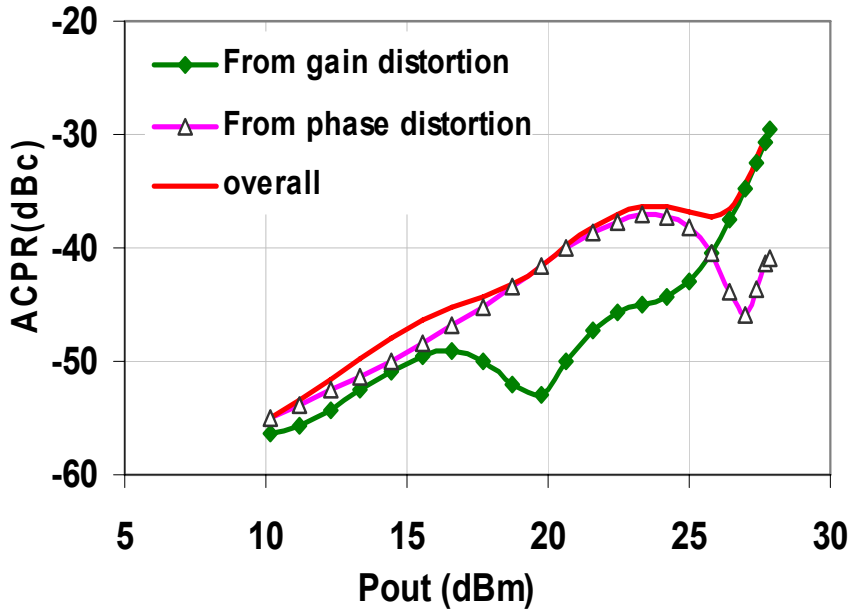


Figure 3.2: Simulated ACPR of the Doherty amplifier and ACPR contributions from gain or phase distortion alone

3.3 DSP Control Strategy for the Doherty Amplifier

The linearization strategy based on DSP is twofold: (A) dynamically adjust the gate bias of the auxiliary amplifier at the rate of the signal envelop to obtain gain flatness (i.e. AM-AM distortion correction); and (B) use DSP to adjust the phase of the input signal at baseband for AM-PM distortion correction. DSP control over the Doherty amplifier with the system shown in Fig. 3.3 was studied. Baseband signal is generated in the form of I & Q, and then up-converted to RF. After being amplified by a pre-amplifier, the signal is split by a 1:2 ratio Wilkinson power divider into the main

and auxiliary amplifier paths. DSP generates another voltage signal V_{gg2}, which is applied to the gate bias of the auxiliary amplifier. This system is also used for baseband phase predistortion. By doing both AM-AM and AM-PM correction, DSP can solve the problem of compressed gain and non-constant output phase in a Doherty amplifier and provide great linearity improvement.

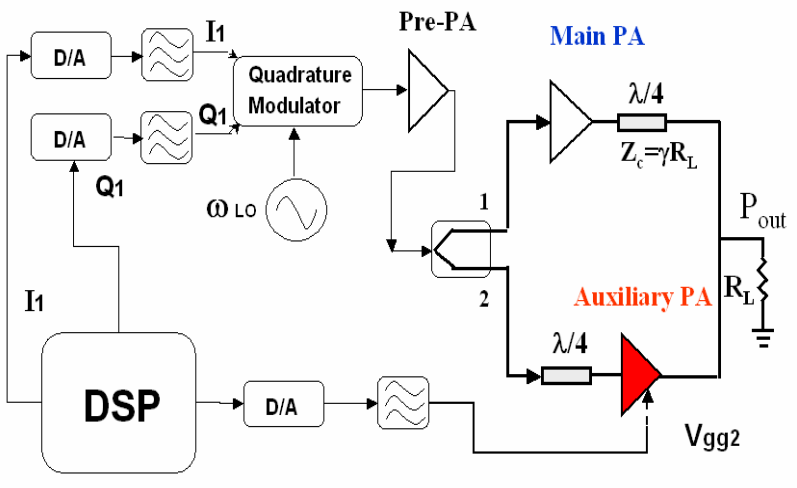


Figure 3.3: System implementation of the DSP with the Doherty amplifier

3.3.1 Gain Correction with Dynamic Gate Bias

Fig. 3.4 shows representative gain curves of a Doherty amplifier with changing bias voltage at the gate of the auxiliary amplifier. Fig. 3.5 shows representative PAE curves of a Doherty amplifier with same conditions. From these representative data, it is evident that: 1. A single fixed gate bias (V_{gg2}) can not satisfy the requirement of a flat gain over the whole output power range; 2. Decreasing bias V_{gg2} to get high efficiency will result in undesired gain compression; 3. At sufficient low power levels, increase V_{gg2} bias to increase gain is ineffective.

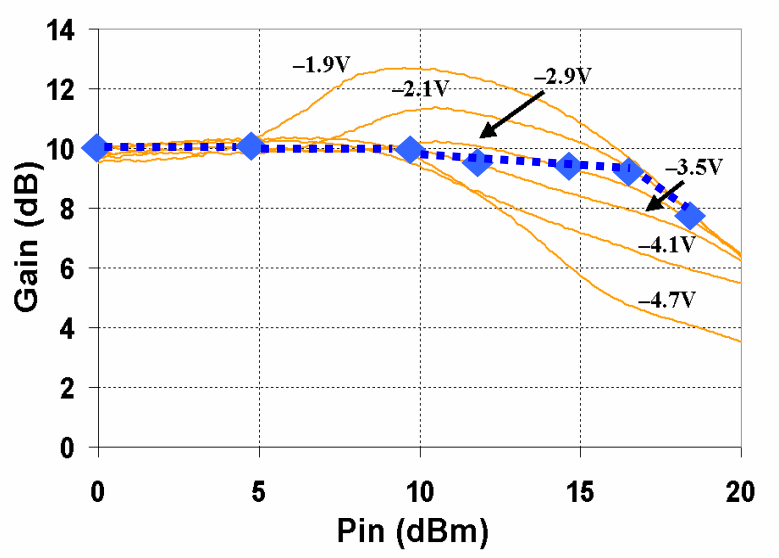


Figure 3.4: Representative data of gain with different bias voltage V_{gg2} on gate of auxiliary amplifier in Doherty

Because of these reasons, it is best for efficiency to keep the bias of the auxiliary amplifier at a low level until input power level reaches 10dBm. Consequently, the feature of increased efficiency peak at low power can be preserved. The diamond points and dotted line in Fig. 3.5 clearly demonstrate this claim. It is then best for gain flatness to increase V_{gg2} with further increase of input power. This helps to maintain the gain as flat as possible through the rest high power levels, which is illustrated in Fig. 3.4 by the diamond points. Not surprisingly, generating such a dynamic bias function for V_{gg2} is exactly what DSP excels in doing.

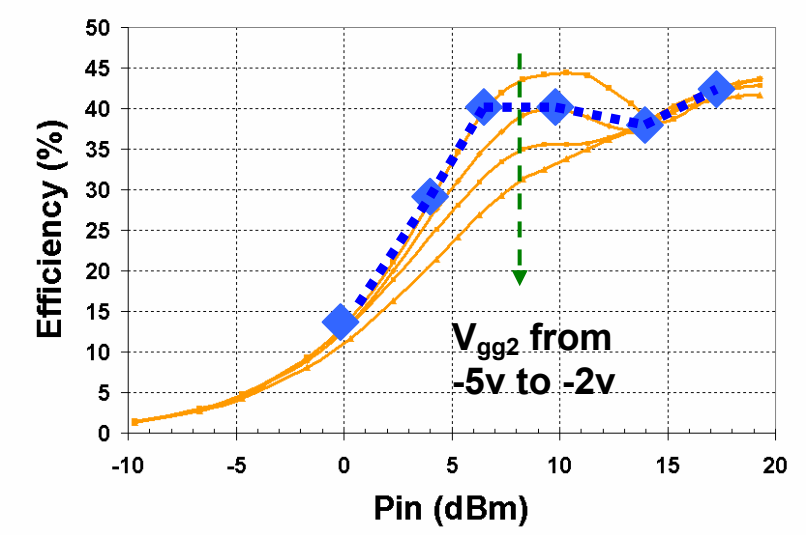


Figure 3.5: Representative data of Power Added Efficiency with different bias voltage V_{gg2} on gate of auxiliary amplifier in Doherty

In order to meet the requirement of a flat gain and a good efficiency tradeoff, the desired auxiliary amplifier gate bias voltages vs. input power were experimentally characterized and are shown in Fig. 3.6 (based on the same GaAs FETs Doherty amplifier). The V_{gg2} curve shows a flat value of –4.7 Volts in low Pin region where the auxiliary amplifier should be shut down to save DC current consumption. V_{gg2} begins to increase nearly linearly after the auxiliary amplifier turns on at P_{in}=7dBm point, where the main amplifier enters into saturation. The increasing V_{gg2} helps to enhance the RF output current contribution from the auxiliary amplifier to the overall Doherty amplifier, thus keep the overall gain flat. On the other hand, the efficiency does not suffer a severe drop at low input power levels as could happen if a constant V_{gg2} is applied over all input levels.

At the input levels high than 17dBm, since the auxiliary amplifier also goes into saturation, increase of the V_{gg2} no longer helps with the gain and the overall Doherty amplifier goes into saturation. As a result, the increase of the V_{gg2} is 'slowed down' to avoid unnecessary DC current draw from the power supply and thus maintain high efficiency.

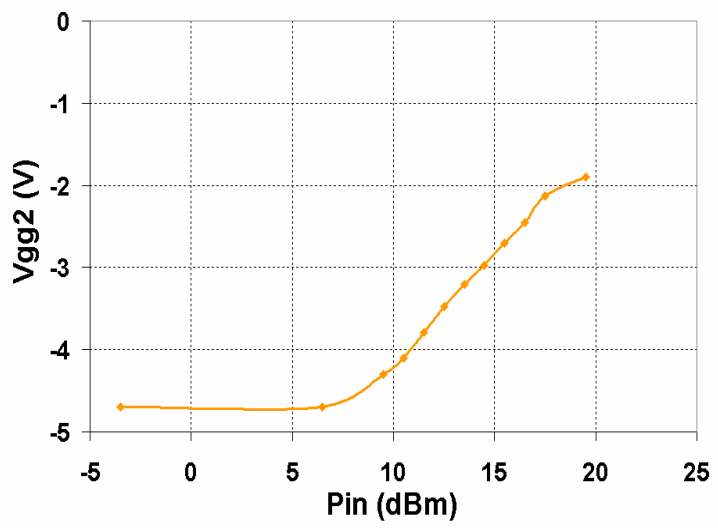


Figure 3.6: Desired gate bias voltage on auxiliary amplifier for flat gain and high PAE in the Doherty amplifier

It should be pointed out that in order to fulfill the desired function of gain control, the gate bias V_{gg2} needs to be controlled at the rate of the signal envelop. When the input signal is CDMA IS-95 with 1.25MHZ bandwidth, the bias voltage V_{gg2} needs to be at a comparable rate. Fig. 3.7 shows a representative time domain measurement of V_{gg2} and a CDMA IS-95 envelope waveform. In Fig. 3.7, the dynamically changing gate bias voltage V_{gg2} tracks the input CDMA envelop closely in time dimension (X axis), which shows that they have similar frequency

components. For the amplitude dimension (Y axis), V_{gg2} is a transformed waveform from the input CDMA envelop based on the transfer function mentioned in Fig. 3.6.

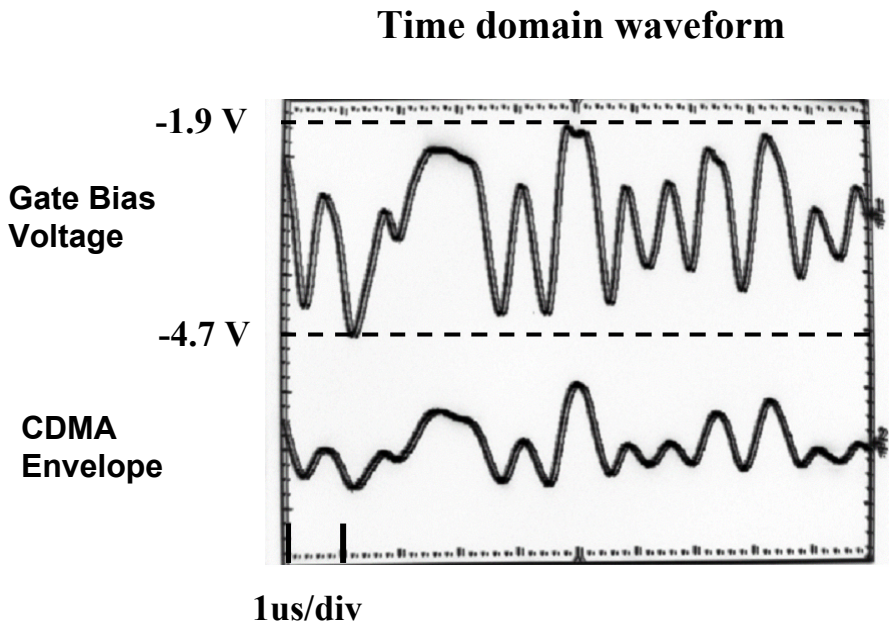


Figure 3.7: Measured control bias voltage and CDMA envelope

The dynamic gate bias control strategy requires detailed characterization of the gain vs. power characteristics over a wide range of gate voltages. This is accomplished by performing a single tone power sweep with an Agilent 8753ES vector network analyzer. By recording the bias voltages and building an interpolated table in Matlab, the optimum V_{gg2} values which maintain constant gain and maximize efficiency can be calculated for each instantaneous signal power. V_{gg2} is outputted to the gate bias network of the auxiliary amplifier at the same delay as the RF input signal of the auxiliary amplifier.

3.3.2 Phase Correction with Baseband Predistortion

Phase distortion (AM-PM) was also found to play an important role in influencing the ACPR, particularly in the region when the auxiliary amplifier is turned on. This is evident in the output phase vs. power shown in Fig. 3.1 where the phase varies as much as 25°. Generally speaking, phase distortion in Doherty amplifier rises from varies mechanisms. The phase distortion of Class AB biased main amplifier can dominate phase distortion of Doherty amplifier in the low power region, where the auxiliary amplifier is off. In high power region, interactions between main and auxiliary amplifier usually dictate the phase behavior. A number of things can shape output phase, including device characteristics, bias level and output impedance levels. In Doherty, because a dramatic load-pulling behavior happens between the two building-block amplifiers, it is very difficult to maintain small phase distortion over the full dynamic range. The mechanism of phase distortion will be addressed a little further in chapter 4 in a case of a GaAs HBT device based Doherty amplifier.

In this work, digital phase predistortion was carried out at baseband to solve the AM-PM distortion issue, to further improve the linearity of the Doherty amplifier. First, phase data from the same measurements made for the gain characterization was analyzed. Fig. 3.8 shows AM-PM distortion curves measured at various values of V_{gg2}. From the table of gate bias voltages calculated for gain compensation, a list of phase values interpolated from the data in Fig. 3.8 that correspond to the respective gate biases is created as a function of output power. Such a plot is shown in Fig. 3.9.

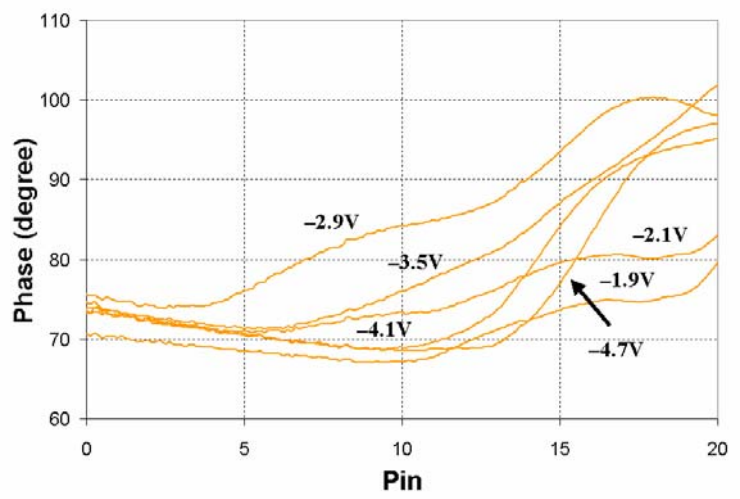


Figure 3.8: Output Phase vs. input power with different bias V_{gg2} of the auxiliary amplifier

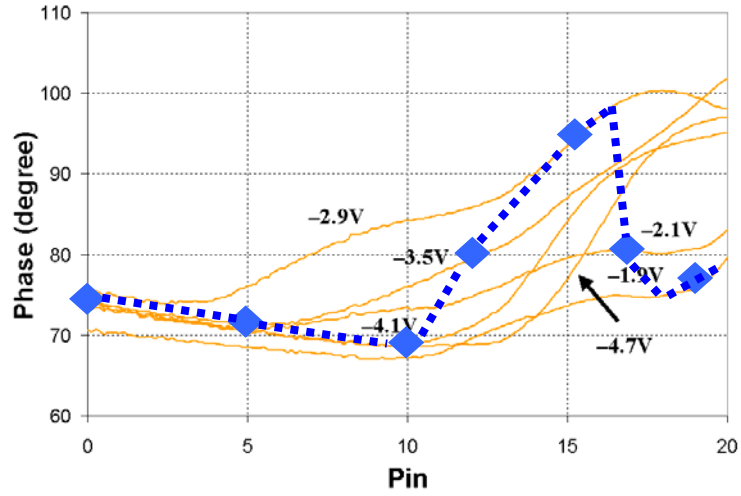


Figure 3.9: Output Phase vs. input power with different bias V_{gg2} of the auxiliary amplifier

It is noticeable that the dynamic bias set by the requirement of gain and efficiency tradeoff can result in a dramatic change of output phase, exceeding the existing phase distortion from the Doherty amplifier itself. If not compensated through predistortion, this can lead to severe distortion output. To compensate for this, the

"mirror image" of this data is calculated for the phase predistortion data, normalized, and programmed into the DSP controller. This phase predistortion data is also shown in Fig. 3.10.

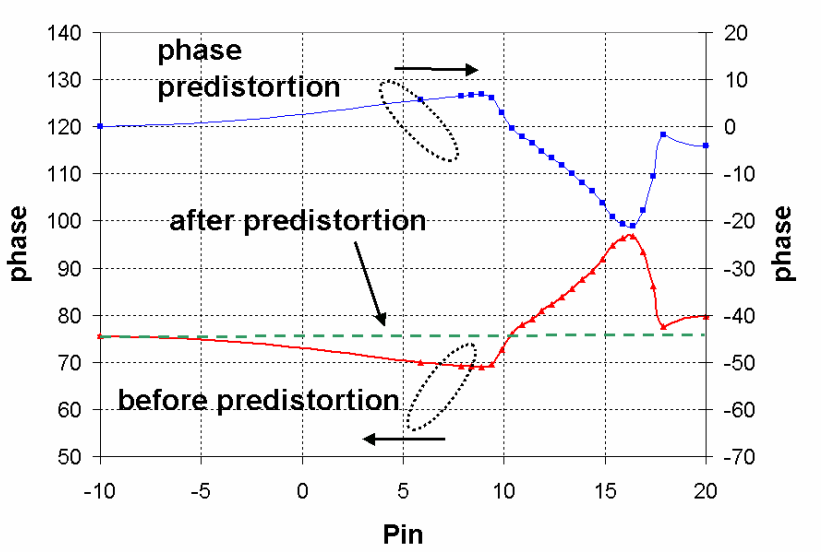


Figure 3.10: AM-PM distortion of DSP controlled Doherty amplifier and the predistorted phase

It should be noted that the conventional approach of gain predistortion at baseband gives very little benefit in improving the ACPR in the system described in Fig. 3.3, since it is ultimately the gate bias of the auxiliary amplifier that limits the overall gain of the Doherty amplifier. Even if the power at the input is increased (assuming gain compression compensation), this will further force the main amplifier into saturation and gain will be reduced. In order to effectively apply gain predistortion to the Doherty amplifier, separate input paths for the main and auxiliary amplifiers have to be supplied so that the input drive levels can be independently adjusted. Therefore, we choose not to apply gain predistortion here. For the DSP

linearization strategy described in this chapter, gain distortion is corrected first by the dynamic gate biasing of the auxiliary amplifier (as described in the previous subsection), and subsequently, the phase is corrected by predistortion of the phase at baseband based on the dynamic gate bias voltage values from gain correction.

3.3.3 System Model and Synchronization Issues in DSP Control

3.3.3.1 System Model

Assuming that all the circuit components used in the system have enough bandwidth to cover the modulated signal in envelope domain, a simple bandpass model can be used to represent signal flow in the DSP-controlled Doherty amplifier system. This bandpass model method is the mathematical basis for generating the predistorted baseband signals in DSP. Based on the model, the input signal envelop for the Doherty amplifier can be written as:

$$V_{in}=A_{in}*\exp(j*\pi*\theta_{in}) \tag{3-1}$$

A_{in} is the time dependent amplitude of the input signal envelop and θ_{in} the phase. When the input signal passes through the nonlinear power amplifier, the output signal envelop will be:

$$V_{out}= V_{in} * F_{amplifier} \tag{3-2}$$

$F_{amplifier}$ is the nonlinear transfer function of the power amplifier.

$$F_{amplifier} = Gn(A_{in})*\exp(j*\pi*\theta(A_{in})) \quad (3\text{-}3)$$

The amplitude and phase distortions from the PA are embodied in the functions Gn (A_{in}) and θ (A_{in}), respectively. Gn (A_{in}) and θ (A_{in}) are both nonlinear functions dependent on the instantaneous input signal envelope power level. By combining (3-2) and (3-3):

$$V_{out} = A_{in}*Gn(A_{in})*\exp(j*\pi*(\theta_{in}+\theta(A_{in})) \quad (3\text{-}4)$$

For the case of the DSP controlled Doherty system, the desired bias V_{gg2} can be generated by using a transfer function $V_{bias}(A_{in})$ based on the relationship in Fig. 3.6. The effect of applying $V_{bias}(A_{in})$ on the gate of the auxiliary amplifier is equivalent to adding a gain correction factor Δgn (A_{in}) to the transfer function except that it also changes the phase response of the Doherty amplifier as explained in the section 3.3.2. The modified phase response can be modeled as $\theta_m(A_{in})$ in the transfer function to replace θ (A_{in}). The phase distortion it generates can be taken care of by a baseband phase predistortion factor, $\Delta\theta(A_{in})$. With that, the output can now be written as:

$$V_{out} = A_{in}*Gn(A_{in})*\Delta gn(A_{in})*\exp(j*\pi*(\theta_{in}+\theta_m(A_{in})+\Delta\theta(A_{in})) \quad (3\text{-}5)$$

If the $\Delta gn(A_{in})$ can effectively cancel out the A_{in} dependence in $Gn(A_{in})$ and make gain of Doherty amplifier constant, the gain distortion can be eliminated. By having $\Delta gn(A_{in})$ and $\Delta\theta(A_{in})$ as correction factors, the nonlinearity of Doherty amplifier in both gain and phase can be cancelled and the output should be linear.

It should be noted that all the signals of interest in this bandpass model are considered in the envelop domain. RF carrier has no involvement in this model.

3.3.3.2 Synchronization Issues

A very important factor that affects the performance of the DSP control is the synchronization between the bias control voltage V_{gg2} and the signal envelop at the input of PA. Since the bias control voltage V_{gg2} and the input signal are generated separately through DACs and filter chains of their own, and the input signal will be further delayed by other circuit components before entering the gate of the auxiliary amplifier, they can experience different group delays. The group delay difference between the two can result in asymmetry in output spectrum sidebands thus degrading the IMD3 or ACPR results. An example of this distortion is shown in Fig. 3.11, where the measured spectrum output of a nonlinear GaN amplifier shows asymmetry in 3rd order inter-modulation under two tone test [3]. This GaN amplifier is a single ended amplifier with dynamic gate bias control for linearity improvement. Unlike the case of dynamic bias control in the Doherty, the bias control in this case does not affect the efficiency of the amplifier very much. The green curve in Fig. 3.11 is the measured spectrum when input and bias control are not well synchronized. It shows uneven 3rd order sidebands which degrades the overall IMD3 results. Compared with that, the blue curve, which has input signal and bias well synchronized, shows more symmetric sideband and better IMD3 results [5]. Uneven sidebands can also happen with wide band input signals such as CDMA or OFDM signals if input and bias is not well matched in group delay.

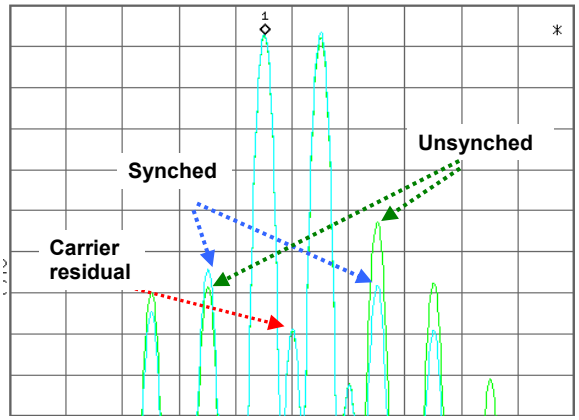


Figure 3.11: Uneven 3rd order sidebands as a result of bad synchronization between input signals and gate bias control signal in a GaN amplifier

Based on the bandpass model, system level simulation can be done to further understand the effects of group delay difference between bias control and the signal envelop. In the simulation, the output signal is represented as in (3-5), except that the Δgn function is shifted intentionally in time domain by a group delay of τ. The value of τ is swept from 0 to 2.5 us, which is about 3 times the chip length in IS-95. The sweep of τ emulates the effect of different group delay difference between bias control signal V_{gg2} and the input signal envelop. Simulation results of ACPR and EVM as a function of delay difference are shown in Fig. 3.12 and Fig. 3.13. Simulation results clearly show that linearity performance ACPR or EVM of the DSP controlled Doherty amplifier can change significantly with group delay difference between bias voltage V_{gg2} and input signal envelop. To attain system performance, a high level of synchronization between the two is needed. In Fig. 3.12, ACPR increase with τ and reaches -42dBc at τ = 2.5 us. Similarly the EVM increases to about 11% at τ = 2.5us. IS-95 signal has an ACPR specification at -42dBc. It does not have an EVM

requirement. But other systems, such as WCDMA and OFDM, have either stringent requirement on ACPR (could be defined differently) or EVM or both. More than that, the ACPR and EVM degradations introduced by bad synchronization can be added on top of linearity degradations introduced by other non-ideal factors in the system, thus its effect is necessary to be minimized.

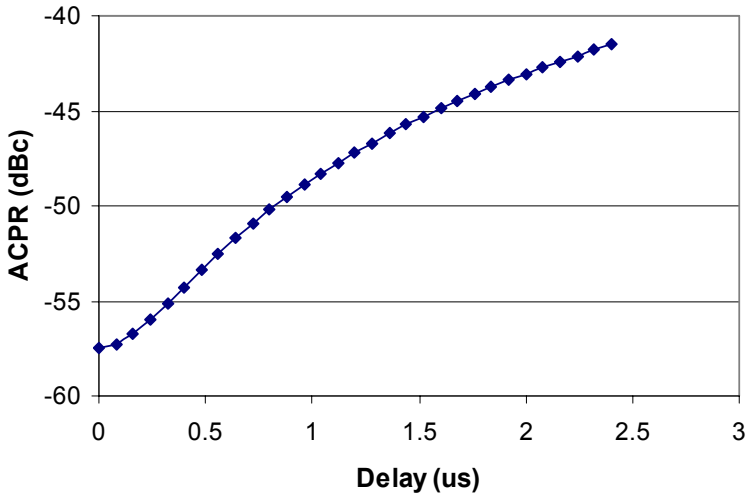


Figure 3.12: ACPR vs. Group delay difference (τ) between input signal and bias voltage Vgg2 on auxiliary amplifier in DSP controlled Doherty system

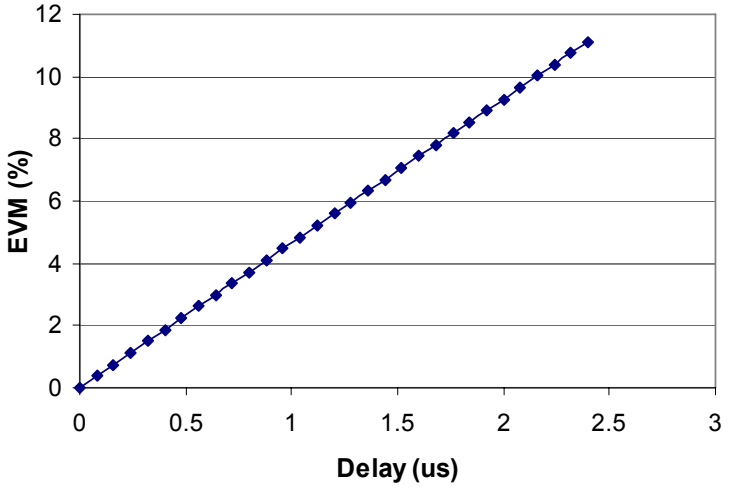


Figure 3.13: EVM vs. Group delay difference (τ) between input signal and bias voltage Vgg2 on auxiliary amplifier in DSP controlled Doherty system

Nonetheless, the synchronization issue is not a severe problem in the narrow banded IS-95 case since a group delay difference on a scale of micro-seconds magnitude is relatively easy to achieve. In the wideband OFDM case, since signal bandwidth is more than 10 times that of the IS-95, the same level of synchronization could be 10 times harder to achieve [4]. In this DSP controlled Doherty amplifier system with IS-95 signal as input, care was taken to ensure a good synchronization between main signal path and bias control signal path. It was ensured by two means: First, physical length of cable, transmission line and group delay of reconstruction filters are carefully matched. This can be considered a coarse tuning; Second, sub-period time delay is added to the bias voltage V_{gg2} by having the data sequence shifted circularly in the digital domain before outputting to DAC. This is a fine tuning process.

3.3.4 Measurement Results of the Doherty Amplifier with DSP Control

To demonstrate the effectiveness of the DSP control strategy to improve linearity and efficiency, the same Doherty amplifier described previously in chapter 2 was used in the system [5]. Fig. 3.14 shows a comparison of ACPR between the original and the DSP-controlled amplifier. The effectiveness of the DSP is very clear, where ACPR1 specification of -42dBc for IS-95 is met over the operating range up to 26.5 dBm, at which point the auxiliary and main amplifiers both saturate. To reach a higher output power, such as the 28.5 dBm requirement of many CDMA amplifier products, a redesign with slightly larger transistors may be employed.

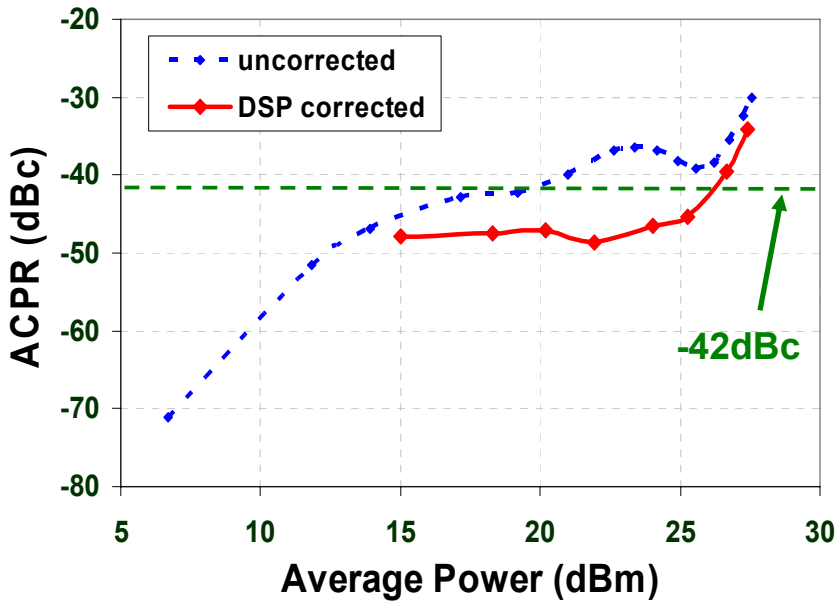


Figure 3.14: ACPR1 (885kHz offset at the right shoulder) vs. CDMA average output power of uncorrected and DSP-corrected amplifier

The ACPR is improved due to the dynamically biased gate voltage of the auxiliary amplifier and baseband phase predistortion. The improvement is as large as 9dB at Pout= 23dBm. On the other hand, the improved ACPR at close to peak power levels, while not large, is significant since it provide the opportunity of operating the Doherty amplifier with less power back-off and thus achieving even higher efficiency performance. Due to system limitations, improvement of ACPR by DSP control below Pout of 20dBm is relatively small. The present results at low power may be affected by noise in the control system.

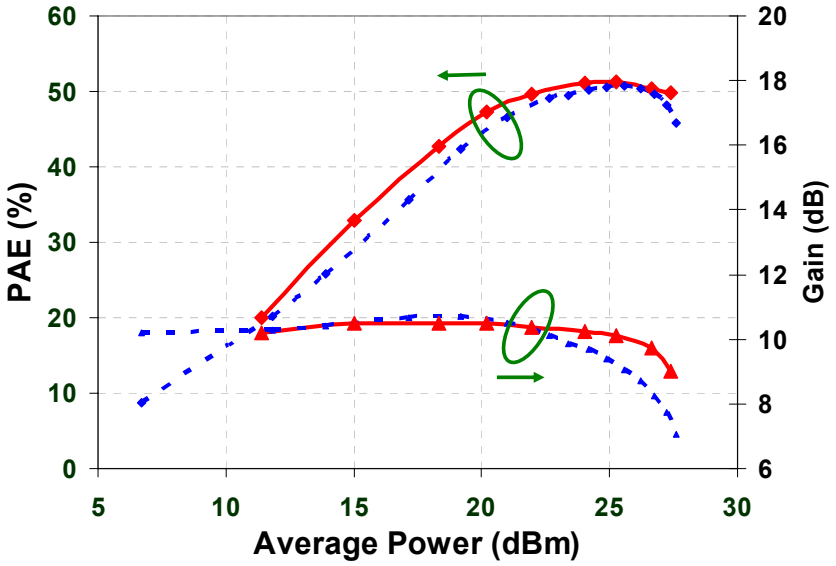


Figure 3.15: PAE and Gain vs. CDMA average output power of uncorrected and DSP-corrected amplifier

Another significant advantage of the DSP controlled Doherty system is that the high efficiency performance of the Doherty amplifier without DSP control is maintained after the DSP is used to improve the linearity, even with IS-95 signal input. This can be seen from Fig. 3.15. In fact, when Pout is between 12 to 22 dBm, PAE of the Doherty with DSP is enhanced. This is because that with DSP, the gate bias of the auxiliary amplifier is lower in the low power region and only becomes higher than the fixed bias case when the input power increases beyond a certain level. DSP-control also improves the PAE in the high power region as seen in Fig. 3.15. This is because the dynamic bias control compensates the gain roll-off, allowing higher output power and thereby increasing PAE. As pointed out in chapter2, average PAE can be calculated based on a chosen signal PDF profile, which is an intermediate between urban and suburban environment. For the DSP controlled Doherty amplifier,

the calculated average PAE based on such PDF is 20%, which is 4 times the average PAE calculated for a Class AB amplifier. This is even high than the 18% average PAE calculated for the Doherty amplifier without DSP control.

Fig. 3.16 shows a spectrum of a CDMA signal at 23dBm average power with and without DSP-control. There is more than 10dB improvement of ACPR (right shoulder) by utilizing the proposed DSP techniques.

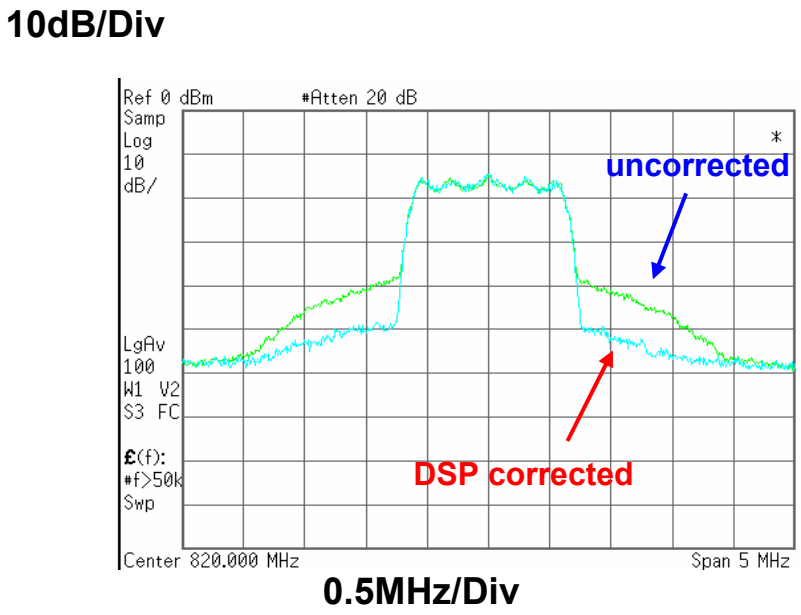


Figure 3.16: ACPR improvement in CDMA spectrum at 23dBm average power

Overall, DSP techniques were applied to the Doherty amplifier in CDMA operation to improve both the linearity and efficiency. AM-AM distortion was corrected by dynamically adjusting the bias of the auxiliary amplifier at the rate of the signal envelope. AM-PM distortion was improved by adjusting the phase of the signal at the baseband frequency. The results clearly demonstrate the importance of synergistically combining DSP with power amplifiers to improve system performance.

3.4 Analog Based Linearity Correction for Doherty Amplifiers

Traditional digital predistortion is powerful in compensating nonlinearities in power amplifiers. However, DSP based methods can impose additional requirements on transmitter circuits; By contrast, analog based predistotion can potentially avoid those requirements. By replacing digital control with control by analog components, one may avoid the need for high resolution, wide bandwidth DACs for the predistorted I and Q signals, which have significantly broader bandwidth than the original signal. On may also avoid difficulties with the channel filters which must be expanded to accommodate the expanded bandwidth of the predistorted signals, and reduce the complexity of the whole up-conversion chain. With linearization based on analog components, one can potentially achieve similar functionality while avoiding extra complexity in the transmitter.

3.4.1 Bandwidth Issue of DSP Control

Today's conventional wisdom suggests that to achieve considerable linearity improvement, baseband predistortion needs a bandwidth that is about three to five times the nominal signal bandwidth. On the contrary, analog component based predistortion can often achieve the same function while avoiding increase of bandwidth. In an analog component based predistortion system, the predistortion of the signal is realized by an analog component, for example a diode or a phase shifter. This analog predistortor either self-generates the predistortion function by having a nonlinear characteristic inverse to that of the power amplifier's, or is controlled by a

baseband signal generated in DSP. The latter is a better choice for sake of accuracy and flexibility. In the controlled case, the system requires additional circuit components for generating control signals, which are first generated digitally in DSP and then converted to analog by DACs. These control signals typically have narrower bandwidth and less amplitude change than a predistorted signal in a baseband predistortion case, and consequently require only low complexity circuit components, although potentially more of them. This is a considerable advantage in general, noting that the cost of analog circuit components can shoot up exponentially with complexity.

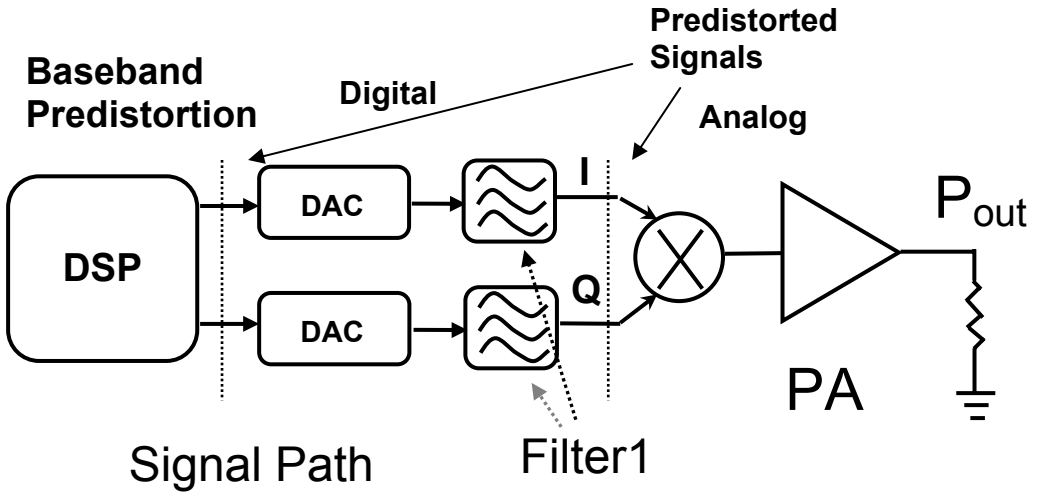


Figure 3.17: Schematic of a baseband predistortion system

An example of a baseband predistortion system is shown in Fig. 3.17. Filter1 in Fig. 3.17 needs a wider bandwidth than that in the original system. Using the bandpass model, output of the system is similar to equation (3-5) and can be written as:

$$V_{out}= A_{in} *Gn(A_{in})* \Delta gn(A_{in}) *exp(j* \pi * (\theta_{in} + \theta (A_{in}) + \Delta\theta(A_{in})) \qquad (3\text{-}6)$$

The predistorted signal before the input of the nonlinear PA can be written as:

$$V_{predistorted} = A_{in} * \Delta gn(A_{in}) * \exp(j * \pi * (\theta_{in} + \Delta\theta\ (A_{in})) \quad (3\text{-}7)$$

The disturbance of $\Delta gn(A_{in})$ and $\Delta\theta(A_{in})$ on A_{in} and θ_{in} is the cause for bandwidth increase in $V_{predistorted}$.

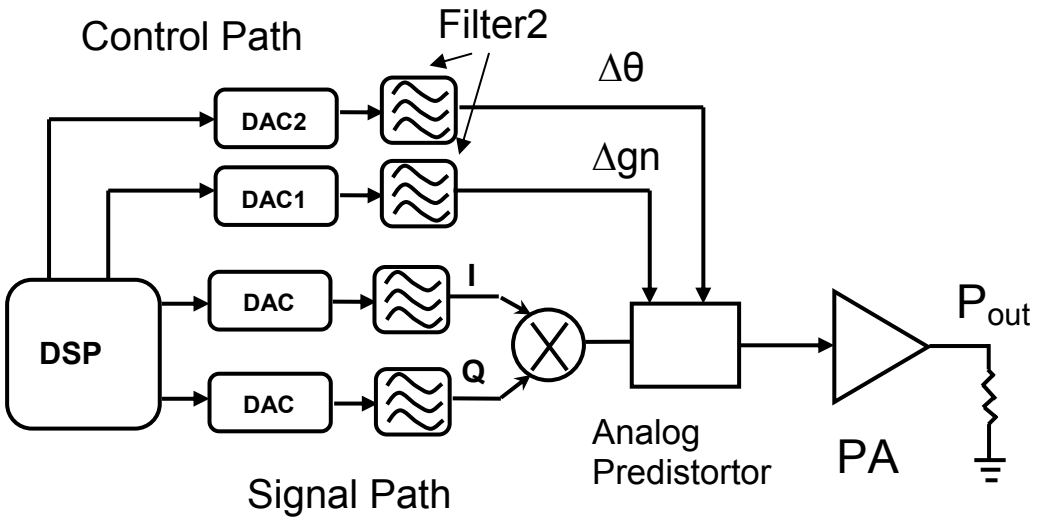


Figure 3.18: Schematic of an analog component based predistortion system

For comparison, an example of the analog component based predistortion system is shown in Fig. 3.18. Unlike the baseband predistortion case, filters in the main signal path can now be kept unchanged. The signal passing through the main path is still $V_{in}=A_{in}*\exp(j*\pi*\theta_{in})$. The control signals are Δgn and $\Delta\theta$, generated by DSP and converted to analog to be applied to the analog predistorter. Both Δgn and $\Delta\theta$ will have narrower bandwidth than that of the 'predistorted signal' in the baseband predistortion case so that bandwidth requirement on Filter2 can be less than that on Filter1. The analog predistortor can be either a phase shifter for phase control or a

diode for gain control, or have both for phase and gain control. The signal after the analog predistortor is the same as the 'predistorted signal', which is $V_{predistorted} = A_{in} * \Delta gn(A_{in}) * exp(j* \pi * (\theta_{in} + \Delta\theta(A_{in}))$. By separating the control function from the original signal, neither the main signals nor the control signals in this system will have a higher than original bandwidth requirement.

As has been pointed out before, all the signals of interest here are considered in the envelop domain. RF carrier has no involvement in this bandpass model based method.

In order to further compare the two predistortion systems, simulations were carried out using CDMA IS-95 signal as input for both systems. The PAs in both systems were implemented in simulation as a black box having the gain and phase characteristics of the Doherty amplifier as shown in Fig. 3.1. For simulation results, the spectrum of the input signal and the 'predistorted signal' are compared in Fig. 3.19. The 'predistorted signal' has a higher shoulder than the input signal. Its spectrum looks just like a distorted output signal of a nonlinear PA. The shape of the shoulder can vary with the input signal power level. In Fig. 3.20, the spectrum of Δgn and $\Delta\theta$ are shown and compared with that of the 'predistorted signal'. Both Δgn and $\Delta\theta$ have a strong DC component since both stay at a constant zero value when input signal power level is low and no predistortion function is needed. The sidebands of Δgn and $\Delta\theta$ are both low and have relatively narrow bandwidth.

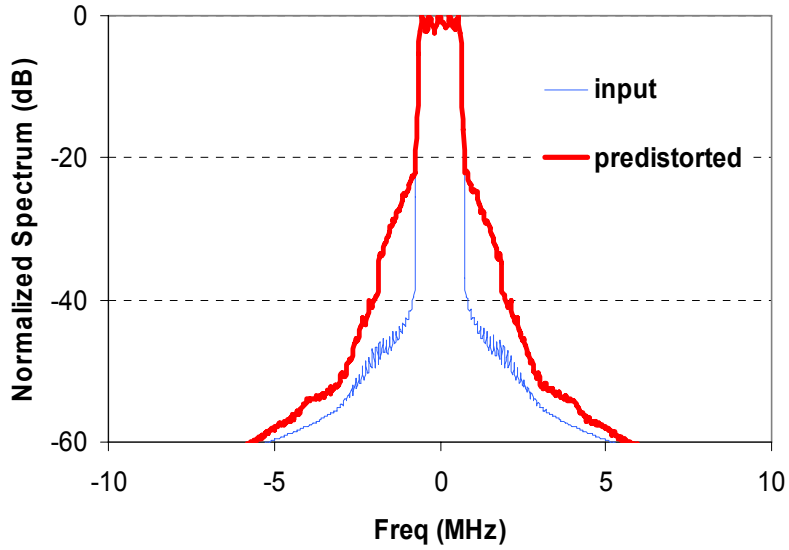


Figure 3.19: Spectrum of input IS-95 signal and the predistorted signal

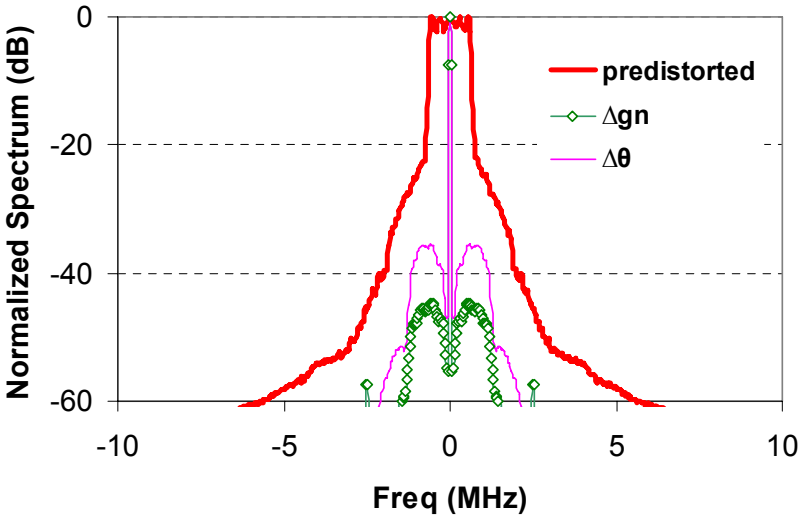


Figure 3.20: Spectrum of predistorted signal in baseband predistortion case and spectrum of Δgn, Δθ for analog component based predistortion case

To quantitatively understand different bandwidth requirement in the two predistortion systems, bandwidth of Filter1 and Filter2 are swept over 1 to 10MHZ range. This can emulate the bandwidth limiting effect in the two systems. Results of simulated ACPR and EVM are shown in Fig. 3.21 and 3.22. The IS-95 input signal

has a bandwidth of 1.25MHz. Fig. 3.21 shows ACPR and EVM performance of the Doherty amplifier with baseband digital predistortion. Both ACPR and EVM drop quickly when bandwidth of Filter1 increases from 1MHz up to around 5MHz. ACPR is about –57dBc and EVM is 5% at this corner point. After that, ACPR and EVM only decrease slowly with further increase of filter bandwidth. The 5MHz bandwidth is directly related to the shoulder width of the 'predistorted signal' in Fig. 3.19. It can also vary with the input signal power level. Fig. 3.22 shows ACPR and EVM of the Doherty amplifier with analog component based predistortion. While ACPR is very similar to that of the other system, EVM starts with a low value at 7% when Filter2 bandwidth is equal to 1MHz. EVM rolls off to about 2% at 5MHz bandwidth and changes little after that. Comparison between Fig. 3.21 and Fig. 3.22 clearly shows that in order to achieve the same level of linearity improvement, the baseband predistortion system needs a wider bandwidth than the analog component based predistortion system.

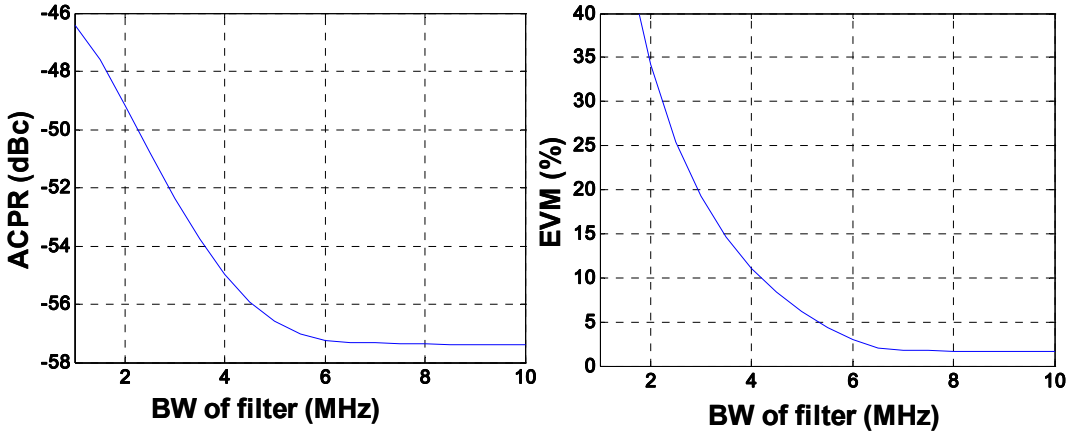


Figure 3.21: Results of sweeping filter bandwidth in baseband predistortion system

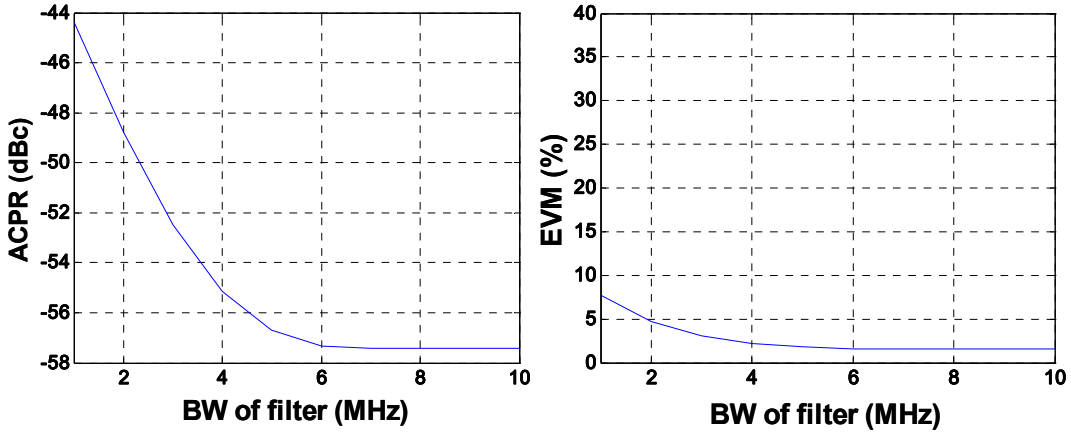


Figure 3.22: Results of sweeping filter bandwidth in analog component based predistortion system

3.4.2 Analog Phase Predistortion

In order to demonstrate the efficacy of the analog based linearization, an alternative way to linearize the Doherty amplifier was carried out by using a BaSrTiO3 (BST) based tunable analog phase shifter. The reason to use this type of control is that the phase variation in a Doherty amplifier is very significant as can be seen in the Fig. 3.23. In this measurement data of a Doherty amplifier, the phase variation was found to be as much as 40°. Consequently, the nonlinearity of the Doherty PA is considered to be mainly from the non-flat phase. In this particular case, gain variation does not contribute to the nonlinearity as much as phase variation. Gain control as mentioned in section 3.3 was not implemented for this measurement but if the gain control does become necessary, we can always use the same gate bias control scheme as described in section 3.3 to correct Doherty amplifier's gain distortion to achieve further linearity

improvement. In addition, the Vgg based gain control is also controlled in analog fashion, giving lower bandwidth and resolution requirement to the DACs used to generate the control signals.

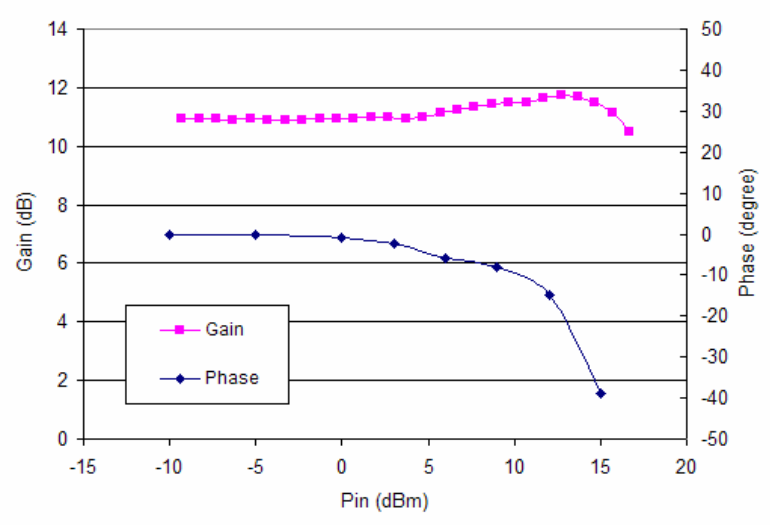


Figure 3.23: Measured gain and phase vs. input power of Doherty with single-tone input

DSP is used to control the phase shifter to predistort the phase of the input signal in the RF domain. This implementation not only helps to correct the nonlinearity caused by the non-flat AM-PM characteristic of the Doherty PA, but also relieves the high bandwidth and resolution requirements on circuit components, which are typical in a digital predistortion configuration. As a result, the Doherty amplifier's linearity is improved and its high efficiency performance maintained.

The block diagram of the proposed scheme to linearize the Doherty amplifier with a BaSrTiO3 (BST) based phase shifter is shown in Fig. 3.24. This phase shifter is controlled by DSP to provide phase predistortion in the RF signal path before the PA.

Predistorting in this fashion provides advantages by avoiding extra complexity in the transmitter.

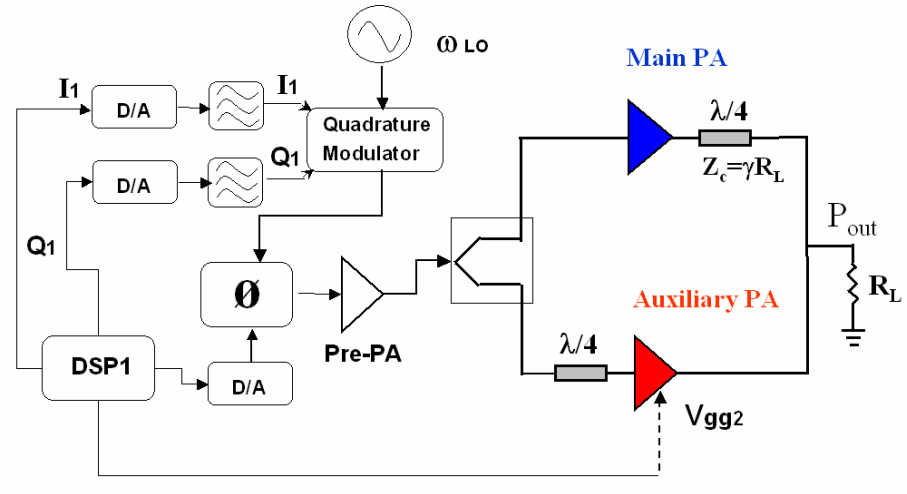


Figure 3.24: Doherty architecture with analog phase shifter based control only

Baseband signal is generated in the form of I & Q, and then up-converted to RF. After being amplified by a pre-amplifier, the signal is split by a 1:2 ratio Wilkinson power divider into the main and auxiliary amplifier paths. DSP generates another voltage signal, which is applied to the BST phase shifter to control the phase behavior of the RF signal. With the relatively flat gain characteristic obtained, gain control through V_{gg2} at the gate of the auxiliary PA was not carried out in this work. DSP was only used to correct the non-flat phase of the amplifier.

3.4.3 Phase Shifter

The analog phase shifter was implemented using voltage-controllable BST-based capacitors in a lumped LC transmission line. A packaged BST-based phase

shifter is shown in Fig. 3.25. This BST-based phase shifter is donated by Agile Materials and Technologies.

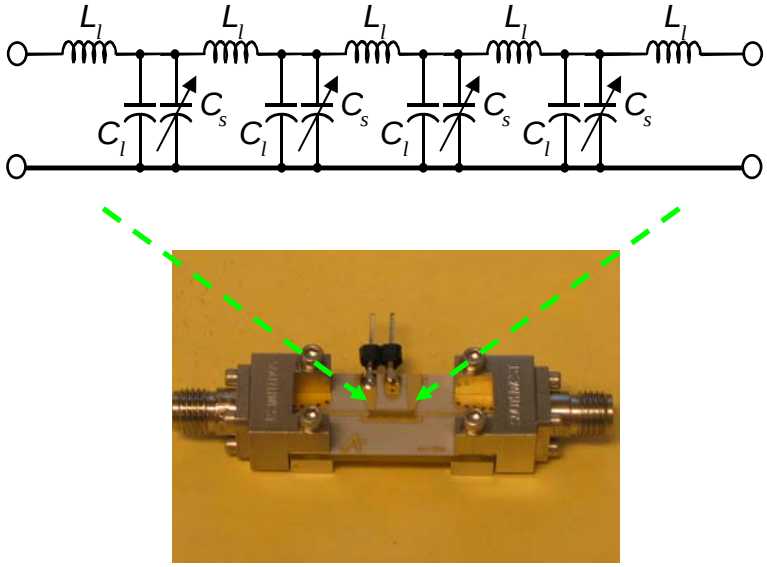


Figure 3.25: A packaged phase shifter based on BST material (Courtesy of Agile Technology, Inc)

3.4.4 Measurement Results

To verify the efficacy of the described phase predistortion, the performance of the Doherty power amplifier was measured in terms of power added efficiency, gain and ACPR. Shown in Fig. 3.26 is the measured PAE and Gain vs. output power of the Doherty amplifier with a CDMA IS-95 test signal prior to phase correction. High PAE (>40%) is obtained over an approximately 6dB wide region. Compared with the single-tone test in Fig. 3.23, the PAE and gain here are both rounded, which is due to the fact that the measured output power is the average power of the CDMA signal. It is estimated that, when averaged over the possibility distribution for output power usage in a CDMA system, the overall efficiency of this amplifier is higher by more than 2.5

times than that of a class AB amplifier. The gain and efficiency curves in power are not expected to change from applying phase correction.

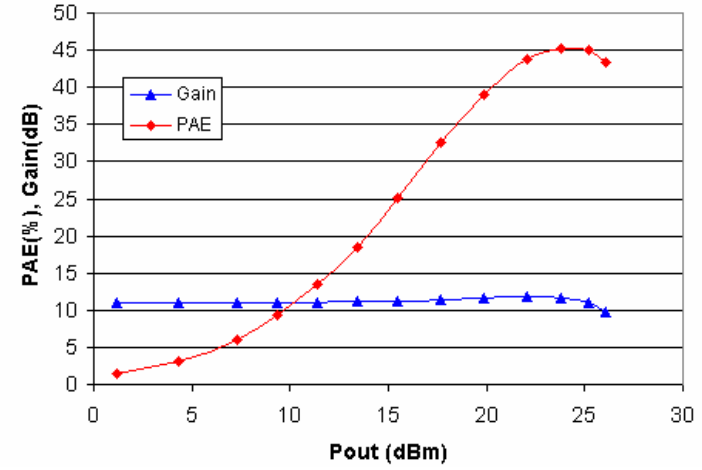


Figure 3.26: Measured Gain and PAE of the Doherty PA tested with IS-95 signal

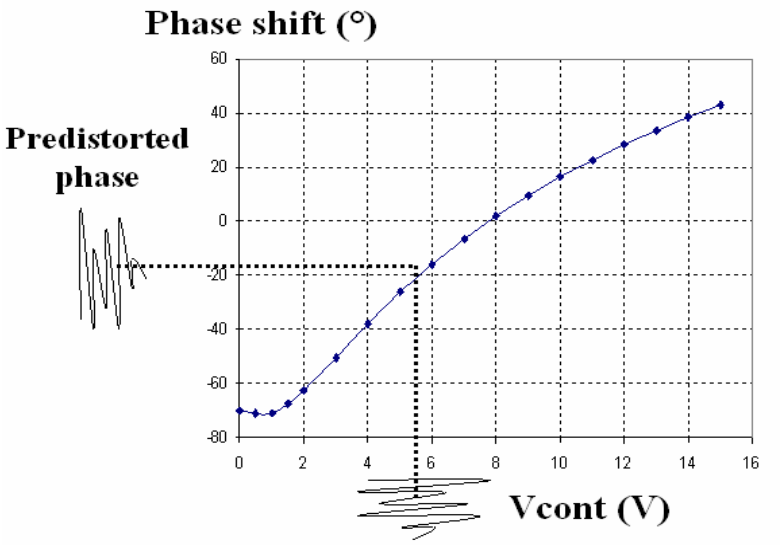


Figure 3.27: Phase vs. Vcont at 840MHz of the BST phase shifter

Phase data from Fig. 3.23 was analyzed to develop the phase predistortion strategy. The same phase characteristics of the amplifier vs. output power prior to predistortion are used to get a "mirror image" of this data, which is the desired phase

predistortion curve to obtain flat phase (similar to Fig. 3.9). From these curves, together with the calibration curve of the phase shifter (Fig. 3.27), a signal-dependent control voltage was derived, and generated (via PC and suitable DAC) during the amplification of an IS-95 CDMA signal.

Shown in Fig. 3.28 is the measured ACPR with IS-95 signal vs. output power of the Doherty amplifier before and after the analog phase predistortion. The largest improvement of ACPR achieved by this phase predistortion is 5.2 dB at 22dBm output power, which is particularly significant because it allows the amplifier to meet the linearity specifications of –42dBc ACPR for the IS-95 standard. It is expected that further improvement will be possible by combining gain predistortion (obtained by dynamically biasing the gate of the peaking amplifier) along with the phase correction. Representative frequency spectra corresponding to the output with and without phase predistortion are shown in Fig. 3.29. The "uncorrected" is the spectrum before the phase predistortion and the "corrected" is the spectrum after the phase predistortion.

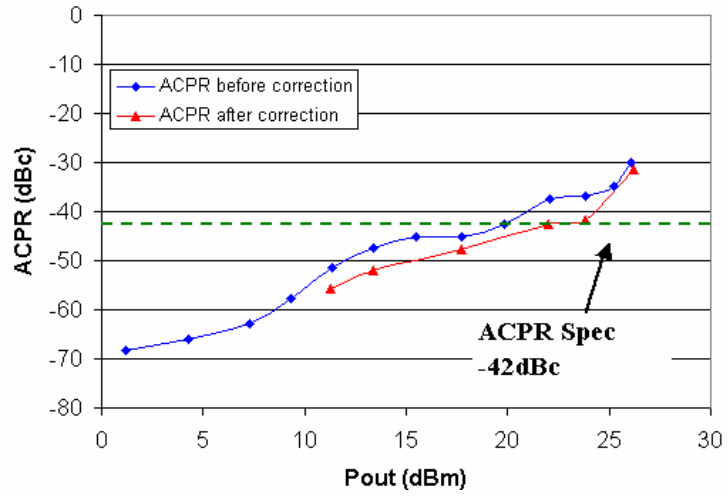


Figure 3.28: Measured ACPR of the Doherty PA before and after correction tested with IS-95 signal

It should be noted that the DSP system used here is the same as the one used for system described in Fig. 3.3. The system components such as DACs and filters have a bandwidth of 50MHz which is not only enough for passing CDMA signal but also for transmitting digitally predistorted signal without frequency domain distortion. The resolution of DACs is 12 bits, also much higher than needed. These will not allow us to evaluate the possibility of performance degradation caused by insufficient bandwidth or resolution for digital predistortion in a practical handset system.

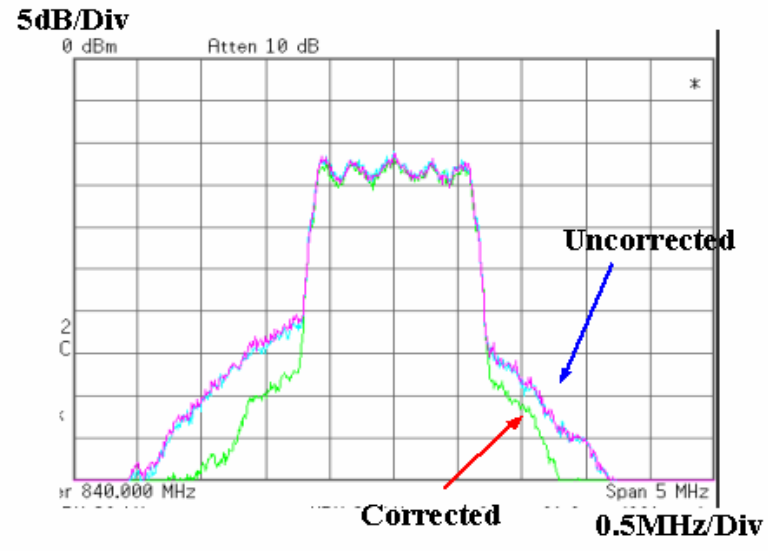


Figure 3.29: Spectrum comparison between the Doherty PA without and with phase predistortion

Overall, when tested with an IS-95 signal, a higher than 40% PAE was achieved for this Doherty amplifier. DSP techniques were applied to the Doherty amplifier in CDMA operation to improve both the linearity and efficiency. AM-PM distortion was corrected by using DSP to adjust the phase of the signal at the RF frequency through a BST material based analog phase shifter. ACPR was improved as

much as 5.2dB to meet the CDMA specification by this means. This demonstrates the efficacy of the analog phase shifter based linearization scheme, which is advantageous in achieving similar performance while requiring less system complexity relative to a digital baseband predistortion scheme.

3.5 Summary

In this chapter, characteristics of the Doherty amplifier, which was designed in chapter 2, were further analyzed. It was shown that power dependent adjustment of the gate bias voltage (V_{gg2}) of the auxiliary amplifier can help to achieve better linearity for the Doherty amplifier while maintaining its high efficiency performance. DSP control was introduced to implement the V_{gg2} control on the auxiliary amplifier at the rate of the input CDMA signal envelope. DSP was also used to apply digital predistortion to correct phase distortion in the Doherty amplifier. With a careful DSP control strategy, the measured linearity performance of the Doherty amplifier was improved significantly to meet the -42 dBc ACPR specification with an IS-95 input signal. High PAE performance of the original Doherty amplifier is maintained and even improved slightly. Extension of that, an analog based predistortion strategy was introduced and shown in simulation to achieve comparable performance while only requiring a narrower bandwidth than the traditional baseband digital predistortion scheme. Experimental results of an analog based predistortion method using a DSP controlled BST phase shifter demonstrate the efficacy of this analog based predistortion scheme.

3.6 Acknowledgements

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Some of the material in chapter 3 is as it appears in "Doherty Amplifier with DSP Control to Improve Performance in CDMA Operation," Y. Zhao, M. Iwamoto, L. E. Larson, P. M. Asbeck, *IEEE International Microwave Symposium Digest*, vol.2, pp.687-690, June 2003. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.

3.7 References

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Chapter 4
Linearity Analysis of Doherty Amplifier

4.1 Motivation

In chapter 3, Doherty amplifiers have been demonstrated to be able to achieve extended high efficiency and high linearity at the same time with help of a DSP linearization technique. However, it is still difficult to obtain optimum efficiency and high linearity performance in the Doherty amplifier without DSP. In order to do a better design tradeoff between efficiency and the linearity based on circuit itself, it is critical to achieve a better understanding of the nonlinear behavior of the Doherty amplifier. Many previous publications on Doherty amplifiers described that non-ideal interactions between the main and the auxiliary amplifier in Doherty can cause undesired high distortions, however, none of them analyzed this distortion in detail. Although people knew it is the key to understand Doherty amplifier's linearity behavior, there was no effective method to achieve the target. Volterra series is a useful tool in analyzing nonlinear amplifiers with rather simple structure, for example, a single ended amplifier [1]. For the case of Doherty amplifier, in which two nonlinear amplifiers interact with each other, it is very challenging to manage very lengthy Volterra series calculations to get meaningful insights.

4.2 Introduction to the Simple Analytical Model

A simple way to analyze the Doherty amplifier is needed. In fact, a paper published by H.Yamada and his colleagues has suggests a possible solution [2]. In that paper, a simplified amplifier model has nonlinear components that were functions of operating power level, and contain nonlinearities of all orders. From the simple model, analytical equations were developed to describe phase distortion of the nonlinear amplifier. From the analysis, contribution of individual nonlinear components and their interactions to the phase distortion of the amplifier can be readily understood and insights for better amplifier design can be achieved. In H.Yamada's paper, the simple analytical method was used to understand phase distortion behavior of a handset amplifier used in PHS application. Compared with Doherty amplifier, it is a simple single-ended structure without load impedance change. However, from discussions in this chapter, one can see that similar ideas can be applied effectively to Doherty amplifiers.

In this chapter, a simple analytical model is proposed [3]. The analytical model is based on linear and nonlinear components extracted from a Vertical Bipolar Inter Company model (VBIC) for Skyworks InGaP/GaAs HBT devices. Equations derived from the model provide insights into effects of individual components on the gain and phase of both the single-ended and the Doherty amplifiers. Before the model being applied to a Doherty amplifier, it is first applied to analyze single-ended amplifiers. It is shown to be effective in predicting the nonlinear behavior of both a Class AB and a

Class C biased amplifier, which are the two active building blocks for a Doherty amplifier. Following that, the model is also shown to be predicting output gain and phase of a Doherty amplifier well. In a later part of this chapter, further results from the model analysis indicate that tuning the phase delay inserted in front of the auxiliary PA within the Doherty can improve linearity at high input power. The efficacy of the model is demonstrated by experimental results, in which for a Doherty PA with a tuned phase delay at the auxiliary PA side, the measured gain and phase agree with the simulation results. Furthermore, the IMD3 performance is improved as much as 8 dB when compared with a Doherty PA without phase delay tuning.

This chapter is organized as follows. In 4.3, the analytical model for single ended Class AB and Class C amplifiers is discussed. Then in 4.4, the extracted nonlinear components from both of these amplifiers are used to build an analytical mode for a Doherty amplifier. In 4.4.1, the analytical model results are discussed for Doherty amplifiers with different configurations. Section 4.4.2 describes the load dependence of the extracted components and its impact on the modeling. Next, experimental results are given in 4.5. Finally, a summary is provided in 4.6.

4.3 The Model for Single-Ended Amplifiers

To develop insights into the nonlinear behavior of Doherty amplifiers, a simple physically-based nonlinear analytical model for GaAs HBTs is developed here and applied to single-ended amplifiers and later to Doherty amplifier designed for handset applications. Unlike nonlinear analyses using Volterra Series, the nonlinear

components in this model are functions of operating power level, and contain nonlinearities of all orders. A representative schematic of the model is shown in Fig. 4.1.

The nonlinear components in the proposed model of Fig. 4.1 are: base-emitter junction capacitance C_{be}, and conductance g_{be}; output capacitance C_{ce} and conductance g_{ce}; and trans-conductance g_m. For convenience, in later references, C_{be} and g_{be} will be collectively expressed as Y_{ce}, and C_{be} together with g_{be} as Y_{ce} . For simplicity, C_{bc} effects are incorporated within the input and output admittances. The remaining components (base resistance R_b and emitter resistance R_e) are considered to be linear. The linear and nonlinear components are extracted from a VBIC model for Skyworks InGaP/GaAs HBT devices. A schematic of the HBT device is also shown in Fig. 4.1. The detail of the extraction for nonlinear components will be discussed in section 4.3.1.

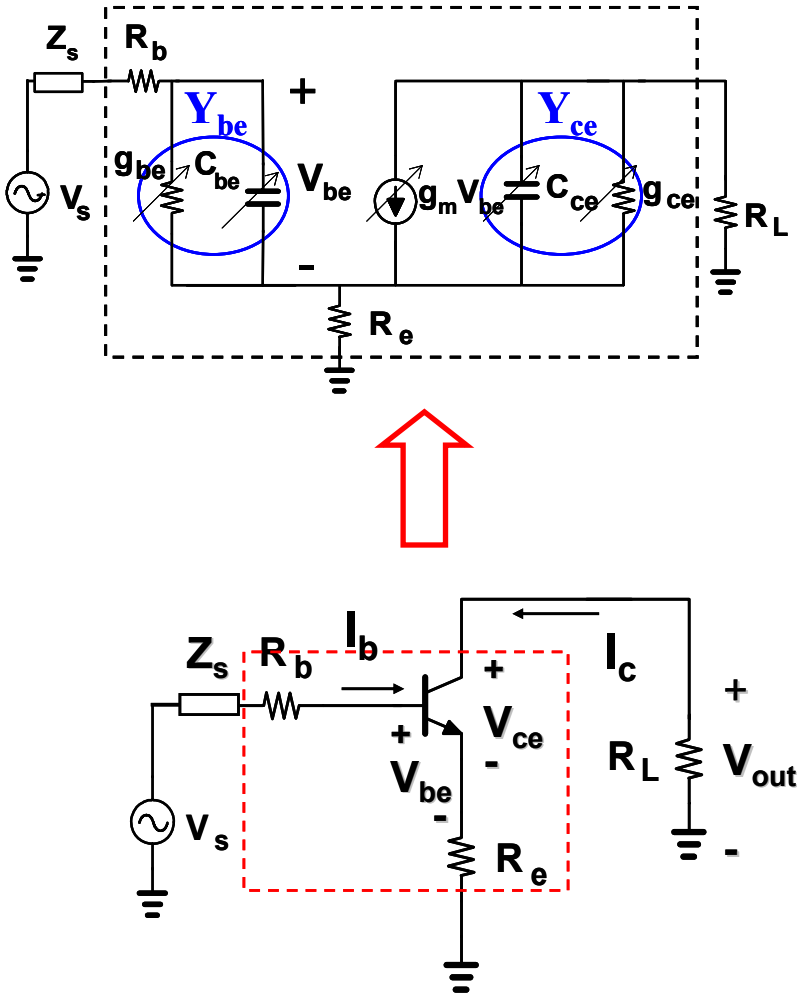


Figure 4.1: Schematic of proposed HBT amplifier model

The key advantage of the model is simplicity. With the simplicity of the model, closed form explicit expressions for the complex transfer function of the PA circuits can be derived, and insights of how the gain and phase are shaped by individual nonlinear and linear components can be achieved. In fact, solving Kirchoff's Current and Voltage Law for the circuit shown in Fig. 4.1 gives the complex voltage transfer function in the model as follows:

$$\frac{V_{out}}{V_s} = R_L \frac{a}{bc - aR_e} \tag{4-1}$$

$$a = R_e - g_m/(Y_{be}Y_{ce});\ b = R_b' + 1/Y_{be} + R_e$$

$$c = R_e + R_L + 1/Y_{ce};\ R_b' = R_b + Z_s$$

$$Y_{ce} = j\omega C_{ce} + g_{ce};\ Y_{be} = j\omega C_{be} + g_{be}$$

If R_e is small and can be neglected, then the analytical model can be simplified and equation (4-1) becomes:

$$\frac{V_{out}}{V_s} \approx -R_L \frac{g_m}{(1 + R_b' Y_{be})(1 + R_L Y_{ce})} \tag{4-2}$$

In the following, how the model components, especially the nonlinear components, are extracted will be discussed in detail. Then the model components can be placed into the equation (4-1) or (4-2) to calculate the gain of the amplifiers.

4.3.1 Model Parameter Extractions

The nonlinear components are dependent on the bias conditions of the transistor, on the input power and, in general, on the circuit embedding. The transistor used for this evaluation was an InGaP/GaAs HBT from Skyworks Solutions high-volume manufacturing process in Newbury Park, CA. The technology features a DC gain (β) of 115, f_T=31 GHz (at V_{ce}=1.5, J_c=0.1 mA/μm^2), and a BVCEO of about 15 Volts. In this work, the linear and nonlinear components values were extracted from a foundry-provided VBIC device model using ADS in harmonic balance simulation.

For the extraction of the nonlinear elements, appropriate ratios of current and

voltage components at the fundamental frequency were calculated under large signal conditions. The nonlinear elements are defined through the following:

$$I_b^{(1)} = Y_{be} V_{be}^{(1)}$$

$$I_c^{(1)} = g_m V_{be}^{(1)} + Y_{ce} V_{ce}^{(1)} \qquad (4\text{-}3)$$

Here the superscript $^{(1)}$ indicates that the fundamental frequency component of the time waveform should be used. With three unknowns (g_m, Y_{be}, Y_{ce}) in two equations, an extra input is needed. In fact, Y_{ce} value is provided by an extra step.

The actual extraction process in ADS simulation are: First, a large signal S-parameter simulation is carried out, from which $Z_{ce}=1/Y_{ce}$ can be calculated as $Z_0 \cdot (1+S_{22})/(1-S_{22})$, and further elements can be determined through $\omega C_{ce}=\text{imag}(Y_{ce})$, $g_{ce}=\text{real}(Y_{ce})$; Second, a harmonic balance simulation is done. From its results, the remaining nonlinear components for the analytical model can be calculated, following $Y_{be}=\text{imag}(I_b^{(1)}/V_{be}^{(1)})$, $\omega C_{be}=\text{imag}(Y_{be})$, $g_{be}=\text{real}(Y_{be})$ and $g_m=(I_c^{(1)}-V_{ce}^{(1)}Y_{ce})/V_{be}^{(1)}$.

While the element values are valid only for a fixed circuit embedding, in this work we use them approximately over a range of power levels and circuit contexts that are different (although not very different) from those used in their definition. It is also worthwhile to point out that since the model components are only extracted at the fundamental frequency, the model will not be a complete representation such as Volterra Series for all the harmonics. Because of that, this method is only an approximation. However, we will see from later comparison with simulation results that it is a close approximation.

In the following, the analytical model will be applied to Class AB and Class C

amplifiers, which are the two basic active components in the Doherty amplifier.

4.3.2 Model for a Class AB Amplifier

The Class AB amplifier uses a Skyworks HBT device with active emitter area of 1600 um^2. From the VBIC model, R_b is found to be 0.336 Ω and $R_e$is 0.0372 Ω. A simulation was set up in Agilent ADS for the model parameter extractions. The base quiescent bias current of 53 mA is provided by a current mirror bias circuit. A source impedance Z_s=2.24+0.8j Ω is used to achieve proper input matching. The load impedance is Z_0=16 Ω, which is the value the Class AB main amplifier sees within the Doherty amplifier before the auxiliary amplifier turns on. The nonlinear components for the Class AB biased amplifier are extracted following the procedure discussed in 4.3.1. First, from a large signal S-parameter simulation, $Z_{ce}=1/Y_{ce}$ is calculated as $Z_0 \cdot (1+S_{22})/(1-S_{22})$, and $\omega C_{ce}=\text{imag}(Y_{ce})$, $g_{ce}=\text{real}(Y_{ce})$. Second, a harmonic balance simulation is done to give $Y_{be}=\text{imag}(I_b^{(1)}/V_{be}^{(1)})$, $\omega C_{be}=\text{imag}(Y_{be})$, $g_{be}=\text{real}(Y_{be})$ and $g_m=(I_c^{(1)}-V_{ce}^{(1)}Y_{ce})/V_{be}^{(1)}$. The extracted magnitudes of g_m, Y_{be} and Y_{ce} are shown in Fig. 4.2 (a). The extracted ωC_{be}, g_{be}, ωC_{ce} and g_{ce} values are shown in Fig. 4.2 (b).

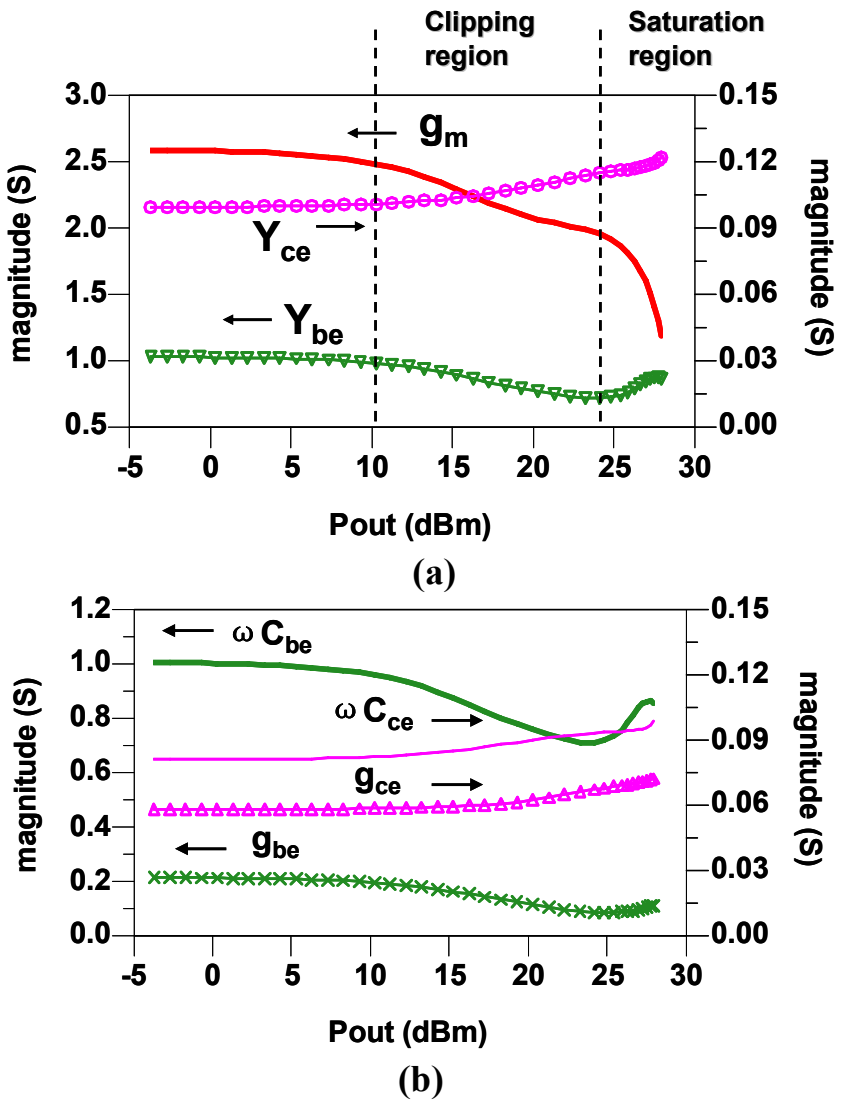


Figure 4.2: Extracted components for a Class AB: (a) magnitude of gm, Ybe and Yce; (b) ωCbe , gbe , ωCce and gce

With increasing power level, g_m is found to decrease slowly with RF power as a result of clipping of the current waveform in cutoff, and to drop rapidly above 25 dBm as a result of the onset of saturation at the minimum of the voltage waveform. Similarly, C_{be} decreases with increasing power level (as does Y_{be}) as a result of clipping, but increases as saturation is reached. $Z_{ce}=(1/Y_{ce})$ has a complex value of 10 ohms/-55° at low power, and changes slightly with power level. It is worthwhile to

point out that C_{be} variation over the power levels is a major reason why output phase of the amplifier varies over the power levels. This will be reflected in Fig 4.3.

The emitter resistance R_e of 0.0372 Ω is negligible in this case and equation (4-2) can be used for the analysis. The calculated output gain and phase according to (4-2) are shown in Fig 4.3, and for comparison, the simulated gain and phase from ADS using the complete Skyworks device model. Good agreement between the two is found.

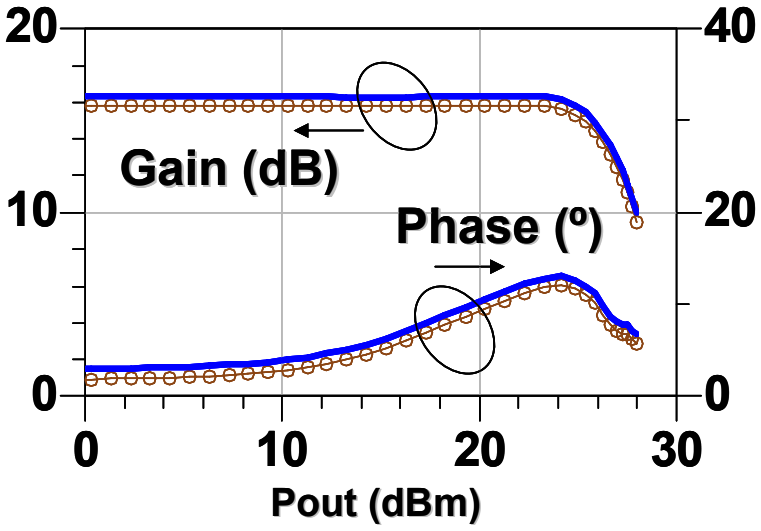


Figure 4.3: Results from the analytical model for a Class AB PA: gain and phase from simulation (solid) and the analytical model (triangle)

The analytical model can be used to achieve insights into the amplifier's nonlinear behavior. Fig. 4.4 shows the magnitudes of the g_m, $d_{in}=1/(1+R_b'Y_{be})$, $d_{out}=1/(1+R_LY_{ce})$ and the calculated voltage gain on a linear scale. As indicated by the subscripts, d_{in} is the contribution to gain by components from the circuit input side and d_{out} by components from the output side. Rb'= Rb+Zs affects d_{in} and consequently the complex voltage gain, which implies that source impedance can be optimized for

linearity as reported by H.Yamada in [2]. Moreover, as can be seen in Fig. 4.4, the nonlinearity of g_m is largely cancelled by that of Y_{be} (within the d_{in} factor) in the clipping region, leading to nearly flat gain before saturation region. This phenomenon has been originally reported in works by Maas [4], Samelis [5] and others.

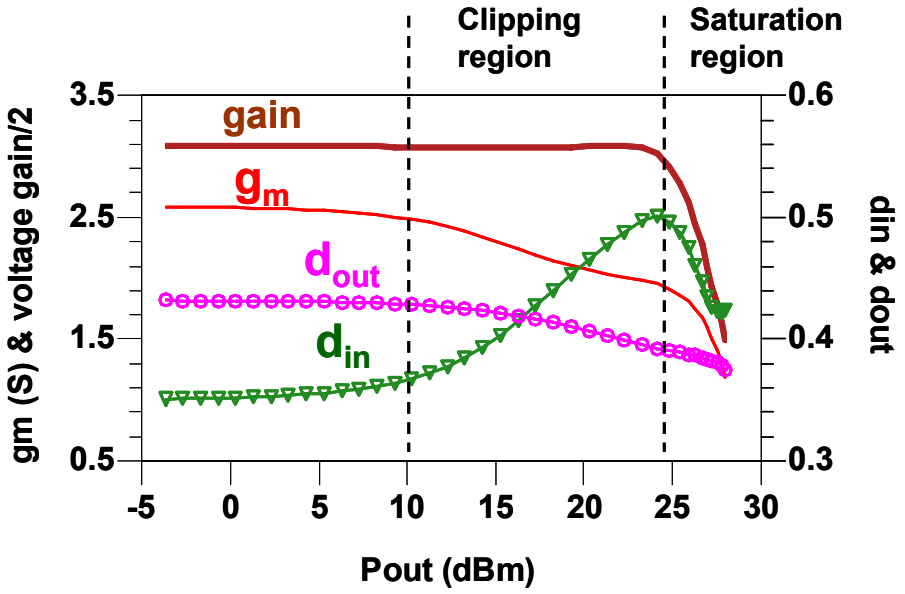


Figure 4.4: Results from the analytical model for a Class AB: voltage gain(solid), gm(dot), din(triangle) and dout(circle)

4.3.3 Model for a Class C Amplifier

The Class C biased amplifier uses the same device as the Class AB amplifier described above. The same current mirror circuit (with different reference voltage) is used to provide a quiescent current of 1 mA. The same simulation set up as for the Class AB amplifier is also used for the Class C case. A load impedance of Z_0= 4 Ω was used, which is the value a Class C auxiliary amplifier sees in the Doherty context. The magnitude of extracted g_m, Y_{be} and Y_{ce} are shown in Fig. 4.5(a), while the

extracted ωC_{be}, g_{be}, ωC_{ce} and g_{ce} values are shown in Fig. 4.5(b). The values differ considerably from those found for Class AB operation.

In Fig. 4.5(a), g_m increases sharply with power as a result of Class C self-bias effect, and reaches saturation at about 30dBm. The input capacitance also increases significantly with power (as does Y_{be}). The output capacitance increases dramatically at peak power levels (as does Y_{ce}), when the base-collector junction reaches saturation at the extremes of the voltage waveform. It should be pointed out that this analytical model incorporates Cbc into Cbe and Cbc. Effect of Cbc change contributes to large ωCbe and ωCce changes at high power levels as shown in Fig. 4.5(b). Compared with the admittance, the conductance of g_{be} and g_{ce} are both small in the Class C amplifier.

The calculated output gain and phase according to equation (4-2) is shown in Fig. 4.6, and for comparison, the simulated gain and phase from ADS using the complete Skyworks device model. Good agreement between the two is found.

Based on (4-2), the magnitudes of g_m, $d_{in}=1/(1+R_b'Y_{be})$, $d_{out}=1/(1+R_L Y_{ce})$ and the calculated voltage gain in linear scale for the case of the Class C biased amplifier are shown in Fig. 4.7. For comparison with g_m, the voltage gain has been divided by a factor of 4.2 Ω, which is the small signal value of the product of $R_L/(d_{in}d_{out})$. The sharply increasing g_m dominates the gain in most power levels and the increase of Y_{be} (within the factor d_{in}) leads to a minor gain compression at high power.

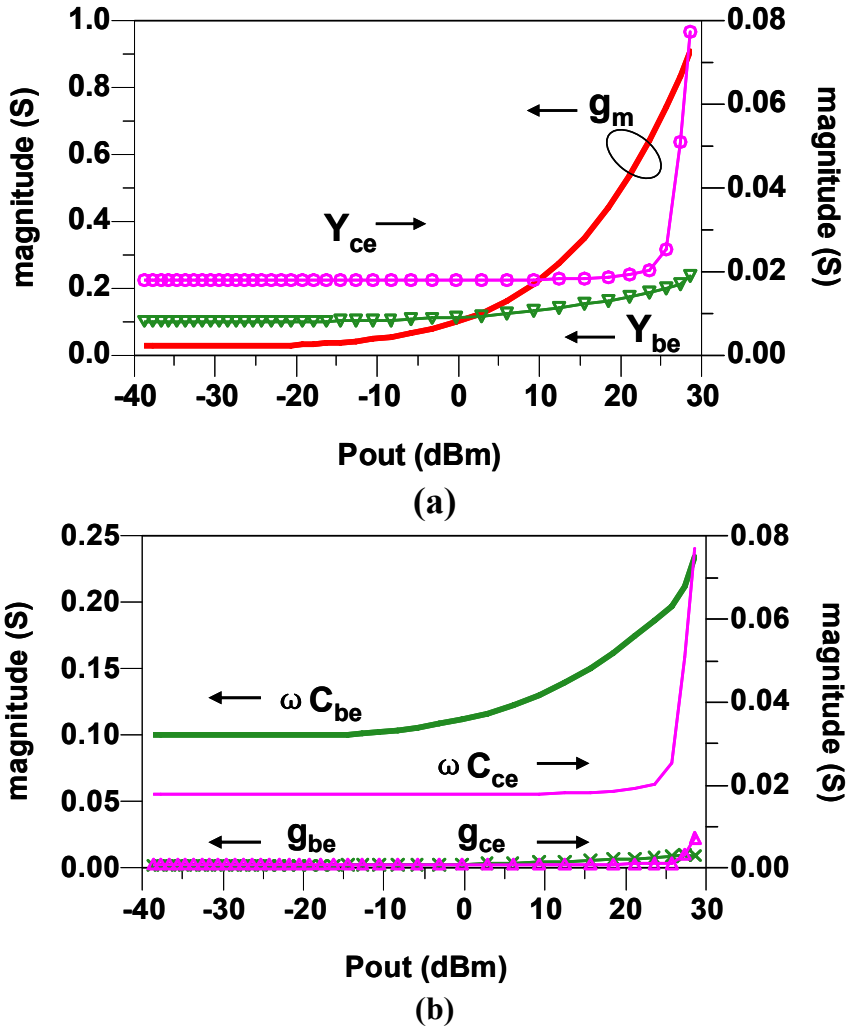


Figure 4.5: Extracted components for a Class C PA: (a) magnitude of gm, Ybe and Yce; (b) ωCbe , gbe , ωCce and gce

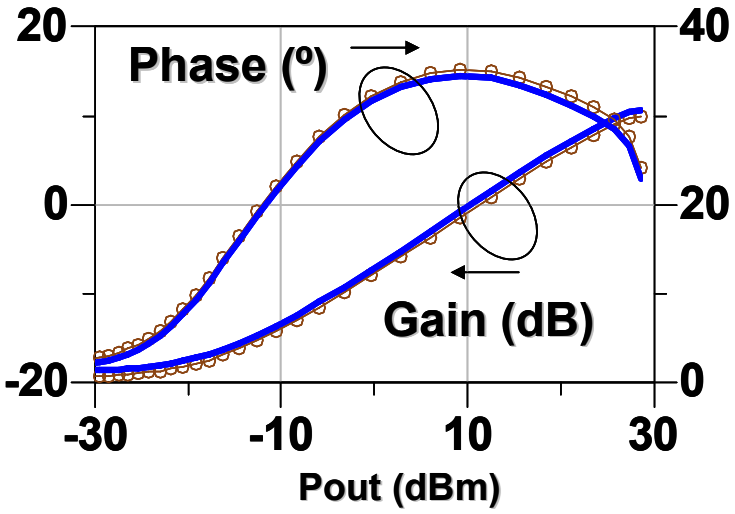


Figure 4.6: Results from the analytical model for a Class C PA: gain and phase from simulation (solid) and the analytical model (triangle)

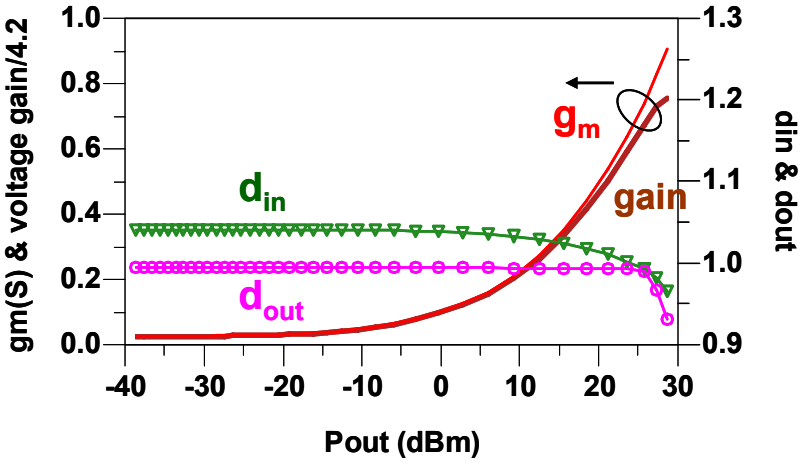


Figure 4.7: Results from the analytical model for a Class C PA: voltage gain(solid), gm(dot), din(triangle) and dout(circle)

It should be pointed out that since g_m is extracted as $g_m=(I_c-V_{ce}Y_{ce})/V_{be}$ for both Class AB and Class C amplifiers, it is not constrained to be real. For the present amplifiers, g_m has a small imaginary part, which is necessary to include in the modeling to give accurate phase predictions for the amplifiers.

4.4 The Analytical Model for a Doherty Amplifier

The analytical model for separate Class AB and Class C amplifiers forms the foundation for Doherty amplifier. Because the circuits used for extracting nonlinear and linear components in Class AB and Class C amplifiers are configured the same as they appear in the Doherty amplifier, the extracted parameters from the two separate amplifiers can be used approximately to analyze the full Doherty amplifier. In both the separate and Doherty cases, the Class AB and Class C amplifiers have the same input matching, bias condition, output impedance and also the same input power level, respectively.

With that, the analytical model for a Doherty amplifier using identical transistors can be structured by adding the individual models for the Class AB and the Class C amplifiers together. The schematic of the model for Doherty amplifier is shown in Fig. 4.8. There is an $e^{-j\theta}$ factor applied to the source of the auxiliary PA which stands for the delay line inserted in front of the auxiliary PA in a typical Doherty structure. The nominal value for θ is 90º. The derivation of the output voltage expression for the Doherty is more complicated than for the single-ended PA, however, it is still analytically tractable.

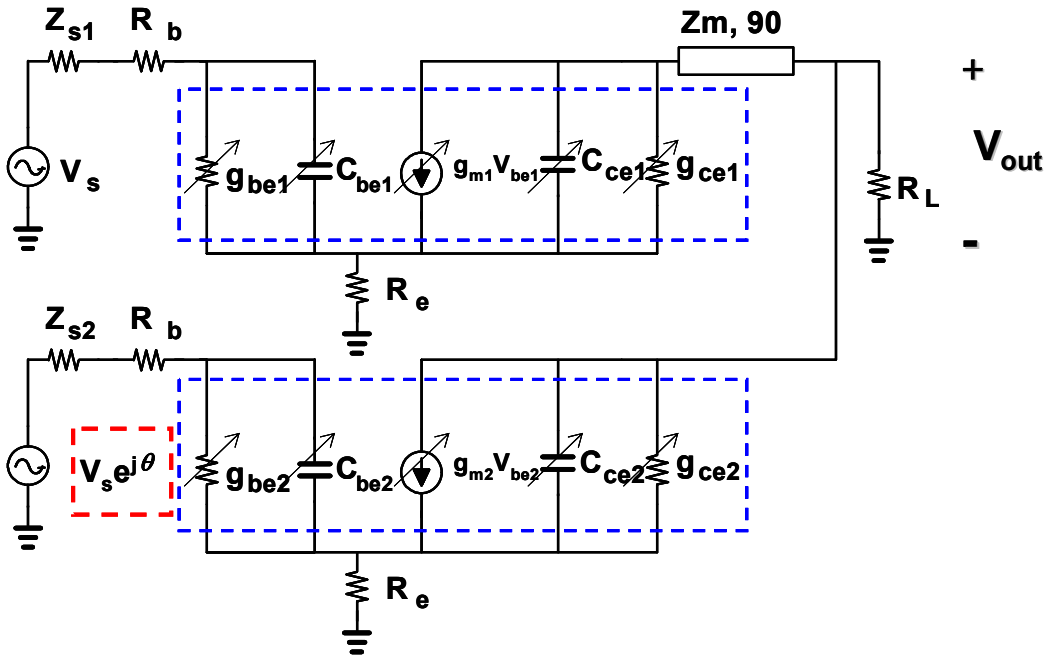


Figure 4.8: Schematic of the proposed model applied to Doherty architecture

From the voltage and current relations in the Doherty schematic, we have:

$$\frac{V_{out}}{V_s} = -jZ_m \frac{A_1B_2 + jZ_mC_1A_2}{B_1B_2 + Z_m^2C_1(C_2 + B_2/R_L)} \tag{4-4}$$

$$A_1 = R_{e1} - g_{m1}/(Y_{be1}Y_{ce1}); \quad A_2 = e^{-j\theta}(R_{e2} - g_{m2}/(Y_{be2}Y_{ce2}))$$

$$B_{1,2} = (C_{1,2} + g_{m1,2}R_{e1,2}/Y_{be1,2})/Y_{ce1,2} + (R_b'_{1,2} + 1/Y_{be1,2})R_{e1,2}$$

$$C_{1,2} = R_b'_{1,2} + 1/Y_{be1,2} + R_{e1,2}$$

The model elements extracted for the Class AB and Class C cases are used in the Doherty amplifier for the main and auxiliary amplifiers, respectively. Subscripts1, 2 in the above expression indicate elements extracted from the Class AB and Class C amplifiers, respectively.

Equation (4-4) can be simplified since R_e is small and can be neglected in this case, and the expression for the transfer function becomes:

$$\frac{V_{out}}{V_s} \approx jZ_m \frac{g_{m1}/(R_{b1}'Y_{be1}+1) + e^{-j\theta} jZ_m Y_{ce1} g_{m2}/(R_{b2}'Y_{be2}+1)}{1+Z_m^2 Y_{ce1}(Y_{ce2}+1/R_L)} \quad (4\text{-}5)$$

Using equation (4-5), the gain and phase of a Doherty amplifier, with θ set equal to 90º as a nominal case, were calculated and are compared with full ADS simulation results in Fig. 4.9. Good agreement between the two cases is found. The gain differences between the two approaches are less than 1 dB over all the power levels and most importantly, the analytical results show the same trends as the simulation with changing power level. The difference of phase at peak power is about 5º, however, the analytical results show similar trends with changing power.

The analytical and simulated results show that the Doherty behavior is non-ideal, in that the gain drops at high power and phase distortion is large (more than 20º). Further analyses based on the model will provide insights into the causes of the distortion.

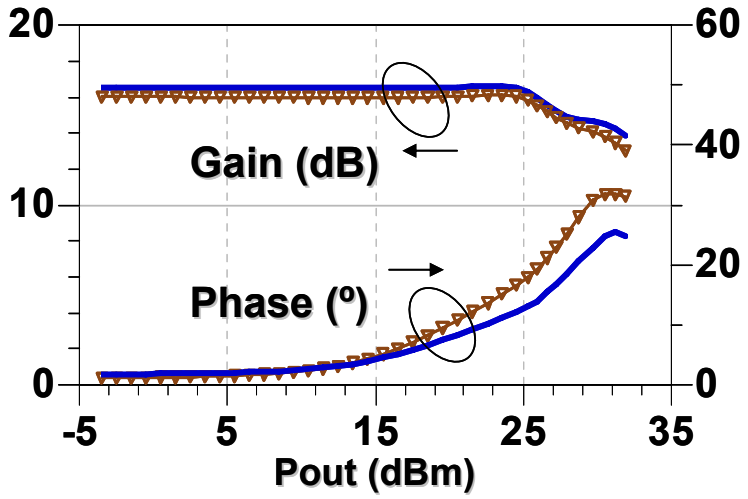


Figure 4.9: Results from the analytical model for a Doherty PA with nominal θ =90º: gain and phase from simulation (solid) and the analytical model(triangle)

4.4.1 The Model Analysis

4.4.1.1 The Model Analysis for Nominal Case with θ =90º

Let us re-examine equation (4-5) now. In equation (4-5), for the numerator, we define $N_m=g_{m1}/(R_{b1}'Y_{be1}+1)$, $N_a=e^{-j\theta}jZ_mY_{ce1}g_{m2}/(R_{b2}'Y_{be2}+1)$. For the denominator, $D=(1+Z_m^2Y_{ce1}(Y_{ce2}+1/R_L))/jZ_m$ is defined. With these definitions, the gain of the Doherty amplifier becomes $mag(N_m+N_a)/mag(D)$ and the output phase of the Doherty amplifier becomes $phase(N_m+N_a)$-$phase(D)$. N_m is the contribution to gain by the main PA, and N_a the contribution by the auxiliary PA weighted by a coefficient of $e^{-j\theta}jZ_mY_{ce1}$. D includes contributions from Y_{ce1} and Y_{ce2}.

Results of analyzing equation (4-5) by N_m, N_a and D are shown in Fig. 4.10. The Calculated overall gain and phase are shown in Fig. 4.10 (a) for comparison. Fig. 4.10 (b) and 4.10 (c) shows the magnitude and phase of N_m, N_a, N_m+N_a and D,

respectively. Their behaviors are different at different power levels. In Fig. 4.10, region I indicates low power levels before the auxiliary amplifier turns on. Region II indicates a transition region where the auxiliary PA turns on while the main amplifier remains in saturation. Region III indicates the high power region where the overall Doherty amplifier saturates. As can be seen, the main amplifier dominates the gain in region I while the auxiliary amplifier compensates the drop of gain in region II (although it does not do so completely, as seen in Fig. 4.10 (b). The contribution from Y_{ce1} and Y_{ce2} (in D) to the variation of gain is insignificant.

The output phase distortion of the Doherty amplifier comes mainly from the main PA (phase(N_m)) in region I, because the contribution from the auxiliary amplitude (N_a) is small in magnitude. At high power (regions II and III), the output phase is a result of contributions from both the main and auxiliary amplifier, combined vectorially. In region III, Y_{ce1}, Y_{ce2} provide an additional negative phase contribution.

The large output phase distortion of the Doherty may be seen to result from the phase difference of 70º between N_m and N_a. The contributions from the main and the auxiliary amplifiers to the gain of the Doherty amplifier have a phase offset which is not compensated effectively by the insertion of a quarter-wave line in front of the auxiliary amplifier. A major part of that phase offset comes from the Y_{ce1} factor in N_a, which has a 55º insertion phase (changing slightly with power) by itself. This phase offset reduces the effectiveness of the vector combination of N_m and N_a, and leads to inadequate gain compensation from the auxiliary amplifier to the main amplifier in region II.

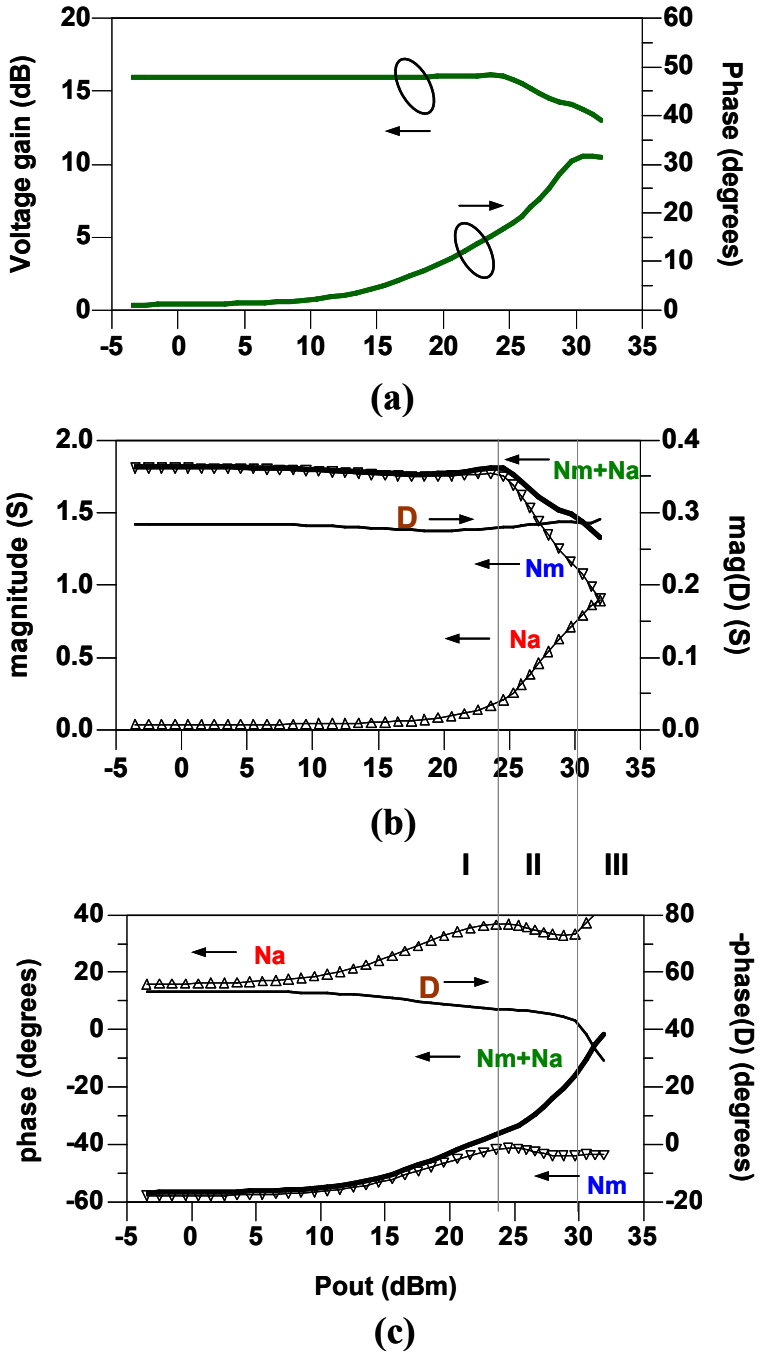


Figure 4.10: Results from the analytical model for the Doherty with θ =90°: (a) gain and phase from the analytical model (b) magnitudes of Nm, Na, Nm+Na and D (c) phases of Nm, Na, Nm+Na and D

4.4.1.2 The Model Analysis for a Case with θ =150º

The analysis implies that correcting the phase offset brought by Y_{ce1} between N_m and N_a would improve both of the gain and the phase of the Doherty amplifier. Tuning the phase delay at the input of the auxiliary PA is one way to correct that phase offset. We demonstrate here that this is an effective way to improve the behavior of the Doherty PA. Shown in Fig. 4.11 are the gain and phase results calculated with θ equal to 150º both by the analytical model and by the full ADS simulation. The analytical results match well with the simulation results. Both the gain and phase are improved, leading to a corresponding linearity improvement for the Doherty PA.

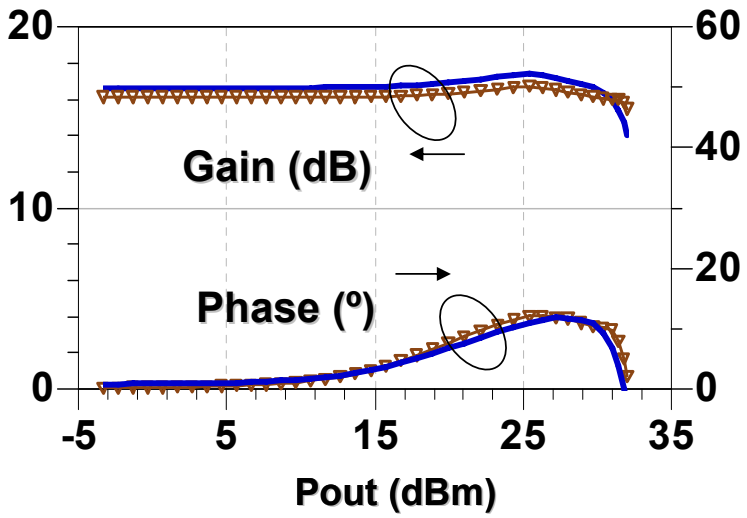


Figure 4.11: Results from the analytical model for a Doherty PA with θ =150º : gain and phase from simulation(solid) and the analytical model(triangle)

To further illustrate the effect of θ tuning to the performance, simulated gain and output phase with θ varying from 90º to 150º are given in Fig 4.12. Arrows show the direction of change as θ increases.

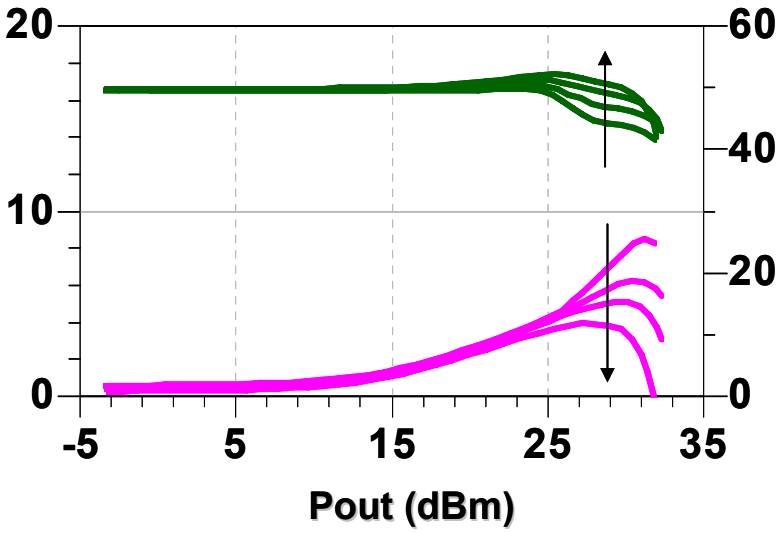


Figure 4.12: Effect of tuning the phase delay on output of Doherty amplifier

For the case of θ=150º, analysis results based on equation (4-5) are shown in Fig. 4.13 with Fig. 4.13 (a) showing the calculated overall gain and phase and Fig. 4.13 (b) and 4.13 (c) showing the magnitude and phase of N_m, N_a, N_m+ N_a and D, respectively. Because of the reduced phase offset between N_m and Na (15º), the gain contributions from the auxiliary amplifier now compensate the decrease of gain from the main PA more effectively, causing a flatter mag(N_m+ N_a) in Fig. 4.13(b) accordingly. Allowing the phase of N_a to remain 15-20º larger than that of N_m generates a positive slope for phase(N_m+ N_a) in region III, which compensates the negative phase change from D and achieves the lowest overall output phase variation for the Doherty. The value of θ that optimizes performance will in general vary with device, with bias condition, and with circuit configurations.

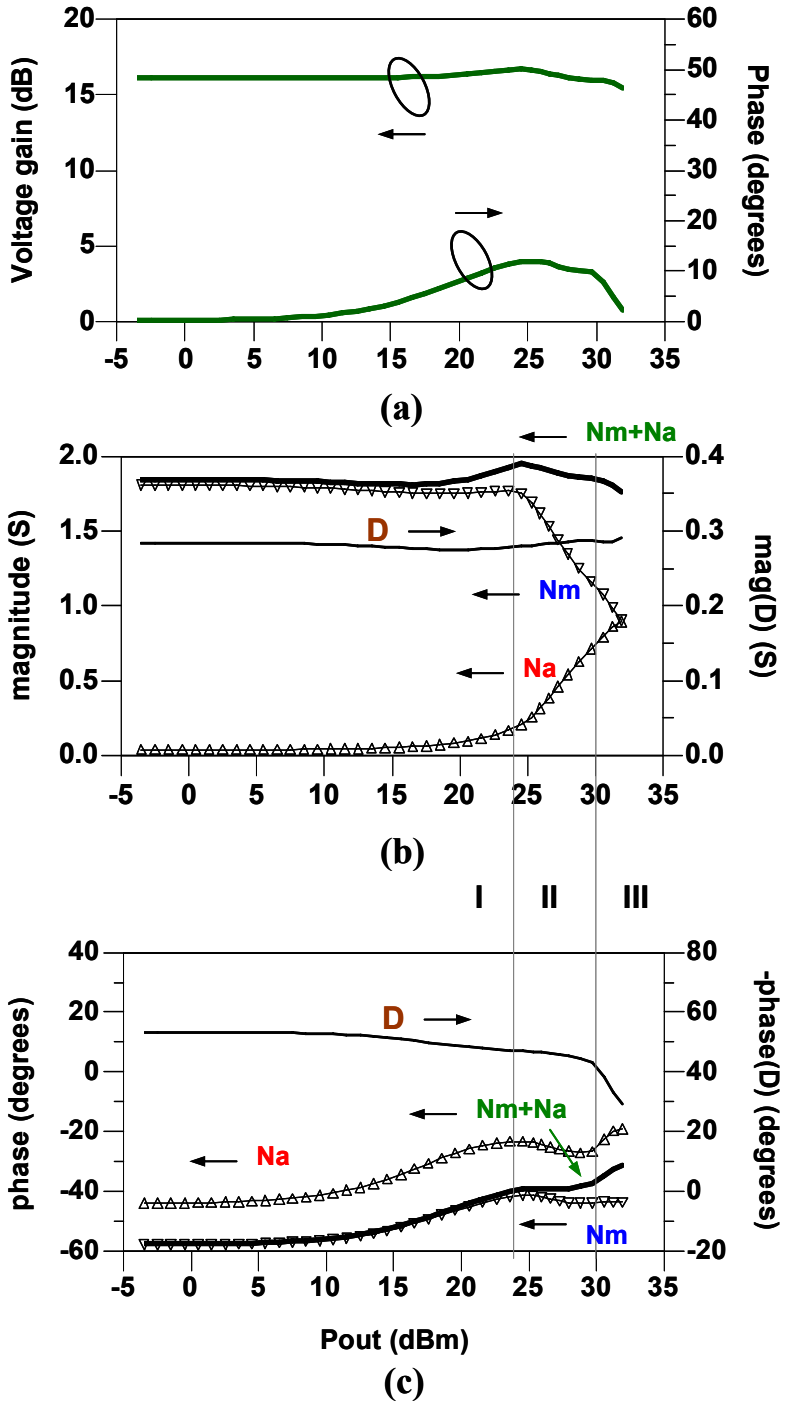


Figure 4.13: Results from the analytical model for the Doherty with θ =150º: (a) gain and phase from the analytical model (b) magnitudes of Nm, Na, Nm+Na and D (c) phases of Nm, Na, Nm+Na and D

The above analysis shows that by adding an additional phase shift in front of the auxiliary amplifier, the phase offset by Y_{ce1} in N_a is compensated and the resultant linearity performance of the Doherty PA is improved. A similar offset line had been used at output of Doherty PA as reported in reference [6],[7]. That offset line was used to compensate non-open off-state output impedance of auxiliary PA for leakage current and efficiency improvement. In this paper, the delay line is used for linearity improvement.

4.4.1.3 The Model Analysis for an Uneven Split Ratio Case

The analytical model provides a convenient way to analyze changes of Doherty behavior in the case of other changes to the amplifier structure, such as bias or device size changes in transistors and uneven input power split. For the latter case, with a power split ratio 1:2 between the main and the auxiliary amplifiers, a factor of $\sqrt{2}$ is added to the input voltage of the auxiliary amplifier, which then becomes $\sqrt{2}\cdot V_s e^{-j\theta}$.

Based on equation (4-5), the output gain and phase for this case (1:2 input power split, θ=90º) is calculated and shown in Fig. 4.14. An improved gain in region II results from the increased input power of the auxiliary amplifier. This is reflected in the increase of N_a magnitude shown in Fig. 4.14 (b). However the phase is worsened and changes by as much as 40º. This is because without correction of the phase offset between N_m and N_a, the increased magnitude of N_a aggravates its effect on the phase of (N_m+ N_a), leading to a larger phase variation of (N_m+ N_a) in region II. This analysis suggests that tuning the delay line is a better choice than changing the input

power split ratio in improving the linearity of the Doherty amplifier. Furthermore, tuning the delay line will result in optimum PAE performance, since the use of a 1:2 power split reduces the overall gain and therefore sacrifices PAE. More thorough and complete examination of the Doherty configuration with uneven power split can be found in reference [7].

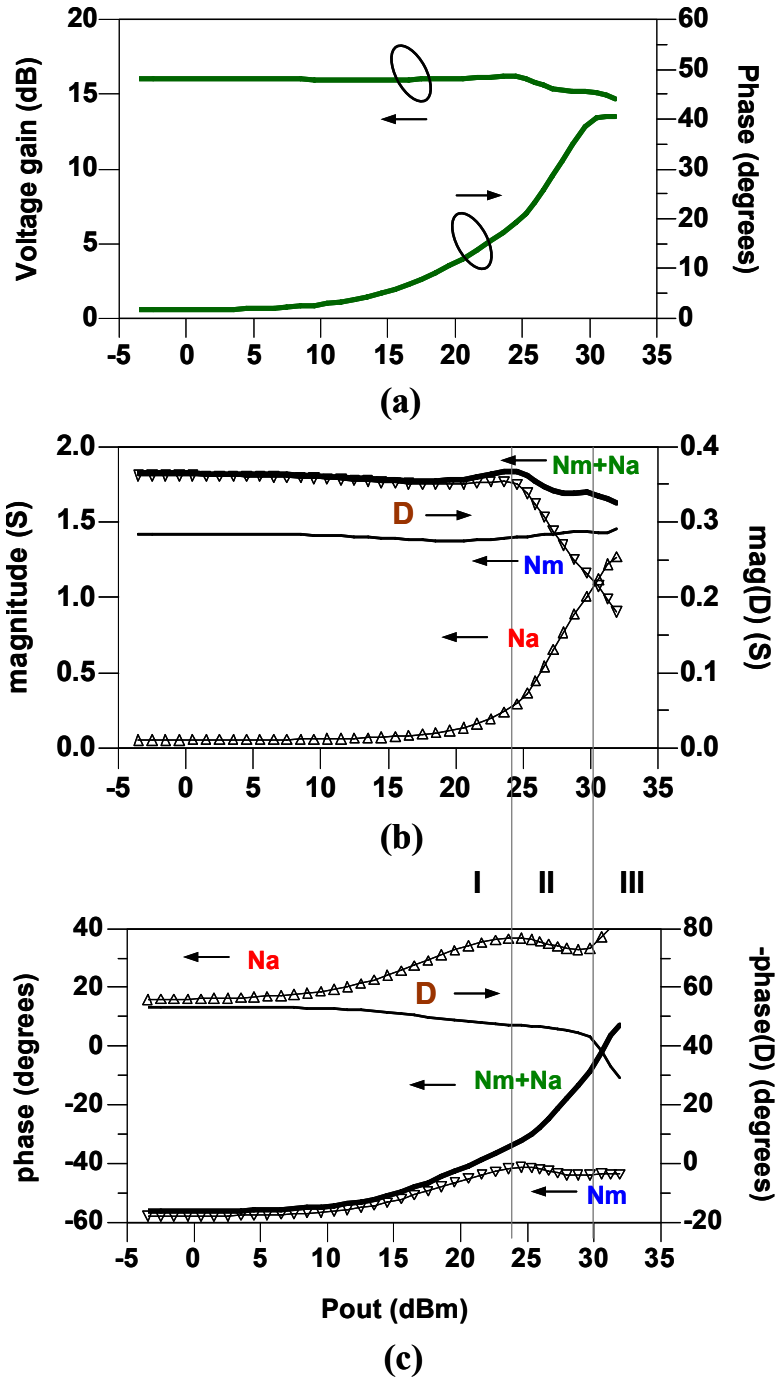


Figure 4.14: Results from the analytical model for the Doherty with 1:2 input power split ratio: (a) gain and phase from the model; (b) magnitudes of the contributing elements; (c) phases of the contributing elements

4.4.1.4 Major Nonlinear Contributions in a Doherty Amplifier

The analytical model is also useful in identifying nonlinearity contributions from each of the individual nonlinear components. The nonlinearity of each individual component can be turned off in the analytical model, by using its linear value from the small signal level for all power levels. The corresponding output gain and phase can be calculated, and subsequently IMD3 can be calculated by using the output gain and phase as inputs to a Matlab behavioral model (similar to the one used in [8]). Shown in Fig. 4.15 are the IMD3 contributions calculated using this method for different cases.

In the 'no g_{m1}+Y_{be1}' case, in which the g_{m1} and Y_{be1} are set as constants, the major nonlinearities from the main amplifier are eliminated, leading to lower IMD3 in the low power region. In the 'no g_{m2}' case, IMD3 is high in the high power region when the g_{m2} is kept at its small signal value and the auxiliary amplifier is not turned on. The 'no Y_{be1}' case has a higher IMD3 at low power indicating that Y_{be1} nonlinearity is necessary to cancel the g_{m1} nonlinearity in that power region.

The analysis suggests that the IMD3 of the full Doherty amplifier around 20dBm Pout (about -30dBc) is mainly from the nonlinearity of the main amplifier. It should be noted that there were no harmonic traps implemented in the circuit. The linearity of the main amplifier and also of the overall Doherty at low power could be further improved with proper harmonic traps at the output of the main amplifier.

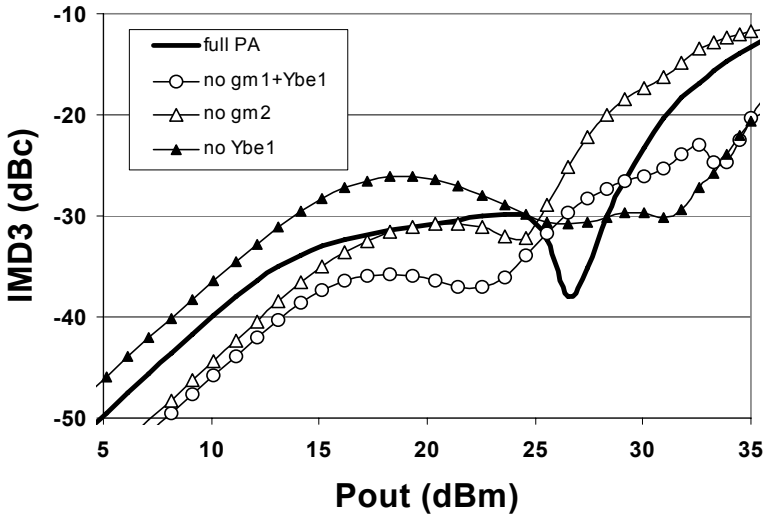


Figure 4.15: Calculated IMD3 showing effect of individual nonlinear components

4.4.2 Impedance Dependence of Model Components

One distinctive phenomenon in the Doherty amplifier is that the load impedances seen by the main and the auxiliary amplifiers change with input power level. The impedances seen by the main and auxiliary PA are defined as Z_{main} and Z_{aux} (see in Fig. 4.16), and calculated in large signal analysis by taking the ratios of the fundamental components of the overall voltage and overall current.

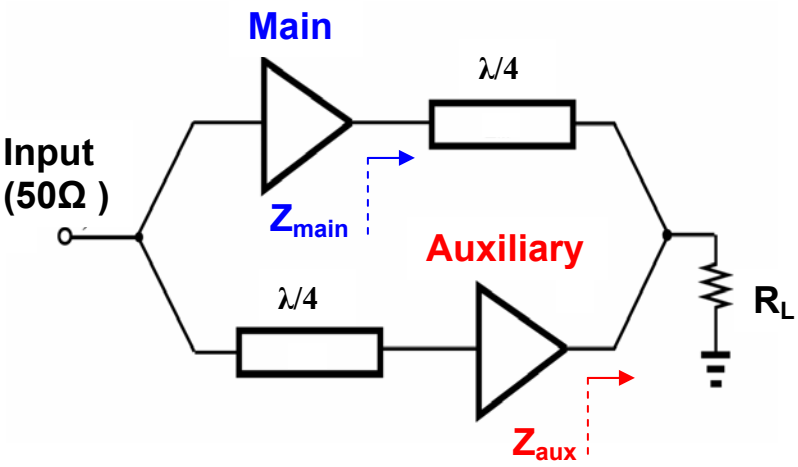


Figure 4.16: Load impedances seen by the main and auxiliary PA in a Doherty amplifier

The active load-pulling by the auxiliary amplifier on the main amplifier is a key reason why the Doherty amplifier can achieve high efficiency at low power levels. As calculated by M. Iwamoto[4], in the ideal case, the main amplifier should have a high resistance load $Z_m=\gamma^2 R_L$ (16 Ω in this design with R_L=4 Ω and γ=2) at low power, and with the auxiliary PA turning on at high power levels, that resistance value should change gradually to γR_L (8 Ω). The auxiliary amplifier experiences a $Z_{aux}=\gamma/(\gamma-1)R_L$ (8 Ω) at peak power. In the real circuit, with reactive output impedances from the transistor, Z_{main} and Z_{aux} are no longer constrained to be pure real. An example can be seen in Fig. 4.17 (a), which shows the impedances seen by the main and the auxiliary amplifiers with the improved Doherty amplifier (in which θ has been chosen to be 150º). Fig. 4.17 (b) shows the impedances in a Smith Chart.

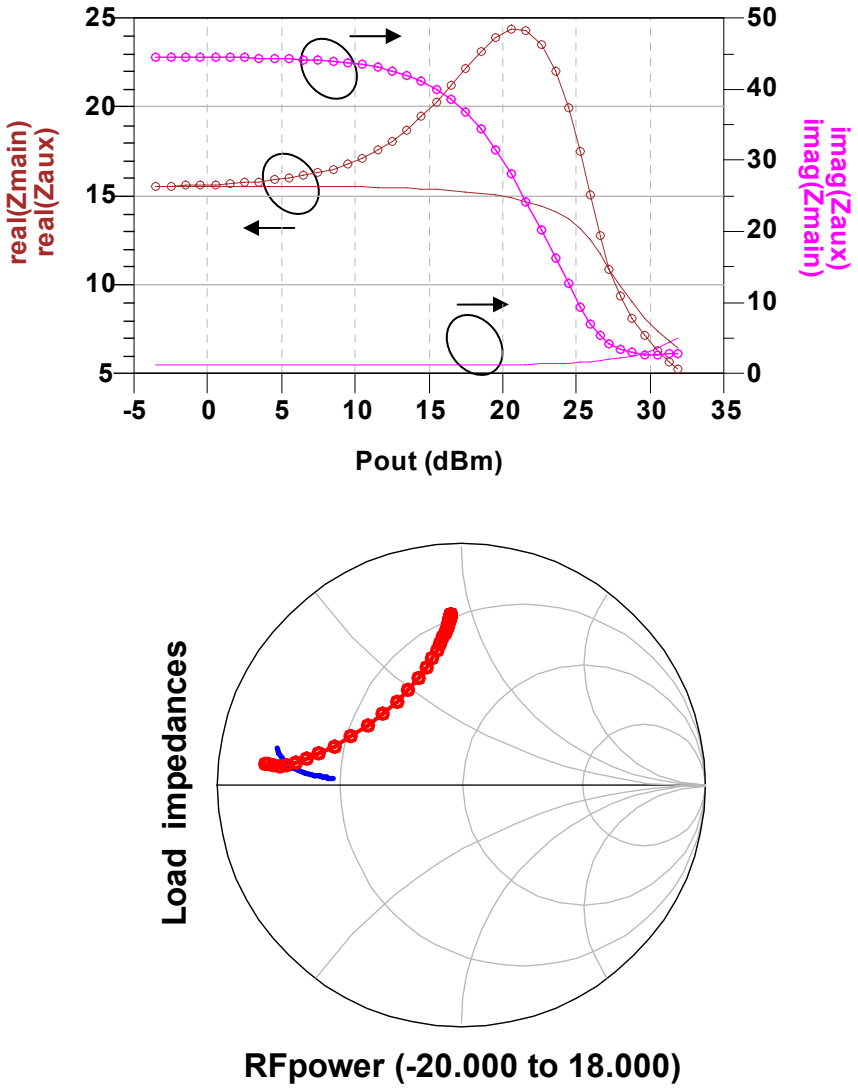


Figure 4.17: Load impedances seen by main and auxiliary amplifiers in the improved Doherty (with θ set to 150º). Solid: for main PA; Circles: for auxiliary PA

It should be noted that while the analytical model presented in previous sections describes the key phenomena leading to Doherty amplifier distortion, it does not accurately represent the full Doherty behavior. For this, the changes of g_m, Y_{be} and Y_{ce} with load impedance should be taken into account, since the load seen by the amplifiers changes with power level. The initial load impedances are chosen to be 16

Ω and 4 Ω. But with the load-pulling effect between the main and auxiliary PA, the load impedance seen by the main PA changes to around 8 Ω at peak power level and the load impedance seen by the auxiliary PA is highly reactive. In the present model, the effect of changing load impedance can only be accounted for approximately, by considering the g_m, Y_{be} and Y_{ce} values at representative load values. To illustrate the effect of the load impedance changes to the extracted model parameters, representative g_m and Y_{be} of the main PA extracted with three load impedances are shown in Fig. 4.18.

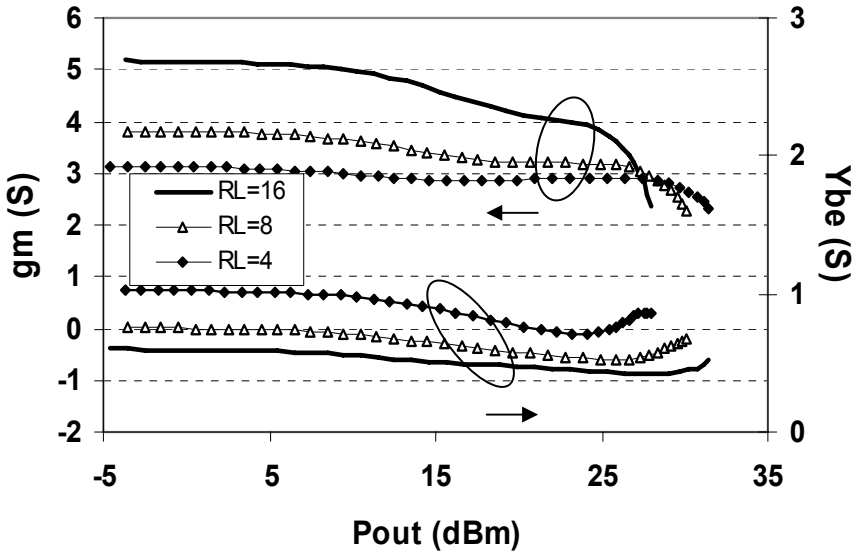


Figure 4.18: Extracted g_m and Y_{be} for the main amplifier with three different load impedances

With an understanding of the load dependence of the model parameters, modifications can be made to the model. Load impedances (Z_L=8 Ω for the main PA, and Z_L=6+4j Ω for the aux PA) closer to the values the two amplifiers experience at high power can be selected for use in the parameter extraction procedure. This

generates extracted components that better characterize Doherty's behavior at high power. Consequently, the prediction of the model matches more accurately with the full simulation results in high power, both are shown in Fig. 4.19. Noticeable is that the gain calculated from the model is increased for low power levels in this case.

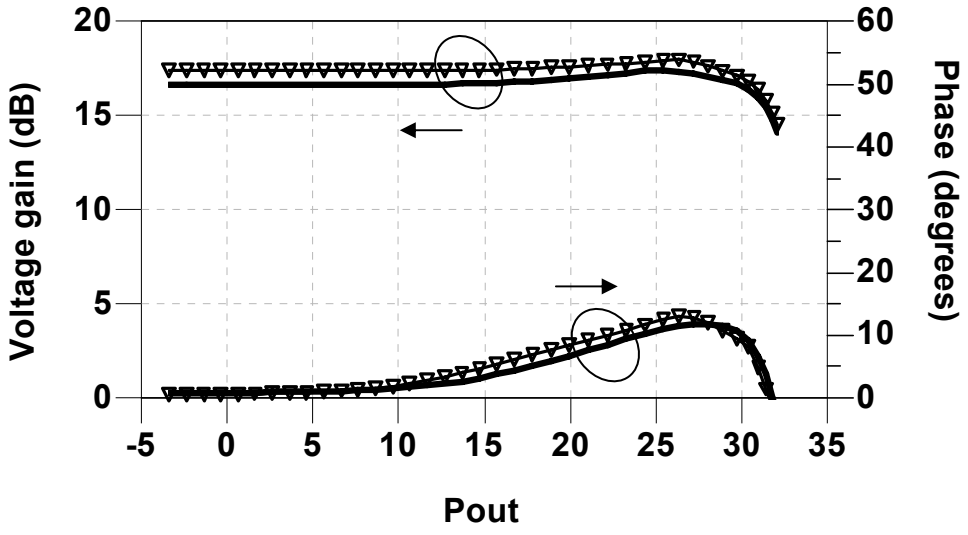


Figure 4.19: Output gain and phase for Doherty amplifier. Triangles: analytical results with optimized load impedances; Solid: simulated

4.5 Experimental Results of a Modified Doherty Amplifier

To demonstrate the efficacy of the analytical model, a Doherty amplifier was fabricated on Roger 4350 PCB board using Skyworks InGaP/GaAs HBTs as represented by the models. Two PA chips (inside the boxes in Fig. 4.20, the actual die photograph is shown in Fig. 4.21) with input matching and bias circuit integrated on chip were mounted on the board. A circuit diagram is shown in Fig. 4.20. The base bias of the main and auxiliary PA is provided by current mirror circuits, which operate

close to a constant voltage source. The quiescent base bias current is set as 55 mA for the main amplifier (Class AB) and 2 mA for the auxiliary amplifier (Class C). The bias current was optimized to achieve an acceptable tradeoff of efficiency and linearity behavior. The output circuits were realized by transmission lines implemented on the PCB board, while the input match was implemented with discrete components on chip. A Wilkinson power divider was used at the input to split the power equally between the main and auxiliary amplifiers. On board are transmission lines with different length used in phase delay tuning. The Doherty amplifier was design to work at 1.88 GHz, and the maximum output power reached 29 dBm (with single tone tests). Predictions by the analytical model are verified in the following experimental results.

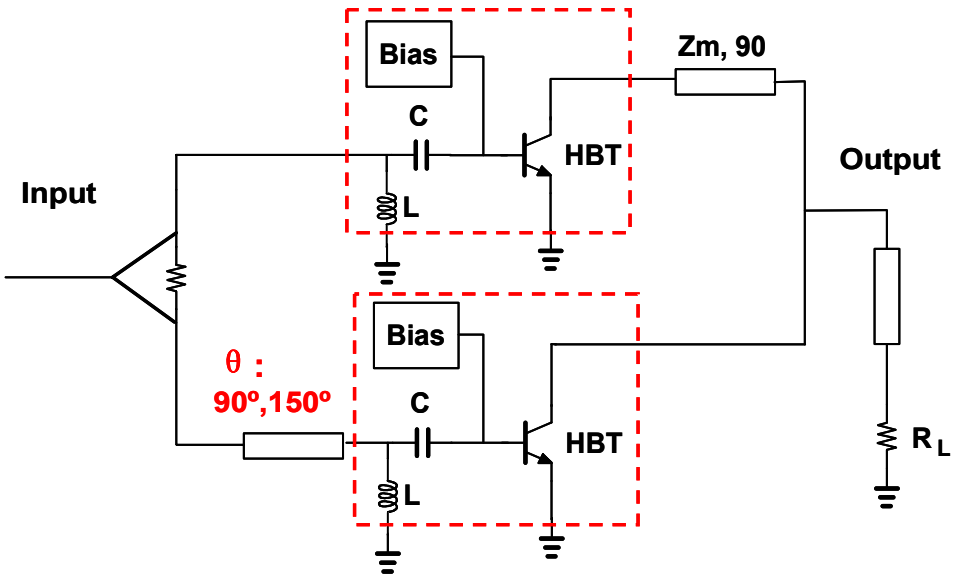


Figure 4.20: Schematic of the experimental Doherty amplifier

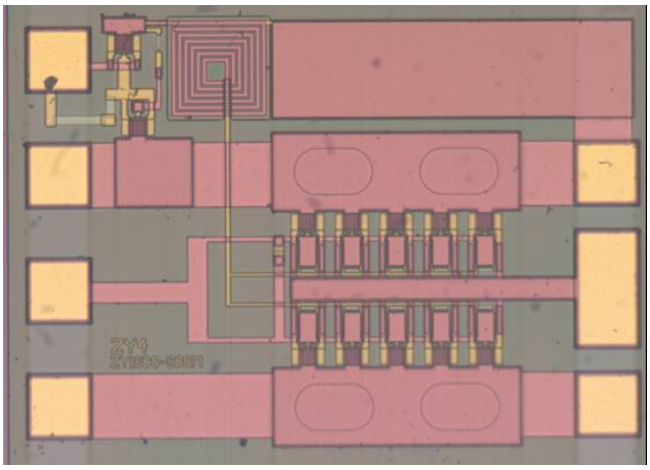


Figure 4.21: Die photograph of the active device

Fig. 4.22 compares the measured gain and phase for the Doherty amplifier when the phase delay in front of the auxiliary PA is 90º and when the phase delay is switched to 150º.

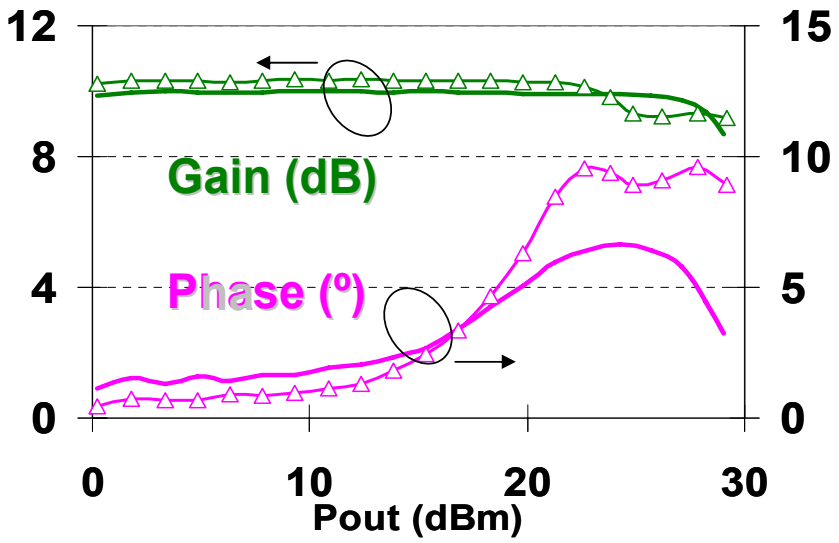


Figure 4.22: Measured gain and phase for the Doherty amplifier with 90º and 150º phase delays feeding auxiliary amplifier. Triangles: 90º; Solid: 150º

With the 150º delay, the Doherty PA shows flatter gain and smaller phase variation (similar to the simulation results) and consequently achieves better IMD3

performance (with improvement as much as 8 dB at 23 dBm), shown in Fig. 4.23. As pointed out earlier, the θ=150º is the point at which we can achieve lowest phase predistortion. In the experiment, it proves to be the best trade off point for overall linearity as well. The experimental results clearly show linearity improvement with θ=150º as the analytical model has predicted, although there is some discrepancy between the measured phase and the simulated one for θ=90º case.

Fig. 4.24 shows the measured power added efficiency with a 2 tone input signal. The Doherty amplifier with 150º delay shows better efficiency particularly at the power level where the auxiliary amplifier turns on.

Using the measured gain and phase data for the case of 150º delay as input for a behavioral model, we can calculate the IMD3 as well as the IMD3 contributions from the gain and phase distortions, individually. Shown in Fig. 4.25 are the measured and calculated IMD3, as well as the IMD3 values resulting from gain and phase distortion alone. It can be seen that the phase is the major cause of IMD3 for output power between 8 and 23 dBm in this Doherty amplifier. At higher Pout levels, the gain distortion is dominant.

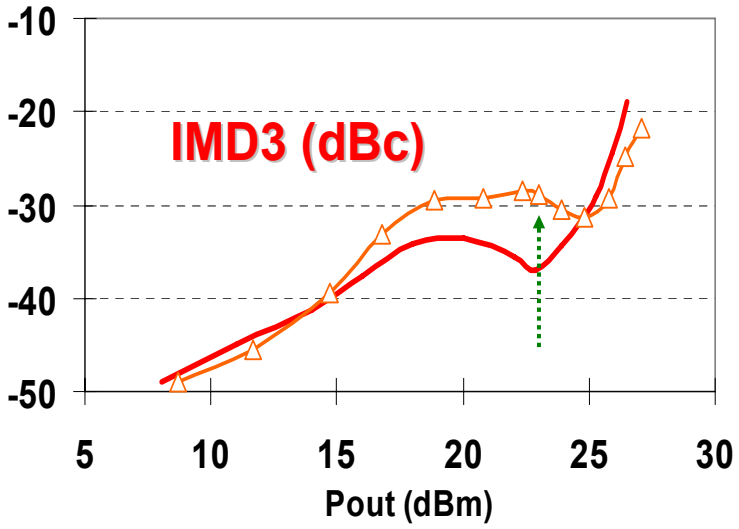


Figure 4.23: Measured IMD3 for the Doherty amplifier with 90º and 150º phase delays

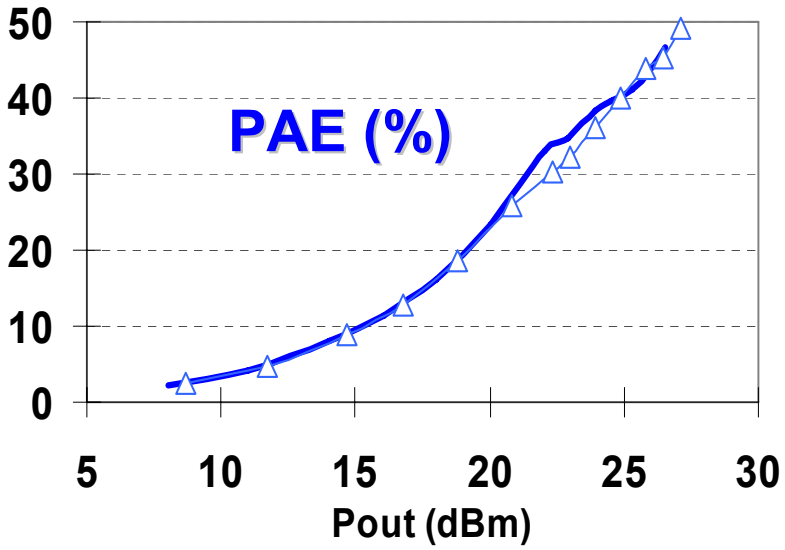


Figure 4.24: Measured power-added efficiency (with 2-tone input) for the Doherty amplifier with 90º and 150º phase delays

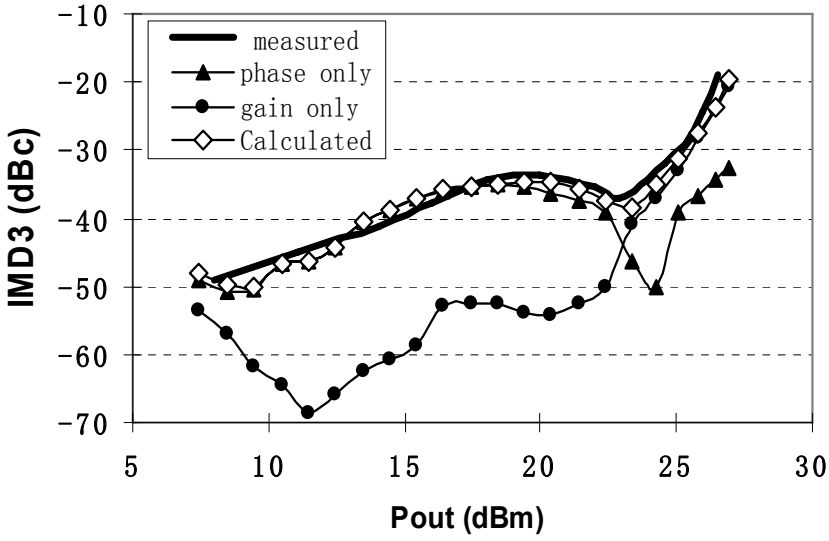


Fig 4.25: Measured and calculated IMD3 for the Doherty amplifier with 150º phase delays feeding the auxiliary amplifier. Also shown are calculated results using only the gain distortion, and only the phase distortion

4.6 Summary

In this chapter, a simple analytical model is developed based on a VBIC device model for InGaP/GaAs HBT devices. This analytical model is shown to be effective in predicting the nonlinear behavior (particularly gain and phase) of single-ended HBT amplifiers as well as Doherty amplifiers. Consequently, this model is very useful in achieving detailed understanding for Doherty amplifiers. It is found that by tuning the phase delay at the input of the auxiliary amplifier, better output gain, phase and consequently better linearity can be obtained for the Doherty amplifier. Explanation is provided based on the analytical model. The efficacy of the model is demonstrated by experimental results, in which a Doherty amplifier with 150º phase delay at the

auxiliary amplifier input shows significant linearity improvement while maintaining its high efficiency performance. Overall, the simple analytical model is shown to be an effective tool for analyzing nonlinear behavior in Doherty amplifiers. The model could potentially be applied to other structures with nonlinearly interacting amplifiers.

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Chapter 5
Conclusions and Future Work

5.1 Dissertation Summary

Recent progresses in wireless communications have led to more complex but highly spectrum efficient modulation schemes. These modulation schemes impose stringent requirements on the wireless transmitters and the power amplifiers within it, especially for those used in handsets. The Doherty amplifier structure has attracted much research interest for this type of application due to its feature of high efficiency over an extended power range. This dissertation studied the characteristics of Doherty amplifiers in simulation and experiment, and then arrived at solutions that led to a simultaneous high efficiency and high linearity performance, which has not been demonstrated adequately in previous work for Doherty amplifiers.

In this dissertation, an overview of the operation of the Doherty amplifier based on simplified current source transistor model was provided. Practical circuit design considerations for a Doherty amplifier were investigated, including load impedances, device size, uneven input power splitting, bias of the auxiliary amplifier, and harmonic terminations. Simulation and measurement results of a Doherty amplifier implemented with GaAs FET devices were discussed to provide a description of performance issues of a Doherty amplifier. Also, for the purpose of

demonstrating the possibility of an integrated Doherty amplifier, a lumped element based Doherty amplifier was built and its performance investigated.

In the experimental work, a Doherty amplifier was demonstrated with high efficiency (PAE>40%) over an extended output power range (>9dB). Its originally poor linearity can be enhanced by DSP control. Special characteristics of Doherty amplifiers were shown to justify controlling the input gate bias voltage of the auxiliary amplifier. DSP was utilized to mitigate variations in gain through this gate bias control and to eliminate phase distortion through baseband phase predistortion. It was shown that, with CDMA IS-95 as input signal, the DSP controlled Doherty amplifier can meet the ACPR specifications while maintaining its high PAE performance. Advantages of analog component based predistortion were also studied and demonstrated by experiments.

Finally, in an effort to find a circuit solution for high linearity, this dissertation delved into nonlinear behaviors in Doherty amplifiers implemented with HBTs. An analytical model was developed based on full device model. The simplicity of the model enables nonlinearity analysis associated with each nonlinear component in the transistor. This results in accurate distortion prediction for both single-ended amplifiers and Doherty amplifiers. The model was used for the diagnosis of nonlinearity in an InGaP/GaAs HBT based Doherty amplifier. Accordingly, circuit modifications were made and shown to significantly improve linearity of the Doherty amplifier.

5.2 Future Work

5.2.1 A Doherty Amplifier with Closed-Loop Control

It was shown in chapter 3 that digital signal processing based control can greatly enhance the linearity performance of the Doherty amplifier without sacrificing its efficiency. It was also shown in chapter 3 that DSP can be used to control the Doherty amplifier in an analog fashion to achieve lower circuit complexity in a transmitter. However, closed-loop control is often needed to ensure a stable and continuous performance under widely changing temperature and other environment conditions. Base-station amplifiers often employ another down conversion chain to feed back the complex envelope signal and thus carry out some adaptations and other functions in digital domain. For a Doherty amplifier oriented for handset applications, the closed-loop control should be implemented entirely in an analog circuit embedding. This could be done in a Cartesian like feedback loop [1]. A potentially more suitable solution for a Doherty amplifier is to use peak detectors to monitor output voltage of the main and the auxiliary amplifier. If indicators of nonlinearity can be found in terms of output voltage values for the main and the auxiliary amplifier, adjustments can be potentially made also through analog circuit (phase shifter, attenuator or diode) on the input side of the circuit. Research works are being carried out in UCSD to implement feedback loop based performance enhancement techniques for RF power amplifiers, including Doherty amplifiers.

5.2.2 Extended Applications of the Simple Analytical Model

In chapter 4, the developed simple analytical model was shown to be very effective in analyzing nonlinear behavior in a Doherty amplifier as well as single-ended amplifiers. The most important feature is its simplicity. In situations like Doherty amplifiers, multiple nonlinear transistors interact with each other. Other analytical tools such as Volterra Series would be too complicated to solve. Potentially, this new analytical model could also be applied to other power amplifiers with nonlinearly interacting devices, for example, Chireix (or outphasing) type of amplifiers [2].

5.2.3 Doherty Amplifiers in Other Applications

In this dissertation, Doherty amplifiers have been designed for handset applications for CDMA Systems. However, potential applications for a Doherty amplifier should not be limited to this. The Doherty structure should also be an intriguing candidate for W LAN applications, WiMax and other applications.

In this dissertation, Doherty amplifiers are designed with either GaAs FETs or GaAs HBTs. With the recent surge of research interest on CMOS based amplifiers, suitable solutions to use CMOS technology to fully integrate the Doherty amplifier on chip are beginning to appear [3]. The need for creative designs to adequately reduce loss in integrated output impedance match for a Doherty remains a key for protecting its high efficiency performance. Further inventions need to done in the future.

5.3 References

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