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Liliental, Z.

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TEM INVESTIGATION OF TITANIUM-SILICIDE SCHOTTKY CONTACTS ON GaAs

Z. Liliental, C. Kocot,* J. Washburn and R. Gronsky

Materials and Molecular Research Division, Lawrence Berkeley Laboratory
University of California, Berkeley, California 94720

ABSTRACT

Titanium silicides were used as Schottky contacts on GaAs. Samples with two different ratios of Ti:Si 1:2 and 1:3 were prepared. The composition with the 1:3 Ti:Si ratio was found to result in good Schottky contact parameters. Structural and analytical investigations, including high resolution electron microscopy and energy dispersive X-ray spectroscopy, were used to characterize the formed contacts.

*Hewlett Packard Laboratories, Palo Alto, CA 94304.

INTRODUCTION

The formation of Schottky barriers on GaAs has been a field of wide interest for several decades due to its importance for many devices.^[1-5] However, our present understanding of Schottky barrier formation is still unsatisfactory. Several present models assume that the interface between metal and semiconductor, the defects that are present there, and the interface chemistry can strongly influence the electrical properties of Schottky and ohmic contacts on GaAs.^[6-8]

Metal silicides are used widely for both ohmic and Schottky contacts in silicon very large scale integration (VLSI) technology for lowering the contact resistance and controlling Schottky barrier heights as well as for gate materials in metal-oxide-semiconductor (MOS) devices.^[9-15] Among the refractory metals Ti is the most popular material. Successful use of titanium silicides as contacts on Si suggested the possibility of their application as Schottky contacts on GaAs.

SAMPLE PREPARATIONS

For the investigations reported here, alternate layers of titanium and silicon were deposited on n-type GaAs by electron beam deposition. The measured vacuum was $\sim 10^{-7}$ torr. Standard organic solvent cleaning procedures (1 sec in $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$) were applied to the GaAs samples before the layer deposition. Different layer thickness of Ti and Si were deposited on GaAs in order to achieve different Ti to Si ratios. Alloying treatment was carried out for 5 sec in Ar ambient on each sample by transient thermal annealing

(flash lamp annealing [16]) at 800°C, 825°C, 875°C, or 950°C. The temperature was measured by a thermocouple located inside the Si wafer on which the samples were placed.

ELECTRICAL RESULTS

I-V forward characteristics were used to measure the ideality factor and barrier height for about 100 diodes. The Ti:Si composition with a 1:3 ratio annealed for 5 sec at 875°C resulted in good Schottky contacts. The barrier height and ideality factor for these samples were 0.8 eV and 1.15 respectively. The same heat treatment procedure for the Ti:Si composition with a 1:2 ratio gave poorer electrical parameters. The barrier height and ideality factor for these samples were 0.75 eV and 1.5, respectively.

ELECTRON MICROSCOPY

Ten cross-section samples of Ti:Si of each ratio (1:2 and 1:3) were prepared for both the annealed and unannealed compositions, for a total of 40 samples. These samples were examined in a JEOL 200 CX electron microscope at a primary voltage of 200 KV and a point-to-point resolution of 2.5 Å. All high resolution images were recorded with the beam parallel to the GaAs [011] direction, where two sets of GaAs (111) planes and also the (200) planes were directly resolved. Energy dispersive X-ray spectra (EDX) were taken using a Philips 400 FEG electron microscope at 100 KV accelerating voltage.

Ti:Si WITH A 1:2 RATIO

Unannealed structures with Ti:Si ratios of 1:2 consisted of four layers: Ti (with a thickness of 420 Å) adjacent to GaAs, followed by Si (770 Å thick), Ti (580 Å thick), and Si (730 Å thick) (Fig. 1).

The interface of the first Ti layer with GaAs was very flat and abrupt, whereas both the Si interfaces with the second Ti layer were rather diffuse. All four layers were clearly distinguishable. EDX spectra of these layers showed the presence of Ti or Si in respective layers.

After transient thermal annealing for 5 sec at 875°C, the layers were still clearly distinguishable (Fig. 2), but metal-semiconductor interfaces were very rough in most cases. There were only a few areas where flat interfaces were still present. High resolution images of the interface with GaAs showed that in many cases, the orthorhombic TiSi_2 (C49) phase, with lattice parameters $a = 3.62 \text{ \AA}$, $b = 13.76 \text{ \AA}$, and $c = 3.605 \text{ \AA}$, had been formed. Epitaxial growth of this compound was observed where (220) GaAs planes were parallel to (040) TiSi_2 planes. This growth was confirmed by the HREM image and the diffraction pattern taken from the interface (Fig. 3). This phase is not the only one found on the interfaces. The other TiSi_2 (C54) phase, with lattice parameters $a = 8.27 \text{ \AA}$, $b = 4.79 \text{ \AA}$, and $c = 8.55 \text{ \AA}$, was also found in a few cases near the interface. The volume fraction of this phase was about 50% lower than that for TiSi_2 C49 for the Ti:Si 1:2 specimens.

EDX spectra showed that the ratio of $\text{TiK}\alpha/\text{SiK}\alpha$ does not remain constant in all areas of the contact material (Fig. 4). This finding suggests that during annealing more than one compound was formed. The contact material consisted of many small grains. Often the selected area diffraction (SAD) patterns showed overlapping of different phases. The chemical reactions that occurred during annealing caused a thickness change of all the layers. The Ti layer adjacent to the GaAs was

almost completely replaced by rapid irregular growth of TiSi_2 on the interface with GaAs. The thickness of this layer varied from a few Å to 1000 Å. The second layer of amorphous Si had an approximately constant thickness of 250 Å. The third layer (Ti in the unannealed case) decreased in thickness to 450 Å. This layer consisted of many grains of different composition: TiSi_2 C49, TiSi_2 C54, and Ti.

The top Si layer consisted of two sublayers: 400 Å of amorphous Si and 400 Å of partially crystalline Si. The existence of these layers was confirmed by high resolution images (Fig. 5). The top layer consisted of many Si grains, and lattice fringes characteristic for Si(111) planes were visible. On the same picture (Fig. 5), the top part of the original second Ti layer is shown (labeled Ti), with lattice fringes of 2.3 Å. The ASTM data files [17] show the dominant line for Ti corresponds to the 2.24 Å spacing. For TiSi_2 C49 the spacing is 2.23 Å, and for TiSi_2 C54 it is 2.3 Å. It is therefore not possible to distinguish conclusively which of these compounds were present in those particular areas, because there was only one row of spots on the diffraction pattern and in the HREM image there was only one set of lattice fringes with 2.3 Å spacing.

Ti:Si WITH A 1:3 RATIO

The samples with the Ti:Si ratio of 1:3 after transient thermal annealing for 5 sec at 875°C (Fig. 6) looked similar to the Ti:Si 1:2 samples, but often the distinction between all four layers almost disappeared. In most cases only small isolated amorphous Si volumes were present at the depth of the deposited Si layers.

The interface with GaAs was rough, similar to the interface for the 1:2 Ti:Si samples. There were some interpenetration of silicide and GaAs along the original interface. Figure 7 shows the trace of the original interface (from the unannealed deposited sample) inside the newly formed silicide grains. The grains on the interface are much larger (up to 5000 Å long). Diffraction patterns taken from the interface (Fig. 8a) and at the center of the contact (Fig. 8b) show mostly the TiSi_2 C54 phase. The TiSi_2 C49 phase was found as well, but it was found less often than was the C54 phase. The higher concentration of Si in these samples appeared to favor the formation of the TiSi_2 C54 phase.

All phases formed on both unannealed and annealed samples with Ti:Si ratios of 1:2 and 1:3 are shown schematically in Fig. 9. In the samples with 1:2 ratios, the TiSi_2 C49 phase dominated, whereas in the samples with 1:3 ratios, the C54 phase dominated.

SUMMARY

The results show that titanium silicide contacts are far from being homogeneous, continuous TiSi_2 . However, good electrical properties are achieved for the 1:3 Ti:Si ratio (barrier height 0.8 eV and ideality factor 1.15) in spite of the very incomplete reaction and rough interface. Longer annealing times or furnace annealing would probably result in more uniform structures. However, such longer heat treatment could be undesirable for high electron mobility (HEMT) GaAs-AlGaAs circuits.

Therefore the superior electrical properties of the 1:3 Ti:Si samples have been tentatively attributed to the presence of a higher volume fraction of the TiSi_2 C54 phase. Further investigations are in progress to correlate structural and analytical information with the electrical properties.

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FIGURE CAPTIONS

Fig. 1. Alternate layers of Ti and Si with a 1:2 ratio deposited on GaAs.

Fig. 2. The layers shown in Fig. 1 after transient thermal annealing at 875°C for 5 sec (notice the very rough interface with GaAs).

Fig. 3. High resolution image of the GaAs/TiSi₂ interface shown in Fig. 2. (The insert is a diffraction pattern from the interface - indices are given for TiSi₂ C49 phase).

Fig. 4. EDX spectrum from a sample annealed at 875°C for 5 sec with a 1:2 Ti:Si ratio:

- a) the layer adjacent to the GaAs substrate;
- b) the second layer;
- 3) the third layer (Ti in the unannealed sample);
- 4) the top layer.

Fig. 5. High resolution image of the top layers of a sample with a 1:2 Ti:Si ratio annealed at 875°C for 5 sec. The 2.3 Å lattice fringes are visible on the left side of the image, and the grains with Si lattice fringes are visible on the right side.

Fig. 6. Bright field image of a sample with a 1:3 Ti:Si ratio annealed at 875°C for 5 sec.

Fig. 7. The layer adjacent to the GaAs substrate in a sample with the 1:3 Ti:Si ratio. The trace of the original interface from the unannealed sample is visible (marked by the arrows) inside the newly formed silicide grain.

Fig. 8. Diffraction patterns representing the TiSi_2 phase from different areas of an annealed sample with a 1:3 Ti:Si ratio:

- a) the interface - the diffraction pattern represents both the $\text{TiSi}_2\text{C54}$ phase and the [110] GaAs;
- b) the middle part of the contact (the second Ti layer in the unannealed case).

Fig. 9. Schematic diagram of the phases formed in unannealed and annealed samples:

- a) unannealed sample with a Ti:Si ratio of 1:2; the unannealed samples with 1:3 ratios are similar, with some differences in the thickness of the layers;
- b) as above, annealed at 875°C for 5 sec;
- c) annealed sample with a Ti:Si ratio of 1:3.

XBB 852-1174 B

Fig. 1

XBB 852-1174 C

Fig. 2

XBB 852-1169

Fig. 3

XBL 855-2461

Fig. 4

XBB 852-1171

Fig. 5

XBB 852-1174A

Fig. 6

XBB 855-3860

Fig. 7

XBB 855-3859

Fig. 8

XBL 855-2508

Fig. 9

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BERKELEY, CALIFORNIA 94720*