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UNIVERSITY OF CALIFORNIA, SAN DIEGO

**Silicon Nanowire Phototransistor:
Designing, Fabricating and Characterizing a High Responsivity,
Broadband Photodetector**

A dissertation submitted in partial satisfaction of the requirements
for the degree Doctor of Philosophy

in

Electrical Engineering (Applied Physics)

by

Arthur Yasheng Zhang

Committee in charge:

Professor Yu-Hwa Lo, Chair
Professor Peter Asbeck
Professor Prabhakar Bandaru
Professor Andrew Kummel
Professor Deli Wang

2010

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Chair

University of California, San Diego

2010

DEDICATION

To my family,
without whom this dissertation would not be possible.

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ABSTRACT OF DISSERTATION

Silicon Nanowire Phototransistor: Designing, Fabricating and Characterizing a High Responsivity, Broadband Photodetector

by

Arthur Yasheng Zhang

Doctor of Philosophy in Electrical Engineering (Applied Physics)
University of California, San Diego, 2010

Professor Yu-Hwa Lo, Chair

Nanowire photodetectors have been attracting increased attention due to their potential for very high sensitivity detection stemming from the unique properties of these quasi-one dimensional structures. Silicon photodetectors are of particular interest due to their low cost, ease of processing and ability for integration with conventional fabrication techniques. This work focuses on

utilizing silicon nanowires towards creating a very high responsivity detector sensitive to a wide range of wavelengths from the ultraviolet to the near infrared spectrum.

A physical understanding of the silicon nanowire phototransistors studied in this work is crucial for applying them towards high sensitivity imaging. The novel device concept is first presented qualitatively, illustrating how surface states in conjunction with geometrical effects of the nanowire create a large phototransistive gain. The device theory is then formalized mathematically, revealing the important physical quantities responsible for gain and the theoretical sensitivity achievable in such devices. Subsequently, simulations are performed to validate the concept and determine the parameters which govern device behavior.

A top-down fabrication approach is utilized in creating these devices, allowing for precise control over geometry, traditional doping techniques, large area device formation, and compatibility with industrial fabrication lines. The devices are patterned through either traditional technology with e-beam lithography or maturing technology with nanoimprint lithography, and the nanowires formed through highly anisotropic dry etching. The finished devices are embedded in dielectric to support a top transparent contact.

Characterization of these devices exhibits very high responsivity and phototransistive gain. Static measurements at room temperature show the initial demonstration of the device. Spectral measurements are then

performed, showing absorption enhancement effects in vertical nanowire structures. Temperature dependent measurements demonstrate the capabilities of the device to detect illumination levels down to the sub-femtowatt at visible wavelengths, and picowatt at infrared wavelengths, unseen in bulk or thin-film devices. Finally, dynamic measurements determine the bandwidth of the device and a critical time constant in the kHz range.

The characterization of these devices reveals both their potential and limitations. Future work on this device is proposed to engineer more reliable control over gain, lowered dark current for room temperature operation, and increased sensitivity.

Chapter 1

Introduction

1.1 Photodetection

Photodetectors are an essential component in many applications. They are pervasive in a myriad of devices from every day commercial items, most commonly noticed in digital cameras, to highly specified research tools. Photodetectors are found in receivers for optical communication from common optical fibers, to laser based space communication. They are used in medical diagnostic equipment to analyze blood samples and image tissue samples. The requirements for each of these applications vary greatly in their need for differently levels of sensitivity, power usage, bandwidth, resolution and responsivity to various wavelengths. However, many of these applications can benefit from a truly high sensitivity, low power, broadband detector that has a small footprint and is easily scalable.

Semiconductor materials are often used to build photodetector devices. As research into the area of semiconductor photodetection progresses, devices have continued to scale toward nano-sized dimensions. As the devices enter the nanometer scale, new device properties have been discovered, which when designed properly can be greatly beneficial to device performance. Nanowire devices are one such device geometry which has

shown much promise^{1, 2}. The fabrication of nanowires has been an intense research area in the past decade, and now nanowires can be realized from semiconductors, to metals, to superconductors in precisely engineered manners. This creates many opportunities for the understanding and use of the unique properties that arise from low-dimensional systems and their incorporation into devices including transistors, chemical sensors, nanomotors, and in particular photodetectors. The potential of using the unique properties of nanowires to create a photodetector with greatly improved performance is investigated in this work through silicon nanowire phototransistors to create a scalable, low power, high responsivity detector sensitive to a wide spectrum. Before delving into the details of this research, it is prudent to briefly review the basics of photodetection and the previous advances in the field of nanowire photodetection.

1.2 Overview of Nanowire Photodetectors

The continued scaling of photodetector devices has brought quasi-one-dimensional nanowire structures into the forefront of research. These devices not only promise to provide a smaller footprint, allowing for increased pixel density, but also allow for increased device performance through the unique physics that arises from the shrinking of dimensionality towards one dimension.

1.2.1 Fabrication

Fabrication of nanowire photodetectors follows two general approaches: bottom-up growth, and top-down etch, each with their benefits and disadvantages. Traditionally, nanowires have been formed through growth techniques. Using this method, nanowires of many different semiconductors are able to be formed, with homo- or hetero-junctions both in the axial or radial directions. This gives great flexibility when designing devices with specific properties. Initially, this technique entailed using a growth catalyst (typically gold) dispersed on a substrate of the same material to be grown, and relied on the vapor-liquid-solid (VLS) technique to grow homogeneous material in a chemical vapor deposition (CVD) chamber³⁻⁷. Through control of the growth conditions, one could control the length and morphology of the wires, although specific placement of the wires, and uniformity and reproducibility of wire dimensions was difficult. This method also sometimes resulted in impurities from the growth catalyst left in the nanowire, creating defects and traps. Substrates of rare materials have also been expensive to acquire. Recent advances have overcome many of these difficulties. Growth of nanowires has been demonstrated with high purity without the need of a catalyst and on patterned substrates of dissimilar material than the nanowires themselves⁸⁻¹¹.

The top-down approach for nanowire fabrication has been a more recent development usually utilized in silicon¹²⁻¹⁴. This approach entails the

lithographic patterning of the nanowire structures (usually through e-beam lithography or more recently nanoimprint lithography), forming a mask that is then used to etch material away from the substrate. This allows for the formation of both planar and vertical structures with uniform and reproducible geometries in precisely defined positions, and allows for the incorporation of homojunctions formed beforehand in the substrate. This methodology has the potential of being easily scalable, and able to be incorporated with complementary metal oxide semiconductor (CMOS) circuitry into a standard CMOS fabrication line.

1.2.2 Structures

Quasi-one-dimensional photodetector structures based on semiconducting, superconducting, or metallic nanowires are being actively investigated for effective conversion of optical to electrical signals. Conventional photodetector concepts and architectures such as semiconductor photodiodes are being replicated in nanowire structures through homo- and hetero-junctions to create photodetectors with potential for denser integration. Additionally, novel concepts arising from the large surface to volume ratio or from the small nanowire dimensionality show promise to enhance photosensitivity, and ultimately reach single-photon detectivity. A few of these structures are introduced in the following sections.

1.2.2.1 Photodiodes

Nanowires offer a variety of methods to form photodiode architectures, which include Schottky metal-semiconductor junctions and homo- or heterojunctions and can be formed either axially or radially. These photodiodes have been created on a variety of materials for detection of different wavelengths. GaN based ultraviolet photodetectors using axial p–n homojunctions have shown rectifying behavior, relatively fast photoresponse, and a strong photoconductive increase at small reverse bias¹⁵. InAs/InAsP based infrared photodetectors based on single nanowires with axial heterojunctions operated at low temperature exhibited very low dark current due to the conduction band offset between the dissimilar materials and a contributions to the photoconductive response from both the InAs and InAsP portions¹⁶.

Core shell nanowire structures are of great interest for efficient photosensing that take advantage of a more effective charge carrier separation, and the possibility of enhanced light absorption in vertically aligned arrays¹⁷. Thus far, efficient photoresponse has been demonstrated in both single Si nanowire devices¹⁸ and vertical GaAs nanowire arrays¹⁹ with radial homojunctions. Core/shell nanowire heterostructures with type-II band offsets have also been proposed²⁰ and demonstrated²¹ to enhance charge carrier separation and improve both the photosensitivity and enhance the spectral response.

Vertical nanowire photodetectors formed from heterojunctions between nanowires and their growth substrates have also been investigated. Large nanowire densities are desirable in these cases to increase the photoactive area and thus enhance the photoconductive response. In particular, due to the ease of fabrication by a variety of methods, including chemical vapor deposition,^{22, 23} solvothermal methods,²⁴ or magnetron sputtering,²⁵ a substantial amount of work has been dedicated to heterojunction photodetectors made of ZnO nanowires on doped Si substrates. In these structures, depending on the density of the nanowire network, the top electrode can be either deposited directly onto the nanowire layer or a transparent dielectric can be used to reduce leakage current. Intrinsically-doped, n-type ZnO nanowires have been grown on both, p-type or n-type Si substrates^{8, 26, 27}. In a study of n-ZnO nanowire/n-Si heterojunction devices, the spectral sensitivity could be tuned from the visible to the ultraviolet spectrum by applying forward or reverse bias to the device, thus controlling the band-offset at the material interface and selectively collecting photocarriers that are generated in the Si substrate, or in the ZnO nanowires²⁵. Recent advances in the direct epitaxial growth of III-V nanowires on Si will also open up new opportunities for vertical nanowire array photodetectors and photovoltaics²⁸⁻³⁰.

Another interesting class of nanowire photodetectors is found in avalanche photodiodes. These devices operate at large reverse bias, which

allows each photogenerated carrier to be multiplied through avalanche breakdown caused by band-to-band carrier impact ionization. Carrier multiplication results in internal gain within the photodiode, which increases the responsivity of the device. So far, nanowire avalanche photodiodes have been demonstrated in two different configurations: a “crossed” n-CdS/p-Si nanowire heterojunction and an axial p-i-n Si nanowire homojunction^{31, 32}. In the case of the n-CdS/p-Si avalanche photodiode, a photocurrent increase of $\sim 10^4$ higher than an individual n-CdS or p-Si nanowire photoconductor has been observed and a detection limit of 75 photons estimated³¹. Very similar results were obtained with the axial p-i-n Si nanowire avalanche photodiode, where complementary doping within a single nanowire was used instead of the assembly of two distinct nanowires. A maximum multiplication factor of $M = 40$ was derived in these devices³².

A third category of photodiodes is devices with metal-semiconductor junctions. Here both the electrons photogenerated in the metal and the electron-hole pairs photogenerated in the semiconductor can contribute to the photocurrent. One of the advantages of Schottky photodiodes is their fast response speed due to the short carrier transit time across the junction under reverse bias. Despite a good understanding of metal-semiconductor junctions in nanowire devices, the intentional fabrication of Schottky photodiodes has been rarely pursued in materials other than ZnO nanowires. Noble metals including Au, Ag and Pd form Schottky contacts with n-ZnO. Therefore two-

terminal nanowire devices with symmetric contacts made of these metals usually behave as back-to-back Schottky diodes, and are responsive to ultraviolet illumination³³⁻³⁶.

1.2.2.2 Phototransistors

A traditional phototransistor is often composed of a bipolar or unipolar transistor where light is able to reach the base creating optically generated carriers. This modulates the base-collector junction which results in an amplified current through transistor action. Such structures have been successfully implemented in nanowire architectures as well. In addition to bipolar devices, nanowire field-effect transistors have also been an area of study and have been fabricated by dispersing nanowires on a dielectric-semiconductor substrate³⁷⁻⁴² or by patterning nanowires through conventional lithographic methods⁴³⁻⁴⁶. Subsequently, a gate bias is applied through a lithographically patterned top gate, or a back gate. In the case of these field effect phototransistors, an electrical gate bias is used to modulate the lateral field across the nanowire. However, a similar effect is also present in the nanowire phototransistors presented in this work in which surface states give rise to a radial electric field. As discussed in more detail in the following chapter, this causes the separation of photogenerated carriers in the nanowire channel, which greatly extends the carrier recombination lifetime leading to a much higher sensitivity. Thus, these nanowire devices can be viewed as

phototransistors where the internal field arising from the large density of surface states in conjunction with light illumination act as an optically modulated gate. Depending on the nanowire material, band bending can be caused by different surface mechanisms, such as the presence of a strong surface potential, found in GaN nanowires^{47, 48} the presence of deep trap states, as in oxygen-related hole traps in ZnO nanowires, or surface states, seen in Si or Ge nanowires^{39, 49}.

1.2.2.3 Superconducting Photodetectors

Another photodetector concept that makes use of the unique geometrical properties of nanowires is that of superconducting nanowire photodetectors. Thus far, demonstrations of this concept have been focused on NbN nanowires, with typical dimensions of ~5 nm thickness and 50-200 nm width, which have yielded single photon sensitivity with GHz counting rate and high detection efficiency⁵⁰⁻⁵². The high sensitivity of superconducting nanowire detectors relies on the much smaller (by two to three orders of magnitude) energy bandgap than in a semiconductor. Thus a photon absorbed in a superconducting detector creates an avalanche of electron charge two to three orders of magnitude greater than in a semiconductor for the same photon energy. The absorption of a photon creates a local non-equilibrium perturbation with a large number of excited hot electrons. This increases the average electron temperature and results in the formation of a hotspot and

thus local non-superconducting region. The size of the resistive region grows as hot electrons diffuse out of the hotspot, and a non-superconducting barrier is formed across the entire width of the device, hence the need for nanowire geometry with narrow width. Ultimately, this results in a photoresponse characteristic⁵⁰. Since the energy relaxation time of excited electrons in superconductors are on the order of picoseconds, single photon detectors with GHz repetition rate are achievable by these devices^{50, 51} with sensitivity from the visible to the infrared spectral range.

1.2.2.4 Metal and Metal-Dielectric Photodetectors

Another novel nanowire photodetector concept makes use of metallic nanowires with diameters of few nanometers. Large photoconductive increases have been observed in Au nanowires with small restrictions when illuminated by light pulses⁵³, an effect that would be completely unexpected in metals. Recently, photoinduced voltage has also been observed in macroscopic bundles of Ag core, Ni shell nanowire heterojunctions⁵⁴. This type of nanowire photodetector may prove useful in conjunction with plasmonic elements for nanophotonic applications. Metal-dielectric nanowires, such as “peapod” systems in which metal nanoparticles are embedded in dielectric nanowires can also be utilized for light sensing applications. For example, Au nanoparticle embedded in silica nanowires have shown large photoresponse at photon energies resonant with surface plasmons⁵⁵.

1.2.3 Materials

Many semiconducting materials which have shown photoconducting behavior have been investigated as possible building blocks for photodetectors. The myriad of materials allows for the ability to engineer a variety of behaviors from device bandwidth to spectral sensitivity. Below we outline a few groups of these materials.

1.2.3.1 Group III-V Materials

III-V compound semiconductors have been shown to be very promising materials for nanowire photodetectors due to their excellent transport properties, ease of doping, and the possibility to tune their optical absorption over a wide spectral range through bandgap engineering. Studies on the photoresponse of III-V compound nanowires have been focused primarily on their ultrafast photocarrier dynamics^{56, 57}. GaAs, AlGaAs and InGaAs nanowires have all shown ultrafast charge carrier relaxation in the picoseconds time domain⁵⁶. More recently, fast photoconductive response has been demonstrated in an intersecting array of InP nanowires.⁵⁷

Group III-nitride based nanowires have also been attracting increasing attention for ultraviolet photodetection, which could potentially be extended to the entire visible spectrum by alloying with InN. Similar to metal-oxide nanowires, networked GaN nanowires have shown strong sensitivity to the ambient conditions (air vs. vacuum)⁵⁸ and the existence of persistent

photocurrents^{37, 58} due to surface states in forming deep-level traps. As mentioned earlier, surface states in a nanowire device can play a major role in determining the photocarrier lifetime, and ultimately the nanowire photoconductive response. As a result, the photocurrent density may strongly depend on nanowire diameter, as was observed in GaN nanowires. Due to the presence of a surface depletion space charge layer, carrier lifetime in these devices is greatly prolonged in nanowires with diameter larger than 100 nm while is significantly reduced in smaller diameter nanowires due to enhanced surface recombination⁴⁷.

1.2.3.2 Group VI Materials

One of the main advantages of group VI semiconductor nanowires, including Se and Te, is the availability of solution-based synthetic methods^{59, 60}, which could potentially allow low-cost and large scale production of nanowires on a variety of host substrates. A large photoconductive increase has been shown in Se nanowires upon exposure to light, and the photoconductive response was found to saturate at high light intensities⁵⁹. Photoactive Te nanowires have also been studied in a multilayer Te nanowire/polyelectrolyte thin solid film, demonstrating extremely long rise and decay times of the photoconductance of about 40 seconds⁶⁰.

1.2.3.3 Group II-VI materials

II-VI semiconducting compounds are widely employed in optoelectronic applications due to their direct bandgap and a wide coverage of bandgap energies. A large variety of II-VI semiconductor nanowires has been synthesized by different methods, and showed significant photoresponse in the infrared, visible, and ultraviolet spectral range. HgCdTe, for instance, is one of the most important semiconductor materials for infrared detection since its bandgap can vary over a wide spectral range, from the far-infrared to 1.5 eV. Infrared photodetectors have also been realized by using electrochemically self-assembled CdS and ZnSe nanowires electrodeposited in porous alumina. In these devices, the nanowire resistance increased up to two orders of magnitude upon exposure to infrared radiation (negative photoreponse), most likely due to photoinduced electron trapping from the semiconductor nanowires to the surrounding alumina⁶¹. Wide bandgap II-VI materials, such as CdTe, ZnTe, CdSe, ZnSe, and CdS are typically used for visible light detection. CdS nanowires and nanobelts are among the most studied photoconductors in group II-VI for visible and ultraviolet light detection⁶². Similar to the case of metal-oxide nanowires, the photoresponse of CdS nanowires is strongly affected by surface oxygen photochemistry, which can significantly alter the photocarrier relaxation dynamics⁶³⁻⁶⁶. ZnSe nanowires have also been studied as visible light detectors^{67, 68} achieving a

high responsivity showed persistent photocurrent behavior with slow relaxation components attributed to the presence of deep traps^{67, 68}.

1.2.3.4 Metal Oxide Materials

Metal-oxide nanowires are a very important group of photoconductors. Due to their wide bandgap, metal-oxides have attracted great attention for the creation of both transparent electrodes and ultraviolet photodetectors. In addition, the strong influence of surface chemistry on the conductive and photoconductive properties of metal-oxide nanowires makes them especially suitable for gas and chemical sensing.

A combination of ease of synthesis and attractive optical, mechanical, and magnetic properties makes ZnO one of the most studied nanowire materials. Of these, the material's photoconductivity has been of great interest. Due to its wide bandgap, ZnO nanowires may find application in visible-blind ultraviolet photodetectors. Additionally, the presence of oxygen vacancies sometimes results in deep level donor states which may be used to extend the spectral range of ZnO to the visible spectrum⁶⁹⁻⁷². In one of the earliest reports on ZnO nanowire photodetectors, high photoconductive response has been observed upon exposure to ultraviolet light⁷³ with extremely long photocurrent relaxation times, related to carrier trapping. It is known that photoconduction in ZnO nanowires is governed by a charge-trapping mechanism due to oxygen adsorption and desorption at the surface^{39, 40, 42, 49,}

^{69, 74-79} making them promising devices for gas sensing applications. Besides ZnO, a variety of other metal-oxide nanowire photoconductors have also been investigated, among which are gallium, tin, indium, cadmium, and vanadium oxides.

1.2.3.5 Group IV Materials

Group IV semiconductor nanowires are most commonly comprised of Si and Ge. Si has been the material of choice for visible light detection for many years due to its well known material properties and ease of fabrication in line with traditional processing methods. Si nanowire based photoconductive devices have been fabricated through both chemical synthesis⁸⁰⁻⁸² and etch-back methods^{43, 44, 83}, followed by standard lithographic processes. In most of these cases, devices have shown large photoconductive gain which saturates at high irradiation intensities⁴⁴. Typical rise and decay times in intrinsic nanowires are less than 100 μ s, but those times greatly increase with doping due to the formation of midgap states created by defects in the crystalline structure⁸². The photoresponse has also been found to depend significantly on the device geometry and contacts. Schottky-like contacts to the nanowires can lead to a spatial dependence of the photoresponse, with higher sensitivity near the contacts⁸⁰.

Ge is widely used in bulk and thin film photodetectors, and is extremely valuable in detection of optical communication wavelength of 1550 nm.

However, only sparse literature has shown photoresponse from Ge devices upon only visible illumination^{39, 84}. From the available data, Ge nanowires displayed photocurrent rise and decay kinetics with time constants much longer than bulk Ge, with multiple components ranging from sub-milliseconds to seconds^{39, 84}.

1.3 Synopsis of Dissertation

A concise summary of the research undertaken in the area of nanowire photodetection has been presented in this chapter. With an understanding of this vast field in general and with the motivation for creating a high sensitivity, broad spectrum detector, we may now delve into greater detail the research performed for this work on silicon nanowire phototransistors.

Chapter 2 presents the theory and physical understanding of the behavior of silicon nanowire phototransistors. First a brief review on the basics of photoconductivity is provided. Then an understanding of the physical phenomena leading to the phototransistive behavior of our devices is presented conceptually. This is then elaborated upon through mathematical models, derived from first principles, and followed by computer simulations which incorporate a more rigorous device physics model to determine the important parameters in dictating device behavior.

Chapter 3 details the fabrication methodology for both planar and vertical nanowire structures created through top-down processing. The

benefits of each process are elaborated upon which provide an understanding of how these methods would be viable towards low cost, large area detectors, compatible with traditional fabrication techniques. The advantages of vertical nanowire structures are also shown through electromagnetic computer simulations.

Chapter 4 presents the characterization of the fabricated devices. First, static measurement results at room temperature are shown for determining the amount of responsivity and gain achievable in these devices to ultraviolet and visible illumination. Then spectral measurements are shown and compared with simulated results. Further characterization details the device's behavior with varying temperature, showing ultra high responsivity at low temperatures when dark current is reduced. Lastly, dynamic measurements show the time constants responsible for the high gain observed in the devices and the device's bandwidth.

Chapter 5 provides concluding remarks and reveals areas in which the device performance could be improved. A new device concept is then presented to overcome many of these challenges and simulations are shown to validate the proposed theory.

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Chapter 2

Phototransistive Gain

2.1 Introduction

A few previous studies have been performed to show photoresponse in silicon nanowires¹⁻⁹, but an active investigation into the physics behind such behavior is not prevalent. A physical understanding of these devices is crucial for applying them towards high sensitivity, high resolution imaging. The unique properties of nanowires create new and interesting phenomena greatly beneficial to a photodetector device. In this chapter, we introduce the basic concepts of photoconductivity and how they may be adapted to conceptually understand the characteristics of our nanowire device. We then produce a mathematical model of the device and derive from first principles the phototransistive gain, and the theoretical achievable sensitivity of the device. Lastly, we provide simulations of the photodetector to better define the parameters that determine device behavior which become useful when designing the real structure.

2.2 Basics of Photoconductivity

Before delving into the physics and behavior of the silicon nanowire devices developed in this work, it is helpful to introduce the basics of

photoconductivity in semiconducting materials. Here we present the photoelectric process for conversion of photons into an electrical signal and some of the equations that govern the measurable electrical response in these devices.

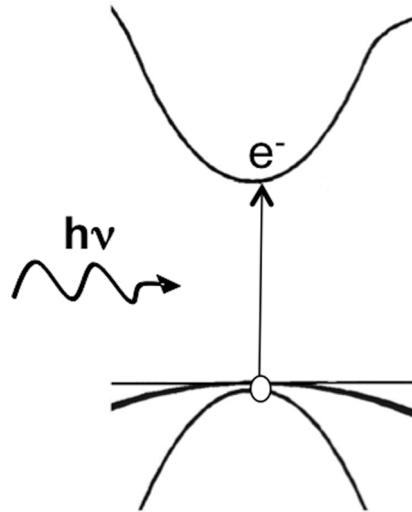


Figure 2.1: Illustration of the photoelectric process in a semiconductor material. A photon is absorbed when it has enough energy to excite an electron from the valence band to the conduction band, leaving behind a hole.

A photon incident on a semiconductor crystal is absorbed when it has enough energy (equal to or above the bandgap energy, E_g , of the material) to break one of the lattice bonds, freeing a valence electron into the conduction band, and leaving behind a hole (Figure 2.1). The amount of light absorption that occurs depends on the thickness of the material and the absorption coefficient of the material at that photon energy and follows an exponential relation given by the Beer-Lambert law as:

$$A = 1 - e^{-\alpha x} \quad (2.1)$$

where A is the percentage of light absorbed, α is the absorption coefficient at that photon energy, and x is the path length of the light. Thus, although most of the light is absorbed closer to the surface of the material, a significant material thickness may be needed for a small absorption coefficient value. The photogenerated carriers are then free to move about the crystal lattice until they recombine, releasing that energy.

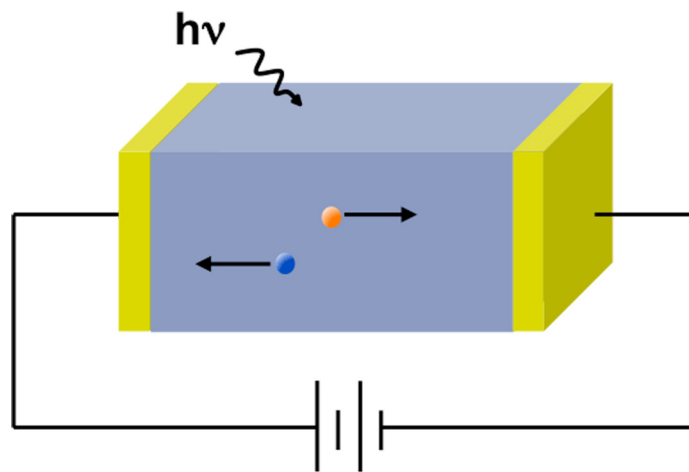


Figure 2.2: Diagram of a photoconductor. Incident light generates excess electrons and holes which under an applied bias create a current in the material.

In a photoconductor device (Figure 2.2), the absorption of light in the semiconductor increases the number of electrons and holes in the material above their initial value:

$$\begin{aligned} n &= n + \Delta n \\ p &= p + \Delta p \end{aligned} \tag{2.2}$$

where n and p are electron and hole concentrations respectively. This in turn increases the conductivity of the material above its initial value:

$$\begin{aligned}\sigma &= e(\mu_n n_0 + \mu_p p_0) + e(\mu_n \Delta n + \mu_p \Delta p) \\ \sigma &= \sigma_0 + \Delta\sigma\end{aligned}\quad (2.3)$$

where σ is the conductivity, e is the electron charge, and μ is the mobility of each type of carrier. Under steady state conditions in which the generation rate, g is constant, the number of excess carriers in the material also does not vary with time and can be written as:

$$\begin{aligned}\frac{\Delta n}{\Delta t} &= g - \frac{\Delta n}{\tau_n} = 0 \\ \Delta n &= g\tau_n\end{aligned}\quad (2.4)$$

Here τ_n is the time it takes for the electron to recombine with a hole. When an electric field, E , is applied across the photoconductor, any free carriers in the material move along the field gradient, generating a current. The photocurrent density, J_{ph} , associated with the excess carriers created from the absorbed light is then:

$$J_{ph} = \Delta\sigma E = e(\mu_n + \mu_p)\Delta n E \quad (2.5)$$

Since the number of generated holes equals generated electrons, the above equation is simplified to an expression with only excess electrons. By rearranging terms, the photocurrent can then be expressed as:

$$J_{ph} = e\Delta n v_d = e\Delta n \frac{L}{t_t} = eLg \frac{\tau_n}{t_t} \quad (2.6)$$

where v_d is the drift velocity, L is the length of material across the contacts, and t_t is the transit time of carriers across the device. From this expression, we can extract the gain of a photoconductor as being the ratio of the recombination lifetime of excess photogenerated minority carrier, in this case electrons, and their transit time¹⁰:

$$G = \frac{\tau_n}{t_t} \quad (2.7)$$

Physically this expression can be interpreted as the number of times a carrier can traverse between the contacts before it recombines. It is interesting to note that as the carriers reach the contacts of the device, they do not simply disappear, but due to the charge neutrality condition, are simply re-injected from the opposite contact. Thus for a photoconductor, the amount of gain the device achieves comes at a price of bandwidth. A large photoconductive gain requires the carriers to produce multiple passes through the device, which decreases the bandwidth.

2.3 Concept of Phototransistive Gain

The above mentioned processes in a photoconductor are of an ideal device in which carriers are freely injected at the truly ohmic contacts, and are unaffected by the semiconductor surface. However for real world devices this is most definitely not the case. Contacts are always seen to create at least a slight barrier, and surfaces are most often riddled with traps and defects,

causing surface recombination which can seriously decrease the gain of photoconductor devices. Therefore in traditional photoconductor devices, passivation of the surface is often a benefit to device performance. However, in our work, we make use of the many defects and states at the surface of a semiconductor to enhance device performance, and exploit the larger surface to volume ratio of nanowires to amplify these effects.

As the dimensions of a semiconductor are reduced, the ratio between surface area and volume increases substantially. In the case of quasi-one-dimensional structures such as nanowires, the reduction occurs in two dimensions, forming very long and thin device structures. With the increase in surface to volume ratio, comes the increasing importance of surface properties to device behavior.

The classification of nanowires encompasses a wide range of device dimensions, but generally is considered to have diameters from only a few nm up to around 200 nm with lengths from 1 μm to 1 mm. At the smallest range of diameters, quantum effects begin to play a major role in device behavior¹¹⁻¹³, leading to many interesting effects. The silicon nanowire structures we have utilized for our photodetectors are at the larger end of the spectrum, taking advantage of the larger surface to volume ratio while not entering the quantum regime. These structures, illustrated in Figure 2.3, consist of diameters between 100 and 200 nm and a length of 4 μm and spaced a few μm apart,

giving a surface to volume ratio of about 10^6 cm^{-1} , substantially larger than that of thin film or bulk devices.

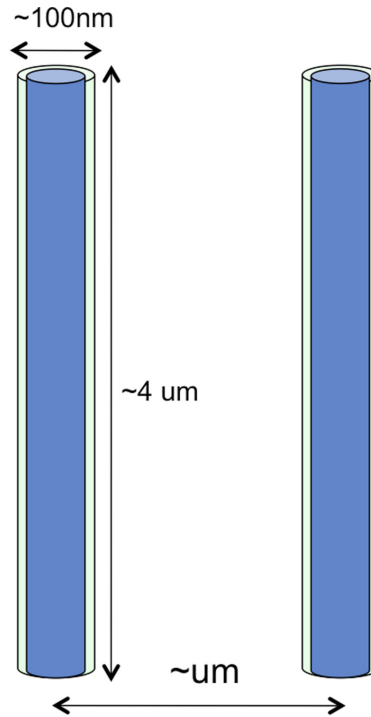


Figure 2.3: Illustration of nanowire dimensions used in our silicon nanowire photodetectors. These structures consist of diameters between 100 to 200 nm, with a length of 4 μm and spacing between 0.5 to 2 μm .

The effect the surface has on a device depends on the surface properties of a given material and any conditioning of the surface that occurs during the processing of the device. Previously, we have demonstrated that ZnO nanowires have a substantial photoresponse due to the role of oxygen desorption at the surface¹⁴. However, in the case of silicon surface states, and in particular the large number of donor (hole trap) states, are the dominating factor in device behavior and lead a phototransistive behavior. At

the silicon surface, surface states are distributed in the energy bandgap including Gaussian shaped distributions with two peaks, one approximately $1/3 E_g$ below the conduction band called acceptor states, and a larger peak $1/3 E_g$ above the valence band called donor states¹⁵⁻¹⁷. Due to their location, acceptor states are often neutrally charged when empty of an electron, and become negatively charged when they trap an electron from the conduction band. Donor states are often neutral when filled with an electron, and positively charged when they are empty (e.g. have trapped a hole from the valence band).

The effect of these surface states that leads to a very substantial photoresponse is diagrammed in Figure 2.4 for the p-type silicon which composes our devices. Due to the surface states, free holes created from the acceptor dopants are trapped at the surface, depleting the silicon of mobile carriers (Figure 2.4a). This causes a radial electric field and band bending between the trapped holes and the fixed dopant atoms which acts much like a gate bias of a transistor. When photons with energy greater than E_g are incident on the nanowire, electron hole pairs are generated in the semiconductor (Figure 2.4b). Due to the band bending, electrons follow the field gradient and are swept to the surface where they recombine with a trapped hole, which in effect modulates the gate bias, while the holes are confined to the center of the nanowire and change the conductivity of the nanowire channel (Figure 2.4c). When an external bias is applied along the

length of the nanowire, a measurable current is produced. Due to the radial potential, the lifetime of holes to become retrapped at the surface (Figure 2.4d) is greatly extended beyond the normal recombination lifetime of a photoconductor.

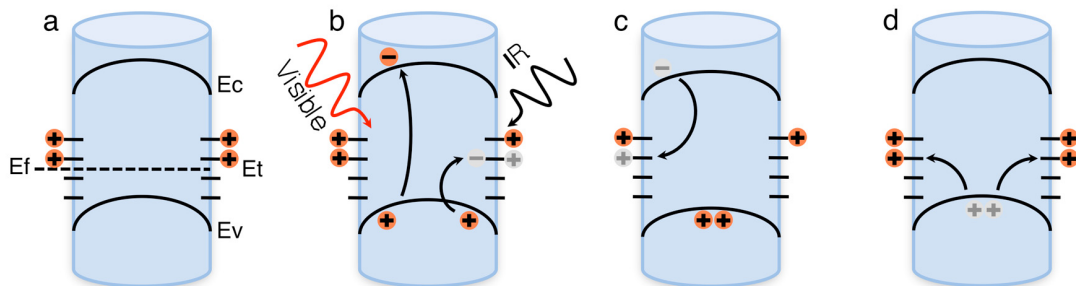


Figure 2.4: Diagram of phototransistive process. (a) Surface states cause mobile carriers to be trapped at the surface, causing the nanowire body to be depleted, a radial electric field, and bandbending. (b) When light is absorbed, electrons and holes are generated. Photons with energy greater than the bandgap will create an electron in the conduction band, while photons with energy less than the bandgap can excite electrons from the valence band into surface states. (c) Electrons in the conduction band are swept to the surface by the potential gradient and recombine with a hole, while holes are confined in the center of the nanowire. (d) After a certain lifetime, the holes overcome the potential barrier with the surface and become trapped at the surface.

It is important to notice another process that can occur in these structures in which these devices can also absorb photons with energy smaller than the bandgap, shown in Figure 2.4b. This work is the main focus of a lab member, Hongkwon Kim, and will only be overviewed here. Due to the presence of the surface states, light having sub-bandgap energy is able to

excite electrons from the valence band into an empty surface state. In a bulk or thin film device, this absorption is usually negligible due to the much smaller surface to volume ratio and the short interaction length between the surface states and normally incident light. However, in our nanowire structures the large number of surface states increases absorption substantially. In addition to this, surface states are bound states, localized in position and thus do not have a well defined momentum. Thus the k-selection rule, normally a factor in band to band transitions, does not apply to the absorption of photons into these states, which greatly increases their absorption cross-section.

2.4 Mathematical Formulation

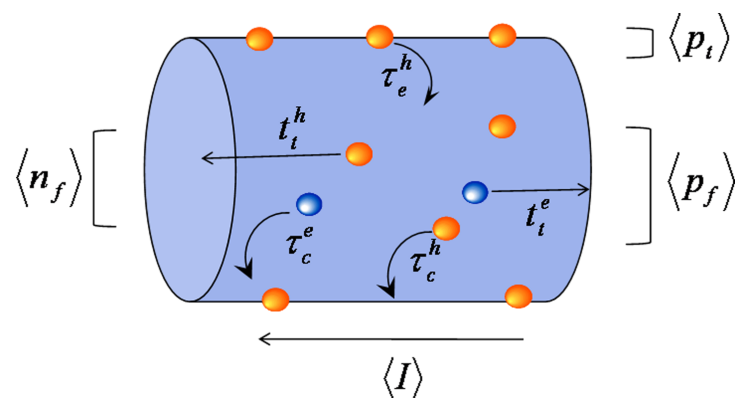


Figure 2.5: Diagram of important terms in a nanowire phototransistor. These terms include: total number of free holes (p_f), free electrons (n_f), and trapped holes (p_t), capture time by a surface state for holes (τ_c^h) and electrons (τ_c^e), hole escape time (τ_e^h), and the transit times for holes (t_t^h) and electrons (t_t^e).

The previous section gives a conceptual overview of the processes occurring within the nanowire photodetector leading to a high gain. Here we present a more formal mathematical derivation starting from first principles to develop the photocurrent and gain terms. The important terms in the derivation are shown in Figure 2.5.

To begin, we start with a definition of steady state, or time averaged electrical current $\langle I \rangle$ where the $\langle \rangle$ indicate time averaging:

$$\langle I \rangle = \frac{e \langle p_f \rangle}{t_t^h} + \frac{e \langle n_f \rangle}{t_t^e} \quad (2.8)$$

Here t_t^h and t_t^e are the transit times for holes and electrons, and p_f and n_f are the total number of free holes and electrons in the material. Next we introduce the rate equations for changes in the hole and electron numbers:

$$\begin{aligned} \frac{d}{dt} \langle p_f \rangle &= -\frac{\langle p_f \rangle}{\tau_c^h} + \frac{\langle p_t \rangle}{\tau_e^h} + \left[g_{th} + \eta_{QE} \frac{P_{opt}}{h\nu} \right] = -\frac{\langle p_f \rangle}{\tau_c^h} + \frac{\langle p_t \rangle}{\tau_e^h} + g_{tot} \\ \frac{d}{dt} \langle p_t \rangle &= \frac{\langle p_f \rangle}{\tau_c^h} - \frac{\langle p_t \rangle}{\tau_e^h} - \frac{\langle n_f \rangle}{\tau_c^e} \\ \frac{d}{dt} \langle n_f \rangle &= -\frac{\langle n_f \rangle}{\tau_c^e} + g_{tot} \end{aligned} \quad (2.9)$$

where p_t is the number of trapped holes, τ_c^h and τ_c^e are the capture times of the holes and electrons, τ_e^h is the hole escape time, η_{QE} is the quantum efficiency, P_{opt} is the optical power incident on the material, $h\nu$ is the photon energy, g_{th} is the thermal generation rate, and g_{tot} is the total generation rate

from both thermal and optical processes. These equations list out all the possible factors which result in a change in the number of free and trapped holes and free electrons. Thus the factors which change the number of free holes include a decrease in number when free holes are trapped in surface states, an increase when trapped holes escape surface states, and any generated holes from either thermal or optical processes, where the conversion of a photon into an electron/hole pair is determined by the quantum efficiency, total power incident, and the photon energy. Likewise, the number of trapped holes increases when free holes are trapped at the surface, decreases when trapped holes escape, and also decreases when free electrons are captured, causing recombination of the electron/hole pair. Free electron numbers change when electrons are generated through thermal or optical processes, and decreases when they are captured at the surface. Note that we did not include a rate equation for trapped electrons, as any electron at the surface will instantly recombine with one of the many trapped holes. Under steady state conditions, all above rate equations must be zero:

$$d\langle p_f \rangle / dt = d\langle p_t \rangle / dt = d\langle n_f \rangle / dt = 0 \quad (2.10)$$

The steady state concentrations may then be found and put into the original current equation (2.8) to find:

$$\langle I \rangle = \frac{e\tau_c^h \langle p_t \rangle}{t_t^h \tau_e^h} + \frac{e\tau_c^h g_{tot}}{t_t^h} + \frac{e\tau_c^e g_{tot}}{t_t^e} \approx e \frac{\tau_c^h}{t_t^h} \left(\frac{\langle p_t \rangle}{\tau_e^h} + g_{tot} \right) \quad (2.11)$$

Here a simplification is taken by noting that the capture time of electrons is much shorter than holes since in the former case, the potential gradient sweeps the electrons to the surface while in the latter case the potential creates a barrier for holes to become trapped. From this equation we can see that the total current is dependent on the number of carriers in the channel from holes that escape the surface states and the total generation rate from thermal and optical processes, all of which is amplified by the amount τ_c^h/t_t^h . This term we define as the steady state phototransistive gain, written out formally as:

$$G_{dc} = \frac{\tau_c^h}{t_t^h} \quad (2.12)$$

This term looks surprisingly like that of a photoconductor with one important difference: for the phototransistor, the time constant in the numerator is now the capture time of the majority carrier, in this case holes, not the minority carrier recombination lifetime in a photoconductor. This important quality demonstrates that when designed properly, the gain of the phototransistor can be substantially higher than a photoconductor. To obtain an idea of the magnitude of this value, we can estimate that for a device with a typical transit time of ~ 100 ps, and a hole capture time of ~ 100 μ s, the steady state gain would be on the order of 10^6 . The substantial amount of gain in such a device holds great promise for detecting very low photon numbers.

To formulate this further, we can mathematically derive the response of this structure to the absorption of a single photon. To do this, we start with the rate equations seen earlier in equation (2.9), but with an additional impulse term with the magnitude of one, signifying the creating of a single electron/hole pair at time $t=0$:

$$\begin{aligned}
 \frac{d}{dt}\langle p_f \rangle &= -\frac{\langle p_f \rangle}{\tau_c^h} + \frac{\langle p_t \rangle}{\tau_e^h} + g_{tot} + \delta(t) \\
 \frac{d}{dt}\langle p_t \rangle &= \frac{\langle p_f \rangle}{\tau_c^h} - \frac{\langle p_t \rangle}{\tau_e^h} - \frac{\langle n_f \rangle}{\tau_c^e} \\
 \frac{d}{dt}\langle n_f \rangle &= -\frac{\langle n_f \rangle}{\tau_c^e} + g_{tot} + \delta(t)
 \end{aligned} \tag{2.13}$$

To solve for the time dependent solutions, we must take the Laplace transform to linearize the set of differential equations:

$$\begin{aligned}
 sP_f(s) - P_f(0) &= \frac{-P_f(s)}{\tau_c^h} + \frac{P_t(s)}{\tau_e^h} + \frac{g_{tot}}{s} + 1 \\
 sP_t(s) - P_t(0) &= \frac{P_f(s)}{\tau_c^h} - \frac{P_t(s)}{\tau_e^h} - \frac{N_f(s)}{\tau_c^e} \\
 sN_f(s) - N_f(0) &= \frac{-N_f(s)}{\tau_c^e} + \frac{g_{tot}}{s} + 1
 \end{aligned} \tag{2.14}$$

This set of equations can then be solved algebraically with the following reasonable assumptions: the electron capture time is fast ($|\tau_c^e s| \ll 1$), the hole emission time is slow ($|\tau_c^h s| \gg 1$), there are many trapped holes at the surface ($P_t(0) \gg 1$), and the number trapped holes is greater than the free electrons

($P_t(0) \gg N_f(0)$). Solving the set of equations and taking the inverse transform yields:

$$\begin{aligned}\langle p_t(t) \rangle &\approx \langle p_t(0) \rangle \\ \langle p_f(t) \rangle &\approx \langle p_f(0) \rangle + e^{-t/\tau_c^h}\end{aligned}\quad (2.15)$$

We see that following a single carrier generation event, the average number of trapped holes does not significantly differ from the initial value, and that the number of free holes averaged over many events shows an exponential decay with a time constant of the hole capture lifetime. These values can then be used to find the change in current as:

$$\langle \Delta I(t) \rangle = \frac{e}{t_t^h} (\langle p_f(t) \rangle - \langle p_f(0) \rangle) = \frac{e}{t_t^h} e^{-t/\tau_c^h} \quad (2.16)$$

In any measurement system, it is not the instantaneous current that is measured. Any system will have a limited bandwidth and will output an integrated signal. Thus the measured change in current is:

$$\langle \Delta I \rangle = \frac{e}{t_t^h} \frac{\int_0^T e^{-t/\tau_c^h} dt}{T} = \frac{e\tau_c^h}{t_t^h T} \left(1 - e^{-T/\tau_c^h}\right) \approx \begin{cases} \frac{e\tau_c^h}{t_t^h T} & \text{for } T \gg \tau_c^h \\ \frac{e}{t_t^h} & \text{for } T \ll \tau_c^h \end{cases} \quad (2.17)$$

where we have integrated the current signal for a period of T. We can see that this expression can be simplified for two domains. When the integration time is much greater than the hole capture time constant, the signal amplitude depends inversely on T. Thus for a very long integration time, the signal becomes very weak. When the integration time is much shorter than the hole

capture time, the result is a constant, only dependent on the hole transit time. A compromise must therefore be found to find the integration time that leads to the largest detectable signal. To obtain an idea of this value, we first need to consider the intrinsic noise of the detector. In general, the major noise sources of a device are excess noise, thermal noise, shot noise, and generation-recombination (GR) noise. For our high impedance device, the GR and shot noise are the dominating factors and can be expressed as:

$$\langle I^2 \rangle = \frac{2eIB(\tau_c^h/t_t^h)}{1 + (2\pi B\tau_c^h)^2} + 2eIB \quad (2.18)$$

where the bandwidth is $B = 1/2T$. This noise expression is modified from the traditional GR expression¹⁸ by a change in coefficients from 4 to 2, since our device is a single carrier device. Thus, the signal to noise (S/N) ratio is:

$$\frac{S}{N} = \frac{\langle \Delta I \rangle^2}{\langle I^2 \rangle} = \frac{\left(\frac{e\tau_c^h}{t_t^h T} (1 - e^{-T/\tau_c^h}) \right)^2}{\frac{2eIB(\tau_c^h/t_t^h)}{1 + (2\pi B\tau_c^h)^2} + 2eIB} \quad (2.19)$$

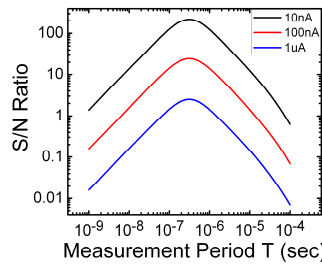


Figure 2.6: Plot of S/N ratio for single photon detection limit. Plot generated from equation (2.19) in Matlab with $\tau_c^h=100 \mu\text{s}$ and $t_t=100 \text{ps}$ at various dark currents.

This function is plotted in Figure 2.6 using a hole capture time of $100 \mu\text{s}$ and transit time of 100ps at various dark current levels, and the S/N ratio is found to be large enough to detect a signal when the integration time T is comparable to τ_c^h . The S/N ratio is found to depend heavily on the dark current of the device, since the dark current can be a significant noise source. Thus it is theoretically possible to detect single photon resolution in these nanowire devices, provided that the nanowire is fully depleted, the dark current is small, and the external noise of the system is kept to a minimum.

2.5 Device Modeling

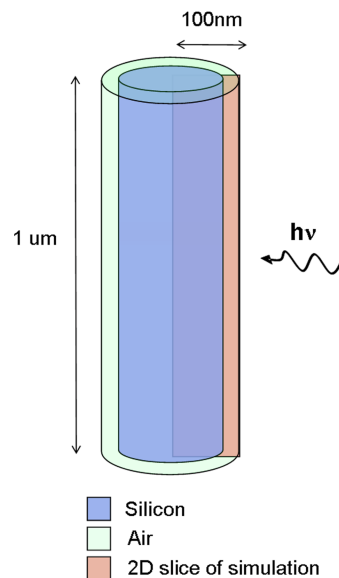


Figure 2.7: Diagram of structure simulated in Silvaco. The device consists of a uniformly doped p-type silicon (blue), surrounded by air (green). Surface states are defined at the silicon/air interface and light input from the side. A pseudo-3D simulation is performed by taking a radial slice (pink) and integrating around the nanowire. Device dimensions are: 100 nm in radius and $1 \mu\text{m}$ in length.

The mathematical modeling formulated in the previous section is important for understanding the significant terms in determining device performance, and the foundation for expressing device metrics. However, to effectively design and engineer preferential device properties, the dependences of device behavior on the various design parameters must be determined. These parameters are namely the nanowire doping concentration (N_a), diameter (d) and surface state density (N_{gd}). A critical balance between these variables is needed for maximizing the phototransistive gain, while minimizing the dark current.

To verify our conceptual model presented earlier and determine how various parameters affect device behavior, silicon nanowire structures have been simulated using a device modeling software, Silvaco. This allows for a rigorous model, incorporating a large quantity of device physics, to provide a more accurate view inside the device. The simulated structure, shown in Figure 2.7 consists of a uniformly doped p-type Si nanowire with varying surface state density, doping concentration, and illumination intensity. The nanowire consists of a 100 nm radius and 1 μm in length with uniform illumination along the side. Surface states, illustrated in Figure 2.8 are distributed along the bandgap of Si following a general model of the silicon surface¹⁵⁻¹⁷ with an donor peak three times greater than the acceptor peak. Ohmic contacts to the ends of the wire are used to bias the wire at 1 V. A

pseudo-3D simulation is performed by taking a radial slice of the nanowire and integrating around the body of the wire.

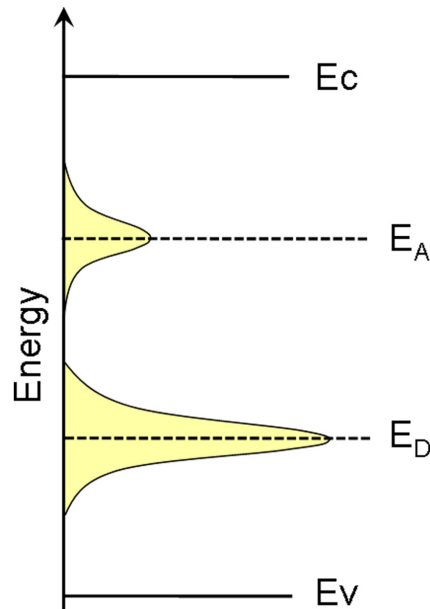


Figure 2.8: Illustration of surface state distribution in simulated nanowire structure. The states consists of two Gaussian curves located at 0.4 eV above and below the valence band and conduction band respectively for donor and acceptor states with a full width half maximum of 0.1665 eV. The donor peak is three times greater than the acceptor peak.

The results of the simulations are seen to validate the conceptual model presented earlier of the processes leading to large phototransistive gain. Through the use of Silvaco, we are able to numerically visualize the parameters discussed in the previous section. Figure 2.9a shows the hole and electron concentration for a simulation with a p-doping concentration of $4 \times 10^{16} \text{ cm}^{-3}$ and a surface state density of $5 \times 10^{10} \text{ cm}^{-2}$ in which we can see the depletion of the nanowire extending from the surface into the body. This leads

to an electric field, shown in Figure 2.9b, between those charges trapped at the surface and the ionized impurities, thus creating a barrier for any additional optically generated holes.

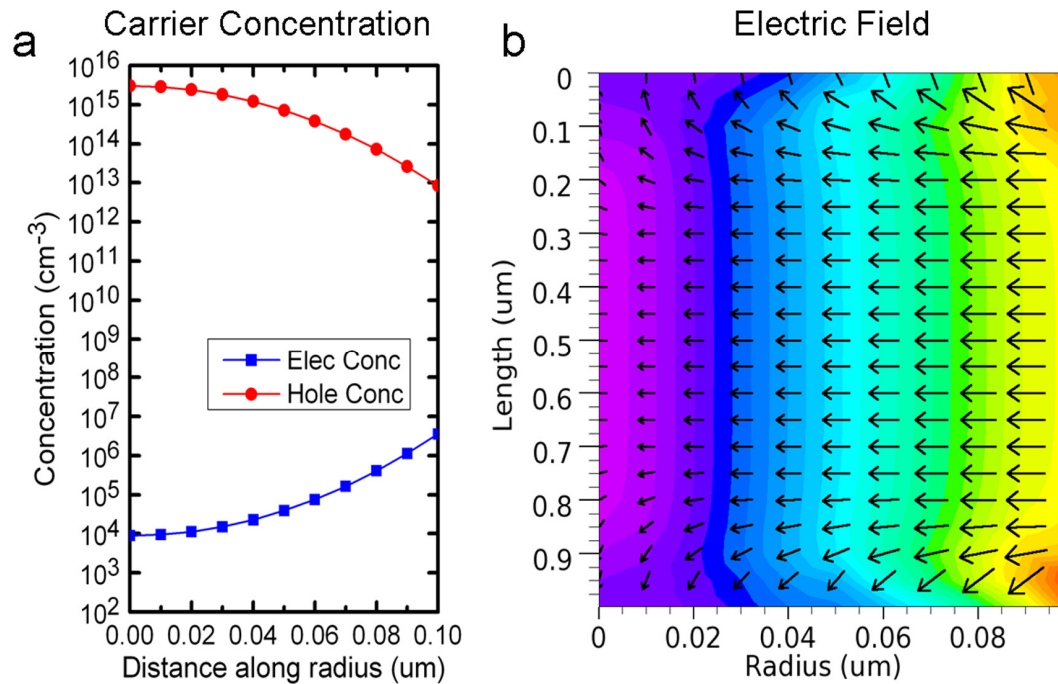


Figure 2.9: Carrier concentration and electric field along the radius of a nanowire phototransistor. Simulated structure has doping of $4 \times 10^{16} \text{ cm}^{-3}$ and surface state density of $5 \times 10^{10} \text{ cm}^{-2}$. (a) Carrier concentration shows depletion due to surface states extending to the center of the wire. (b) Electric field between trapped holes and ionized impurities lead to the built in radial gate bias. Arrows show the direction of the electric field and arrow length and warmer colors indicate increasing magnitude of electric field.

The magnitude of this barrier depends greatly on the ratio between surface state density, surface to volume ratio, and doping concentration. Figure 2.10 shows how this barrier varies when holding both the radius (e.g. surface to volume ratio) and surface state density constant. At low doping

concentrations, the surface states are able to fully deplete the nanowire, but due to the few number of impurities within the nanowire, the electric field and therefore band bending is minimal. As the doping increases, more holes are trapped at the surface which leads to an increase in the built in gate bias. However, beyond a certain limit, the surface states become saturated, and are unable to trap additional ionized holes, and the nanowire becomes undepleted. This also tends to reduce the barrier as the depletion width significantly decreases.

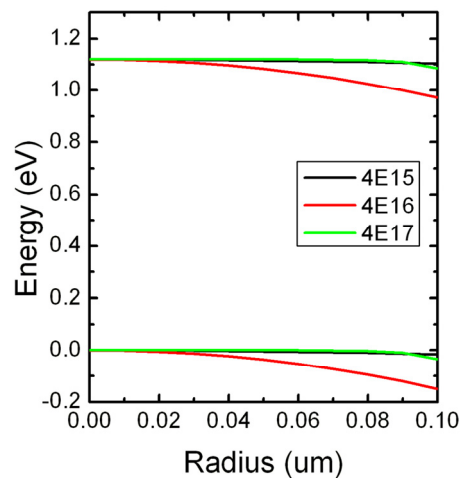


Figure 2.10: Diagram of band structure along a radial slice of nanowire with varying doping concentration. The surface state density is held constant at $5 \times 10^{10} \text{ cm}^{-2}$. Low and high doping concentrations lead to a minimal barrier, while a certain doping concentration, corresponding to the maximum number of ionized holes that are able to be trapped by the given surface states, will lead to the maximum amount of band bending.

The interplay between the three different parameters directly impacts the nanowire's phototransistive gain. Figure 2.11 summarizes the amount of

gain achievable while changing two of these parameters: doping concentration and surface state density. The curves show that for each given surface state density, there is a doping that leads to the highest gain due to the conditions expressed earlier. Furthermore, the ratio between surface state density to doping at the highest gain remains constant. As seen from the curves, an increase in N_{gd} also shifts the peak doping concentration by the same amount. A third phenomenon shown in these curves is that the peak gain increases with increasing surface state density. This arises due to the increase in radial bandbending and electric field at higher surface state densities. Larger surface state densities allow for the capture of more majority carriers which increases the barrier for holes to overcome before being retrapped at the surface.

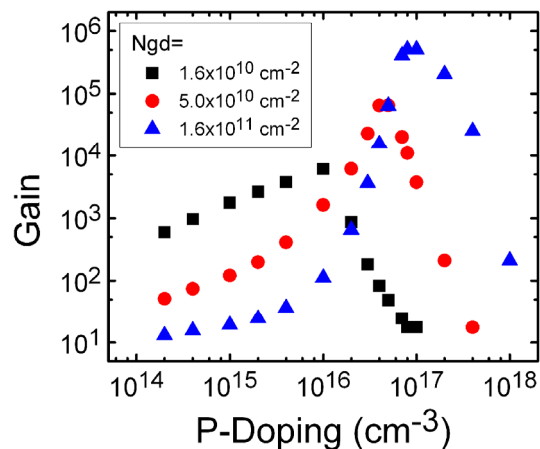


Figure 2.11: Simulation results of gain vs. nanowire doping with varying surface state density. Nanowire structure is 100 nm in radius. Each curve shows a certain ratio of doping and surface state density which leads to highest gain. This ratio stays roughly constant as seen by the shift in doping concentration leading to highest gain when the surface state density is varied.

The dependence of gain on illumination intensity has also been characterized through simulations. As shown in Figure 2.12, the gain for a given structure is constant at low illumination intensities and decays above a certain threshold. At low illumination intensities, the photogenerated carriers do not significantly deviate from thermal equilibrium and do not greatly affect the population of trapped carriers at the surface. However as the photogeneration rate increases, the number of holes confined to the center of the nanowire increase the potential and reduce the energy barrier while the electrons that recombine at the surface empty a significant number of surface states. This has the effect of drastically reducing the hole lifetime which lowers the gain.

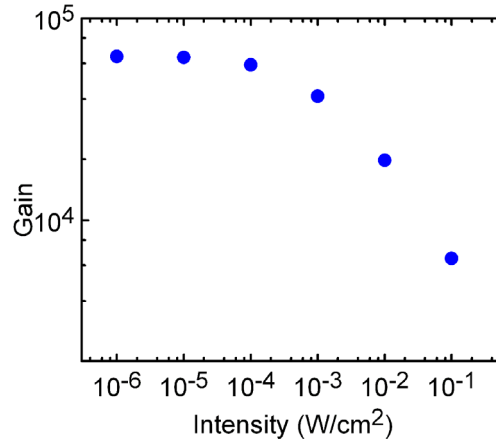


Figure 2.12: Simulation results of gain vs. intensity. Simulated structure consists of nanowire doping of $4 \times 10^{16} \text{ cm}^{-3}$, and surface state density of $5 \times 10^{10} \text{ cm}^{-2}$.

2.6 Conclusion

As we have shown, the scaling of traditional photoconductors from large bulk devices to quasi-one-dimensional nanowire structures creates new and interesting physical phenomena which, when engineered correctly, can lead to greatly improved photodetector behavior. Namely, by scaling the photoconductor down to nanowire dimensions, the surface interactions with the body of the nanowire dominate the characteristics of the device and in effect create a phototransistor. By designing the doping, diameter and surface state density correctly, this interaction can lead to a very large phototransistive gain. With this idea in hand, we may now discuss the fabrication of working silicon nanowire phototransistors and characterization of their device behavior.

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Portions of this chapter have been published in the Proceedings of SPIE 2010. Zhang, Arthur; Cheng, James; Kim, Hongkwon; Liu, Yisi; Lo, Yu-Hwa, SPIE, 2010. The dissertation author was the primary investigator and author of this paper.

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Chapter 3

Device Fabrication

3.1 Introduction

As devices scale into the nanowire regime, extensive research has also been undertaken to discover new fabrication methods to create such small structures. Traditionally there are two fabrication methods employed by those making nanowire devices: bottom-up growth and top-down etching, each with its benefits and disadvantages. The bottom up approach entails the chemical formation of nanowires through introduction of gases comprised of its constituent materials¹⁻⁵, and has shown some major advances in the control of nanowire geometry and placement⁶⁻⁹. This method also allows for the creation of nanowires of many different materials on various substrates, and thus a very important research tool. However, thus far this method does not generally allow for the fabrication of scalable, large area detectors suitable for commercial applications.

Due to this restriction we chose to fabricate our silicon nanowire photodetectors using the top-down approach. Nanowires fabricated in this fashion are now becoming more prevalent in the literature¹⁰⁻¹². The top-down approach utilizes lithographic patterning and etching, both very established elements in commercial fabrication processes. This allows for precise

placement, fine definition of geometry and traditional doping techniques for creating homojunction structures.

For this work, we use traditional and novel lithography techniques with advanced etching processes, which allow for both research and potentially commercial large area detectors to be fabricated. This chapter details the fabrication methods we utilized for creating both planar and vertically standing nanowire phototransistors from single wires to large area arrays. These devices were fabricated in the Nano3 Cleanroom facility of Calit2 at U.C. San Diego.

3.2 Planar Device Fabrication

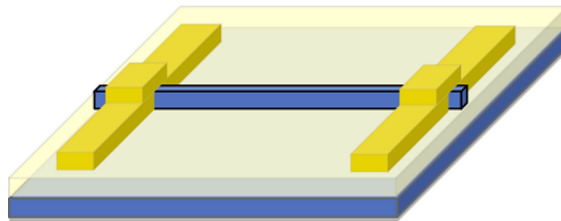


Figure 3.1: Diagram of planar nanowire phototransistor structure. Silicon nanowire (blue) on top of insulating silicon dioxide (cream), contacted at ends with metal (gold).

The initial investigation into the device properties of silicon nanowire phototransistors was done with planary oriented devices. Figure 3.1 shows a diagram of the device with a nanowire on top of an insulating silicon dioxide layer, contacted at either ends. The techniques for fabricating these devices

were simple and quick to realize a fast turn around time for measuring device behavior and obtain a baseline for further research. The fabrication of these devices contains all traditional fabrication techniques from UV photolithography, to thermal oxidation and wet etching on a standard silicon on insulator (SOI) wafer.

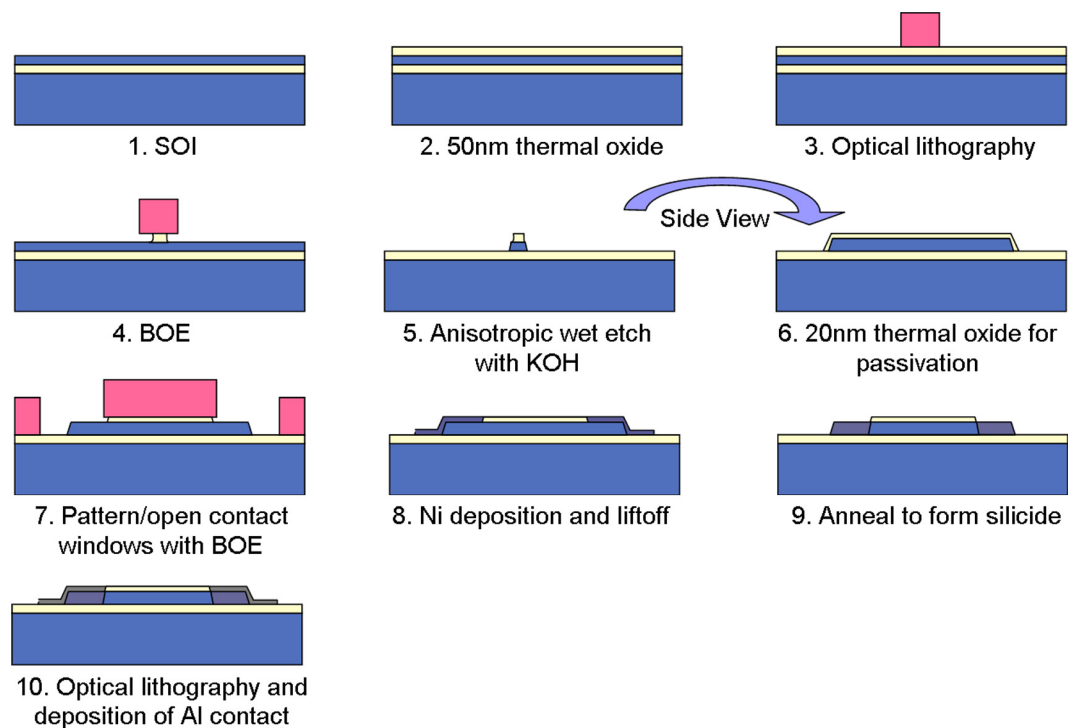


Figure 3.2: Process flow for planar silicon nanowire phototransistors. Materials are: silicon (blue), silicon dioxide (cream), photoresist (pink), nickel (purple), aluminum (gray).

The process flow for fabricating these devices is shown in Figure 3.2. We begin with an SOI wafer with a (100) oriented p-doped device layer with a doping concentration of $\sim 10^{15} \text{ cm}^{-3}$, and a thickness of 230 nm. This sits on top of a buried oxide layer of 380 nm in thickness. A thermal oxide is grown

on the device layer 50 nm in thickness to act as the etch mask for nanowire formation. Photolithography is then used to pattern large nanowire lines into Shipley 1805 positive photoresist. These lines vary in width from 1.2 μm to 2.4 μm in increments of 200 nm. Traditional photolithography cannot resolve the small dimensions of the nanowire diameters, and thus a range of larger widths are used which will then be narrowed. The photoresist mask is then converted into the thermally grown oxide mask through an isotropic wet etch of buffered oxide etch (BOE). By controlling the etch time of this step, we are able to undercut the photoresist pattern, narrowing the pattern until the thinnest photoresist lines are lifted off of the surface. When this occurs, the next narrowest pattern will have a diameter of ~ 200 nm. The range of varying photoresist lines allows for some tolerance in this step, thus allowing for a range of diameters to be easily produced. Once the pattern is converted into the oxide, the device layer is again wet etched with the buried oxide acting as an etch stop, this time using an anisotropic etchant of KOH. This solution preferentially etches along the (110) crystal plane, and very slowly along the (111) plane of silicon, giving the device a trapezoidal shape. The oxide etch mask is then removed using BOE, and a new 20 nm thick thermal oxide is grown to uniformly cover the nanowire. Photolithography is then used to pattern contact areas onto the ends of the nanowire using NR9-1500PY negative photoresist. The oxide is removed from these contact areas using BOE, and 60 nm of Ni is evaporated over the surface and the photoresist

removed using acetone taking with it, the Ni over unwanted areas. The remaining Ni over the contact areas is annealed at 650 °C in 90%:10% N₂:H₂ forming gas for 5 minutes which creates NiSi nickel silicide. The remaining Ni is then removed using Transene TFB metal etchant. Finally, large contact fingers and pads are patterned using photolithography (NR-9), and Al is evaporated, and lifted off. Images of the final structures are shown in Figure 3.3 for a single nanowire and nanowire arrays. The spacing between fingers is varied from 1 μm to 20 μm.

The major challenge when creating these devices is producing ohmic contacts on either nanowire end. The formation of NiSi produces a noticeable barrier with the low doped nanowire body. The Al contacts on top of this stack also produces asymmetries in IV characteristics from any misalignment of the contact onto the low doped nanowire body, which creates a Schottky contact.

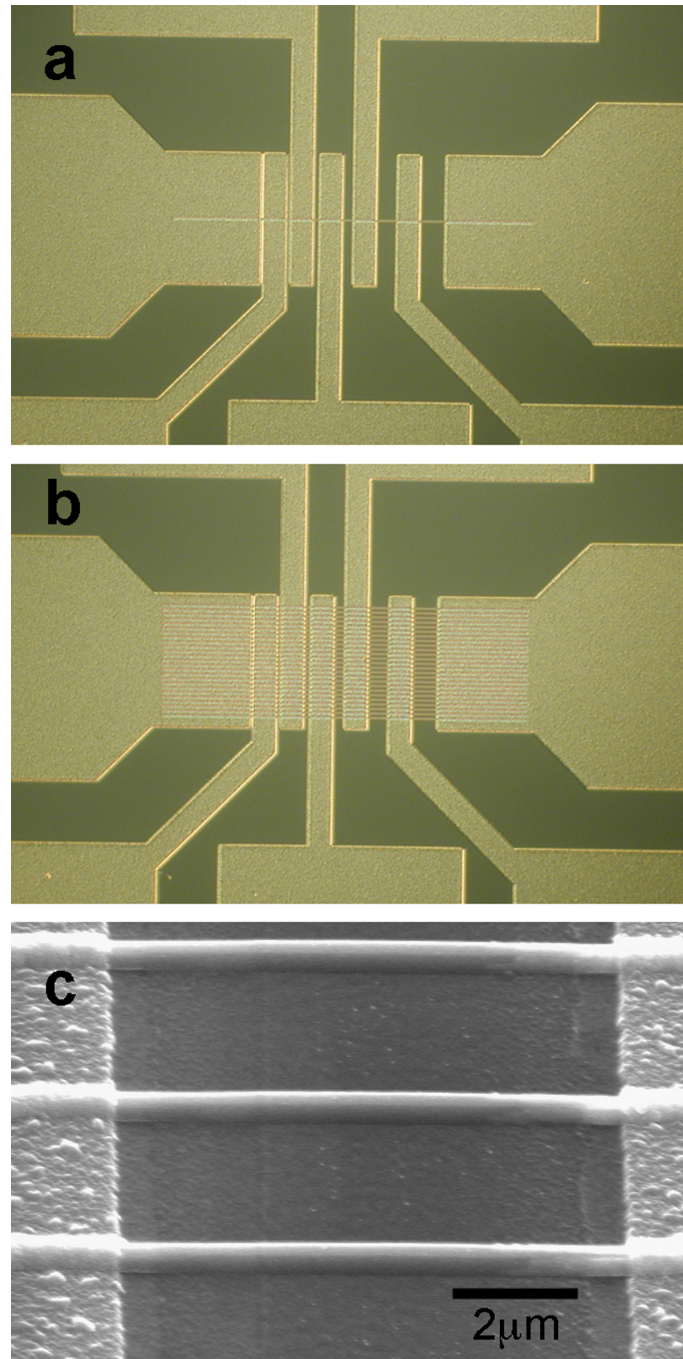


Figure 3.3: Images of fabricated planar silicon nanowire phototransistors. (a) Optical photo of single nanowire devices with multiple electrode spacing. (b) Optical photo of 25 nanowire devices. (c) Scanning electron microscope image of nanowires in a finished device.

3.3 Vertical Device Fabrication

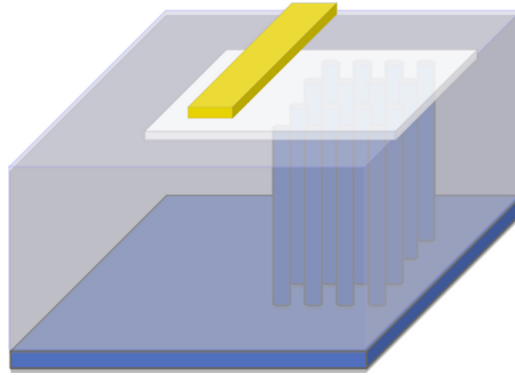


Figure 3.4: Diagram of vertical nanowire phototransistor structure. Silicon nanowires (blue) are embedded in dielectric (gray), with a top transparent contact (white) and metal contact finger (gold).

Planar devices fabricated using the method described previously are able to quickly prove the device concept and demonstrate high phototransistive gain, but are impractical in real world applications due to their extremely low external quantum efficiency to light incident perpendicular to the surface. In that scenario, the nanowire footprint is very small, and much of the light is lost in areas around the nanowire, and on the contacts. Due to the planar orientation of the nanowires, the absorption depth for light incident on the nanowires is also low, since the light only has a path length equal to the thickness of the wire.

By moving to a vertical structure diagrammed in Figure 3.4, the external quantum efficiency can be greatly improved in both regards. By standing the nanowires vertically, along the axis of light propagation, the path length for

light becomes extended to a few microns, greatly enhancing the amount of energy absorbed. Although in the vertical geometry the footprint of the nanowires is even smaller and thus one would expect more light to be wasted in areas without nanowires, we have demonstrated through simulations that this geometry actually leads to enhanced absorption stemming from a funneling effect of radiation surrounding the nanowire much like that of a waveguide. These two advantages motivate the fabrication of the more complex vertical structures. Here we take advantage of advanced technologies for device fabrication. For the initial research phase of this device, we pattern the nanowires using e-beam lithography, and subsequently move to nanoimprint lithography (NIL). NIL is a maturing technology that allows for very fast parallel printing of nanosized patterns. Nanowires are then formed from the printed samples using highly anisotropic plasma etching allowing for aspect ratios of 1:20 to be created. The following subsections discuss in detail the physics behind enhanced absorption in vertical structures and their fabrication methodologies. Both $p^+/p^-/p^+$, and $p^+/n^-/n^+$ structured devices were created in this geometry which allows for a more accurate determination of the device's phototransistive gain.

3.3.1 Enhanced Absorption

Although the small diameter of nanowires is responsible for producing the phototransistive effect and high gain, it also produces a very small footprint

which traditionally would lead to very low external quantum efficiency. In vertical structures, the photosensitive nanowire area is only a small fraction of the total pixel exposed to incident light. In our devices, the photosensitive area approaches zero for light normally incident on the substrate as the devices are capped with metal as a contact. Thus, one would expect only very small photoresponse due to light absorbed from scattering from surfaces or slight orientation differences from normal incidence. However, the properties of nanowires are again responsible for producing enhancements to device performance which overcome this barrier. Due to the high contrast in index of refraction of the nanowire material to the surrounding medium, the device behaves similarly to a step index waveguide in which light in the cladding material is coupled into the high index waveguide causing large absorption enhancements to light incident surrounding the nanowires.

This effect is demonstrated in our nanowire structures through simulations using the Comsol Multiphysics tool. A 3-dimensional structure is created in which a 200 nm diameter, 2 μm length nanowire is embedded in a lossless polymer. The side and bottom boundaries of the simulation are perfectly reflecting and thus create a periodic structure, simulating an infinite array. The pitch, or nanowire center to center spacing, is changed by increasing the lateral dimensions of the boundaries. Light of 350 nm wavelength is input into the top boundary surrounding the nanowire, with no light incident directly above the nanowire to more accurately reflect our

structure. The material properties are inputted as a complex index of refraction for the given inputted wavelength with silicon being $\tilde{n} = 5.43 + 3.15i$, and a typical lossless polymer of $\tilde{n} = 1.6$. The high contrast of the real part of the index between silicon and the lossless polymer is responsible for the confinement of light within the nanowire, while the large imaginary component of the index is responsible for the strong absorption of any energy within the nanowire. These two effects coupled together lead to the large absorption enhancement in vertical structures. To quantify the enhancement, an electromagnetism add-on is used to solve the set of physical equations pertaining to the energy distribution of the multidimensional problem.

The results of these simulations are shown in Figure 3.5. Figure 3.5a shows a visual representation of energy distribution for a steady state solution in which the material absorption in silicon is removed. The energy which is initially completely located outside the nanowire is shown to be largely located within the nanowire body. The amount of energy absorbed for a given nanowire pitch is shown in Figure 3.5b. As seen in the plot, for small pitches, the energy confinement within the nanowire approaches 100%, and remains high as the pitch increases, while the actual footprint of the nanowire quickly drops to zero. Thus even for large nanowire pitches, which is useful for lowering the dark current, the amount of light absorbed can still be substantial. The amount of absorption enhancement can be quantified as the ratio of energy confined to physical footprint and shown in Figure 3.5c. This

enhancement grows as the pitch quickly decays and reaches levels approaching 40 times that of the footprint. Through this effect, the barrier of low external quantum efficiency can be overcome with vertically oriented nanowire devices.

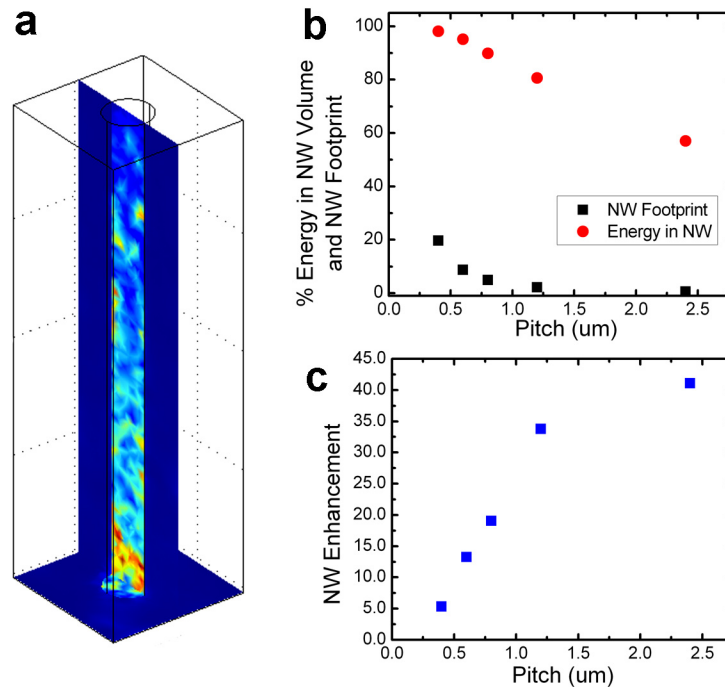


Figure 3.5: Simulation results of absorption enhancement in vertical nanowire structures. (a) Visual result of energy confinement within nanowires. Warmer colors represent higher energy concentration. (b) Percentage of total inputted energy confined within nanowire at varying pitches, and for comparison, the nanowire footprint per pixel. (c) Absorption enhancement in nanowires above the nanowire footprint.

3.3.2 Fabrication Methodology

Vertically standing nanowire devices are formed by a top-down process of lithographic patterning and dry etching shown in Figure 3.6. The starting substrates consist of p^-/p^+ or n^-/n^+ epitaxial silicon wafers. The $4\ \mu\text{m}$ p^- or n^-

device layer has a resistivity of 10 ohm-cm and the substrate of 0.01 ohm-cm used as the source/drain region. Boron is diffused into the wafer at 950 °C for 1 hour resulting in 0.3 μm p^{++} diffused layer to create the top contact region. The layer thickness was characterized through simulations in Silvaco's Athena tool, and 4 point probe measurements on the diffused substrate. The wafer is then patterned using either ebeam lithography or nanoimprint lithography to form a pattern with diameters between 100 and 200 nm with varying pitch and 70 nm of Ni is deposited as both the nanowire etch mask and self aligned contact. Extraneous Ni dots are removed to form the device areas using photolithography and wet etch. The nanowires are then formed through a highly anisotropic reactive ion and inductively coupled plasma dry etch of silicon with C_4F_8 and SF_6 gases to 4 μm in thickness. Precise control of the ratio between these gases is needed to form vertical etch profiles. An increase in C_4F_8 to SF_6 yields a positive profile and more cone shaped nanowires, while a decrease in this ratio results in a tapered nanowire base, and in the extreme case results the collapse of the structures. The contacts are then annealed to form Ni silicide at the top drain electrodes for 30 s at 650 °C in an RTA under 10% $\text{N}_2:\text{H}_2$ forming gas.

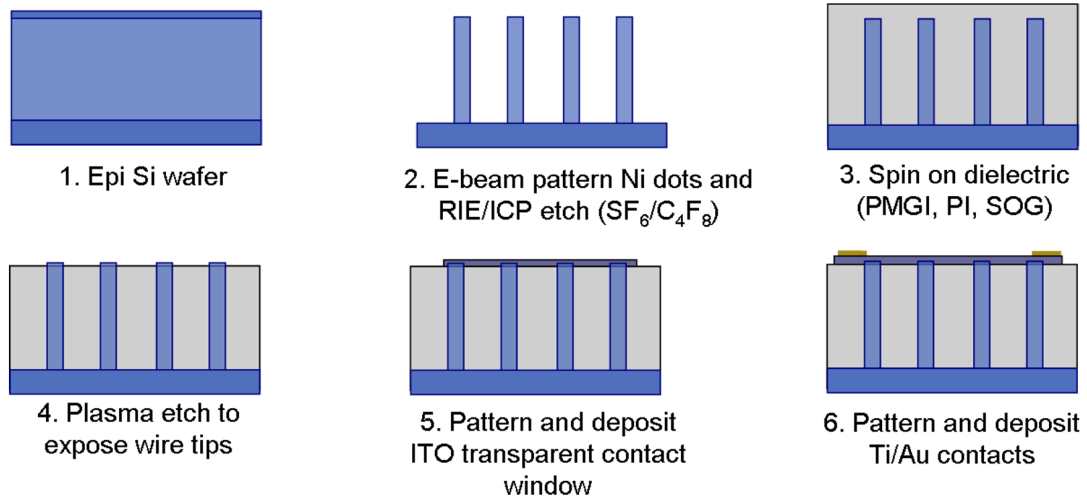


Figure 3.6: Process flow for vertical silicon nanowire phototransistors. Materials are: silicon (blue), dielectric (gray), ITO (dark gray), metal contact (gold).

The nanowires are then embedded in a spin on dielectric. One of most difficult aspects of device fabrication is finding suitable dielectrics for nanowire support. Ideally this insulator needs to be thermally matched to the nanowire material. It must also be process compatible: it must be able to fill between nanowires to act as support, be etched with a high selectivity to silicon, and be solvent compatible. Lastly, it must be transparent to the wavelengths of interest. For a broadband detector, this encompasses wavelengths from the ultraviolet 350 nm, to the near infrared 2 μm range. A large number of spin on dielectrics were investigated for this use as they can flow into the crevices between wires. The first of these was polymethylglutarimide (PMGI). This polymer resist is transparent to the wavelengths of interest and easily etched, but was not stable under exposure to solvents, even after curing. Thus the

fabricated devices had poor morphology and low yield. The devices tested under UV exposure use this polymer as the supporting material. We then investigated spin on glass (SOG). This material is both transparent and solvent compatible, but due to the large thermal mismatch and very large thickness needed, the stresses in the film cause it to easily crack during curing. Thus a great deal of care is needed in this process, and resulted in a large failure rate. Next, polyimide PI-2611 was investigated. This polymer has a close thermal match to silicon, and thus has a reduced stress, and is solvent compatible after curing, but is not transparent at the UV wavelengths of interest. Thus only visible and infrared illumination was used to characterize these devices. Recently, we have switched to another polymer polydimethylsiloxane (PDMS). This polymer has a very low elastic modulus, and thus can easily conform to the nanowires. PDMS is also transparent to all the wavelengths of interest, and solvent compatible for short periods of time. For all cases, the material is spun onto the wafer surface, and cured. The polymer is then dry etched to expose the nanowire tips.

To contact the nanowires, we use the substrate as the source and fabricate transparent contacts above the photosensitive region using indium tin oxide (ITO). The windows for top electrodes are defined by photolithography and a 200 nm ITO layer is sputtered at 150 °C and lifted off in unwanted regions. Contact pads away from the photoactive regions are then defined with photolithography and Ti (20 nm)/Au (200 nm) was deposited. The

structure after a few of the key fabrication steps are shown in Figure 3.7. The major fabrication challenges encountered for this structure are finding a suitable dielectric for nanowire and top contact support, and creating reliable ohmic contacts. Many spin on dielectrics were investigated in this work with the most promising being PDMS. Ohmic contacts were more difficult to produce reliably, as devices have shown varying current levels across a chip.

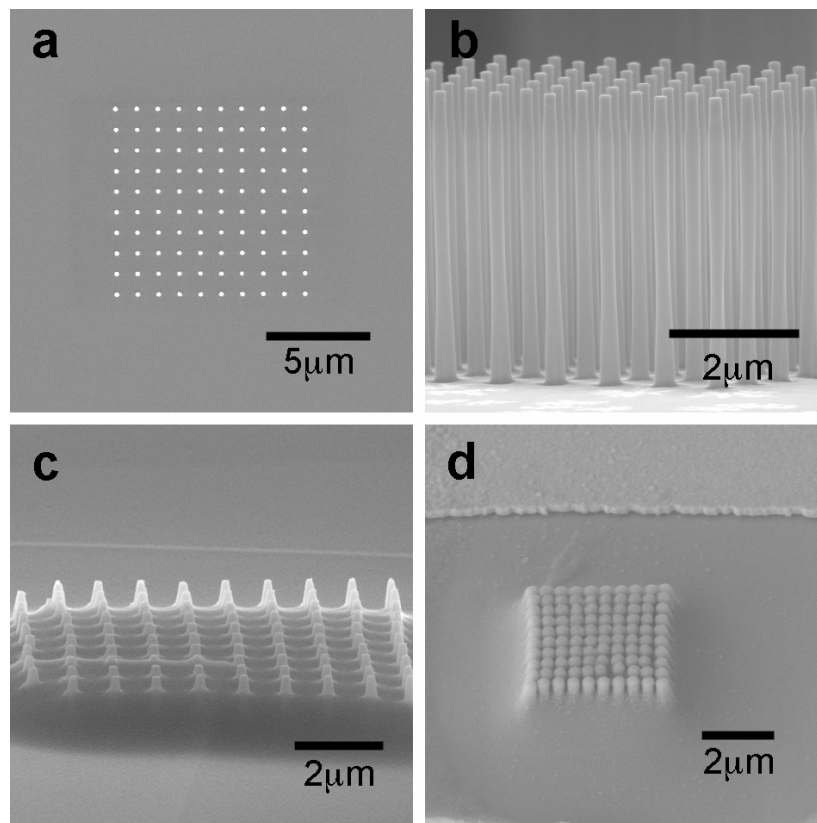


Figure 3.7: Images of fabricated 10x10 vertical silicon nanowire phototransistors. Nanowire diameters are 200 nm with a pitch of 1 μm. (a) SEM image of nanopatterned Ni dot array. (b) SEM image of nanowire array after etching to 4 μm in length. (c) SEM image of nanowires embedded in polymer with tips exposed. (d) SEM image of finished device the nanowire array embedded in dielectric with ITO contact and Ti/Au metal finger.

3.4 Conclusion

Through the use of standard and maturing fabrication technologies, silicon nanowire phototransistors of both planar and vertical orientation have been fabricated. Large area devices are quickly and cost effectively produced using nanoimprint lithography, which holds great promise as a future technology. Although during the development of the fabrication process of nanowire devices we encountered complications and difficulties, the formulated process is compatible with commercial fabrication and presents a fast and cost effective method for creating large area photodetector arrays. The two most difficult aspects of nanowire devices that continue to be challenges are the finding of a suitable dielectric for embedding vertical devices, and the creation of reliable and consistent ohmic contact made to each nanowire, which requires the careful choice of doping, silicides, and metal stacks. With these fabricated devices we now discuss their characteristics and performance.

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Portions of this chapter have been published in Nano Letters, 2010, Zhang, Arthur; Kim, Hongkwon; Cheng, James; Lo, Yu-Hwa, American Chemical Society, 2010. The dissertation author was the primary investigator and author of this paper.

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Chapter 4

Device Performance

4.1 Introduction

Although nanowire electronics and devices have been an area of extensive research, including silicon nanowire photodetector devices¹⁻⁸, a study has yet to be performed on silicon nanowire phototransistor like devices in which their full range of benefits have been discussed. The physics of nanowire phototransistors leading to beneficial device performance has been presented in earlier chapters through modeling and simulations and these devices have been realized using state of the art fabrication techniques. To quantify the device performance in these real world devices, they have been characterized under many different conditions. The following sections provide the details of the measurements performed on these devices, from their steady state response, broadband spectral response, temperature behavior, and dynamic response.

4.2 Steady State Response under Ultraviolet and Visible Light

The most basic measurement to demonstrate the performance of a photodetector is the measurement of their photoresponse under steady state bias and illumination. This provides us with the initial characterization of our

devices and provides some key information to the responsivity, quantum efficiency, and phototransistive gain. In these measurements, both planar and vertical devices were measured under ultraviolet and visible illumination.

The optical response of planar nanowire devices were characterized under steady state ultraviolet illumination using a mercury vapor lamp with a 390 nm (± 50 nm) band-pass filter. The illumination power was varied using neutral density filters. Devices were probed at the contacts and the IV characteristics measured using an Agilent 4155B parameter analyzer.

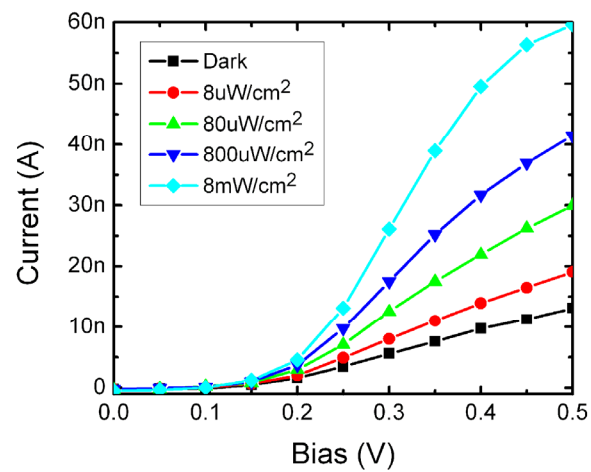


Figure 4.1: IV measurement results of planar device under varying optical intensities. The device consists of 10 nanowires with 250 nm in width, 8 μ m in length. Asymmetries in the curve are due to misalignment of contacts to the nanowires during fabrication.

DC Measurements of a 10 NW array device under dark and varying illumination levels are shown in Figure 4.1. An asymmetry in the IV characteristics is seen in these devices indicative of a one-sided Schottky

contact most likely due to a slight misalignment in the Al metal contact deposited during fabrication onto the low doped nanowire body⁹. Measurements taken by forward biasing the junction circumvent this barrier and allow the device to be properly biased. Reverse biasing the junction leads to very small photoresponse as expected with a Schottky junction device. The phototransistive gain, G , of the detector can be extracted experimentally through the definition:

$$G = \eta \frac{I_{ph}}{q} \frac{h\nu}{P_{opt}} \quad (4.1)$$

where η is the quantum efficiency, I_{ph} is the photocurrent, q is the elementary charge, $h\nu$ is the energy of the photons, and P_{opt} is the incident power. This gives the steady state phototransistive gain as the ratio of number of charges per second to number of photons per second or photon flux. The gain vs. estimated photon flux of this device biased at 0.5 V is shown in Figure 4.2. The photon flux is estimated for an exposed area of 10 NWs each having dimensions of 250 nm in width and 8 μm in length. Since these devices are of a planar geometry, the light coupling effect is not significant. 33% of the incident light on the exposed area is estimated to be absorbed (derived from 45% surface reflection and 60% absorption in Si for 230 nm wire thickness at $\lambda=390$ nm). A large gain saturation at high light intensities is seen due to the barrier lowering from the large number of carriers generated in the body of the nanowire. The gain is seen to increase as the

light intensity is lowered, reaching a gain of 35,000 at the lowest light intensities measured. The gain does not saturate even at these lowest illumination levels suggesting that the device is still saturated, and promises to demonstrate even higher gains at lower light intensities.

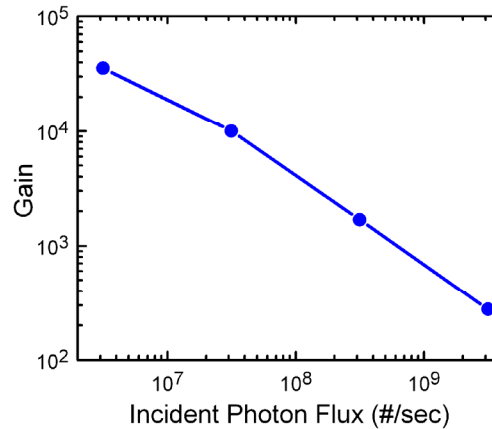


Figure 4.2: Gain vs intensity for planar device. The device consists of 10 nanowires with 250 nm in width, 8 μm in length and is biased at 0.5 V.

Static measurements of fabricated vertical devices, both $p^+/p^-/p^+$ phototransistors and $p^+/n^-/n^+$ photodiodes are characterized in the dark and under varying light intensities with a red 635nm laser, and the same parameter analyzer is used to measure the planar devices. The resulting IVs for phototransistor and photodiode devices with 200 nm diameter, 4 μm length, and 0.5 μm pitch are plotted in Figure 4.3. The phototransistor shows a symmetrical and linear IV indicating a good ohmic contact to the device is achieved, while the photodiode shows rectifying behavior as expected.

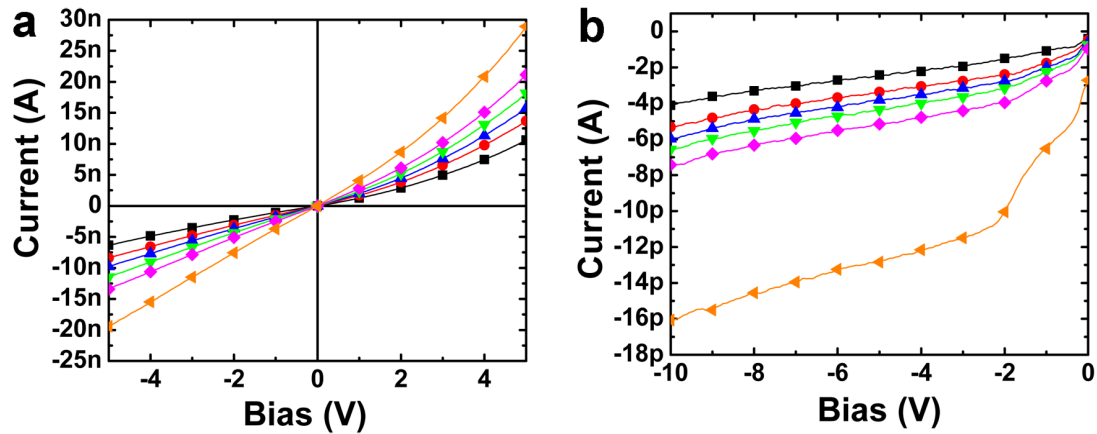


Figure 4.3: IV measurements of vertical devices under varying optical intensities: dark (black squares), 1.9 pW (red circles), 2.8 pW (blue triangle up), 4.1 pW (green triangle down), 4.9 pW (purple diamond), and 15.1 pW (orange triangle left). The current and powers indicated correspond to amount of power incident for a single nanowire. (b) I-V curve of photodiode at varying illumination powers same as (a).

With vertical nanowire phototransistors, it is difficult to very accurately extract the gain of the device due to the estimations necessary to find the quantum efficiency. Although the previous simulations have found the absorption enhancements in vertical structures, their absolute value is subject to interpretation. Thus to extract the gain in the vertical phototransistor, a photodiode of similar structure is used to provide baseline results. The photodiode device has an intrinsic gain of unity since carriers reaching the contact cannot be reinjected at the opposing contact as is the case with the phototransistor. By having the same structure as the phototransistor, the photodiode also has the same quantum efficiency, thus allowing for the gain to be extracted by comparing the total currents between the two devices. Due to

the nature of the gain mechanism in the phototransistor, in which both dark and photogenerated carriers are affected by the surface potential, the total current is used to determine gain. The drawback of this method is that due to the very low amount of reverse bias current from the photodiode, any leakage current from the device or in the setup will be included in the calculation of the gain which results in an underestimation of the true value. The gain vs bias is shown in Figure 4.4a and seen to depend linearly with bias. This is expected, as the transit time of the device varies inversely with applied voltage:

$$t_t = \frac{I^2}{\mu V} \quad (4.2)$$

$$G = \frac{\tau_c^h}{t_t} = \frac{\tau_c^h \mu V}{I^2}$$

For the surface state concentration of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ expected with our oxidized surface¹⁰, doping of 10^{15} cm^{-3} , and nanowire geometry, our fabricated device operates in the condition in which the device is depleted, yet the band bending is not optimized due to the low doping of the nanowire body. Thus we would expect even higher gain by using a higher doped device layer. At room temperature the high dark current also tends to saturate the device as the many carriers in the nanowire channel lower the barrier produced by the surface. Due to these factors, the gain observed at 5 V bias is modest at slightly over 2,000 at room temperature. The gain, shown in Figure 4.4b vs. light intensity, is constant at low light intensities and decays at higher light intensities. At low light intensities, the amount of photogenerated carriers is

small when compared to the dark current and thus do not cause the device to deviate from the dark conditions. However when the light intensity causes more photogenerated carriers than dark carriers, the device becomes more saturated and the decay in gain is observed.

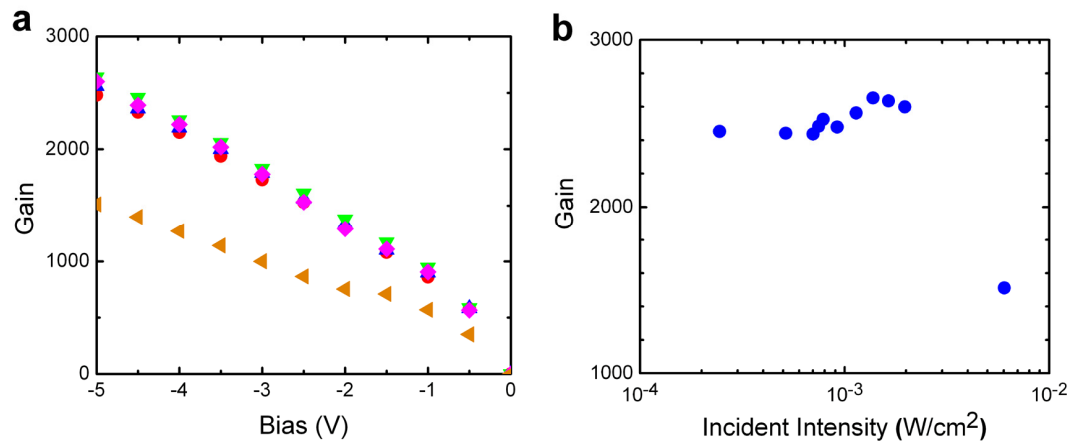


Figure 4.4: Gain results for vertical phototransistor. (a) Gain vs bias at varying intensities extracted from the I-V curves of the phototransistor and photodiode in Figure 4.3. 1.9 pW (red circles), 2.8 pW (blue triangle up), 4.1 pW (green triangle down), 4.9 pW (purple diamond), and 15.1 pW (orange triangle left). The powers indicated correspond to amount of power incident for a single nanowire. (b) Gain vs intensity at 5 V bias.

4.3 Spectral Response

The broadband characteristics of the silicon nanowire phototransistor have been investigated through spectral measurements on the device. Since the device is a system which incorporates many elements, each with its own spectral response resulting in a conglomerated observed behavior, we must first decouple the elements to determine each element's contribution. Each

element is characterized using a monochromator, sweeping the illumination wavelength from the ultraviolet to the near infrared.

As light illuminates the device it must first pass through the transparent ITO contact and then through the dielectric medium embedding the nanowires. The transmission of each of these elements to the wavelengths of interest is characterized and shown in Figure 4.5. Each material is deposited on glass slides along side the device during fabrication to ensure that the same material properties and thicknesses are measured. The spectral response of the ITO shows that it is transmissive to wavelengths down to 390 nm, after which it drops to half nearly, though still an acceptable value. The polyimide however demonstrates a sharp drop in transmission below 390 nm which indicates it is only suitable for visible and infrared detection.

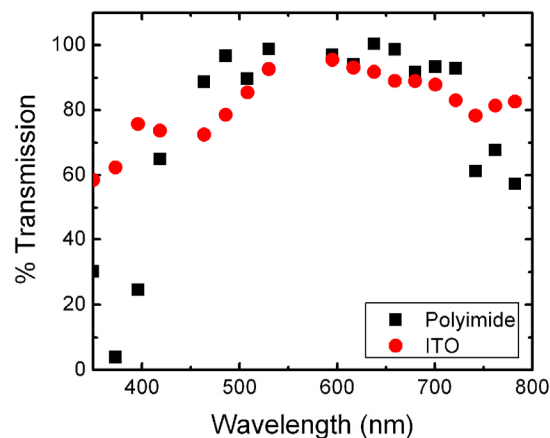


Figure 4.5: Spectral transmission curves of device films. ITO (200 nm), and polyimide PI-2611 (4 μm cured at 350 $^{\circ}\text{C}$ for 30 min) deposited on glass slides. The measurements are normalized to the response of the glass slide.

Fabricated vertical nanowire devices are then measured under 1 V bias and normalized to the transmission of ITO and polyimide. The response of these devices, shown in Figure 4.6, is seen to be enhanced at shorter wavelengths and to decay at longer wavelengths, deviating from silicon's intrinsic material absorption properties¹¹, due to the diminishing effect of the absorption enhancement in the vertical structures as the wavelength increases. The cause of this stems from the lowering of the complex index of refraction of silicon at longer wavelengths. This decreases the contrast between the real component of the index of silicon with the surrounding polymer, and lowers the amount of absorption as the imaginary component drops significantly. To show only the effect of the nanowire geometry to the absorption enhancement, the material absorption of silicon is removed from Figure 4.6b. This is compared with simulations performed in Comsol multiphysics performed in the same manor as described in Chapter 3. The simulations and experimental results shown in Figure 4.6b correlate nicely, indicating that the nanowire absorption enhancement is responsible for the large absorption at short wavelengths.

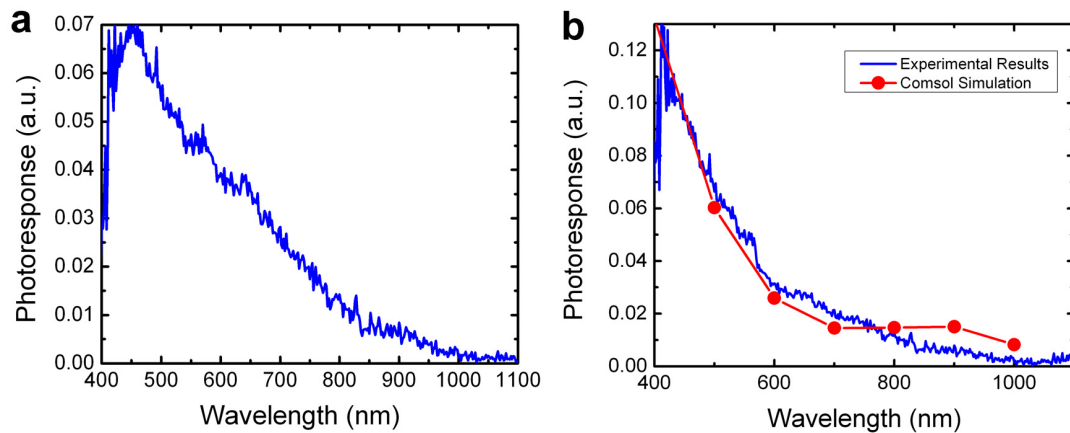


Figure 4.6: Spectral measurement of vertical silicon nanowire phototransistor. (a) Measurement of device at 1 V bias. (b). The intrinsic effect of silicon is removed from measurement results from (a) to show the effect of the nanowire light coupling effect compared with results from Comsol simulations.

4.4 Temperature Dependence under Visible and Infrared Light

The previous measurements have shown the device's characteristics at room temperature. Due to the large dark current at room temperature, the device demonstrates limited response and lowered gain. Also, the spectral measurements have shown that the device's responsivity quickly decays at longer wavelengths due to a decrease in absorption enhancement. In this section we probe the device further with temperature dependence measurements to obtain better characteristics as lower dark current, and demonstrate that the device shows a large photoresponse for both visible and infrared wavelengths.

The same 10x10 nanowire arrays, with dimensions of 200 nm in diameter, 4 μm in length, and 1 μm in pitch, are characterized at various

temperatures and illumination intensities in a temperature controlled cold-finger cryostat chamber under low vacuum. Light from diode lasers with wavelengths of 635 nm for visible and 1550 nm for infrared illuminate the sample through an optical port and the intensity is varied by controlling the current supplied to the laser. The optical power used in these measurements is greatly reduced from the previous measurements to view the device's response to low level illumination which becomes possible at lower temperatures. The IV characteristics of the device are then measured using a parameter analyzer. Plots of the IV characteristics at a few characteristic temperatures under visible illumination are shown in Figure 4.7. At room temperature, the device shows a substantial dark current which masks the photoresponse from the much lower light illumination. However, as the device is cooled, the dark current drops dramatically. At 150 K, the dark current is reduced by three orders of magnitude, and at 90 K, the dark current is lowered by another two orders of magnitude. With this reduction in dark current, an incident power of 0.1 fW/nanowire can be distinguished.

As the device is cooled, the IV characteristics become more exponential in behavior. This is attributed to the p+/p- barrier that is present in the device between the heavily doped source/drain and the body of the nanowire allowing for ohmic contacts to be formed to the source and drain. At room temperature, carriers easily overcome this barrier and are freely injected

into the channel. However, at lower temperatures, the barrier becomes more significant as carriers do not have the thermal energy to be injected.

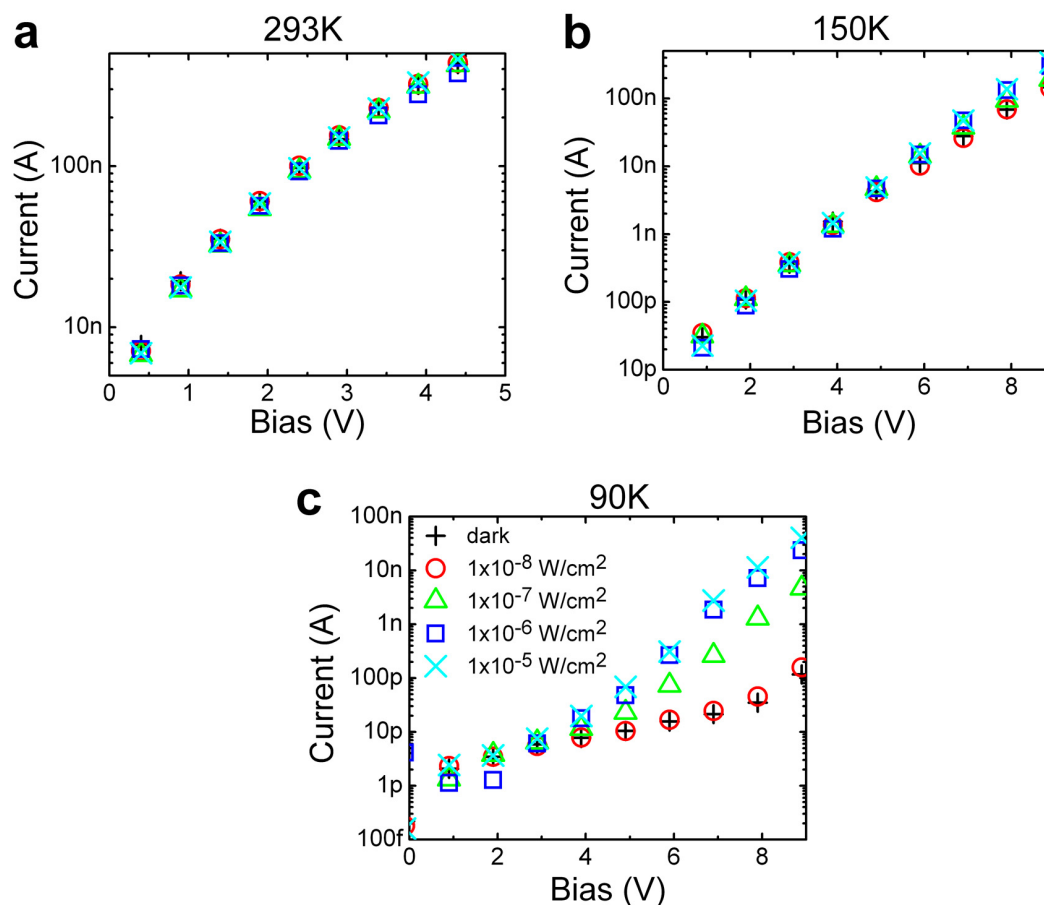


Figure 4.7: IV measurements of a silicon nanowire phototransistor measured at varying temperatures and incident illumination intensity. (a) 293 K, (b) 150 K, (c) 90 K.

A promising characteristic of silicon nanowire phototransistors is their sensitive behavior to both above bandgap absorption of visible light, and as we will show sub-bandgap absorption of infrared light. Figure 4.8 shows the photocurrent of a device illuminated at various intensities using 635 nm and

1550 nm lasers at various temperatures. Under visible illumination, the device shows a very high responsivity with detection levels of $0.1 \text{ fW}/\mu\text{m}^2$ incident power per nanowire, which is the limit of background level illumination in our setup. The incredible sensitivity is possible due to the low dark current and associated noise at the lower temperatures and the high internal gain of the nanowire structure. The device also shows a significant response to infrared illumination measured at 1550 nm wavelength greatly beyond what is possible in band to band absorption in bulk, single-crystalline silicon. These measurements were performed in collaboration with a lab member, Hongkwon Kim. In bulk silicon, infrared absorption resulting from band to surface state transitions is negligible due to the small surface to volume ratio. However, as we have demonstrated in nanowire devices, the surface to volume ratio can be significantly high, allowing for a substantial responsivity to infrared light. The observed infrared response of this detector is many orders of magnitude higher than one would expect by considering only the absorption coefficient of bulk silicon at this wavelength¹² and shows a detectable response at incident illumination levels on the order of 1 pW per wire. The infrared responsivity has a four order of magnitude reduction compared to visible illumination partly due to the decreased absorption enhancement from the waveguiding effect at longer wavelengths described in the previous section and a lower absorption cross section from the fewer number of states available for band to surface generation compared to band to band transitions. The photocurrents in each

measurement scenario decrease with decreasing temperature due to the injection barrier at the p^+ source in which photogenerated carriers must obtain enough energy to overcome this barrier to contribute to the photocurrent.

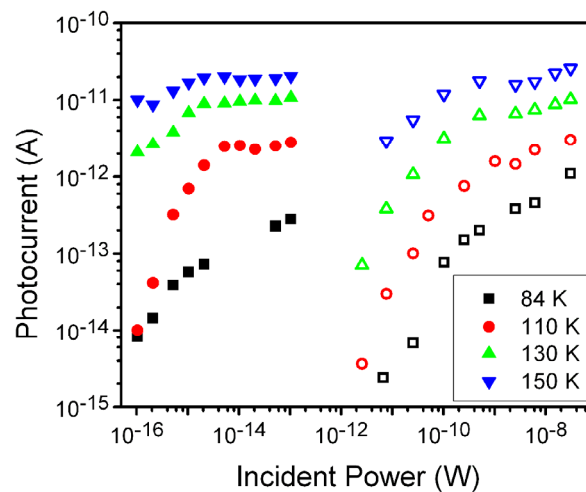


Figure 4.8: Photocurrent under various illumination levels for visible (solid symbols) and infrared (hollow symbols). The device (200 nm in diameter, 4 μm in length and 1 μm pitch) is biased at 5 V and measured at different temperatures. Photocurrent and incident power are normalized to a single wire.

The steady state device performance at the varying temperatures can be expressed in terms of the responsivity, directly related to the internal gain of the device, and is plotted against incident optical power in Figure 4.9 for both visible and infrared illumination. By using the metric of responsivity, we can remove the estimation of quantum efficiency needed to calculate the gain of the device, and thus we believe is a more accurate representation of the device's performance. At very low incident light intensities in which the device

is unsaturated, a peak responsivity of 10^5 A/W is observed for visible illumination and 10^2 A/W for infrared illumination. These values are much greater than similar nanowire devices^{2, 5, 13, 14}, or conventional silicon photodiodes with a typical responsivity below 1 A/W.

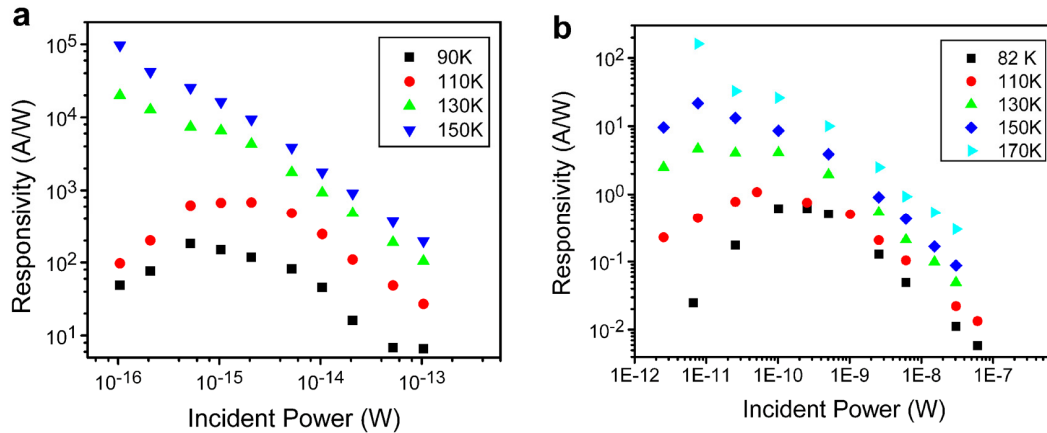


Figure 4.9: Responsivity vs laser power incident on a silicon nanowire phototransistor array at various temperatures for (a) visible illumination at 5 V bias and (b) infrared illumination at 9 V bias. Incident power is normalized to a $1 \mu\text{m}^2$ area around a single wire.

An important characteristic of these devices is the decay of the responsivity at higher optical power. As the light intensity increases, the number of electron hole pairs generated in the nanowire increasingly deviates from thermal equilibrium values. The increasing number of holes in the center of the wire lowers the potential barrier confining the holes, which decreases the lifetime of holes and therefore the gain and responsivity. This effect parallels automatic gain control circuits, which allows for a much larger dynamic range, making these devices excellent candidates for applications requiring either very low light intensity detection, or normal photodetector

arrays. The gain in these devices is also seen to increase with increasing temperature. As the temperature is lowered, the barrier for hole capture at the surface states effectively increases, which increases the lifetime and gain. However, the barrier for hole injection at the contacts also increases with decreasing temperature, which lowers the photocurrent and gain. This effect dominates the behavior of the device but becomes negligible at high enough temperatures allowing for holes with enough thermal energy to overcome this barrier. Thus the increase in gain is seen to saturate between 150-170 K. Although the level of gain is maintained with further increasing temperature, the detection of such small signals is increasingly more difficult as the dark current, and its associated noise eventually overwhelms the photoresponse. Thus for maximum responsivity, an operating temperature to balance these two factors must be considered for this device.

4.5 Dynamic Response

Additional measurements have been performed to investigate the dynamics of the device and determine the time constants associated with the gain and bandwidth of the phototransistor. The measurements were performed using a similar setup as before in cryo chamber under low vacuum at varying temperatures. A 635 nm diode laser is used as illumination source which passes through a 50% duty cycle mechanical chopper with frequency range from 1 Hz to 6 kHz, resulting in a square wave modulated signal. The

device is electrically connected to a current transimpedance amplifier which provides a 5 V DC bias and measures the signal after low pass input frequency filters to remove the DC component of the signal. The 50 ohm output of the amplifier is connected to the 50 ohm input of an oscilloscope for data collection.

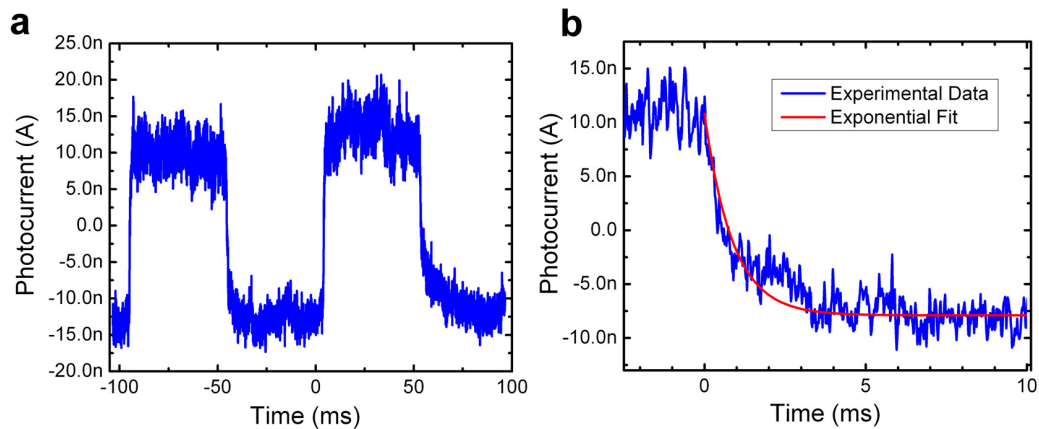


Figure 4.10: Dynamic response of phototransistor to 10 Hz square wave modulated light. 10x10 nanowire device (200 nm in diameter, 4 μm in length and 1 μm pitch) measured at 82 K with 5 V applied bias. Devices illuminated with a 635 nm laser passing through a mechanical chopper with a power of 260 pW. (a) Plot showing two periods of modulation. (b) Enlargement of falling edge to show a decay time constant of 0.87 ms.

The dynamic response of the device recorded by the oscilloscope to an optical modulation frequency of 10 Hz is seen in Figure 4.10. The rise and fall times of the device response can be measured from these plots and shows a time constant of 0.87 ms reflecting the hole capture lifetime. Using equation 4.2 and the low temperature bulk mobility for holes¹⁵ of 2000, leads to an expected phototransistive gain of 5×10^7 .

The bandwidth of the device is determined by plotting the amplitude of the signal with varying frequency shown in Figure 4.11. The bandwidth thus determined shows a 3 dB cutoff frequency of over 1 kHz, corresponding to the time constant measured earlier.

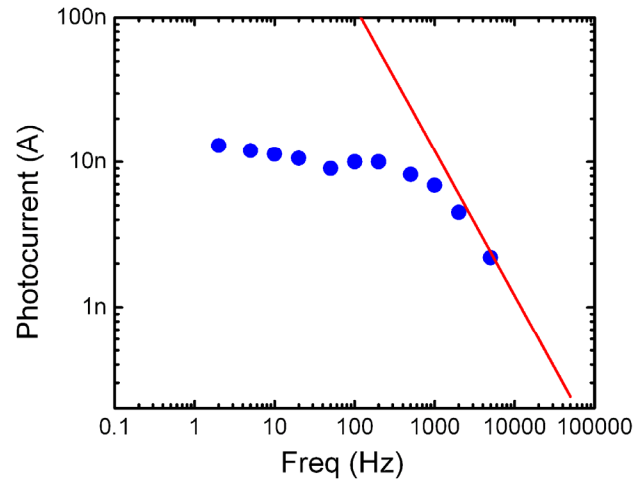


Figure 4.11: Photocurrent vs chopper frequency of phototransistor. The device is measured at 130 K with 5 V applied bias and illuminated with 10 pW of 635 nm light over the $10 \times 10 \mu\text{m}$ area. Device shows a 3 dB cutoff frequency of 1.5 kHz.

4.6 Conclusion

The characterization of silicon nanowire phototransistors has shown their unique properties. They are seen to have much higher responsivity than similar devices in silicon, with a detection of down to 0.1 fW per nanowire. The cause of this is due to the phototransistive gain in nanowire structures arising from an intrinsic gate bias which forms a subthreshold channel within the center of the nanowire, allowing for a long lifetime of photogenerated holes.

These devices also improve upon their counterparts by their ability for broadband detection, and in particular from their sub-bandgap response to infrared light, unseen in traditional silicon devices. This is due to the large number of surface states to volume of the nanowire structure, which increases the effect of valence band to surface state absorption. However through our characterizations we have also found limitations of the device and areas in which this device can be significantly improved. The major limitation is from how the gain is derived in the device. To have a large photoresponse and phototransistive gain, the device must be intrinsically slow. With this method of gain, no additional carriers are created from the initial generation of absorbed photons. Therefore the large response of the device is due to the persistent photocurrent which is sustained from the long carrier lifetime. In the devices we have fabricated thus far, the gain has been limited by the barrier from the source to the nanowire channel which reduces the photoresponse of the device, without decreasing the lifetime of the carriers. This can be improved in future devices by engineering the source channel to reduce this barrier. The other major limitation of current devices is their high dark current at room temperature. This increases the amount of noise from the device which limits its sensitivity. To overcome this obstacle, a new device geometry is proposed in the following chapter under future work.

Portions of this chapter have been published in Applied Physics Letters 2008. Zhang, Arthur; You, Sifang; Soci, Cesare; Liu, Yisi; Wang, Deli; Lo, Yu-Hwa, American Institute of Physics, 2008. The dissertation author was the primary investigator and author of this paper.

Portions of this chapter have been published in Nano Letters, 2010, Zhang, Arthur; Kim, Hongkwon; Cheng, James; Lo, Yu-Hwa, American Chemical Society, 2010. The dissertation author was the primary investigator and author of this paper.

Portions of this chapter have been published in the Proceedings of SPIE 2010. Zhang, Arthur; Cheng, James; Kim, Hongkwon; Liu, Yisi; Lo, Yu-Hwa, SPIE, 2010. The dissertation author was the primary investigator and author of this paper.

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Chapter 5

Conclusions

5.1 Conclusions

Nanoelectronics and nanodevices are at the forefront of the latest device research. The unique properties of nanostructures make them an interesting research topic for exploring new physical phenomena but also can be practically beneficial to many devices' performance. In the area of photodetection, many nanowire structures have been investigated. One such structure which has shown great performance due to the properties which arise from the device size is found in the silicon nanowire phototransistors investigated in this work. Through the shrinking of typical bulk or thin film photoconductor into nanoscale dimensions, the device is transformed into a phototransistor. By utilizing the many surface states of the nanowire, and the large surface to volume ratio, a gate bias is created, forming a depleted nanowire channel. This can then be optically modulated to vary channel conductivity and produce an amplified signal.

Investigation into nanodevices spurs the continuing advancement of fabrication methodology to produce a variety of nanostructures. For nanowire devices, this has led to much research in both bottom-up and top-down approaches. While the bottom-up approach allows for great flexibility in

forming a myriad of device structures for research applications, the top-down approach have been found to be both cost effective and quick, providing an enabling technology for large area devices suitable for incorporation into traditional fabrication lines. Large area devices can be patterned using nanoimprint lithography, while etching enables precise positioning and engineering of geometries with traditional doping techniques for accurate control.

Sizable quantum efficiency is necessary to create a practical photodetector. Although the small size of nanowires inherently produces a very small footprint for incident light, vertical devices have been shown to capture a large percentage of optical power even with large nanowire spacing. This effect arises due to the long interaction length of light along the nanowire channel and increased coupling of light surrounding the nanowire into the structure for enhanced absorption.

Characterization of fabricated nanowire phototransistors shows the device's very high responsivity to broadband light, from ultraviolet to visible to near infrared. In the visible spectrum, a sub 0.1 fW per nanowire response can be observed, corresponding to approximately 300 photons per second. In addition, significant sub-bandgap infrared absorption is observed in these devices unseen in traditional Si detectors. This response is possible in nanowires due to significant band to surface state transitions only possible in nanostructures with high enough surface to volume ratio. The observable

photoresponse to 1550 nm light is down to picowatt levels. Characterizations to determine the dynamic response of the phototransistor have shown the device bandwidth to be approximately 1 kHz. This value is suitable for some applications where very fast speed is not critical such as imaging, and radiation detection. The high responsivity to a broad spectrum of light of this device shows great promise as a valuable photodetector for high resolution imaging from very low to high light levels.

As investigation into these devices continue to progress, a few challenges must be overcome to better device performance. The first of these is in finding suitable dielectrics to support the nanowires and top contact. The dielectric must be able to fill in between wires, be transparent to all wavelengths of interest, thermally matched to silicon, and process compatible. Secondly, designing and fabricating contacts to nanowires can be improved. The contact must be reliable and uniform across devices and chips, and must minimize the barrier between the source and nanowire channel. A third challenge arises from the fundamental design of the device, relying on surface states for producing high phototransistive gain. The density of surface states can vary with processing conditions which greatly changes the phototransistor's performance. Another major drawback for the surface state device is a high dark current at room temperature. In this device, surface state to band transitions produce a significant source of dark current as carriers escape traps. The high dark current results in higher noise, and gain

saturation since both dark and photogenerated carriers contribute to gain. To overcome this challenge, the device needs to be reengineered to increase sensitivity for room temperature operation required for many applications. A new device concept to solve this challenge is presented in the next section.

5.2 Future Work

The above mentioned challenges are all significant towards building a robust and commercially viable photodetector. This work has shown silicon nanowires to become a powerful photodetection tool. These devices have demonstrated the very high sensitivity in such structures, and that sub-bandgap detection is possible, unseen in their bulk or thin film counterparts. Most of the characteristics of the phototransistor have been shown at below room temperatures due to the high dark current resulting from low energy transitions by holes escaping surface states into the valance band. However, to make this detector truly perform at room temperature, we need to reengineer the device to remove this contribution of dark current by moving away from using surface states to create gate bias, which will also make the device more reliable and reproducible.

An alternative to using surface states to create the radial bias is to use a core shell p-n junction structure in which the shell now provides the radial depletion to create the nanowire channel. The highly doped shell separates the nanowire channel from surface states, thus isolating the channel from low

energy transitions from the surface states to nanowire channel which drastically reduces the dark current.

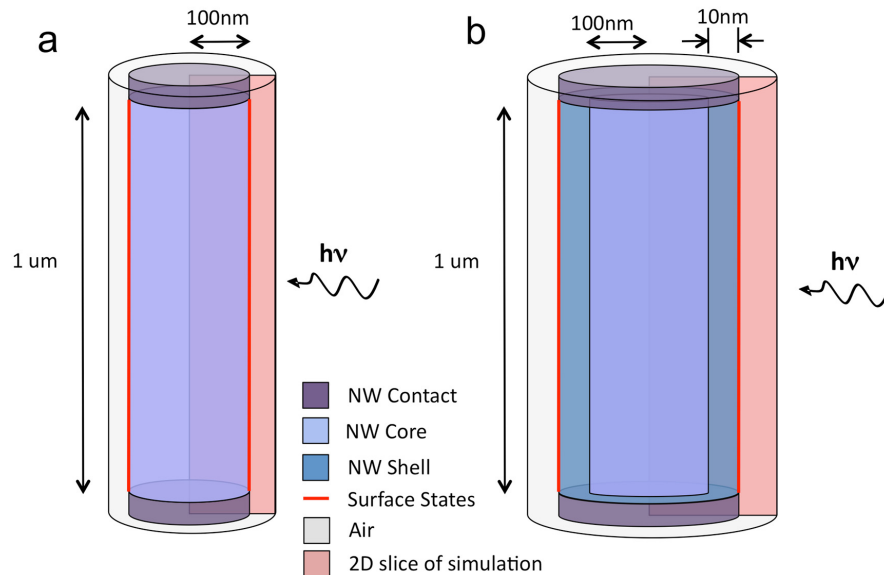


Figure 5.1: Diagram of simulated (a) surface state and (b) core-shell structures in Silvaco.

To show the device concept in more detail and determine the parameters which yield the best performance, simulations have been performed on the new structure using Silvaco. The simulations consist of both surface state and core shell structures shown in Figure 5.1 to compare their behavior. Both sets of devices consist of a p-type nanowire core with varying doping concentration, 1 μm in length and 100 nm in radius. P^+ contacts are made to both structures to reflect the real device structure. In addition, the core shell structure has a 10 nm thick n^+ shell doping. The value of the shell doping is chosen to be $1 \times 10^{19} \text{ cm}^{-3}$, high enough to isolate the channel from the surface states, and able to fully deplete the nanowire channel. Varying

surface state densities with the same distributions as the previous simulations detailed in Chapter 2 are applied to the surface of both structures.

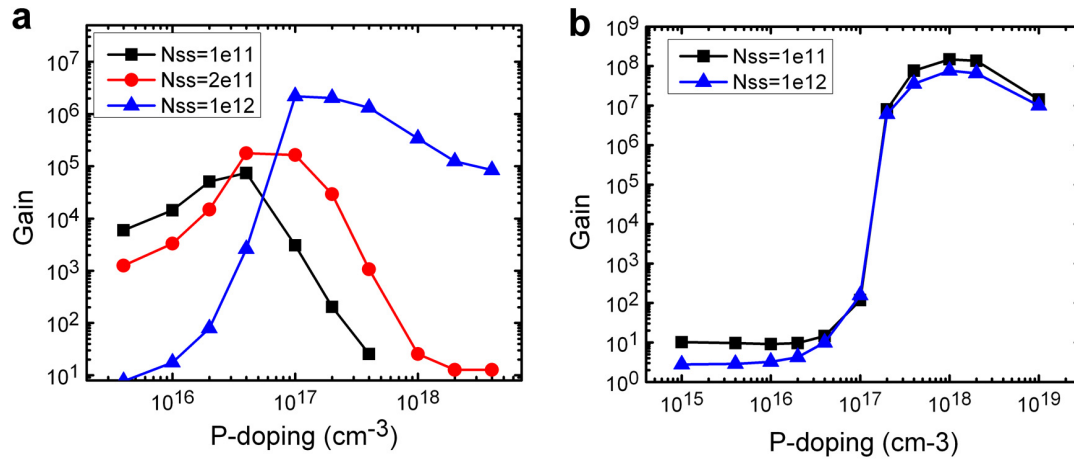


Figure 5.2: Gain plots of simulated (a) surface state device and (b) core shell structure. Surface state device shows a large dependence of gain on surface state density (Nss) while the gain of the core shell structure remains unaffected.

Figure 5.2 shows the gain vs p-type core doping for both structures with varying surface state densities. We see that for the device relying on surface states, the gain is very sensitive to the density, while for the core shell structures, the gain does not vary much when varying surface state density by an order of magnitude. This demonstrates the ability for core-shell structures to overcome the sensitivity of gain to varying surface conditions, which allows the device to be more reliable and reproducible. Another benefit of the core shell structure is the possibility of much larger gain. The plots show that the gain of the core shell structure is more than two orders of magnitude larger

than the surface state device. This is possible in the p-n structure which allows for a much larger radial energy barrier to occur.

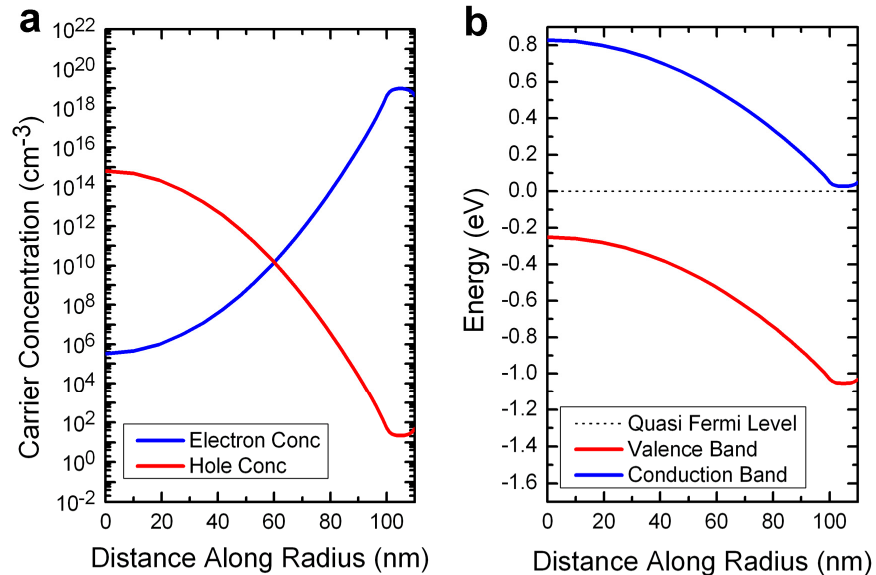


Figure 5.3: Radial cross-section of carrier concentration and band diagram of simulated core shell structure. Structure consists of p-type core doping of $2 \times 10^{17} \text{ cm}^{-3}$, shell doping of $1 \times 10^{19} \text{ cm}^{-3}$ and surface state density of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. (a) Carrier concentration shows the core to be completely depleted. (b) Band bending between the core and shell shown to be a significant portion of the bandgap.

The core shell structure creates a radial gate bias through depletion between the p-n junction. Figure 5.3 shows the carrier concentrations and band structures along a radial cross-section of the core shell structure for a core doping of $2 \times 10^{17} \text{ cm}^{-3}$, and surface state concentration of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The n-type shell is seen to deplete the core of the nanowire, while creating a potential well for electrons in the shell. The gain of the device is still dictated by the amount of time required for holes to move from the nanowire core

channel to shell to recombine with electron. However in this structure, the holes must overcome a much larger energy barrier, close to the bandgap of silicon, thus increasing the recombination lifetime and gain. This paves the way for the device to show great potential for even higher sensitivity possibly down to single photon limits.

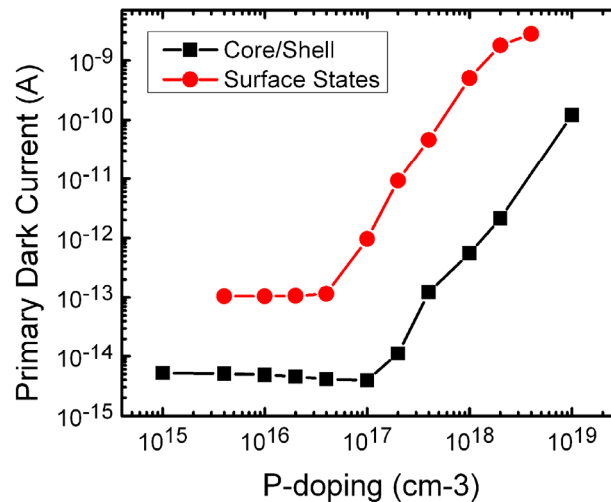


Figure 5.4: Primary dark current of simulated surface state and core shell devices vs. p-type core doping. Surface states of both structures is $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Primary dark current is calculated by dividing the total dark current by the gain. Core shell structure shows a reduction of primary dark current by 2 to 3 orders of magnitude.

The core shell structure also allows for a dramatic decrease in dark current over the surface state device. We analyze the primary dark current of each device to compare the primary generation rate of each structure. The primary dark current is determined by taking the total dark current and dividing it by the gain and is shown in Figure 5.4. From the plot, we observe that the

primary dark current in the core shell structure is reduced by 2 to 3 orders of magnitude at certain dopings. This is due to the isolation of the nanowire channel from the surface states. Thus any low energy transitions are between the surface states and the n-type shell. However, due to the p-type contacts which create back to back p-n junctions, these thermally generated carriers do not contribute to the dark current. With this reduction, room temperature operation is expected to be possible while operating with high sensitivity.