UNIVERSITY OF CALIFORNIA SAN DIEGO

Circuits and Techniques for Power-Efficiency Enhancement of IoT Sensor Nodes

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits & Systems)

by

Somok Mondal

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2020

The dissertation of Somok Mondal is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

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Chair

University of California San Diego

2020

DEDICATION

To my parents.

EPIGRAPH

The "Amazing" can only be created by facing fear, risk, and failure during the process.

– Superman

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ACKNOWLEDGEMENTS

When I initially joined the Ph.D. program at UCSD in Fall 2013, little did I know how the journey would turn-out, except that it is likely going to be one of the toughest as well as rewarding challenges encountered. My Ph.D. experience has indeed lived up to this reputation. It has been a long and quite a few times an uncertain journey. However, having stood though, thanks to several people acknowledged here, I have eventually been able to make some meaningful research contributions. Overall, as I write this thesis in Spring 2020, I am happy to see that my research has panned-out quite well and, importantly, that I am able to end this journey on a high-note.

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Chapter 3, in part, contains materials from "Somok Mondal, Omid Ghadami and Drew A. Hall, An Audio-band Continuous-time Delta Sigma Modulator using Chopped AC-coupled OTA-Stacking" that is being prepared for publication. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in part, contains materials from "Somok Mondal and Drew A. Hall, A 67-µW Ultra-Low Power PVT-Robust MedRadio Transmitter", to appear in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2020, and its journal version that is being prepared for publication. The dissertation author was the primary investigator and author of these papers.

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PUBLICATIONS

Somok Mondal, Omid Ghadami and Drew A. Hall, "An Audio-band Continuous-Time Delta–Sigma Modulator with Chopped AC-coupled OTA-Stacking," In Preparation.

Somok Mondal and Drew A. Hall, "A 67-µW Ultra-Low Power Short-Range MedRadio Transmitter achieving 27% global efficiency at -17.5 dBm Pout in 22nm FDX," In Preparation.

Somok Mondal, Chung-Lun Hsu, Roozbeh Jafari, and Drew A. Hall, "A Dynamically Reconfigurable ECG Analog Front-End with a 2.5× Data-Dependent Power Reduction," Submitted.

Somok Mondal and Drew A. Hall, "A 67-µW Ultra-Low Power PVT-Robust MedRadio Transmitter," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2020. To Appear.

Somok Mondal and Drew A. Hall, "A 13.9-nA ECG Amplifier Achieving 0.86/0.99 NEF/PEF Using AC-Coupled OTA-Stacking," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 55, no. 2, pp. 414-425, Feb. 2020.

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Somok Mondal, Abhishek Agarwal, and Drew A. Hall, "Analysis of Amplifier Characteristics with OTA-Stacking," In Preparation.

ABSTRACT OF THE DISSERTATION

Circuits and Techniques for Power-Efficiency Enhancement of IoT Sensor Nodes

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits & Systems)

University of California San Diego, 2020

Professor Drew A. Hall, Chair

Advances in semiconductor technology over the last few decades has caused an influx of electronic devices into our daily lives, leading to the emergence of the Internet-of-Things (IoT) era. The IoT is a cluster of many miniaturized devices (also called sensor nodes) that unobtrusively capture data from our lives and surrounding environment to improve our quality of life. The IoT

is expected to have a transformative impact on a wide variety of applications ranging from biological sensing such as wearable electrocardiogram-recording (ECG) to track our well-being, to physical sensors for industrial and environmental monitoring, to entertainment and infrastructure related devices, such as audio devices, for smart-homes and smart-cities.

From a circuit design perspective, enabling the IoT requires overcoming an important technological hurdle: maximizing energy efficiency. With many of these nodes requiring uninterrupted seamless operation, a small form-factor, an unobtrusive or remote location, and high longevity, there are severe constraints on the power source (*e.g.*, battery, energy harvester, etc.). Henceforth, enhancing the power efficiency is, by-far, the key challenge to be addressed for the practical deployment of such IoT sensor nodes.

Generically speaking, a typical IoT sensor node comprises two basic building blocks: 1) an analog front-end (AFE) with amplifiers and data-converters and, 2) a transmitter for wireless communication. Most AFEs for IoT applications need to amplify/acquire low bandwidth signals while introducing minimal circuit noise. Power efficiency is fundamentally limited by noise for these AFEs. Since many IoT transmitters only need to communicate to a nearby base-station, such as smartphone or smartwatch, the output power P_{out} delivered to the antenna is often low. Power efficiency is limited by frequency synthesis considerations for these transmitters. In this dissertation, multiple circuits and techniques to enhance the power efficiency of the aforementioned IoT blocks are proposed. These are demonstrated by three prototype chips, namely: 1) an amplifier for implantable ECG recording, 2) a data-convertor for precision audio, and 3) a transmitter for short-range, narrowband communication.

The ECG amplifier is intended for implantable recording. There is significant interest in implantable devices, in general, due to their unobtrusive nature, improved environmental artifact

tolerance, and that some biological signals can be only be obtained *in vivo*. However, these are also associated with very stringent power budgets of only a few nanowatts (nWs). An ultra-low power, 13.9 nA ECG amplifier is first described. This work achieves state-of-the-art noise-efficiency and power-efficiency factors of less than unity, which correspond to ~3× improvements over prior sub-100-nW amplifiers. The key enabling idea, also the main contribution of this work, is an operational transconductance amplifier (OTA)-stacking technique that fundamentally improves the noise efficiency of noise limited amplifiers.

Next, the OTA-stacking technique was expanded for use in oversampling analog-to-digital converters (ADCs). This ADC is intended for audio devices for entertainment, smart-homes, automobiles, etc. where continuous-time delta-sigma modulators (CTΔΣMs) are often the power bottleneck for such devices. These ADCs need high dynamic range (DR), which is challenging with the power constrains associated with portable sensor nodes. Several techniques such as finite impulse response (FIR) feedback, 4-stage feedforward op-amp, tail-less operation, and OTA-stacking were integrated into a 3rd-order CTΔΣM to achieve near state-of-the-art performance. The ADC achieved >100 dB DR while consuming only 121 μW with a 2.1 dB improvement in the Scherier's Figure of Merit (FoM) due solely to the OTA-stacking.

Lastly, a narrowband transmitter is reported for short-range wireless communication (<2 meters) over the 400 MHz MedRadio-band. Enabling the interconnection functionality for the IoT devices while being power-efficient is another critical challenge. A process, voltage, and temperature (PVT)-robust frequency synthesis technique using a crystal oscillator integrated with a passive polyphase filter was demonstrated. A state-of-the-art global efficiency of 27% at -17.5 dBm P_{out} and low power of 67 μW compared to prior sub-1 mW transmitters was achieved.

Chapter 1.

Introduction

1.1 Motivation: An Internet-of-Things (IoT) World

The most noticeable and consistent trend associated with electronic hardware of any kind over the last 50 years is its ever-shrinking form factor and increase in portability. The last decade predominantly saw integration of portable cellular devices, such a smartphone, into our daily routine. The next decade is bound to see further integration of several miniaturized, interconnected gadgets all around us and, perhaps in some cases, even inside of us. These are collectively termed the “Internet-of-Things” or the IoT.

The scope of these IoT devices span a very wide range of applications [1]. One of the most popular of these is related to the healthcare sector [2]. The advent of wearable and implantable biosensors has tremendous potential in the sense that they can facilitate automated and remote monitoring, thereby enabling early detection or medical diagnosis. Addressing such mobile health (mHealth) applications is the focus of this work. Another very popular application is related to personalized audio and entertainment devices and has widespread applicability in smart-homes, cars, and shops requiring far-field voice capture [3], and is the secondary focus of this work.

1.2 An IoT Wireless Sensor Node

A generic IoT sensor node is shown in Figure 1.1 and comprises two main components:

1. **Precision Analog Front-End (AFE) Circuits**

The analog environment is interfaced with the electronic/digital world via sensors and transducers which are realized using amplifier and data-converter circuits. Most of these sensing circuits share a few important common traits: 1) The signal acquisition needs to be seamless and always running in the background; 2) The signal to be sensed is low bandwidth but weak in nature. As such, the noise requirements limit the front-end power efficiency.

2. **Wireless Communication Circuits**

The other important aspect is maintaining constant communication to a near-by base-station, such as a smartphone or smartwatch. Due to the asynchronicity, the node may be controlled via a wake-up receiver (WuRX) that can be realized at exceptionally low power [4]. A transmitter is therefore the critical, power-hungry, wireless component. Owing to the short-range of the communication link (< 2 m), contrary to conventional radios, the power amplifier

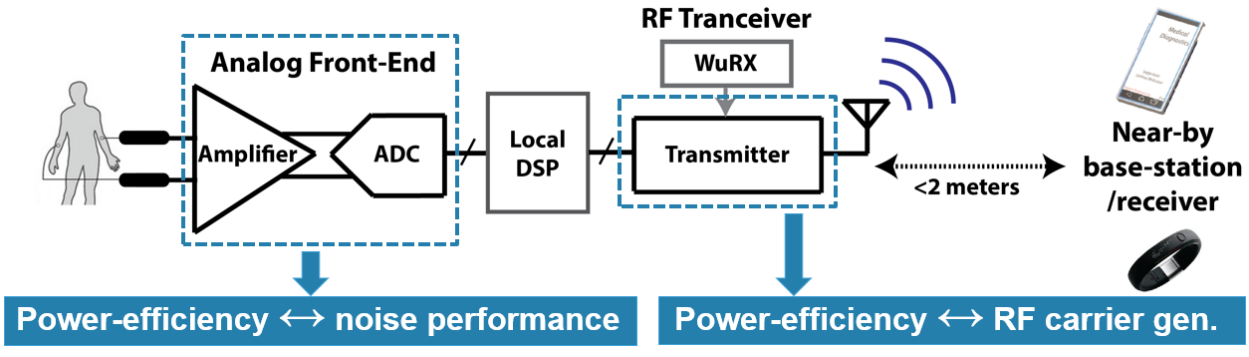


Figure 1.1 An IoT wireless sensor node

is not the critical block. As such, synthesis of the RF carrier limits the transmitter power efficiency.

1.3 Ultra-low Power Analog Front-Ends (AFEs) for Biosensing

Research and development related to biosensors has always been an extensively sought-after discipline because of the scope of impactful contributions to the healthcare sector such as early disease diagnosis, individualized medicine, ultrasensitive point-of-care detection of biomarkers, etc. Biosensing applications can be categorized into a wide variety raging from physiological, electrochemical [5], [6], optical [7], magnetic [8], [9], etc. Among these applications, physiological sensing with portable wellness products has seen a dramatic increase in recent years as individuals have become more engaged and proactive in their own healthcare. However, the small form-factor and need for continuous bio-signal acquisition, imposes stringent power budgets. Energy-efficient designs are hence critical for long-lasting operation.

These bio-signals are typically very low bandwidth in nature. The sensor front-end requirements are, henceforth, primarily to amplify and acquire weak bio-signals. This implies that, from a power consumption perspective, the front-end design is usually noise-limited. There exists a fundamental limit to the noise-power tradeoff for amplifiers and the best noise-efficient performance is achievable when the input devices are in sub-threshold mode of operation.

Overcoming this noise-power tradeoff was one of the primary motivations behind this dissertation work. A data-dependent power reduction technique was initially proposed to tackle this noise-power tradeoff with respect to a wearable electrocardiogram (ECG) sensor [10], [11]. However, this relied on an ECG-specific quasi-periodicity property and had limited scope. Later,

a more general purpose, ac-coupled operational transconductance amplifier (OTA)-stacking technique was proposed in [12], [13], which fundamentally improves over the noise-power tradeoff. State-of-the-art performance in terms of noise-efficiency was demonstrated for an ultra-low power ECG amplifier intended for implantable applications.

1.4 Precision Data-Converter for Audio Applications

The OTA-stacking technique has a limitation when it comes amplifier's input-referred noise and power tradeoff. The benefits saturate as one also needs to increase the supply voltage to accommodate stacking. However, for the tradeoff between dynamic range and the power, the OTA-stacking technique offers direct improvements, as explained in detail later. Hence, the stacking technique forms an excellent choice for oversampled data-converters.

The stacking technique was applied to a continuous-time delta sigma modulator (CTΔΣM). A classical audio application was chosen for benchmarking purposes. Improvements in the ADC figure of merit (FoM), which was originally introduced in an audio ADC [14], have been shown via measurements from two ADCs. Several other techniques such as finite impulse response (FIR) feedback, four stage feedforward compensation, chopping, etc. have been integrated to achieve the high-performance specs of an audio application.

1.5 Short-range Transmitters for Connected Health

The data acquired by the front-end of the IoT node needs to be relayed to a nearby base station. Contrary to the sensor front-end, the transmitter is usually not functional continuously but

is aggressively duty-cycled. However, since the instantaneous/peak power consumption for transmission is much higher, especially compared to a biosensing front-end, power-efficient operation of the transmitter is equally important. Due to the low output transmission power requirement, the frequency synthesizer used to generate the RF carrier is the power-hungry component in these transmitters, not the power amplifier, as in conventional radios. Low-power ring oscillator-based injection-locked clock multipliers (ILCMs) without dedicated frequency tracking loops (FTLs) or phase locked loops (PLLs) are widely accepted as the state-of-the-art. However, in practice, this comes at the expense of unwanted sensitivity to process, voltage, and temperature (PVT) variations. Towards this end, a technique based on multi-phasor generation using an *RC* polyphase-filter for PVT-robustness was proposed [15] and forms another part of this dissertation work.

1.6 Thesis Organization

The dissertation presents circuit techniques for power efficiency enhancement over multiple key components of an IoT wireless sensor node. These are demonstrated through: 1) an ultra-low power chopper-stabilized amplifier for implantable ECG recording application, 2) a precision audio-band continuous-time delta-sigma ADC and, 3) a low power short-range, narrowband MedRadio transmitter. The amplifier and the ADC use a proposed OTA-stacking technique as the core novelty. The stacking technique is generic in nature and can be applied to a wide variety of sensor front-ends. The transmitter utilizes a proposed PVT-robust frequency synthesis which is again general purpose in nature and can be applied to several applications that injection-locking techniques for a small frequency multiplication factor. The prototype chip implementations of the ECG amplifier in 180 nm CMOS, audio ADC in 65 nm CMOS, and the

MedRadio transmitter in 22 nm CMOS FDX are described in Chapter 2, Chapter 3, and Chapter 4, respectively. Finally, Chapter 5 concludes this dissertation with a summary and future directions.

Chapter 2.

A 13.9-nA ECG Amplifier using OTA-Stacking

2.1 Introduction

The Internet-of-Things (IoT) concept has created widespread interest in miniaturized sensor nodes ranging from biological sensors for healthcare monitoring [10], [16]–[22] to physical sensors for infrastructure, industrial, and environmental monitoring [23]–[25], as illustrated in Figure 2.1(a). From a healthcare perspective, there is significant interest in implantable devices due to their unobtrusive nature, improved environmental artifact tolerance, and that some biological signals can be only be obtained *in vivo* [26], [27]. With respect to an electrocardiogram (ECG) recording, the focus of this work, the key benefits associated with implantable operation include a stronger signal [28], better rejection of interference (*e.g.*, 50/60 Hz) [2], and immunity to motion artifacts and baseline wander owing to a more robust electrode-tissue contact [29], [30].

However, to realize the unobtrusive form factor there are constraints on the allowable battery capacity. For example, the state-of-the-art commercial 7 mm^3, 190 μWh thin-film battery [31] enables a 1-year lifetime when the sensor is limited to 20 nW. Similarly, state-of-the-art energy harvesters offering 7.4 $\mu W/cm^3$ power density [32] translate to a 3 mm^3 device for the same

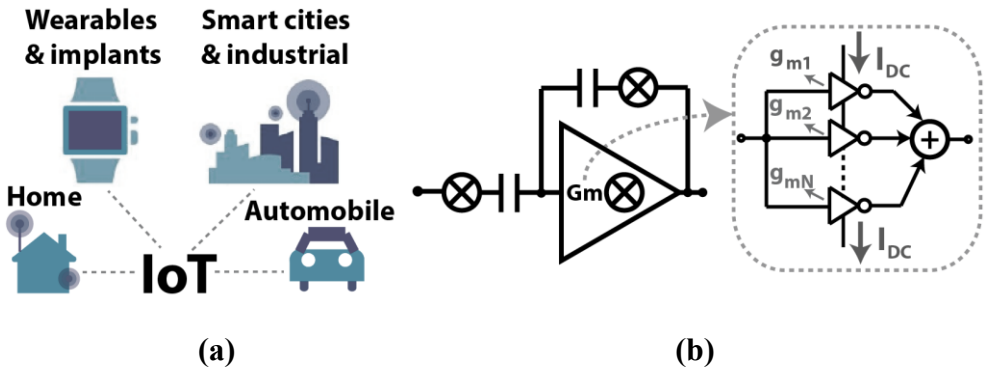


Figure 2.1 (a) Examples of IoT sensor-node applications and (b) block diagram of the proposed OTA-stacking technique.

20 nW power budget. This is a very challenging aspect for the realization of implantable devices that acquire high fidelity bio-signals and simultaneously require long lifetimes. While several µW-level ECG analog front-end (AFEs) for wearable applications were reported over the last decade [33]–[35], recent AFEs intended for implantable applications must deal with even more stringent power budgets [16], [17].

For most sensors, including ECG, the amplifiers in the AFE sense weak, low-bandwidth signals and are noise-limited. Improving their noise efficiencies has always been an important design objective, often quantified using metrics such as the noise efficiency factor (NEF) and power efficiency factor (PEF). To improve the energy-efficiency, a new technique based on OTA-stacking with chopping, as shown in Figure 2.1(b), was proposed in [12] and is implemented here. This is an extension of the classical current reuse technique where the transconductances are summed [36]–[38]. The proposed technique fits nicely with capacitively coupled amplifier topologies used for bio-potential recordings and, despite a shortcoming of increased area, which only marginally impacts the overall device form-factor considering the large battery dimension

needed for high longevity, is a useful technique for implantable ECG sensors wherein ultra-low power operation is critical.

To explore the design space, prototype ultra-low power ECG amplifiers with 3- and 5-stack versions were designed and fabricated in a 180 nm CMOS process. The 3- and 5-stack designs consume 13.2 and 18.7 nW, respectively. State-of-the-art NEF and PEF metrics of less than unity, 0.86 and 0.99, respectively, are reported. The rest of the chapter is organized as follows: Section 2.2 briefly reviews the NEF and PEF metrics and prior art. Section 2.3 introduces the proposed stacking technique. Section 2.4 describes the circuit architecture followed by implementation details in Section 2.5. Measurement results and a conclusion are presented in Sections 2.6 and 2.7, respectively.

2.2 Amplifier Noise Efficiency: Background

The NEF and PEF metrics and relevant prior work are briefly reviewed to set the stage for the proposed work. The NEF, introduced in [39], captures the noise-current tradeoff

$$NEF = v_{\mathrm{ni,rms}}\sqrt{\frac{2I_{\mathrm{tot}}}{V_{\mathrm{T}}4k_{\mathrm{B}}T\pi BW}} \tag{2.1}$$

where V_{T} is the thermal voltage, k_{B} is Boltzmann's constant, T is the temperature, I_{tot} is the amplifier's current, BW is its bandwidth, and $v_{\mathrm{ni,rms}}$ is its input-referred noise. The NEF benefits from maximizing the transconductance efficiency, $g_{\mathrm{m}}/I_{\mathrm{D}}$, where g_{m} is the transistor's transconductance and I_{D} is the drain current. A common technique to achieve this is to bias the transistors in subthreshold [40]. Correspondingly, a theoretical limit NEF_{o} is set [41], which for a

fully-differential topology with κ, the gate coupling coefficient, being 0.7, and considering only the input pair's thermal noise, evaluates to

$$NEF_{\mathrm{o}} = \sqrt{2/\kappa^2} \cong 2.02 \tag{2.2}$$

This implies that even with optimal sizing, a designer can, *at best*, achieve an NEF of 2.02. Overcoming this limit has therefore been the subject of intense research [12], [34]–[38].

The concept of current reuse is commonly employed in this regard and has taken several forms over the years. The most simplistic form is to use inverter-based OTAs to double the transconductance [42], [43] and reduce the NEF limit to 1.43. Stacking can further increase the extent of the current reuse. To the authors' knowledge, this was originally proposed in a patent [44] and although not intended for noise benefit, the same current was reused among independent amplifiers in a multi-channel configuration to save power. More recently, this idea was proposed in [45] by stacking differential-pairs for orthogonal current reuse among multiple channels. An analogous single channel version was subsequently proposed with chopper amplifiers in [36] by applying the same input modulated/chopped at different frequencies onto stacked differential-pairs. For the ADC in [37], inverter-based OTAs were stacked and a closed-loop, switched capacitor amplifier was realized using split arrays of feedback and sampling networks corresponding to each stacked stage. A technique involving an ac-coupled OTA with applicability for capacitively-coupled, closed-loop chopper amplifiers was proposed by the authors in [12], which is the basis behind the implementation in this work. Another recent work [38] has also utilized the stacking concept for a closed-loop amplifier and is a continuous-time counterpart to [37] using split-capacitor arrays. Aside from amplifiers, this stacking technique has also been used in a crystal oscillator to leverage the G_{m}-boosting and sustain oscillation with lower power [46].

While both the NEF and PEF are used in practice as metrics, the PEF, defined in [47] as NEF^2V_{DD}, is more relevant in quantifying a low power design since it captures the actual noise-power tradeoff with V_{DD} being the supply voltage. Incidentally, the previous best reported PEF was from a low supply (0.45 V) design using a simple dual-tail inverter-based OTA with two-fold current reuse [48]. Although, prior work with six-fold amplifier stacking [36], [38] have reported superior NEFs, the PEFs are worse. This stems from overheads of associated summation circuits resulting in the NEF not scaling aggressively enough to counter the required increase in supply voltage.

Other techniques to improve the PEF include removing the tail source to operate the first stage of a two-stage amplifier at a lower supply voltage (0.2 V) [49] and dynamically reconfiguring the amplifier for data-dependent power savings [12]. The former requires an additional common-mode rejection (CMR) circuit with power overhead. Furthermore, the CMR functionality is inevitably compromised being only possible for low frequencies and requires the chopping frequency to be much higher than the desired CMR frequency range, which is not always feasible at such low power levels. Dual supply generation is another shortcoming. The latter work relies on an ECG specific quasi-periodicity signal property and is not generalizable to all applications. Another NEF/PEF reduction technique was proposed in [50] by sharing parallel OTAs for the reference electrode but is applicable only for neural array applications.

A common drawback of prior amplifier stacking implementations is the use of additional power consuming circuits for the output summation. In [36], 4$^{\mathrm{th}}$-order filters are required and the implementation is open-loop with limited linearity. In [37], [38], active circuits are required to sum the currents. Another significant shortcoming is the single gain stage, which is a consequence of the proposed implementation wherein the summation currents are driven onto arrays of feedback

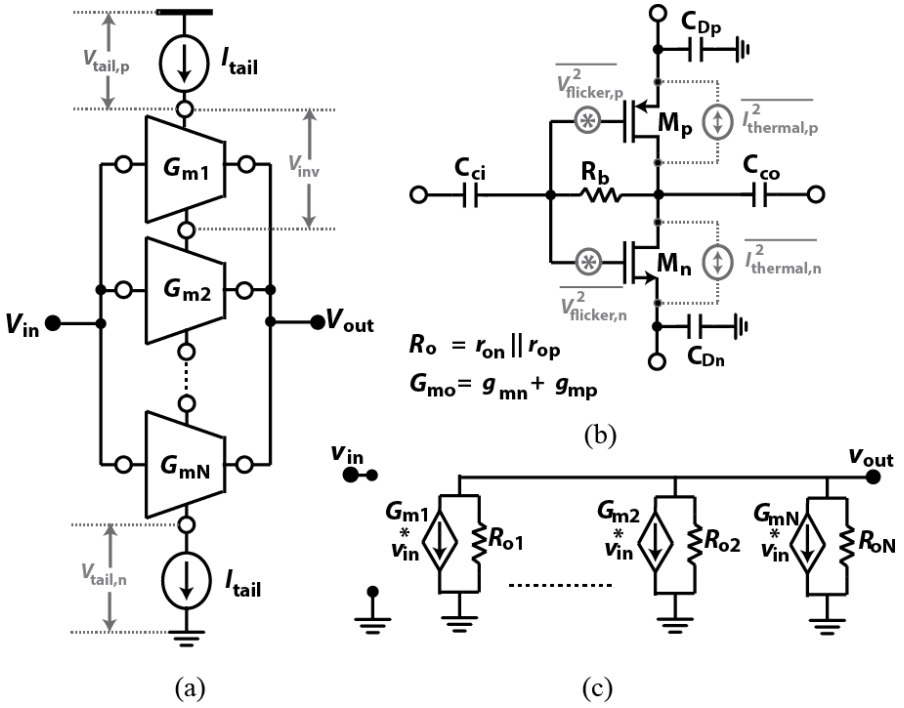


Figure 2.2 Schematic of the proposed (a) stacked OTA, (b) ac-coupled inverter-based transconductor, and (c) equivalent small-signal model.

capacitors of the same amplifier and is needed to realize the G_m-boosting. The closed-loop gain, gain accuracy, and linearity are limited if the open-loop single stage gain is not high enough. Noise attenuation from succeeding stages is also lowered. Finally, circuit complexity is increased if additional loops (*e.g.*, impedance boosting, offset rejection, etc.) also needed to be arrayed.

2.3 OTA-Stacking Principle

The proposed OTA-stacking principle and the resulting noise-efficiency benefits are explained in this section with the help of a single-ended version for simplicity. As shown in Figure 2.2(a), multiple OTA stages are stacked on top of one-another. Each stage is realized as an inverter

that traditionally offers a 2× transconductance improvement ($g_{mp} + g_{mn}$) and, as shown in Figure 2.2(b), is self-biased through the same, reused dc current, I_{tail}. Since all the transistors operate in subthreshold carrying the same current, each stage has an identical small-signal equivalent circuit exhibiting the same transconductance $G_{mo} = 2\kappa I_{tail}/V_T$ and the same output impedance, R_o. Furthermore, the inputs and outputs are all ac-coupled through capacitors, C_{ci} and C_{co}, respectively. The adjacent stacked stages, on the other hand, are decoupled from one-another using $C_{Dp,n}$. In a differential implementation, as will be discussed later, this decoupling occurs inherently with the relevant nodes being virtual grounds in the differential-mode operation. This ac-coupling and decoupling results in the simplified small-signal equivalent circuit shown in Figure 2.2(c) wherein all the individual transconductances, G_{mi}, sum and the output impedances appear in parallel. Thus, the overall compound transconductance, G_m, from stacking *N* stages is increased by the factor *N* and the compound output impedance, R_{out} is reduced by *N*. The open-loop gain of this stacked OTA remains the same as that of a single stack.

2.3.1 Input-referred Noise

Although the OTA-stacking does not offer any improvement in the gain, it results in lower noise. Since the thermal noise currents from each stacked transistor shown in Figure 2.2(b) are uncorrelated, they sum at the output. Henceforth, owing to the G_m-boosting, the total input-referred thermal noise power spectral density (PSD) from stacking *N* inverter-based OTAs is

$$\overline{v_{ni,thermal}^2} = \frac{4k_B T\gamma}{2Ng_m}, \tag{2.3}$$

where γ is a technology dependent noise coefficient. Thus, there is a reduction in the thermal noise power by a factor of 1/*N*. The flicker noise, henceforth referred to as 1/*f* noise, can be found by modelling each transistor's noise contribution as a voltage source in series with the gate, as shown

in Figure 2(b). Assuming these flicker noise sources also result in uncorrelated output noise currents that add-up, the total input-referred 1/f noise PSD from stacking N inverter-based OTAs is

$$\overline{v_{\mathrm{ni},1/f}^2} = \frac{1}{4Nf}\left[\frac{K_\mathrm{n}}{C_\mathrm{ox}(WL)_\mathrm{n}} + \frac{K_\mathrm{p}}{C_\mathrm{ox}(WL)_\mathrm{p}}\right]. \tag{2.4}$$

where $K_{n,p}$ are technology-dependent noise constants for NMOS and PMOS devices, respectively, C_ox is the oxide capacitance per unit area, W and L are the transistor sizes, and f is the frequency. Thus, the 1/f noise is also reduced by the same 1/N factor due to OTA-stacking. However, 1/f noise from stacked devices may exhibit partial correlation, and hence, the noise reduction is not direct. This is because the 1/f noise is known to have a dependence on the drain current and its fractional changes due to charge traps [51] and the drain current flowing through one device in a stack is also dependent upon the noise of the other devices. It may be noted that the actual noise reduction factor in (2.4) cannot be measured and hence cannot be conclusively stated. Nevertheless, chopping removes the 1/f noise, whereas the white noise, which is uncorrelated, has obvious benefits from the proposed stacking.

2.3.2 NEF/PEF Improvements

With chopping, the reduction in thermal noise by a factor discussed in (2.3) translates to an improvement over the NEF_o in (2.2) by a factor $\sqrt{2N}$ given the other amplifier parameters like BW and I_{tot} in (2.1) remain the same. Thus, the theoretical NEF limit for a 3-stack of inverters is improved by $\sqrt{6}$ to 0.82 and a 5-stack is improved by $\sqrt{10}$ to 0.63. These improvements suggest that larger N would continue to improve the amplifier's efficiency. While the NEF does continue to benefit from increasing N, the PEF saturates since one also needs to increase the supply voltage

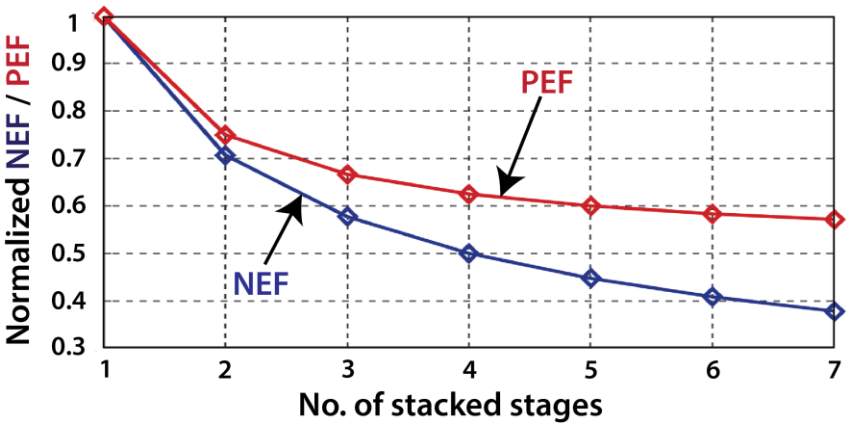


Figure 2.3 Tradeoffs associated with the number of stacked stages

to accommodate the increased number of stacked stages. For the stacked-OTA in Figure 2.2(a), one can express the minimum operable supply as

$$V_{\mathrm{DD},min} = NV_{\mathrm{inv}} + V_{\mathrm{tail}}\,, \tag{2.5}$$

where V_{inv} and V_{tail} are the voltage headrooms allotted to each inverter and the combination of the two tail current sources (*i.e.* $V_{\mathrm{tail,p}} + V_{\mathrm{tail,n}}$ in Figure 2.2). With the NEF $\propto 1/\sqrt{N}$, it follows that the PEF corresponding to the minimum supply voltage in (2.5) is

$$PEF = V_{\mathrm{inv}} + \frac{V_{\mathrm{tail}}}{N}\,. \tag{2.6}$$

As N becomes large, V_{tail}/N is small relative to V_{inv} and thereby further increasing N only marginally improves the PEF. For illustrative purposes, plots of the normalized NEF and PEF with $V_{\mathrm{inv}} = V_{\mathrm{tail}}$ (*i.e.* equal headroom across the drain-source terminals of each transistor) are shown in Figure 2.3. It may be noted that a minimum PEF can be obtained by removing the tail source altogether without any OTA-stacking; however, tail sources are necessary to establish a well-defined nA-level current and to achieve good CMR. Overall, OTA-stacking helps in that it

Table 2.1

Effect on Circuit Parameters with N× Inverter Stacking

Parameter	Effect	Parameter	Effect
G_m	↑ N ×	R_o	↓ N ×
A_v		BW	↑ N ×
$\overline{v_{n1,thermal}^2}$	↓ N ×	$\overline{v_{n1,1/f}^2}$	↓ N ×
NEF	↓ $\sqrt{N}$ ×	PEF [#]	↓ 2/(1+1/N) ×
$V_{DD,min}$	↑ (N+1) ×	Area	↑N ×

[#] For $V_{inv} = V_{tail}$

diminishes the tail source's power contribution. It may also be noted that a single-ended amplifier exhibits a lower NEF limit of 0.7 [52] for 1-stack, which improves similarly with stacking and should be used if the application permits.

2.3.3 OTA-Stacking Tradeoffs

Table 2.1 summarizes the effect of OTA-stacking on various amplifier parameters. The G_m-boosting also results in an N× increase in the bandwidth. Although, the bandwidth requirement for the targeted application is not important, there are benefits with respect to chopping wherein a higher bandwidth is needed by the stage processing the upmodulated chopped signals. This aids in easier settling of upmodulated signals thereby reducing the chopper settling spikes/ripple. A potential drawback of the OTA-stacking is that it leads to a slight increase in the input parasitic capacitance degrading the feedback factor and thus the input-referred noise in a closed-loop amplifier. Inevitable drawbacks are the increase in area and supply voltage which needs to be traded for improvements in the power efficiency.

2.4 ECG Acquisition Amplifier

2.4.1 Application-Specific Requirements

An important requirement while amplifying weak ECG signals is to introduce minimal noise. The noise specification typically depends on the downstream signal processing. Early ECG AFEs such as [18] targeted an input-referred noise floor ~60 nV/√Hz to ensure high accuracy at the expense of μW-level power consumption. However, stringent power budget of a few tens of nWs is more critical for implantable sensors. Ultra-low power AFEs exhibiting 250 and 1,400 nV/√Hz noise floors have hence been reported in [17] and [16], respectively, and are applicable for arrhythmia detections. Accurate QRS-detection with a noise floor of 126 nV/√Hz has been demonstrated in [10]. In this work, a 150 nV/√Hz noise floor is targeted while meeting a stringent power budget of less than 20 nW.

Aside from the power budget, there are additional requirements, namely: 1) The $1/f$ noise that would otherwise be dominant in the bandwidth of interest must be mitigated. 2) Due to electrode polarization, a large dc offset appears at the amplifier inputs and must be rejected to avoid saturating the amplifier. 3) Implantable ECG devices use electrodes that are in direct contact with subcutaneous tissue [53]. The associated electrode-tissue impedances are typically high (~100 kΩ) for implantable electrodes [54] and hence the input impedance of the AFE should be sufficiently higher to prevent signal attenuation and avoid other issues/artifacts arising from electrode mismatch. 4) The recording environment is often prone to interference (*e.g.*, 50/60 Hz power line interference) and motion artifacts, thus high amplifier CMRR and PSRR are also important. It turns out that these additional considerations while being accounted for by using standard techniques have only a minimal impact on the power consumption compared to the noise specification. Improving the thermal noise efficiency by OTA-stacking offers significant benefit.

A few key challenges need to be addressed to employ the proposed OTA-stacking technique for an ECG amplifier. Since the ECG is a slowly varying signal (BW of ~250 Hz), ac-coupling at such frequencies would require large capacitors, possibly prohibitively large for an on-chip implementation. Furthermore, although OTA-stacking offers higher current-reuse, it limits the transistor's headroom lowering the allowable swing. The first concern can be resolved by upmodulating the baseband signals to a higher frequency using the well-established technique of chopper-stabilization, which is also required to mitigate the $1/f$ noise. The limited headroom issue can be addressed by using OTA-stacking only at low swing nodes, such as the first stage of a two-stage amplifier.

2.4.2 Architectural Overview

The capacitively-coupled chopper amplifier architecture shown in Figure 2.4 is similar to the ones presented in [55], [56]. Since the target specs are such that the noise requirement is far more stringent than the bandwidth, the first stage usually consumes a significant portion of the power budget and is a prime candidate for OTA-stacking. It is also clear that this stacked-OTA only processes upmodulated, low swing signals. As a result, the ac-coupling is naturally simplified since the signal of interest lies at the chopping frequency and the implementation is now possible using smaller, on-chip capacitors. Ensuring the operation of all stacked transistors in saturation becomes much easier with the associated voltage swings being negligible and helps maintain high linearity. The low swing also helps in that the G_m-boosting is strictly valid only for small signals.

Down-chopping is performed at an intermediate node before the second stage to suppress distortion due to chopper settling errors using the inherent feedback [55]. With the first stage outputs ac-coupled, the second stage requires additional biasing resistors R_b to set its dc input

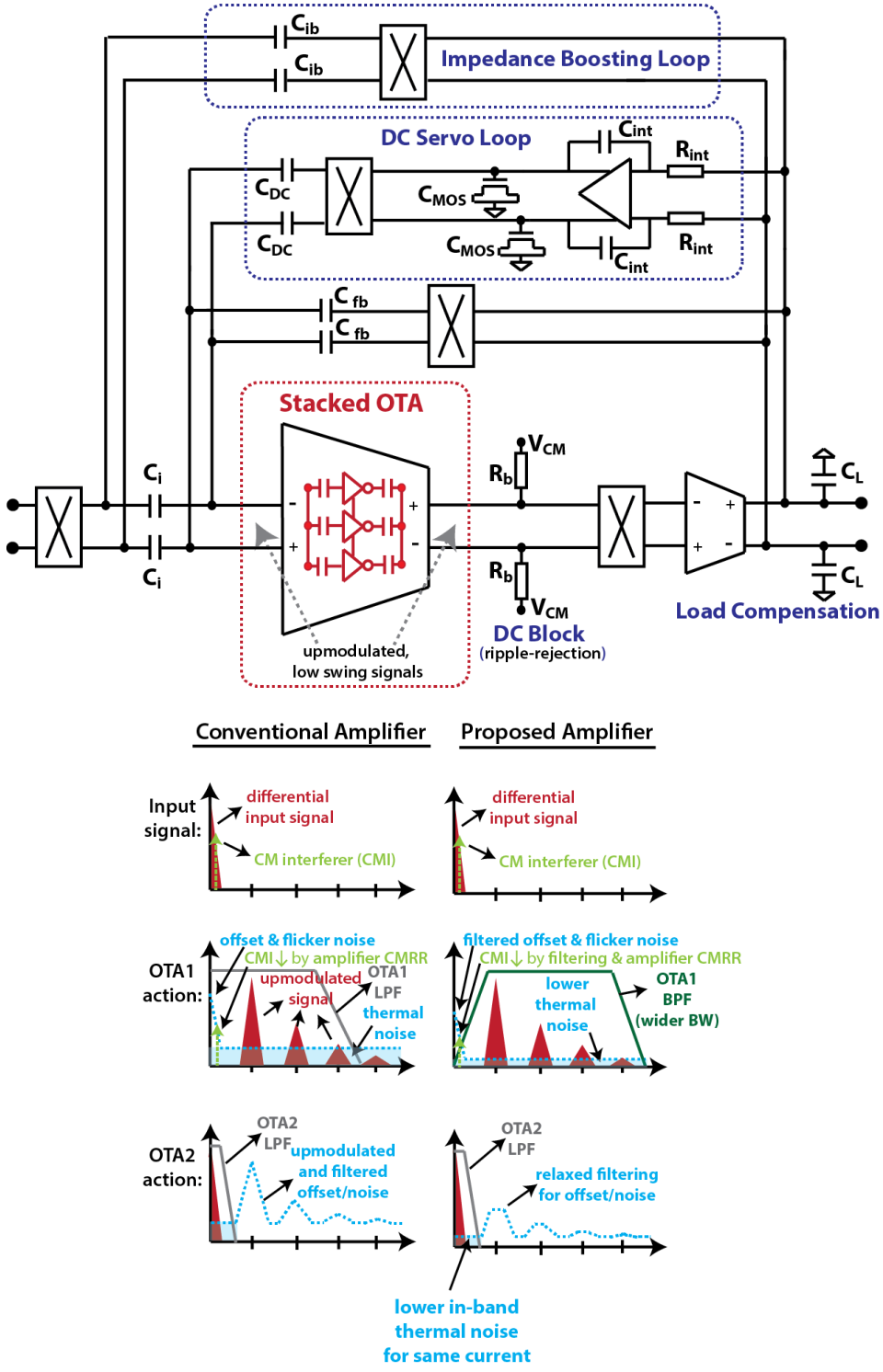


Figure 2.4 Chopper-stabilized ECG amplifier: architecture and illustration of functional benefits.

common-mode voltage. The coupling capacitors of the stacked-OTA along with these biasing

resistors result in high-pass filtering. The placement of R_{b} before the down-chopper ensures that the relevant up-modulated signals remain unaffected. Moreover, the dc-blocking between the first and second stages adds a ripple-rejection functionality to the amplifier [18]. It may be noted that the stacked-OTA also requires resistors for self-generation of the bias potentials that similarly adds to the dc-blocking action. Since low frequency common-mode interferers are not up-modulated by chopping, these are high-pass filtered by the first stage thereby further improving the CMR. To summarize, contrary to a conventional amplifier, the first stage acts as a band-pass filter rather than a low-pass filter with additional benefits of wider bandwidth and, more importantly, lower noise due to the OTA-stacking.

The closed-loop gain is set by the ratio between the input and feedback capacitors, $C_{\mathrm{i}}/C_{\mathrm{fb}}$. A dc servo-loop (DSL) is implemented to suppress the otherwise amplified dc electrode offsets appearing at the amplifier output by integrating them and cancelling at the input. The integrator is adopted from [57], which is fully realizable with on-chip components. The amplifier's high-pass cutoff frequency is set by the resistor R_{int} and capacitor C_{int} whereas the DSL OTA's noise is bandlimited using large-valued MOS-capacitors, C_{MOS}. To address the degraded impedance at the input due to chopping before C_{i}, a positive feedback-loop compensates the charge transfer boosting the input impedance [56]. The two-stage amplifier is load compensated for reasons discussed in the next section.

2.5 Circuit Implementation

The details of key circuit blocks and the associated design considerations are discussed below.

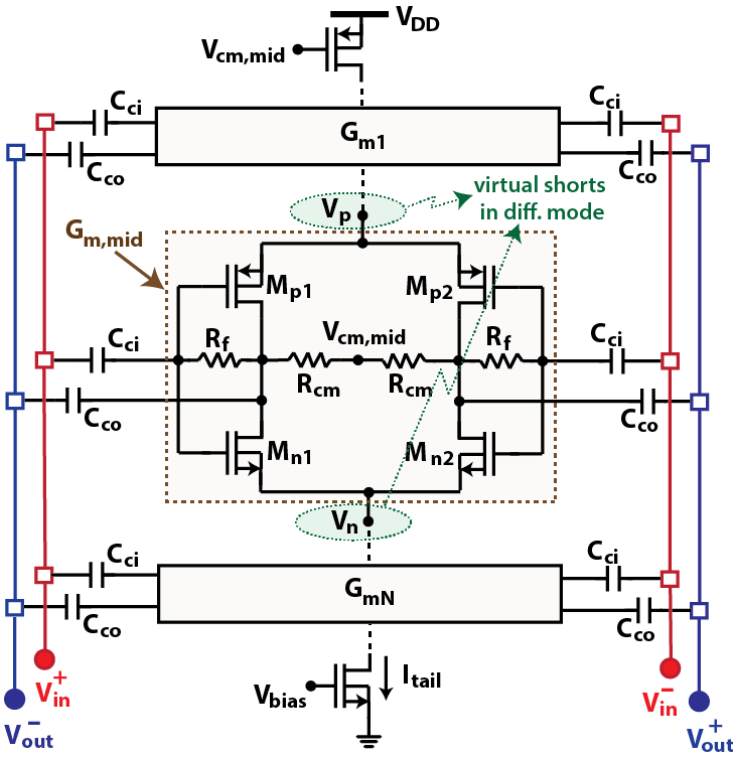
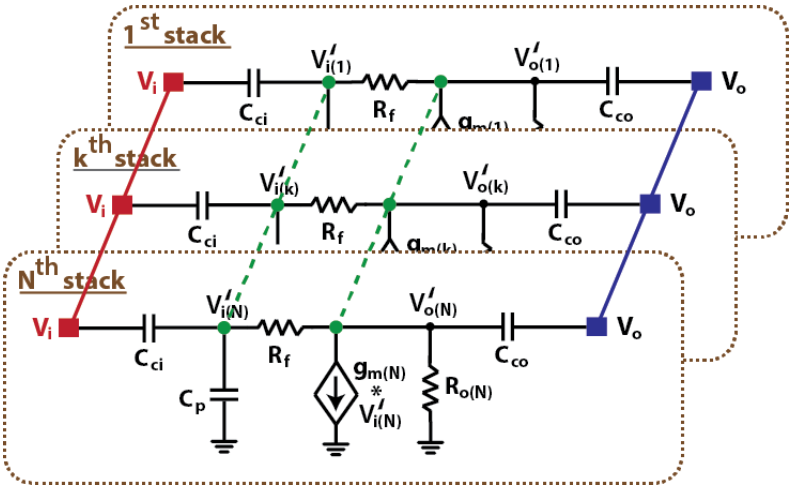


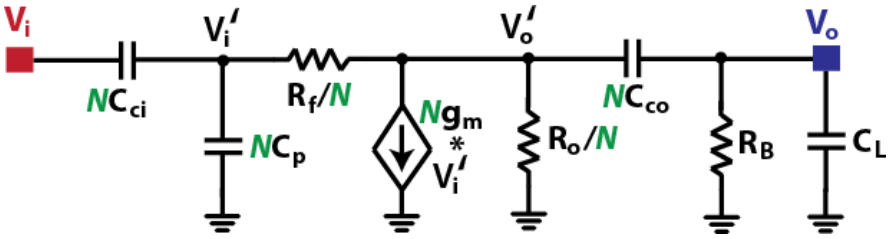
Figure 2.5 Circuit implementation of the fully-differential stacked-OTA.

2.5.1 OTA Implementation

The fully-differential version of the implemented stacked-OTA circuit is shown in Figure 2.5. Each of the inverters is self-biased using resistive feedback through R_f, implemented as pseudoresistors. All the inverters' transistors have their body-source terminals tied together to avoid threshold voltage variation from the body-effect. This ensures symmetry to simplify and maintain robust operation from the self-biasing. The top transistors in the stack would otherwise have larger drain-source voltage, V_{DS} while the bottom ones would be pushed closer to triode. Deep N-well (DNW) devices were used to allow this body-source tie for the NMOS transistors. For both the 3- and 5-stack versions, transistors are sized such that nominally each inverter is allocated ~220 mV headroom leaving ~250 mV for the two tail sources. This guarantees that all



(a)

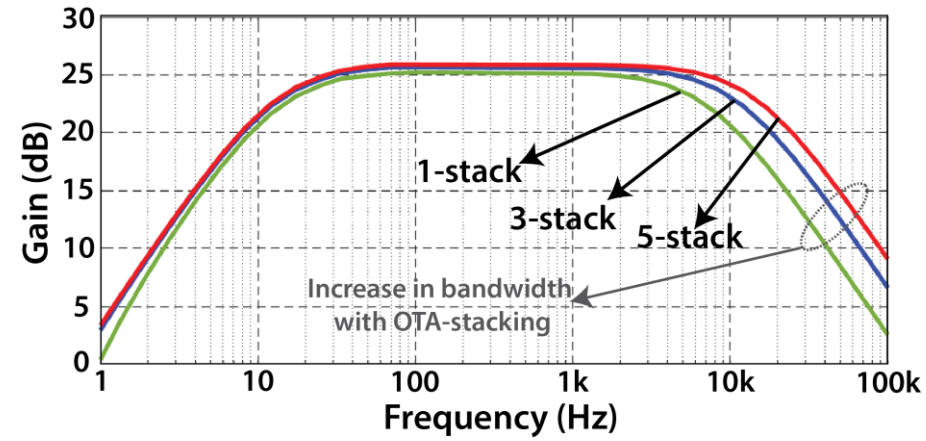


(b)

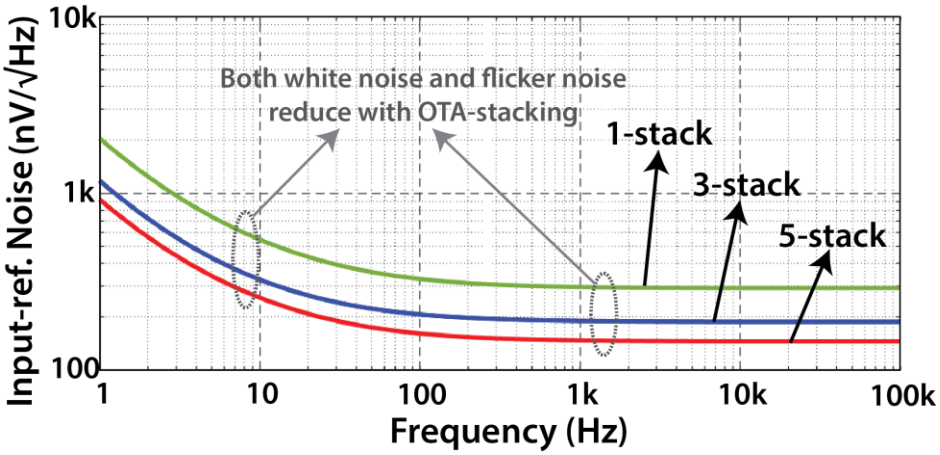
Figure 2.6 Differential-mode (a) small-signal model of the stacked-OTA and (b) equivalent simplified circuit.

the transistors in subthreshold, considering the associated swing, are always in saturation (V_{DS} > 100 mV) across process corners, including the most critical slow-slow corner. Although the first stage transistors are at the edge of saturation, the linearity is not compromised due to the negligible signal swing. The isolated DNWs have an area overhead that is negligible (<0.01 mm^2 for all transistors) compared to the coupling capacitor's area.

For the common-mode feedback (CMFB), a resistive divider senses the common-mode voltage of the central inverter to bias the top PMOS tail source. With this CMFB, the number of



(a)



(b)

Figure 2.7 Simulation of the stacked-OTA showing (a) open-loop frequency response and (b) input-referred noise.

stacked stages is chosen to be odd as vertical symmetry is maintained. The overall amplifier is designed such that the dc gain from first stage is ~25 dB while the second stage is ~45 dB, thus the swing at the intermediate node is negligible. The second stage is implemented as a traditional inverter-based OTA with CMFB as in [1]. For higher intrinsic gain, I/O transistors are used in the second stage.

2.5.2 AC-coupling/decoupling of Stacked-OTAs

For proper ac-coupling, the capacitor values for C_{Ci} and C_{Co} shown in Figure 2.5 need to be selected such that their impedances at the chopping frequency (1.5 kHz) are sufficiently smaller than the remaining impedance seen at that node. In other words, the high-pass cutoff frequency, ω_{HPF} should be low enough to not affect the up-modulated signals. From the differential-mode small-signal model and the equivalent reduced circuit shown in Figure 2.6, it can be found that the dominant contributors to ω_{HPF} are the feedback resistor R_{f} and capacitor C_{Ci}. Thus, ω_{HPF} is independent of *N* and expressed as

$$\omega_{HPF} \approx \frac{1}{(R_{\mathrm{f}} + R_{\mathrm{o}})/(1 + G_{\mathrm{mo}}R_{\mathrm{o}})C_{\mathrm{ci}}}. \tag{2.7}$$

With R_{f} being implemented as pseudoresistors offering high impedance, meeting this ac-coupling criterion is easy in practice. Additional constraints from attenuation of the open-loop gain perspective, however, need to be considered. As evident from Figure 2.6, the mid-band gain, A_{v1} of the stacked-OTA is attenuated by capacitive dividers

$$A_{\mathrm{v1}} \approx \frac{C_{\mathrm{Ci}}}{C_{\mathrm{Ci}} + C_{\mathrm{p}}}\, G_{\mathrm{mo}}R_{\mathrm{o}}\, \frac{NC_{\mathrm{Co}}}{NC_{\mathrm{Co}} + C_{\mathrm{L}}}, \tag{2.8}$$

where C_{p} is the total input gate capacitance of each inverter stage and C_{L} is the load seen by the overall OTA. With chopping, there is no need to increase the area of the transistors for $1/f$ noise reasons, thus C_{p} can be kept to a minimal size owing to the ultra-low nA bias current. Minimizing the output attenuation however has implications for the compensation used and is discussed later. It may also be noted from (2.8) that an increase in with the same loading helps slightly lower the output attenuation. Taking into consideration these aspects, C_{Co} and C_{Ci} were chosen to be 9.5 and 11 pF, respectively. While these values are larger than the minimal required values (C_{p} and C_{L} of

150 and 800 fF, respectively), the large coupling capacitors aid in the noise reduction and CMR, as discussed later. The input side coupling here is realized using multiple additional, but smaller capacitors, unlike prior works, such as [24], where multiples/arrays of the otherwise larger amplifier input capacitors, typically ~25 pF, for the application are used. Thus, the input coupling area overhead is lowered compared to prior work using stacked amplifiers. Additional area is needed for the output side coupling but with the benefit of the summation being performed passively without any power overhead.

Decoupling of adjacent stages occurs inherently owing to a fundamental property of differential amplifiers. The source nodes of the intermediate differential pairs (V_{p} and V_{n} in Figure 2.5) act as virtual grounds for small-signals in differential-mode. Explicit capacitors for decoupling are therefore not needed. Furthermore, since this decoupling occurs only with respect to the differential-mode operation while not affecting the common-mode operation, high CMRR and PSRR, as also analyzed later, are maintained.

The simulated open-loop frequency response of this ac-coupled stacked-OTA loaded by the second stage is shown in Figure 2.7(a). The band-pass nature is evident with a high-pass corner set by the dc-blocking action and the low-pass bandwidth being expanded due to the G_{m}-boosting. It is worth noting that this bandwidth expansion from OTA-stacking is also leveraged here to enable chopping at lower power levels. Assuming similar loading conditions, a 1-stack version has ~5 kHz bandwidth, which would not suffice to process the 3$^{\mathrm{rd}}$ (at 4.5 kHz) and higher harmonics of the upmodulated signal. This becomes feasible with the >12 kHz bandwidth offered by the 3- and 5-stack versions here. The improvements for both the $1/f$ and white noise are also shown in the simulated input-referred noise plots of Figure 2.7(b) leading to a lower NEF and PEF.

2.5.3 Load Compensation

The mid-band gain expression for the stacked-OTA in (2.8) indicates that it is important to minimize the load capacitance seen by the first stage to avoid unwanted gain attenuation. The use of conventional Miller compensation in this regard is problematic since the effective load $C_{\mathrm{c}}(1-A_{\mathrm{v2}})$ for a compensation capacitor C_{c} and second stage gain of A_{v2} would be very large. To avoid using a correspondingly large stacked-output coupling capacitor C_{co}, load compensation is instead employed. The first stage offers low gain and high bandwidth, which is advantageous since it processes upmodulated chopped signals. The high gain and low bandwidth second stage filters out the unwanted upmodulated components meanwhile also ensuring the swing is minimized. Compared to Miller compensation, which has the dominant pole associated with the first stage and wherein a higher second stage g_{m} aids the compensation, load compensation needs a lower second stage g_{m}, thereby making it easier to push the power burden solely onto the first stage in low bandwidth applications.

2.5.4 DC Servo-Loop

The offset cancellation using a dc servo-loop further benefits from the higher supply V_{DD} required for OTA-stacking. The maximum offset that can be cancelled can be expressed as $(C_{\mathrm{DC}}/C_{\mathrm{in}})V_{\mathrm{DD}}$, where C_{DC} and C_{in} are the servo-loop and the closed-loop amplifier's input capacitance, as shown in Figure. 2.4. This implies that with a higher V_{DD}, a smaller offset cancelling capacitor C_{DC} is needed for the same offset cancellation range. The closed-loop input-referred noise $\overline{v_{\mathrm{ni,amp}}^2}$ degrades as

$$\overline{v_{\mathrm{ni,amp}}^2} = \left(\frac{C_{\mathrm{in}}+C_{\mathrm{fb}}+C_{\mathrm{DC}}}{C_{\mathrm{in}}}\right)^2 \overline{v_{\mathrm{ni}}^2}\,. \tag{2.9}$$

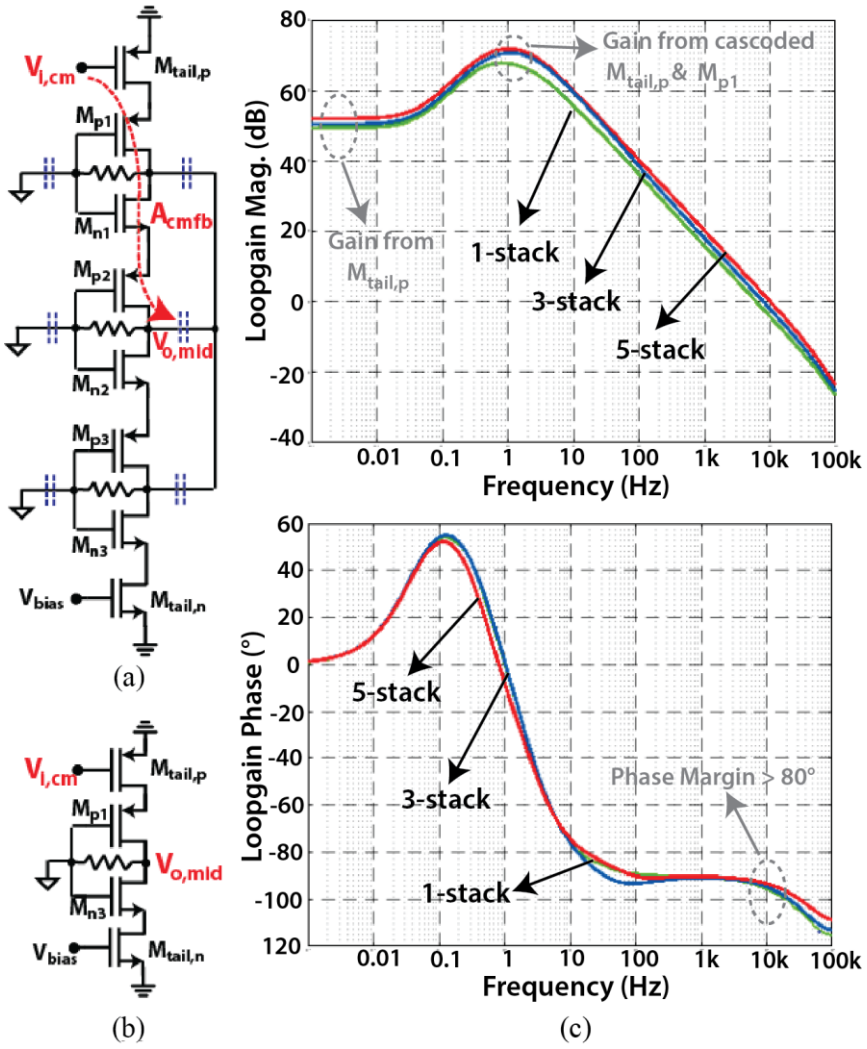


Figure 2.8 Common-mode (a) half-circuit, (b) equivalent simplified circuit for a 3-stack OTA, and (c) simulated CMFB loop-gain using stability (.stb) analysis.

Since the input capacitance at the virtual ground node is dominated by C_{DC}, there is a reduced degradation of the closed-loop input-referred noise to reject the same amount of offset.

2.5.5 CMFB Stability

Since the gain along the path from the tail current source to the central inverter, as highlighted in the common-mode half circuit of a 3-stack inverter in Figure 2.8(a), sees multiple

stacked/cascoded devices, it may appear at first glance that the stability of the CMFB loop would be difficult to ensure due to very high gain and/or multiple poles. However, because of ac-coupling, all the inputs are shorted to ground, and more importantly, all the outputs are shorted together. Thus, the intermediate transistors do not impact the common-mode response and hence the CMFB stability behavior is analogous to the 1-stack equivalent, as shown in Figure 2.8(b). It should be noted the assumption of perfect ac-coupling has been made, which is valid in the vicinity of the unity gain frequency of the CMFB loop and in general is the case for all frequencies above the cut-off set by the output coupling capacitor and the high output impedance (<1 Hz in this design). The simulated CMFB loop-gain is shown in Figure 2.8(c). The dc loopgain is determined solely by the tail source (since the inverter OTAs have a direct dc path through with unity gain at dc), while the mid-band gain is determined by the cascode of the tail source and the adjacent inverter. Both the 3- and 5- stacked versions exhibit similar frequency responses and the phase margin is greater than 80°.

2.5.6 Design Summary

The power breakdown of the two OTAs and the auxiliary components are summarized in Figure 2.9 and are identical for both the 3- and the 5-stack versions. The DSL OTA is implemented as a simple NMOS input fully-differential amplifier. All dc biasing resistors are implemented as high impedance pseudoresistors. The common-mode voltage, V_{CM}, to bias the second stage is generated using a reference ladder with four series diode-connected PMOS devices in sub-threshold. The bias currents for the OTAs are set by a constant-gm circuit using an external resistor. All capacitors in Figure 2.4 (except C_{MOS}) and the coupling capacitors in Figure 2.5 are implemented by MIM capacitors. All design values are identical for the 3- and the 5-stack amplifiers and summarized in Table 2.2.

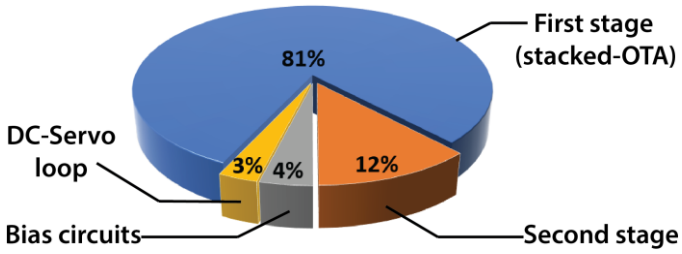


Figure 2.9 Power distribution for the ECG amplifiers.

Table 2.2

Device Sizes and Component Values

Stage 1 (stacked-OTA)			
$M_{pi}\left(\frac{W_p}{L_p}\right)$	$\frac{176\ \mu m}{0.18\ \mu m}$	$M_{ni}\left(\frac{W_n}{L_n}\right)$	$\frac{77\ \mu m}{0.18\ \mu m}$
C_{ci}	9.5 pF	C_{co}	11 pF
Capacitors			
C_i	23 pF	C_{fb}	400 fF
C_{DC}	1.8 pF	C_L	6 pF
C_{int}	4.5 pF	C_{ib}	400 fF
Currents			
Stage 1	11.25 nA	**Stage 2**	1.65 nA
Bias	560 pA	**DC-Servo**	420 pA

2.5.7 Amplifier Non-idealities with OTA-stacking

While offering reduced noise levels, it is important to ensure that the proposed OTA-stacking does not deteriorate other amplifier performance metrics. The potential amplifier non-idealities with OTA-stacking arising from mismatch and the presence of interferences are discussed in this section.

The headroom for each stacked inverter is minimal. It is hence possible that the swing and linearity at the amplifier's first stage output can get severely compromised due to the dc offsets

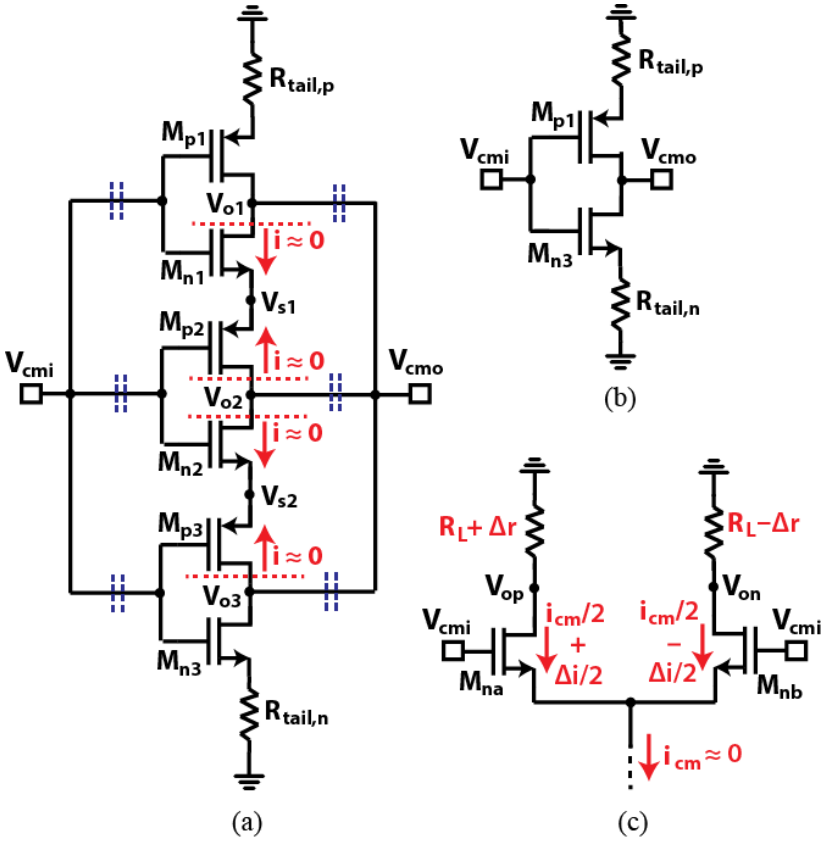


Figure 2.10 Common-mode (a) half-circuit, (b) equivalent simplified circuit for a 3-stack OTA, and (c) CMR by a mismatched differential pair.

resulting from mismatch. However, since each ac-coupled inverter has its own dc feedback through R_f, individual high-pass filtering avoids amplification of the offset from saturating the stacked inverters' outputs.

The behavior of the stacked-OTA from the common-mode rejection perspective is analyzed next. At low frequencies, the CMR is very good owing to the high-pass filtering as common-mode signals are not upmodulated by chopping. Additionally, in general, and at higher frequencies, the self-feedback mechanism, which results from the outputs being ac-coupled, assists

in maintaining a good CMR. This mechanism can be understood from the common-mode half-circuit of a 3-stack OTA in Figure 2.10(a), which is redrawn and annotated differently for the ease of explanation. Assuming perfect ac-coupling, it is evident that there can be no common-mode small-signal current flowing across the intermediate stacked transistors $M_{\mathrm{n1,2}}$, $M_{\mathrm{p2,3}}$, since the nodes $V_{\mathrm{o1,2,3}}$ are at the same potential. As such, the equivalent simplified circuit shown in Figure 2.10(b) results. Thus, the common-mode response (*e.g.*, the common-mode gain) is mostly determined by the top and bottom most transistors and the associated tail current sources. Although low impedances are seen looking into the source nodes of other intermediate transistors at $V_{\mathrm{s1,2}}$, implying the absence of a conventional source degeneration, the associated common-mode gain contribution from these intermediate stages is still very low.

In practice, mismatch causes additional non-idealities with respect to common-mode to differential-mode conversion. Although with chopping these unwanted signal components are later upmodulated and filtered out, it is still important that their signal levels are low in the first stage. The impact of mismatch among intermediate differential-pairs in this case is also reduced due to the above-mentioned self-feedback. This can be understood by first considering the CMR mismatched differential pair carrying a common-mode small-signal current, i_{cm}, as shown in Figure 2.10(c). In a traditional differential amplifier, the high impedance of the tail source causes the common-mode current to be minimal ($i_{\mathrm{cm}} \approx 0$) . As such, the absolute difference Δi (*e.g.*, due to mismatch) among the otherwise equally split versions of this small current is also small, thereby causing the resultant differential component $\Delta i R_{\mathrm{L}}$ to be small. Impedance mismatch, Δr, also results in a low differential amplitude $i_{\mathrm{cm}}\Delta r$. In the case of the stacked-OTA, the common-mode current associated with each intermediate differential pair is minimized by the self-feedback thereby assisting the mismatch related CMR in a similar fashion. Good CMRR/PSRR is henceforth

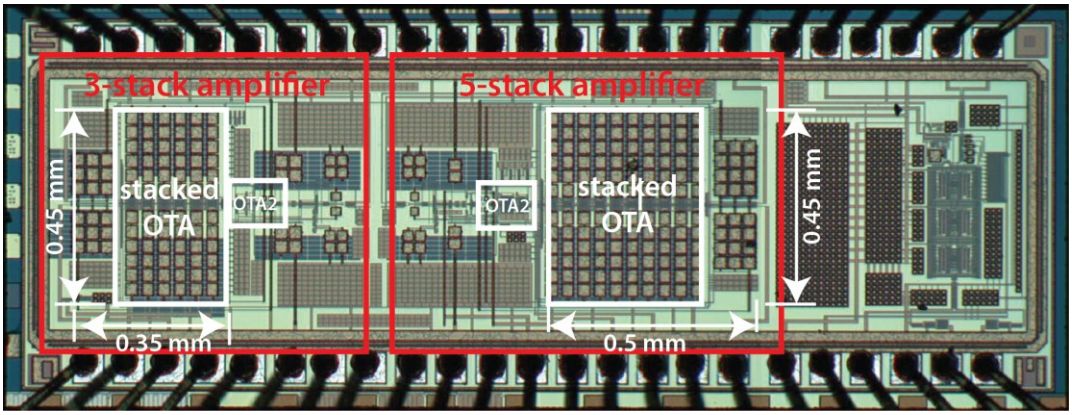


Figure 2.11 Annotated chip micrograph.

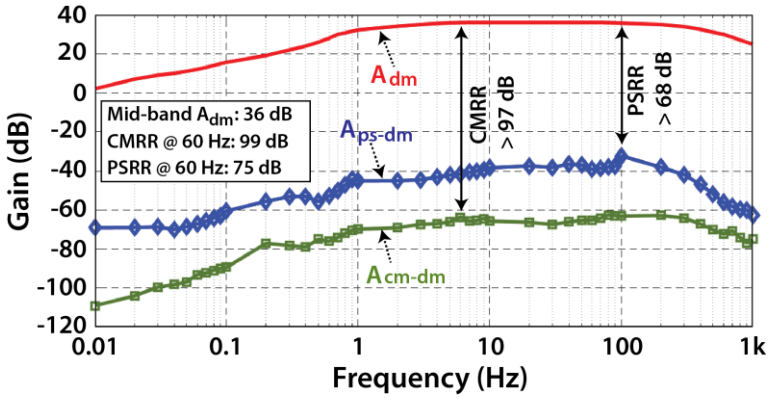


Figure 2.12 Measured 5-stack amplifier frequency response.

maintained with the high tail source impedances aiding the CMR for M_{n1} and M_{p1}, and the self-feedback doing the same for $M_{\mathrm{n1,2}}$ and $M_{\mathrm{p2,3}}$.

2.6 Measurement Results

Measurement results from prototype amplifiers with 3-stack and 5-stack versions are presented in this section. Fabricated in a TSMC 180 nm CMOS process, the two amplifiers occupy

a 2×1 mm^2 area including pads. The total active area occupied by the 3- and 5-stack amplifiers are 0.18 and 0.24 mm^2, respectively and mostly dominated by the MIM capacitors. An annotated chip micrograph is shown in Figure 2.11. The nominal supply voltages selected for the 3-stack and 5-stack versions are 0.95 V and 1.35 V, respectively. It should be noted that in comparison with the prior best reported PEF work [48] wherein a 0.45 V supply (0.2 V for inverter and 0.25 V for tail sources) was used for a four transistor inverter-based OTA, the supply voltages here are higher (analogous headroom allotment would lead to 0.85 V and 1.25 V supply for 3- and 5-stack, respectively). The supply voltages were chosen to maintain robust operation and consistent linearity, as discussed later.

Both the amplifiers exhibit a measured closed-loop mid-band gain of 36 dB with a bandwidth of 240 Hz. The measured frequency response of the 5-stack amplifier is shown in Figure 2.12. The CMRR and PSRR for both versions measured over multiple chips (n=10) is greater than 95 dB and 68 dB, respectively. The input impedance of the 5-stack amplifier was boosted from 9 to 93 MΩ whereas the 3-stack was boosted to 87 MΩ. The benefits of the increased supply voltage for the DSL (with same C_{DC} for both versions to provide more than ±50 mV offset cancellation) were also observed through measurement. The measured residual offset at the amplifiers' outputs normalized by the respective supplies versus the applied dc input are plotted in Figure 2.13. Offsets of ±50 mV and ±70 mV can be tolerated by the 3-stack and the 5-stack versions, respectively, without saturating the amplifier.

The measured input-referred noise PSDs are shown in Figure 2.14. Both the amplifiers consume an ultra-low 13.9 nA current that would typically result in a white noise PSD of 350 nV/√Hz using a single stack inverter-based OTA. The improvements with further stacking are clearly seen. The input-referred noise floor exhibited by the 3-stack amplifier is ~200 nV/√Hz

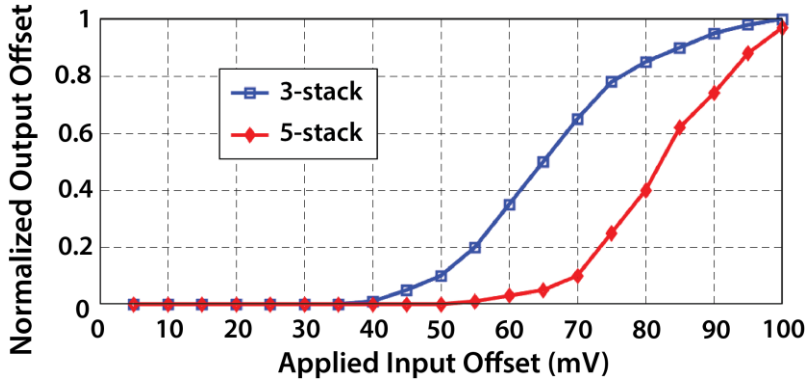


Figure 2.13 Measured dc offset tolerance.

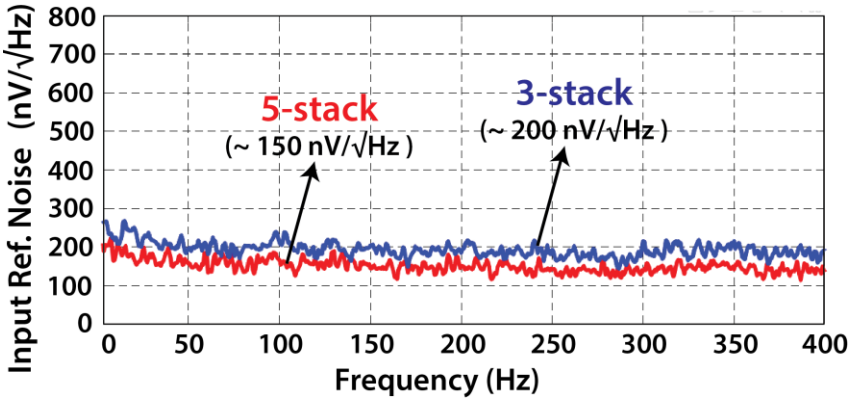


Figure 2.14 Measured amplifier input-referred noise.

while that for the 5-stack amplifier with further current-reuse is lowered to ~150 nV/√Hz. The corresponding measured NEF and PEF for the 3-stack version are 1.08 and 1.12, respectively. These are improved to 0.86 and 0.99, respectively for the 5-stack version. To demonstrate robust operation over temperature, measurements of the NEF were taken from -40 to +80 °C. As evident from Figure 2.15, the NEF for both amplifiers remains consistent over a -10 to +70 °C temperature range. This is readily acceptable for body implanted operation where the temperature sensitivity requirement is relaxed owing to proximity to the human body.

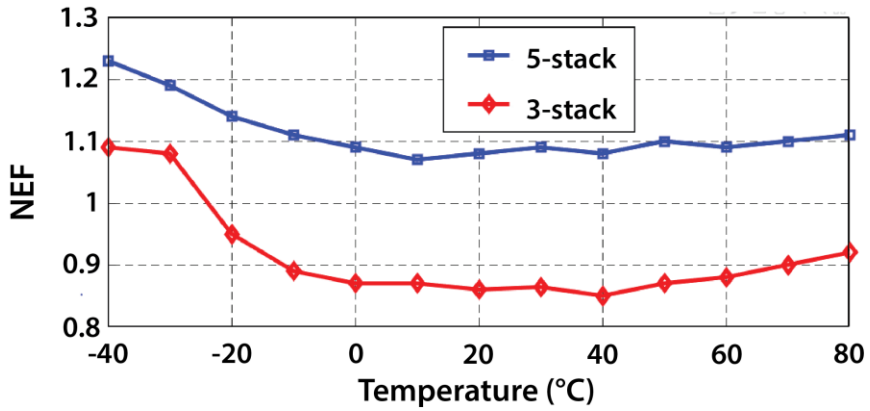
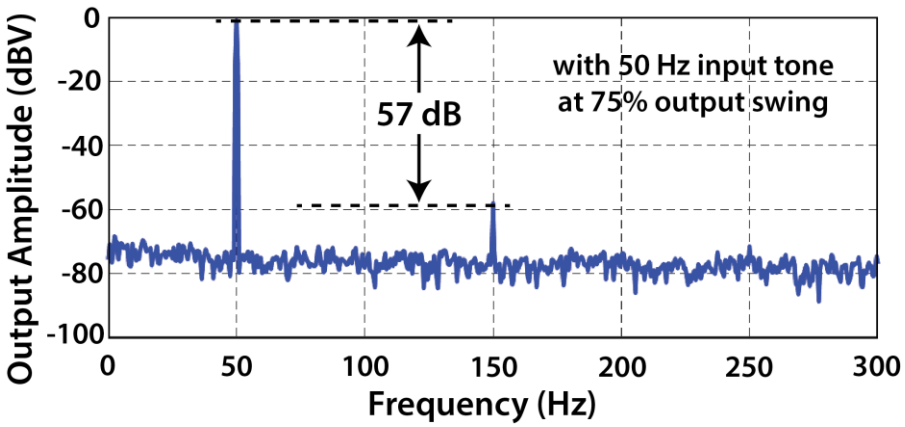
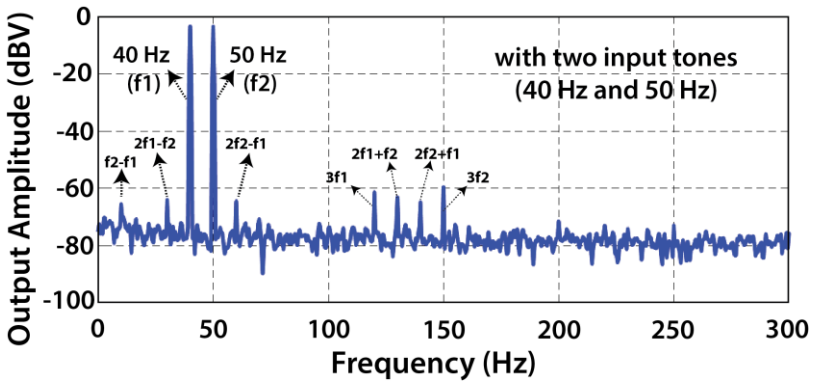


Figure 2.15 Temperature sensitivity of the amplifier.

The measured linearity for the 5-stack version are shown in Figure 2.16(a) and (b). With an output swing of 75% of the supply voltage, the amplifier has a measured total harmonic distortion (THD) of 0.16% (56.7 dB SFDR or 9-bit linearity) which suffices for ECG recording. Based on simulations, the linearity is limited by the 1.5 nA second stage rather than the DSL pseudoresistors. Figure 2.16(b) shows the two-tone linearity measurements. The resultant intermodulation tones are as expected and have low amplitudes consistent with the linearity measured from the single-tone test. This implies there is no unwanted crosstalk between the stacked OTAs that would otherwise have resulted in degraded and possibly additional intermodulation products. The amplifiers' linearity performance with supply variation is shown in Figure 2.16(c) justifying selected supply voltage. For the 5-stack amplifier, good linearity above 1.25 V is maintained implying a robust operation at the chosen 1.35 V supply. For each of these measurements the input amplitude of a 50 Hz tone is adjusted to maintain an output swing that is 75% of the supply voltage used.



(a)



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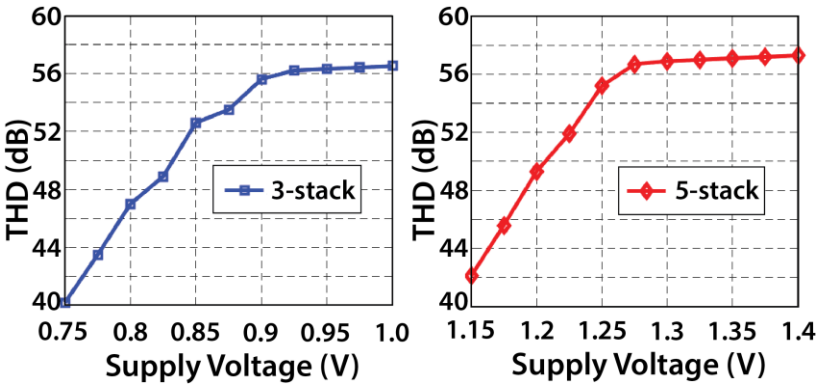


(c)

Figure 2.16 Measured ECG from a human subject recorded from *N*=5 amplifier.

The fabricated chip has also been used perform ECG recordings from a human subject using a standard three electrode set-up with the third electrode grounded. A measured ECG

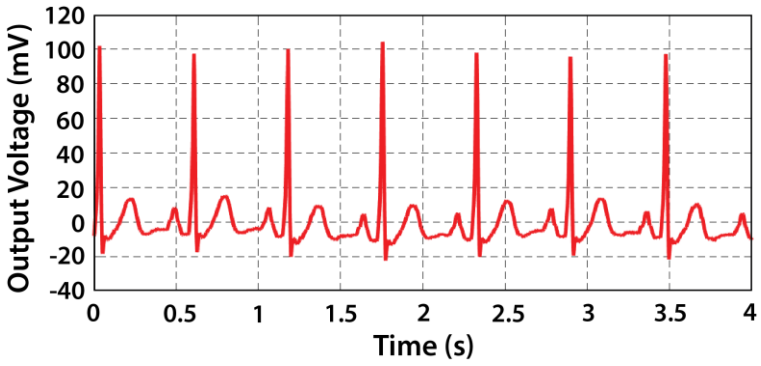


Figure 2.17 Linearity of (a) single tone and (b) two tones. (c) Linearity vs. supply voltage.

waveform in Lead II electrode configuration is shown in Figure 2.17.

The performance of the prototype amplifiers is summarized and compared with existing state-of-the-art work in Table 2.3. It should be noted that the PEF improvement is not as drastic compared to prior works as expected from theory presented in Section 2.2. This is because the prior state-of-the-art PEF was reported from amplifiers with power consumption in μW range wherein the reported power of peripheral circuits was minimal (*e.g.*, a few nW is reported for biasing circuits in [34]). A substantial power is consumed in this work to ensure robust operation and meet application needs mentioned earlier. Nevertheless, the measured NEF and PEF compared to prior works from the 5-stack version are the best reported, to the author's knowledge, and significantly better ~3× compared to nW level ultra-low power amplifiers [16], [17].

2.7 Conclusion

A novel technique for improving the power efficiency of a two-stage op-amp with chopping was presented. The benefits were demonstrated for an amplifier intended for an

Table 2.3

Performance Summary and Comparison of Low Power Amplifiers

	JSSC '17 [49]	JSSC '16 [16]	JSSC '15 [17]	JSSC '18 [37]	ISSCC '13 [48]	JSSC '17 [18]	This work JSSC'20 [13]	
							3-stack	5-stack
Application	ECG/ EEG	ECG	ECG	–	EEG	EEG	ECG	
Technology	180 nm	65 nm	65 nm	180 nm	180 nm	40 nm	180 nm	
Supply (V)	0.2 / 0.8	0.6	0.6	1	0.45	1.2	0.95	1.35
Area (mm^2)	1	0.2	0.6	0.29	0.25	0.071	0.18	0.24
Power (nW)	790	1	16.8	250	730	2,000	13.2	18.7
Current (nA)	987	1.67	28	250	1,622	1,666	13.9	
Gain (dB)	58	32	51–96	25	52	26	36	
BW (Hz)	670	370	250	10,000	10,000	5,000	240	
CMRR (dB)	85	60	80	84	73	-	> 95	
PSRR (dB)	74	63	67	76	80	-	> 68	
THD (%)	0.3 (75% out)	-	2.8	-	0.53 (90% out)	0.02 (40 mV_p in)	0.19 (75% out)	0.16 (75% out)
Peak Ripple/V_{DD}	-	-	-	-	-	-100 dB	-81 dB	-85 dB
Input-Ref. Noise (nV/√Hz)	36	1,400	253	43	29	40	194	158
NEF	2.1	2.1	2.64	1.07	1.57	4.9	1.08	**0.86**
PEF	1.6 / 1.8*	2.64	4.1	1.14	1.12	28	1.12	**0.99**
Blocks/features under comp.	LNA, chop PGA, AA-filt	LNA	LNA, chop DSL	LNA	LNA, VGA	LNA, Chop, Imp, Ripple-rej.	LNA, chopping, DSL, Imp-boost, Ripple-rej.	

* With DC-DC converter overhead

implantable ECG application. The proposed OTA-stacking technique could also be extended for other applications such as local field potential (LPF) or spike recording AFEs [47], [55], Wheatstone bridge sensors [58] and continuous-time ADCs such as [59] that require a capacitively-coupled chopper-stabilized input stage. The proposed G_m-boosting resulting in lower noise also assists chopping owing to the associated higher bandwidth to process the upmodulated signals and owing to the high pass filtering to minimize chopper ripple. The self-biased feedback mechanism helps maintain a good CMR. Compared to prior works, a two-stage implementation is feasible and output summations are realized passively without any power overhead. With the

stacking of five OTAs, the best reported NEF of 0.86 and PEF of 0.99 are achieved from an amplifier consuming only 13.9 nA current.

Chapter 2, in full, is a reprint of the material published in the *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 414-425, Feb. 2020, “Somok Mondal and Drew A. Hall, A 13.9-nA ECG Amplifier Achieving 0.86/0.99 NEF/PEF Using AC-Coupled OTA-Stacking". The dissertation author was the primary investigator and author of this paper.

Chapter 3.

An Audio-band Continuous-time Delta-Sigma ADC with OTA-Stacking

3.1 Introduction

Audio applications require analog to digital converters (ADCs) with high dynamic range (>100 dB) and resolution (>16 bits) while also being power-efficient. Continuous-time delta sigma modulators (CTΔΣMs) have gained widespread popularity for such ADC implementations owing to their inherent anti-aliasing, resistive inputs, and relaxed settling requirements as compared to their discrete-time counterpart. Linearity, speed, and noise are often the main design considerations for these ADCs. Several techniques [60]–[64] are already well-established to meet the audio application linearity (>100 dB SFDR or spur-free dynamic range) in a power-efficient manner. Speed considerations are usually not critical due to the targeted low bandwidth of audio signals. Noise considerations, however, impose a fundamental limitation to the ADC performance. As such, the noise-efficiency of the first integrator's input operational transconductance amplifier (OTA) has a substantial influence on the overall ADC's power and figure of merit (FoM).

Minimizing the power consumption of the first stage while meeting the targeted noise spec has always been an important design aspect for CTΔΣMs. The use of finite impulse response (FIR)

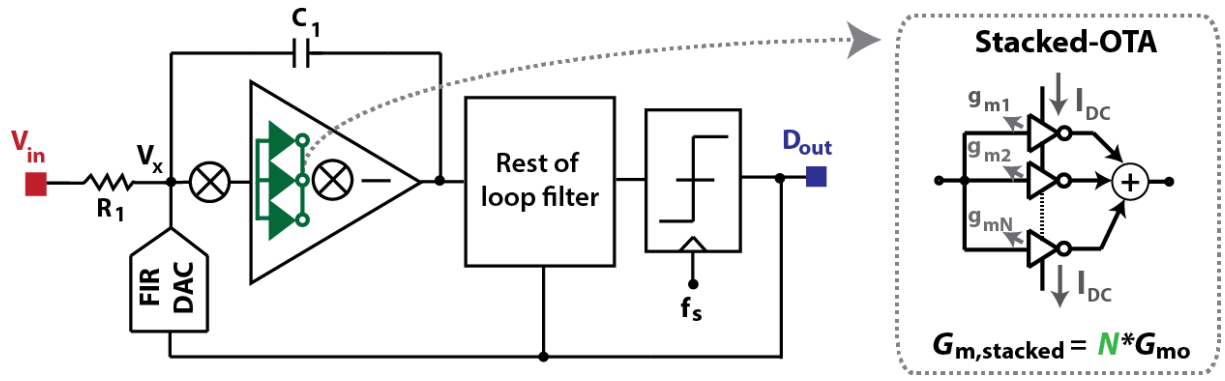


Figure 3.1 Overview of OTA-stacking in a chopped CTDSM.

feedback DACs [65] enables chopping at lower frequencies, which removes the OTA's 1/*f* noise, but cannot reduce the thermal noise. Inserting a capacitively coupled gain buffer upfront in [59] diminishes the contribution of the first integrator's resistor noise. However, the easy-to-drive resistive input property of CTΔΣM is lost and the buffer requires a wide bandwidth to not impact the loop filter, limiting the applicability to low speed sensors. With negative resistance assistance [63], the OTA's noise is reduced at the expense of increased resistive noise. Furthermore, the negative resistance is sensitive to process, voltage, and temperature (PVT) variations as it depends on a cross-coupled pair's open-loop transconductance.

OTA-stacking is a recently reported technique to fundamentally improve upon the noise-power tradeoff in a continuous-time chopper amplifier [13]. Contrary to amplifier applications, wherein the increase in supply voltage to accommodate for stacking results in only marginal improvements in amplifier's power-efficiency, an oversampled data-converter sees direct benefits from both an increase in supply voltage and stacking, with the FoM improvements discussed in detail later. This forms the underlying motivation behind employing the OTA-stacking technique in a CTΔΣM in this work.

An overview of the ADC implementation with OTA-stacking enabling power reductions in the input stage is shown in Figure 3.1. It may be noted that a discrete-time ADC with a switched-capacitor stacking amplifier was presented in [37]. However, this implementation required split feedback networks limiting the implementation to a single stage and hence a higher supply voltage (5.4 V) was required. High gain from a single stage is also challenging, requires large channel length, and hence can likely support only slow-speed applications. Several architectural innovations have also been proposed in recent years to improve the energy-efficiency. The Zoom ADC architecture [66] utilizes a low power SAR-based ADC for coarse quantization and has gained popularity. The input OTA for the fine quantization is the dominant contributor to the overall ADC power. Other implementations have explored voltage-controlled oscillator (VCO)-based [67], cascaded [68], and incremental [69] topologies. In these, the input OTA stage remains the power-hungry component. The proposed OTA-stacking can potentially be integrated with all such oversampling ADC architectures to further improve the efficiency.

To incorporate the OTA-stacking technique into the ADC and meet the audio application resolution/linearity specs, chopping, FIR DACs, and a 4-stage feedforward compensated amplifier are used. Stacking 3 OTAs theoretically leads to a 4.8 dB improvement in the FoM, assuming the noise-limited input OTA is the sole power consuming block. Measurements from two prototype 1- and 3-stack ADCs exhibiting a 2.1-dB improvement in the Schreier FoM establishes the efficacy of the proposed technique.

The rest of this chapter is organized as follows: Section 3.2 reviews OTA-stacking and motivates the work. Section 3.3 describes the challenges and the key novelties of the proposed CTDSM. Implementation details at the architectural level and the circuit level are provided in

Sections 3.4 and 3.5, respectively. Measurement results are presented in Sections 3.6 and finally conclusions are drawn in Section 3.7.

3.2 Noise-Efficiency Enhancement: OTA-Stacking

This section briefly reviews the existing OTA-stacking concept [13] and discusses its potential benefits for an oversampled ADC to set the stage for the proposed work.

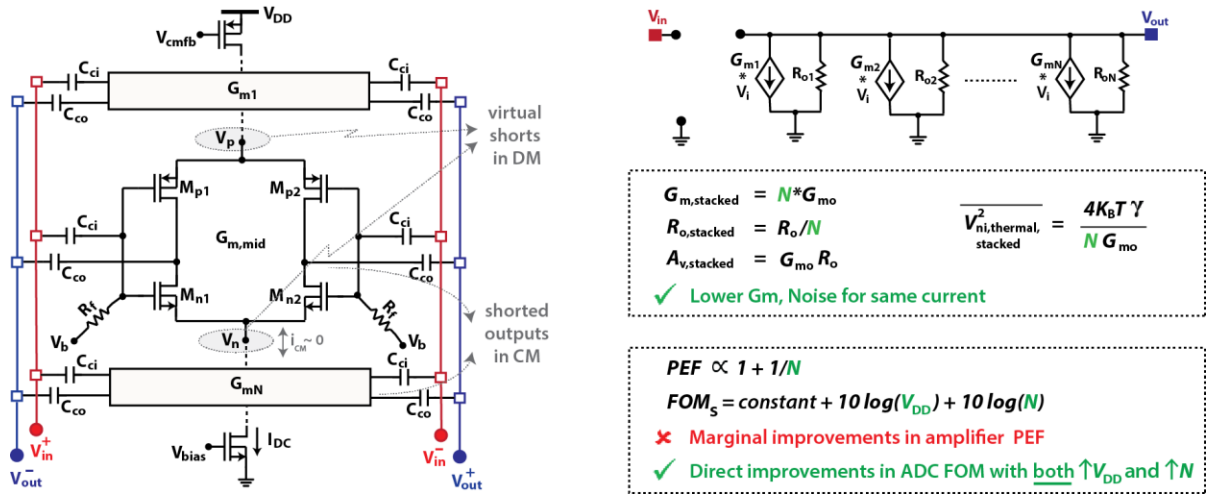
3.2.1 OTA-Stacking and Tail-less Amplifiers

The OTA-stacking concept is illustrated in Figure 3.2. In the small-signal differential-mode, adjacent inverter-based OTAs are decoupled since the source nodes are virtual shorts while all inputs and outputs are ac-shorts. This results in a G_m-boosting and a proportionate input-referred noise reduction while reusing the same current. For the common-mode, a self-feedback mechanism with the outputs shorted together maintains high common-mode rejection (CMR).

While the noise is lowered for the same current, this comes at the expense of a higher supply voltage requirement. The improvements in the power efficiency factor (PEF), which captures the amplifier's input-referred noise vs. the power tradeoff, is related to the tail sources [13] and the stacking factor N as

$$PEF \propto V_{\text{inv}} + \frac{V_{\text{tail}}}{N}. \tag{3.1}$$

where V_{inv} and V_{tail} are the voltage headrooms allotted to each inverter and the combination of the tail current sources. This indicates a drawback of OTA-stacking for amplifiers. The PEF improvement is, in practice, only marginal and saturates with an increase in stacking or N.



(a) **(b)**

Figure 3.2 OTA stacking concept with (a) a simplified single-ended OTA and (b) simplified equivalent small-signal model showing the benefits of stacking.

It can be seen from (3.1) that setting $V_{\text{tail}} = 0$ or removing the tail source altogether results in the minimum possible PEF. In classical OTA implementations, the tail source is typically needed for common-mode rejection (CMR). A tail-less operation, as discussed in detail later, is also feasible with a combination of chopping and filtering aiding the CMR.

3.2.2 Benefits of OTA-Stacking in CTΔΣM

With tail-less operation, (3.1) indicates a minimum PEF can be realized by tail-less, low supply operation alone and without the need for any stacking. However, even ignoring other considerations such linearity, the need for higher chopping frequency for CMR, etc., there are benefits of OTA-stacking along with tail-less operation for an oversampled ADC. This can be understood from the FoM limit as derived in *Appendix 1* that can be expressed as

$$FoM_S \cong 191 + 10\log(\boldsymbol{V_{DD}}) + 10\log(\boldsymbol{N}). \quad (3.2)$$

The above indicates that the ADC FoM benefits from both an increase in supply voltage, V_{DD}, as well as an increase in the stacking factor, N. Therefore, contrary to the marginal improvements in the amplifier PEF, the OTA-stacking technique requiring a higher supply, leads to straightforward improvements the ADC energy efficiency. While this is clearer upon following the analysis in *Appendix 1,* briefly this difference is a result of the PEF capturing tradeoff between input-referred noise and power, while the ADC FoM capturing the tradeoff between SNDR and power.

It may appear that the FoM would keep improving with an increase in V_{DD} alone. However, in a practical ADC, there is power contribution from the latter analog blocks, digital blocks, such as the comparator, and importantly the feedback DAC whose power contribution increases with V_{DD}, thereby eventually limiting the benefits of using a higher supply. In this work, based on the target specs for audio applications, stacking three OTAs with a 1 V supply represented a reasonable design choice.

3.3 CTΔΣM with OTA-Stacking: Challenges and Solutions

Having understood the benefits of OTA-stacking for an oversampled ADC, the considerations to use it as the input stage in a CTΔΣM are discussed in this section. Incorporating the OTA-stacking technique in CTΔΣMs requires addressing the several key challenges which are related to the ac-coupling required for stacking. These key challenges are as follows: 1) The proposed OTA with ac-coupled inputs, blocks dc whereas the op-amp for an integrator application needs a very high dc-gain; 2) A known problem in CTDSMs, especially with single bit feedback, is the difficulty in transient settling with the feedback being a rail-to-rail square wave from a non-

return-to-zero (NRZ) digital-to-analog converter (DAC), which degrades the ADC linearity. The transient settling response due to DAC steps at the modulator's summing node is further worsened with large ac-coupling capacitors. 3) Finally, and most importantly, the ac-coupled OTA acts as a band-pass filter which causes unwanted notches in the frequency response that changes the loop-filter response and can thereby degrade the noise-transfer function (NTF) and, in the worst case, can even compromise the loop-filter's stability.

This first issue of no dc gain is readily addressed by chopping. The low frequency signals are upmodulated, processed by the mid-band gain of the stacked-OTA, and downmodulated back, thereby offering good dc gain. The second issue can be addressed using a conventional multi-bit feedback DAC. An alternate is to use an FIR DAC with multi-level feedback, which also facilitates lower signal swings for the first integrator and improves linearity without the added complexity and overhead of the otherwise needed mismatch shaping techniques and comparators [70]. The FIR feedback DAC has been adopted here.

Figure 3.3 elaborates on the aforementioned third challenge and illustrates how to addresses it. The band-pass OTA's signal response to chopped inputs is shown in Figure 3.3(a). For low frequency/baseband inputs, the entire signal content is upmodulated and processed by the constant mid-band gain of the OTA. The signal fidelity upon demodulation henceforth remains consistent. However, for higher frequency signal around the chopping frequency f_{chop}, a significant part of the signal gets downmodulated to dc and filtered out by the band-pass OTA, as evident from Figure 3.3(a). Upon demodulation this implies that signals with frequency content around f_{chop} are attenuated or exhibit a low gain. The resulting frequency response hence exhibits notches at multiples of f_{chop}, as shown in Figure 3.3(b). While this is not an issue for chopper

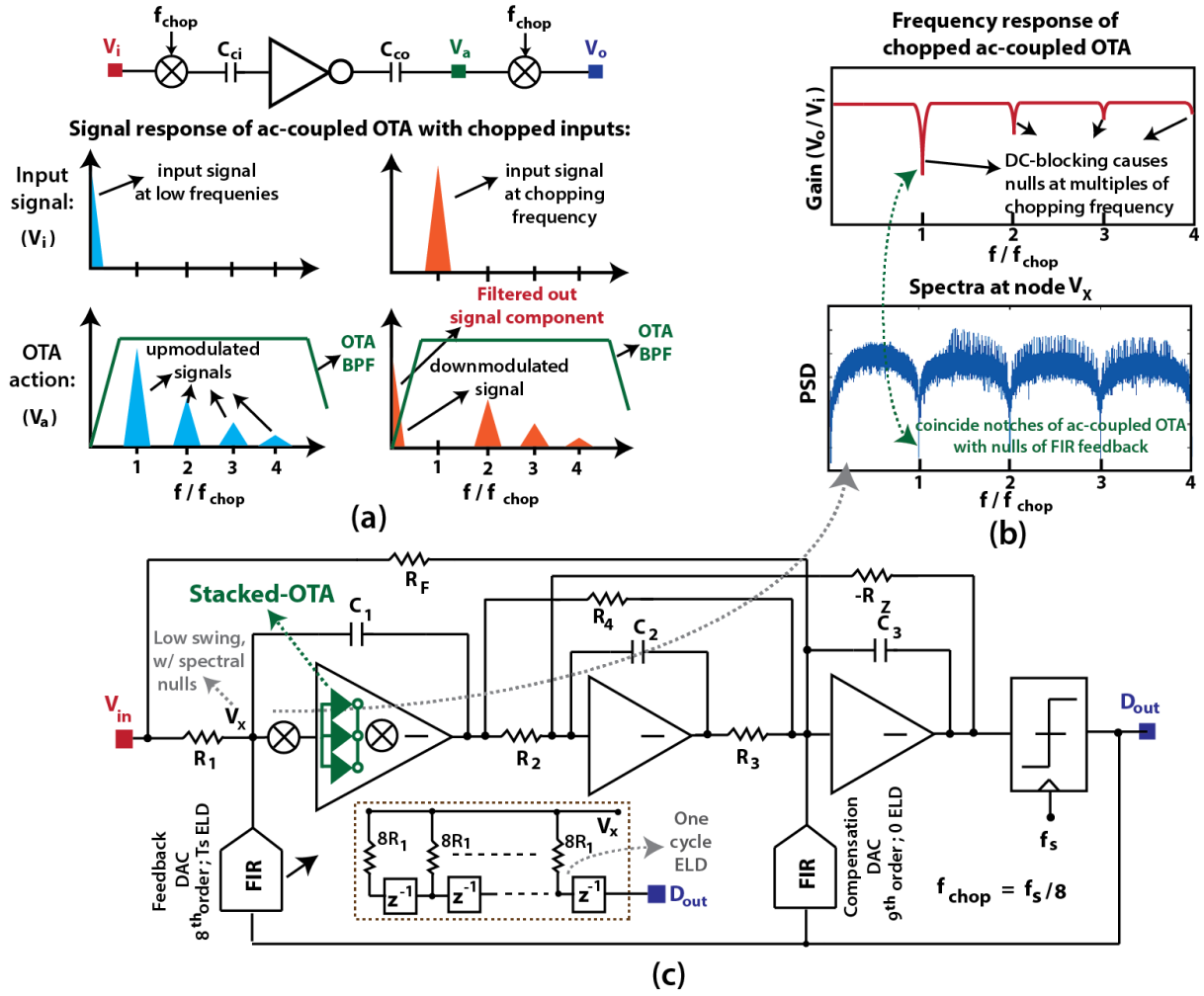


Figure 3.3 OTA-stacking for a CTDSM ADC (a) key challenge and proposed solution with FIR feedback. (b) DSM architecture with CIFF-B topology.

amplifiers in sensor front-ends that are meant to process signals at frequencies much lower than f_{chop}, it is highly problematic in a CTΔΣM that must process quantization noise at higher frequencies as well.

A straightforward solution is to apply the stacking technique with a band-pass OTA into a band-pass delta-sigma modulator. However, audio applications strictly require a low pass ADC.

Another option is to chop at the sampling frequency. However, this is a power inefficient solution limiting the speed. Interestingly, the FIR DAC also offers an additional property. The FIR feedback results in spectral nulls at multiples of f_s/N_{FIR}, where N is the FIR filter order. As shown in Figure 3.3(b), with $N_{FIR} = 8$, there are nulls at multiples of $f_s/8$. This property was utilized in [1] to mitigate performance degradation due to aliasing issues from chopping artifacts by selecting $f_{chop} = f_s/2N_{FIR}$. In this work, $f_{chop} = f_s/N_{FIR}$ is used to coincide the notches in the frequency response of the proposed OTA with the nulls of the FIR feedback, as shown in Figure 3.3(b). Henceforth, the OTA doesn't need to process signal content at multiples f_{chop} making the use of an ac-coupled band-pass OTA in a CTΔΣM viable and extends the utility of the recently popularized FIR feedback technique.

3.4 Circuit Implementation Details

The details of the key circuit blocks and the associated design considerations are discussed next.

3.4.1 Proposed ADC: Architectural Overview

The architectural implementation of the 3rd -order, 1-bit audio-band CTΔΣM is shown in Figure 3.3(c). A cascade of integrators in feedforward and feedback (CIFF-B) topology [2] with optimized zeros is used to realize the loop filter. The continuous-time integrators are implemented using opamp-based active *RC* structures. Non-return-to-zero (NRZ) resistive FIR DACs are used as feedback elements. The ADC is clocked at f_s = 6.4 MHz with an oversampling ratio (OSR) of 160 for an audio signal bandwidth of 20 kHz. The main FIR feedback is 8th-order and hence f_{chop} is (6.4/8) MHz or 800 kHz.

The input resistor R_1, chosen to be 13 kΩ, is maximized for high closed-loop linearity from the first integrator and is the dominant noise source. The ADC is designed such that 93% of the circuit noise is contributed by the input and the DAC resistors, 4.5% by the first integrator's input stage, and 2.5% by the latter stages and other sources. The input stage is implemented using OTA-stacking integrated with tail-less operation, as described next.

3.4.2 Tail-less Amplifier Operation

As established earlier in Section 3.2, removing the tail sources and minimizing the supply results in a best possible amplifier PEF. However, maximizing the supply and stacking leads to improvements in the ADC FoM. Henceforth, tail-less operation, which relaxes headroom requirements and facilitates stacking a larger number of OTAs for a given supply, is adopted here. In a conventional inverter-based amplifier, two tail sources are typically essential for CMR. However, a combination of chopping and filtering can alternatively be used to ensure good CMR, even with tail-less operation [49]. This CMR functionality can be understood from Figure 3.4. Differential-mode (DM) signals, when chopped, are upmodulated, processed by the mid-band gain of the band-pass OTA, and downmodulated back to baseband. However, when a common-mode (CM) signal is chopped, it is unaffected because chopping is essentially a flip of input polarity and both inputs are the same for a CM signal. Thus, as shown in Figure 3.4, the CM interferer stays at low frequency and is suppressed by the high-pass filtering from the ac-coupling at the OTA's input devices. DM components originating from this suppressed CM due to mismatch are also proportionately lower. These are further translated to higher frequencies after down-chopping and do not affect the signals of interest.

A critical drawback, as evident from the description above, is that the CMR is inevitably compromised being only possible for low frequencies and requires the chopping frequency to be

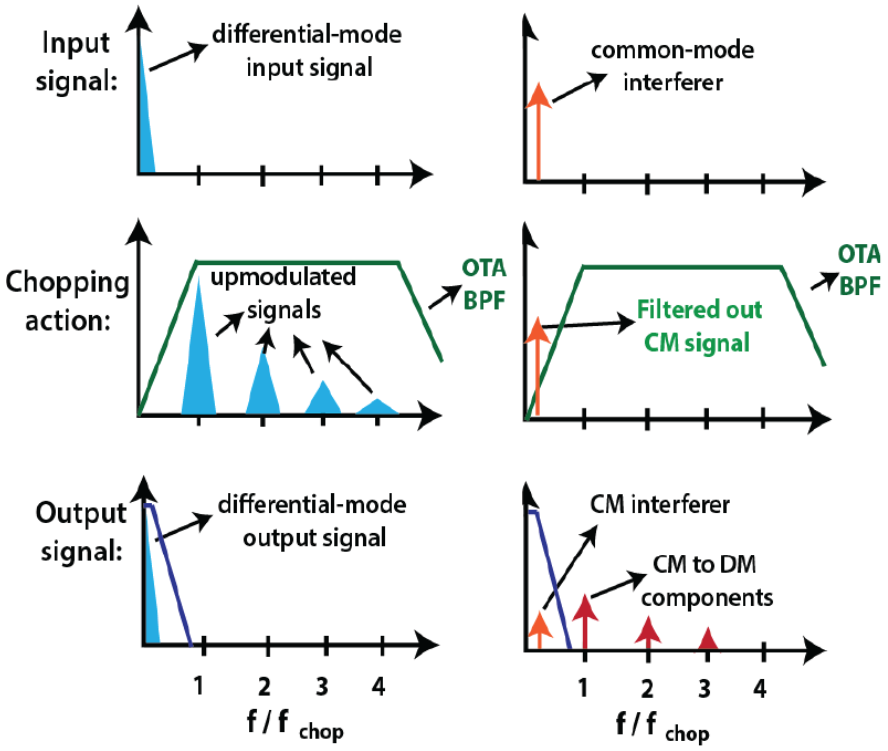


Figure 3.4 Tail-less OTA functionality: common-mode rejection with chopping and filtering.

much higher than the desired CMR frequency range. This may not always be feasible for low power sensor applications, such as the ones intended in [49], [71]. However, for high-performance precision sensing associated with low noise and high power, such as audio conversion, chopping at higher frequencies can be easily accommodated and is often required. In this work, with f_{chop} of 800 kHz and the high-pass corner of 30 kHz for the ac-coupled input OTA, low frequency CM signals (*e.g.,* power line interferers at 60 Hz) are attenuated by ~50 dB. A large attenuation is essential since allowable excess voltage headroom for the stacked stage is minimal.

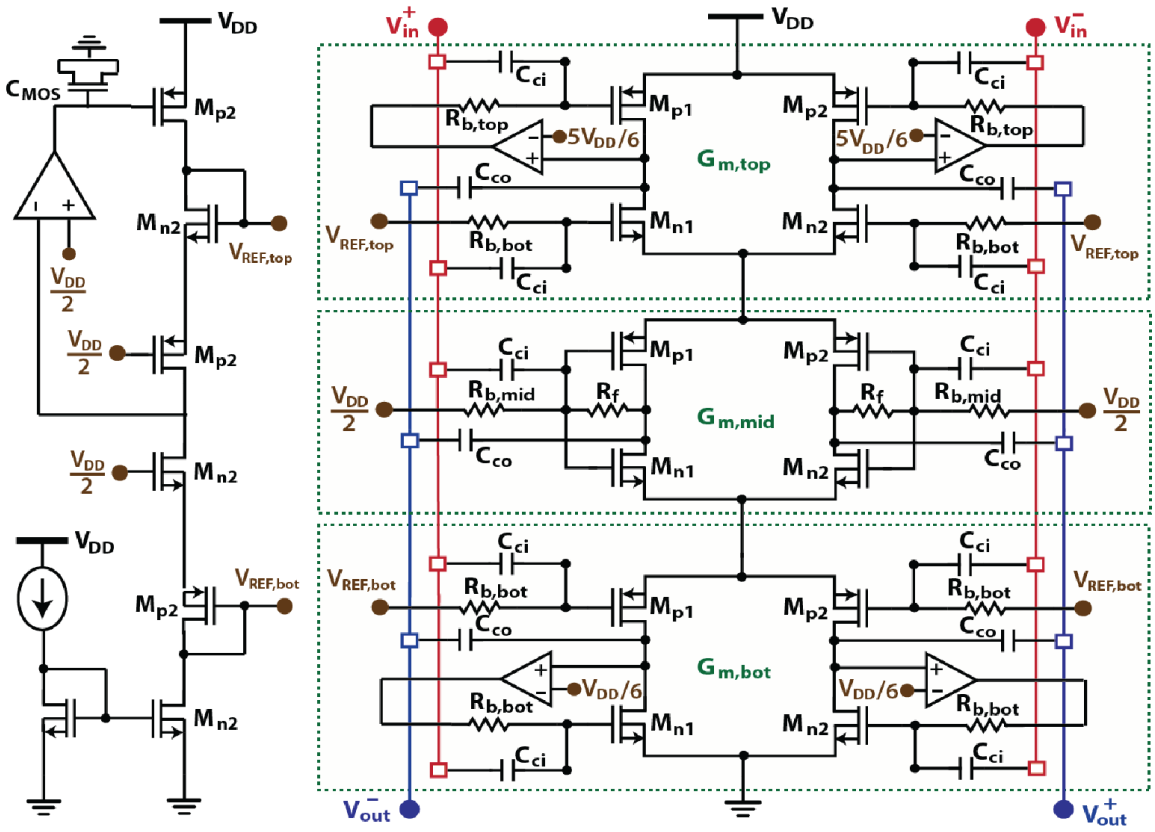


Figure 3.5 Noise-efficient tail-less input stage implementation with stack of 3x OTAs.

3.4.3 Stacked-OTA Implementation

The proposed implementation of the fully-differential, stacked-OTA is shown in Figure 3.5. Three inverter-based OTAs are stacked vertically and the tail current sources are removed. The inputs and the outputs of all the OTAs are ac-coupled together, respectively, for the desired G_{m}-boosting. The central inverter's inputs and outputs are biased explicitly to $V_{\mathrm{DD}}/2$. The intermediate transistors are biased to the references $V_{\mathrm{REF,top/bot}}$ generated by a replica network which also sets the bias current. Such biasing scheme is also conventionally used in folded cascode

amplifiers with complementary inputs, except that there is an inverter in-between that is explicitly biased. Good CMR from all the intermediate diff-pairs is maintained due to the self-feedback mechanism described in [13]. Individual feedback loops for the top- and bottom-most transistors bias the respective inverters and guarantee CMR despite the lack of high impedance source degeneration from the tail sources [71]. These local feedback loops are readily stable owing to the low bandwidths and have phase margins ~ 90°. All biasing resistors are implemented with <5 MΩ poly-resistors rather than GΩ pseudo-resistors for better linearity, well-defined high-pass cutoff frequencies, and avoid the otherwise large voltage drops due to gate leakage current. MIM capacitors are used to implement all the coupling devices. The local feedback loop of the replica network is stabilized by load compensation via a large 25 pF MOS capacitor, C_{MOS}. The non-linearity of the MOS capacitor is not an issue since it is connected to a dc node. The replica network is sized such that it consumes only $1/16^{\mathrm{th}}$ of the stacked-OTA's current. The auxiliary amplifiers for CMR contribute less than 2% overhead to the stacked-OTA's power consumption. The NMOS devices in each stack are in a deep-N well and has its body-source tied together to avoid body-effect and maintain a vertical symmetry for better linearity.

3.4.4 First Integrator Implementation

In traditional CTΔΣMs, the first integrator op-amp is a two-stage Miller compensated amplifier with the first stage being cascoded to meet the high gain and bandwidth requirements. However, cascoding is not possible in the first stage when implemented as a stacked OTA. Additionally, there are restrictions on using Miller compensation to avoid attenuation from a capacitive divider at the ac-coupled output and on the limited swing allowable across the stacked stages. In view of these restrictions, a four-stage feedforward compensated topology is used and is shown in Figure 3.6 (a). An explicit resistor R_{b} biases the second stage and also contributes to

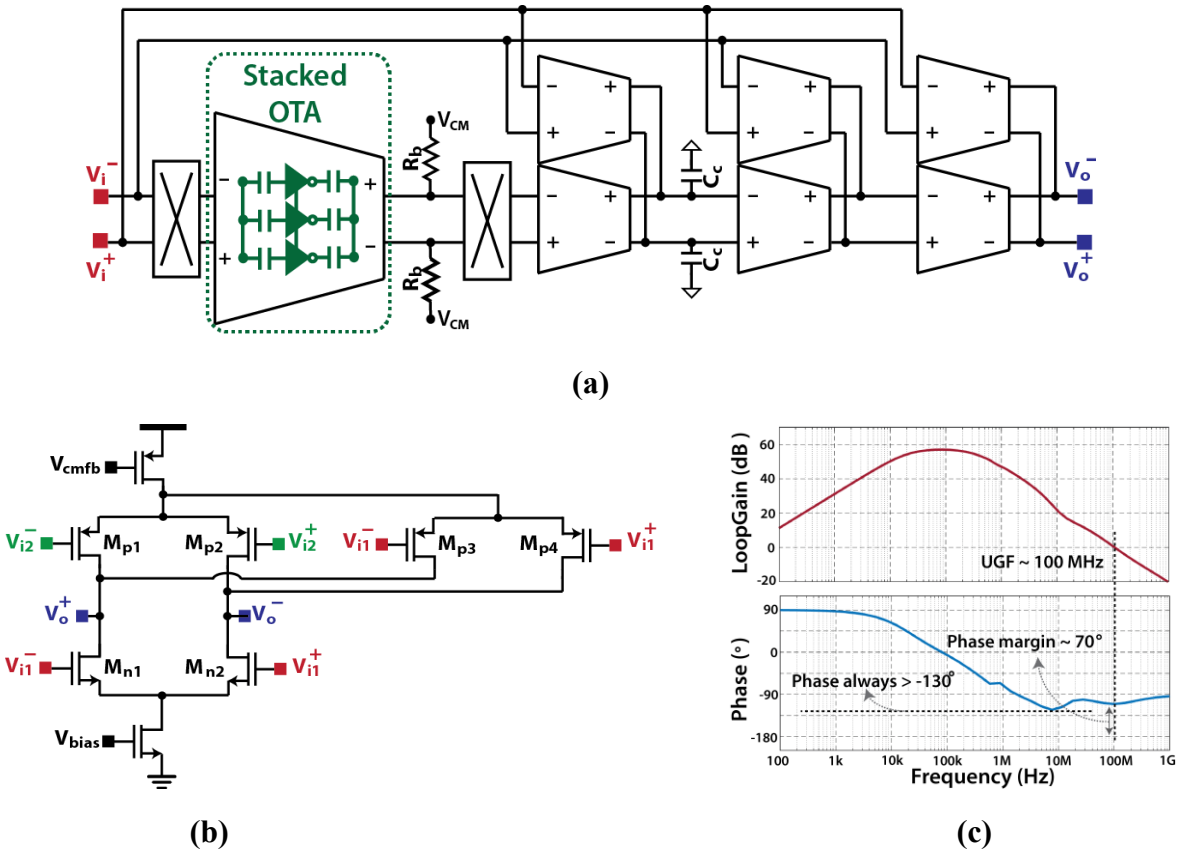


Figure 3.6 First integrator (a) 4-stage opamp implementation, (b) feedforward OTA, and (c) simulated stability.

the high-pass corner of the band-pass first stage. The dominant contributor the high-pass corner is, however, the feedforward resistor R_f for the central inverter in Figure 3.5 and the associated input coupling capacitors. Each of the latter stages is implemented as dual-tail inverter-based OTAs partially sharing the same current, as shown in Figure 3.6(b).

The stability with feedforward compensation is dependent upon the relative pole-zero cancellations. For a 4-stage implementation, the four-pole system is compensated with appropriate placements of three zeros. A known issue with this compensation is that if the cancelling zeros are much higher frequency than the poles, there can multiple phase crossover frequencies with loop-gain greater than unity, such as in [72]. From control theory [73], the stability can no longer be inferred from a Bode diagram and requires complex assessment using Nyquist plots. In this work, an explicit capacitor C_c between the second and third stage assists the compensation. Given that a feedforward zero location depends on the pole of the prior stage [74], C_c provides an extra degree of freedom to control the relative pole-zero positions of the system in a way that multiple gain crossover frequencies are avoided and stability evaluation can be made using standard Bode plot techniques. The simulated stability of the first integrator from a periodic steady-state (pstb) analysis is shown in Figure 3.6(c). The simulated phase margin is > 70° while the dc gain is > 90 dB across all process corners.

The intermediate 2nd and 3rd stages do not affect the unity-gain frequency (UGF) of the 4-stage op-amp since the poles are cancelled at frequencies lower than the UGF. Therefore, these gain stages can be implemented with very low power overhead (< 5%). However, the 4th stage needs to drive the feedback capacitor loading the output and accounts for ~25% of the op-amp power. The feedforward compensation is a good choice to push the power burden to the input stage contrary to traditional Miller compensation that needs a higher second stage g_m or load compensation, which can also push the power burden to the first stage but at the expense of much lowered UGF.

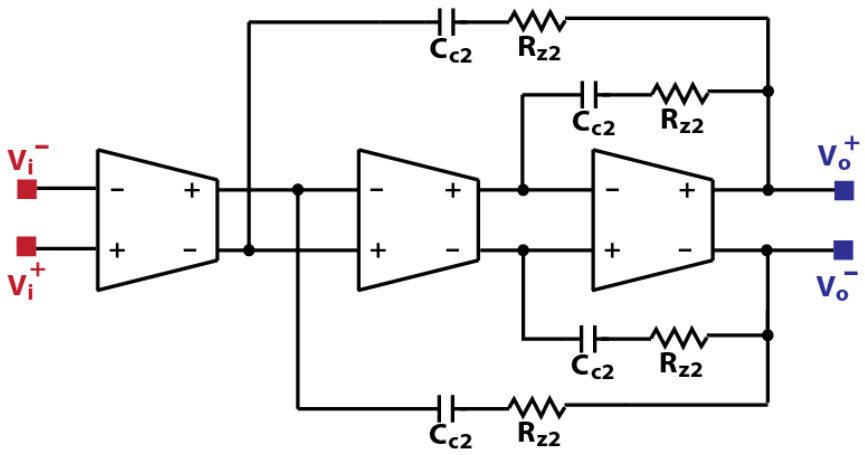


Figure 3.7 Three stage nested Miller op-amps for 2nd and 3rd integrators.

3.4.5 FIR Feedback

The proposed ADC in Figure 3.5 uses two DACs. One is used as the main feedback DAC and the other is used as a compensation DAC to restore the otherwise changed NTF due to the delayed FIR feedback [61]. A semi-digital 9-tap FIR structure realizes the DACs. Mismatch between the DAC elements do not degrade linearity and only affects the filter's frequency response while providing a multi-level output [73]. For the main DAC, the first tap is absent and the rest are equally weighted. This allows for a full clock cycle excess loop delay (ELD) to lower the comparator power consumption. The compensation DAC has a finite valued first tap and no associated ELD. It was found during the design phase for simulations that, with the low power comparator implemented here, providing no ELD to the feedback DACs resulted in SNDR degradation due to higher third harmonic distortion. This is likely attributed to signal dependent delay from the comparator. ELD to the main DAC alone was found sufficient to mitigate this SNDR degradation and is the motivation behind the FIR DAC implementation described above.

However, this asymmetric 8^{th}- and 9^{th}-order FIR feedback is also suspected to cause some performance degradation discussed in the measurements section later.

The 9-tap main DAC with first tap absent and the rest equally weighted provides an 8^{th}-order moving average filtered feedback with spectral nulls at multiples of 800 kHz. The -3 dB width of the FIR feedback nulls are >250 kHz at the summing node of the CTΔΣM, as determined by simulations. The -3 dB high-pass corner frequency of the stacked-OTA is 30 kHz implying that the frequency notch width is <60 kHz when the OTA is chopped. Thus, the feedback nulls of 250 kHz are sufficiently wider. The selection of $N_{FIR} = 8$ has been made considering tradeoffs related to f_{chop} as a lower chopping frequency eases the op-amp design, the signal swings reduce with a higher N_{FIR}, and importantly the null width as a higher N_{FIR} lowers the null width.

3.4.6 Auxiliary Circuits and Design Summaryz

The ADC is designed such that 93% of the circuit noise is contributed by the input and the DAC resistors, 4.5% by the stacked-OTA in the first integrator, and 2.5% by the latter stages and other sources. The other integrators are realized with conventional nested Miller compensated 3-stage OTAs, as shown in Figure 3.7. The dynamic comparator is a conventional Strong-Arm latch. Two ADCs are implemented on the chip, 1-stack and 3-stack versions. The 1-stack version is analogous to the 3-stack version albeit, the input stage is a conventional dual-tail inverter OTA with three times the current, the same noise floor, and without any ac-coupling. The power breakdown of both the ADC designs are presented in Figure 3.8. The synthesis of loop-filter coefficients with the FIR DACs is described in *Appendix 2*.

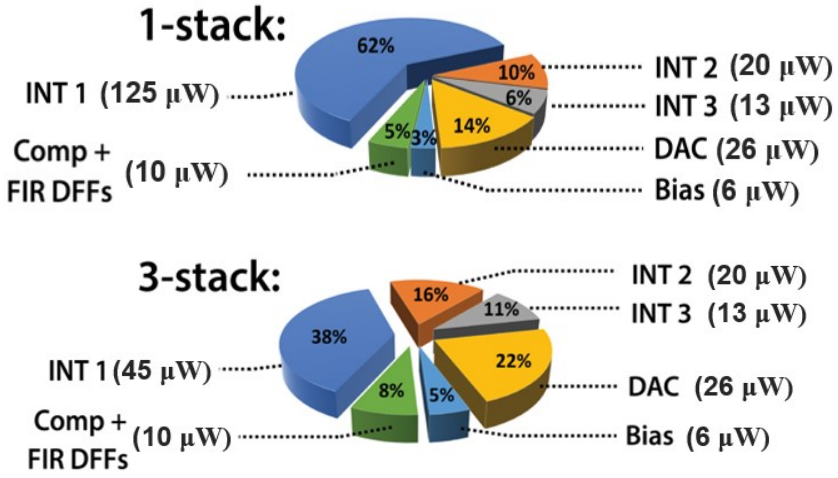


Figure 3.8 Power breakdown for the two ADCs.

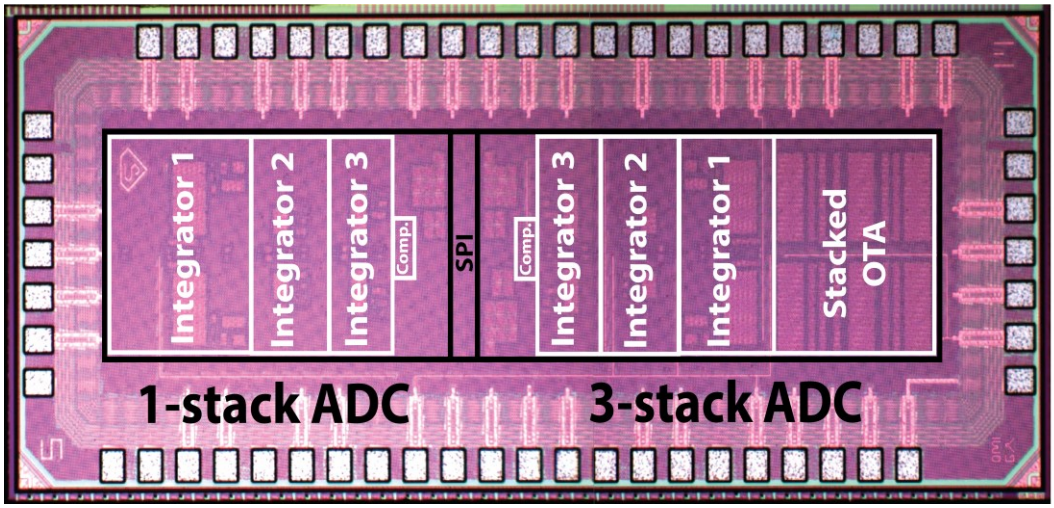


Figure 3.9 Annotated chip micrograph.

3.5 Measurement Results

Measurements from the two prototype ADCs fabricated in a 65 nm CMOS technology are presented in this section. Both 1- and 3-stack ADCs are operated from a 1 V supply and occupy

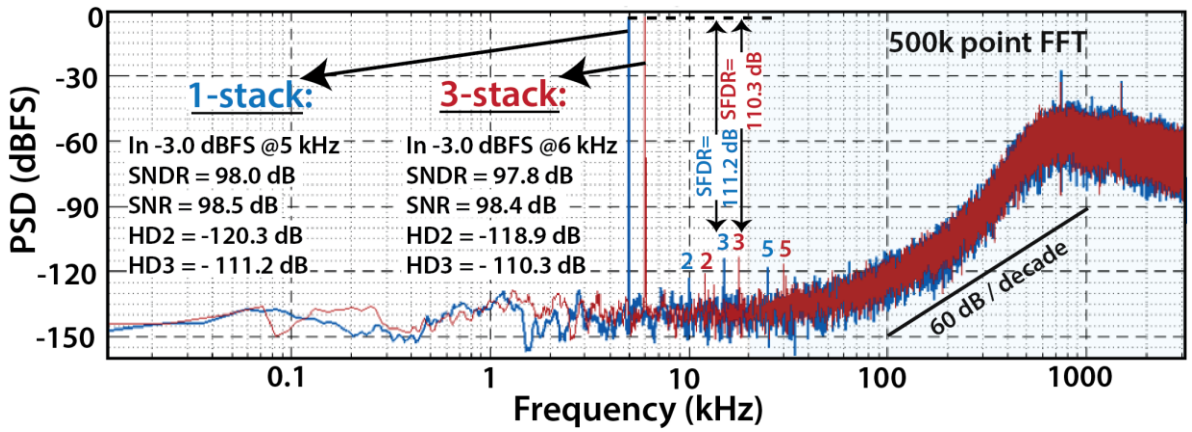
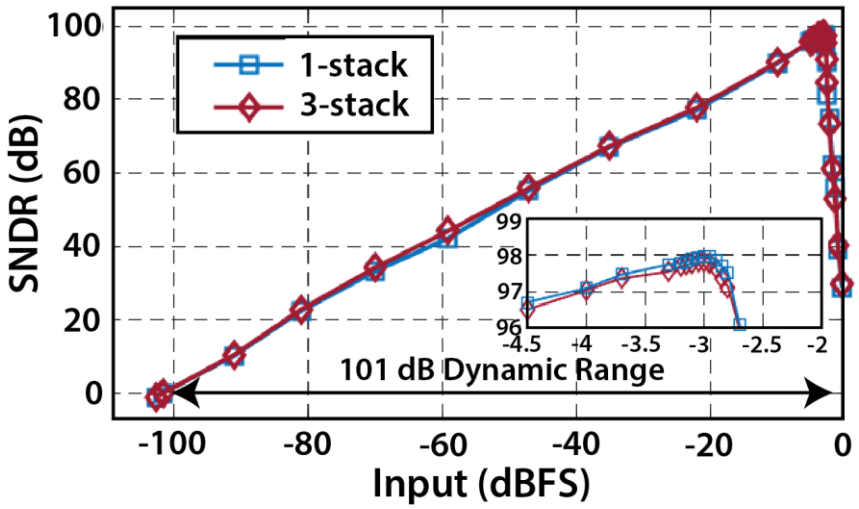


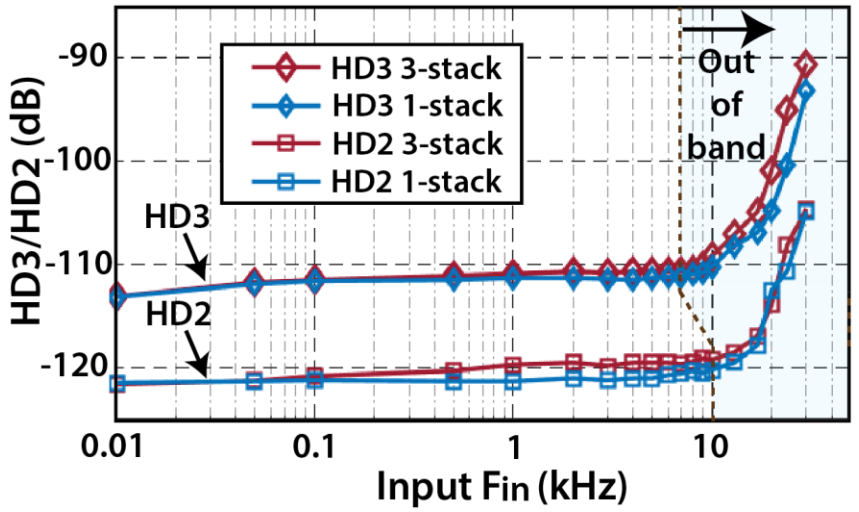
Figure 3.10 Measured ADC spectra.

0.25 and 0.39 mm^2, respectively. The annotated chip micrograph is shown in Figure 3.9. Both the ADC versions are designed for the same performance specs. These are determined by their input-referred noises, which is the same for both versions. As such, the measured power drawn from the 1-stack ADC is 202 µW power while that from the 3-stack ADC is 121 µW.

The measured power spectral density plot for the two ADC versions from the same chip is shown in Figure 3.10 corresponding to a 5 kHz, -3 dBFS input for the 1-stack and a 6 kHz, -3 dBFS input for the 3-stack. The corresponding signal to noise and distortion ratio (SNDR) over a 20 kHz bandwidth is measured to be 98.0 and 97.8 dB for the 1- and the 3-stack versions, respectively. Both ADCs exhibit excellent linearity with an SFDR > 110 dB. It may be noted that the spectral plot exhibits a deterministic tone at a frequency of $f_s/8.5$ and also NTF peaking around



(a)



(b)

Figure 3.11 Measured ADC (a) dynamic range (b) linearity vs. input frequency.

it. This could be the result of asymmetric FIR feedback with an 8th-order main DAC and a 9th-order compensation DAC. The ADC's measured peak SNDR is less than expected based on

simulations and could be attributed to the aforementioned non-ideality observed in measurements.

A plot of the measured SNDR versus the input signal amplitude at 6 kHz is shown in Figure 3.11(a). The dynamic range (DR) is measured to be 101.3 and 101.2 for the 1- and 3-stack ADCs, respectively. Figure 3.11(b) shows the linearity performance of the ADCs with harmonic distortion plotted versus the input frequency. The third harmonic (HD3) and the second harmonic (HD2) distortion components are always below -110 dB and -120 dB, respectively.

Overall, the ADC performance metrics for both the versions remain consistent. This signifies the challenges with integrating OTA-stacking for a CTΔΣM have been well addressed using the techniques described in Sections 3.3 and 3.4. Specifically, the issue of unwanted notches in the frequency response of an ac-coupled OTA has been mitigated using an FIR DAC and good linearity is ensured using the four-stage feedforward compensated op-amp.

Table 3.1 presents a performance summary of this work and compares it against other recently published audio bandwidth ADCs. The $FoM_{SNDR/DR}$ are 177.9/181.3 dB for the 1-stack and 180.0/183.4 dB for the 3-stack. The 1-stack FoM_{SNDR} of 177.9 dB is in line with a prior reported CTΔΣM having a very similar architecture with a 3rd-order loop filter and FIR DAC feedback. With 3-fold stacking and corresponding 3-fold reduction in the input bias current, the FoM_{SNDR} improves to 180.0 dB. This 2.1 dB increase in the Scherier FoM, implying a significant improvement in the ADC's power efficiency while other performance metrics remain the same, demonstrates the efficacy of the proposed technique.

Table 3.1

Summary and comparison with recently published audio-band ADCs.

	Billa JSSC'17 [65]	Jang JSSC'19 [63]	Gonen JSSC'20 [66]	Billa ASSCC'19 [77]	Wang JSSC'19 [69]	Liao JSSC'19 [71]	Jang ISSCC'20 [76]	This Work	
								1-stack	3-stack
Topology	CT 1b FIR DAC	CT 1.5b Neg.-R	CT Zoom	CT 2-1 MASH FIR	DT Increment	DT 2-1 MASH	CT Neg.-R 1.5b FIR	**CT 1b FIR DAC OTA-stacking**	
Tech. (nm)	180	65	160	180	65	65	65	**65**	**65**
Area (mm^2)	1	0.14	0.27	0.64	0.134	0.41	0.28	**0.25**	**0.39**
Supply (V)	1.8	1.2	1.8	1.8	1.2	1	1.2	**1**	**1**
BW (kHz)	24	24	20	24	20	25	24	**20**	**20**
f_s (MHz)	6.144	6.144	5.12	6.144	10.24	5	8	**6.4**	**6.4**
SNDR (dB)	98.5	94.8	106.4	100.6	100.8	94.6	99.4	**98.0**	**97.8**
DR (dB)	103.6	98.2	108.5	104	101.8	98.5	103.5	**101.3**	**101.2**
SFDR (dB)	107.6	107	113	109	N/A	100.3	110.2	**111.2**	**110.3**
Power (µW)	280	68	618	560	550	175	134	**202**	**121**
FoM_{SNDR}	177.8	179.5	181.5	180.2	176.4	176.2	181.9	**177.9**	**180.0**
FoM_{DR}	182.9	183.6	183.6	183.6	177.4	180.1	186	**181.3**	**183.4**

3.6 Conclusion

A novel technique based on OTA-stacking for improving the power efficiency of oversampled ADCs is reported. The benefits with respect to an ADC's dynamic range and power tradeoff being far significant compared to an amplifier noise-power tradeoff was theoretically established. This motivated the use of OTA-stacking in an oversampling ADC. A classical audio-band CTΔΣM's design space was chosen for implementation. To integrate the proposed continuous-time G_m-boosting functionality in a CTΔΣM, several additional techniques were incorporated. Chopping was used to allow an effective dc gain for the ac-coupled/dc-blocking OTA to be used in an integrator. A critical issue of unwanted frequency response notches due to the dc blocking was resolved by coinciding these with nulls of FIR feedback with the selection of appropriate filter order and chopping frequency. Finally, the swing and gain limitations of the

stacked-OTA were addressed using a four-stage feedforward compensated op-amp. Consistent performance metrics with >101 dB DR and <-110 dB HD3 were reported from two prototype 1- and 3-stack ADCs. A Schrier FoM_{DR} of 183.4 dB was achieved form the 3-stack ADC, which is competitive with state-of-the-art and 2.1 dB better than the 1-stack version with the same SNDR and DR, thereby establishing the utility of the techniques proposed. The techniques can be readily integrated with other recent FIR feedback based CTΔΣMs with negative-R assistance [76], [77], multi-stage noise shaping topology, and, in general, can be ubiquitously integrated with any precision oversampling ADC.

Chapter 3, in part, contains materials from "Somok Mondal, Omid Ghadami and Drew A. Hall, An Audio-band Continuous-time Delta Sigma Modulator using Chopped AC-coupled OTA-Stacking" that is being prepared for publication. The dissertation author was the primary investigator and author of this paper.

Chapter 4.

A 67-µW Ultra-Low Power PVT-Robust MedRadio Transmitter

4.1 Introduction

The IoT era is experiencing rapid growth with deployment of a wide variety of sensor nodes, most notably for healthcare monitoring and industrial automation. An important distinction from classic radios is that such IoT nodes only need to wirelessly communicate over short distances, typically ~1-2 meters, to reach a nearby data-aggregator (*e.g.*, smartwatch, smartphone, etc.), as shown in Figure 4.1(a). Owing to their autonomous and unobtrusive nature, enabling high deployment lifetimes through ultra-low power (ULP) operation is critical and often achieved through aggressive duty cycling.

Hence, simplistic transmitter topologies are preferred. In contrast to conventional radios, the power amplifier (PA) in a short-range radio is not the highest power consuming block due to the low output power, P_{out}. Instead, the frequency synthesizer or phase-locked loop (PLL) consumes a significant fraction of the overall transmitter power. The MedRadio/ISM band (~400 MHz) is widely used for the aforementioned applications due to its relatively low carrier frequency

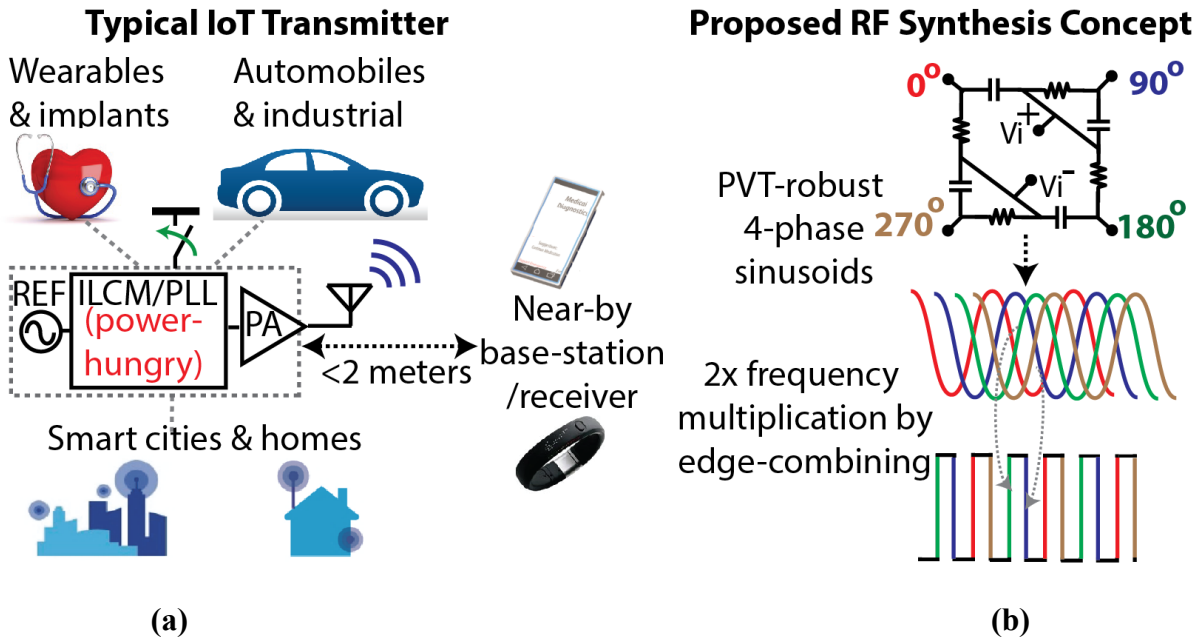


Figure 4.1 (a) A typical IoT transmitter and applications. (b) Conceptual overview of the proposed technique with a 2× multiplier example.

and considering the link distance [78]. To generate this RF carrier in an ULP manner, ring oscillator (RO)-based injection-locked clock multipliers (ILCMs) with small frequency multiplication factors (~8-12×) are regarded as the state-of-the-art [79]–[83].

Excellent low-power performance using open-loop ILCMs has been reported in [79]. However, without a dedicated frequency tracking loop (FTL) or PLL to continuously set the oscillator frequency and ensure lock leads to an inevitable compromise in the robustness, especially since ROs are very sensitive to process, voltage, and temperature (PVT) variation. Henceforth, latter works have performed an initial frequency calibration [80], [83] or used temperature compensation techniques [82], at the expense of higher power consumption. The former technique only accounts for static variations and suffers from slow start-up if calibration is

needed each time. While dynamic temperature variation is addressed in the latter work, the RO sensitivity to supply voltage is not addressed. Dynamic voltage variation is important since IoT sensor nodes are often powered through energy harvesting, the design of which can be relaxed if imprecise voltage regulation and slow drift can be tolerated.

Towards this end, a new transmitter architecture is introduced to simultaneously realize ULP operation and ensure PVT robustness. Illustrated in Figure 4.1(b), the key idea is to use a passive polyphase filter (PPF) to generate PVT insensitive, multiphase sinusoids that are subsequently used for frequency multiplication via edge combining. Fast start-up and a high-efficiency, low P_{out} inverse class-E PA are other key features of this work. The prototype 400 MHz narrowband MedRadio transmitter was fabricated in a 22 nm CMOS FDX process and achieves state-of-the-art performance.

4.2 MedRadio Transmitter Architecture

The proposed transmitter architecture is shown in Figure 4.2. A differential crystal oscillator (DXO) generates a 50 MHz reference frequency. An amplitude control loop controls the swing to minimize power and a chirp injector enables fast start-up. Similar to ILCMs, the small frequency multiplication factor (8×) needed for the MedRadio carrier frequency is leveraged to synthesize the 400 MHz carrier from the 50 MHz reference without a PLL. This is done with the aid of a 16-phase passive *RC* PPF integrated within the DXO. The polyphase sinusoids at 50 MHz are generated in a PVT-insensitive, calibration-free manner and, importantly, incur no additional

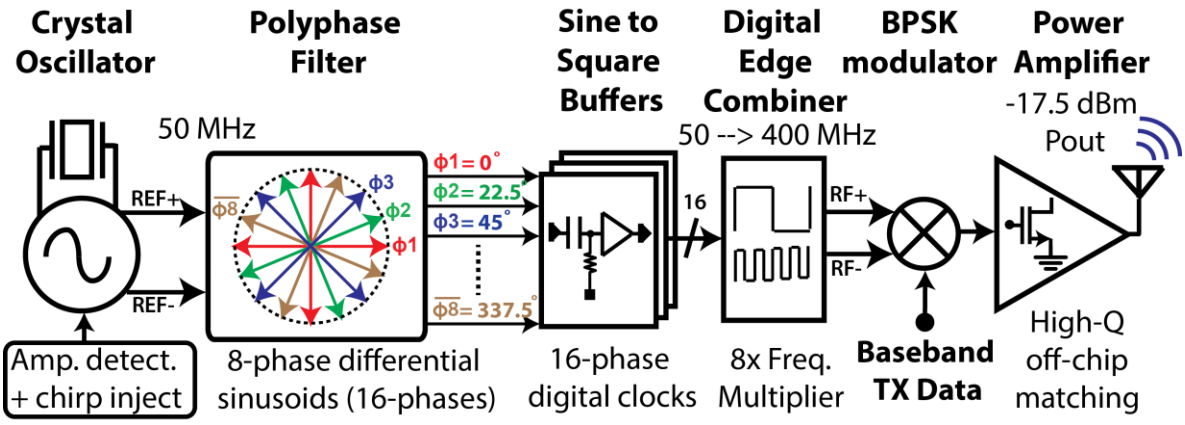


Figure 4.2 Proposed MedRadio transmitter architecture.

power overhead. It may be noted that integrating a PPF with a bulk acoustic wave (BAW) resonator was reported in [84] to generate 4-phases for quadrature phase shift keying (QPSK) modulation. In this work, the 16-phases are buffered and processed by a digital edge combiner for RF carrier synthesis. The resulting differential RF carrier is binary phase-shift keying (BPSK) modulated and transmitted via an inverse class-E PA with an off-chip matching network and P_{out} of -17.5 dBm.

4.3 Circuit Implementation

4.3.1 Current-Reuse Differential Crystal Oscillator

The proposed PPF-based technique requires a differential reference at 50 MHz generated by the digitally current-tunable DXO, as shown in Figure 4.3(a). The oscillator uses cross-coupled differential pairs that are ac-coupled by 200 fF capacitors, C_{hp}. This prevents latch-up due to the high dc impedance of the crystal resonator. Furthermore, the biasing resistors, R_{hp}, dampen unwanted low-frequency parasitic oscillation modes due to the ac-coupling. Both the ac-coupling and resistive biasing techniques are incorporated from [85]. The ac-coupling also provides an

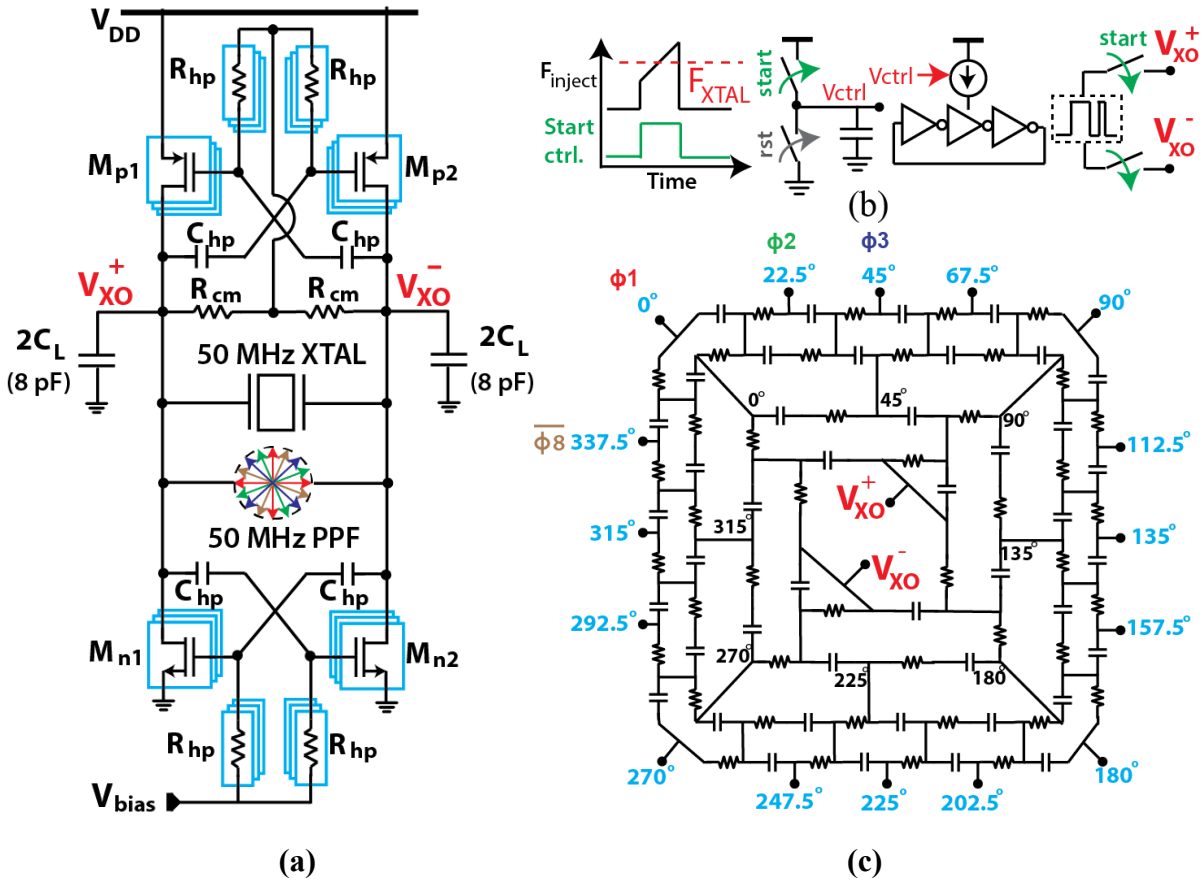


Figure 4.3 Implementation of (a) differential current-reuse crystal oscillator, (b) chirp injector, and (c) 16-phase, 4-ring passive *RC* polyphase filter.

opportunity to use complementary cross-coupled transistors. A current-reuse structure with 2× transconductance G_m boosting is realized to improve the power efficiency. The NMOS differential pairs are biased to set the desired current whereas the PMOS devices are self-biased by the output common-mode voltage, as shown in Figure 4.3(a).

Arrays of switchable G_m blocks provide the digital control feature. A Schmitt-trigger-based amplitude detector regulates the output amplitude and minimizes the power consumption for a one-time setting of the DXO. It may be noted that the criteria to avoid parasitic oscillations

depends on the $G_{\mathrm{m}}R_{\mathrm{hp}}$ product. Hence, R_{hp} is tuned in tandem with G_{m}. The overall transmitter duty-cycling is limited by the crystal oscillator start-up time. To enable fast start-up, chirp injection is used. As shown in Figure 4.3(b), a current starved voltage-controlled oscillator (VCO) is controlled by a ramp to inject frequencies swept across the 50 MHz reference frequency at start-up. The crystal is an Abracon ABM10W with a 4 pF load capacitance, C_{L}, and an 8.4 Ω equivalent series resistance (ESR).

4.3.2 Passive RC Polyphase Filter

The *RC* PPF used to generate the 8-phase differential sinusoids is shown in Figure 4.3(c). The choice of R and C values impacts the phase noise where a larger C or charge swing is associated with lower phase noise. Each PPF unit resistor, R, is 37 kΩ while each unit capacitor, C, is 85 fF and loads the DXO negligibly considering its own C_{L}. An additional fourth outer balanced *RC* ring in the PPF performs phase averaging and maintains symmetry when the outputs are equally loaded.

The PPF robustness is well known. For a 4-phase PPF it can be shown that a small ΔRC change in the RC product (*e.g.*, due to PT variations) results in each phasor being shifted equally by $\Delta RC/2RC$ and attenuated [86]. The generated phasors incur no frequency error and exhibit no voltage dependence. Systematic imbalance and mismatch do result in spurs at multiples of the reference frequency; however, good carrier-to-spur ratio (CSR) is maintained due to the harmonic suppression of the PA.

4.3.3 RF Synthesis by Edge Combining and Data Modulation

The differential PPF outputs are buffered using ac-coupled inverters that also convert the sinusoids to square wave digital signals, as shown in Figure 4.4(a). The edge combining is

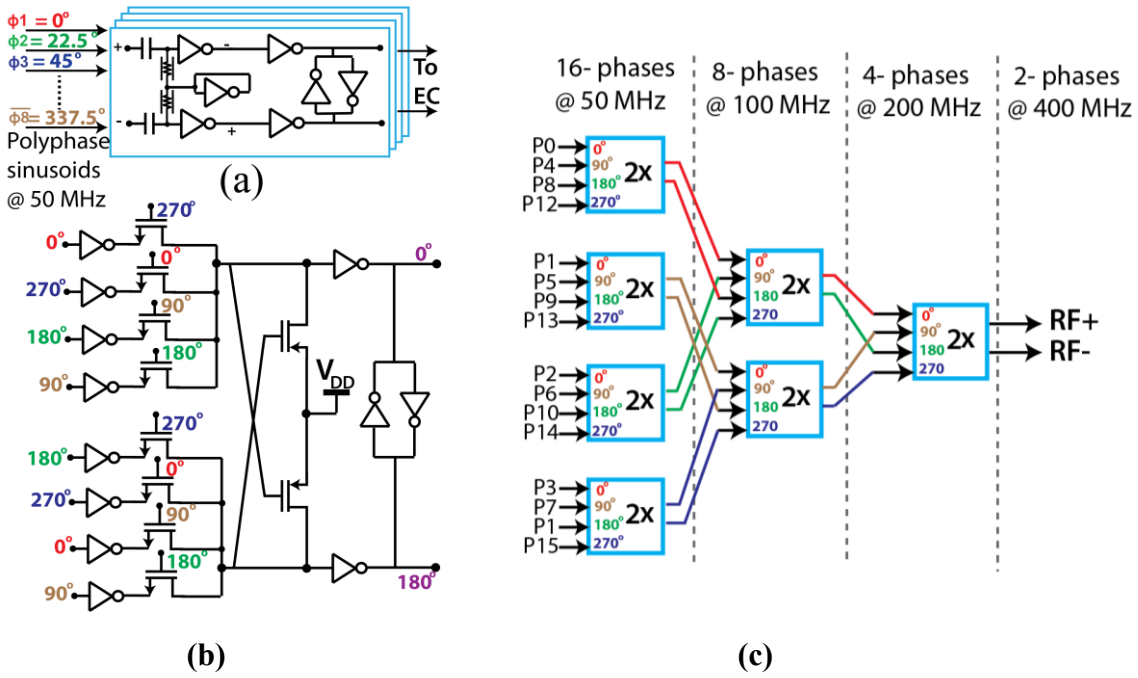


Figure 4.4 Implementation of (a) PPF output buffer, (b) 2× frequency multiplier, and (c) 8× frequency multiplier via edge combining.

performed with transmission gate logic based ULP digital circuits. Implementation of a 2× multiplier block is shown in Figure 4.4(b). Multiple such blocks arranged in a tree-like structure, as shown in Figure 4.4(c), are used to synthesize the differential 400 MHz RF carrier. BPSK modulation is realized with a phase mux controlled by the baseband data.

4.3.4 Power Amplifier

A generic PA, as shown in Figure 4.5(a), comprises a resonant network based on the PA's class and a matching network to transform the antenna load, R_{L}, by a factor N to an impedance $R_{\mathrm{p}} = NR_{\mathrm{L}}$ and thereby set a desired $P_{\mathrm{out}} \propto V_{\mathrm{DD}}/R_{\mathrm{p}}$, where V_{DD} is the supply voltage. For most PA classes, the low P_{out} (< 20 μW) requirement translates to $N > 1$ or R_{p} to be a few kΩs as opposed to a few Ωs in a conventional high P_{out} PA. This causes significant losses in the matching

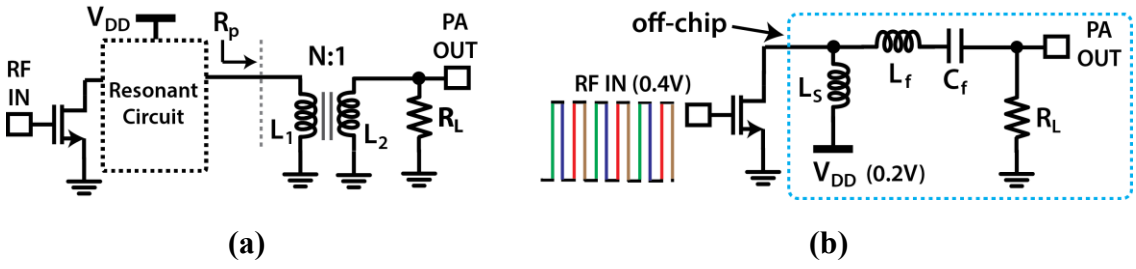


Figure 4.5 Implementation of a (a) generic PA and (b) inverse class-E PA.

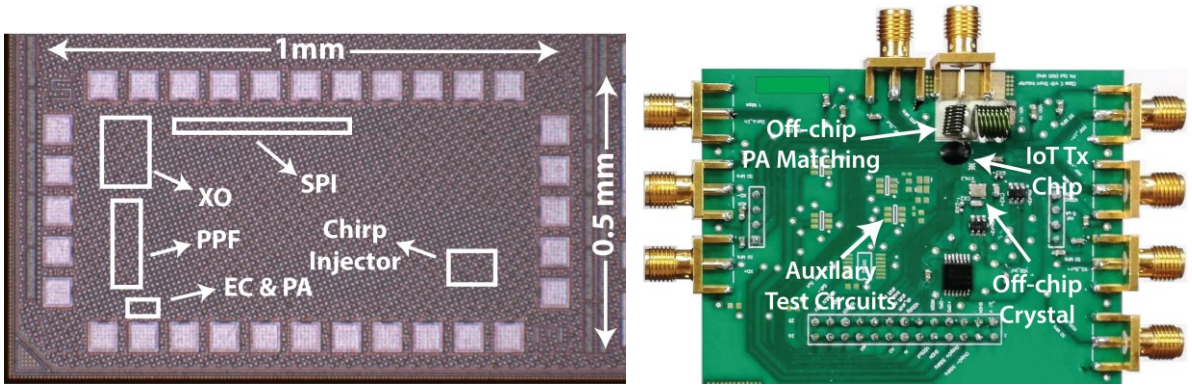
network [46] that severely limits the efficiencies of short-range PAs. In this work, a class-E PA with a shunt inductor or inverse class-E [87] with

$$P_{\text{out}} = \frac{8}{\pi^2(\pi^2+4)} V_{\text{DD}}^2/R_{\text{p}} = 0.058\, V_{\text{DD}}^2/R_{\text{p}} \tag{4.1}$$

is implemented. A dual supply scheme with a PA V_{DD} of 0.2 V, half of the 0.4 V core, is used. Thus, a low P_{out} is readily delivered, eliminating the need for any impedance transformation ($N = 1$). High-Q off-chip 50-130 nH Coilcraft inductors are used for the implementation shown in Figure 4.5(b).

4.4 Measurement Results

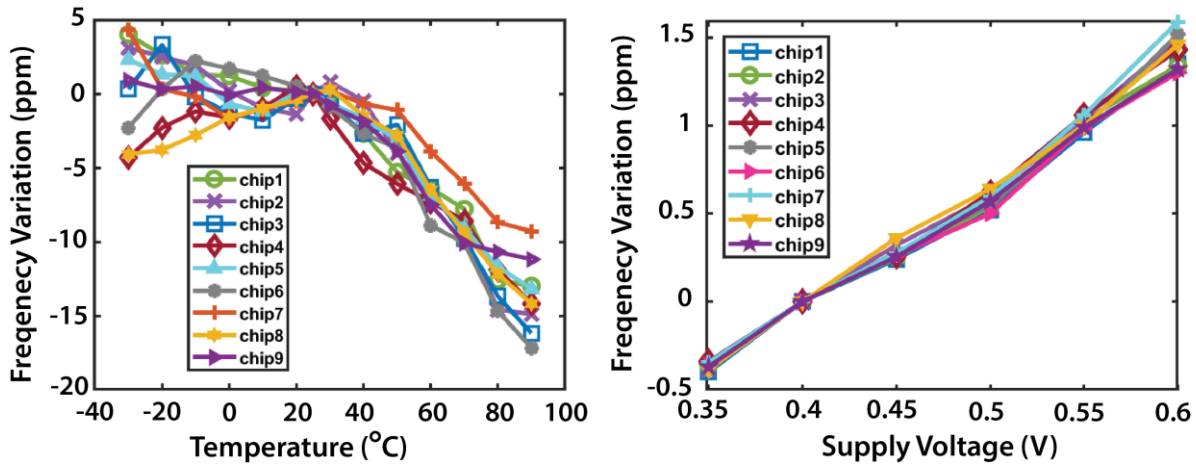
This MedRadio transmitter was fabricated in a 22 nm CMOS FDX process and occupies an active area of 0.03 mm^2. The DXO, edge combiner, and PA drivers are operated at 0.4 V while the PA is operated at 0.2 V. A chip micrograph and a photograph of the printed circuit board implementation with the off-chip components used are shown in Figure 4.6.



(a) **(b)**

Figure 4.6 Annotated (a) chip micrograph and (b) photograph of the printed circuit board (PCB).

The key novelty of this work is the PVT-robust frequency synthesis and hence relevant measurements are discussed first. The 8× frequency multiplication functionality remained consistent over a wide temperature range (-30 to 90 °C). The associated frequency variation of the generated 400 MHz RF carrier measured over multiple chips (n = 9) is plotted in Figure 4.7(a) and is less than 25 ppm, validating the stability of the reference generated from the DXO with integrated PPF. Excellent supply insensitivity is maintained with less than 2 ppm frequency variation when the supply was swept from 0.35 to 0.6 V, as shown in Figure 4.7(b). It may be noted that this is a significant benefit compared to ILCMs that suffer from poor line sensitivity and need re-calibrating with voltage drift. The measured phase noise of the RF carrier and the reference DXO are shown in Figure 4.8. A phase noise of -109 dBc/Hz at 100 kHz offset of the RF carrier was measured at room temperature. This remains consistent over temperature, as shown in Figure



(a) **(b)**

Figure 4.7 Measured frequency variation of the synthesized RF carrier versus (a) temperature and (b) supply voltage.

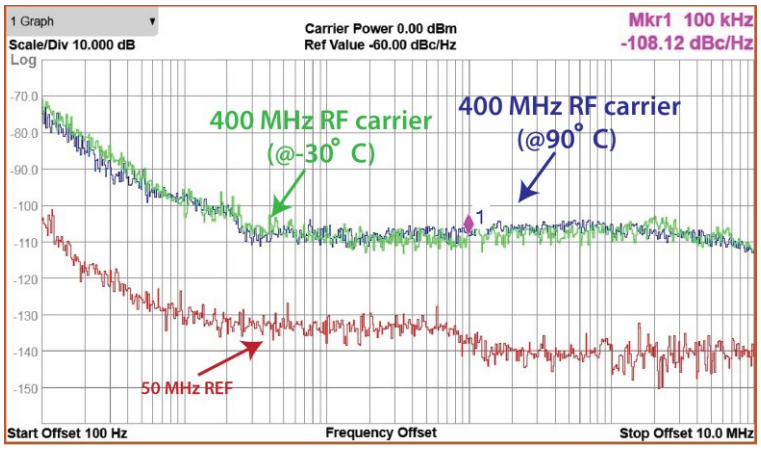


Figure 4.8 Measured phase noise of the 50 MHz DXO and the synthesized 400 MHz RF carrier for the temperature endpoints of -30 and 90 °C.

4.8, demonstrating the temperature robustness. The spectrum of an unmodulated transmitter output is shown in Figure 4.9 along with overlaid plots at different temperatures for comparison. The CSR

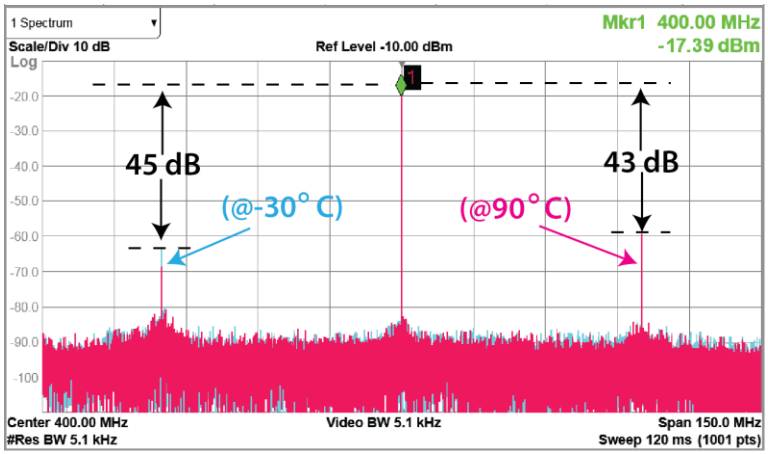
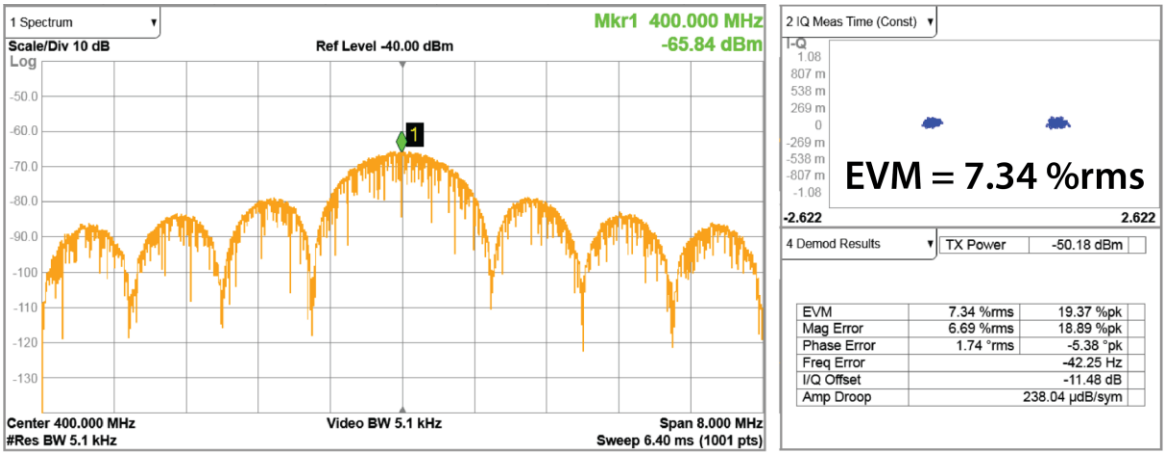


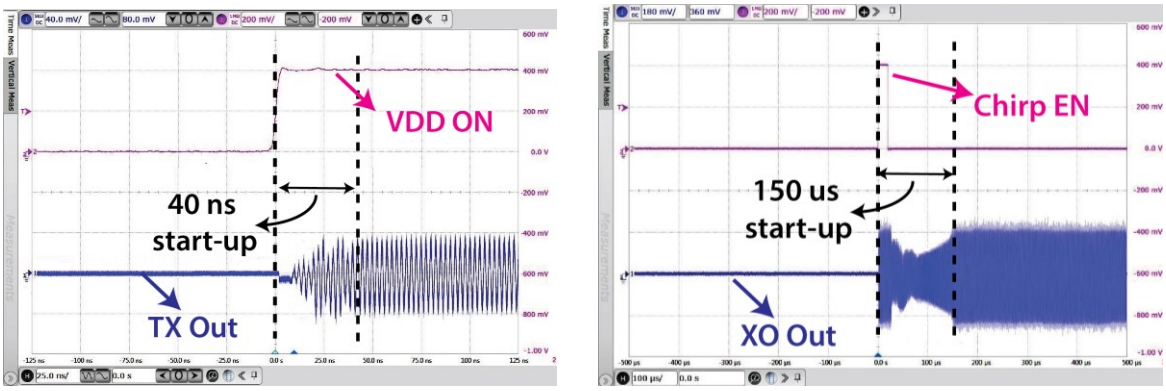
Figure 4.9 Measured unmodulated transmitter output spectra at room temperature and temperature endpoints of -30 and 90 °C.



(a) **(b)**

Figure 4.10 Measurements of BPSK modulated (a) received spectra and (b) demodulated constellation at 1 Mbps data-rate.

is better than 40 dB across temperature. Overall, the MedRadio regulations which require a 100 ppm/°C frequency accuracy over 0 to 55 °C and attenuation of out-of-band spurs by 20 dB are met with significant margin. The spectrum of the data transmitted and received using 400 MHz quarter-



(a) **(b)**

Figure 4.11 Measured start-up transients for (a) transmitter and (b) DXO.

wave whip antennas at 1-meter separation is shown in Figure 4.10. The error vector magnitude (EVM) is 7.34% rms at a 1 Mbps data-rate. The open-loop operation of the frequency synthesizer permits aggressive duty-cycling (considering only the frequency multiplier and PA). Contrary to ILCMs where a RO needs to first have stable oscillation set-up and then wait to get locked, the start-up with the proposed technique is instantaneous, in theory. The settling time upon applying a ramp on the supply is shown in Figure 4.11(a) and confirms start-up within ~10 cycles of the RF carrier (< 40 ns). A power-efficient overall shutdown feature for sensor node is also supported by the fast DXO start-up. With a chirp-injection settling time of 150 µs, shown in Figure 4.11(b), compared to an otherwise more than 3 ms slow settling, is achieved. This work is summarized in Table 4.1 and compared to prior relevant short-range transmitters [76]–[78], [81], [87]–[97]. Finally, survey plots showing transmitter energy-efficiency versus power consumption and the transmitter global efficiency versus the output power are presented in Figures 4.12 and 4.13, respectively.

Table 4.1 Comparison of Short-Range Narrowband Transmitters

	JSSC'11 [79]	TBioCAS'13 [83]	RFIC'13 [98]	JSSC'14 [80]	RFIC'15 [97]	ISSCC'19 [91]	This work
Supply (V)	0.7	0.6	0.7/1.2	0.8	1.2	1.2	**0.4/0.2**
Technology (nm)	90	90	130	65	130	65	**22 FDX**
Active Area (mm^2)	0.04	0.06	0.41	0.08	0.29	0.49	**0.03**
Frequency (MHz)	400	400	405	900	915	2400	**400**
	Frequency Synthesizer						
Phase Noise (dBc/Hz)	-105.2 @0.3 MHz	-87.9 @0.3 MHz	-69 @0.1 MHz	-100 @1 MHz	-100.2 @1 MHz	-118 @1 MHz	**-109 @0.1 MHz**
Power (µW)	<78*	-	72	538	224	-	**10**
Freq. Multiplier	9×	25×	25×	9×	60×	1×	**8×**
CSR (dB)	44	22	48	56	-	-	**45**
	Power Amplifier						
P_{out} (dBm)	-17	-17	-16	-15	-18	-8.4	**-17.5**
PA Efficiency (%)	30	-	33	9	12.5	-	**40**
Power (µW)	<78*	-	80	351	110	-	**44**
	Crystal Oscillator/Reference						
Frequency (MHz)	45	16	-	100	16	16	**50**
Power (µW)	<12	External	External	External	32	External	**13**
	Transmitter						
Topology	ILRO+EC-PA	2-step ILRO	PLL+PA	ILRO+PA	PLL+PA	PO.+PLL calib.	**XO-PPF+EC+PA**
Modulation	BFSK	OOK	BFSK	QPSK	FSK	GFSK	**BPSK**
Data-rate (Mbps)	0.2	1	0.08	10	3	1	**1**
Energy/bit (pJ/bit)	450	160	2375	130	122	606	**67**
Settling Time (ns)	250[1]	250[1]	-	88[1]	-	-	**40[1] / 150 µs[2]**
PVT-robust?	P× V× T×	P✓ V× T×	P✓ V✓ T✓	P✓ V× T×	P✓ V✓ T✓	P✓ V✓ T✓	**P✓ V✓ T✓**
Calibration reqd.?	✓	✓	×	✓	×	×	**×[#]**
Total Power (µW)	90	160	190	1,300	367	606	**67**
Global Efficiency%	22	16	13	4	12	24	**27**

Global Efficiency% = P_{out} / Total Power; ILRO: Injection-locked RO; PO: Power oscillator; EC: edge combiner; XO: crystal oscillator;

[#]XO calibrated once but not repeated for dynamic variations; Start-up time [1]w/o XO and [2]w/ XO; *EC and PA are merged and reported together

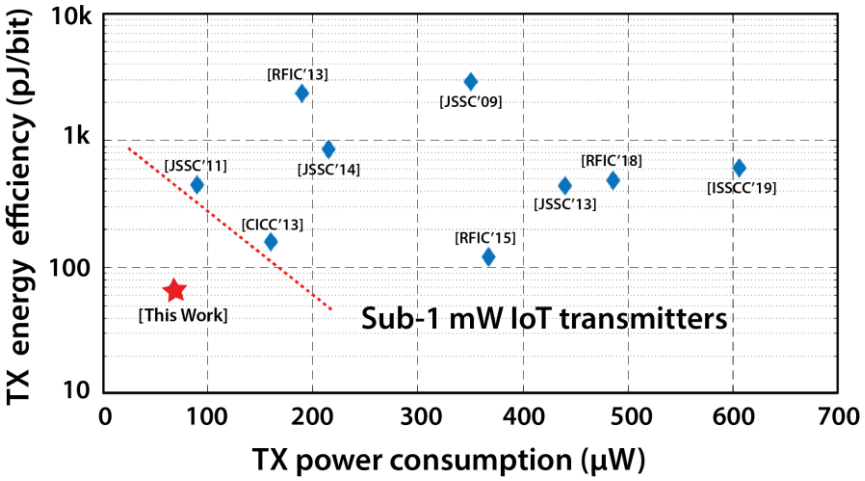


Figure 4.12 Transmit efficiency compared against prior sub-1 mW transmitters.

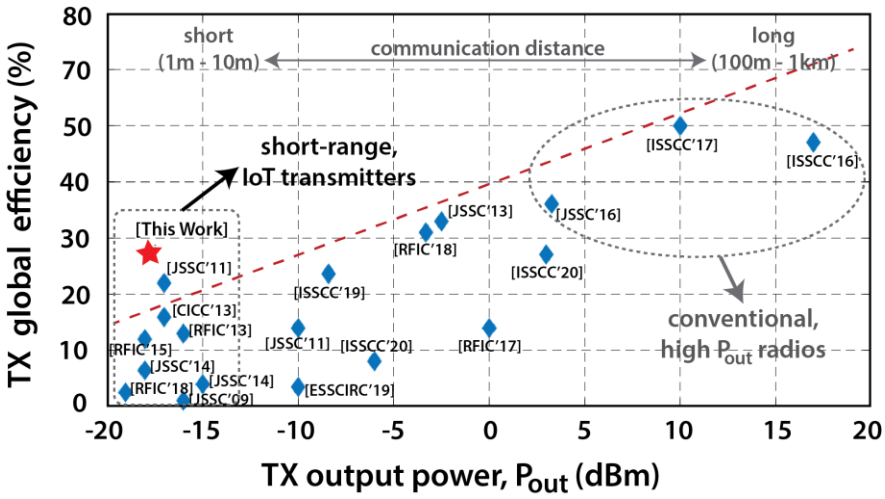


Figure 4.13 Transmitter global efficiency compared against prior works.

4.5 Conclusion

An ultra-low power MedRadio transmitter is presented. Robustness of the RF frequency synthesis is enabled with the aid of a passive PPF that is integrated within the DXO and hence has no power overhead and does not require any calibration. Although the DXO is trimmed once for amplitude regulation, re-calibrations to account for dynamic VT variations are not needed. The proposed concept can also be extended for higher frequency or smaller area applications using film bulk acoustic resonators (FBARs). In this work, at a data-rate of 1 Mbps, an energy efficiency of 67 pJ/bit is achieved. Aggressive duty-cycling of 40 ns is supported. A class-E inverse PA operates with a 40% efficiency delivering a low output power of -17.5 dBm. To the authors' knowledge, a best-reported power consumption of 67 µW and a global efficiency of 27% for short-range narrowband transmitters is achieved.

Chapter 4, in part, contains materials from “Somok Mondal and Drew A. Hall, A 67-µW Ultra-Low Power PVT-Robust MedRadio Transmitter”, to appear in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2020, and its journal version that is being prepared for publication. The dissertation author was the primary investigator and author of these papers.

Chapter 5.

Summary

5.1 Summary of Dissertation

This dissertation presents several innovations made to analog front-ends and short-range transmitters, both of which are the most important and fundamental building blocks of IoT sensor nodes. All the proposed novelties are focused on addressing the key challenge in enabling these IoT devices, which is, enhancing the power efficiency. The following is a summary of the main novelties and results presented in the dissertation.

Chapter 2 describes an ultra-low power electrocardiogram (ECG) recording front-end intended for implantable sensors. The noise-limited, high power first stage of a two-stage amplifier utilizes stacking of operational transconductance amplifiers (OTAs) for noise and power efficiency improvements. The proposed technique involves upmodulated/chopped signals being applied to ac-coupled, stacked inverter-based OTAs that inherently sum the individual transconductances while reusing the same current, thereby enhancing the noise efficiency. Two prototype designs were fabricated in a 180-nm CMOS process. The three-stack version consumes 13.2 nW and occupies 0.18 mm^2, whereas the five-stack implementation consumes 18.7 nW and occupies 0.24 mm^2. State-of-the-art NEF and PEF metrics of less than unity, 0.86 and 0.99, respectively, are reported for the five-stack version. These correspond to ~3× improvement in terms of energy efficiency compared to prior ultra-low power, sub-100-nW amplifiers. This work was published

in the *IEEE International Symposium on Circuits and Systems* and the *IEEE Journal of Solid-State Circuits*.

Chapter 3 describes a continuous-time delta-sigma modulator (CTΔΣM) for audio applications. The same ac-coupled OTA-stacking technique proposed in Chapter 2 form the core novelty to improve the noise-efficiency of the first integrator. It is shown that OTA-stacking offers a more straightforward and significant benefit to improve over the dynamic range and power tradeoff of oversampling ADCs compared to benefits with respect to an amplifier's noise and power tradeoff. To incorporate this OTA-stacking technique into the ADC and maintain high linearity, chopping, FIR DACs, and a 4-stage feedforward compensated amplifier are used. Two ADCs were fabricated in a 65 nm CMOS process to validate the proposed concept. The 3-stack version achieves 97.8 dB SNDR and 101.2 dB DR in a 20 kHz BW while consuming only 121 μW from a 1 V supply. The Schreier FoM_{DR} is 183.4 dB for the 3-stack, 2.1 dB better than the 1-stack with the same SNDR and DR, thereby demonstrating the efficacy of the proposed technique.

Chapter 4 describes a 400 MHz narrowband MedRadio transmitter for short-range communication. A new technique for PVT-robust, calibration- and regulation-free synthesis of the RF carrier is reported based on generating poly-phasors at 50 MHz with no power overhead. This is accomplished using a passive polyphase filter (PPF) directly integrated within a crystal oscillator followed by an 8× edge combiner to synthesize the RF carrier with -109 dBc/Hz phase noise at 100 kHz offset. A dual supply, inverse class-E power amplifier is implemented for high efficiency at low output power (-17.5 dBm). Open-loop operation permits aggressive duty-cycling (< 40 ns start-up time). State-of-the-art ultra-low power is reported from a prototype BPSK transmitter fabricated in 22 nm CMOS FDX when operated from a 0.4/0.2 V supply consuming 67 μW with

27% global efficiency. This work will appear at the *IEEE Radio Frequency Integrated Circuits Symposium*.

5.2 Areas of Future Work

The two key contributions of this work: 1) OTA-stacking for precision analog front-ends and 2) polyphase filter-based frequency synthesis for short-range transmitters can be expanded on in several ways.

OTA-stacking is a very promising approach which fundamentally improves noise-efficiency of amplifiers. This can be ubiquitously incorporated into all sensor applications, beyond the biological sensing and the audio sensing regimes, such as image and optical sensing, temperature and environmental sensing, chemical sensing, motion and vibration sensing, etc., all of which are typically noise-limited applications. Yet another useful and somewhat obvious extension of the stacking technique would be to use these for the low noise amplifiers (LNAs) in wireless receiver front-end as extensions to existing current reuse LNAs [99] to show benefits in terms of noise figure. Another scope of future work could be to use it for high speed sensor or ADC applications. This may offer implementation benefits since the ac-coupling inherently becomes easier at high frequencies, thereby removing the coupling capacitor area overhead drawback. As an example, stacking could be used in a wideband bandpass CTΔΣM for RF digitizing applications such as [72]. Additionally, a bandpass ADC would not require FIR feedback. Apart from improving the noise-efficiency, the G_{m} -boosting also offers wider bandwidth. This aspect with respect to bandwidth extension and its applicability remains to be explored.

The transmitter at 400 MHz could be extended for use in higher frequencies such as at 2.4 GHz for Bluetooth low energy (BLE) applications by integrating the polyphase filter with a film bulk acoustic resonator (FBAR) instead of a crystal. Injection locking with small multiplication factor has been proposed for several other applications recently such as mm-wave frequency synthesis where an RF PLL output is further translated to a higher frequency by injection locking [100]. The polyphase filter-based approach, in theory, could also be useful for these application by essentially replacing the injection locked multipliers without the need for power hungry and complex frequency tuning or calibration.

Overall, both the main contributions of this dissertation, namely OTA-stacking and PPF-based frequency synthesis, though intended for low-power IoT nodes here, are very generic in nature, and can therefore find use in a wide-variety of applications.

Appendix 1

FoM in a Noise-limited CTΔΣM

A theoretical limit for the FoM of a CTΔΣM, considering the first integrator resistors and the input stage of the OTA being the sole contributors to noise and the input stage of the OTA being the only power consuming block, is derived here. For a differential implementation, the input-referred noise can be expressed as

$$\overline{v_{\text{noise}}^2} = 16k_{\text{B}}TR + \frac{8k_{\text{B}}T\gamma}{g_{\text{m}}}, \tag{A1.1}$$

where R is the input and DAC resistor value, $g_{\text{m}}$is the transconductance of the input device of the OTA, k_{B} is Boltzmann's constant, T is the temperature, and γ is a device noise coefficient. The value of R is typically maximized for linearity. This could be understood from an integrator transfer function $A(s)$ given by

$$A(s) = -\left(\frac{G_{\text{m}}R}{1 + G_{\text{m}}R}\right)\frac{1}{sCR} \tag{A1.2}$$

where G_{m} is the open-loop transconductance of the multi-stage OTA used in the integrator and C is the feedback capacitor of the integrator. Nonlinearities in the open-loop G_{m} can be suppressed if $G_{\text{m}}R$ is maximized. Therefore, the resistor noise dominates and the g_{m} is chosen such that the OTA noise is proportionately lower than the thermal noise. Selecting $g_{\text{m}} = \alpha/R$, implies the g_{m}

is high enough, based on the factor α, that the resistor noise is $\alpha/2\gamma$ larger than the transistor noise. Hence, although the ADC noise is determined by the resistor, one needs to burn power to keep the transistor noise floor well below the resistor's noise floor.

The peak SNDR for a 3rd order ΔΣM typically occurs at -3 dBFS, hence the Scherier FoM can be expressed as

$$FOM_{SNDR} = 10log\left(SNDR\ \frac{BW}{Power}\right) \tag{A1.3}$$

$$\cong 10log\left(\frac{\frac{1}{2}(2V_{\mathrm{DD}}/\sqrt{2})^2}{16k_{\mathrm{B}}TR\ *BW}\ \frac{BW}{V_{\mathrm{DD}}2I_{\mathrm{D}}}\right) \tag{A1.4}$$

$$\cong 10log\left(\frac{V_{\mathrm{DD}}}{8\alpha}\frac{g_{\mathrm{m}}}{I_{\mathrm{D}}}\ \frac{1}{4k_{\mathrm{B}}T}\right), \tag{A1.5}$$

where V_{DD} is the supply, BW is the ADC bandwidth, I_D is the drain current through the input transistors, and g_{m} is the corresponding transconductance. From (A1.5), it can be seen that $g_{\mathrm{m}}/I_{\mathrm{D}}$ directly impacts the FoM where $g_{\mathrm{m}}/I_{\mathrm{D}}$ can be increased by *2N* by stacking *N* inverters. The FoM in (A.5), for $\alpha = 16$ (transistor noise 12× lower than resistor noise with $\gamma = 2/3$), using a sub-threshold device parameter $\eta = 1.5$ and thermal voltage $V_{\mathrm{T}} = 26$ mV can be further simplified as

$$\begin{aligned} FOM_{\mathrm{SNDR}} \cong &-10\ log(4k_{\mathrm{B}}T) - 10\ log(8\alpha\ .\eta V_{\mathrm{T}}) \\ &+ 10\ log(V_{\mathrm{DD}})\ + 10\ log\ (N) \end{aligned} \tag{A1.6}$$

$$\cong 191 + 10\ log(\boldsymbol{V_{DD}})\ + 10\ log\ (\boldsymbol{N}). \tag{A1.7}$$

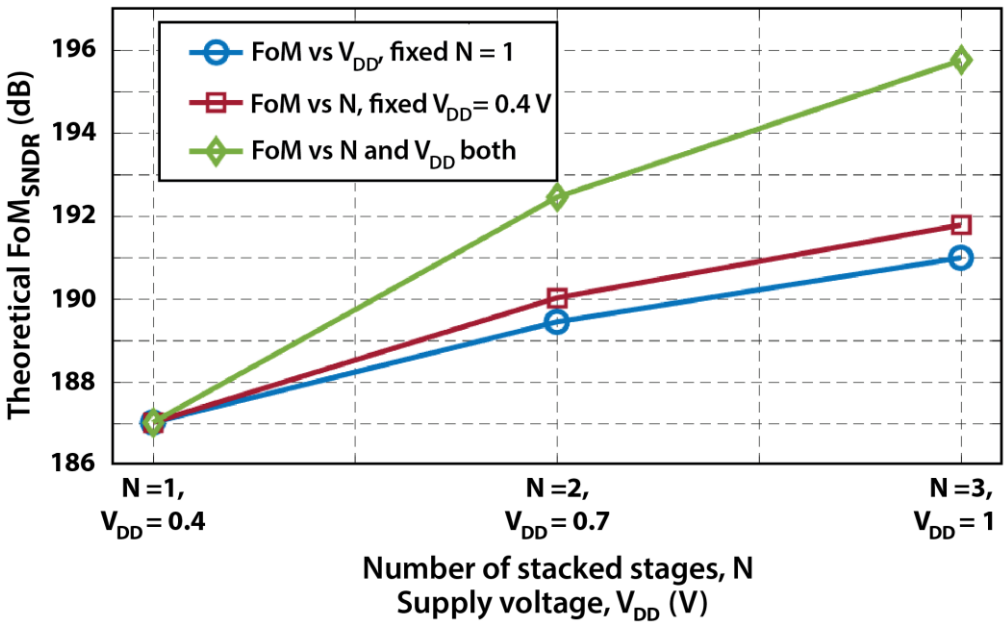


Figure A1.1 Tradeoffs in ADC FoM with stacking and supply voltage

The derived FoM limit in (A1.7) indicates improvements with an increase in both V_{DD} and N. These tradeoffs are further plotted in Figure A1.1. For a single stack, increasing V_{DD} alone can improve the FOM. This follows from (A1.4) – (A1.5) with the signal power increasing with V_{DD}^2 while the noise power dependent only to the first order over g_{m} or I_D. For a fixed low supply, say 0.4 V, stacking is beneficial as also shown in Figure A1.1. However, to accommodate stacking, an increase in V_{DD} is required, which fortunately, results in further improvements. Compared to operation at a low 0.4 V supply with a single stack, a 3-fold stacking with a higher 1V supply, theoretically leads to a 8.7 dB improvement in the Scherier's FoM as plotted in Figure A1.1.

Appendix 2

Loop-filter Coefficients of a CTΔΣM with FIR DAC

The synthesis procedure to determine the loop-filter coefficients for a CTΔΣM using a CIFF-B topology with FIR DACs as shown in Figure A2.1 is discussed here. In this topology the main feedback is an arbitrary *M*-tap FIR DAC, F(z) with coefficients a_i of the form

$$F(z) = \frac{1}{M}\left(a_0 + a_1 z^{-1} + \ \ldots \ + a_{N-1} z^{-(N-1)}\right). \tag{A2.1}$$

Additionally, a *M*-tap compensation FIR DAC, $C(z)$ with coefficients b_i is also used. The objective is to determine the coefficients $\widehat{k_2}$, $\widehat{k_3}$ as annotated in Figure A2.1 and the *M* filter taps b_i, given the arbitrary taps a_i and the desired noise transfer function $NTF(z)$.

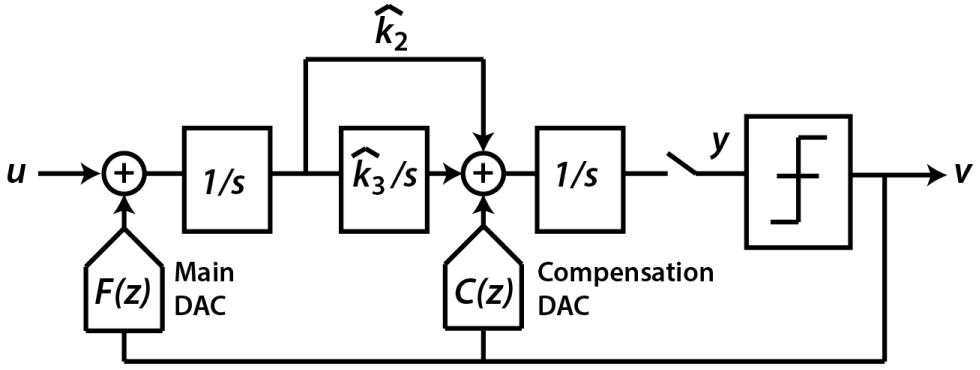


Figure A2.1 A CTΔΣM with CIFF-B topology and FIR feedback

The loop filter coefficients need to be synthesized such that response from the ADC output $v[n]$ to the quantizer input $y[n]$ also annotated in Figure A2.1 remains identical to that of a discrete-time ADC with the desired $NTF(z)$. Henceforth, the following equality needs to hold

$$\widehat{k_3}F(z)H_3(z) + \widehat{k_2}F(z)H_2(z) + C(z)H_1(z) = \frac{1}{NTF(z)} - 1. \quad \text{(A2.2)}$$

where $H_i(z)$ are the discrete-time (DT) transfer functions which result in the same impulses as a $1/s^i$ path corresponding to a non-return-to-zero (NRZ) feedback. and are listed in Table A2.1 below. These can also be evaluated in MATLAB using the '*c2d*' function. e.g. to evaluate discrete-time equivalent for the $1/s^3$ path, one can use ">>*c2d* (*tf* ([1], [1 0 0 0]),1)".

The equality in (A2.2) can have multiple solutions implying multiple coefficients can realize the same loop-filter. A set of real and positive solutions need to be determined. Upon numerically solving *M*+2 equations constructed form (A2.2) using *M*+2 different values of z, given the constraint z < 1, the *M*+2 unknows can be determined. For the ADC discussed in Chapter 3, with $M = 9$, $a_0 = 0, a_{1..8} = 1/8$ and the $NTF(z)$ synthesized using the Schrier's MATLAB

Table A2.1

DT equivalent transfer function for a continuous time path with NRZ feedback

	Path	**DT Transfer function**
$\boldsymbol{H_1}(z)$	$\frac{1}{s}$	$\frac{z^{-1}}{1-z^{-1}}$
$\boldsymbol{H_2}(z)$	$\frac{1}{s^2}$	$\frac{0.5(z^{-1}+z^{-2})}{(1-z^{-1})^2}$
$\boldsymbol{H_3}(z)$	$\frac{1}{s^3}$	$\frac{0.17z^{-1}+0.66z^{-2}+0.17z^{-1}}{(1-z^{-1})^3}$

toolbox [101], real and positive solutions are typically found upon using the synthesis procedure described above. Also, even when different sets of z are used, the resultant solutions or the coefficients are usually similar in terms of the numerical values.

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