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Electrical Properties of Modified Graphene and Carbon Nanotube Devices

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For my beloved family

ABSTRACT OF THE DISSERTATION

Electrical Properties of Modified Graphene and Carbon Nanotube Devices

by

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Graphene and carbon nanotubes are the two-dimensional and one-dimensional forms of carbon allotropes, respectively, and have been ideal materials for scientific and technological exploration due to their ultra small size and extraordinary physical properties such as high carrier mobility, large thermal conductivity and strong tensile strength. In this thesis, I focus on modifying the properties of graphene and carbon nanotubes, via chemical functionalization, strain, or encapsulation, so that they are better suited for applications.

To create a band gap in the otherwise gapless spectrum of graphene, one common route is chemical functionalization. However, most functionalization methods are invasive and result in degradation in graphene's quality. In contrast, our chemically functionalized graphene using organometallic chemistry behaves as semiconductors with improved on / off ratios, while retaining high mobility.

Application of strain in graphene is another route to tailor transport properties. We developed devices based on nano-electromechanical system (NEMS), which allows us to apply in situ strain in suspended graphene. Changes in contact resistance and mobility have been observed in single- and bi-layer graphene devices.

Apart from graphene, we also focus on carbon nanotube devices. We developed techniques to fabricate carbon nanotube devices encapsulated in hexagonal boron nitride (hBN) with zero-dimensional ohmic contacts. These devices can carry high current density, and Coulomb blockade diamonds with excited state have been observed.

Lastly, we explored a device geometry that combines both graphene and carbon nanotubes, with the goal of studying momentum-conserved tunneling between 1D and 2D systems. We developed techniques to fabricate suspended devices with dual gates, which allow us to observe interesting quantum transport features arising from both portions of graphene and carbon nanotubes. We also proposed hBN-based devices for future studies.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1. Introduction

Graphene and carbon nanotubes are interesting material platforms for scientific and technological exploration. When carbon atoms are arranged into a honeycomb structure in single two-dimensional plane, they become graphene[1, 2], the world's thinnest material that is only one atom thick. Since its first isolation from a bulk graphite pieces onto insulating substrates in 2004 by Dr. Geim and his colleagues in the University of Manchester[3], it has attracted enormous amount of attention from both scientific and technological communities. For instance, graphene's extraordinary electrical properties include ultra high carrier mobility[4, 5] and unique dispersion spectrum[1]; it has great potential to replace the current silicon-based industry and to become a promising candidate for next generation electronics. In addition to the electrical properties, the ultra high Young's modulus of 1TPa[6] makes graphene one of the strongest materials. It is so strong that one square meter graphene sheet could support a human standing on it. Graphene also has exceptionally large thermal conductivity of ~ 5,300 $W \cdot m^{-1}K^{-1}$, suggesting potential applications in thermal management[7].

Graphene also forms the basis of other members of the carbon family, such as carbon nanotube and fullerenes. Specifically, the one-dimensional material carbon nanotube can be obtained by rolling up a graphene sheet. Carbon nanotubes also have ultra high Young's modulus[8]. Depending on how the tube was rolled up, the electrical property ranges from metallic to semiconducting with band gaps of different sizes.[9]

These excellent physical properties have been exploited for various applications such as electronics, actuators, thermal conduction pastes, and sensors.

Despite the outstanding capabilities of graphene and carbon nanotubes, several obstacles are yet to be overcome before fully realization their promise for technological applications. For instance, graphene is gapless and cannot be switched off for digital electronic applications. Researchers seek to engineer band gaps in graphene via application of an external electric field[10–12], or strain[13–17], chemical modification[18–22], or lateral confinement such as patterning into nano-ribbons[23, 24]. So for an energy gap up to 250meV has been observed in bilayer graphene devices in the presence of an external electric field[10]. Nevertheless, it is still considered narrow for current Si-based electronics, which needs a band gap of 1.11 eV. Chemical modification is a simple and promising method but most of chemically derived graphene cannot maintain its original high quality. Carbon nanotubes can be gapped, though the gap size depends on chirality that is not readily controlled. It has been quite challenging to produce exclusively semiconducting nanotubes with a given chirality. In addition, carbon nanotubes can be used as the smallest electric wires but the current carrying capacity of 25 μA in each nanotube still creates a barrier in applications.

This thesis focuses on our work in modification of electronic properties of graphene and carbon nanotubes, including chemical funcionalization of graphene, *in situ* measurement of strain-dependence of transport properties of suspended graphene devices, carbon nanotube devices encapsulated in boron nitride and graphene-carbon nanotube junctions. The thesis is organized as follows. Chapter 2 begins with theoretical models of

the electrical dispersion relations of graphene and carbon nanotubes. Chapter 3 will describe the experiment procedures for graphene devices including graphene identification, fabrication procedures for substrate-supported and suspended graphene devices, transfer steps, and electrical characterizations. Chapter 4 discusses organometallic hexahapto functionalization of single layer graphene. Chapter 5 presents our transport measurements of suspended graphene devices under *in-situ* strain. Chapter 6 will describe the fabrication procedures for carbon nanotube devices. Chapter 7 will describe our technique for edge-contacting carbon nanotube devices encapsulated in boron nitride. By making 0-dimensional metallic contacts to 1D carbon nanotubes, we are able to fabricate ultra-clean carbon nanotube devices for transport studies. Chapter 8 will focus on the graphene-carbon nanotube hybrid devices including device fabrications and discussions of our preliminary results of electrical transports. Chapter 9 concludes the thesis with a summary and a brief discussion of outlook.

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Chapter 2. Band Structures of Graphene and Carbon Nanotube

2.1 Introduction

In this chapter, I will discuss the theoretical models of the band structures of single layer graphene and single-wall carbon nanotube using tight-binding approximation.[1] The linear energy-momentum dispersion relation of graphene at low-energies will be derived. The different dispersion relations of metallic and semiconducting carbon nanotubes will be derived from that of graphene using zone-folding approximation.[2]

2.2 Tight-Binding Calculation of Band Structure of Single Layer Graphene

Graphene is a two-dimensional material with carbon atoms arranged in a honeycomb lattice. Its real-space and reciprocal lattices are shown in Figure 2.1 (a) and (b), respectively. The band structure of single layer graphene can be calculated using the tight-binding method. The primitive vectors are

$$\vec{a}_1 = \frac{a}{2}(3, \sqrt{3}) \text{ and } \vec{a}_2 = \frac{a}{2}(3, -\sqrt{3}),$$

where a is the distance between two carbon atoms, $a = 1.42\text{Å}$.

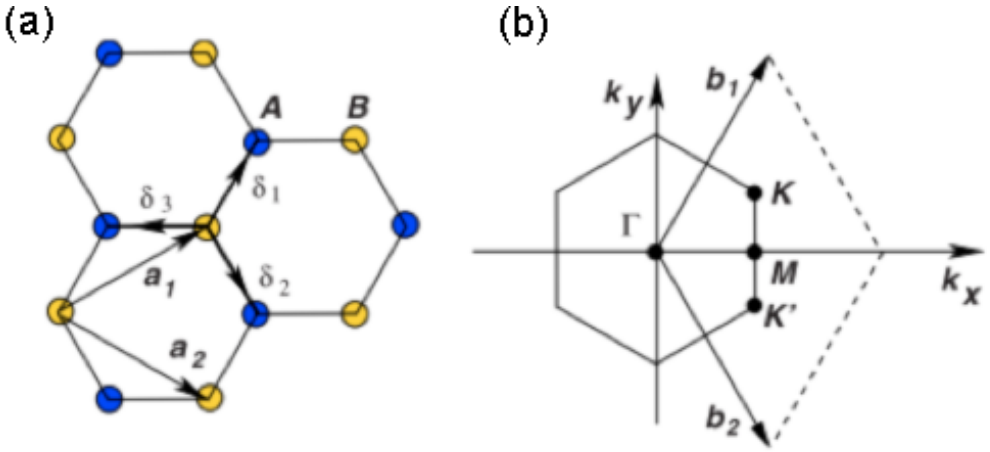

Figure 2.1. Lattice structure of graphene. (a). Real-space lattices. $\mathbf{a_1}$ and $\mathbf{a_2}$ and are the primitive vectors. δ_1, δ_2 and δ_3 are the nearest-neighbor vectors. (b). Reciprocal lattices. $\boldsymbol{b_1}$ and $\boldsymbol{b_2}$ are the reciprocal primitive vectors.[1]

The reciprocal primitive vectors are

$$\vec{b}_1 = \frac{2\pi}{3a}(1, \sqrt{3}) \text{ and } \vec{b}_2 = \frac{2\pi}{3a}(1, -\sqrt{3}).$$

Using the Bloch function, the wave function can be written as

$$\Phi(\vec{k}, \vec{r}) = \frac{1}{\sqrt{N}} \sum_{i=1}^{N} e^{i\vec{k}\cdot\vec{R}_i}\, \phi(\vec{r} - \vec{R}_i),$$

where N is the number of unit cells, $\vec{k}$ is the momentum, $\vec{R}_i$ is the position of ith atom. Then we can write down the secular equation for the two atoms A and B in a unit cell as

$$det[H - ES] = 0.$$

Then,

$$\begin{vmatrix} H_{AA} - ES_{AA} & H_{AB} - ES_{AB} \\ H_{BA} - ES_{BA} & H_{BB} - ES_{BB} \end{vmatrix} = 0,$$

where E is the eigenvalue and

$$H_{j,j'}(\vec{k}) = \langle \Phi_j | H | \Phi_{j'} \rangle \text{ and } S_{j,j'}(\vec{k}) = \langle \Phi_j | \Phi_{j'} \rangle.$$

Since the two atoms are equivalent,

$$H_{AA} = H_{BB} \text{ and } S_{AA} = S_{BB}.$$

In the following, we will solve the equation by only considering the contributions from the three nearest atoms, which are

$$\vec{\delta}_1 = \frac{a}{2}(1, \sqrt{3}),\ \vec{\delta}_2 = \frac{a}{2}(1, -\sqrt{3}) \text{ and } \vec{\delta}_3 = -a(1,0).$$

The elements in the secular equation can be written as following

$$H_{AA}(\vec{r}) = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N} e^{i\vec{k}\cdot(\vec{R}_{A,j} - \vec{R}_{A,i})} \langle \phi_A(\vec{r} - \vec{R}_{A,i}) | H | \phi_A(\vec{r} - \vec{R}_{A,j}) \rangle$$

$$= \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N} \langle \phi_A(\vec{r} - \vec{R}_{A,i}) | H | \phi_A(\vec{r} - \vec{R}_{A,j}) \rangle = E_{2p}$$

$$S_{AA}(\vec{k}) = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N} e^{i\vec{k}\cdot(\vec{R}_{A,j} - \vec{R}_{A,i})} \langle \phi_A(\vec{r} - \vec{R}_{A,i}) | \phi_A(\vec{r} - \vec{R}_{A,j}) \rangle = 1$$

$$H_{AB}(\vec{r}) = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N} e^{i\vec{k}\cdot(\vec{R}_{B,j} - \vec{R}_{A,i})} \langle \phi_A(\vec{r} - \vec{R}_{A,i}) | H | \phi_B(\vec{r} - \vec{R}_{B,j}) \rangle$$

$$= \gamma_0 u_0(\vec{k})$$

$$S_{AB}(\vec{k}) = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N} e^{i\vec{k}\cdot(\vec{R}_{B,j} - \vec{R}_{A,i})} \langle \phi_A(\vec{r} - \vec{R}_{A,i}) | (\vec{r} - \vec{R}_{B,j}) \rangle$$

$$\approx \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{3} e^{i\vec{k}\cdot(\vec{R}_{B,j}-\vec{R}_{A,i})}\langle\phi_A(\vec{r}-\vec{R}_{A,i})|(\vec{r}-\vec{R}_{B,j})\rangle$$

$$= s_0 u_0(\vec{k}),$$

where

$$\gamma_0 = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N}\langle\phi_A(\vec{r}-\vec{R}_{A,i})|H|\phi_B(\vec{r}-\vec{R}_{B,j})\rangle$$

$$s_0 = \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N}\langle\phi_A(\vec{r}-\vec{R}_{A,i})|\phi_B(\vec{r}-\vec{R}_{B,j})\rangle$$

$$u_0(\vec{k}) \approx \sum_{i=1}^{N}\sum_{j=1}^{3} e^{i\vec{k}\cdot(\vec{R}_{B,j}-\vec{R}_{A,i})} = \sum_{i=1}^{3} e^{i\vec{k}\cdot\vec{\delta}_i}$$

$$= e^{-ik_x a} + 2e^{ik_x\frac{a}{2}}\cos\left(\frac{\sqrt{3}}{2}k_y a\right).$$

By plugging in all elements in the secular equation, we get

$$\begin{vmatrix} E_{2p}-E & \gamma_0 u_0 - E(s_0 u_0) \\ \gamma_0 u_0^* - E(s_0 u_0^*) & E_{2p}-E \end{vmatrix} = 0$$

$$E(\vec{k}) = \frac{1}{1-s_0^2\left|u_0(\vec{k})\right|^2}\left[E_{2p} - s_0\gamma_0\left|u_0(\vec{k})\right|^2 \pm \left|u_0(\vec{k})\right|(E_{2p}s_0 - \gamma_0)\right]$$

$$= \frac{E_{2p} \pm \gamma_0\left|u_0(\vec{k})\right|}{1 \pm s_0\left|u_0(\vec{k})\right|}.$$

The resulting band structure can be seen in Figure 2.2, where the $E_{2p} = 0\ eV, \gamma_0 = -3.033eV$ and $s_0 = 0.129$.

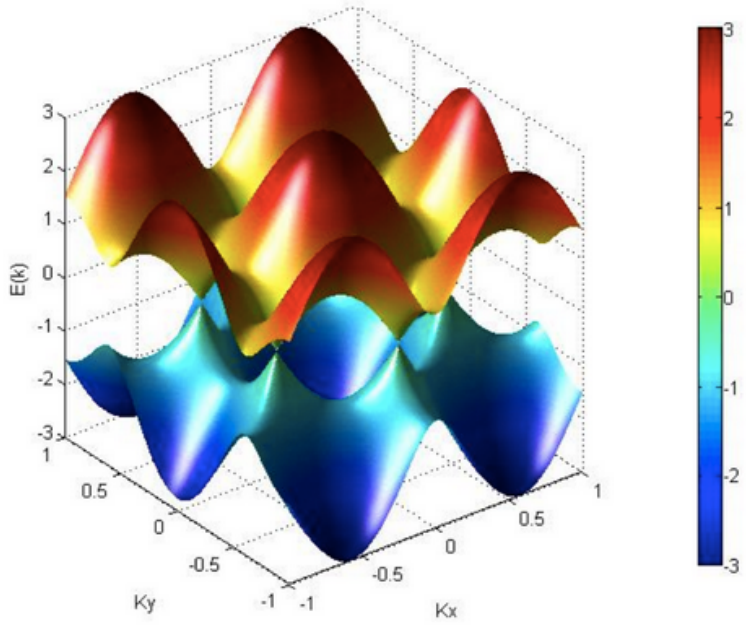

Figure 2.2. Electronic dispersion of graphene.[3]

2.3 Band Structures of Single-Walled Carbon Nanotubes

A single-walled carbon nanotube can be considered as a rolled-up sheet of graphene, and by rolling in different directions results in either metallic or semiconducting nanotubes. In Figure 2.3, a single-walled carbon nanotube is formed by rolling up along the chiral vector $\vec{C}_h$ with circumference $\left|\vec{C}_h\right|$. The vector can be further expressed as $n\vec{a}_1 + m\vec{a}_2$, where $\vec{a}_1$ and $\vec{a}_2$ are the unit vectors of the hexagonal lattice and n and m are integers. Thus, we can write down the diameter of the tube as

$$d_t = \frac{\left|\vec{C}_h\right|}{\pi} = \frac{a}{\pi}\sqrt{n^2 + nm + m^2},$$

where $a = 1.42\sqrt{3}$Å, and the chiral angle as

$$cos\theta = \frac{\vec{C}_h \cdot \vec{a}_1}{|\vec{C}_h| \cdot |\vec{a}_1|} = \frac{2n+m}{2\sqrt{n^2+nm+m^2}}.$$

With different chiral angle, the structure of tubes can be zigzag $(n,0)(\theta = 0^{\circ})$, armchair $(n,n)(\theta = 30^{\circ})$ and chiral $(n, m \neq n \neq 0)$ tubes, where the names "zigzag" and "armchair" refers to the end-view of the atomic arrangements of the nanotubes.

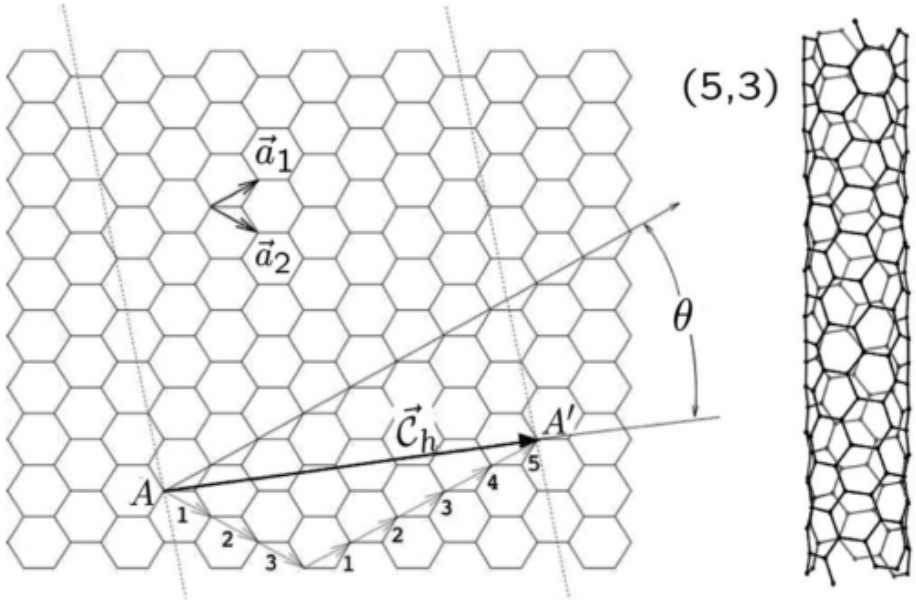

Figure 2.3. Forming a carbon nanotube by rolling up a graphene sheet along the $\vec{C}_h$ vector.[2]

The electronic structure of a carbon nanotube can be constructed by "slicing" the energy bands of graphene along the corresponding allowed $\vec{k}$ lines, which are determined by the periodic boundary condition along the circumference of the tubes. Here we consider the dispersion relations of two classes of nanotubes, metallic ones with $n - m = 3 \times (integers)$ and semiconducting ones with $n - m = 3\times(integers) \pm 1$. For metallic nanotubes, the $\vec{k}$ vector near the Fermi surface can be written as $\vec{k} = \vec{K} + \delta\vec{k}$. Using the reciprocal primitive vectors as an example, $\vec{K} = \frac{\vec{b}_1 - \vec{b}_2}{3} = (0, \frac{4\pi}{3a})$, so $\vec{k} = (\delta k_x, 4\pi/3a + \delta k_y)$. Applying the boundary condition,

$$e^{i\vec{K}\cdot\vec{C}_h} = 1,$$

the constraint is $\delta\vec{K} \cdot \vec{C}_h = 2\pi q$ (q integer). We can write down the general form the dispersion relation as $E^2(k_x, k_y) = \gamma_0^2|u_0|^2$. By expanding $|u_0|^2$ near the $\vec{K}$ point, we obtain

$$\left|u(k_x, k_y)\right|^2 \simeq \frac{3}{4}\left(\delta k_x^2 + \delta k_y^2\right) + O(\delta k^3).$$

Then, the dispersion relation near the Fermi level will be

$$E^{\pm}(\delta\vec{k}) \simeq \pm(\sqrt{3}a/2)\gamma_0\left\|\delta\vec{k}\right\|.$$

The Fermi velocity is $v_F = \sqrt{3}a\gamma_0/2\hbar \simeq 8.1\times10^5\ m/s$ for $\gamma_0 = 2.9\ eV$.

An example of the band structure is shown in Figure 2.4.

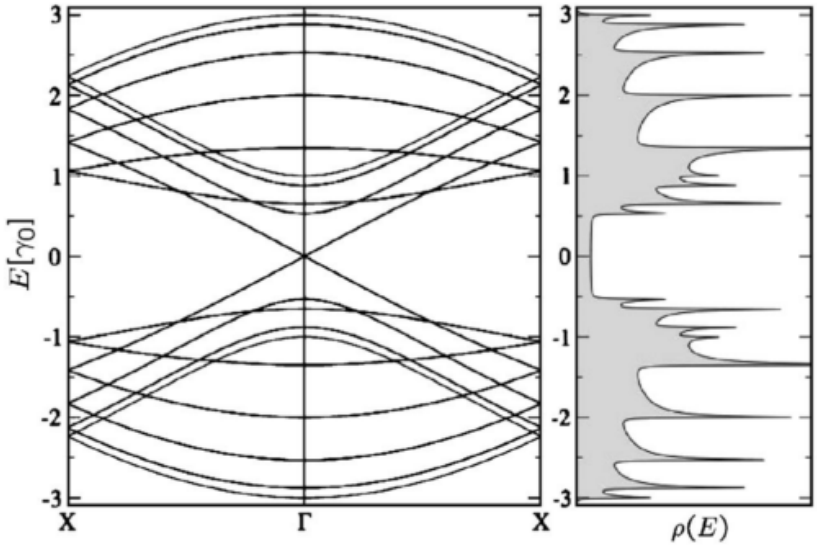

Figure 2.4. Band structure and density of states for a metallic carbon nanotube with chiral vector (9,0).[2]

For semiconducting nanotubes, the boundary condition becomes

$$e^{i\vec{K}\cdot\vec{C}_h} = \pm e^{2i\pi/3}$$

and $\delta\vec{k}$ is

$$\delta\vec{k} = \left(2\pi/\left|\vec{C}_h\right|\right)(q \pm 1/3)\kappa_\perp + k_\parallel\kappa_\parallel,$$

where $\kappa_\perp$ and $\kappa_\parallel$ are the basis vectors along $\left|\vec{C}_h\right|$ and $\vec{T}$, respectively. $\vec{T}$ is the translational vector along the tube axis. Then, the dispersion relation near the Fermi level is

$$E_q^{\pm}(k_\parallel) \simeq \pm\frac{\sqrt{3}a}{2}\gamma_0\sqrt{\left(\frac{2\pi}{\left|\vec{C}_h\right|}\right)^2\left(q \pm \frac{1}{3}\right)^2 + k_\parallel^2},$$

where q is the number of available bands. At $k_\parallel = 0$, there is a gap opening since

$$E^{+}_{q=0}(k_{\parallel}=0) - E^{-}_{q=0}(k_{\parallel}=0) = \frac{2\pi a\gamma_0}{\sqrt{3}\left|\vec{C}_h\right|} = \Delta E^1_g.$$

Plugging the tube diameter $d_t = \frac{|\vec{C}_h|}{\pi}$ and Fermi velocity $v_F = \sqrt{3}a\gamma_0/2\hbar$ into ΔE^1_g, one can write down the relation between band gap and diameter as

$$\Delta E^1_g = \frac{4\hbar v_F}{3d_t}.$$

An example band structure of a semiconducting nanotube is shown in Figure 2.5.

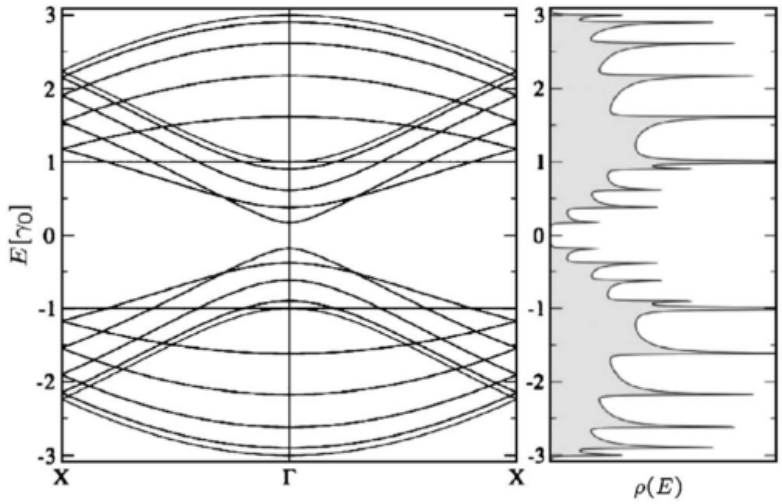

Figure 2.5. Band structure and density of states of a semiconducting carbon nanotube with chiral vector (10,0).[2]

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Chapter 3. Graphene Device Fabrication and Characterization

3.1 Introduction

In this chapter, I will present the fabrication and characterization procedures of graphene devices. Sections 3.2 will describe the graphene sample preparation including mechanical exfoliation and graphene layer identification. Section 3.3 will detail the fabrications for substrate-supported devices, which are used for our study in organometallic hexahapto functionalization of single layer graphene (Chapter 4), and suspended graphene devices that are used for studies in that combines transport with *in situ* strain modulation (Chapter 5), and in graphene-carbon nanotube junctions (Chapter 8). Section 3.4 will describe three transfer-techniques – wet transfer and dry transfer via resists or via van der Waals pick-up – which are used in the study of electrical contact to carbon nanotube devices encapsulated in hexagonal boron nitride (Chapter 7) and Chapter 8. Section 3.5 will illustrate our device characterization methods and setups.

3.2 Graphene Flake Preparation

Graphene flakes are mechanically exfoliated from a piece of Kish using scotch tape.[1] Specifically, a small piece of graphite with size about 1 mm^3 is placed on the adhesive side of a piece of tape, which is then repeatedly folded and unfolded until small graphite pieces are uniformly distributed over the tape. Clean silicon substrates with 300 nm SiO_2 are prepared by sonicating in acetone for 15 minutes to remove any contamination, rinsing with isopropyl alcohol (IPA) and blow-drying with nitrogen. To deposit the graphene flakes, we press the adhesive side of the tape onto a SiO_2 / Si chip and gently scratch the back of the tape. Graphene flakes, often together with tape residues, are thus deposited on the chip. The tape residues can later be cleaned by acetone and IPA rinse. Further cleaning involves annealing in oxygen ambient at 300 °C for 1 ~ 3 hours, which removes the tape residues, water and other absorbents, and can improve the quality of graphene.

My studies mainly focus on single layer graphene. Graphene sheets are located and their numbers of layers are identified by optical microscopes, as the color contrast is proportional to the number of layers. Using a Visual Basic-based program that I built, the number of layers in a given graphene flake can be readily identified by the relative green channel shift in the optical images. Another important tool of characterization is Raman spectroscopy[2], which is used to determine the stacking order and layer numbers. For instance, the ratio of the intensities of the 2D peak at ~ 2700 cm^{-1} to that of the G peak at ~ 1580 cm^{-1} can be used to determine the number of layers – for single-, bi- and tri-layer

graphene. The ratio is > 2.0, ~ 1.2 and ~ 0.6, respectively. Figure 3.1 shows a typical image of a single layer graphene flake under an optical microscope and the corresponding Raman spectrum.

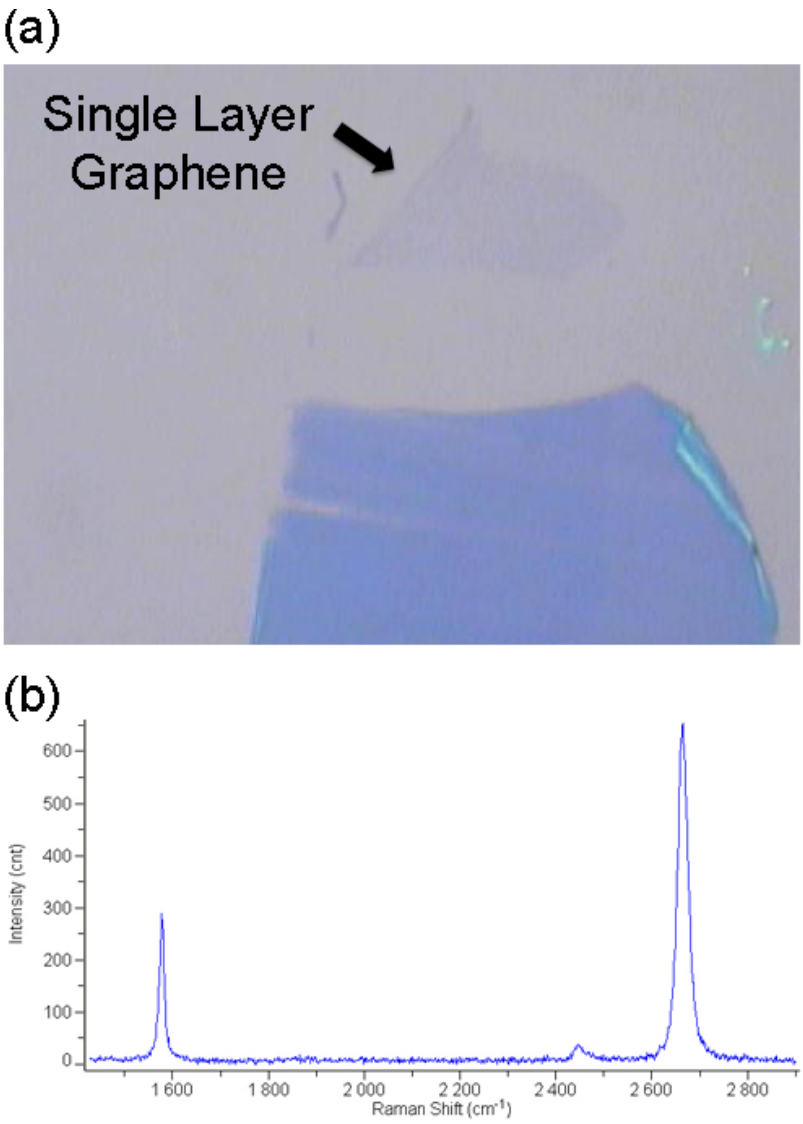

Figure 3.1. (a). Optical image and (b). Raman spectrum of a single layer graphene flake.

3.3 Device Fabrications

3.3.1 Substrate-Supported Devices

Fabrication of substrate-supported graphene devices begins with patterning of alignment marks. After exfoliating graphene flakes on SiO_2 / Si chips (Figure 3.2 (a)), we spin-coat one layer copolymer (MMA (8.5) MAA) (MMA) and one layer Poly(methyl methacrylate) (PMMA) onto the chip at 4000 rpm for 40 seconds; each layer is baked at 180 °C for 10 minutes, resulting in 300 nm- and 200 nm- thick layers, respectively. MMA is used as the bottom layer since it leaves less residue and allows creation of undercut after developing, which will facilitate lift-off. E-beam lithography is used to pattern the alignment marks around the graphene flake, with typical dosage 400 ~ 800 μC / cm^2 at 20 kV (normal resolution) or 30 kV (higher resolution). The chip is then developed in MIBK : IPA (1:3) solution for 60 seconds, followed by IPA rinse. We deposit 10 nm Cr and 50 nm Au using electron beam evaporator; though we find that metal depositon is not always necessary because the alignment marks after developing are often visible in SEM, and the PMMA layer with alignment marks can be directly used for the next lithography step that patterns electrodes. If metal is deposited, PMMA is lifted-off by acetone.

The electrode patterns are designed using DesignCAD. To fabricate the electrodes, another two layers of the resist are spin coated (if metal deposition and lift-off are performed in previous step). We use MMA / PMMA bilayer for devices that require cleaner substrates and two layers of PMMA for high resolution. The chips are exposed to

electron beam of 400 ~ 800 μC / cm^2 dosage at 20 kV or 30 kV (Figure 3.2 (b)), and developed in MIBK : IPA (1 : 3) for 10 ~ 15 seconds and IPA rinse (Figure 3.2 (c)).

Electron beam evaporation at high vacuum < 1 x 10^{-6} Torr is used for depositing metals in the windows on the resist bilayers. For resist that consists of two layers of PMMA, the total thickness of deposited metals should be less than 1 / 3 of the total thickness, since lift-off would be difficult otherwise. For alignment marks and graphene electrodes, we deposit 10 nm Cr / 50 nm Au or 10 nm Ti / 50 nm (Figure 3.2 (d)). Cr (or Ti) functions as an adhesion layer and also provides a better match to graphene's work function. After metal evaporation, the chips are lifted-off in acetone at 80 °C for at least 20 minutes (Figure 3.2 (e)).

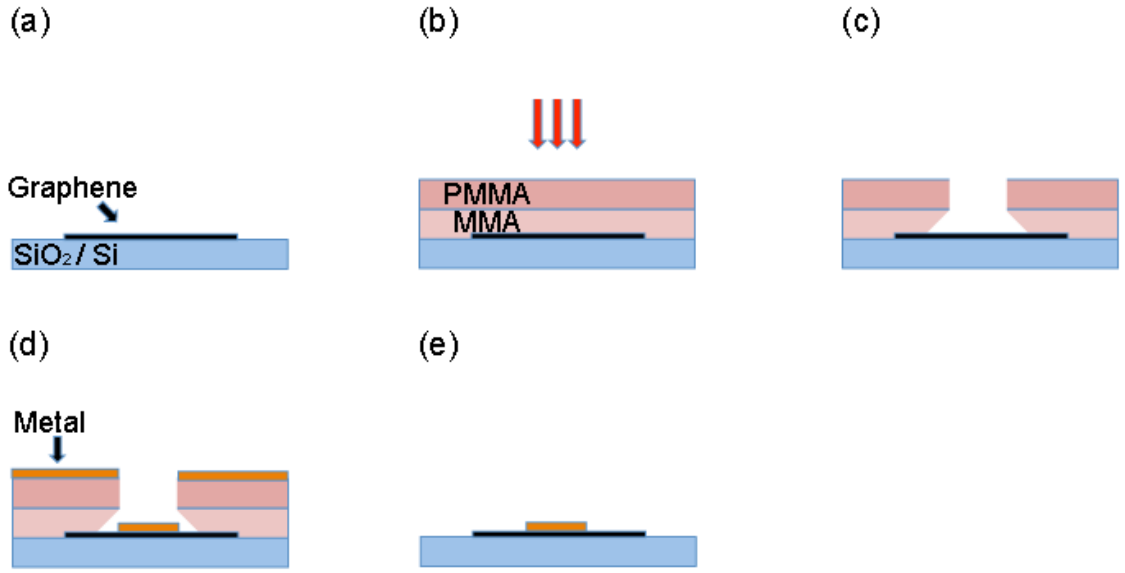

Figure 3.2. Fabrication of substrate-supported device. (a). Exfoliated graphene onto SiO_2 substrate. (b). E-beam lithography on MMA / PMMA resist bilayer to define patterns. (c). Developing patterns in MIBK : IPA (1 : 3). (d). Metal deposition. (e). Completed device after lift-off.

3.3.2 Suspended Devices

Suspending graphene or SWNTs can yield extremely high mobility samples, since the substrate is often the mobility bottleneck due to the presence of trapped charges, corrugations and other scatterers.[3, 4] The fabrication process is similar to that of substrate-supported devices, albeit with two crucial differences: (1). the acid that is used to release graphene from the underlying SiO_2 substrate also etches Ti and Al, thus constraining materials that can be used as electrodes; here we use 10 nm Cr / 150 nm Au; (2). to avoid

collapsing, the device must be sufficiently small – suspended graphene devices are mostly limited to width ~ 1 μm and channel length ~ 1.3 μm (Figure 3.3 (a)).

To suspend the device, a completed substrate-supported device is submerged in buffered oxide etchant (BOE) at room temperature for 90 seconds. The etching rate is about 2.2 nm/s, so about 200 nm of SiO_2 is etched. The device is submerged in DI water multiple times to dilute the BOE, then in IPA. It is important that the device is kept wet during the entire process, so as to avoid collapse of the suspended structures by the surface tension of the drying liquids.

The devices can be dried via two different methods. The first method is by heating the chip in a hot IPA solution at 80 °C, then placing the wet chip on a clean glass slide at 70 °C. This method is simple, but less reliable than the second method of using a critical point drier (CPD), in which IPA is replaced with liquid CO_2, and the chip is dried at the critical point that completely eliminates surface tension (Figure 3.3 (b)).

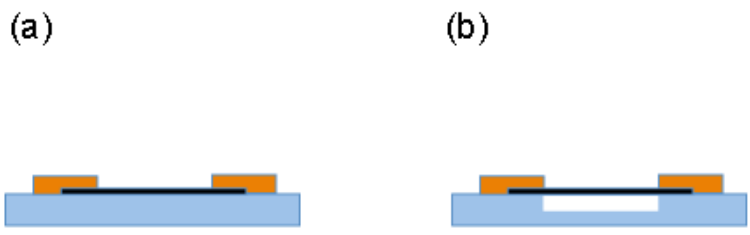

Figure 3.3. Fabrication of suspended device. (a). before BOE etching. (b). after BOE etching.

3.4 Graphene Transfer

Nowadays, transfer technique is very essential since it allows researchers to access interactions among different two-dimensional materials.[5] For instance, graphene is transferred onto hexagonal boron nitride (hBN) sheets, which have been demonstrated to not only dramatically improve graphene's mobility[6] but also give rise to the fractal spectrum of Hofstadter butterfly[7–9]. Generally, transfer techniques can be categorized into dry and wet transfers. In the following, I will describe our procedures for transferring graphene flakes onto hBN flakes, using both methods.

3.4.1 Wet Transfer

Wet transfer begins with an exfoliated graphene flake on a SiO_2 / Si substrate. Two layers of PMMA are spin-coated onto the substrate and will serve as a carrier. Since PMMA itself is very thin, flexible and difficult to handle, we place "handles" onto the PMMA layer, which consist of pieces of tape with an opening that is centered at the flake. By submerging the whole stack in BOE or NaOH for a day (Figure 3.4 (a)), the SiO_2 layer is etched, releasing the tape / PMMA / graphene stack (Figure 3.4 (b)). The stack is cleaned with DI water and IPA, and attached to a glass slide. It is now ready for transfer.

The hBN flakes that will serve as substrates are also mechanically exfoliated on a SiO_2 / Si substrate. We usually use hBN with thickness about 30 nm or less. Our homemade transfer stage allows high accuracy transfer with 600x magnification. After

aligning the graphene flake with the target hBN flake (Figure 3.4 (c)), we heat the stage to 90 °C or higher to melt the PMMA layer, and then remove the glass slide. The PMMA and graphene will stay on the target substrate (Figure 3.4 (d)). PMMA is removed in acetone at 80 °C for 20 minutes (Figure 3.4 (e)). Annealing in O_2 at 300 °C can further remove the PMMA residue or other contaminants.

The wet transfer process is quite robust and relatively straightforward. However, it still leaves contaminants, folds and bubbles in graphene, which are less desirable. In the next section, I will describe the dry transfer technique, which leaves much less contaminants and enables much higher quality devices.

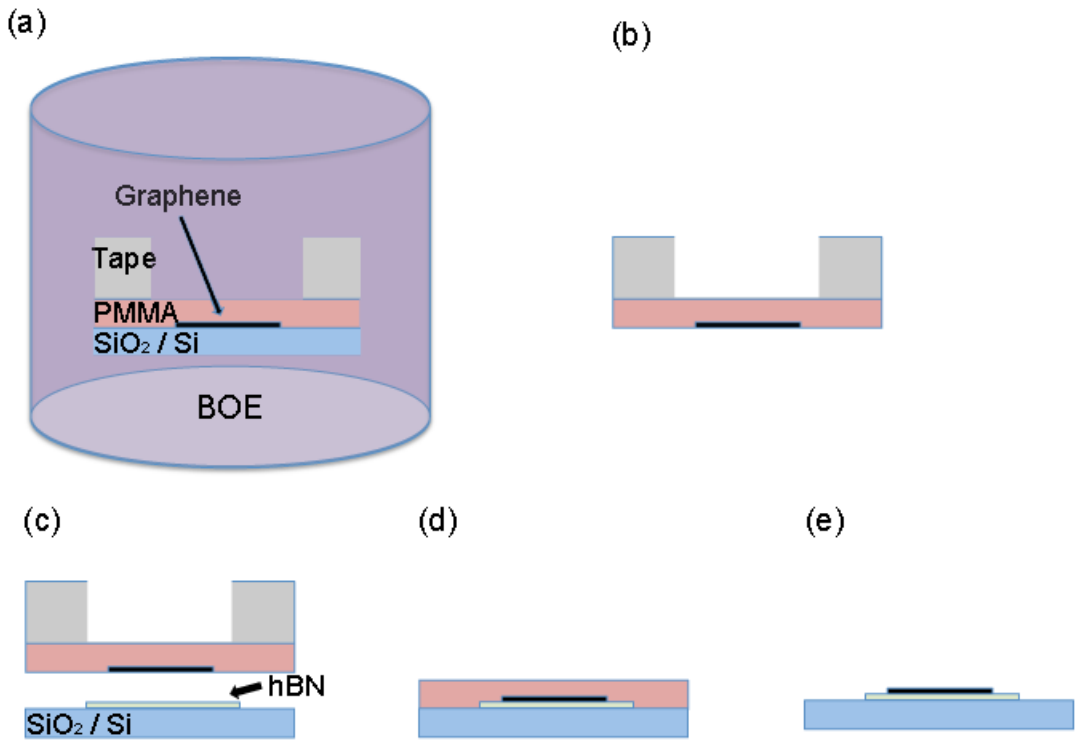

Figure 3.4. Wet transfer process. (a). BOE removes the SiO_2 layer. (b). The tape / PMMA / graphene stack is released from SiO_2 substrate. (c). Graphene flake is aligned with hBN flake during transfer. (d). After transfer, the tape is separated. (e). After cleaning PMMA, graphene is transferred onto hBN.

3.4.2 Dry Transfer via Resists

This technique is developed based on a previous study.[10] It starts with preparing transfer carriers, which is a stack consisting of top to bottom, PMMA, LOR (MicroChem LOR3B), tape and glass slide. First we place a piece of tape on a glass slide (adhesive

side down), and the tape will act as backing for the rest of the stack. A layer of LOR is spin-coated on the tape at 1000 rpm for 40 seconds; this layer facilitates tape removal in a later step. Without further drying the LOR, a layer of PMMA is spin-coated at 3000 rpm for 40 seconds. We let the resist dried naturally and exfoliate graphene flakes on the PMMA layer (Figure 3.5 (a)), which are located using optical microscope. A transfer stage is used to align the graphene flake with the hBN flake (Figure 3.5 (b)) and brought them into contact (Figure 3.5 (c)). By heating up the stage to 90 °C, the PMMA layer will melt and attach to the target substrate. We now have a stack of substrate / hBN / graphene / PMMA / LOR / glass slide (top to bottom), which is placed on a hot plate at 160 °C for a few seconds (Figure 3.5 (d)). The tape will shrink and delaminate. The LOR and PMMA layers are removed by MF319 and acetone, respectively (Figure 3.5 (e)), leaving the hBN / graphene stack on the target substrate. Further cleaning can be performed in O_2 environment at 300 °C.

The advantages of this technique are its stability and high yield. However, due to the low color contrast, it is difficult to locate single layer graphene sheets on PMMA / LOR layers. Also, one side of the graphene flake is contaminated by the PMMA.

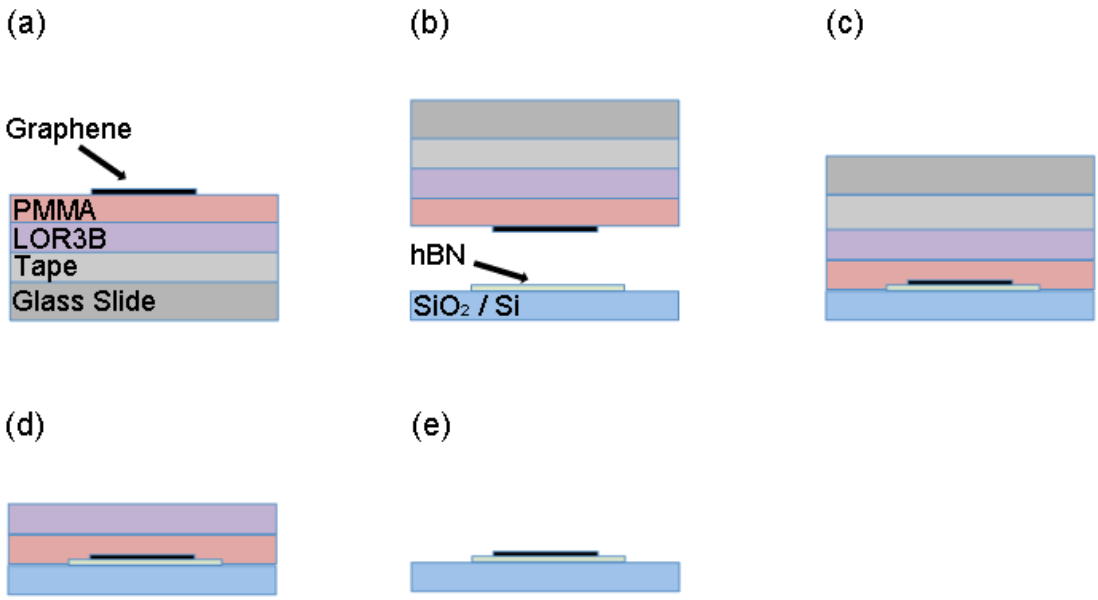

Figure 3.5. Dry transfer process via resists. (a). Graphene is exfoliated on the dry transfer carrier. (b). Graphene is aligned with hBN. (c). Graphene is brought into contact with hBN. (d). By heating the stack at 160 °C, the tape is removed. (e). Cleaning in MF319 and acetone removes the LOR and PMMA layers, respectively.

3.4.3 Dry Transfer via van der Waals Pick-up

The technique, recently developed by L. Wang et al.[11], enables fabrication of ultraclean graphene / hBN devices. Briefly, taking advantage of the strong van der Waals force between two atomic layers, an hBN flake is used to directly pick up a graphene flake. The process can repeat several times to create hBN / graphene / hBN heterostructures. Since the interfaces are never exposed to any chemical or resists, ultra-

high quality devices can be fabricated. Another innovation is that by using etching to expose the graphene edges and depositing metals, 1D contacts can be made to the stack.

The process begins with preparing polypropylene carbonate (PPC) solution by dissolving PPC particles in anisole and stirring the solution at 80 °C until the solution is clear (about 1 day). The concentration of the solution is ~ 30 wt.%. The solution can be reused for about 1 month before it loses the ability to pick up flakes.

The carrier is a stack of glass slide / Polydimethylsiloxane (PDMS) / PPC. We tape the edges of the PDMS to the glass slide, then spin-coat the PPC on the stack at 8000 rpm for 60 seconds and baked the stack at 180 °C for 2 minutes. The stack is then ready to pick up flakes.

We exfoliate the hBN flakes on SiO_2 substrates. After choosing a large and flat hBN flake with thickness about 30 nm, the homemade transfer stage is used to bring the glass slide / PDMS / PPC stack and the hBN flake into contact (Figure 3.6 (a)). By heating up the substrate to 60 °C and then naturally cooling it down to 40 ~ 43 °C, it should allow the PPC to completely cover the hBN flake. By separating the glass slide and the substrate, the hBN flake is then picked up.

The graphene flake can be picked up by the hBN flake due to the strong van der Waals force between them. We use the transfer stage to align the two flakes and bring them into contact (Figure 3.6 (b)). By heating up the substrate to 60 °C and cooling it to 40 ~ 43 °C, the graphene flake can be picked up after separating the glass slide and the substrate.

Finally, by depositing the hBN / graphene stack on an hBN flake (Figure 3.6 (c)) and heating up the substrate to 80 °C ~ 90 °C, the PPC film melts and detaches from the PDMS (Figure 3.6 (d)). We clean the PPC layer in chloroform for 10 minutes and rinse it by acetone and IPA (Figure 3.6 (e)).

To make electrical contact the graphene, we use e-beam lithography to open windows at the edges of the stack on two layers of PMMA, which act as an etching mask, and etch the stack in reactive ion etcher (RIE) with RF power 60 W and flowing gas SF_6 at 40 sccm and O_2 at 4 sccm. The PMMA layer is removed by immersing the chip in PG Remover for 5 minutes (Figure 3.6 (f)) (acetone is ineffective at removing PMMA that is cross-linked in RIE).

Electrodes are then fabricated by e-beam lithography. Immediately before metal deposition, a gentle O_2 etching at 20 W RF power for 10 seconds with O_2 flow rate 40 sccm is performed to functionalize the edges such that oxygen bridges the carbon and chromium. Subsequently, 10 nm Cr at ~ 0.5 Å/s and 40 nm Au at ~ 1.5 Å/s are deposited in the e-beam evaporator at $< 1 \times 10^{-6}$ Torr. Lastly, the resist layer is removed by PG Remover at 80 °C for at least 20 minutes (Figure 3.6 (g)).

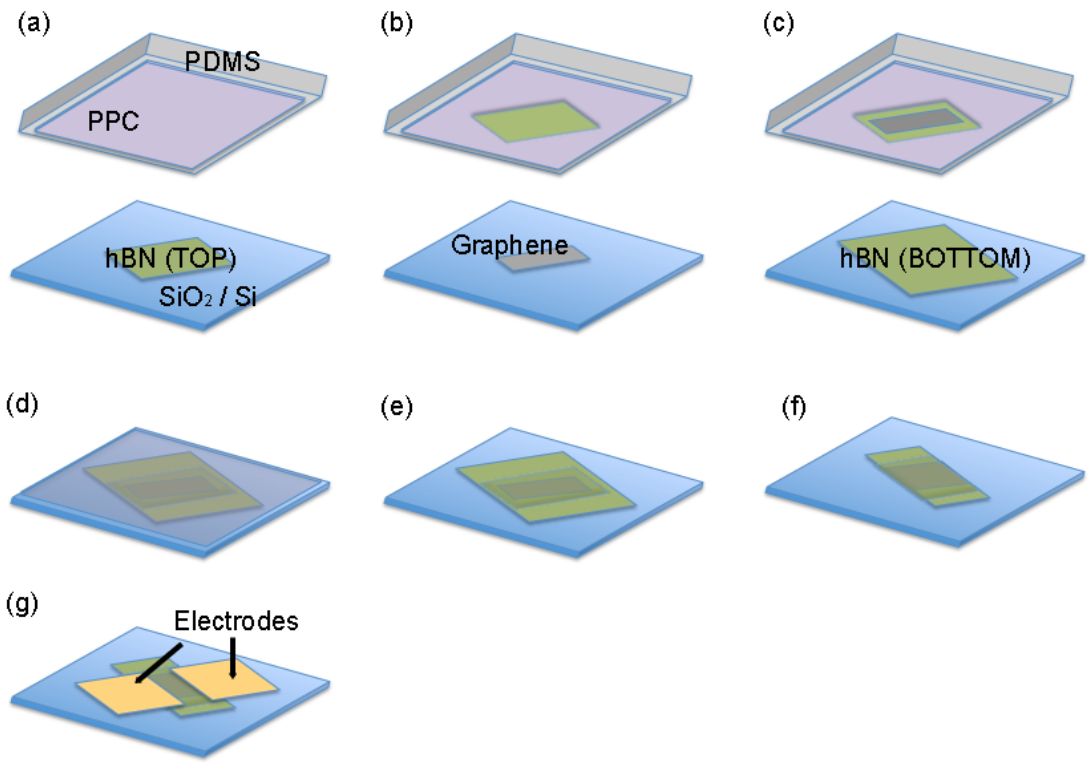

Figure 3.6. Dry transfer process via van der Waals pick-up. (a). hBN is to be picked up by PPC. (b). Graphene is to be picked up by hBN. (c). hBN / graphene is to be stacked on another hBN. (d). After transfer, PDMS is removed. (e). PPC is removed by chloroform. (f). Edges of graphene are exposed by RIE. (g). Metals are deposited at the edges of graphene to make electrical contacts.

3.5 Device Characterization

We mount our finished device in a chip carrier and wire-bond the electrodes to the pins using a West·Bond wedge wire bonder. For room temperature measurements, the device is characterized in our homemade probe station. Low temperature measurements are performed in either the Oxford helium-3 refrigerator or Janis cryostat with a variable temperature insert.

The device is typically characterized using dc (Figure 3.7) or ac lock-in (Figure 3.8) measurements. We use National Instrument (NI) PCI-6251, and NI BNC-2090A to provide DC bias and to acquire data. A lock-in amplifier (Stanford Research SR830) is used to measure the differential conductance dI / dV. The output current from the device is amplified by a current preamplifier (Ithaco model 1211). A source-meter (Keithley 2400) provides the gate voltage. The software used to control the instruments is Mezurit 2, a program developed in Python by Dr. Brian Standley.

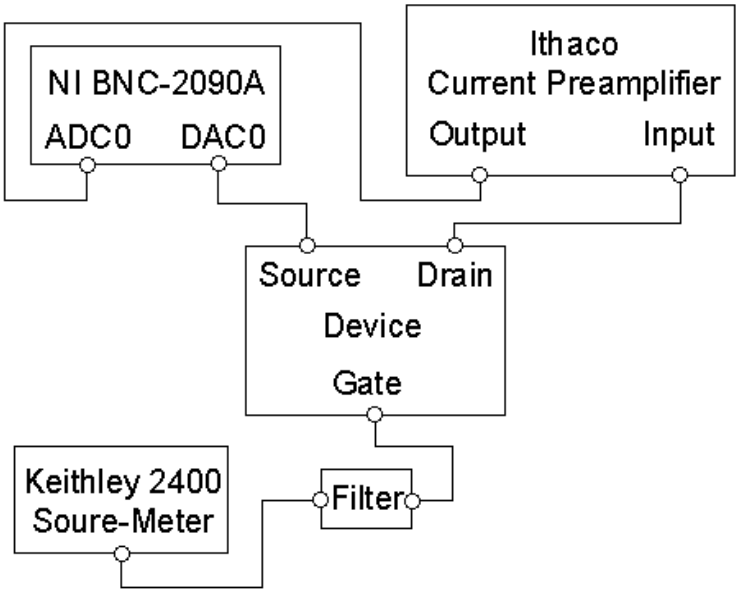

Figure 3.7. DC measurement setup.

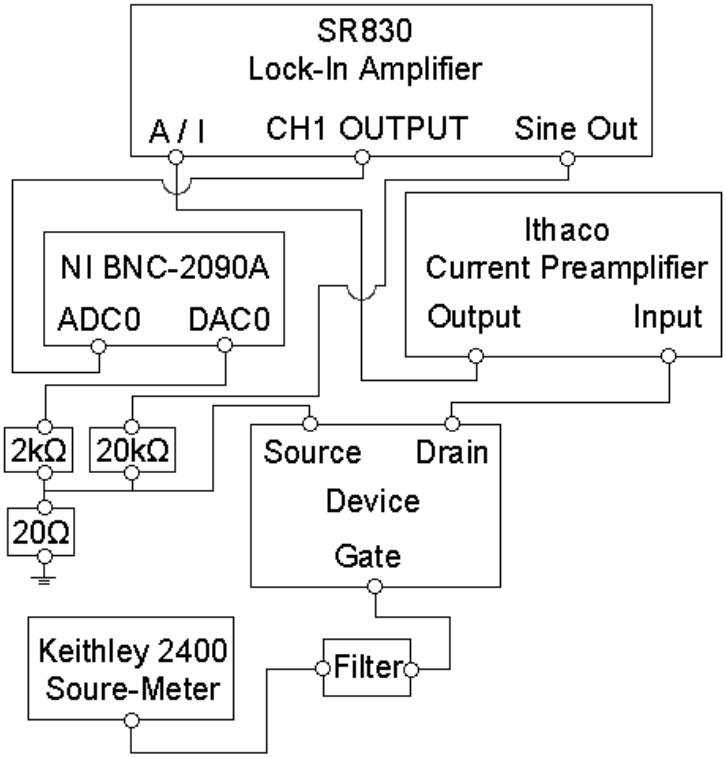

Figure 3.8. Differential conductance measurement setup.

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Chapter 4. Organometallic Hexahapto Functionalization of Single Layer Graphene Devices

4.1 Introduction

The extremely high carrier mobility of graphene has shown itself as a promising candidate for next generation electronics. At room temperature, typically, the mobility in SiO_2 / Si substrate-supported graphene devices can reach 4,000 – 20,000 cm^2/Vs. When suspended, graphene mobility reaches 500,000 – 1,000,000 cm^2/Vs.[1–3] However, its applications are limited since pristine graphene does not have a band gap. Much effort has been devoted to band gap engineering in graphene. One effective approach is by (partially) saturating the valences of some conjugated carbon atoms.[4–19] It has been shown that nitrophenyl functionalization can modify both electronic and magnetic structure of graphene by introducing a fully rehybridized sp^3 carbon atom in the lattice, though this functionalization route and can significantly reduces the field effect mobility.[20–24] We consider this as a destructive rehybridization[25] since this type of functionalization creates resonant scatterers.[26]

Most of chemical modifications of graphene are done by replacing the conjugated sp^2 carbon atoms with sp^3 carbon centers in the graphene lattice. Our collaborator's recent study in the covalent hexahapto modification of graphitic surfaces with zero-valent transition metals such as chromium[14, 27] has proposed a method by applying

organometallic chemistry and forming the hexahapto (η^6)-arene-metal bond in graphene, which leads to very little structural reorganization of the π-system. In the reaction of the zero-valent chromium metal with graphene, the vacant d_π orbital of the metal (chromium) constructively overlaps with the occupied π-orbitals of graphene. This process is gentle and does not remove any of the sp^2 carbon atoms from conjugation.[14, 27] Previous study has shown that the formation of such bis-hexahapto transition metal bonds between the conjugated surfaces of the benzenoid ring systems present in the surfaces of graphene and carbon nanotubes can dramatically change their electrical properties.[14, 25, 27–29] These prior works focus on using the bis-hexahapto-metal bond as an interconnection for electrical transport between the conjugated surfaces. Thus, it increases the dimensionality of the carbon nanotube and graphene materials and leads to the concern with the use of the bis-hexahapto-metal bond as a conduit for electron transport between surfaces. In contrast to previous study, the current study is to investigate the effect of the hexahapto-bonded chromium atoms on the electronic properties of graphene itself (within the plane of a single layer), by using mono-hexahapto-metal bonds to the graphene surface.

4.2 Sample Preparation

Single layer graphene (SLG) flakes used in this study were mechanically exfoliated on a Si substrate with 300 nm SiO_2. 10 nm of Cr and 150 nm of Au were deposited on SLG as electrodes defined by e-beam lithography. The devices were then annealed in vacuum by passing a high current through the channel for a short time to remove contaminants from the surface.[30] After initial characterization, the devices are

then immersed in a chromium hexacarbonyl solution for organometallic functionalization. The hexahapto metal complexations reactions were performed at elevated temperatures under argon atmosphere using the following three different methods as shown in Figure 4.1.

Method A: SLG devices were immersed in a chromium hexacarbonyl [$Cr(CO)_6$, 0.1 M] solution in dibutyl ether/tetrahydrofuran (THF) (5:1) and refluxed under argon atmosphere at 140 °C for 48 hours. After functionalization, the graphene devices were rinsed carefully with THF.

Method B: SLG devices were immersed in a solution of $Cr(CO)_6$ (as in Method A), with the addition of 0.25 equivalents of naphthalene ligand and heated to 80 °C for 12 hours. The naphthalene was added in order to form the labile complex (naphthalene) $Cr(CO)_3$ complex (resulting from the haptotropic slippage of the naphthalene ligand from η^6- to η^4- or η^2-coordination) in-situ, which is known to be a very effective reagent for the transfer of the - $Cr(CO)_3$ group between ligands. We know that there is a facile arene exchange reaction between naphthalene and the more reactive graphene layer, which allows the reaction to proceed at relatively low temperature.

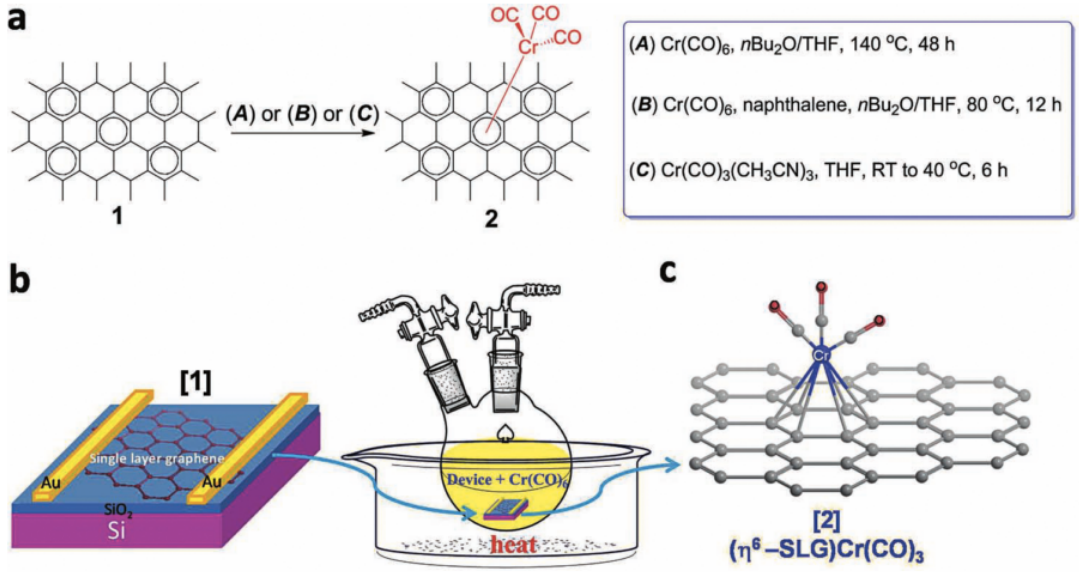

Figure 4.1. Organometallic functionalization of single-layer graphene devices. (a). Schematics of functionalization approaches using three different reaction routes to obtain hexahapto-chromium complex, (η^6-SLG)$Cr(CO)_3$; Method A: $Cr(CO)_6$, n-Bu_2O/THF, 140 °C, 48 h, under argon, Method B: $Cr(CO)_6$, naphthalene, n-Bu_2O/THF, 80 °C, 12 h, under argon, and Method C: $Cr(CO)_3(CH_3CN)_3$, THF, room temperature to 40 °C, 6 h, under argon. (b). Illustration of the graphene device and the functionalization process; and (c). Three-dimensional model of the (η_6-SLG)$Cr(CO)_3$ organometallic complex.

Method C: SLG devices were immersed in a solution of tris(acetonitrile)tricarbonylchromium(0) $[Cr(CO)_3(CH_3CN)_3]$[31–34] in THF (~ 0.1 M) inside a glove-box. The reaction vessel was closed with rubber septum to maintain the argon atmosphere and contained the graphene device and the solution. They were

removed from the glove box, connected to an argon line and heated slowly from room temperature to 40 °C for 6 hours. In order to avoid doping the graphene, this procedure required rigorous exclusion of the atmosphere as a result of the decomposition of the chromium reagent to chromium oxide.

4.3 Characterization

The devices were characterized in a custom-built helium cryostat. All the measurements were performed in a high vacuum environment. The temperature of the devices was measured with a semiconductor thermometer mounted close to the graphene devices. Data were acquired by National Instrument PCI-6251 card controlled by LabWindows / CVI.

To probe the effectiveness of different functionalization methods, Raman spectroscopy was employed to characterize the graphene sheets before and after the reaction (λ_{ex} = 532 nm, Nicolet Almega XR). In the Raman spectra, pristine single layer graphene has two characteristic bands, G-band (1585 cm^{-1}) and 2D-band (2680 cm^{-1}), as shown in Figure 4.2 (a)(i).

After the organometallic covalent hexahapto (η^6-) functionalization, the intensity of the D-band located at ~ 1345 cm^{-1} increases (Figure 4.2 (a)(ii)-(iv)). The Raman spectra showed that all three methods were effective in the formation of Cr-complexed graphene, although Method C was found to provide functionalized graphene flakes with slightly weaker D-band intensity, which may be due to a lower degree of hexahapto (η^6-) complexation. We also observed the reactivity of the flakes towards hexahapto

organometallic functionalization reaction and found that the reaction depended on the number of graphene layers; analysis of the integrated I_D / I_G ratios indicated that single-layer graphene (SLG) was more reactive than few-layer graphene (FLG) and HOPG was least reactive.

We performed transport measurements before and after functionalization of the devices in order to understand the effect of the hexahapto (η^6-) covalent binding of chromium atoms [-$Cr(CO)_3$ moieties] on the electronic properties of graphene. The (η^6-SLG)$Cr(CO)_3$ devices were first characterized without annealing since the Cr-graphene product can decompose at elevated temperatures.[14, 27] More than 10 devices were studied; in the following, results on two devices prepared with Method A and Method C are discussed here. Based on the Raman spectra (Figure 4.2 (a)) and the transport measurements, the device prepared with Method A appears to have a higher degree of functionalization. The current-voltage (*I-V*) characteristics of the pristine graphene device show linear behavior up to 0.5 V. (Figure 4.3) Figure 4.4 (a) shows the zero-bias conductance (G) as a function of the gate voltage (V_g) of one pristine graphene device. We estimated the room temperature field effect mobility of this device about $\mu \sim 4000$ cm^2/Vs. Both the *I-V* and $G(V_g)$ curves of the pristine graphene device shows weak temperature dependence, in agreement with previous experiments.[23] After functionalizing with chromium (Method A), the transport properties of the device changed significantly: the conductance of the device decreased by 10 times (Figure 4.4 (a) and (b)) and the *I-V* curve became non-linear in the temperature range from 4 K to 300 K, as shown in Figure 4.4 (c) and (d). The estimated field effect mobility of the functionalized device is lowered

to $\mu \sim 200$ cm^2/Vs, while significantly diminished, is higher than previously reported values for functionalized graphene.[5, 23, 35, 36]

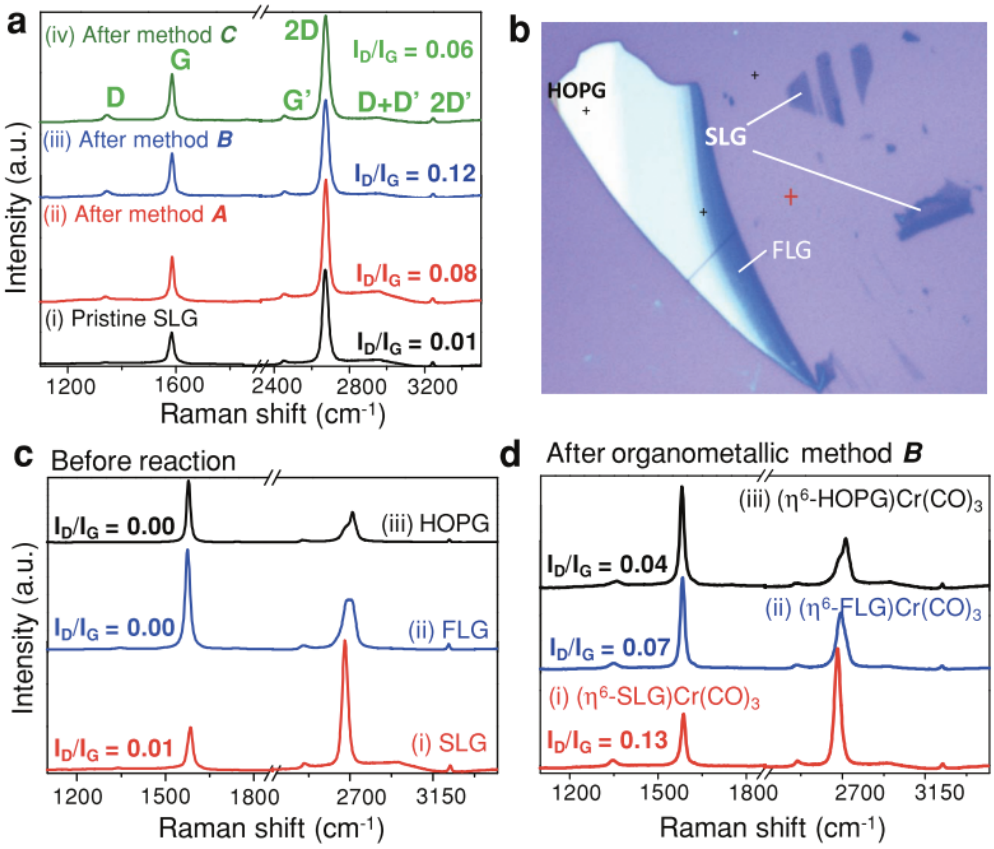

Figure 4.2. Organometallic functionalization of graphene and graphite. (a). Raman spectra of pristine SLG and chromium-functionalized graphene flakes, prepared by Methods A, B and C. (b). Optical image of single-layer graphene (SLG), few layers graphene (FLG) and graphite (HOPG) on SiO_2 / Si substrate. Contrast is enhanced by 30% for clarity. (c). Changes in chemical reactivity with stacking demonstrated by the evolution of Raman spectra before and after functionalization using method B on (i). SLG, (ii). FLG and (iii). HOPG.

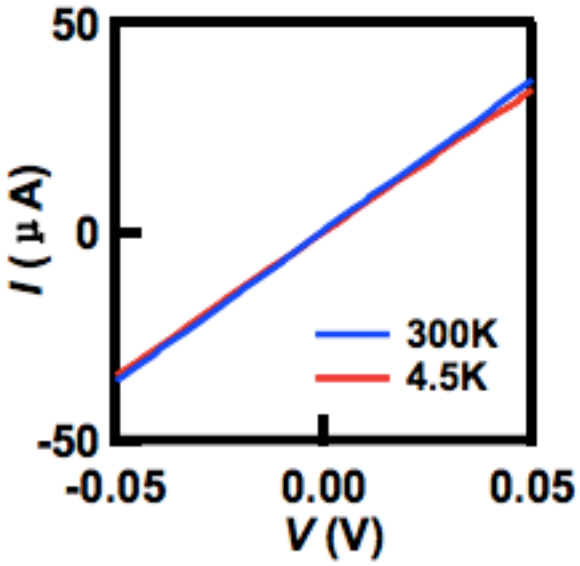

Figure 4.3. *I-V* curves at Dirac point of a pristine graphene device at T = 300 K and 4.5 K.

We also characterized Cr-SLG devices derived by Method C for the purpose to explore the possibility of achieving high-mobility functionalized graphene devices. Typically, (η^6-SLG)$Cr(CO)_3$ devices produced by Method C has a room temperature field effect mobility in the range of ~ 2,000 cm^2/Vs and a current ON / OFF ratio of 5 ~ 13. Figure 4.5 shows the *G(V)* and *I(V)* curves at room temperature and 4.5 K of a weakly functionalized device ((η^6-SLG)$Cr(CO)_3$- Method C).

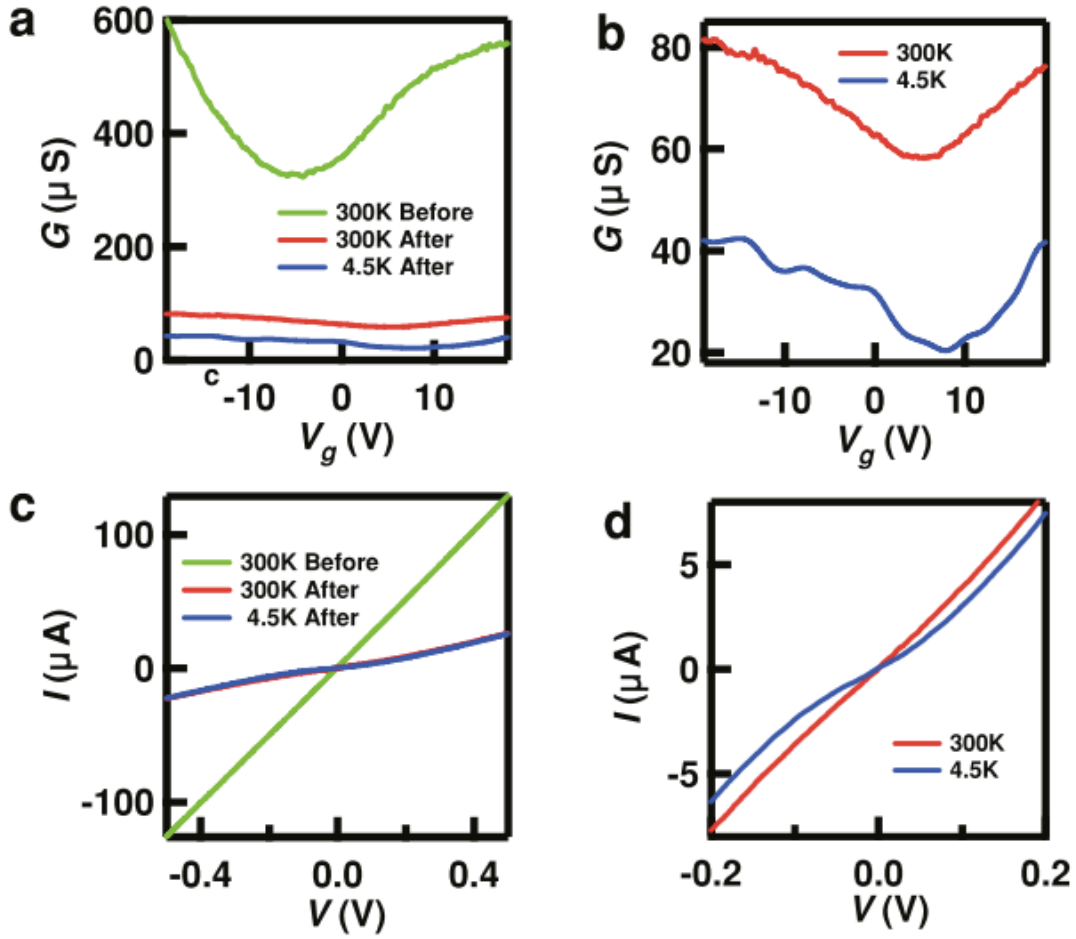

Figure 4.4. (a). $G(V_g)$ characteristic from a device before and after functionalization. (b). $G(V_g)$ characteristic of the functionalized device at 300 K and 4.5 K. (c). $I(V)$ of the device before and after functionalization. (d). $I(V)$ of the functionalized device at 300 K and 4.5 K.

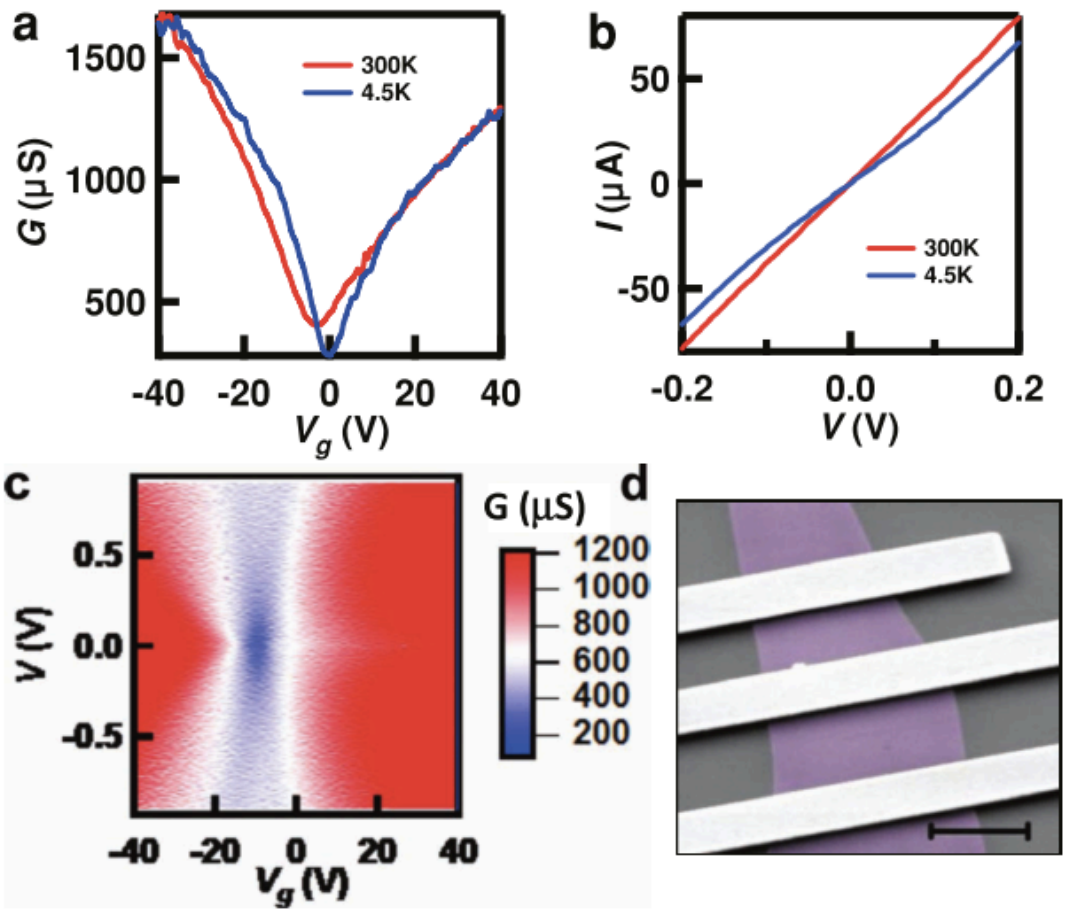

Figure 4.5. (a, b). *G(V)* and *I(V)* characteristics of a weakly functionalized device at 300 K and 4.5 K. The functionalized device has a mobility of ~ 2,000 cm^2/Vs at room temperature and ~ 3,500 cm^2/Vs at 4.5 K. (c). Conductance *G* as a function of bias *V* and gate V_g at 4.5 K of the same device. (d). SEM image of a typical device (scale bar: 2μm).

4.4 Discussion

To determine the transport mechanism of the Cr-functionalized graphene device, we probed the temperature dependence of conductance at the Dirac point and highly doped regimes in the range of 4 K to 300 K. The two most common transport mechanisms in functionalized devices are:

(1) Thermal activation over an energy gap ($2E_A$)[23], in which conductance decreases exponentially with the ratio between the activation energy E_A and thermal energy k_BT,

$$G(T) = G_0 + Aexp(-E_A/k_BT), \quad \text{(Equation 4.1)}$$

where G_0 = the constant background conductance, which is ascribed to the noise floor of the measurement setup, k_B = Boltzmann constant.

(2) Variable range hopping (VRH), which displays a stretched exponential dependence

$$G(T) = Aexp[-(T_0/T)^{\alpha}], \quad \text{(Equation 4.2)}$$

where T_0 is a characteristic temperature and $\alpha \sim 1/2$ to $1/4$ is the exponent.[23]

To analyze the data, we plotted G on a logarithmic scale as a function of T^{-1} and $T^{-1/3}$. The thermally activated regression analysis (Equation 4.1) gives values for the energy gap of $2E_A$ = 3 meV (Dirac point), $2E_A$ = 1 meV [highly doped regime (gate voltage of -42 V)] (Figure 4.6); the largest energy gap that we observed in this study was in a device with a gap of $2E_A$ = 14 meV (Figure 4.7). Thus the consistency of the data indicates the formation of a band gap of $2E_A \approx 10$ meV.[23] The mobility (dynamic nature) of the chromium atoms [-$Cr(CO)_3$ moieties] on the graphene surface might be a possible

complication in analyzing the transport data and can be clearly seen in the data at high temperatures (Figure 4.6). Previous studies of polyaromatic hydrocarbon ligands[37, 38] have demonstrated such fluxional behavior. This may be operative on the two-dimensional surface of the organometallic (η^6-SLG)$Cr(CO)_3$ complexes.[14]

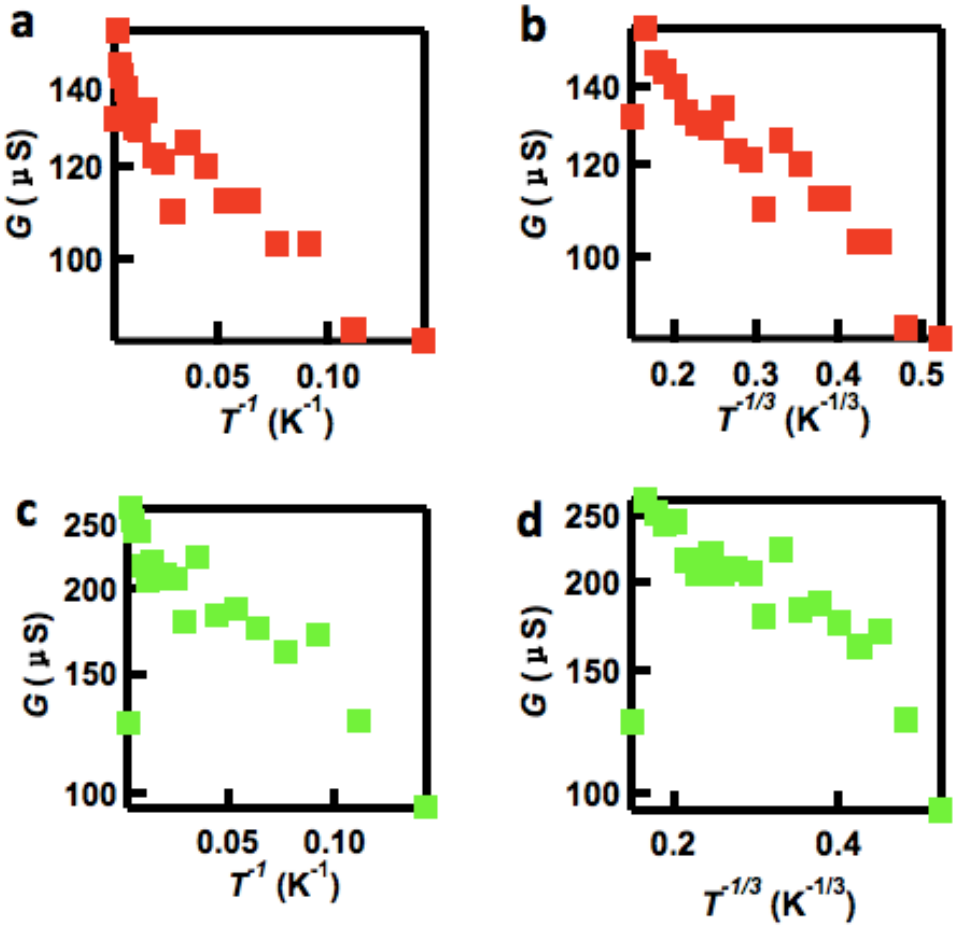

Figure 4.6. (a, b). Zero-bias conductance, G at the Dirac point (at V_g = 0 V) versus T^{-1} and $T^{-1/3}$ for a chromium (Cr) functionalized graphene device. (c, d). Zero-bias conductance, G at a highly doped regime (at V_g = -42 V) versus T^{-1} and $T^{-1/3}$.

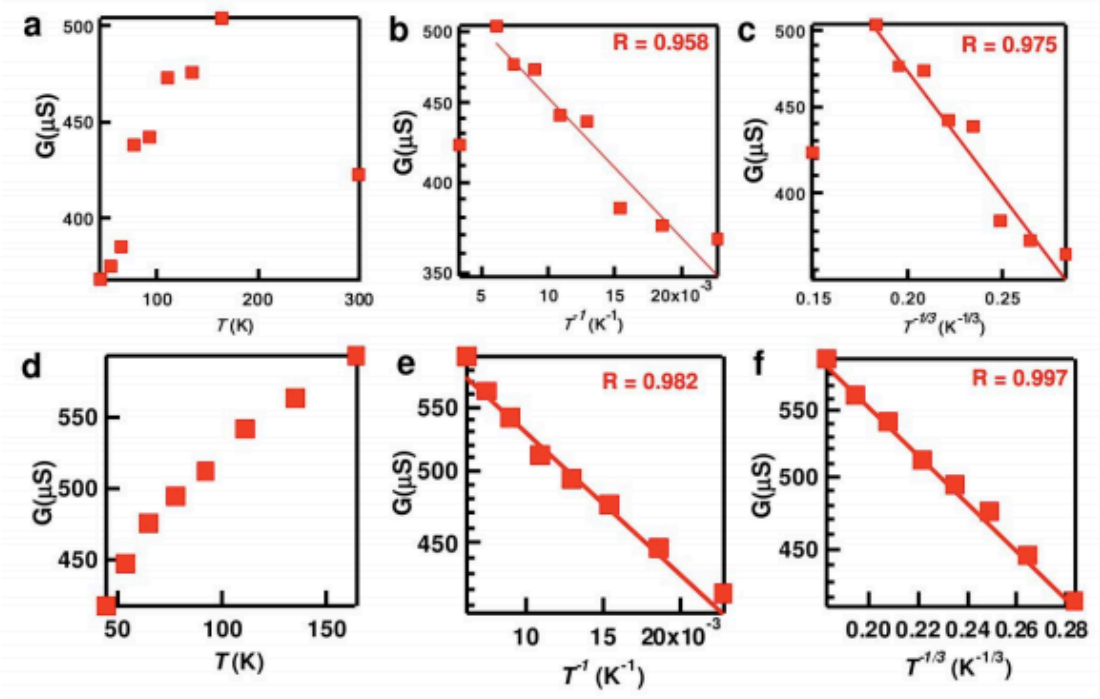

Figure 4.7. (a, b, c). Zero-bias conductance, G at the Dirac point (at V_g = 0 V) vs T, T^{-1} and $T^{-1/3}$ for another chromium (Cr) functionalized graphene device. (d, e, f). Zero-bias conductance, G at a highly doped regime (at V_g = -56 V) vs T, T^{-1} and $T^{-1/3}$.

To estimate the coverage of the -$Cr(CO)_3$ units on the graphene surface, we performed X-ray photoelectron spectroscopy (XPS). Since most of the micro-mechanically exfoliated single-layer graphene (SLG) flakes are very small and the presence of additional graphitic flakes on the silicon substrates is unavoidable, we used CVD-grown SLG (4 mm × 4 mm, on Copper-substrate) for the XPS analysis instead. The SLG samples were functionalized with chromium hexacarbonyl following the procedure

described in Method C. As shown in Figure 4.8, the survey spectrum of the functionalized samples shows the doublet peak corresponding to Cr2p orbitals. The elemental composition was estimated from the areas of the peaks after Shirley background correction and the corresponding sensitivity factors. The analysis gave a C:Cr ratio of about 18:1, which in the ideal case gives a structure such as that illustrated in the inset of Figure 4.8.

Another important characteristic of the chromium functionalization is its reversibility via decomplexation reactions. To achieve decomplexation the functionalized devices, (η^6-SLG)$Cr(CO)_3$ were exposed to an electron-rich ligand, such as anisole (Figure 4.9 (a)). In a typical reaction, the device with an organometallic (η^6-SLG)Cr(CO)3 complex was heated (150 °C) in presence of excess anisole (~ 10 mL) under argon for 12 hours. The device was then rinsed with chloroform, acetone, and hexane and dried under argon.

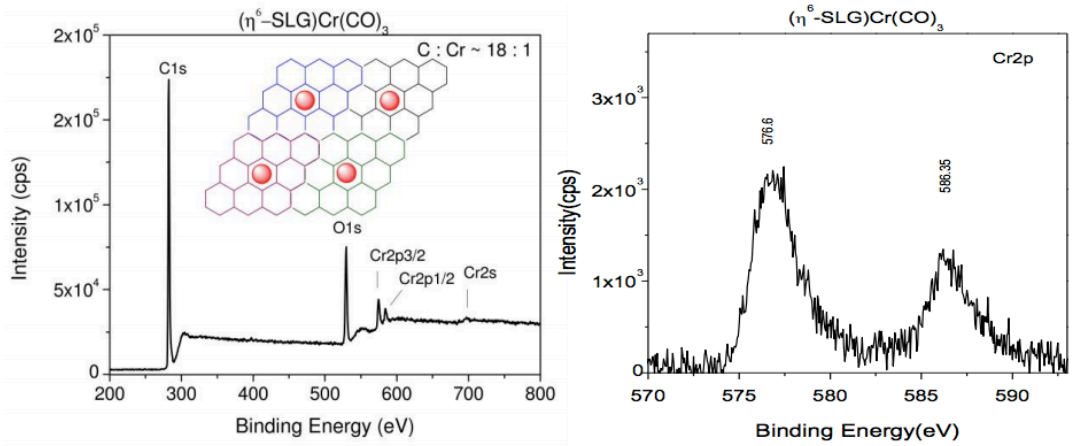

Figure 4.8. (Left). Survey spectrum of CVD-grown single-layer graphene (SLG) functionalized with chromium(0)tricarbonyl moieties. The inset shows the structure corresponding to the C:Cr ratio of 18:1 estimated from the C1s and Cr2p peaks, taking into account the sensitivity factors for carbon and chromium; the colored circles represent each of the hexahapto-bonded –Cr(CO)3 moieties over the graphene surface. (Right). High resolution spectrum of Cr2p signals.

Raman spectroscopy analysis was performed after the complexation and decomplexation reactions. As shown in Figure 4.9 (b), the intensity of the D-band was significantly reduced after the decomplexation reaction ($I_D / I_G = 0.03$). The small remaining D-band after the chemical reversal of the complexation reaction is presumably due to the generation of metal clusters or to the oxidation of the metal on the graphene lattice during heating in the organic solvent (tetrahydrofuran).

Mass spectroscopic (ESI-MS) analysis of the concentrated extract, which resulted from the competitive arene exchange reaction between $(\eta^6\text{-SLG})Cr(CO)_3$ and anisole, led

to the identification of a product corresponding to (η^6-anisole)$Cr(CO)_3$, which was detected with m / z = 243.9832. The transport measurements showed that the conductance and mobility of the devices were increased, although a complete recovery of the pristine device performance was not observed.

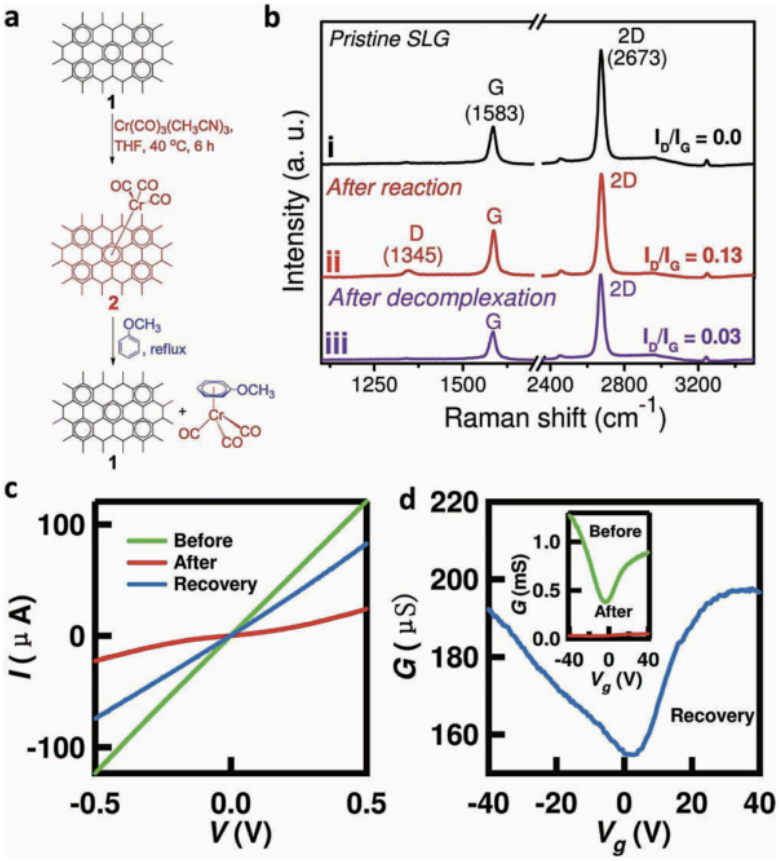

Figure 4.9. Decomplexation of chromium-graphene complexes. (a). Schematics of the complexation of the aromatic rings of graphene with - $Cr(CO)_3$ moieties by use of $Cr(CH_3CN)_3(CO)_3$ reagents (Method C), and decomplexation of the same using electron-rich ligand-anisole, to regenerate a clean graphene and (η^6-anisole)$Cr(CO)_3$. (b). Raman spectra of single layer graphene (SLG)-(i): before reaction, (ii): after reactions with $Cr(CO)_6$, naphthalene, n-Bu_2O/THF, 80 °C, 12 h (Method B), and (iii): after decomplexation. (c). *I(V)* curves and (d), $G(V_g)$ curves of SLG device: pristine device(green), Cr-functionalized graphene device(red), functionalized device after chemical recovery with anisole ligands(blue). The measurements were performed at room temperature.

4.5 Conclusion

In summary, we find that the mono-hexahapto-chromium complexation of single layer graphene allows the fabrication of high performance chemically functionalized devices. We demonstrate that chemically modified graphene devices with a room-temperature field effect mobility in the range of $\mu \sim 200$ - 2,000 cm^2/Vs and an on/off ratio of 5 to 13 can be fabricated via η^6-metal complexation of graphene. Furthermore the graphene organometallic complexation chemistry may be reversed by treatment of the devices with electron rich ligands. These graphene-metal complexes are potential candidates for advanced molecular wires,[39] spintronics devices,[40] and organometallic catalyst supports.[14, 41] The finding that the in-plane transport properties are retained in the presence of mono-hexahapto-coordinated transition metals encourages the pursuit of this mode of bonding in 2-D and 3-D structures, which employ bis-hexahapto-metal complexation.[14, 25, 27–29]

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Chapter 5. Transport in Suspended Monolayer and Bilayer Graphene under Strain

5.1 Introduction

Graphene is a two-dimensional carbon allotrope. Since its first isolation onto insulating substrates[1] and the subsequent development of wafer scale synthesis technology[2–4], graphene has attracted wide attention as a promising candidate for next generation electronics materials[5–13]. As nature's thinnest membrane, graphene's electronic properties are also intimately related to its morphology and/or strain; thus inducing strain may be used to modify the transport properties or band structure of pristine graphene[14–18]. Prior works have demonstrated strain in graphene can be controlled via controlling temperature[17, 19] or chemical modifications[20–23], though *in situ* control of strain was not achieved. In previous study[24], Huang et al. combined transport studies and *in situ* strain control by loading suspended graphene samples with a nano-tip in the chamber of a scanning electron microscope (SEM), though only marginal changes in electrical properties are observed upon application of ~ < 1% strain; moreover, exposure to electron beam irradiation degrades sample quality[25–27]. Thus there is still much to be explored in transport studies on ultra-thin graphene films with *in situ* strain control.

In this letter we present transport measurements of suspended monolayer graphene (MLG) and bilayer graphene (BLG) nanoelectromechanical (NEM) devices, which allows *in situ* modification of strain up to 5%. We study the device behavior before and after repeated straining cycles. For MLG devices, the two-terminal conductance G vs. gate voltage V_g curve becomes smoother, and the minimum conductance shows minimal change (< 1%), in agreement with prior results[25]. For BLG, the minimum conductance decreases by more than 10% and field effect mobility increases. The different behaviors between MLG and BLG devices may arise from the relative shear between the two layers in BLG, or the presence of stacking domains (e.g. AB-BA) whose boundaries are particularly susceptible to strain. Our results underscore the rich interplay between strain and transport offered by suspended devices. Furthermore, these types of NEMS devices are compatible with optical measurements and can be used to study other two-dimensional materials.

5.2 Device Fabrications and Characterization

Graphene sheets were extracted from bulk graphite using standard mechanical exfoliation techniques on top of SiO_2 / Si substrates or a layer of the LOR resist. The number of layers was initially identified via optical microscopy and subsequently confirmed with Raman spectroscopy after completion of transport measurements (Figure 5.1 (a)). To perform transport measurement and *in situ* stretching, we fabricated nano-electromechanical system (NEMS)-based graphene devices, using two different techniques.

In Method A, devices were fabricated with multi-level lithography based on the resists consist of PMMA layer on top of LOR layer. Detailed fabrication process is described in our previous work[28] (Figure 5.1 (b)). Devices thus fabricated have relatively large areas, and graphene are "held" up by electrodes that are suspended above the SiO_2 / Si substrates (Figure 5.1 (c)). The central electrode was designed to be wider and shorter than the neighboring electrodes, so that it can sustain higher actuating voltages.

In Method B, which is used to fabricate the majority of the devices, three Cr / Au (10 nm / 150 nm) electrodes were attached to graphene flakes using standard electron beam lithography (Figure 5.1 (d)). Then the whole device was submerged into buffered oxidant etchant (BOE) solution for 90 – 120 seconds[29, 30]. For each device, the central electrode is designed to be 2 – 3 times wider (800 – 1000 nm wide, 25 – 40 μm long) than the two neighboring electrodes (300 – 400 nm, 20 – 30 μm long). All electrodes are anchored by large contact pads at the ends. By controlling etching time, we can control the extent of SiO_2 etched underneath the electrodes and graphene flake, so that narrower features and graphene flakes are suspended, whereas the wider features (central electrodes and anchors) remain supported by residual of SiO_2 underneath (Figure 5.1 (e)). After etching, the device was transferred into water and isopropyl alcohol (IPA) in succession, in order to rinse and cover the sample with a liquid with lower surface tension. Finally, the device was taken out from hot IPA (to further decrease surface tension of IPA) and placed onto a hot plate at 70 °C. The fabrication process is very robust: despite the fragility of suspended graphene devices, the yield is ~ 90%. Figure 5.1 (f) illustrates the schematics of a typical device with this method.

The devices were placed in a custom-built helium cryostat. All the measurements were performed in a high vacuum environment. The temperature of the devices was measured with a semiconductor thermometer mounted in close proximity to the chip carriers. Data were acquired by National Instrument PCI-6251 card controlled by a C++ based program.

To avoid contamination and damage caused by SEM imaging, all SEM characterizations were done on devices after finishing all the transport measurements or "SEM-imaging-only" devices.

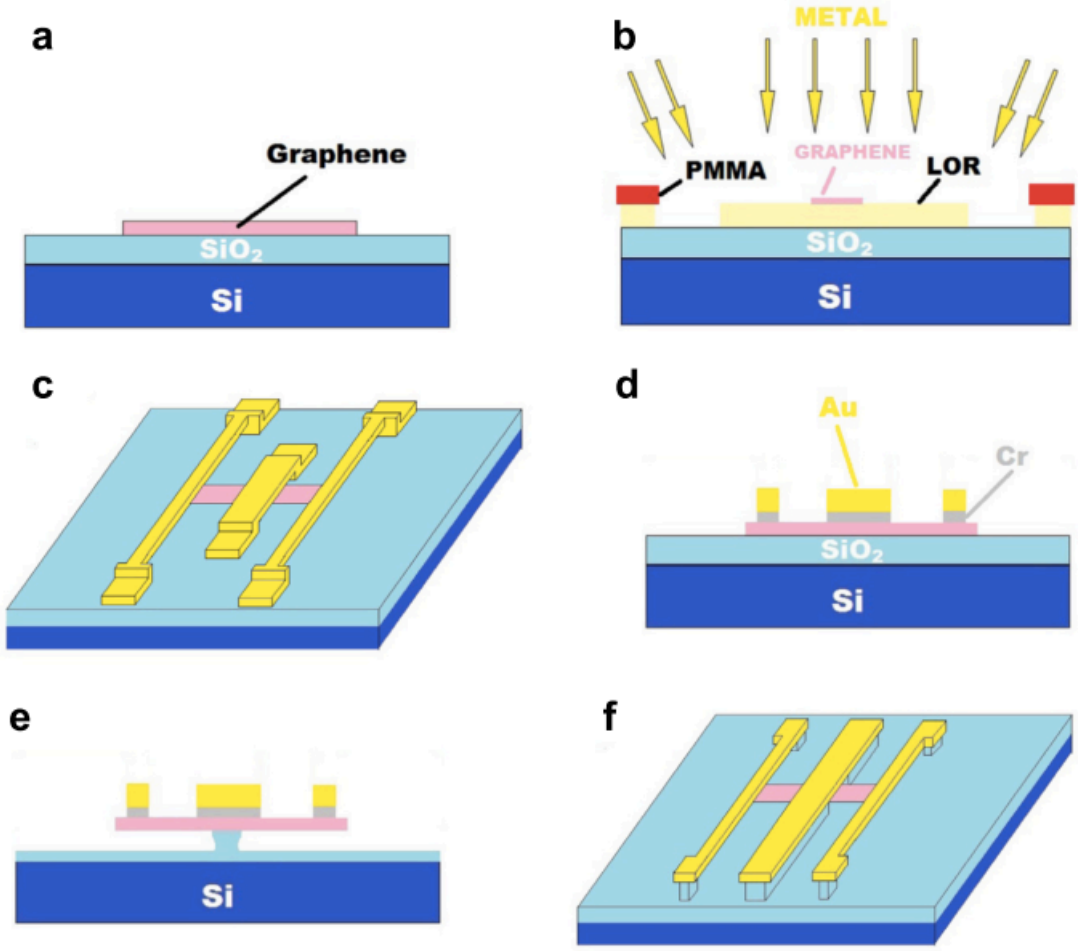

Figure 5.1. (a). Graphene sample exfoliation and identification. (b). Fabrication process using Method A and angled deposition. (c). Three dimensional schematic of a device fabricated with Method A. (d). Fabrication of a device using Method B, which is initially non-suspended. (e). BOE etching selectively removes SiO_2 underneath graphene samples and electrodes. (f). Three dimensional schematic of a device fabricated with Method B.

5.3 Results and Discussion

Figure 5.2 (a) illustrates the general principle of applying *in situ* strain. A suspended electrode and the back gate (Si substrate) form a capacitor. Initially both electrodes and the back gate are grounded, thus they remain parallel, as outlined by solid lines in Figure 5.2 (a). Upon applying the actuating voltage (bias voltage between electrodes and back gate), the electrostatic force induces deflection in the outer suspended or longer electrodes toward the substrate, whereas the central electrode (that is shorter, wider and/or partially supported by the substrate) remain suspended; thus the far ends of the attached graphene sheet move downward accordingly. From the geometry of our device, we can estimate the strain γ exerted on graphene

$$\gamma = \sqrt{1 + \frac{h^2}{L_0^2}} - 1,$$

where h denotes the maximum vertical deflection of the suspended electrode under the electrostatic force, L_0 indicates the initial length of suspended graphene sample. We estimate that at maximum load, up to 5% strain can be induced in the graphene sheets.

Figure 5.2 (b) and (c) show a device fabricated using Method A at gate voltage V_g = 0 and 30 V, respectively. Initially all electrodes and the graphene sheet are well-suspended. When the gate voltage ramps, the narrower electrode on the left slowly deflects downward; at V_g = 30 V, it buckles and collapses to the substrate. This collapse is irreversible even when V_g is reduced to 0. We note that when the measurement is repeated on a control device with the same geometry but without the graphene flake, the suspended electrode collapses at much smaller voltage $V_g \sim 7$ V. Since the electrostatic

force is proportional to V_g^2,we estimate that at V_g =30 V, ~ 95% of the electrostatic force is exerted on the graphene sheet. Figure 5.2 (d) shows another device before and upon applying V_g ~ 100 V. Periodic ripples appears in the graphene sheet afterwards arises from the longitudinal strain induced[17].

For devices fabricated with Method B, the suspended electrodes can reversibly move between parallel and deflected positions. Figure 5.2 (e) shows a device made by Method B before stretching. Figure 5.2 (f) displays SEM image of the same device is stretching a suspended sample under a V_g ~ 50 V. A zooming in image shows one narrower electrode clearly deflected toward the substrate (inset in Figure 5.2 (f)). Figure 5.2 (g) displays the same device when V_g is returned to 0 V, and the suspended electrode returns to its original height. To avoid collapsing the samples, we typically limit the actuating voltage to less than 60 V.

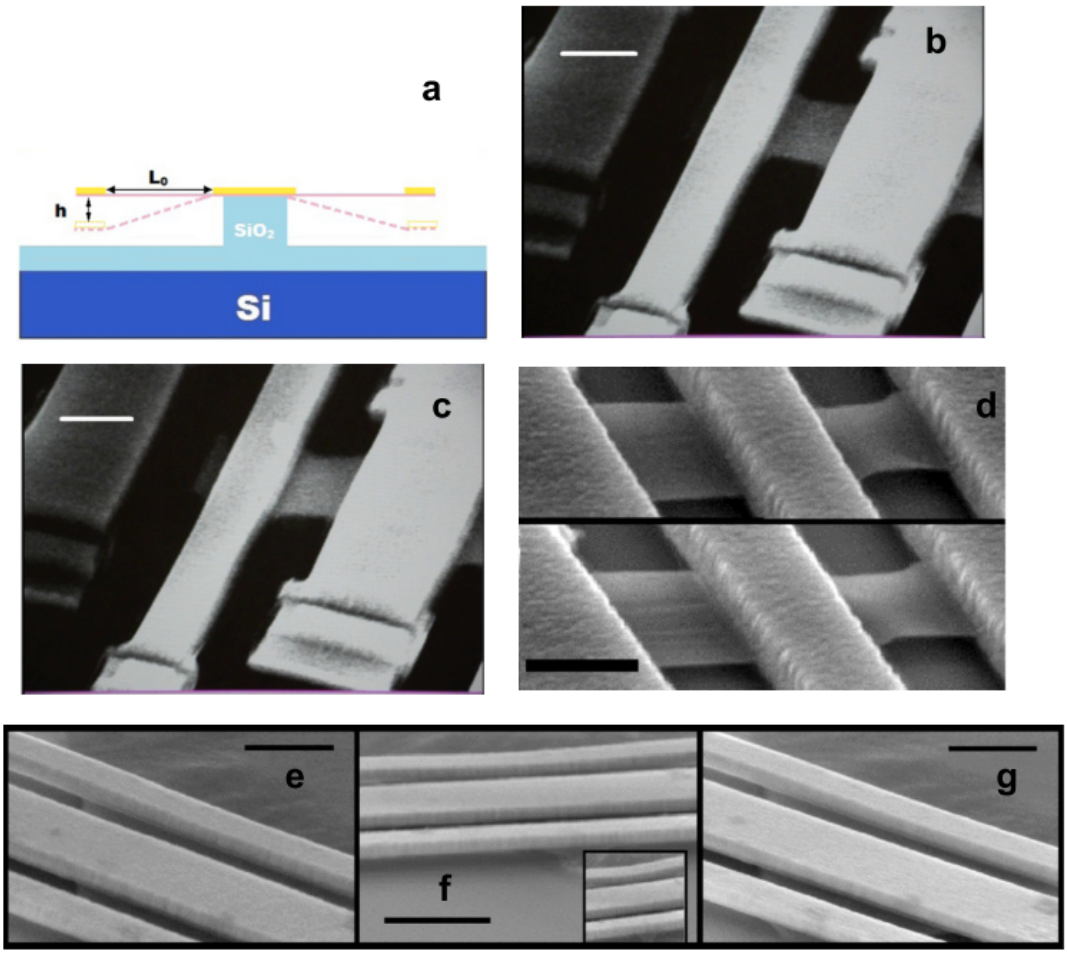

Figure 5.2. (a). Schematic of a device with and without applying the actuating voltage between electrodes and the gate. (b, c). SEM images of a device fabricated with Method A at V_g = 0 V and V_g = 30 V, respectively. Scale bars: 2 μm. (d) SEM images of another graphene sample fabricated before (upper panel) and after stretched (lower panel). Scale bars: 2 μm. (e, f, g). SEM images of a device made by Method B at V_g = 0 V, V_g = 50 V, and when V_g is returned to 0 V. Scale bars: 1 μm (e) and (g), 2 μm (f). The inset in (f) shows a zoom-in image of the deflected region.

To perform transport measurements, the devices are cooled down to 4.2 K in vacuum. Current annealing was applied to remove contaminants on the graphene sheet. The devices are first characterized by measuring its conductance G as a function of V_g;(Figure 5.3 (a) red curve) here V_g is limited to < ±10 V, so that strain is negligible. All devices show repeatable $G(V_g)$ curves over such small V_g range.

After extracting data from its initial state, we start stretching the sample by gradually ramping up actuating voltage to -50 V. Figure 5.3 (b) shows the conductance changes as time elapsed, when the actuating voltage is maintained at 50 V. The conductance fluctuates noticeably and decreased by more than 20 μS(~ 1%). We note that this effect cannot be explained by the changing capacitance between graphene and the gate – at the strained position, the device has stronger coupling to the gate, thus should give rise to a higher conductance value. Thus the modulation in conductance must be induced by movement of the electrode itself, e.g. strain and/or changing the graphene-electrode interface.

The tension in the sample is then released by lowering the actuating voltage back to 0 V, and characterized again by measuring $G(V_g)$ for limited V_g range (Figure 5.3 (a) blue curve). For single layer graphene, minor changes such as slightly improved mobility are observed, but generally the minimum conductivity and the current–voltage (I-V) characteristics (Figure 5.3 (d)) stay relatively constant. After several repeated sweeping cycles (between ±50 V), the gate response became stable (Figure 5.3 (c)) even at large gate voltage.

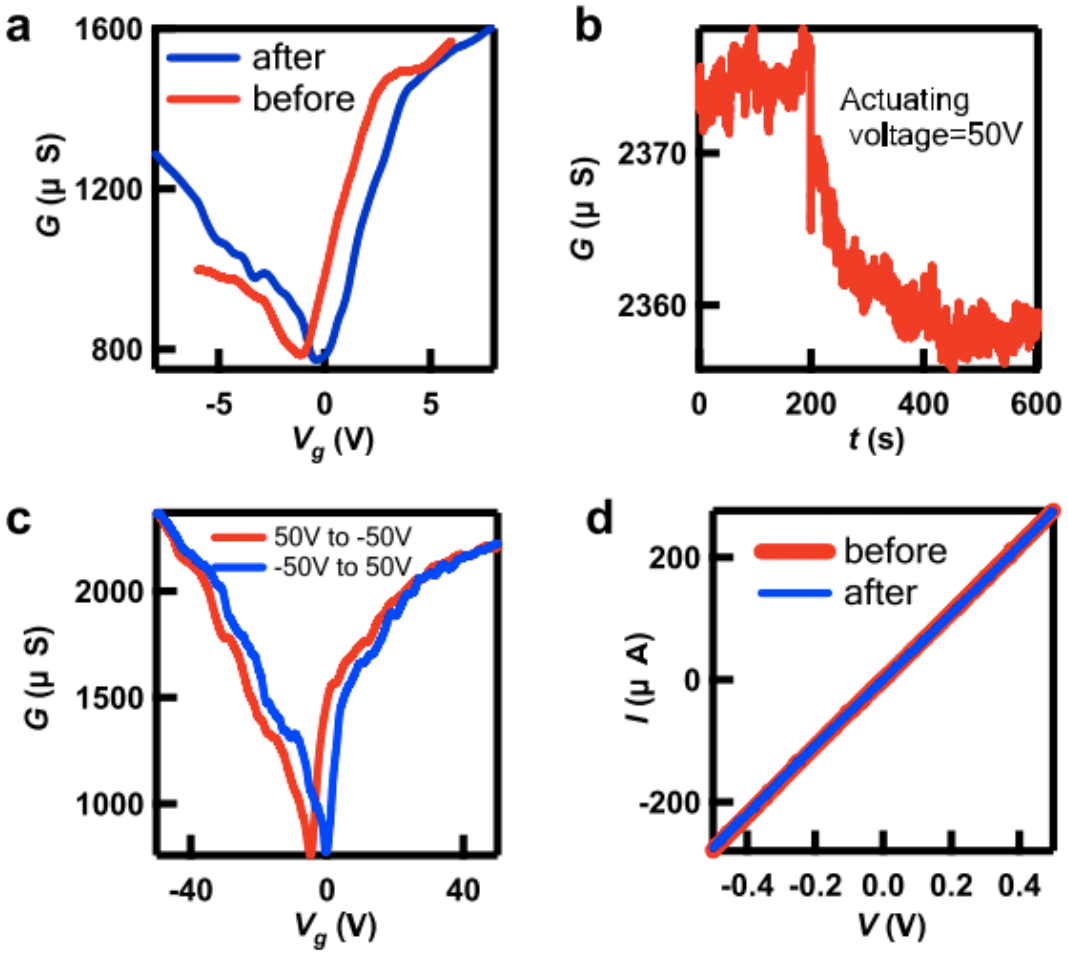

Figure 5.3. (a). Conductance as a function of gate voltage, before (red) and after (blue) stretching process, from a single layer graphene device. (b). Conductance versus time when the actuating voltage was kept at 50 V. (c). Conductance as a function of gate voltage after several stretching cycles. (d). I-V curves of a typical single layer device before and after stretching process.

Compared with single layer samples, bilayer devices be- haves quite differently. Figure 5.4 (a) shows the $G(V_g)$ curves before and after stretching from a typical bilayer devices. After releasing from external strain, the curve becomes steeper and smoother, and the mobility improves. Interestingly, the minimum conductance decreased considerably. This can also been seen in the *I-V* curves, which is more non-linear after stretching (Figure 5.4 (b)). Typically, after stretching process, the conductance of bilayer devices decreases by 10 - 15%. After several stretching cycles several times, the device's $G(V_g)$ becomes stable (Figure 5.4 (c)) with the improved mobility and lower minimum conductance. The device shows no appreciable change in appearance after the stretching cycles (Figure 5.4 (d)).

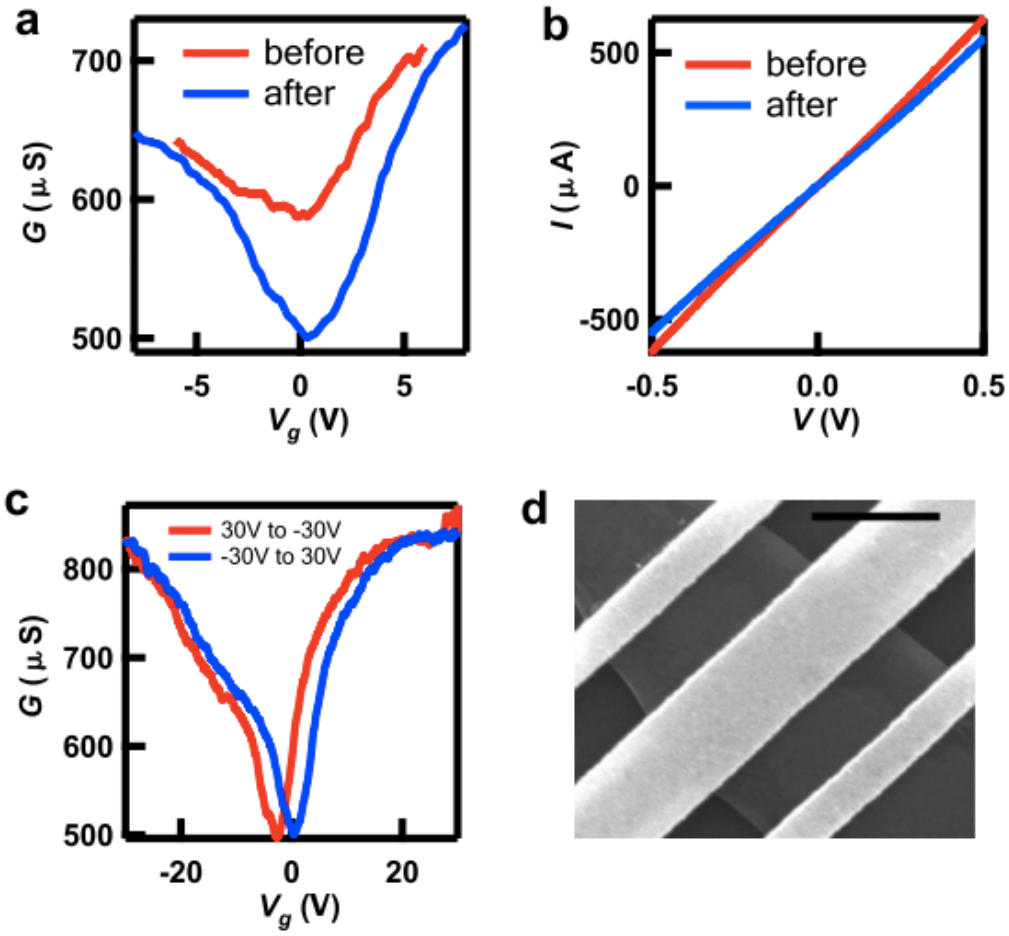

Figure 5.4. (a). Conductance as a function of gate voltage, before (red) and after (blue) stretching process, from a bilayer graphene device. (b). *I-V* curves from one typical bilayer device before and after the stretching process. (c). Conductance as a function of gate after several cycles. (d). SEM image of one bilayer graphene device after stretching. Scale bar: 1 μm.

These intriguing observations suggest the rich interplay between strain and transport offered by suspended devices. The improvement in device mobility likely arises from releasing the strain or ripples that are built-in during the fabrication process. The different behaviors between single layer and bilayer devices are particularly intriguing, e.g. the significant decrease in minimum conductance is unique to bilayer devices. A possible explanation is the improved contact at the electrode-graphene interface; however, one expects that this scenario should occur in single-layer devices as well. We also exclude strain-induced cracks, which should occur at much higher strain[31, 32] and also lead to lower mobility. Our present proposal is that the decrease in minimum conductance may be caused by relative shift and/or shear between two layers induced by the stretching cycles[24, 33, 34], or the presence of AB-BA stacking domains whose boundaries may shift in response to strain[35, 36]. This hypothesis can be verified by low temperature transport measurements, as the modified band structure is expected to lead to reduced density of states and different Landau level spectrum than that of an AB-stacked bilayer graphene.

5.4 Conclusion

In conclusion, we developed two types of NEMS-like devices to stretch suspended single crystal graphene samples and perform in situ measurements. The stretching process can be observed via SEM imaging. Transport property investigation shows that after stretching process, the gate response of conductance from graphene samples improved, and dramatic decrease in minimum conductance is observed in bi-

layer graphene samples. The experimental system and method introduced in this work provides a new approach in strain engineering researches.

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Chapter 6. Fabrication of Carbon Nanotube Devices

6.1 Introduction

In this chapter, I will present the fabrication procedures of carbon nanotube devices. Sections 6.2 will describe the sample preparation including carbon nanotube growth and visualization. Section 6.3 will describe the fabrication process for substrate-supported carbon nanotube devices. The nanotubes are used in two projects – zero-dimensional contacts to carbon nanotube devices encapsulated in hexagonal boron nitride (Chapter 7) and electrical transport in graphene-carbon nanotube junctions (Chapter 8).

6.2 Growing and Locating Carbon Nanotubes

Single-walled carbon nanotubes (SWNTs) are grown by chemical vapor deposition (CVD) method[1], in which iron catalyst decompose methane (CH_4) gas at 900 °C and "assemble" the carbon atoms to form SWNTs. The catalysts are prepared by adding 40 mg of $Fe(NO_3)_3 \cdot 9H_2O$, 2 mg of $MoO_2(acac)_2$ and 30 mg of Alumina nanoparticles in 30 ml of de-ionized (DI) water. The catalyst solution are then stirred for one day at room temperature and diluted by DI water (catalyst solution: DI water = 1:5). We note that it is important to provide a clean environment for SWNT growth. For

instance, all SiO_2 / Si substrates, beakers and furnace tubes are thoroughly cleaned before use.

We control the location of SWNT growth by patterning catalyst islands. The process begins with cleaning SiO_2 / Si substrates by acetone and isopropyl alcohol (IPA), and annealing those substrates in oxygen with a flow rate 0.4 SLM at 500 °C for 2 hours. Two layers of Poly(methyl methacrylate) (PMMA) are then successively spin-coated onto the substrates (Figure 6.1 (a)) at 4000 rpm for 40 seconds. Each layer is baked at 180 °C for 10 minutes. The catalyst islands are defined by e-beam lithography and developed in MIBK : IPA (1 : 3) for 1 minute (Figure 6.1 (b)). After the pattern is developed, 10 nm Cr / 30 nm Au were deposited. (Figure 6.1 (c))

To deposit the catalysts, we put a few drops of the catalyst solution on the substrates, which are heated on a hot plate at 80 °C until all liquids are evaporated so that the catalyst particles adhere to the metal film (Figure 6.1 (d)). Finally, we lift off the PMMA layers (and the catalysts that adhere to them) in acetone at 80 °C for 20 minutes, gently rinse with IPA and blow-dry with nitrogen (Figure 6.1 (e)).

To grow SWNTs, the substrates are first placed in a furnace, which is flushed by Argon (Ar) flowing at 1.0 SLM for 2 minutes. The temperature is then ramped up to 900 °C in 25 minutes with Ar flow rate 0.25 SLM and hydrogen (H_2) flow rate 0.4 SLM. This process causes the reduction of iron compound to form iron particles. When the temperature reached 900 °C, CH_4 with flow rate 0.52 SLM and H_2 with flow rate 0.7 SLM are introduced for 10 minutes, during which SWNTs grow from the iron catalysts. After 10 minutes, we turn off heater and stop the growing process by flowing Ar at 2.0

SLM for two minutes. The furnace is allowed to cool to room temperature with Ar flow rate 0.4 SLM (the cover of the furnace can be opened to speed up cooling when the temperature reaches 600 °C). The substrates are removed from the furnace once the temperature drops below 30 °C (Figure 6.1 (f)). The entire growth process is summarized in the following table (Table 6.1).

	Ar (SLM)	CH_4 (SLM)	H_2 (SLM)	Process
1	1	0	0	Flush quartz tube for 2 minutes.
2	0.25	0	0.4	Heat up to 900 °C in 25 minutes.
3	0	0.52	0.7	Stay 900 °C for 10 minutes.
4	2	0	0	Flush quartz tube for 2 minute.
5	0.4	0	0	Remove substrates at 300 °C.

Table 6.1. Recipe for growing single-wall carbon nanotubes.

SWNTs can be located by scanning electron microscope (SEM), electrostatic force microscopy (EFM) or atomic force microscopy (AFM). In SEM, SWNTs can be quickly located with 1 kV or lower acceleration voltage. However, electron beam could damage the SWNTs[2, 3] or deposit amorphous carbon that makes ohmic contact difficult. To minimize damage, the SEM is only used for initial quick searching for SWNTs in a large area (Figure 6.2 (a)). EFM, which is slower, is used to further locate the SWNTs

within the known area (Figure 6.2 (b)), and we find that is very effective for locating SWNTs encapsulated in boron nitride. AFM is primarily used for measuring the diameters of the SWNTs (Figure 6.2 (c)).

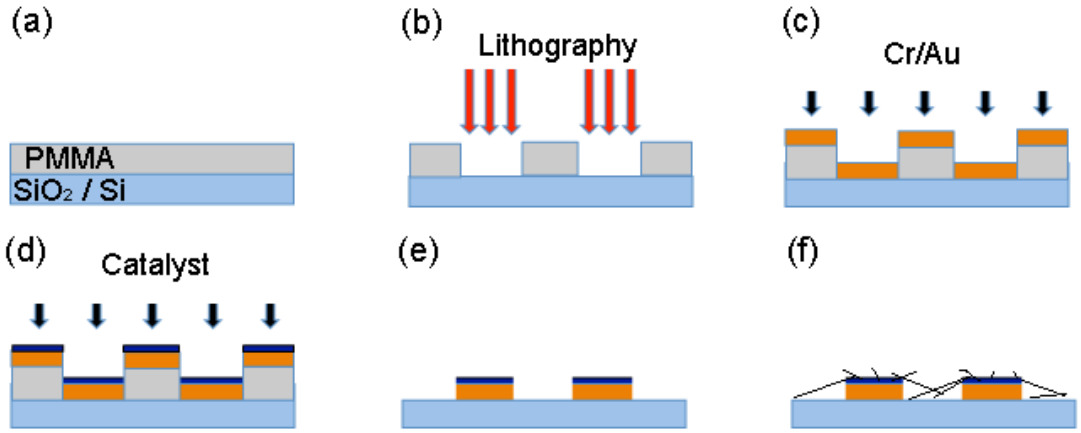

Figure 6.1. Process for growing SWNTs. (a). PMMA layer is spin-coated onto SiO_2 / Si substrate. (b). E-beam lithography defines the catalyst islands. (c). 10 nm Cr / 30 nm Au are deposited. (d). Few drops of catalyst solution are deposited on the Cr / Au layer. (e). PMMA layer together with Cr / Au and excess catalysts are removed in acetone. (f). SWNTs are grown from the catalyst islands in furnace.

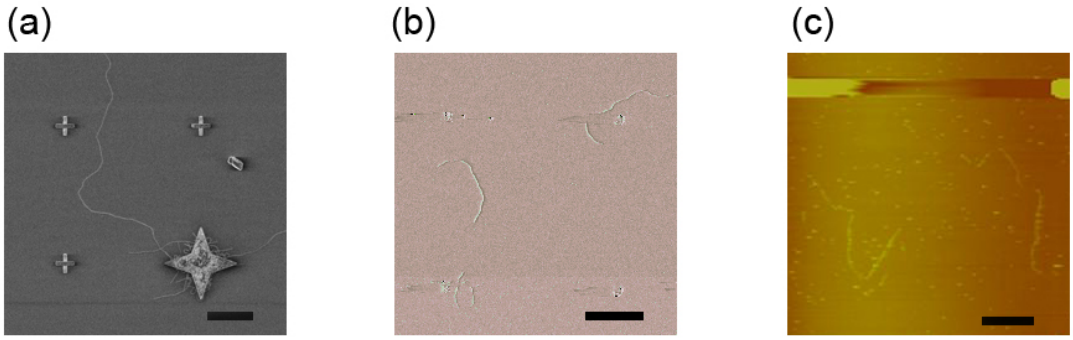

Figure 6.2. Images of single-walled carbon nanotubes in (a). SEM. (b). EFM. (c). and AFM. (Scale bar: 10 μm)

6.3 Device Fabrications

To fabricate carbon nanotube devices, LOR (MicroChem LOR3B) / PMMA bilayer are used instead of PMMA or MMA / PMMA as used for graphene devices since it is more difficult to make reliable contact to SWNTs with PMMA or MMA, and LOR leaves much less residue. Here the catalyst islands also serve as alignment marks. After locating desirable carbon nanotubes in SEM or EFM, we spin-coat LOR solution onto the chips at 4000 rpm for 40 seconds, and bake the chip at 190°C for 5 minutes. This will result in a 300 nm-thick LOR layer. We then spin-coat a layer of PMMA at the same rate and time and bake at 180 °C for 10 minutes. The electode patterns are exposed to electron beam of 400 ~ 800 μC / cm^2 dosage at 20 kV or 30 kV, developed in MIBK : IPA (1 : 3) for 10 ~ 15 seconds and rinse in IPA. The LOR layer is developed in MF319 for 1 ~ 2 seconds, creating undercuts. We rinse the chip with DI water to stop the development.

Due to the match in their work functions, we use Pd as the contacting metal to SWNTs[4, 5]. However, Pd usually does not stick to the substrate well, so we deposit 1 nm Cr as the adhesion layer. In general, 1 nm Cr / 5 nm Pd / 40 nm Au is deposited for carbon nanotube devices. The devices are completed by lifting-off in PG Remover at 80 °C for at least 20 minutes, and characterized using the method described in Section 3.5.

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Chapter 7. Superior Current Carrying Capacity of Boron-Nitride Encapsulated Carbon Nanotubes with Zero-Dimensional Contacts

7.1 Introduction

Carbon nanotubes (CNTs) has been demonstrated to be an ideal material for fundamental studies such as Luttinger liquid[1], Wigner crystals[2] and Mott Insulator[3] due to its ultra small size and extraordinary electrical properties. It is also a promising candidate for potential applications such as logic-gate circuits and electrical interconnects. However, its excellent material properties are often compromised by the conventional SiO_2 substrates that are rough topographically and host trapped charges. This problem can be circumvented by suspending the CNTs, though suspended devices face other challenges in terms of mechanical instability and ease of implementation. Recently, hexagonal boron nitride (hBN) has been widely adopted as a new substrate or dielectric for two-dimensional (2D) material studies[4, 5], because it is atomically flat with few or no dangling bonds[4, 6] and has been shown to improve graphene's mobility for electrical and optical studies. In addition, hBN shares the similar lattice structure as graphene with less than 2 % lattice mismatch. Placing graphene on hBN with slightly different orientations can result in superlattices, which give rise to fascinating phenomena such as the

emergence of the secondary Dirac points and Hofstadter butterfly fractal spectrum.[7–9] Since CNTs can be considered as rolled up graphene sheets, we expect to observe high quality quantum transport and possibly secondary Dirac points in hBN-supported CNT devices.[10]

Here we report two methods to fabricate the hBN-encapsulated CNT devices that are free from polymer contamination, using a technique similar to that developed by L. Wang et al.[11] This prior study utilize van der Waals (vdW) forces to directly pick up and transfer two-dimensional (2D) atomic layers. In contrast to transfer among 2D materials, the vdW forces between 1D and 2D materials are not sufficiently strong to pick up CNTs from SiO_2 substrates. We developed two different methods that allow the assembly of the hBN / CNT / hBN stacks with the assistance of polymer and with hydrofluoric acid (HF) etching of SiO_2, respectively. Electrical contacts are made to the ends of CNTs that are exposed by reactive ion etching (RIE). Surprisingly, even though the contact area is limited to one circumference of carbon atoms, the contacts remain ohmic with transconductance of up to 30 μS at 4 K, attesting to the high device quality. Coulomb blockade diamonds are observed in such devices. Another interesting finding is that each hBN-encapsulated CNT can sustain currents as high as 350 μA, about one order of magnitude higher than the value of 25 μA in SiO_2-supported CNT devices. We attribute such superior current-carrying capacity to the enhanced heat dissipation of hBN substrates and superstrates.

7.2 Device Fabrication

CNTs are grown by chemical vapor deposition[12] and located using scanning electron microscope (SEM). The hBN / CNT / hBN stacks are assembled in two methods. In the first method, a layer of polypropylene carbonate (PPC) (~ 30 wt% in anisole) is spin-coated on a piece of polydimethylsiloxane (PDMS) using a glass slide as a holder, followed by baking at 180 °C for 2 minutes to remove the solvent. A thin top hBN flake with thickness less than 30 nm is exfoliated on a SiO_2 / Si chip and is first picked up by the PPC in our homemade transfer stage after heating up the substrate to 40 ~ 43 °C. The top hBN flake is then aligned and brought into contact with a CNT (Figure 7.1 (a)), while a segment of the CNT is exposed to PPC. The substrate is heated up to 60°C to melt the PPC so that it can make conformal contact to both hBN and CNT. Both the hBN and the CNT are picked up after naturally cooling down the substrate to 40 ~ 43 °C. Finally, the hBN / CNT stack is brought onto another hBN (bottom) flake (Figure 7.1 (b)). The hBN / CNT / hBN stack is finished after separating PDMS by heating up the substrate to 80 ~ 90 °C and removing the PPC in chloroform (Figure 7.1 (c)). The second method is similar to the method described in a study by P. J. Zomer et al.[13] The top hBN flake is exfoliated onto an Elvacite-based multilayer stack and transferred to cover a CNT. The hBN / CNT is then released from the SiO_2 substrate in HF using a spin-coated Elvacite and a piece of tape as a carrier. Then, the hBN / CNT is transferred onto another hBN (bottom). By heating up the substrate to 60 °C, the tape is separated from the stack. The Elvacite is then removed in acetone. Figure 7.2 (a) shows a finished hBN / CNT / hBN stack imaged in electrostatic force microscopy (EFM). The dark line shows a 40 μm long

CNT with a length of 25 μm encapsulated in hBN and remained contamination free through the transfer process.

To make electrical contacts, both ends of the CNT are exposed by RIE with etching area defined by electron beam lithography and poly(methyl methacrylate) (PMMA) acting as an etching mask. The etching is performed in SF_6 ambient with ICP power 30 W and forward power 300 W. After etching, the PMMA layer is removed in PG Remover (Figure 7.1 (d)). Subsequently, another lithography opens the windows for 10 nm Cr / 50 nm Au metal deposition (Figure 7.1 (e)). Metal deposition can also be performed immediately after etching. Figure 7.2 (b) and (c) show an optical and a false-color SEM image of a device, respectively. In Figure 7.2 (c), the metal contacts were made to the center of the etched area (purple) and also the exposed ends of the CNT (red) such that the CNT acquired charges and glowed under SEM even though it was covered by 30 nm thick hBN. Figure 7.2 (d) shows a zoom-in view of the etched area. The distance of the edge profile in top view is about 40 nm, equivalent to the total thickness of 40 nm of the stack, indicating an angled edge profile such that the metals can contact the CNTs.

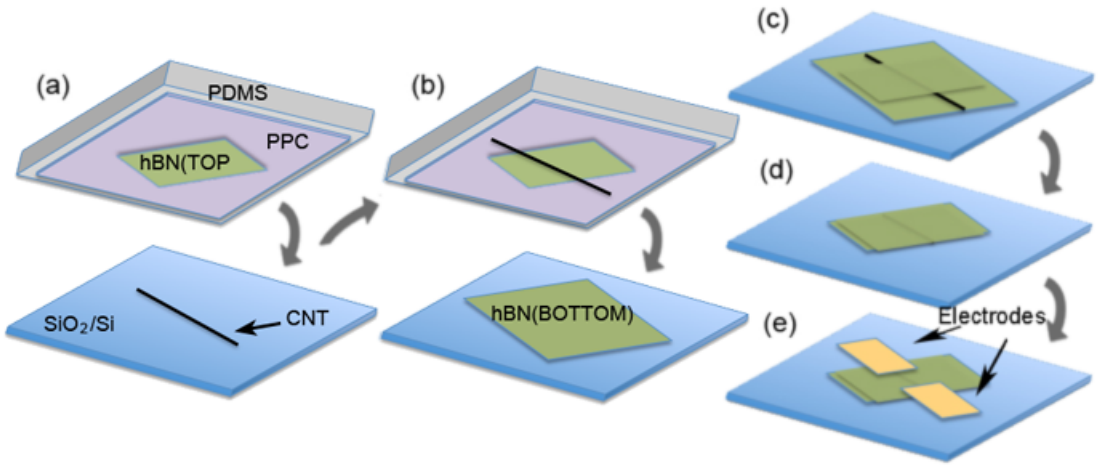

Figure 7.1. Fabrication process for carbon nanotube devices encapsulated in hBN. (a). Top hBN is aligned and brought into contact with a CNT. (b). hBN together with CNT are brought onto the bottom hBN. (c). Finished hBN / CNT / hBN stack after removing PDMS and PPC by heating up the substrate to 80 ~ 90 °C and rinsing with chloroform, respectively. (d). Exposed ends of the CNT are created by SF_6 plasma. (e). Metal contacts are made by depositing 10 nm Cr / 50 nm Au on the ends of CNTs.

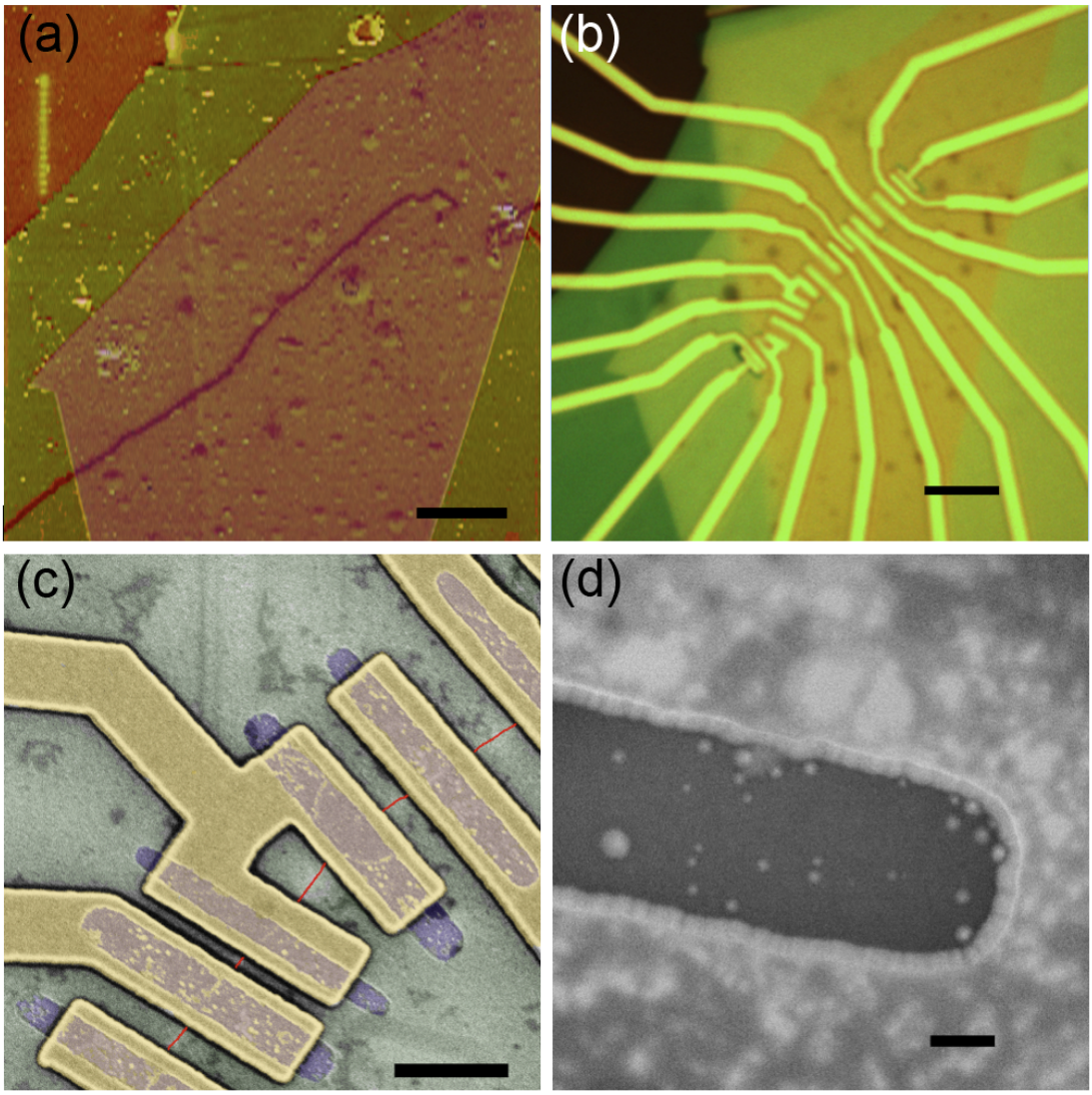

Figure 7.2. Images of an hBN / CNT / hBN device. (a). Electrostatic force microscope image of a finished stack. (b). Optical image of a device. (c). A zoom-in view of the device in SEM. (d). A zoom-in view of the etched area in SEM showing the angled edge profile. (scale bars: (a), (b) 5 μm; (c) 1μm; (d) 100 nm).

7.3 Transport Data and Discussion

In Figure 7.3, the current-voltage (I-V) characteristics of a device with channel length of 600 nm show ohmic contact at 300 K and 4 K. The transconductance are 32 μS and 31 μS at 300 K and 4 K, respectively. The linearity of the curves and the minimal change in transconductance at different temperatures indicate ohmic contact even though the contact area is limited to the 0D ends.

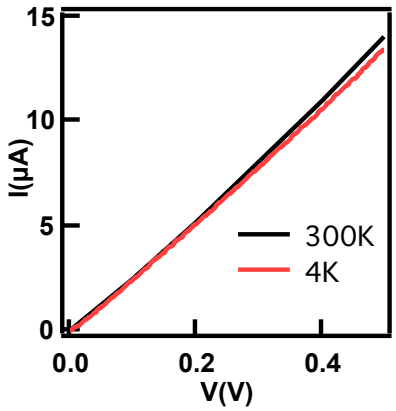

Figure 7.3. Current-Voltage (I-V) characteristics of a device with channel length of 600 nm measured at 300 K and 4 K.

We now focus on the quantum transport features at 4 K. In Figure 7.4, the differential conductance (G) of a device made by the polymer pick-up method is plotted as a function of source-drain bias (V) and gate voltage (V_g). Over ~ 130 Coulomb diamonds were observed in the range $0 < V_g < -5.5$ V. In a zoom-in view of the conductance (in logarithm scale), a series of regular Coulomb diamonds with excited

states is observed, confirming that the device behaves as a quantum dot. The charging energy for the coulomb diamond is $E = e^2/C \sim 8.0meV$, where C is the total capacitance of the device, estimated to be 2.0 x 10^{-17} F, in agreement with previous studies. The energy required for the subsequent excited state is 3.1 meV. The level spacing can be estimated by $\Delta E = \frac{\hbar v_F}{2L}$, where $\hbar$ is Planck's constant. v_F is the Fermi velocity, 8 x 10^5 m/s. The calculated level spacing is 2.8 meV, agrees well with the measured data. We also notice regular features in the middle of diamonds near the center of the gap. Figure 7.5 shows the transport characteristic of a device made by the HF-etching method. The clear Coulomb diamond features suggest that both fabrication methods enable clean, high quality devices.

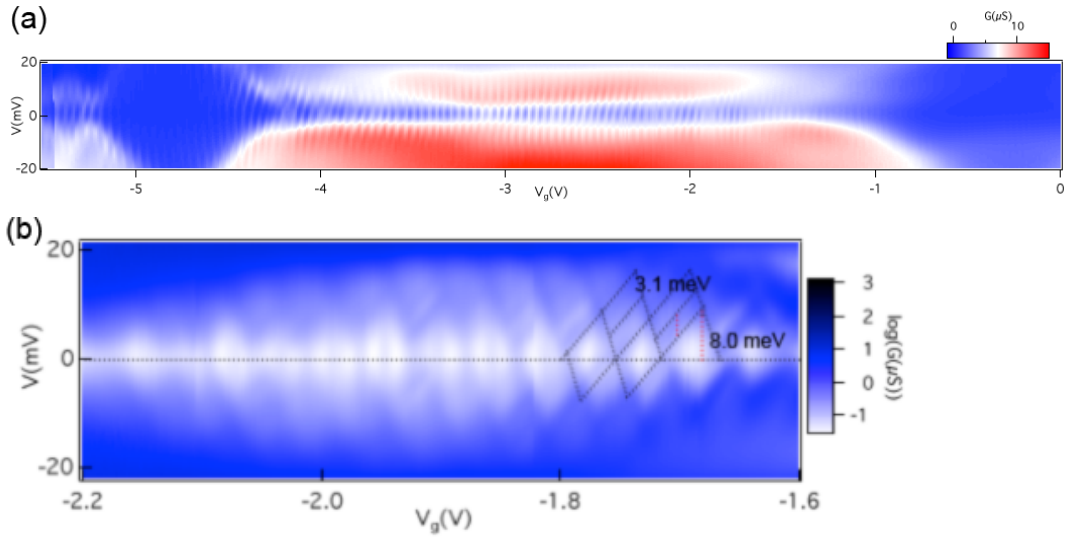

Figure 7.4. Conductance (G) vs source-drain bias (V) and gate voltage (V_g) (T = 4K) of a device made by polymer pick-up method. (a). Over 130 coulomb diamonds are observed in the hole-side ($0 < V_g < -5.5$ V). (b). A zoom-in view of the conductance (in logarithm scale) at the gap centered at $V_g = -4.8$V in (a). A series of regular Coulomb diamonds are observed. A different scale in the V_g is caused by hysteresis.

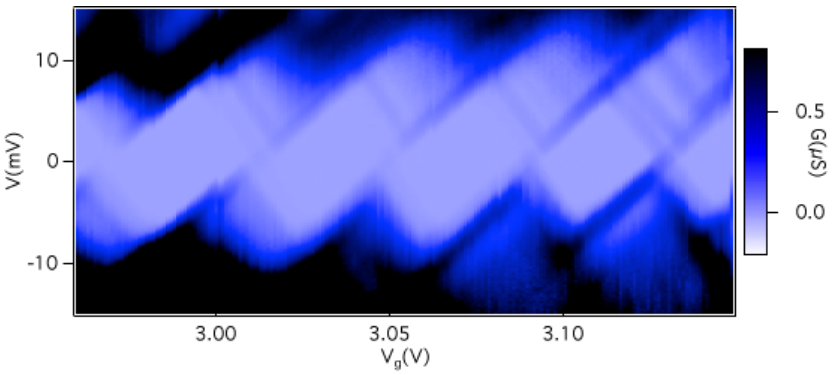

Figure 7.5. Conductance (G) vs source-drain bias (V) and gate voltage (V_g) (T = 4 K) of a device made by HF-etching method.

7.4 High Current Carrying Capacity

Normally, an individual CNT on SiO_2 with typical lengths ranging from 0.25 to 8 μm has limited current carrying capacity ~ 25 μA due to the optical phonon scattering which cause the saturation at high bias.[14, 15] This capacity can be increased to up to 100 μA by making ultra short channel (~ 15 nm) such that the mean free path of optical phonon is more compatible with the channel length.[16] Here we notice that CNTs encapsulated in hBN can sustain higher current than those on SiO_2. Figure 4 shows the *I-V* curves of three CNT devices, two encapsulated in hBN and one on SiO_2, fabricated on the same CNT and with channel length of 600 nm. At low bias, the curves are linear and visually identical. At high bias, the CNT on SiO_2 at 300 K can sustain current up to ~ 190 μA, indicating about 8 walls in the CNT, while the currents of the CNT encapsulated in hBN can carry 320 μA and 350 μA, at 300 K and 4 K, respectively. Table 7.1 summarizes the breakdown currents and powers of these devices. At 300 K, the breakdown power of the CNT encapsulated in hBN is three times that for CNT on SiO_2, suggesting the high heat dissipation efficiency of hBN.

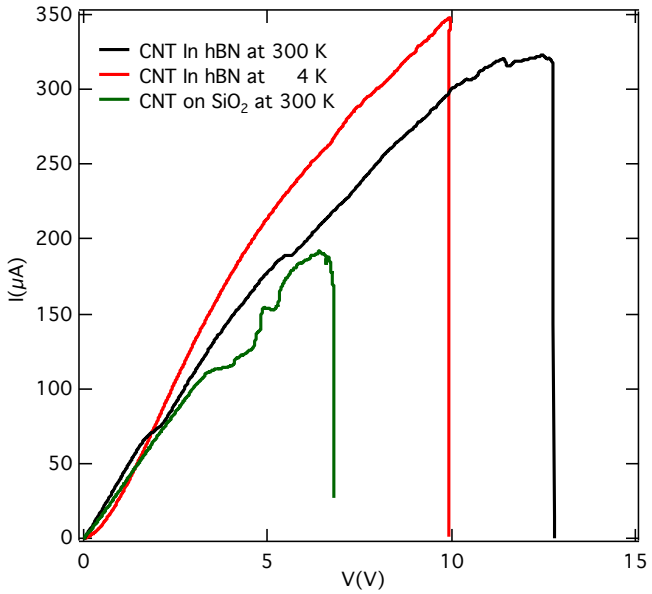

Figure 7.6. *I-V* of two hBN-encapsulated and one SiO_2-supported carbon nanotube devices. Their breakdown currents are 320 μA (300 K, hBN-encapsulated, black curve), 350 μA (4 K, hBN-encapsulated, red curve) and 190 μA (300 K, SiO_2-supported, green curve), respectively.

	Encapsulated in hBN		On SiO_2
Temperature	4 K	300 K	300 K
Current	350 μA	320 μA	190 μA
Power	3.47mW	4.06mW	1.23mW

Table 7.1. Breakdown currents and powers of CNTs encapsulated in hBN and on SiO_2.

7.5 Conclusion

In conclusion, CNT devices encapsulated in hBN are fabricated using two different methods. Zero-dimensional contacts are successfully made to the ends of 1D CNTs. We observe clear Coulomb diamonds with a single period, suggesting high quality devices. Interestingly, these hBN encapsulated CNT devices can also carry higher current density than SiO_2-supported counterparts, likely due to the superior heat dissipation by hBN layers. This study suggests the potential of such devices for fundamental studies and high power applications.

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Chapter 8. Electrical Transport in Graphene-Carbon Nanotube Junctions

8.1 Introduction

Momentum-conserved tunneling between a one-dimensional (1D) wire and a two-dimensional (2D) sheets provides a very useful platform for studying the interaction in many-body system. The tunneling transport depends on the overlap in the spectral functions of the two systems. Here we seek to study the transport between 2D graphene, which has ultra-high carrier mobility and ambipolar effect, and 1D single-walled carbon nanotube (SWNT), which has been shown to behave as Luttinger Liquids[1], Wigner Crystals[2] and Mott insulators.[3]

One of the main challenges of this project is the reliable fabrication of high quality graphene-SWNT junctions. To address this challenge, we have developed two different techniques: (1). fabricating suspended junctions with contactless top-gates, which has yielded some transport data at low temperature, though the devices typically suffer from structural instability; and (2). fabricating devices on hexagonal boron nitride (hBN) that are more stable. The latter technique was only recently developed and we have obtained some preliminary data.

8.2 Device Fabrication

To fabricate suspended graphene-SWNT junctions, we grow SWNT on SiO_2 / Si substrates by chemical vapor deposition, transfer a graphene sheet on top of a SWNT, and use electron bema lithography to fabricate suspended top gates and electrodes that separately contact the SWNT and graphene. The completed devices are then etched in BOE and dried in critical point drier.

This study involves dual-gated suspended devices, in which a contactless top gate and the Si back gate enable independent tuning of the Fermi level of both graphene and SWNTs.

Graphene sheets are transferred to SWNTs using either wet transfer (Chapter 3.4.1) or dry transfer via resists (Chapter 3.4.2). After fabricating the device, two different methods are developed to build a contactless top gate above the suspended junction, as described below.

8.2.1 Method I

In this method[4, 5], the electrodes for graphene and SWNTs are fabricated first via standard e-beam lithography on After the transfer, the graphene / carbon nanotube stack is ready. We pattern the electrodes for the graphene and the carbon nanotube using e-beam lithography on Poly(methyl methacrylate) (PMMA) / LOR (MicroChem LOR3B) resist bilayer and depositing 10 nm Cr / 150 nm Au. Although Pd makes excellent contact to the carbon nanotubes, Pd is not used in the structure because Pd fails to support the

structure after the subsequent BOE etching. After metal deposition, the device is lifted-off in acetone.

To design the top gate, we create two anchors and a suspended bridge across the junction in two separate lithography steps. The resist used in the lithography is PMMA / LOR3B. The anchors are defined in the first lithography step and followed by developing in MIBK : IPA (1 : 3) and MF319. The suspended bridge is defined in the second lithography step, which is only developed in MIBK / IPA (1 : 3). Three-angle evaporations are adopted to ensure robust structure – first deposition of 10 nm Cr / 150 nm Au at 45°, second deposition of 10 nm Cr / 200 nm Au at -45°, and last one of 10 nm Cr / 100 nm Au at 0°. The device is lifted-off in PG Remover at 80°C for at least 20 minutes.

While still wet, the chip is transferred to IPA to dilute the PG Remover, then to BOE for 90 seconds to etch the SiO_2. The device is then dried in critical point drier (CPD).

The pitfall of this technique is that the electrical contacts usually degrade during the lithography steps for top gate fabrication, possibly due to oxidation of the Cr adhesion layer during resist baking.

8.2.2 Method II

Unlike the previous method, this method allows fabrication of the electrodes and top gate in a single lithography step.

To design the patterns, we create four anchors sitting in between adjacent electrodes, so that the suspended bridge will be connected to all four anchors.

The resist used is PMMA / MMA / PMMA / LOR3B (top to bottom). The first two and last two layers provide the undercut for the bridge and anchors, respectively. In the e-beam lithography, we use 800 μC / cm^2 dose at 30 kV to make accurate pattern. The windows for the electrodes and anchors are opened in the first lithography step and developed in MIBK / IPA (1 : 3) for 10 ~ 15 seconds and then in MF319 for 1 ~ 2 seconds. Another lithography defines the suspended bridge. The pattern of the bridge is only developed in MIBK / IPA (1 : 3) for 10 ~ 15 seconds.

After the developing, we perform three-angle metal deposition, lift-off, BOE etching and CPD drying as described in Method I.

8.2.3 Device Images

Figure 8.1 shows the SEM-images of a finished device. It can be clearly seen that under the contactless top gate both graphene and carbon nanotube are suspended. A clearer view of how the two materials are suspended can be seen in a device without top gate as shown in Figure 8.2.

One drawback of this diagonal top gate configuration (as seen in Figure 8.1) is that it is necessarily a local gate in order to avoid the overlap between the electrodes and the top gate. Another configuration we have attempted is a top gate with X-shaped anchors, as shown in Figure 8.3. This type of top gates is more robust and can provide more global gating effect.

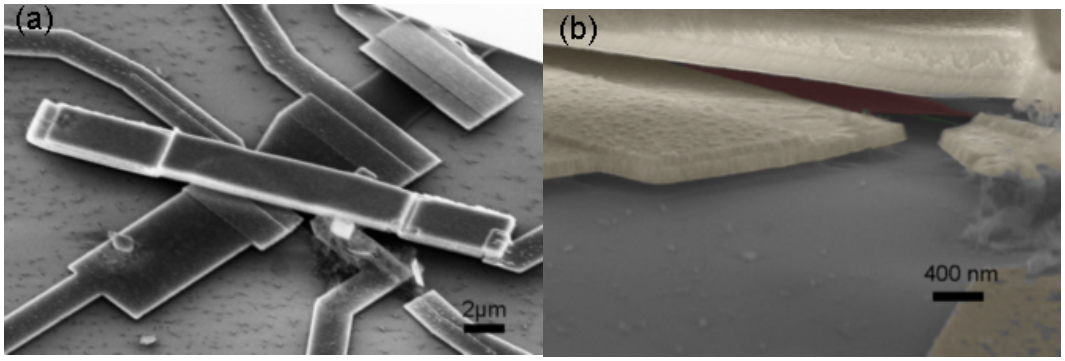

Figure 8.1. SEM-images of suspended graphene-carbon nanotube device with global top gate in (a). top view and (b). tilted view (false colored).

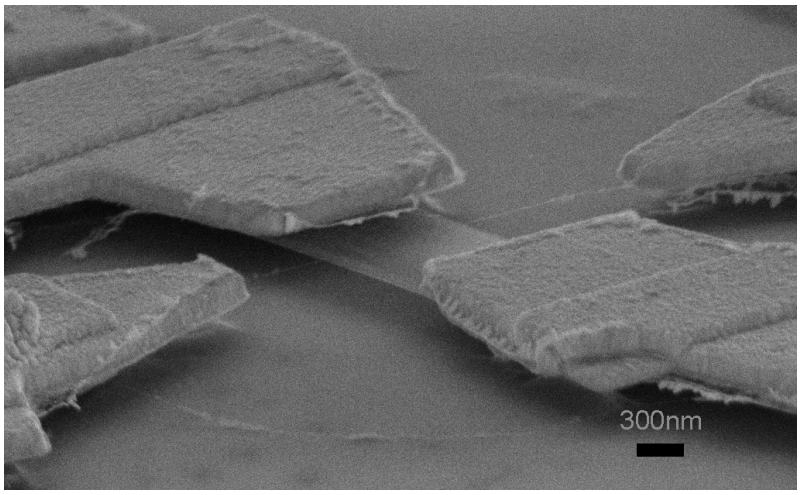

Figure 8.2. SEM-image of suspended graphene-carbon nanotube device.

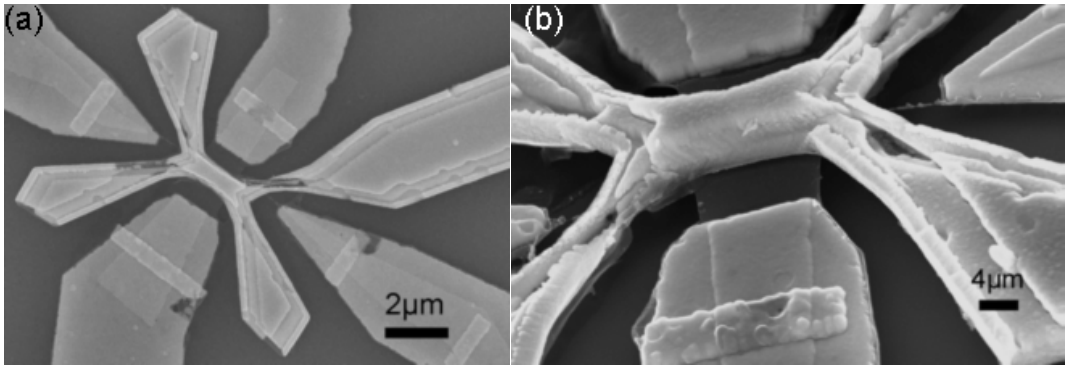

Figure 8.3. SEM-images of suspended graphene-carbon nanotube device with local top gate in (a). top view and (b). tilted view.

In addition to suspended junctions, we also recently started fabricating garphene-SWNT junctions on hBN substrate. Recently, hBN has been widely used as substrates for graphene devices.[6, 7] Since it is atomically flat and has no dangling bond, ultra-high mobility graphene devices on hBN have been demonstrated.[6, 8] In addition, hBN also has honeycomb lattice, with a lattice mismatch from graphene of 1.7 %,[6] giving rise to superlattices and interesting physics such as the Hofstadter butterfly fractal spectrum.[9–11] hBN also is an excellent substrate for carbon nanotubes, e.g. single nanotube quantum dot has been demonstrated using hBN-supported carbon nanotube devices.[12] In our case, using hBN allows high quality devices without the restriction of choice of metals.

The fabrication process begins with transferring top hBN layer and graphene on the bottom hBN layer, as described in Chapter 3.4.3. We perform e-beam lithography to make two edge-contacts to graphene, and using RIE to expose one additional edge of

graphene for the subsequent graphene-SWNT contact. A SWNT is transferred to the exposed graphene edge using the wet-transfer technique described in Chapter 3.4.1. The entire structure now consist of SWNT / hBN / graphene / hBN, with a point contact between the SWNT and graphene. A finished device is shown in Figure 8.4.

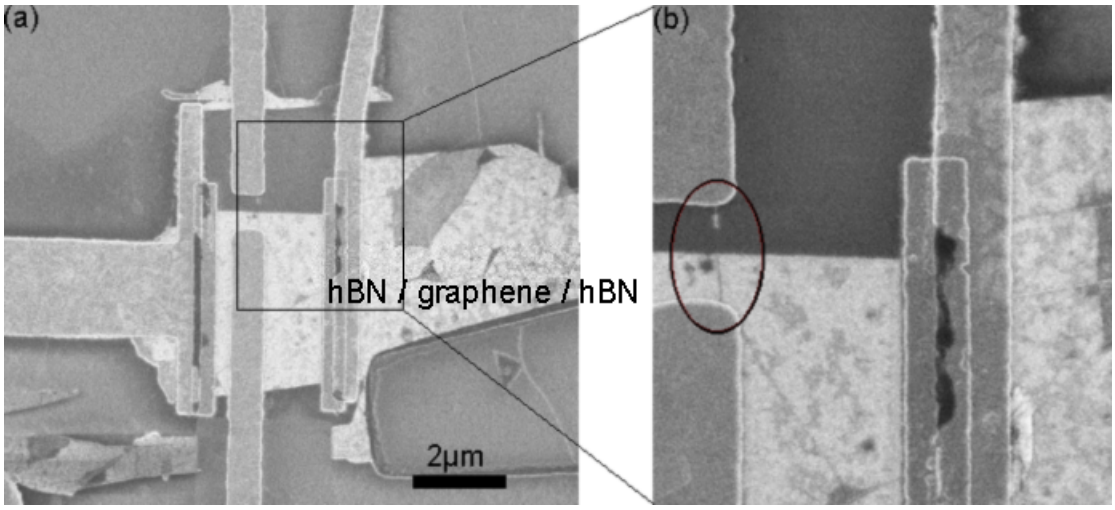

Figure 8.4. SEM-images of hBN-based graphene-carbon nanotube device. (a). The brighter flake is a stack of hBN / graphene / hBN. The graphene was edge-contacted. The carbon nanotube was wet-transferred to the middle of the two electrodes of graphene. The electrodes for carbon nanotube were made top-contacted after the transfer. (b). Zoom-in view of the carbon nanotube (circled area).

8.3 Data and Discussion

We perform low temperature measurements at $T < 4$ K via the standard lock-in technique to probe the two-terminal differential conductance $G = dI/dV$ between SWNT and graphene. Promising data are obtained, as outlined below.

8.3.1 Fabry-Perot Interference

In Figure 8.6, we plot the conductance G of a suspended device (dimensions shown in Figure 8.5) as a function of source-drain bias V and back gate voltage V_{bg} at T = 1.6 K. A striking checkerboard pattern is observed. This is a signature of the Fabry-Perot interference, which arises from the successive reflections of electron waves between two partially transmitting electrodes.[13, 14] The level spacing for metallic carbon nanotube is given by

$$\Delta E = \frac{h v_F}{2L},$$

where h is the Planck's constant, v_F is the Fermi velocity of carbon nanotube, 8.1 x 10^5 m/s, and L is the distance that the charges travels between the two reflective interfaces. In the data, the estimated ΔE is 3 meV, corresponding to $L \sim 0.6$ μm, which is close to the source-drain separation ~ 0.7 μm. The regularity of the checkerboard pattern suggests that much of the reflection takes place inside the nanotube, and graphene likely serves as a good contact in this device. The data hence indicates the relative transparent contacts at the metal-graphene, metal-SWNT and metal-SWNT junctions, and the absence of scatterers inside the nanotube.

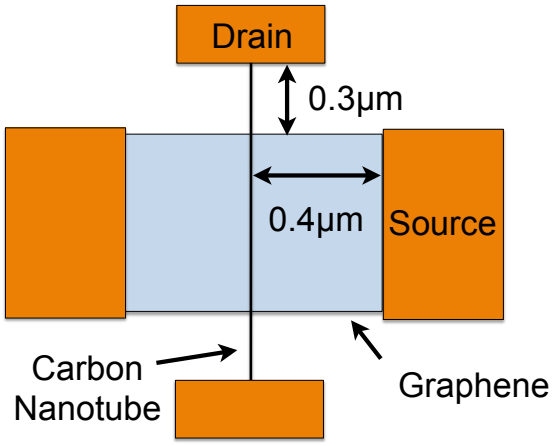

Figure 8.5. Schematic of graphene-carbon nanotube device I.

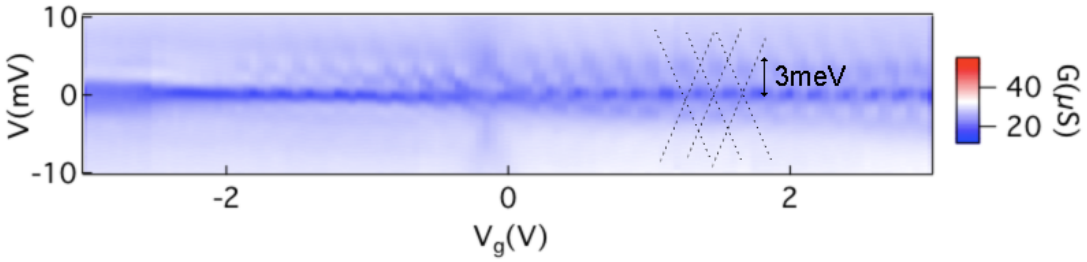

Figure 8.6. Conductance at $T = 1.6$ K of a graphene-carbon nanotube junction measured at as a function of bias and back voltage. The characteristic energy for the Fabry-Perot interference is 3 meV.

Similar phenomenon can be seen in another device probed at $T = 400$ mK with the geometry shown in Figure 8.7. This device has a global top gate and the mobility of graphene is 35,000 cm^2 / V·s. Figure 8.8 is its conductance plotted as a function of bias

and back (top) gate voltage. The plot resembles the Fabry-Perot interference pattern from graphene, and is less regular than that from a nanotube, since more resonator modes can be excited in a 2D cavity. The estimated characteristic energy is $\Delta E = 2\ meV$ in both data so the expected channel length is $L = 0.8$ μm, which is again close to the actual channel length 0.8 μm. The graphene-carbon nanotube junction thus acts as a resonant cavity for such phase coherent transport.

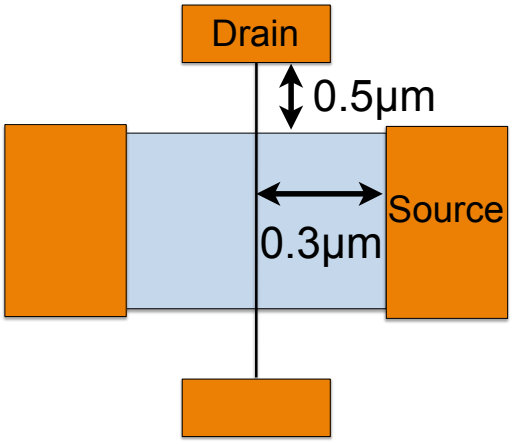

Figure 8.7. Schematic of graphene-carbon nanotube device II.

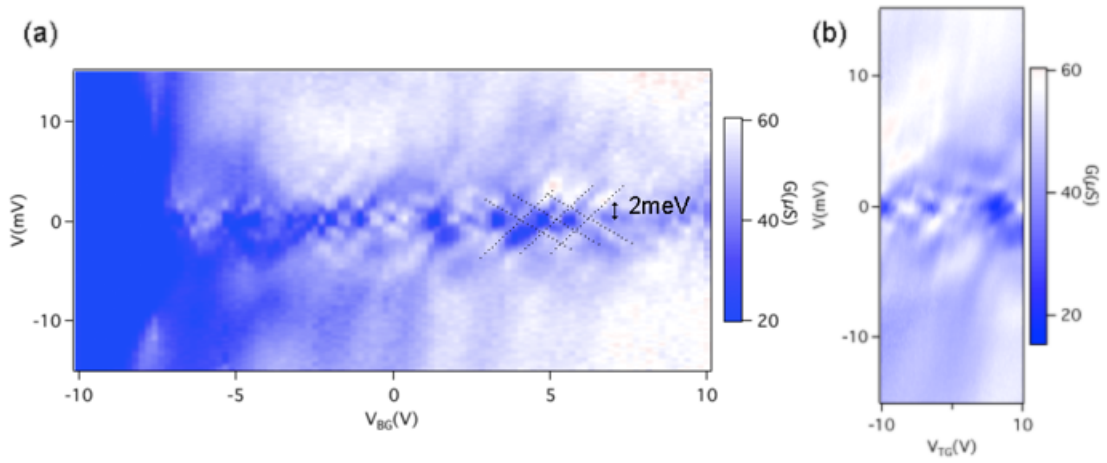

Figure 8.8. Conductance at $T = 400$ mK of a graphene-carbon nanotube junction measured at as a function of bias and back (a). (top (b).) voltage. The characteristic energy for Fabry-Perot interference is 2 meV.

8.3.2 Transport in Magnetic Field

Some suspended devices are measured in magnetic field B with the axis of the tube aligned with field. Figure 8.9 (a) plots device conductance as a function of back gate voltage and magnetic field. We observed features that move in opposite directions with magnetic field, as indicated by the dashed lines. We postulate that these features arise from the magnetic field lifting the degeneracy of charge carriers that transverse the nanotube in clockwise and counterclockwise directions (Figure 8.9 (b)).

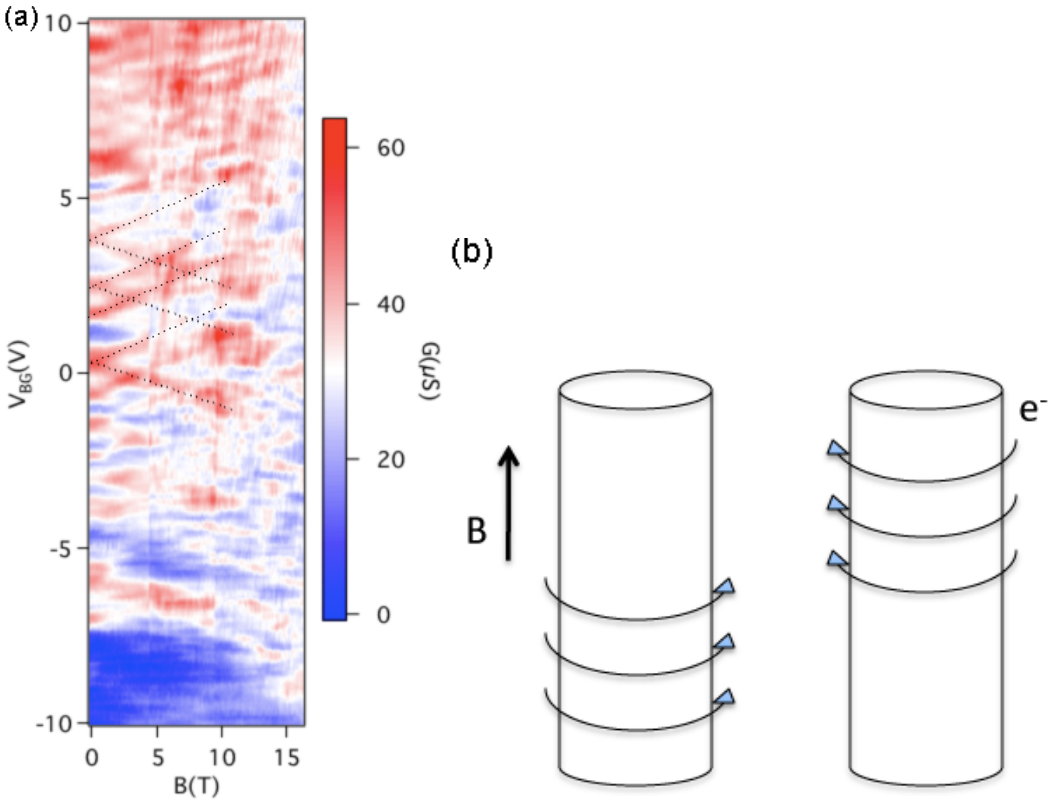

Figure 8.9. (a). Conductance at $T = 400$ mK of a graphene-carbon nanotube junction measured at as a function of back gate voltage and magnetic field. (b). The electrons can travel clockwisely or counterclockwisely due to the presence of magnetic field.

8.3.3 Coulomb Blockade

In another suspended device, the contact between graphene and SWNT is relatively resistive such that it gave rise to the Coulomb blockade with quantum dot forming in the SWNT. Figure 8.10 plots its conductance G vs source-drain bias V and back gate voltage V_{BG}. Several Coulomb blockade diamonds along with additional

excited states were observed in a suspended device. The charging energy required an electron passing though two resistive junctions is $E = \frac{e^2}{C}$, where C is the capacitance of the system.[15] In this device, the estimated charging energy from the data is $E = 6.35meV$, which is consistent with those reported in previous studies.[15]

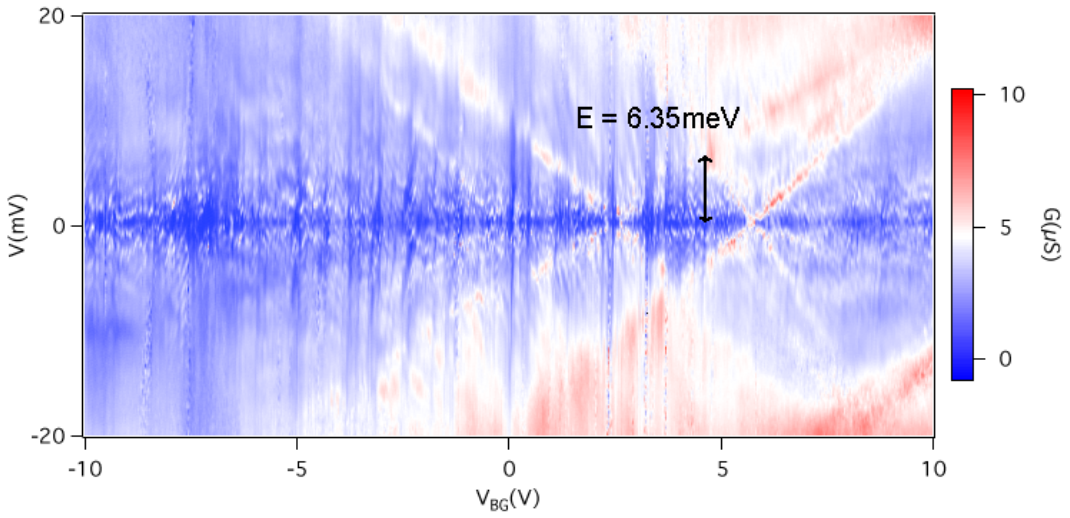

Figure 8.10. Conductance at T = 1.6 K of a graphene-carbon nanotube junction measured at as a function of bias and back gate voltage.

8.4 Conclusion

In this chapter, we discussed the fabrication techniques and our observations in electrical transport properties of suspended graphene-carbon nanotube junctions. We

have seen transport features from both graphene and carbon nanotube such as Fabry-Perot interference and Coulomb blockade. However, all these transport features have been observed in many studies. The expected 1D-2D momentum conserved tunneling eluded our observation. The main limitation, in my opinion, lies with the relative low sample quality. Another problem is that the two materials overlap for extended distances and transport between them does not occur at a well-defined point. Therefore, we developed a different device configuration: placing the graphene-SWNT junction on hBN should yield higher quality devices, and the minimized contact should also provide another opportunity for studying this 1D-2D transport.

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Chapter 9. Conclusion and Outlook

Over the past 5 years, my colleagues and I focused on modifying transport properties of graphene and carbon nanotube devices. We have achieved satisfactory results in chemical modification of graphene devices, suspended graphene devices under *in situ* strain and graphene-carbon nanotube hybrid devices. In particular, in contrast to most variations of chemically derived graphene, we modify the band structure of graphene using organometallic chemistry, which improves the on / off ratio while keeping the graphene's high mobility. This study suggests potential applications in molecular wires and spintronics devices, etc.

Our development of nano-electromechanical system (NEMS) -based graphene devices allows us to study the modification of suspended graphene devices via *in situ* strain. Single- and bi- layer graphene devices have demonstrated their improved field-effect mobilities under repeated strain cycles. More importantly, bi-layer graphene device has shown a lowered conductance at charge neutrality point, likely due to the relative shift between the 2 layers. The device geometry can be applied to other materials for transport or optical studies.

Our successful fabrication of carbon nanotube devices encapsulated in hexagonal boron nitride and achieving zero-dimensional contact to 1D wires are important developments for 1D devices and physics. Also, the boron nitride encapsulation not only provides a clean substrate for the nanotubes but also enables greater heat dissipation and

protects the nanomaterials from ambient environment.[1] Such device geometry could lead to a great improvement in the performance of electronic devices and fabrication of devices based on air-sensitive materials.

In the study of electrical transport in graphene-carbon nanotube junctions, we have developed different techniques for creating graphene-carbon nanotube junctions with dual gates. We have observed quantum transport arising from both graphene and carbon nanotubes portions of the devices. Further pursuit of this should aid our understanding of interactions in many-body systems.

Graphene and carbon nanotubes have great potential in application such as digital electronics, displays, solar cells and sensors. However, the dream of having all-carbon electronic devices is challenging. The obstacles in graphene, for example, are to create a large band gap that is compatible with digital electronics and to produce large-scale high quality graphene sheets. In carbon nanotubes, the problems lie with selectively producing semiconducting or metallic carbon nanotubes, making stable electrical contacts and increasing the current carrying capacities. This thesis work has made progress in addressing some issues in realization of applications. In the future, it is my wish that the obstacles are overcome and these carbon materials can be part of our everyday lives.

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