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Modeling and Analysis of Switched-Capacitor Converters with Finite Terminal Capacitances

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***Abstract*—In pre-existing analytical models of switched-capacitor (SC) converters, the input and output capacitances ($C_{\rm in}$ and $C_{\rm out}$) have long been assumed to be infinitely large so that the input and output can be modeled as ideal voltage sources. However, in practice, the terminal capacitances can be insufficient to ensure ideal input and output behaviors due to space and cost constraints. This paper reveals that finite terminal capacitances can have considerable effects on the output impedance ($R_{\rm out}$) and overall efficiency of SC converters. A general modeling and analysis methodology is proposed for SC converters to characterize the effects of finite terminal capacitances quantitatively. A 2-to-1 SC converter prototype is specially designed to verify the proposed general output impedance model. The relative error between the modeling results and the experimental measurements is less than 8%, which demonstrates the excellent accuracy of the proposed model. It is revealed that the insufficiency in $C_{\rm in}$ can lead to a considerably higher $R_{\rm out}$ and harm the overall efficiency. On the contrary, decreasing $C_{\rm out}$ can counter-intuitively help reduce $R_{\rm out}$, which contributes to both higher efficiency and higher power density, although this benefit comes at the cost of a larger output voltage ripple. In addition, $C_{\rm out}$ has a stronger effect on $R_{\rm out}$ in the slow switching region, while $C_{\rm in}$ is more influential in the fast switching region, especially around the knee of the output impedance curve, which is the typical operating point of SC converters. Several design guidelines are provided based on these findings. Further discussions are provided to explain how to apply the proposed general output impedance model to arbitrary SC topologies.**

***Index Terms*—Circuit modeling, input capacitance, output capacitance, output impedance, switched-capacitor converters.**

I. Introduction

Compared with traditional magnetic-based power converters, switched-capacitor (SC) converters have been demonstrated to have great potential of achieving higher power density and more effective switch utilization [1], [2]. Therefore, they are widely used in various applications, including CMOS integrated power conversion [3]–[6], consumer electronics [7], power amplifier [8], data center power delivery [9], and automotive systems [10]–[12], ranging from DC-DC [13] to DC/AC-AC [14]–[17] conversions.

Although pre-existing models [18]–[23], analyses [24]–[30], and control [31], [32] of SC converters assume input and/or output to be ideal voltage sources, as illustrated in Fig. 1(a), practical implementations of SC converters involve input and output capacitors ($C_{\rm in}$ and $C_{\rm out}$) to stabilize the terminal voltages, as shown in Fig. 1(b). Theoretically, if $C_{\rm in}$ and $C_{\rm out}$ are much larger than the flying capacitor ($C_{\rm fly}$) (i.e. $C_{\rm in}$, $C_{\rm out} \geqslant 10C_{\rm fly}$) the input and output can be regarded as ideal voltage sources. However, in practical applications, the sizes of $C_{\rm in}$ and $C_{\rm out}$ are usually constrained by space and cost and thus can be insufficient to ensure ideal input and output behaviors. Fig. 2 illustrates the schematic drawing of a 2-to-1 SC converter with finite terminal capacitances, with the simulated output impedance curves with different terminal capacitances presented in Fig. 2(b). As shown in Fig. 2(b), the output impedance curve can significantly deviate from the ideal scenario when the terminal capacitances are insufficient.

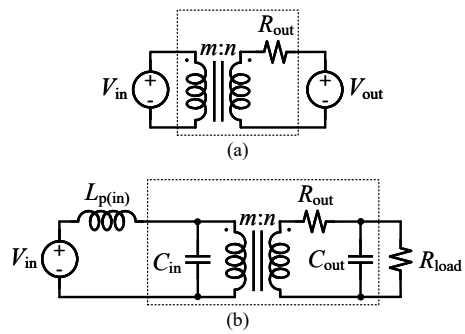


Fig. 1: General steady-state model of an SC converter. (a) Idealized input and output. (b) Practical input and output. ($L_{\rm p(in)}$: the parasitic source inductance)

Although terminal capacitances can have considerable effects on the output impedance, there is currently no analytical tool that is able to characterize their effects quantitatively. The selection of $C_{\rm in}$ and $C_{\rm out}$ in the design of SC converters is mainly based on engineering experiences and trial and error. However, since the die area is typically limited and valuable in integrated circuits such as CMOS converters, quantitative optimizations should be performed to find out the best combination of flying capacitances and terminal capacitances to achieve the lowest output impedance within the limited area. This indicates a need for a general analytical tool to characterize the effects of terminal capacitances in SC converters, which can help practicing engineers and researchers achieve the optimum converter size and performance.

This paper expands upon our earlier conference publication [33] with more detailed analyses, enriched design guidelines, and further explanations for the applicability of this work to arbitrary SC topologies. In this paper, a general modeling and analysis methodology for SC converters is proposed to characterize the effects of finite $C_{\rm in}$ and $C_{\rm out}$. Section II explains the derivation of the proposed general output impedance model in detail. In Section III, a 2-to-1 SC converter pro-

Part of this manuscript was presented at the 2021 IEEE Applied Power Electronics Conference and Exposition (APEC) with the same title. This manuscript includes more detailed analyses, enriched design guidelines, and further explanations for the applicability of the proposed model to arbitrary SC topologies.

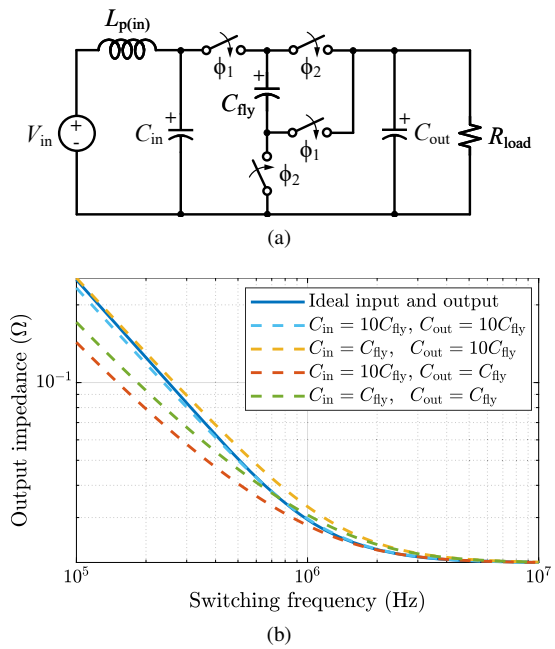


Fig. 2: Output impedance of a 2-to-1 SC converter with different terminal capacitances. (a) Schematic drawing of the 2-to-1 SC converter. (b) Output impedance curves with different C_{in} and C_{out}. ($C_{\text{fly}} = 10$ μF, R_{on} =10 mΩ)

totype is specially designed for model verification, and the modeling results agree well with experimental measurements with less than 8% relative error. To facilitate analysis, the proposed model is approximated by using Taylor expansion in Section IV-A to obtain a simpler mathematical form. Based on the proposed model, it is revealed in Section IV-B that the insufficiency of C_{in} can lead to a significant increase in output impedance, while smaller C_{out} can counter-intuitively help reduce the output impedance and achieve higher efficiency, although this benefit comes at the cost of a larger output voltage ripple. It is also revealed in Section IV-C that the parasitic source inductance and the deadtime can have a nontrivial impact on the output impedance in the slow and fast switching regions, respectively. Based on the above findings, Section IV-D provides several design guidelines. Further explanations for the applicability of the proposed model to arbitrary SC topologies are given in Section V.

II. General Output Impedance Model of SC Converters With Finite Terminal Capacitances

A. Circuit Model

In a general circuit state (or phase) k, an SC topology can be viewed as an *RC* network and represented as the circuit model shown in Fig. 3. It consists of an equivalent resistance R_k and an equivalent capacitance C_k connected in series. With suitable (topology-dependent) R_k and C_k parameters, this general expression can capture any arbitrary SC topologies. The method of calculating the model parameters R_k and C_k for arbitrary SC topologies will be provided in Section V-A.

As illustrated in Fig. 3, two cases should be considered due to the finite input capacitance. The SC converter can be represented as Fig. 3(a) when the input terminal is connected

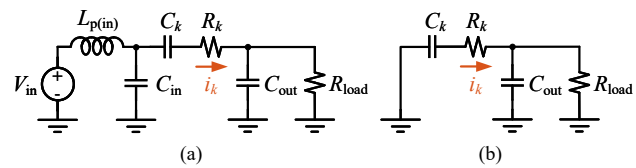


Fig. 3: Complete circuit model of an SC converter with finite C_{in} and C_{out}. (a) Case 1: the input terminal is connected to the source. (b) Case 2: the input terminal is grounded.

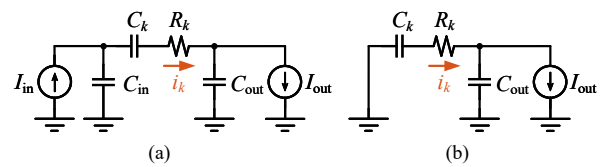


Fig. 4: Simplified circuit model of an SC converter with finite C_{in} and C_{out}. (a) Case 1: the input terminal is connected to the source. (b) Case 2: the input terminal is grounded.

to the source and as Fig. 3(b) when the input terminal is grounded. As conventionally done in topology analysis, the second-order circuit model shown in Fig. 3 can be further simplified as the first-order model illustrated in Fig. 4. First, due to the existence of the parasitic source inductance $L_{\text{p(in)}}$ and the high-frequency operation of SC converters (SC converters typically operate above the critical switching frequency to reach the fast switching limit (FSL) [18]), it can be assumed that the input current ripple is sufficiently small so that V_{in} and $L_{\text{p(in)}}$ together can be regarded as a constant current source I_{in}. Second, since the output voltage ripple is typically designed to be small compared to the average DC output voltage, the ripple on the output current through the resistive load can also be ignored. In addition, some loads are inherently inductive and behave like current sources. Thus, the load can be modeled as a constant current source I_{out}.

B. Calculation of Output Impedance

By definition, the resistive output impedance R_{out} accounts for all conduction losses and charge sharing losses in an SC converter. Therefore, R_{out} can be calculated with the average conduction loss P_{loss} as

$$R_{\text{out}} = \frac{P_{\text{loss}}}{I_{\text{out}}^2}. \tag{1}$$

Note that P_{loss} is the power loss averaged in one switching cycle and thus can be expressed with the summation of the energy losses over all phases as

$$P_{\text{loss}} = f_{\text{sw}} \sum_k E_k \tag{2}$$

where f_{sw} is the switching frequency. E_k represents the energy loss in phase k and can be calculated as

$$E_k = \int_0^{T_{k(\text{eff})}} R_k i_k^2(t)\, dt \tag{3}$$

in which i_k is the current through R_k in phase k and $T_{k(\text{eff})}$ is the effective duration of the phase k. Since there is no forced

freewheeling operation in SC converters during the deadtime, the effective duration of phase k is

$$T_{k(\mathrm{eff})} = T_k - t_\mathrm{d} \tag{4}$$

where T_k is the duration of phase k and t_d is the deadtime.

C. Model Derivation

As indicated by (1)-(3), to calculate the output impedance, we need to find the explicit expression of i_k in all phases based on the first-order simplified model shown in Fig. 4 as

$$i_k(t) = (I_{0k} - I_{\mathrm{f}k})\, e^{-\frac{t}{\tau_k}} + I_{\mathrm{f}k} \tag{5}$$

where I_{0k} and $I_{\mathrm{f}k}$ are the initial value and forced component of i_k in phase k, and τ_k represents the time constant of the equivalent circuit. τ_k and $I_{\mathrm{f}k}$ can be expressed as

$$\begin{cases} \tau_k = R_k C_{k(\mathrm{eff})} \\ I_{\mathrm{f}k} = p_k I_\mathrm{out} \end{cases} \tag{6}$$

in which $C_{k(\mathrm{eff})}$ is the effective capacitance and p_k is a dimensionless ratio. In the two cases illustrated in Fig. 4, for an m-to-n SC converter, $C_{k(\mathrm{eff})}$ and p_k can be given as

$$\begin{aligned} &\text{Case 1}: \begin{cases} C_{k(\mathrm{eff})} = 1 \Big/ \left(\dfrac{1}{C_k} + \dfrac{1}{C_\mathrm{in}} + \dfrac{1}{C_\mathrm{out}}\right) \\ p_k = \dfrac{C_{k(\mathrm{eff})}}{C_\mathrm{in} C_\mathrm{out}} \left(C_\mathrm{in} + \dfrac{n}{m} C_\mathrm{out}\right) \end{cases} \\ &\text{Case 2}: \begin{cases} C_{k(\mathrm{eff})} = 1 \Big/ \left(\dfrac{1}{C_k} + \dfrac{1}{C_\mathrm{out}}\right) \\ p_k = \dfrac{C_{k(\mathrm{eff})}}{C_\mathrm{out}} \end{cases} . \end{aligned} \tag{7}$$

Substituting (2)-(7) into (1) yields

$$R_\mathrm{out} = \hat{R}_\mathrm{out} + \sum_k R_k p_k \left(2a_k - p_k f_\mathrm{sw} T_{k(\mathrm{eff})}\right) \tag{8}$$

where

$$\begin{cases} \hat{R}_\mathrm{out} = \dfrac{1}{2 f_\mathrm{sw}} \sum\limits_k \dfrac{\hat{a}_k^2}{C_{k(\mathrm{eff})}} \coth\left(\dfrac{T_{k(\mathrm{eff})}}{2\tau_k}\right) \\ \hat{a}_k = a_k - p_k f_\mathrm{sw} T_{k(\mathrm{eff})} \end{cases} \tag{9}$$

in which a_k is the ratio of the transferred charged in phase k to the total delivered charge in a switching cycle. A detailed derivation of (8) is provided in Appendix A. The definition and calculation of a_k can be found in [18].

With ideal input and output, $C_{k(\mathrm{eff})}$ and p_k become $C_{k(\mathrm{eff})} = C_k$ and $p_k = 0$, so that

$$R_\mathrm{out} = \hat{R}_\mathrm{out} = \frac{1}{2 f_\mathrm{sw}} \sum_k \frac{a_k^2}{C_k} \coth\left(\frac{T_{k(\mathrm{eff})}}{2\tau_k}\right) \tag{10}$$

which is the same as has been derived in [22].

III. Model Verification

In this section, a 2-to-1 SC converter prototype is designed to investigate the influence of terminal capacitances on the output impedance quantitatively. The accuracy of the proposed general model is verified by comparing the modeling results with circuit simulations and experimental measurements from 2-to-1 SC converter prototype.

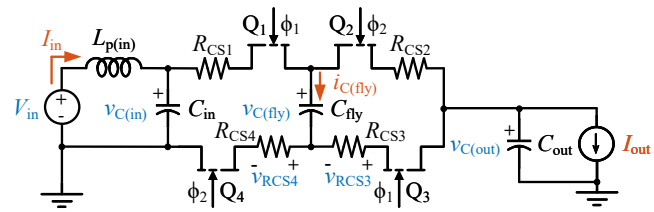


Fig. 5: Schematic drawing of the 2-to-1 SC converter prototype.

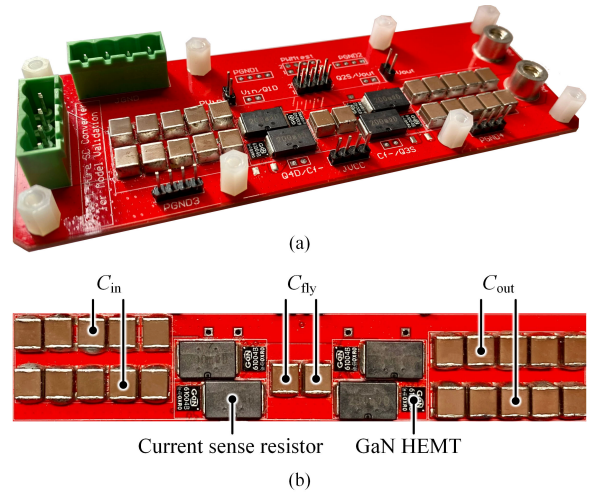


Fig. 6: Photograph of the 2-to-1 SC converter prototype. (a) Overall view. (b) Top view with key components annotated.

A. Experimental Setup

Figures 5 and 6 present the schematic drawing and photograph of the 2-to-1 SC converter prototype for model verification, with the main components listed in Table I. The test condition is $V_\mathrm{in} = 24$ V and $I_\mathrm{out} = 1$ A. The input and output voltages are measured with digital multimeters Keysight 34405A and 34401A, respectively, and the output current I_out is measured by the E-load Rigol DL3031.

For the 2-to-1 SC converter shown in Fig. 6, the topology-dependent parameters in the output impedance model are $C_k = C_\mathrm{fly}$, $R_k = 2\left(R_\mathrm{on} + R_\mathrm{CS}\right) + \mathrm{ESR}_\mathrm{C(fly)}$, $a_k = \frac{1}{2}$, and $T_k = \frac{1}{2 f_\mathrm{sw}}$ $(k = 1, 2)$, where C_fly is the flying capacitance, R_on is the on-state resistance of the GaN HEMT $\mathrm{Q_1}$-$\mathrm{Q_4}$, R_CS is the value of current sense resistors R_CS1-R_CS4, and $\mathrm{ESR}_\mathrm{C(fly)}$ is the ESR of C_fly. The reason why R_CS1-R_CS4 are added in series with the GaN switches will be explained in the following section.

B. Experiment Design Considerations

There are two key considerations to achieve effective model verification:

1) Ensure accurate parameter acquisition. Since the precision of the predicted results is dependent on not only the correctness of the model itself but also the accuracy of the circuit parameters, we should ensure that the circuit parameters will not deviate from the nominal values provided

TABLE I: Component list of the 2-to-1 SC converter prototype

Component	Part number	Parameters
GaN HEMT Q_1-Q_4	GaN Systems GS61004B	100 V, 16 mΩ (@ 25 °C)
Current sense resistor R_{CS1}-R_{CS4}	KOA Speer SLN5TTEDR200D	200 mΩ, 7 W, 75 PPM/°C
Flying capacitor C_{fly}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μF ×8
Input and output capacitors C_{in} and C_{out}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μF ×2-×40*
Gate driver	Analog Devices LTC4440	80 V, high-side
LDO voltage regulator	Texas Instruments LP2985AIM5-6.1/NOPB	2.5-16 V input, 6.1 V output
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky diode

* Measurements are performed with various terminal capacitances.

in the manufacturers' datasheets during the measurement due to temperature variation, voltage bias, etc. There are two categories of variation-prone circuit parameters in the model: a) capacitances: C_{fly}, C_{in}, and C_{out}, and b) resistance: R_{on} and $ESR_{C(fly)}$.

KEMET C2220C474J5GACTU is a Class 1 capacitor with C0G dielectric that can maintain high capacitance stability over a wide range of operating temperature and voltage bias and has extremely low ESR and ESL. Therefore, we select it for C_{fly}, C_{in}, and C_{out}, so that the variation in the capacitances can be minimized and $ESR_{C(fly)}$ can be ignored (i.e. $ESR_{C(fly)} \approx 0$).

The on-state resistance of switching devices can vary significantly due to the changes in operating conditions (e.g. junction temperature, drain-to-source current, gate-to-source voltage, etc.). The on-state resistance of GaN HEMTs is particularly hard to accurately capture due to the dynamic on-state resistance phenomenon [34], [35].

To tackle this challenge, we add a high-precision current sense resistor (KOA Speer SLN5TTEDR200D) in series with each GaN switch to dominate the branch resistance. The current sense resistor can maintain high thermal stability (75 PPM/°C) and has a much higher resistance ($R_{CS} = 200$ mΩ) than the GaN switch ($R_{on} = 16$ mΩ @ 25 °C). As a result, the branch resistance can be stabilized by the current sense resistor against the variation in R_{on}. In addition, the cascaded bootstrap circuit with LDOs [36] is selected to drive the GaN switches since it can ensure stable gate drive voltage V_{drive} and minimize the variation in R_{on} resulting from the change in V_{drive}.

2) Minimize the proportion of switching loss. The proposed output impedance model can only capture the conduction losses and charge sharing losses in the SC converter. Therefore, to achieve effective model verification, we need to ensure that the converter operates in the conduction-loss-dominant condition, and the switching loss takes up only a small proportion of the total loss. Meanwhile, the converter needs to operate above 1 MHz to reach FSL. Therefore, we use GaN switches with small output capacitance and low gate charge and set the external gate resistance as 0 Ω to minimize the overlap loss.

C. Experimental Results

Figs. 7 and 8 show the comparison between the output impedances predicted by the proposed model (Model), simulated by PLECS (Sim.), and measured from the converter prototype (Expt.). Figs. 7(c) and 8(c) present the relative error of the modeling results with respect to the experimental measurements that is calculated by

$$\text{Relative error} = \frac{R_{\text{out(Model)}} - R_{\text{out(Expt.)}}}{R_{\text{out(Expt.)}}} \times 100\% \quad (11)$$

where $R_{\text{out(Model)}}$ and $R_{\text{out(Expt.)}}$ are the output impedance predicted by the model and measured from the prototype, respectively.

As can be seen in Figs. 7 and 8, the modeling results are in excellent agreement with the circuit simulations and the experimental measurements. The relative error of the modeling results with respect to the experimental measurements is less than 8% for various C_{in} and C_{out} within 100 kHz-2 MHz switching frequency range, covering the slow switching limit (SSL) and FSL. This indicates excellent accuracy of the proposed general output impedance model and its applicability in a wide range of switching frequency.

It should be noted that the relative error grows higher when the switching frequency increases. This is mainly due to the increase in the switching loss resulting from higher switching frequency. In addition, the relative error rises dramatically as the switching frequency decreases when C_{in} is small. This results from the undesired oscillation between $L_{p(in)}$ and C_{in}, which will be further explored in Section IV-C.

IV. Effect Analysis of Terminal Capacitances

With the general model derived and verified in Sections II and III, we will use it to explore the effect of finite terminal capacitances on the output impedance of SC converters in this section.

A. Model Approximation by Taylor Expansion

Although the general output impedance model is accurate within a wide range of switching frequency, it can be too complex to provide intuitive engineering insight. The existence of the hyperbolic function $\coth(x)$ makes it hard to handle mathematically. Therefore, to facilitate analysis, we approximate (8) with Taylor expansion to obtain a simplified mathematical form. Inspired by the concepts of SSL and FSL [18], we perform model approximation in the slow and fast switching regions separately, and name the obtained models as *slow switching model (SSM)* and *fast switching model (FSM)*, respectively.

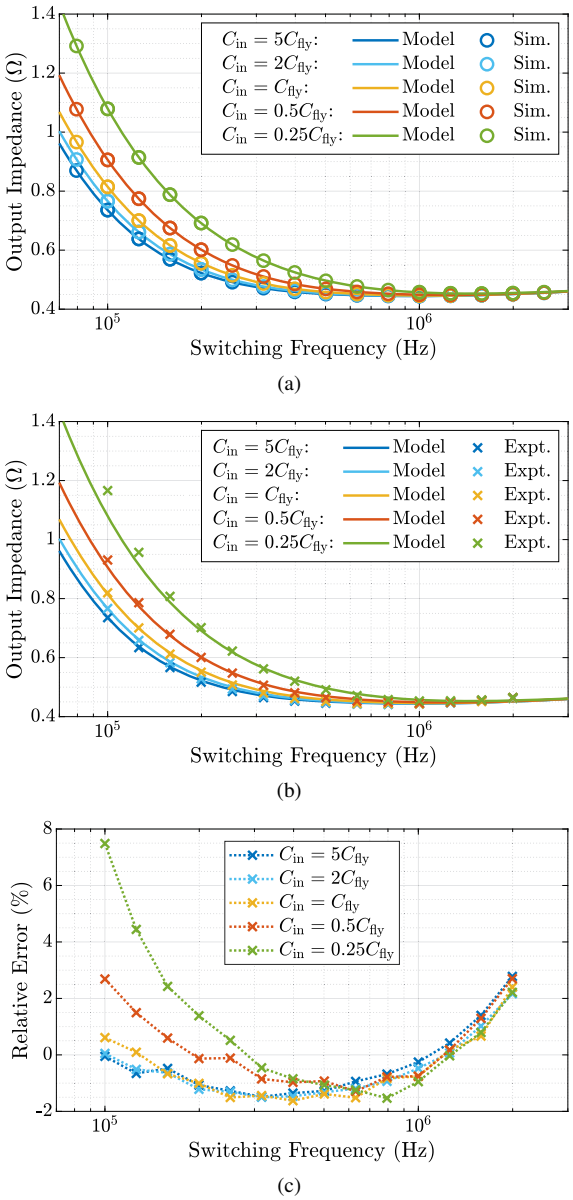


Fig. 7: Output impedance of the SC converter with various C_{in}. ($C_{\mathrm{out}} = 5C_{\mathrm{fly}}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated by PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.). (c) Relative error of modeling results with respect to experimental measurements calculated with (11).

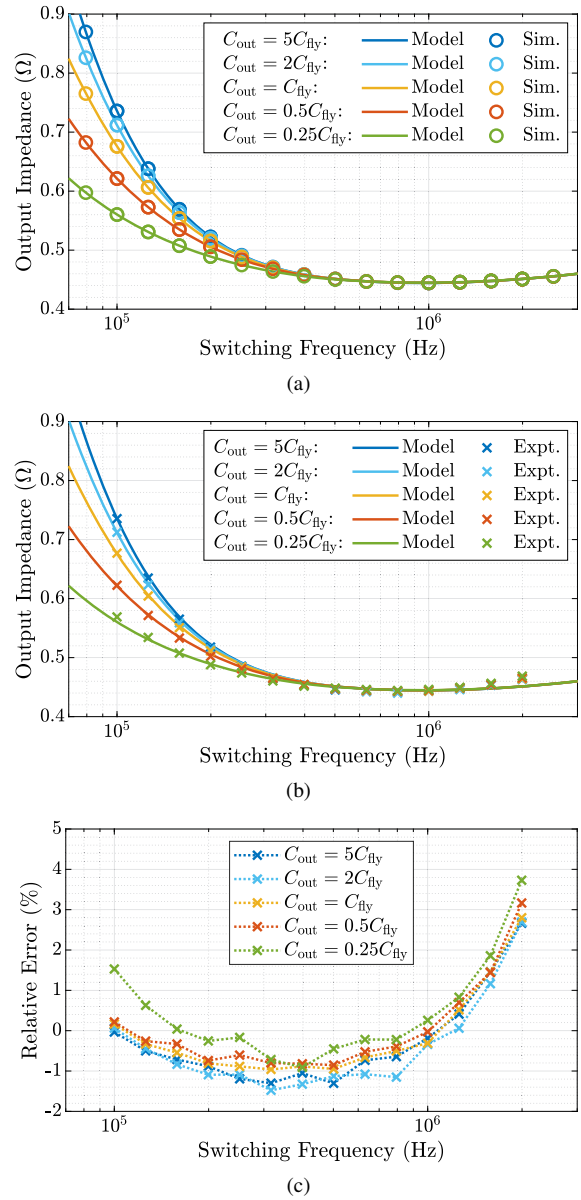


Fig. 8: Output impedance of the SC converter with various C_{out}. ($C_{\mathrm{in}} = 5C_{\mathrm{fly}}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated by PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.). (c) Relative error of modeling results with respect to experimental measurements calculated with (11).

For simplicity, here we perform the approximation to the model of the 2-to-1 SC converter prototype presented in Section III as an example. Note that this approximation technique is applicable to arbitrary SC topologies. To simplify calculation, we set $R_{\mathrm{CS}} = 0\ \Omega$ and assume negligible capacitor ESR and deadtime t_{d}. In the following examples in Sections IV-A and IV-B, $C_{\mathrm{fly}} = 10\ \mu$F, $R_{\mathrm{on}} = 10$ mΩ.

Using Taylor expansion, we can approximate the output impedance model given in (8) for a 2-to-1 SC converter as

$$\begin{cases} R_{\mathrm{SSM}} = \left(b + \dfrac{c}{s}\right) R_{\mathrm{on}}, & s < s_{\mathrm{c}} \\ R_{\mathrm{FSM}} = \left(2 + \dfrac{d}{s^2}\right) R_{\mathrm{on}}, & s \geqslant s_{\mathrm{c}} \end{cases} \tag{12}$$

where

$$\begin{cases} s = 8 f_{\mathrm{sw}} R_{\mathrm{on}} C_{\mathrm{fly}}, \ s_{\mathrm{c}} = \dfrac{1 + k_{\mathrm{in}}/2 \ + k_{\mathrm{out}}}{\sqrt{3}} \\ k_{\mathrm{in}} = \dfrac{C_{\mathrm{fly}}}{C_{\mathrm{in}}}, \ k_{\mathrm{out}} = \dfrac{C_{\mathrm{fly}}}{C_{\mathrm{out}}} \\ b = 2 - \dfrac{(1 + k_{\mathrm{in}}/2\ )^2}{(1 + k_{\mathrm{in}} + k_{\mathrm{out}})^2} - \dfrac{1}{(1 + k_{\mathrm{out}})^2} \\ c = \dfrac{(1 + k_{\mathrm{in}}/2\ )^2}{1 + k_{\mathrm{in}} + k_{\mathrm{out}}} + \dfrac{1}{1 + k_{\mathrm{out}}} \\ d = \dfrac{(1 + k_{\mathrm{in}}/2\ )^2 + 1}{3} \end{cases} \tag{13}$$

TABLE II: Maximum relative errors of the approximated SSM and FSM in (12) with various $C_{\rm in}$ and $C_{\rm out}$

$k_{\rm in}^{-1}$ or $k_{\rm out}^{-1}$	10	7	5	4	3	2	1	0.5	0.25
$C_{\rm in} = k_{\rm in}^{-1} C_{\rm fly}$, $C_{\rm out} = 10C_{\rm fly}$	7.40%	7.27%	7.25%	7.18%	6.91%	7.32%	7.44%	10.6%	15.1%
$C_{\rm out} = k_{\rm out}^{-1} C_{\rm fly}$, $C_{\rm in} = 10C_{\rm fly}$	7.40%	6.89%	6.51%	6.06%	5.84%	4.95%	3.00%	1.52%	0.58%

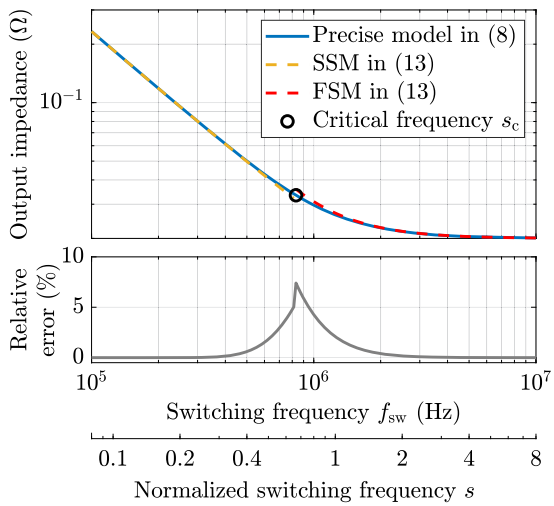


Fig. 9: Comparison between the precise model in (8) and the approximated SSM and FSM in (12). ($C_{\rm in} = C_{\rm out} = 10C_{\rm fly}$)

in which s is a dimensionless product of the switching frequency $f_{\rm sw}$ and the time constant $R_{\rm on}C_{\rm fly}$ and is defined as the normalized switching frequency. Parameter $s_{\rm c}$ is the critical normalized frequency that marks the boundary between SSM and FSM, and $k_{\rm in}$ and $k_{\rm out}$ are the ratios of $C_{\rm fly}$ to $C_{\rm in}$ and $C_{\rm out}$, respectively. The detailed derivation of (12) is given in Appendix B.

Fig. 9 shows the comparison between the precise model given in (8) and the approximated models (SSM and FSM) shown in (12). Table II lists the maximum relative errors of the approximated model with various $C_{\rm in}$ and $C_{\rm out}$. From Fig. 9, we can see that the maximum relative error always appears at the critical frequency $s_{\rm c}$. Table II shows that SSM and FSM can approximate the precise model within 8% relative error except for the cases with extremely small $C_{\rm in}$.

In the slow switching region that ensures complete charge transfer, we have $s \ll 1$ which yields the SSL in (14). When the switching frequency is sufficiently high so that the current through $C_{\rm fly}$ is almost constant in each phase, $s \gg 1$ and therefore yields the FSL in (14).

$$\begin{cases} R_{\rm SSM} \approx R_{\rm SSL} = \dfrac{c}{s} R_{\rm on}, & s \ll 1 \\ R_{\rm FSM} \approx R_{\rm FSL} = 2R_{\rm on}, & s \gg 1 \end{cases} . \tag{14}$$

When the terminal capacitances are sufficiently large so that the input and output can be regarded as constant voltage sources, $k_{\rm in}$ and $k_{\rm out}$ are approximately zero so that we get $R_{\rm SSL} = \frac{1}{4C_{\rm fly} f_{\rm sw}}$ and $R_{\rm FSL} = 2R_{\rm on}$, which is expected and well-known.

B. Effect of Finite Terminal Capacitances

In this section, we first evaluate (12) to analyze the effect of terminal capacitances qualitatively, then perform quantitative analysis with numerical calculations, and finally explore the physical origins for these effects with circuit simulations.

1) Qualitative analysis. In the SSM of (12), when $C_{\rm in}$ becomes smaller, $k_{\rm in}$ increases so that c becomes greater, resulting in higher $R_{\rm SSM}$. Conversely, with smaller $C_{\rm out}$, $k_{\rm out}$ increases so that c becomes smaller, contributing to lower $R_{\rm SSM}$. It is favorable, although counter-intuitive, that decreasing $C_{\rm out}$ can help reduce the output impedance since this will contribute to both higher power density and higher efficiency. But note that this benefit comes at the cost of a larger output voltage ripple. $C_{\rm out}$ should still be sufficiently large to satisfy any ripple constraint.

In the FSM of (12), the coefficient d is only dependent on $k_{\rm in}$ while it is independent of $k_{\rm out}$. This indicates that $C_{\rm out}$ has little effect on $R_{\rm FSM}$. By inspection, we can predict that reducing $C_{\rm in}$ will lead to higher $R_{\rm FSM}$.

2) Quantitative analysis. Figs. 10 and 11 show quantitative comparisons of the output impedance of 2-to-1 SC converters with different terminal capacitances. To generalize the analysis, Figs. 10 and 11 are plotted with the normalized switching frequency s in (13) ($s = 8f_{\rm sw}R_{\rm on}C_{\rm fly}$), with the output impedance normalized to the FSL impedance as $R_{\rm out}/R_{\rm FSL}$ ($R_{\rm FSL} = 2R_{\rm on}$). It can be observed that smaller $C_{\rm in}$ leads to higher output impedance, while the output impedance becomes lower when $C_{\rm out}$ is smaller.

As has been predicted in the qualitative analysis, $C_{\rm out}$ has no influence on the output impedance in the fast switching region. Instead, $C_{\rm in}$ exhibits a greater effect in this region, especially around the knee of the output impedance curve. Since SC converters typically operate around the knee point, $C_{\rm in}$ should be carefully designed to avoid the undesired increase in the output impedance due to insufficient $C_{\rm in}$. These findings are consistent with those from the qualitative analysis and the experimental results presented in Figs. 7 and 8.

In addition, it can be observed in Fig. 7 that $C_{\rm in} = 3C_{\rm fly}$ is sufficient to approximate an ideal input. However, further reduction in $C_{\rm in}$ can cause a significant increase in the output impedance, which harms efficiency. On the contrary, smaller $C_{\rm out}$ can always help reduce the output impedance. Moreover, in the slow switching region, $C_{\rm out}$ exhibits a stronger influence on the output impedance than $C_{\rm in}$. For example, Fig. 10(b) shows that reducing $C_{\rm in}$ to $0.25C_{\rm fly}$ can increase $R_{\rm out}$ by a factor of 1.5, while it is presented in Fig. 11(b) that reducing $C_{\rm out}$ to $0.25C_{\rm fly}$ can decrease $R_{\rm out}$ by a factor of 0.3.

3) Physical origins. Fig. 12 compares the simulated waveforms of the 2-to-1 SC converter with large and small input capacitances, assuming ideal output. Fig. 12 shows that with smaller $C_{\rm in}$, the voltage difference seen by $C_{\rm fly}$ ($V_{\rm C(in)} -$

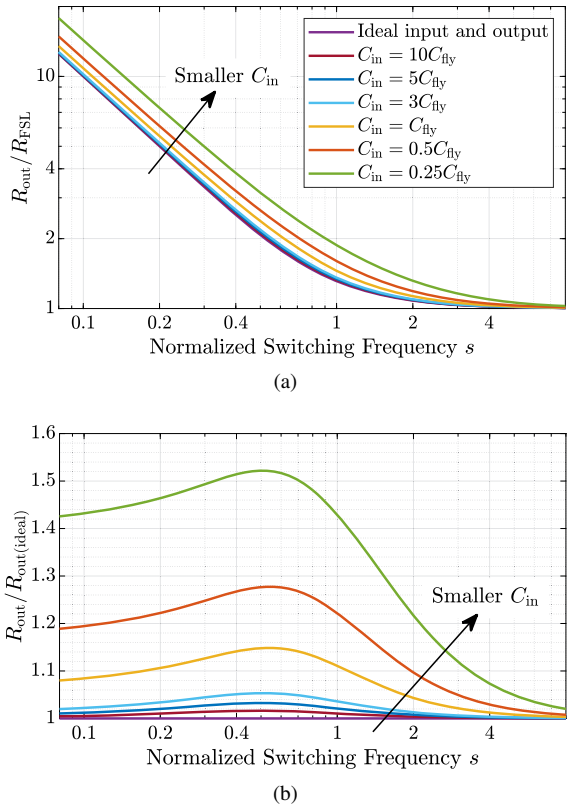


Fig. 10: Effect of C_{in} on output impedance. (Assuming ideal output) (a) Normalized output impedance R_{out}/R_{FSL} with various C_{in}. (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{out(ideal)}$.

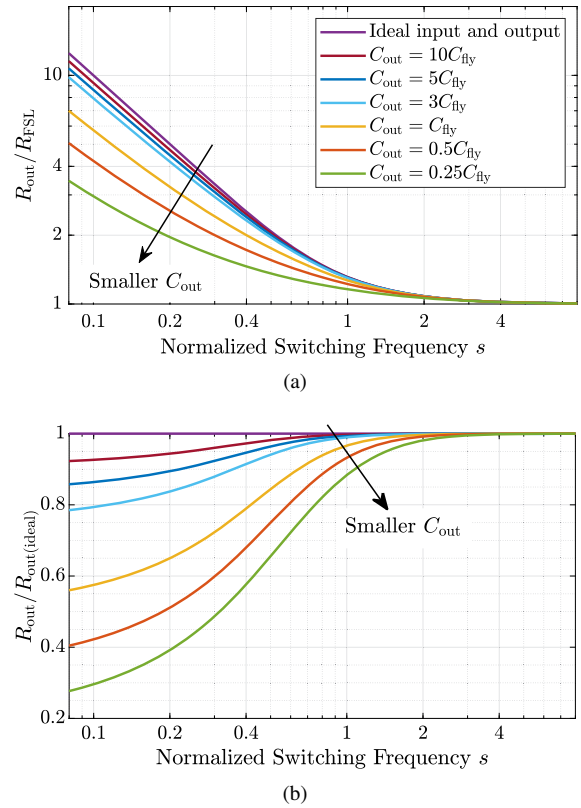


Fig. 11: Effect of C_{out} on input impedance. (Assuming ideal output) (a) Normalized output impedance R_{out}/R_{FSL} with various C_{out}. (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{out(ideal)}$.

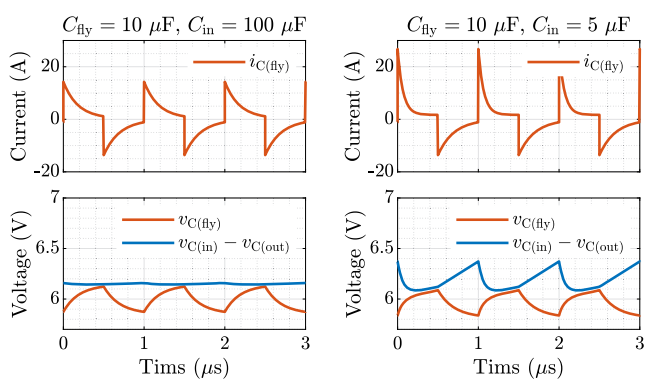


Fig. 12: Comparison of simulated waveforms between large and small C_{in} cases. (Assuming ideal output, $C_{fly} = 10\ \mu F$, $f_{sw} = 1$ MHz, $I_{out} = 5$ A)

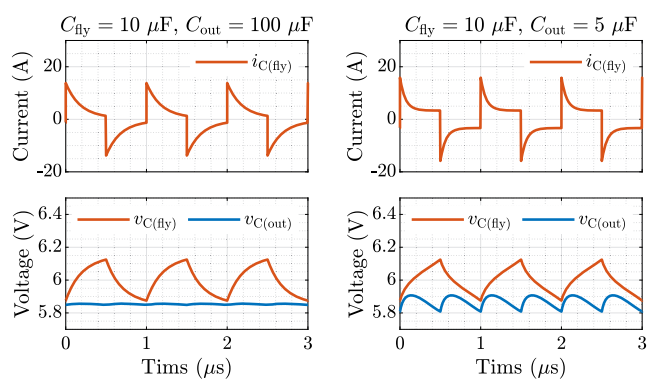


Fig. 13: Comparison of simulated waveforms between large and small C_{out} cases. (Assuming ideal input, $C_{fly} = 10\ \mu F$, $f_{sw} = 1$ MHz, $I_{out} = 5$ A)

TABLE III: Comparison between the RMS and peak-to-peak values of the simulated $i_{C(fly)}$ waveforms between large and small C_{in} cases (Assuming ideal output, $C_{fly} = 10\ \mu F$, $f_{sw} = 1$ MHz, $I_{out} = 5$ A)

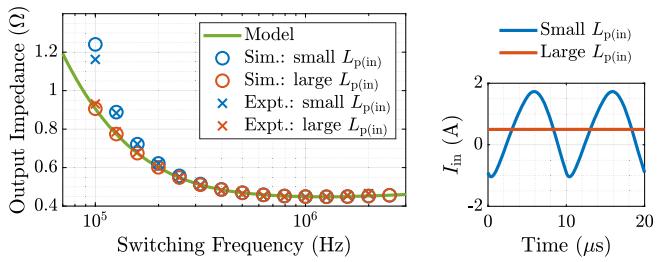
$i_{C(fly)}$ \ C_{in}	100 μF	10 μF	5 μF
RMS value	6.18 A	6.49 A	6.84 A
Peak-to-peak value	28.6 A	34.0 A	40.6 A

TABLE IV: Comparison between the RMS and peak-to-peak values of the simulated $i_{C(fly)}$ waveforms between large and small C_{out} cases (Assuming ideal input, $C_{fly} = 10\ \mu F$, $f_{sw} = 1$ MHz, $I_{out} = 5$ A)

$i_{C(fly)}$ \ C_{out}	100 μF	10 μF	5 μF
RMS value	6.07 A	5.95 A	5.81 A
Peak-to-peak value	28.2 A	30.7 A	32.7 A

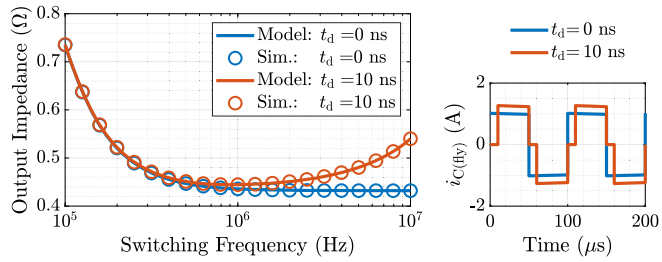
$V_{C(out)} - V_{C(fly)}$) becomes much larger. This results in a higher peak value of $i_{C(fly)}$ in the case 1 shown in Fig. 4. As a result, the RMS value of $i_{C(fly)}$ becomes higher when C_{in} is smaller, which leads to greater loss and higher output impedance.

Fig. 13 presents a similar comparison of output impedance between the 2-to-1 SC converter with large and small output capacitances, assuming ideal input. As listed in Table IV, the RMS value of $i_{C(fly)}$ becomes lower with smaller C_{out}. This is because the output voltage ($V_{C(out)}$) is able to follow $V_{C(fly)}$ more rapidly when C_{out} is smaller. Consequently, $i_{C(fly)}$ drops



(a) (b)

Fig. 14: Effect of $L_{p(in)}$ on the output impedance of the 2-to-1 SC converter prototype. ($C_{in} = 0.5C_{fly}$, $C_{out} = 5C_{fly}$) (a) Output impedance with small and large L_{in}. (b) Simulated waveforms of I_{in} with small and large L_{in}. ($f_{sw} = 100$ kHz)



(a) (b)

Fig. 15: Effect of deadtime on the output impedance of the 2-to-1 SC converter prototype. ($C_{in} = C_{out} = 5C_{fly}$) (a) Output impedance with and without deadtime. (b) Simulated waveforms of $i_{C(fly)}$ with and without deadtime. ($f_{sw} = 10$ MHz)

faster and thus has a lower RMS value, which contributes to less loss and lower output impedance.

In summary, reducing C_{in} exacerbates the imbalance of capacitor voltages between the two cases of Fig. 4, which increases the RMS value of $i_{C(fly)}$. On the contrary, decreasing C_{out} accelerates the charge sharing processes, thus resulting in a lower RMS value of $i_{C(fly)}$. This accounts for the opposite effects of C_{in} and C_{out} on the output impedance of SC converters. Experimental corroboration of the above simulation analyses and theoretical findings is provided in Appendix C.

C. Other Practical Considerations

1) Resonance between $L_{p(in)}$ and C_{in}. As shown in Fig. 14(a), it is observed both in simulation (Sim.) and experiment (Expt.) that, with low C_{in}, there will be an undesired increase in the output impedance in the slow switching region when $L_{p(in)}$ is small. This phenomenon is due to the resonance between $L_{p(in)}$ and C_{in}, and can be explained as follows.

As C_{in} becomes smaller and smaller, the resonant frequency of $L_{p(in)}$ and C_{in}, which can be given as $f_{r(in)} = \frac{1}{2\pi\sqrt{L_{p(in)}C_{in}}}$, gradually decreases. When the switching frequency approaches $f_{r(in)}$, the input current I_{in} will start to oscillate largely between positive and negative values, as illustrated in Fig. 14(b). Such oscillation can dramatically increase the input voltage ripple and therefore augment the voltage difference seen by C_{fly}, thus leading to higher RMS value of $i_{C(fly)}$ and higher output impedance.

It is worth noting that the above analysis is only an example of how the $L_{p(in)}$-C_{in} resonance can affect the input voltage ripple and output impedance of SC converters. Realistic input impedance networks can be more complex and can affect not only the performance but also the stability of power converters. Detailed effect analysis of the resonance between the source impedance and C_{in} is out of the scope of this paper and can be a good research topic for future works.

2) Effect of deadtime. As shown in Fig. 15(a), at very high switching frequency (i.e. beyond several MHz), a practical deadtime t_d of several ns can lead to an unexpected increase in output impedance. This effect can be accurately captured by the proposed model by introducing the effective duration of conduction given in (7).

As illustrated in Fig. 15(b), the average value of $i_{C(fly)}$ in each phase should be the same no matter how long the deadtime is. However, with longer deadtime, the conduction duration of $i_{C(fly)}$ will become shorter, which leads to a higher RMS value and thus higher conduction loss. This indicates that deadtime is also a factor that impedes increasing f_{sw} in practice, apart from higher switching loss.

3) Multiphase interleaving. As discussed in [21], [27], for integrated SC converters, there is usually no penalty for multiphase interleaving. In multiphase interleaved SC converters, the flying capacitor(s) of one SC converter unit can serve as the terminal capacitor(s) for other units. Therefore, with sufficient interleaved phases, no explicit terminal capacitors are needed so that the majority of die area can be used to implement the flying capacitance.

The application of the proposed output impedance model to multiphase interleaved SC converters is out of the scope of this paper and can be a worthwhile topic for future studies. Discussions on how to capture the effect of interleaving can be found in [21].

D. Design Guidelines

- Size of the input capacitance: Since an insufficient input capacitance can increase the output impedance and harm overall efficiency, C_{in} should be sufficiently large to ensure an approximately ideal input behavior. In particular, when Class 2 capacitors are used as the input capacitor, special attention should be paid to ensure that C_{in} is sufficient, since Class 2 capacitors suffer from DC derating with applied input voltage.
- Size of the output capacitance: The output capacitance can be appropriately reduced to achieve both smaller physical size and lower output impedance (i.e. both higher power density and higher efficiency). However, C_{out} should still be sufficiently large to satisfy the ripple constraint on the output voltage.
- Other practical considerations: 1) In the slow switching region, the resonance between $L_{p(in)}$ and C_{in} can cause an undesired increase in the output impedance. This can be avoided by ensuring sufficient C_{in} or operating at a higher switching frequency. 2) At very high switching frequency (i.e. beyond several MHz), a practical deadtime

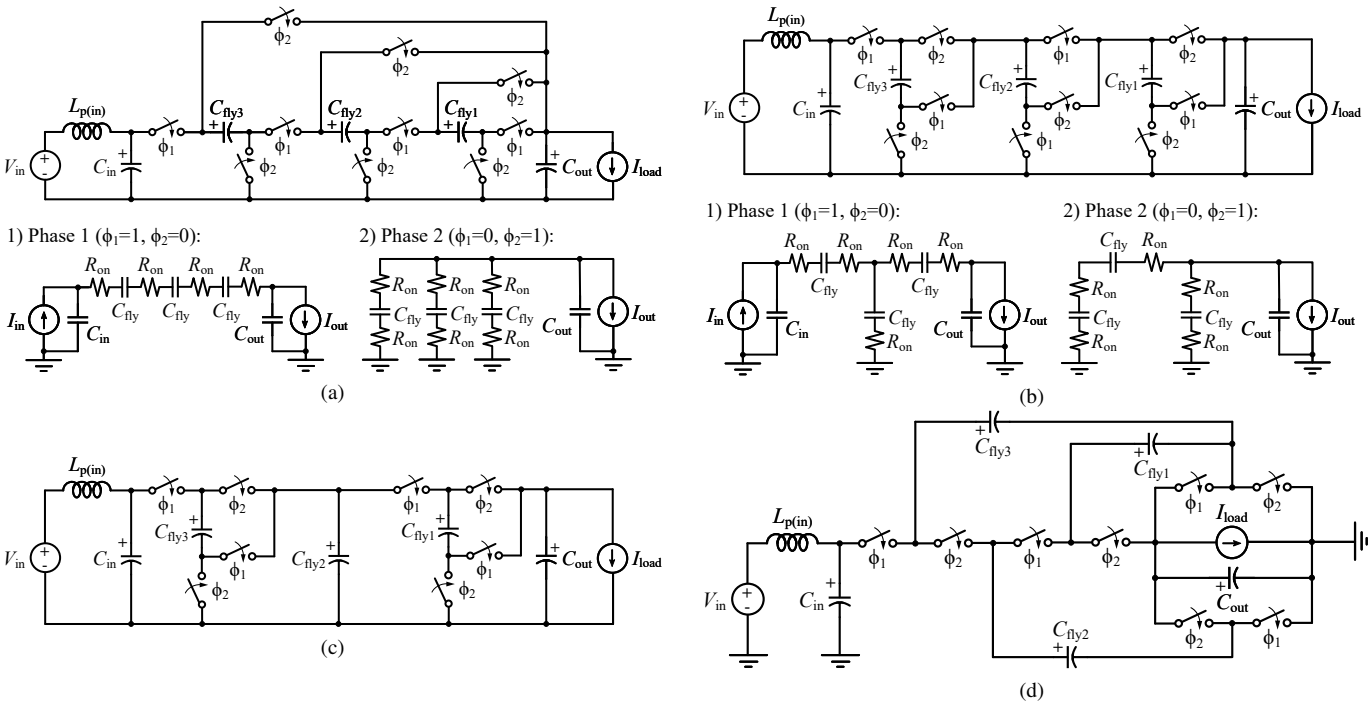


Fig. 16: Common SC topologies. (a) 4-to-1 series–parallel topology and its equivalent circuit in each phase. (b) 5-to-1 Fibonacci topology and its equivalent circuit in each phase. (c) 4-to-1 doubler topology. (d) 4-to-1 Dickson topology.

$t_{\rm d}$ of several nano-seconds can lead to a considerable increase in the output impedance and therefore can no longer be neglected in the analysis and design of SC converters.

Further quantitative optimizations can be performed to find the best combination of $C_{\rm fly}$, $C_{\rm in}$, and $C_{\rm out}$ to achieve the lowest output impedance within the given physical space limits and voltage ripple constraints.

V. Application to Arbitrary SC Topologies

In this section, we apply the proposed modeling and analysis methodology to four commonly-used SC topologies: series–parallel, Fibonacci, doubler, and Dickson topologies, as shown in Fig. 16. These four examples are provided here to demonstrate the applicability of this model to arbitrary SC topologies. The set of converters considered in this section is limited to two-phase SC converters operating at 50% duty cycle. In the following examples, for simplicity, all flying capacitors have the same capacitance $C_{\rm fly} = 10$ μF, and all switching devices have the same on-state resistance $R_{\rm on} = 10$ mΩ.

A. Model Application to Arbitrary SC Topologies

As has been mentioned in Section II-A, the circuit model shown in Fig. 4 can capture arbitrary SC topologies with suitable topology-dependent parameters. Therefore, the key step of applying the proposed model to an arbitrary SC topology is to obtain the equivalent capacitance C_k and equivalent resistance R_k in each phase. There are two cases: a) the simple case where C_k and R_k can be directly acquired by inspection, and b) the general case where the model parameters have to be carefully derived.

1) Simple case. Apart from the 2-to-1 SC topology, the series–parallel topology is also an example of the simple case. Take the 4-to-1 series–parallel topology illustrated in Fig. 16(a) as an example—the model parameters of the series phase (i.e. phase 1) are $C_1 = \frac{1}{3}C_{\rm fly}$ and $R_1 = 4R_{\rm on}$, and those of the parallel phase (i.e. phase 2) are $C_2 = 3C_{\rm fly}$ and $R_2 = \frac{2}{3}R_{\rm on}$, which can be obtained from the equivalent circuits shown in Fig. 16(a) by inspection.

2) General case. In more general cases, C_k and R_k cannot be directly obtained by inspection from the equivalent circuits but have to be carefully derived according to the invariance of the SSL and FSL output impedance.

On the one hand, with ideal input and output, the asymptotic SSL and FSL output impedances of two-phase SC converters have been given in [18] as

$$\begin{cases} R_{\rm SSL} = \dfrac{1}{f_{\rm sw}} \displaystyle\sum_{i\in{\rm caps}} \dfrac{(a_{{\rm c},i})^2}{C_{{\rm fly},i}} \\ R_{\rm FSL} = 2 \displaystyle\sum_{i\in{\rm switches}} R_{{\rm on},i}(a_{{\rm r},i})^2 \end{cases} \tag{15}$$

in which $C_{{\rm fly},i}$ is the value of flying capacitor i, $R_{{\rm on},i}$ is the on-state resistance of switch i, and $a_{{\rm c},i}$ and $a_{{\rm r},i}$ are the charge multipliers of capacitor i and switch i, respectively.

On the other hand, according to the proposed model, the output impedance of a SC converter with ideal input and output is given by (10). By performing the model approximation introduced in Section IV-A, the asymptotic SSL and FSL

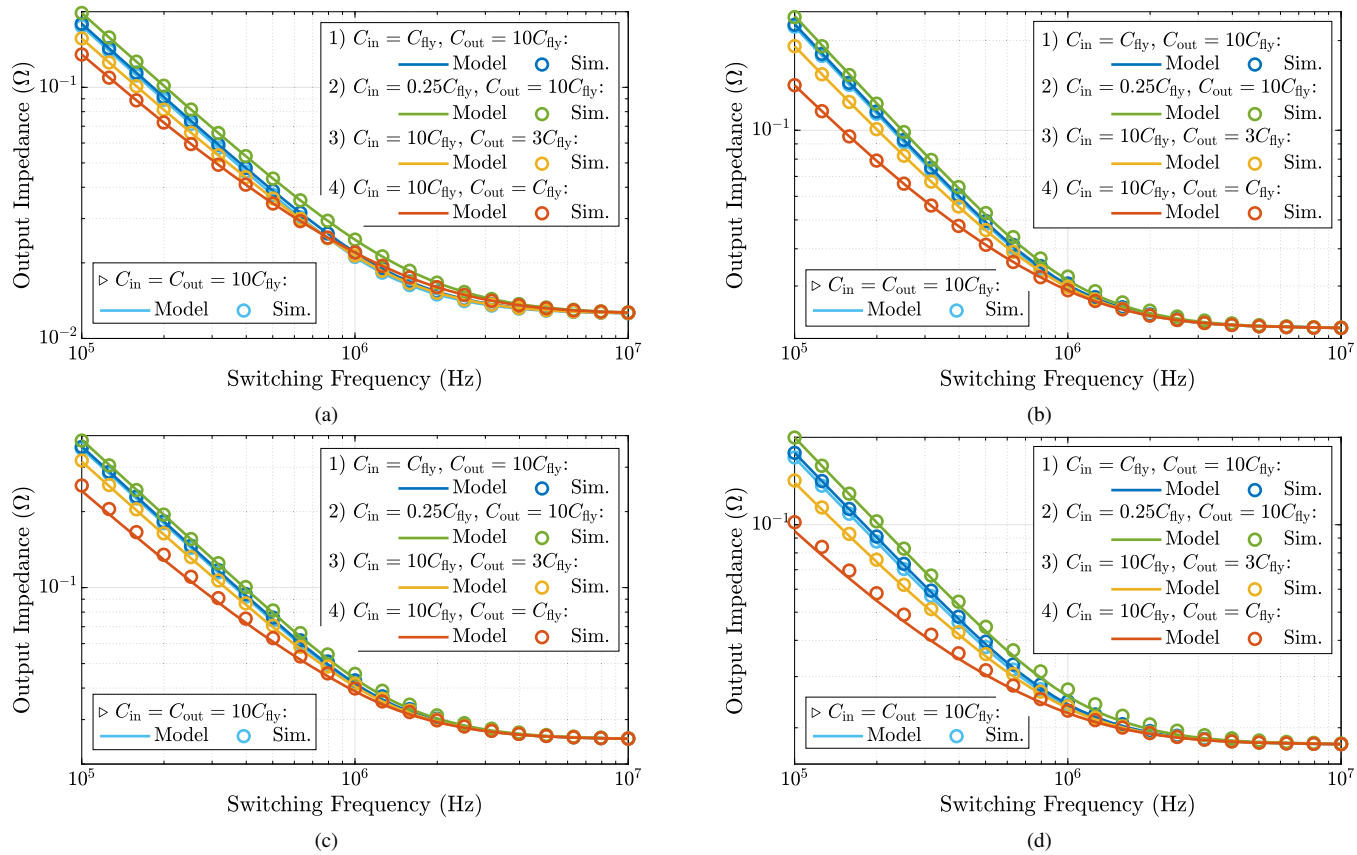


Fig. 17: Output impedance of common SC topologies with various terminal capacitances and comparison between modeling (Model) and simulation (Sim.) results. (a) 4-to-1 series–parallel topology. (b) 5-to-1 Fibonacci topology. (c) 4-to-1 doubler topology. (d) 4-to-1 Dickson topology.

output impedances of (10) can be obtained as

$$\begin{cases} R_{\mathrm{SSL}} = \dfrac{1}{2f_{\mathrm{sw}}} \sum\limits_k \dfrac{a_k^2}{C_k} \\ R_{\mathrm{FSL}} = 2\sum\limits_k R_k a_k^2 \end{cases}. \tag{16}$$

The SSL and FSL output impedances in (15) and (16) should be the same, and therefore we get

$$\begin{cases} \sum\limits_k \dfrac{a_k^2}{C_k} = 2\sum\limits_{i\in\mathrm{caps}} \dfrac{(a_{\mathrm{c},i})^2}{C_{\mathrm{fly},i}} \\ \sum\limits_k R_k a_k^2 = \sum\limits_{i\in\mathrm{switches}} R_{\mathrm{on},i}(a_{\mathrm{r},i})^2 \end{cases}. \tag{17}$$

Splitting (17) into each phase yields

$$\begin{cases} C_k = a_k^2 \Big/ \left(\sum\limits_{i\in\mathrm{caps}} \dfrac{(a_{\mathrm{c},i})^2}{C_{\mathrm{fly},i}} \right) \\ R_k = \dfrac{1}{a_k^2} \sum\limits_{i\in\mathrm{switches}} \delta_{i,k} R_{\mathrm{on},i}(a_{\mathrm{r},i})^2 \end{cases} \tag{18}$$

where $\delta_{i,k}$ equals 1 when switch i is ON in phase k and equals 0 when it is OFF in phase k.

Here, take the 5-to-1 Fibonacci converter illustrated in Fig. 16(b) as an example—we can obtain the model parameters as $C_1 = \frac{2}{3}C_{\mathrm{fly}}$, $C_2 = \frac{3}{2}C_{\mathrm{fly}}$, $R_1 = \frac{11}{4}R_{\mathrm{on}}$, and $R_2 = \frac{16}{9}R_{\mathrm{on}}$. With the C_k and R_k values, we can calculate the output impedance of SC converters with ideal input and output by substituting (18) into (10).

To take the effect of finite C_{in} into consideration, we need to make further modification to C_1 (i.e. the C_k value in case 1 of Fig. 4). Denote the charge multiplier of C_{in} as $a_{\mathrm{c,in}}$, which is defined as the ratio of the charge transferred in C_{in} in one phase to the total charge delivered to the output during a full switching period. For two-phase SC converters operating at 50% duty cycle, the charge transferred in C_{in} in one phase is

$$q_{\mathrm{c,in}} = \frac{T}{2} I_{\mathrm{in}} = \frac{T}{2}\left(\frac{n}{m} I_{\mathrm{out}}\right) = \frac{n}{2m} q_{\mathrm{out}}. \tag{19}$$

Thus, $a_{\mathrm{c,in}}$ can be obtained by inspection as

$$a_{\mathrm{c,in}} = \frac{n}{2m}. \tag{20}$$

Similar to the flying capacitors, the contribution of the input capacitor to the SSL output impedance is proportional to $a_{\mathrm{c,in}}^2/C_{\mathrm{in}}$ which has the same mathematical form of R_{SSL} in (15). Therefore, compared to the situation with ideal input, due to the existence of finite C_{in}, the contribution of phase 1 (case 1 in Fig. 4) to R_{SSL} is increased by

$$f_1 = 1 + \left(\frac{a_{\mathrm{c,in}}^2}{C_{\mathrm{in}}}\right) \Bigg/ \left(\sum_{i\in\mathrm{caps}} \frac{(a_{\mathrm{c},i})^2}{C_{\mathrm{fly},i}} \right). \tag{21}$$

This means that we can incorporate the effect of C_{in} in the model by modifying the C_1 in (18) with the factor f_1 as

$$C_1' = \frac{C_1}{f_1} \tag{22}$$

while still mathematically assuming ideal input in the calculation. Note that here we do not assume $C_{\rm in}$ to be physically infinite but only introduce a mathematical simplification. Additionally, note that since $C_{\rm in}$ is hard-charged in phase 1 and soft-charged [37] by $L_{\rm p(in)}$ in phase 2, it only leads to a greater contribution of phase 1 to $R_{\rm SSL}$ but has no influence on the contribution of phase 2 to $R_{\rm SSL}$, which means only C_1 needs to be modified while C_2 does not.

To sum up, there are four steps to apply the proposed model to arbitrary SC topologies:

i) calculate the model parameters C_k and R_k with (18),

ii) modify C_1 with the factor f_1 given in (21) as (22),

iii) substitute C_1' and C_2 into the case 2 of (3) to calculate $C_{k(\rm eff)}$ and p_k for each phase, and

iv) substitute $C_{k(\rm eff)}$, p_k and R_k into (8), and calculate $R_{\rm out}$.

Fig. 17 presents the output impedance of the four SC topologies shown in Fig. 16 with various terminal capacitances. The comparison between modeling and simulation results in Fig. 17 demonstrates the accuracy of the proposed output impedance model in different SC topologies with various terminal capacitances. Note that the proposed output impedance model is widely applicable to arbitrary SC topologies with practical $C_{\rm in}$ and $C_{\rm out}$ values but can be inaccurate in extreme scenarios that are not usual in practical applications, such as when $C_{\rm out}$ is less than $C_{\rm fly}$.

B. Effect of Terminal Capacitances

As can be observed in Fig. 16, qualitatively speaking, the terminal capacitances exhibit the same effects on output impedance in these common SC topologies as in the 2-to-1 SC converter analyzed in Section IV—the insufficiency of $C_{\rm in}$ leads to higher output impedance while smaller $C_{\rm out}$ helps reduce output impedance.

Quantitatively speaking, we can notice that $C_{\rm out}$ is more influential in the slow switching region while $C_{\rm in}$ has a stronger effect at higher frequency around the knee of the output impedance curve.

It can also be observed that the effect of $C_{\rm in}$ is weaker in these four SC topologies in comparison with the 2-to-1 SC converter. In the four SC topologies shown in Fig. 17, the output impedance with $C_{\rm in} = C_{\rm fly}$ is very close to that with $C_{\rm in} = 10C_{\rm fly}$. SC topologies with higher conversion ratio generally have smaller equivalent capacitance (C_k) in the phase where the input terminal is connected to the source (i.e. case 1 in Fig. 4). Given that the output impedance is dependent on the series capacitance of $C_{\rm in}$ and C_k, $C_{\rm in}$ needs to be smaller to make the same impact on the output impedance of SC topologies with higher conversion ratio. This is a favorable feature which means that smaller $C_{\rm in}$ can be sufficient to ensure an approximately ideal input behavior in SC converters with higher conversion ratio.

VI. Conclusions

This paper proposes a general modeling and analysis methodology that is able to characterize the effect of finite terminal capacitances on the output impedance of SC converters. A general output impedance model is derived and verified by circuit simulations and experimental measurements from a 2-to-1 SC converter prototype with less than 8% relative error. It is revealed that larger $C_{\rm in}$ is favorable for efficiency improvement. On the contrary, smaller $C_{\rm out}$ can help reduce output impedance, which contributes to both higher efficiency and higher power density, although $C_{\rm out}$ should still be sufficiently large to satisfy the ripple constraint on the output voltage. In addition, $C_{\rm out}$ is quantitatively more influential in the slow switching region while $C_{\rm in}$ has a stronger effect on output impedance in the fast switching region, especially around the knee of the output impedance curve where SC converters typically operate. Finally, we demonstrate the applicability of the proposed modeling and analysis methodology to arbitrary SC topologies with four examples of commonly-used SC converters.

This work provides an analytical tool for future investigations, such as design optimizations of SC converters with physical space limits and voltage ripple constraints.

Appendix A
Derivation of the General Output Impedance Model

Denote

$$\begin{cases} \hat{i}_k\left(t\right) = \hat{I}_{0k} e^{-\frac{t}{\tau_k}} \\ \hat{I}_{0k} = I_{0k} - I_{\rm fk} \end{cases} \tag{23}$$

and

$$\hat{q}_k = \int_0^{T_{k(\rm eff)}} \hat{i}_k\left(t\right) dt = \hat{I}_{0k}\tau_k \left(1 - e^{-\frac{T_{k(\rm eff)}}{\tau_k}}\right). \tag{24}$$

Then

$$i_k = \hat{i}_k + I_{\rm fk} \tag{25}$$

so that the transferred charge in phase k can be calculated as

$$q_k = \int_0^{T_{k(\rm eff)}} i_k\left(t\right) dt = \hat{q}_k + I_{\rm fk} T_{k(\rm eff)}. \tag{26}$$

On the other hand, q_k and $I_{\rm out}$ can be expressed as

$$\begin{cases} q_k = a_k q_{\rm out} \\ I_{\rm out} = f_{\rm sw} q_{\rm out} \end{cases} \tag{27}$$

where $q_{\rm out}$ is the total transferred charge to the output in a switching cycle.

Substituting (6) and (27) into (26) yields the relationship between $\hat{q}_k$ and $q_{\rm out}$ as

$$\hat{q}_k = \hat{a}_k q_{\rm out} \tag{28}$$

in which the coefficient $\hat{a}_k$ has been given in (9).

Substituting (23) and (28) into (24) yields

$$\hat{I}_{0k} = \frac{\hat{a}_k q_{\rm out}}{\tau_k \left(1 - e^{-\frac{T_{k(\rm eff)}}{\tau_k}}\right)}. \tag{29}$$

Denote

$$\hat{E}_k = \int_0^{T_{k(\rm eff)}} R_k \hat{i}_k^2\left(t\right) dt = \frac{R_k \hat{I}_{0k}^2 \tau_k}{2} \left(1 - e^{-\frac{2T_{k(\rm eff)}}{\tau_k}}\right). \tag{30}$$

Then substituting (27) and (29) into (30) yields the expression of $\hat{R}_{\text{out}}$ that has been given in (9) as

$$\hat{R}_{\text{out}} = \frac{f_{\text{sw}} \sum_k \hat{E}_k}{I_{\text{out}}^2} = \frac{1}{2f_{\text{sw}}} \sum_k \frac{\hat{a}_k^2}{C_{k(\text{eff})}} \coth\left(\frac{T_{k(\text{eff})}}{2\tau_k}\right). \tag{31}$$

Substituting (25) and (30) into (3) yields

$$E_k = \hat{E}_k + R_k I_{\text{f}k} \left(2\hat{q}_k + I_{\text{f}k} T_{k(\text{eff})}\right). \tag{32}$$

Additively combing (32) over all phases and substituting the summation into (1) and (2) yields the final expression of R_{out} that has been given in (8) as

$$\begin{aligned} R_{\text{out}} &= \frac{f_{\text{sw}} \sum_k E_k}{I_{out}^2} \\ &= \frac{f_{\text{sw}} \sum_k \hat{E}_k}{I_{out}^2} + \frac{f_{\text{sw}} \sum_k R_k I_{\text{f}k} \left(2\hat{q}_k + I_{\text{f}k} T_{k(\text{eff})}\right)}{I_{out}^2} \\ &= \hat{R}_{\text{out}} + \sum_k R_k p_k \left(2a_k - p_k f_{\text{sw}} T_{k(\text{eff})}\right). \end{aligned} \tag{33}$$

Appendix B
Model Approximation by Taylor Expansion

By Taylor expansion, the hyperbolic function $\coth(x)$ $(x > 0)$ can be approximated as

$$\coth(x) \approx \begin{cases} \frac{1}{x} + \frac{x}{3}, & 0 < x \leqslant \sqrt{3} \\ 1, & x > \sqrt{3} \end{cases}. \tag{34}$$

For simplicity, here we consider a two-phase SC converter with 50% duty ratio and negligible deadtime (i.e. $T_{1(\text{eff})} = T_{2(\text{eff})} = \frac{1}{2f_{\text{sw}}}$). Substituting (34) into (8) yields the contribution of phase k $(k = 1,\ 2)$ to R_{out} as

$$\begin{cases} 2R_k \left[p_k \left(a_k - \frac{p_k}{4}\right) + \frac{\hat{a}_k^2}{4f_{\text{sw}}\tau_k}\right], & 0 < 4f_{\text{sw}}\tau_k < \frac{1}{\sqrt{3}} \\ 2R_k \left[a_k^2 + \frac{1}{3} \cdot \frac{\hat{a}_k^2}{(4f_{\text{sw}}\tau_k)^2}\right], & 4f_{\text{sw}}\tau_k \geqslant \frac{1}{\sqrt{3}} \end{cases}. \tag{35}$$

Substituting the topology-dependent parameters mentioned in Section III-B and additively combing the components in all phases yields the SSM and FSM for the 2-to-1 SC converter that has been given in (12) and (13).

Appendix C
Experimental Corroboration for the Effect Analysis of Finite Terminal Capacitances

To corroborate the theoretical findings in Section IV-B, this appendix presents and compares three sets of simulated and experimental waveforms shown in Figs. 18-20 with different C_{in} and C_{out} values. The experimental waveforms were measured from the hardware prototype presented in Figs. 5 and 6. Current sense resistor voltages v_{RCS3} and v_{RCS4} were measured to obtain the current through the flying capacitor $i_{\text{C(fly)}}$ as

$$i_{\text{C(fly)}} = \frac{-v_{\text{RCS3}} + v_{\text{RCS4}}}{R_{\text{CS}}}. \tag{36}$$

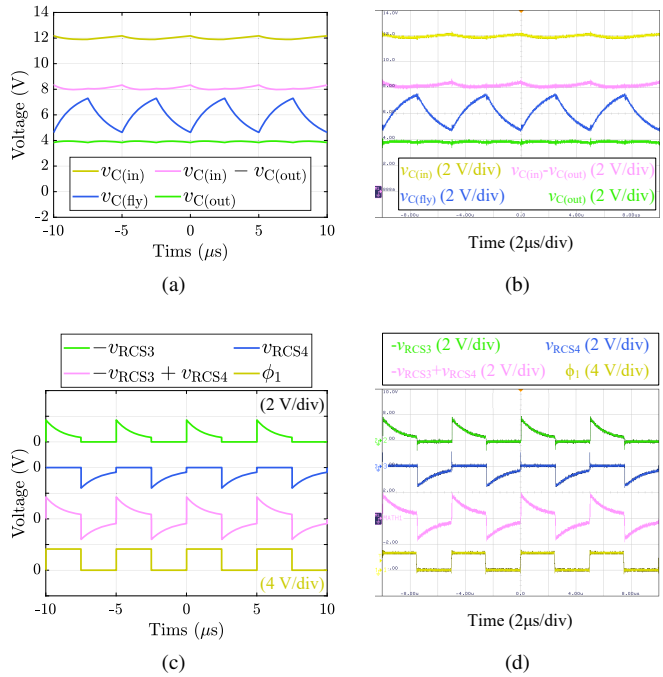


Fig. 18: Comparison between simulated and experimental waveforms when $C_{\text{in}} = C_{\text{out}} = 5C_{\text{fly}}$. (a) Simulated capacitor voltage waveforms. (b) Experimental capacitor voltage waveforms. (c) Simulated voltage waveforms across current sense resistors. (d) Experimental voltage waveforms across current sense resistors.

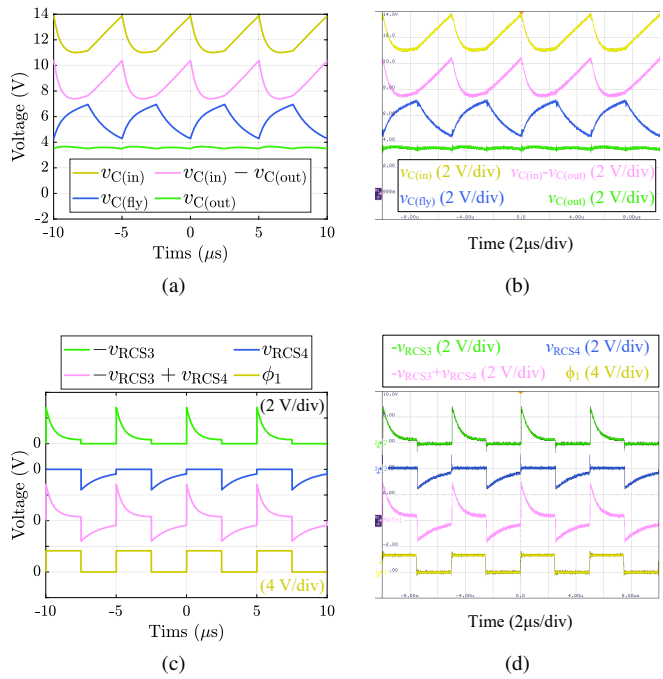


Fig. 19: Comparison between simulated and experimental waveforms when $C_{\text{in}} = 0.5C_{\text{fly}}$, $C_{\text{out}} = 5C_{\text{fly}}$. (a) Simulated capacitor voltage waveforms. (b) Experimental capacitor voltage waveforms. (c) Simulated voltage waveforms across current sense resistors. (d) Experimental voltage waveforms across current sense resistors.

As can be seen in Figs. 18-20, the simulated and experimental waveforms are in excellent agreement. In addition, the waveforms presented in Figs. 18-20 qualitatively match

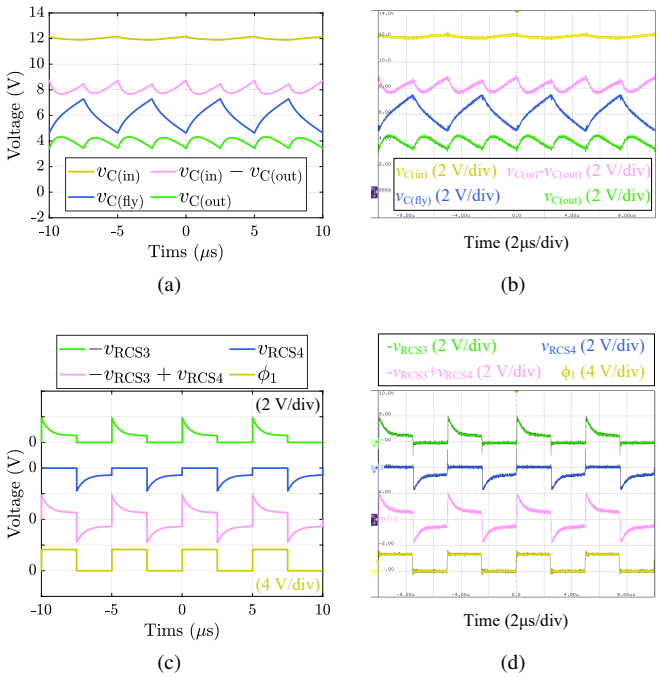


Fig. 20: Comparison between simulated and experimental waveforms when $C_{\text{in}} = 5C_{\text{fly}}$, $C_{\text{out}} = 0.5C_{\text{fly}}$. (a) Simulated capacitor voltage waveforms. (b) Experimental capacitor voltage waveforms. (c) Simulated voltage waveforms across current sense resistors. (d) Experimental voltage waveforms across current sense resistors.

TABLE V: Comparison between the RMS and peak-to-peak values of the simulated (Sim.) and experimental (Expt.) $i_{\text{C(fly)}}$ waveforms with different C_{in} and C_{out} values

$C_{\text{in}}/C_{\text{fly}}$		5	0.5	5
$C_{\text{out}}/C_{\text{fly}}$		5	5	0.5
		(Fig. 18)	(Fig. 19)	(Fig. 20)
RMS value of $i_{\text{C(fly)}}$	Sim.	4.40 A	4.73 A	4.33 A
	Expt.	4.48 A	4.82 A	4.39 A
Peak-to-peak value of $i_{\text{C(fly)}}$	Sim.	16.5 A	22.1 A	18.4 A
	Expt.	19.1 A	23.8 A	20.7 A

those in Figs. 12 and 13. The comparison between Fig. 18 and Fig. 19 shows that a smaller C_{in} leads to a larger voltage difference seen by C_{fly} ($V_{\text{C(in)}} - V_{\text{C(out)}} - V_{\text{C(fly)}}$), which results in higher RMS and peak-to-peak values of $i_{\text{C(fly)}}$ as listed in Table V and thus higher output impedance. Similarly, the comparison between Fig. 18 and Fig. 20 shows that the output voltage ($V_{\text{C(out)}}$) is able to follow $V_{\text{C(fly)}}$ when C_{out} is smaller. As a results, $i_{\text{C(fly)}}$ drops faster and thus has a lower RMS value as listed in Table V, which contributes to less power loss and lower output impedance.

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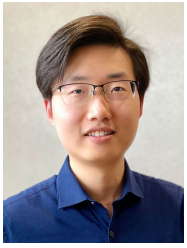

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