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Summary

A compact low-cost large-scale digitizing system for spark chambers has been developed. This system uses a single clocked scaler and a high-speed integrated-circuit memory. The number of words of memory required is equal to the sum of the number of sparks expected in all the chamber gaps plus the number of start fiducial pulses expected (one per transducer channel). Each magnetostrictive transducer is assigned certain addresses in the memory. As pulses arrive from the sensors, the current contents of the scaler are stored in the appropriate preassigned addresses of the memory.

To avoid synchronization problems, a Gray-code scaler is used. The memory is made of 16-bit integrated-circuit scratch pad memory elements. The system could be operated with the clock frequencies of up to 40 MHz. The storage capacity of the system is expandable. This system is compared with other known systems.

Introduction

The function of a spark chamber digitizing system is to produce data which represent the positions of sparks in a spark-chamber array. For acoustic wire (including magnetostrictive) spark chambers, this consists of converting into digital numbers the time intervals between pulses generated by the many transducers. (There are chamber designs that use components similar to those of magnetostrictive wire chambers, but that do not utilize the magnetostrictive effort.[1]) Many designs for performing the digitizations are possible. One classification of design can be made on the basis of the parallelism of the system. On the one extreme (completely serial) the pulses from all transducers may arrive on a single wire, with the information from each transducer being handled in time sequence. On the other extreme (completely parallel), the set of pulses from each transducer arrives on a separate wire, and the digitization of the information from all transducers goes on simultaneously. The system described in this paper is intended to work in the latter domain with large spark chamber arrays; the completely serial method may lead to excessively long digitizing times.

A second classification may be made with regard to the method of digitization. Here the velocity of propagation of sound in metal and the desired spatial resolution are very favorably matched to the capabilities of inexpensive digital integrated circuits. Hence the method of digitizing by counting the number of clock pulses contained in the interval between spark pulses has been almost universally used, and is also used in our system.

A third classification is possible according to the storage of the digitized data. For example, a single digitizing and tagging device may produce one data word for each clock time at which one or more pulses are received. The word contains the "time" at which the pulse (or pulses) arrives and the identification of the transducer producing it. The digitizer-tagger may be followed by a derandomizing buffer, and then by what one hopes is inexpensive bulk store, perhaps of magnetic cores. A less elegant--but, in our opinion, more practical--system consists of a single digitizer plus a one-word storage register for each expected pulse.

In most designs, this single digitizer-storage device has been a gated binary scaler, with a 12- to 14-bit 20-MHz scaler being provided for each spark that the system is required to be able to digitize.[2] Our system uses a single 20 MHz scaler which counts in Gray code rather than binary. As each pulse arrives, the count residing in the scaler at that instant is transferred to a preassigned location in an integrated-circuit scratch-pad memory array. Thus, rather than one scaler per data word, one scratch-pad memory location per data word is used.

Comparison of Digitizing Systems

The various types of systems described above can nearly all be designed in a way that the accuracy and resolution of the digitized results are essentially independent of the method chosen. Therefore, it seems quite reasonable to compare the systems on the basis of the cost to produce them. In this paper, we limit ourselves to comparing systems of the conventional scaler type and our scratch-pad memory design. In both cases there are fixed costs associated with control logic, clocks, etc., and also variable costs. The variable costs in both cases are fairly linear functions of the number of sparks required to be digitized--i.e., storage capacity. For the scratch-pad memory system, the fixed costs are higher than for scaler systems. For this reason, and because an extra word per channel is needed

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to store the start fiducial pulse, the cost per bit of scratch-pad memory storage must be lower than the cost per bit of binary scalers if the scratch-pad system is to be cost-competitive. Since the prices of both components are still falling, it is uncertain which will eventually be the cheaper. As medium-scale integration technology advances, we can hope to see sharp declines in the prices of scratch-pad memory elements. At present the 20-MHz toggling flip-flops of the type used in scaler systems are selling for about $2 a bit in quantities of 1000, but one manufacturer of scratch-pad memories (unfortunately, not the one we chose to use!) is selling completely wired scratch-pad memory cards at a price of $1 per bit. The scratch-pad memory system is therefore competitive for large-scale systems, and if the expected advances in medium-scale integration occur, will probably turn out to be considerably cheaper.

It should be pointed out that the prototype system described has many features, including self-testing facilities, that could be eliminated to reduce the fixed cost. These features were felt to be very useful for proving the reliability of the prototype system.

Digitizing Action of the Scratch Pad System

The basic block diagram of the digitizing system is shown in Fig. 1. A one-bit storage element resides at each intersection of word and bit lines. The clock is started at the same time as the spark chamber is pulsed. The bit lines of the storage array are driven continuously by the Gray-code scaler. As the first (i.e., start fiducial) pulse arrives on, e.g., Channel 1, a short (40-nsec) pulse is applied by the distributor to the top word line assigned to that channel. This causes the contents of the Gray scaler at that instant to be recorded in the top word location of the storage array. Subsequent pulses are received in this channel during the next few milliseconds, and are routed by the distributor onto sequential word lines. This same action is taking place simultaneously on the other channels; if pulses arrive at the same instant on different channels, the same number is recorded in the corresponding word locations.

This configuration of storage is not new to the spark chamber field. A similar configuration has been used in conjunction with sonic spark chamber arrays. There, clock frequencies of a few MHz are normally used, and ordinary magnetic cores have sufficient speed to be useful. The velocity of propagation of acoustic pulses in metal is nearly an order of magnitude faster than the velocity of sound in gases. Hence, to get comparable resolutions, acoustic wire spark chambers require clock frequencies several times as high for sonic chambers. This makes magnetic cores unsuitable. Of the suitable candidates we chose to use integrated-circuit scratch-pad memory chips. Several types of memory chips are commercially available. The design we chose uses the Transitron TMC 3164. It is a 16-bit memory chip, each bit of storage consisting of a flip-flop. The 16 flip-flops are arranged in a 4-by-4 matrix. A given flip-flop in a chip can be accessed by selecting one of the four horizontal (word) lines and one of the four vertical (bit) lines. The chips are interconnected as shown in Fig. 1 to form an N-word storage array, with each word having 16 bits, and with N being a multiple of four. Our tests and the Transitron specifications show that these chips are capable of storing information in periods as short as 15 nsec. They therefore have adequate speed to operate with clock frequencies of at least 40 MHz. Our prototype system uses a 20-MHz clock.

Thirty-two memory chips together with word and bit line drivers are mounted on the printed circuit memory card shown in Fig. 2. Each card has a storage capacity of 32 words of 16 bits each. A complete large-scale digitizing system will contain many such memory cards. A bin having a capacity of six memory cards and associated distributors is shown in Fig. 3.

Gray Code Scaler

A Gray-code scaler is not essential for this scheme. However, the prominent characteristic of the Gray code (i.e., only one bit changes per clock period) removes the necessity for synchronizing the word-line pulses with the clock oscillator. This helps to simplify the logic associated with the digitizing operation.

There are several methods for implementing Gray-code scalers. The method used in the prototype system is indicated in Fig. 4. The "true" outputs from each bit of a synchronous binary scaler are used to toggle a set of flip-flops that generate the Gray output. The Boolean relationship between the Gray and binary codes is

$$G_j = B_j \cdot \overline{B_{j+1}} + \overline{B}_j \cdot B_{j+1},$$

where B_j = the jth bit of the binary code word
and G_j = the jth bit of the Gray-code of equal value

As shown in the example in Fig. 4, proper initial conditions result in each toggling flip-flop generating one bit of Gray code. Commercially available TTL J-K flip-flops were used to build the 16-bit Gray-code scaler. Operation is successful with a clock frequency of 20 MHz. Use of some more recently announced integrated circuits would permit operation at 40 MHz.

Operating Cycles

The logic for controlling the operation of the system is contained in a separate bin, shown in Fig. 5. It can control several memory bins, and represents most of the fixed cost of the system. While digitizing an event, the memory array undergoes operating cycles of Erase, Write, and Read in that order. As already described above digitization takes place during the Write cycle, when

the digitized times of arrival of the pulses are written into memory. During Read, the contents of the scratch-pad memory are read and transferred to some external device. Since the Read is nondestructive, a separate Erase cycle is provided to set all memory of words to zero in preparation for the next Write.

Read Cycle

A flow diagram for the Read cycle is in Fig. 6. The reading of the bits stored in the memory is accomplished by coincident-voltage addressing. First, the proper word line is activated. Then, each bit line to be activated accesses the corresponding bit in the selected word. The design of the TMC3164 memory chip is such that, during Read, only one bit line per chip can be activated at a time. Thus four Read steps are required to read out a complete data word. This accounts for the four Read strobes shown in the figure. During Read, the word lines are selected by the same distributors as are used for Write. All the distributors (one per transducer channel) are reconnected to form one long shift-register chain. A single logic "1" is placed at the start of the long shift register, and is advanced one step after each word is read from memory. Thus, each memory location is selected in turn. As each location containing a digitized start-calibrate pulse is addressed, the logic function marked "Stacal" is activated. This causes the one's complement of the word read from memory to be placed in the subtrahend register (see Fig. 6). The adder then subtracts the Stacal word from each subsequent data word. Thus the contents of the data words output to the permanent storage device represent the time separation between each spark pulse and the start calibrate pulse of the same channel.

The reading of each word from memory is accomplished in eight steps. The Read step assignment is shown in Fig. 7. The eight steps consume about 2 μsec.

Erase Cycle

The Erase cycle is begun from 5 to 10 μsec after the spark chambers are pulsed, after the electrical noise has died away. The Erase cycle consumes only 2 μsec, hence is easily completed before the magnetostrictive pulses start to arrive.

Internal Tests

Facilities are included for exercising the memory to confirm that it is operating properly. In the internal-test mode, the Gray-code scaler is incremented only at the beginning of each test cycle. The stationary contents of the scaler are then set into every word of the scratch-pad memory and into the subtrahend register as well. Then, as the words of the memory are read out in turn, the word in the subtrahend register and the word read from memory are subtracted in the adder. The difference should be zero. If not, the test is stopped. If all memory locations pass the test, the Gray-code scaler is incremented and the procedure repeated until the scaler overflows. If no faults have been detected by this time the test is decreed a "Pass."

Status

The prototype system shown in the photographs has been successfully bench-tested, and is now being prepared for a Bevatron experiment. When used in the experiment, it will have a capacity of about 50 transducer channels. Digitizing capacities of from 2 to 8 sparks will be provided in various channels. The total equivalent scaler capacity will be about 200.

Acknowledgments

We gratefully acknowledge the contributions of Jean Mougel, a visitor from the Centre d' Etudes Nucleaires de Saclay, France, who did the initial design of the Gray-code scaler. We also thank Dr. Victor Perez-Mendez for his constant interest and encouragement.

References

1. R. Grove, L. Kaufman, and V. Perez-Mendez, Sparkostrictive Spark Chambers with Piezoelectric Readout, Nuc. Instr., to be published.

2. F. Kirsten, K. Lee, and J. Conragan, IEEE Trans. Nucl. Sci., Vol. NS-13, (3), 583-590 (1966).

Figure Captions

Fig. 1-Basic block diagram of the digitizing system. The emphasis here is on the digitizing action (Write cycle) and the organization of the scratch-pad memory.

Fig. 2-Memory card. It contains 32 16-bit words of scratch-pad memory plus word and bit line drivers.

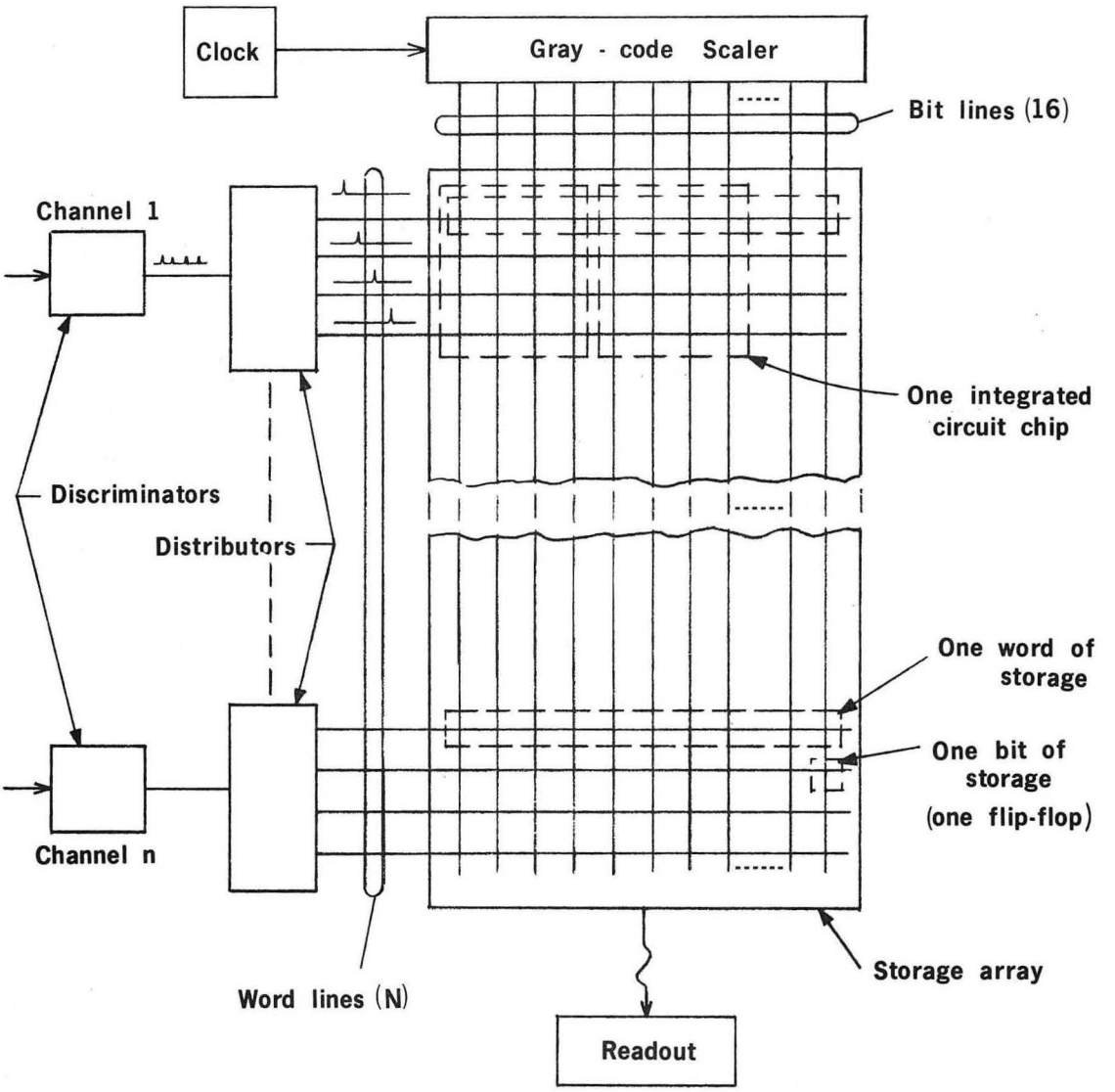
Fig. 3-A partially filled memory bin. Two memory cards are in place; there is space for four more. The smaller cards contain the Gray-code scaler and distributors.

Fig. 4-A block diagram of the Gray-code scaler. The blocks labeled G are toggling (e.g., J-K) flip-flops.

Fig. 5-The bin containing logic for controlling several memory bins.

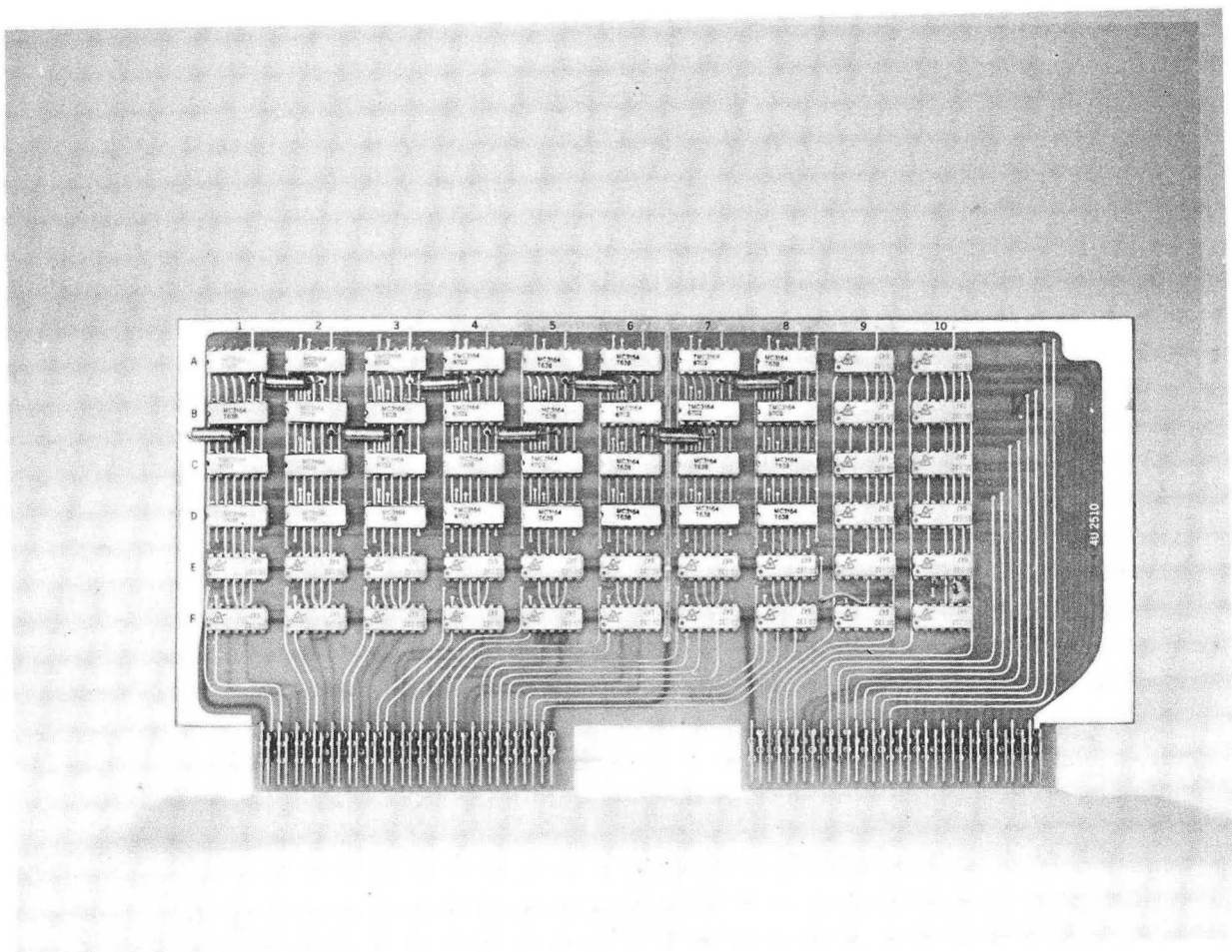
Fig. 6.-This diagram shows the flow of data during the Read cycle.

Fig. 7-Eight steps are required for each word read from memory. This shows the sequence of the steps. Each step consumes about 250 nsec.



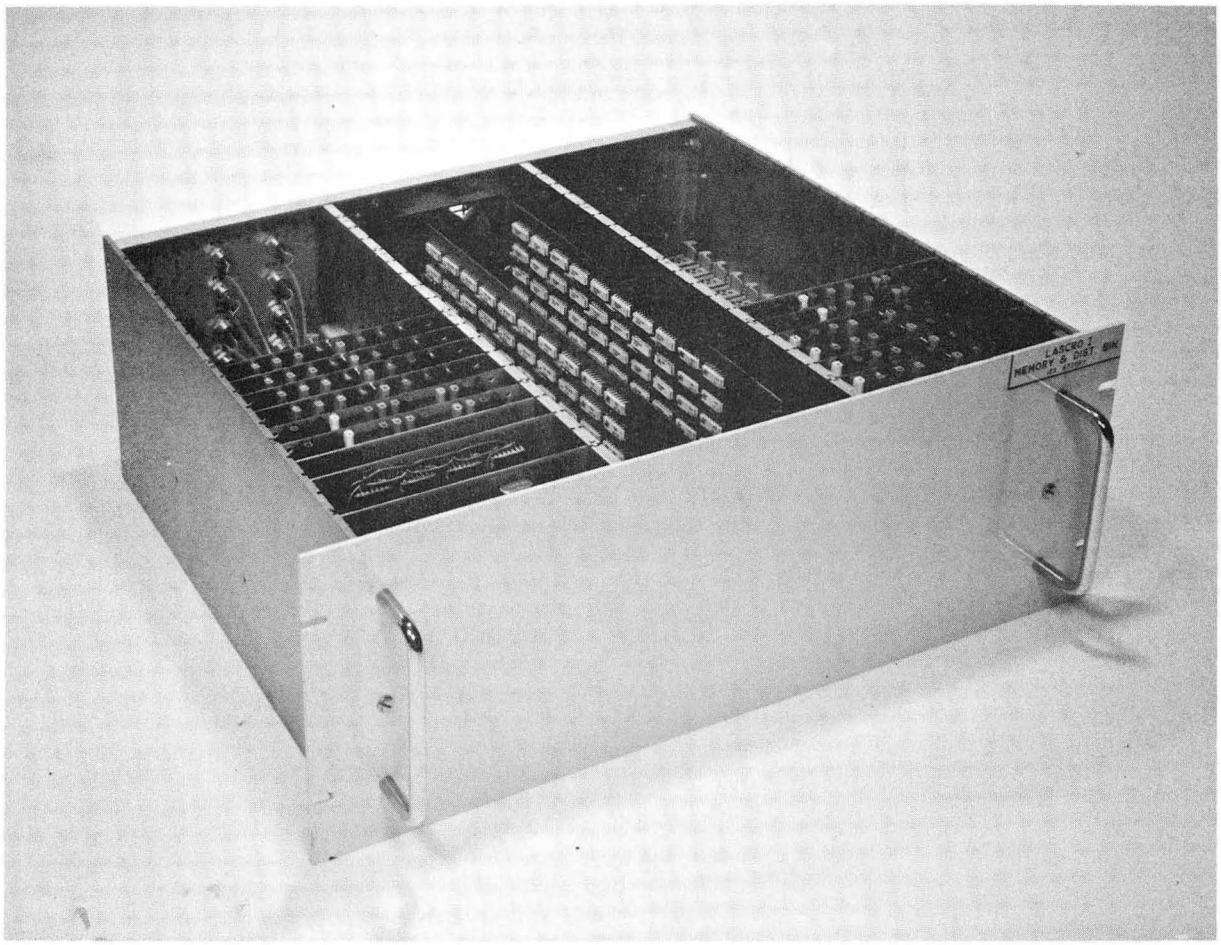
XBL 683-233

Fig. 1



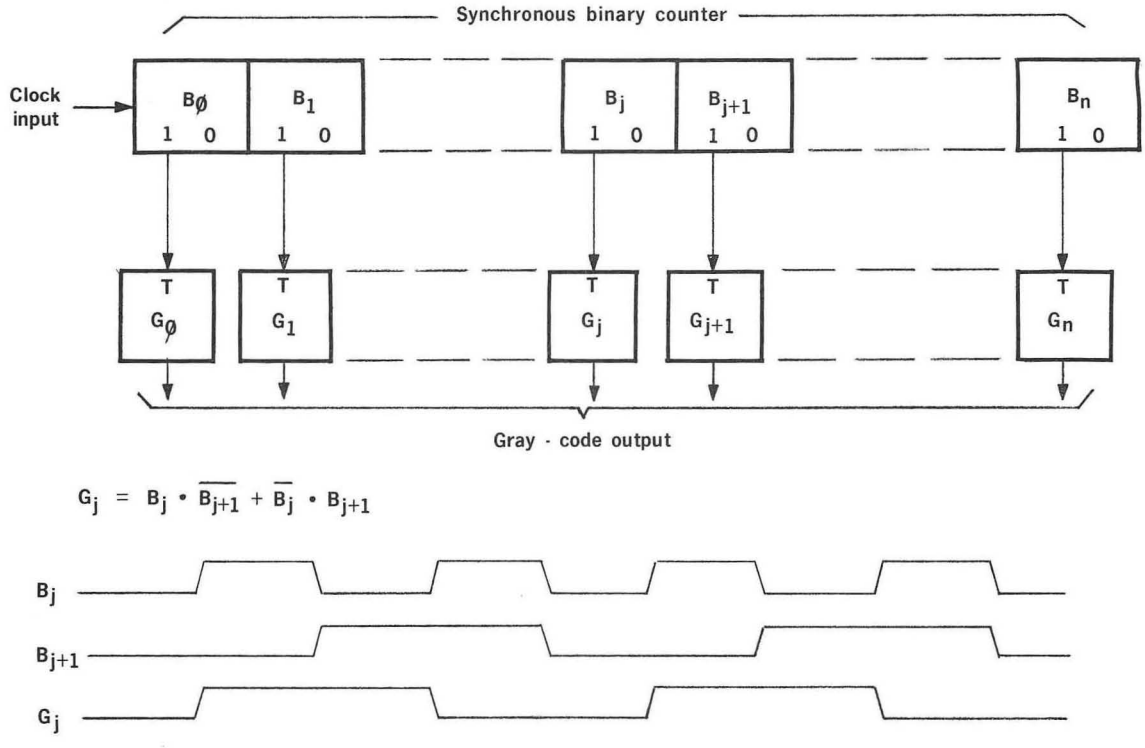
XBB 678-4584

Fig. 2



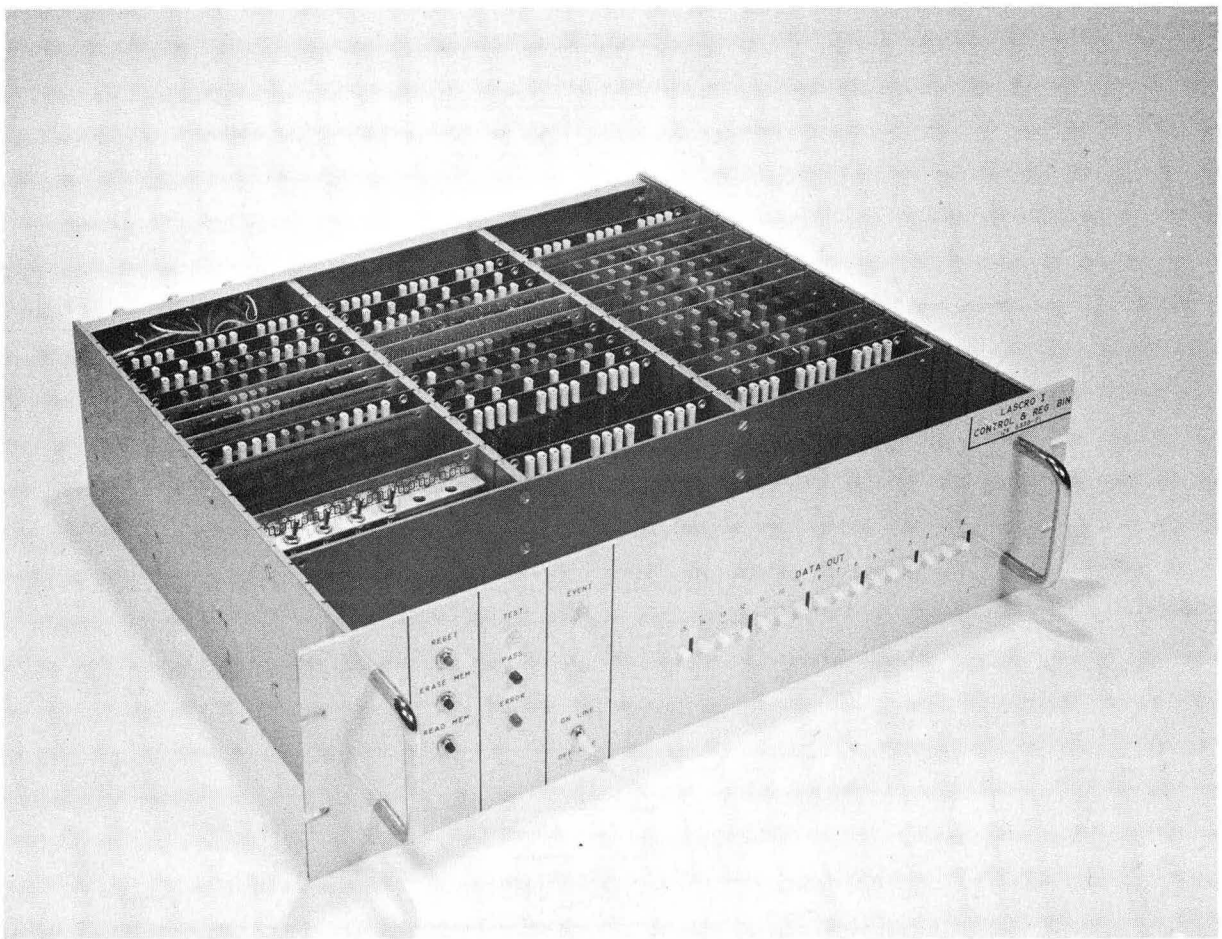
XBB 682-733

Fig. 3



XBL 683-234

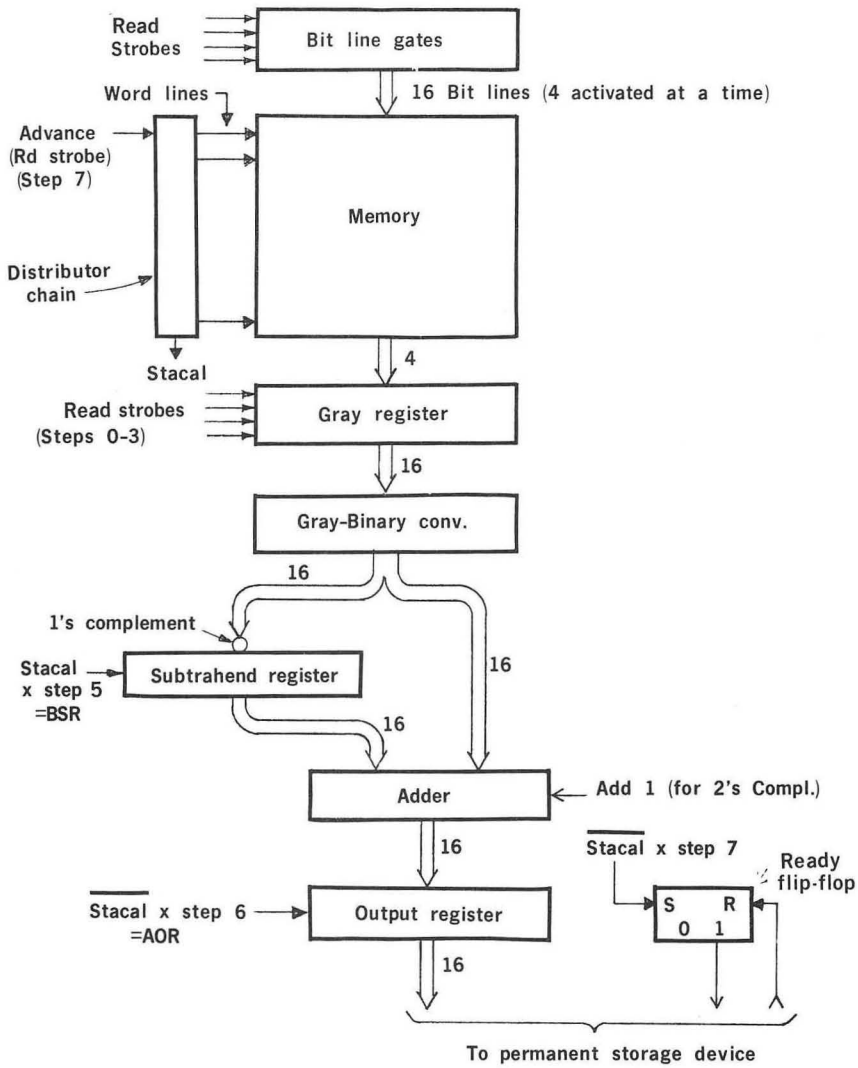
Fig. 4



XBB 682-732

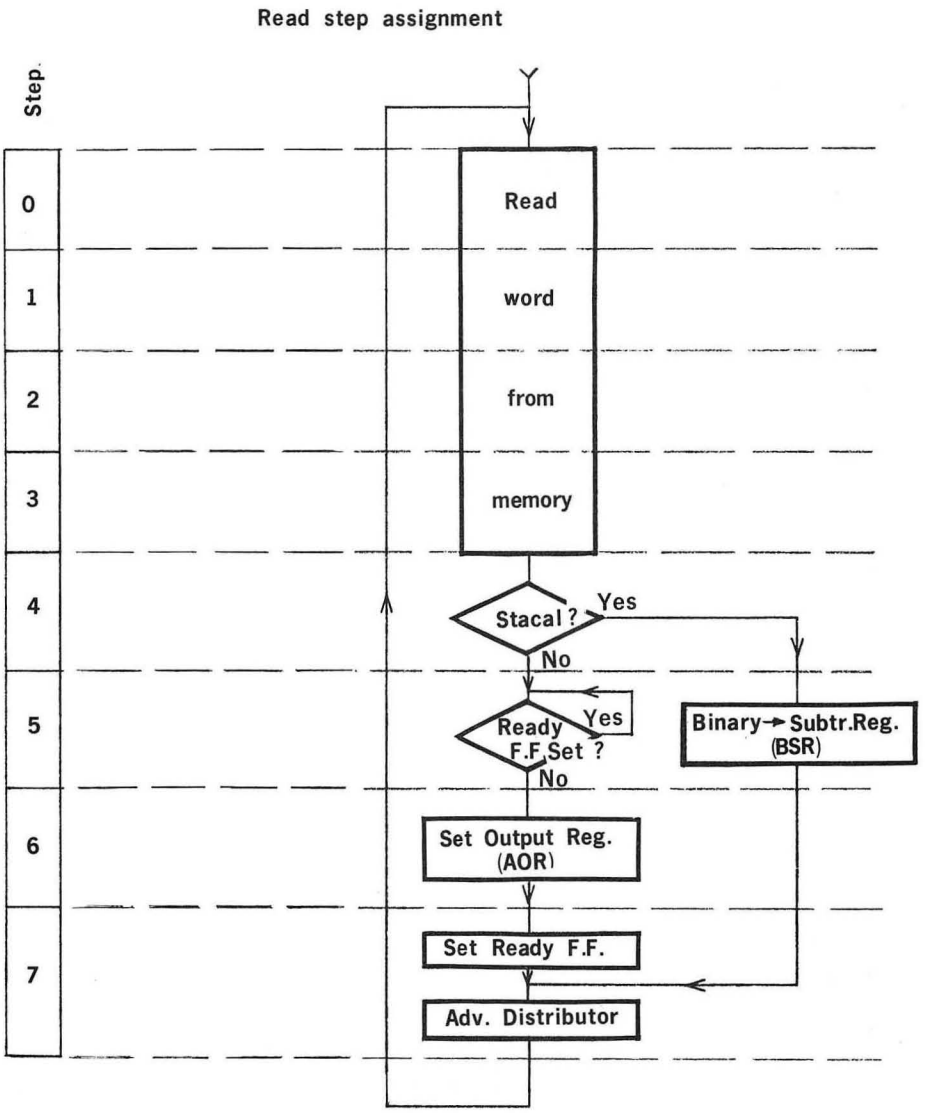
Fig. 5

Read flow diagram



XBL 683-235

Fig. 6



XBL 683-236

Fig. 7