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READY-MADE LOGIC BOARDS AND THE SMALL-VOLUME USER

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Douglas L. Abbott

October 8, 1968

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University of California  
Berkeley, California

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The increased use of integrated circuits and the proliferation of ready-made IC printed-circuit boards in complete logic sets have prompted a discussion of the relative value of buying boards from a volume manufacturer or designing and building boards in-house. There are many well known, persuasive arguments in favor of buying boards from an outside vendor, not the least of which is volume of usage. Thus it is considered more economical for a high-volume systems manufacturer to design his own boards, whereas a small user such as a research laboratory which only builds a few systems a year is better off buying ready-made boards from an outside source. This article does not attempt to dispute the case for buying rather than building, but points out an additional factor which bears heavily on the decision. That is that the number of boards required to justify in-house design costs can be significantly reduced by increasing the complexity of user-designed boards.

All IC logic boards may be grossly divided into two major categories--general purpose and specific function. A general-purpose board consists of number of gates and/or flip-flops arranged in a general pattern which may be interconnected in countless ways with other similar boards to produce the desired logic function (see Fig. 1). This includes functional units such as counters and registers with a relatively low level of intraboard

connection. Ready-made logic boards are necessarily of this type in order to have the widest applicability.

Specific function boards, on the other hand, are designed to accomplish a very specific logic function, and hence their applicability is extremely limited. They are characterized by a high level of intra-board connection and are generally space-limited rather than pin-limited as most general-purpose boards are. Figure 2 shows a typical specific-function board. This particular board is a serial-parallel conversion register used in a time-sharing teletype multiplexer system.

The build-versus-buy decision is based on the simple formula

$$C = P, \tag{1}$$

which says that the cost (C) to design and build boards in-house equals the price (P) to buy ready-made general-purpose boards. This may be expanded as follows:

$$NC_B + N_T C_D = NP_C \tag{2}$$

where N is the total number of boards used,  $C_B$  is the cost to build each board,  $N_T$  is the number of types of boards,  $C_D$  is the cost to design each board type, and  $P_C$  is the purchase price per board.

Previously the factor N has been separated into  $N_s N'$ , where  $N_s$  is the number of systems, and  $N'$  is the number of boards per system. For the small volume user, however, the number of systems built is not as significant as the total number of boards used. In other words, can you use enough boards, whether it be in one system or a hundred, to justify the design cost before new developments make the board obsolete.

Equation 2 may be rewritten as

$$N = MN_T, \quad (3)$$

where  $M = C_D / (P_C - C_B)$  and represents the minimum number of boards per design type which must be used to justify in-house building. Tables I and II give approximate figures for design and building costs respectively. These are, of course, subject to a great many variables but nevertheless serve to illustrate the point. The cost of integrated circuits is based on an average of 20 gates or 10 flip-flops per ready-made general-purpose board. Using the midvalues of  $C_D$  and  $C_B$  and taking  $P_C$  to be \$70,  $M$  comes out about 39. This means you must use at least 39 boards of each design type to "break even."

Equations 2 and 3 make no allowance for the increased complexity possible by designing boards for a specific function. This increased complexity comes about in two ways. First, the higher level of intraboard connection allows more IC's on a board. Second, and perhaps more important, medium-and large-scale integration (LSI) may be utilized to allow more functions per board with the same number of packages. Because they are pin-limited, ready-made boards can not benefit greatly from MSI and LSI. As a typical case, consider a 12-bit shift register built on a board with a 44-pin connector, with 4 pins committed to power and ground. Such a register requires a minimum of 27 input-output connections--12 parallel inputs, 12 parallel outputs, 1 parallel load, 1 clock, and 1 common clear. Other options would require more input-output connections. If this were built with dual flip-flops and quad 2-input gates, it would require 9 dual in-line packages (DIP). Add an extra package of gates or

flip-flops to fill up the extra 13 pins for a total of 10 DIP's. This is a reasonable number for most boards currently available.

This same function could be implemented with three 4-bit shift-register chips such as the Fairchild 9300. Adding an extra package for the remaining pins gives a total of four. True, we have saved six packages, but we have "wasted" the space that those packages occupied because there is no way to connect more packages to the outside world. Now instead of the single package of gates using 12 pins, we could install a complex multi-package circuit with many internal connections to utilize this extra space. Board suppliers, however, are understandably reluctant to do this, since each DIP pin not brought to the outside world reduces the flexibility of the board. A user designing a board for a specific application need not worry about flexibility, and he can squeeze as many IC's on a board as space will allow and perhaps still not use all of the board's input-output pins. This incidently saves on backplane wiring.

The degree of complexity may be expressed by the replacement factor,  $R$ , which represents the number of general-purpose boards required to duplicate the logic function of one specific function board. For example, the serial-parallel register board in Fig. 2 contains seven DIP's and two discrete component lamp drivers, yet it would take approximately three general-purpose boards to duplicate the logic of this one board. Therefore,  $R$  equals 3 in this case. By definition, we have  $R_{GP} = 1$  and  $R_{SF} > 1$ .

Getting back to the economics involved, we may rewrite equation 2 as

$$N_1 C_B + N_T C_D = N_2 P_C, \quad (4)$$



where  $N_1$  is the number of in-house specific-function boards, and  $N_2$  is the number of general-purpose boards required to duplicate the same function.

Equation 4 can be rewritten in the form of Eq. 3 as

$$N_1 = N_T \left[ \frac{C_D}{R P_C - (C_{B1} + R C_{B2})} \right], \quad (5)$$

where  $R = N_2/N_1$  and, in this case, represents an overall system replacement factor. If we let  $N_T = 1$ ,  $R$  may refer to a single board type. The term in brackets is  $M$  as defined previously, but now  $M$  is a function of  $R$ , that is

$$N_1 = N_T M(R).$$

Note that  $C_B$  has been separated into two components:  $C_{B2}$  is the cost of integrated circuits, and  $C_{B1}$  is all other building costs. This is because the cost of integrated circuits increases roughly in proportion to the relative complexity, while other building costs remain essentially the same. The use of complex-function IC's does not alter this since, with few exceptions, they have a relatively constant cost per flip-flop.

The dramatic effect of  $R$  may be seen in Fig. 3, where  $M$  is plotted against  $R$  for two values of design cost. Given the board sizes currently in use, I would consider  $R = 5$  as a practical maximum for this concept. The numbers quoted here are "ball park" estimates and the curves should be shifted up or down as required to fit any specific situation. Although the curves are based on fixed design costs, it is likely that such costs will increase with  $R$ , although not necessarily in direct proportion.

Thus one should tend toward the higher curve as  $R$  increases.

One may ask what degree of complexity would be necessary to reduce  $M$  to 1, that is justify the design cost with only one board.

Taking the same cost and price figures used in Fig. 3, we have

$$R_1 = 18.2 \text{ for } C_D = \$1000$$

$$R_1 = 36.7 \text{ for } C_D = \$2000.$$

Such complexity is, of course, beyond the realm of printed-circuit-board technology and requires something like a wire-wrap IC panel system. The cost considerations are totally different, but this approach may be more economical in the long run.

The application of this concept involves considerations of system architecture. The objective should be to divide the system as far as possible into repeatable subsystems, then design boards for these subsystems which combine the highest degree of complexity consistent with sufficient repeatability to justify the design cost. This in fact is the same problem facing LSI designers.

Obviously, no system consists entirely of neat, regular subsystems. To avoid designing general-purpose boards for these irregular sections, the designer should be able to combine his complex, specific-function boards with commercially available general-purpose boards. The choice of ready-made boards and bin hardware may place severe constraints on the design of specific-function boards, because many boards currently available will not hold enough IC's to make complex function design practical. To take full advantage of this technique, a

board should accommodate at least ten 14-pin DIP's and leave sufficient space for art work.

#### Acknowledgment

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#### Reference

1. John R. Hemmert and Burton L. Leary, To Buy or to Build Logic Cards, Cambion Application Note AN4-67.

Table I. Cost of initial design per type.

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1. Drafting (layout)	
(a) Taping	
(b) Assembly drawing	
(c) Schematic drawing	
(d) Marking drawing	
(e) Detail drawing	
(60 hours at \$10 per hour = \$600)	\$500 to \$1,000
2. Engineering follow-up	\$100 to \$ 500
3. Drill jigs, card holders, routing jib	\$200 to \$ 500
	<hr/>
	\$800 to \$2,000

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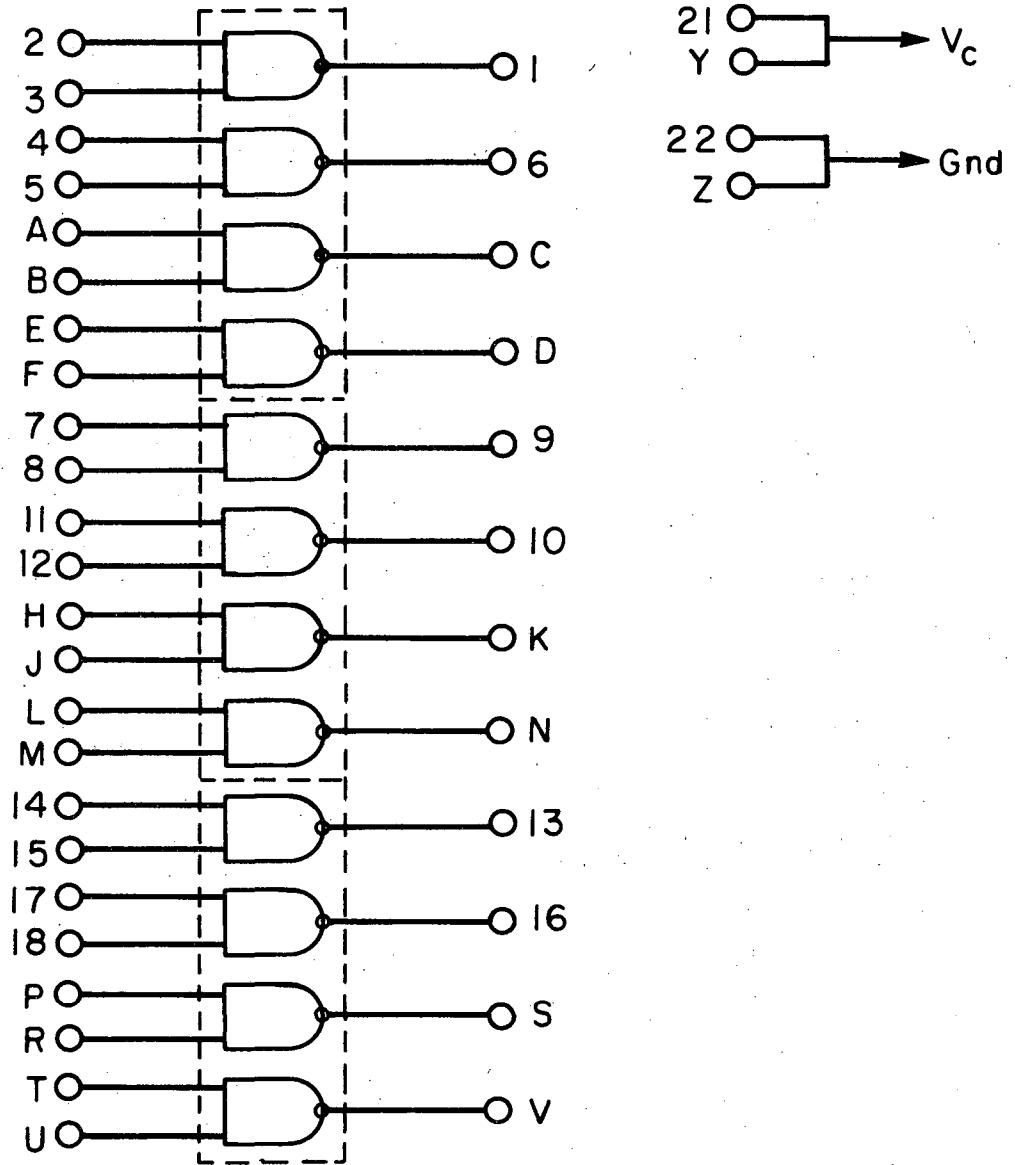
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Table II. Cost of boards (except IC's).

	<u>Min.</u>	<u>Max.</u>
1. Board	.75	1.00
2. Board fabrication	3.00	7.50
3. Drilling	1.50	2.50
4. Eyelet assembly	1.00	2.00
5. Plating	1.00	1.50
6. IC assembly	.50	1.00
7. Wave solder	1.50	2.50
8. Testing	2.00	5.00
9. Ejector (board handle)	.25	1.50
	<u>11.50</u>	<u>24.50</u>
Cost of IC's (see text)		
1. 20 gates @ 60 cents	12.00	
2. 10 flip-flops @ \$2.00		20.00
	<u>23.50</u>	<u>44.50</u>

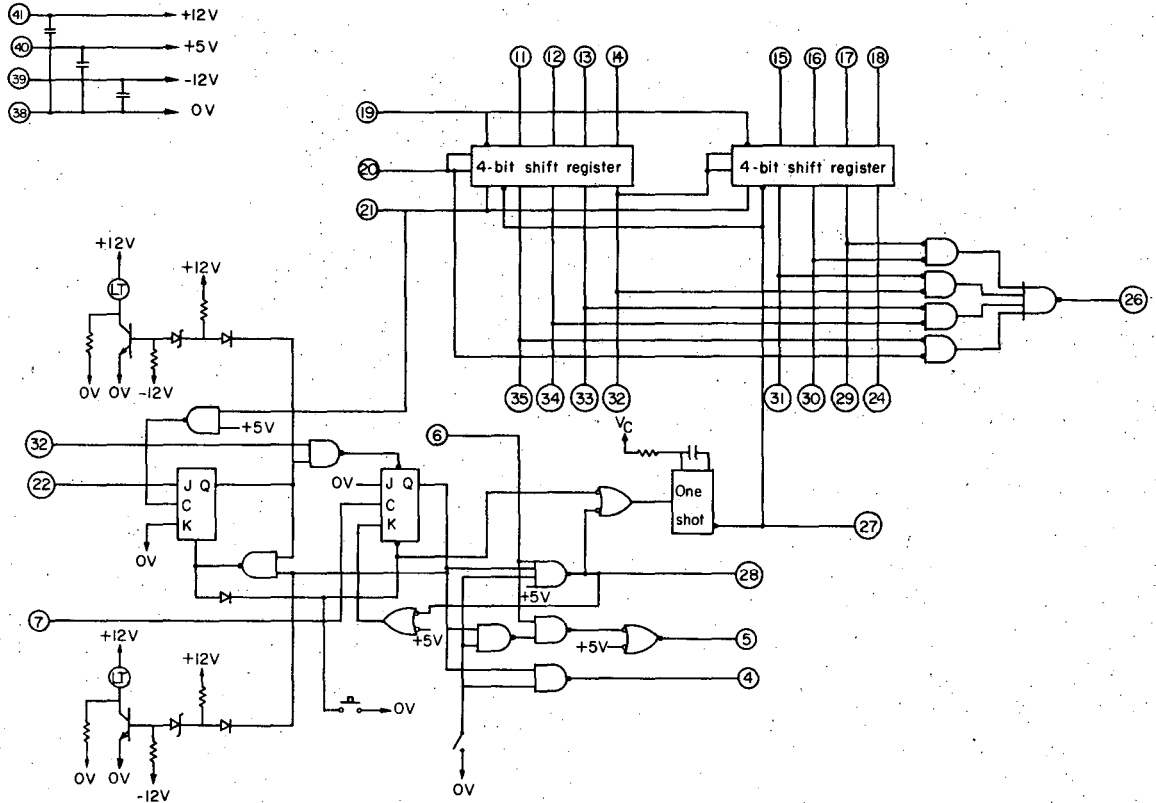
Figure Captions

- Fig. 1. Typical general-purpose IC board.
- Fig. 2. Example of user-designed specific-function board.
- Fig. 3. Minimum number of boards required to justify design cost as a function of relative complexity.



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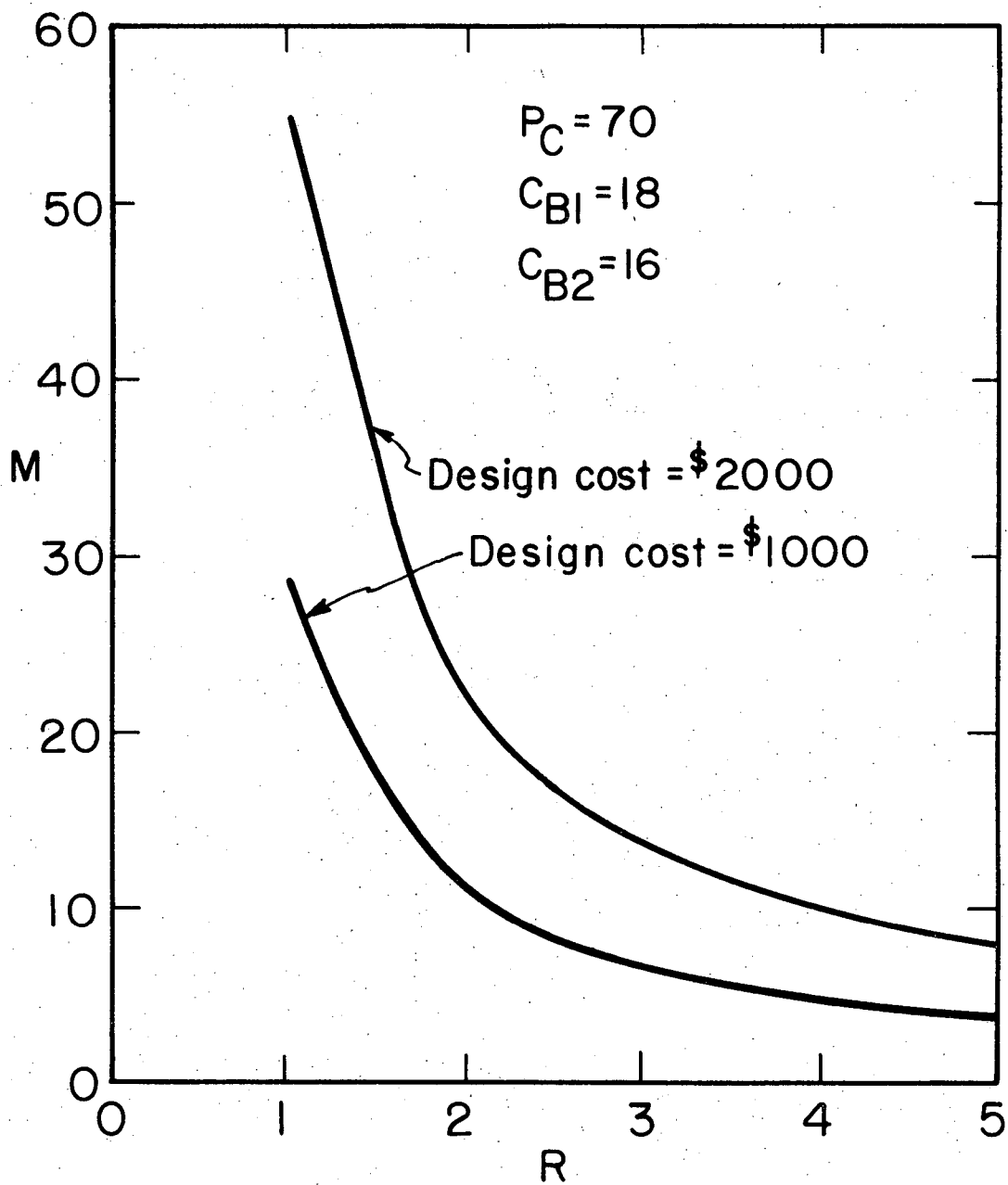
Fig. 1



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Fig. 2





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Fig. 3

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