UNIVERSITY OF CALIFORNIA
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Optimization of Thermal Performance of the Three-Dimensional Integrated Circuits (3D ICs) Utilizing the Rectangular-Shaped and Disk-Shaped Heat Pipes and Integrated Chip-Size Double-Layer and Multi-Layer Microchannels

A Dissertation submitted in partial satisfaction
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by

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Dedication

To my dearest parents for all your love and care:

Feng Wang and Yanli Lu

ABSTRACT OF THE DISSERTATION

Optimization of Thermal Performance of the Three-Dimensional Integrated Circuits (3D ICs) Utilizing the Rectangular-Shaped and Disk-Shaped Heat Pipes and Integrated Chip-Size Double-Layer and Multi-Layer Microchannels

by

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Doctor of Philosophy, Graduate Program in Mechanical Engineering
University of California, Riverside, September 2022
Dr. Kambiz Vafai, Chairperson

Moore's law has been applicable for many of the electronics advancements. The issue of coming up against proper thermal management prevents these features from being produced much smaller. Hence, the industry has moved from a two-dimensional approach to a three-dimensional setup to utilize the volume more efficiently. A three-dimensional integrated circuit (3D IC) is a metal-oxide semiconductor-integrated circuit manufactured by stacking silicon wafers or dies and interconnecting them vertically using through-silicon vias (TSVs), such that they behave as a single integrated device to achieve higher performance, lower power consumption, higher functional density, lower transistor packaging density, and a smaller form factor than conventional two-dimensional integrated circuits. Due to drastically increased integration density of 3D ICs, the tasks of removing a large amount of dispersed heat from a constrained space is beyond the capability of conventional cooling techniques.

Rectangular-shaped and disk-shaped heat pipes (RSHPs and DSHPs) and integrated chip-size double-layer and multi-layer microchannels (DLMCs and MLMCs), as innovative heat sinks, are investigated to optimize the thermal performance of 3D ICs in this work. The results show that both RSHPs and DSHPs contribute to improve the overall thermal performance and reduce the hotspot temperature by 7K and 11K on average, respectively. Furthermore, utilizing the RSHP or DSHP as the heat spreader in place of the solid copper heat spreader further optimizes the thermal performance with the reduction of the junction temperatures 14K and 16K on average, respectively. The chip-size integrated DLMC without a heat spreader and a heat sink reduced the hotspot temperature by almost 15 K for a nominal 3D IC structure. Meanwhile, the weight of the chip-size integrated DLMC is 1288 times lighter and the size is significantly smaller than the copper heat sinks. In addition, two chip-size integrated DLMC lowered the hotspot temperature by another 6.77 K compared with utilizing just one integrated DLMC on top of the chip structure. The results also show that the MLMC have a great effect on reducing the hotspot temperature. The proposed structures and results presented in this study pave the way for major innovations in resolving the thermal issues for the 3D ICs.

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Chapter 1

Introduction and Background

1.1 The significance of the transistor

The most important advancement humankind has ever made is the transistor (Figure 1.1). A transistor is a miniature semiconductor that regulates or controls current or voltage flow in addition amplifying and generating these electrical signals and acting as a switch or gate for them [1]. Humankind is living in a time of incredible growth and the age of information, the one that has already started to transform the way of living. The human race is more intertwined than ever before by being connected to the internet. It is the invention of the transistor that led to the amazing life style and advancement, and this single invention gave rise to the smartphone equipped generation. The transistor is information itself. The series of ones and zeros beaming across the planet to be interpreted by the processors in the computers. Without the transistors, people wouldn't have access to the wealth of information on the internet, to do the research projects, to use the animation software, to accomplish all the simulations works in all the industry companies, to millions of works that humankind needs to develop and to grow. The transistor is the foundation for all the modern computers.

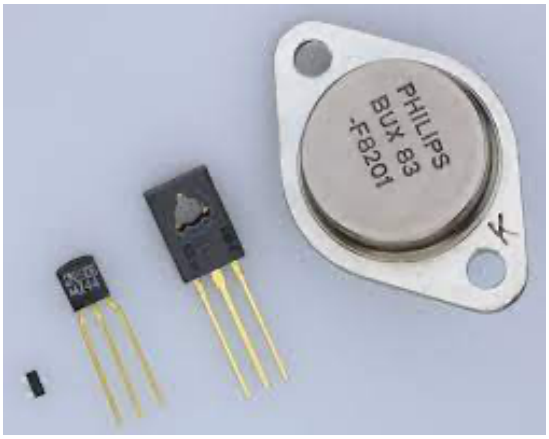

Figure 1.1 Assorted discrete transistors. Packages in order from top to bottom: TO-3, TO-126, TO-92, SOT-23.– This image is in the public domain in the US and is taken by Misterrf

1.2 The history of transistors

Before the transistor existed, the vacuum tubes [1-2] are used, see Figure 1.2, which is a device that controls electric current flow in a high vacuum between electrodes to which an electric potential difference has been applied. The triode vacuum tube consisted of three parts, the cathode, grid, and anode. A current is passed through the cathode and begins to heat up, causing it to release electrons, as the gases have been removed from the tube, the electrons have very little resistance to their movement and they are attracted to the positively charged anode. This completes the circuit and a current flow. The flow of electrons can be manipulated in many useful ways with the grid. For instance, it can be used as a switch. If a light bulb is placed as an appliance, it will only light up when there is a positive voltage across the grid. If a negative voltage is applied, the negative voltage

will repel electrons passing through. This is the foundation for binary coding, which is the ones and zeros that gave birth to the age of information. For the light bulb example, 1 is the positive voltage and 0 is negative voltage. Hence, 1 turns the light on, and 0 turns it off.

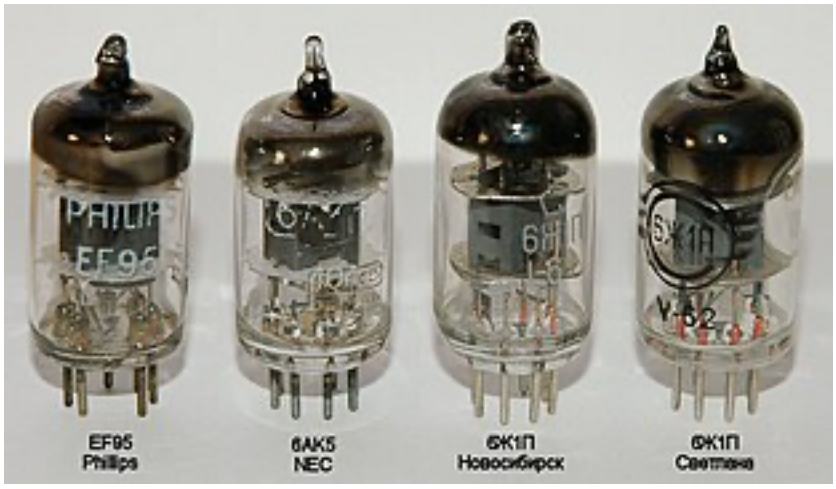

Figure 1.2 The vacuum tubes for the first generation of computers. This image is in the public domain in the US and 6AK5 vacuum tubes.JPG is captured with Nikon D70 by Tvezymer

The world's first general purpose electronic computer in 1945, the ENIAC [3,4], see Figure 1.3, used 18,000 vacuum tubes to perform calculations. ENIAC calculated a trajectory in 30 seconds that took a human 20 hours, one ENIAC could replace 2400 humans [5]. However, the ENIAC weighed 30 tons and took up an entire room [6, 7]. It was incredibly power hungry, as the vacuum tubes cathodes needed to be heated to work, which also meant that the vacuum tubes burnt out regularly and needed to be replaced. All this is to perform a function that a phone basically does with a simple game, like Angry

Birds. On top of that, it’s computing power could be contained on a silicon chip no larger than a grain of sand.

Figure 1.3 Programmers operate ENIAC's main control panel at the Moor School of Electrical Engineering. This picture is in the public domain in the US and taken by United States Army

The first working device built was a point-contact transistor invented in 1947. The most widely used type of transistor is the metal-oxide-semiconductor field-effect transistor (MOSFET), which was invented at Bell Labs in 1959 [8-10]. Transistors revolutionized the development of electronics and paved the way for smaller radios, calculators and computers. Most of the transistors are made of silicon. Silicon is a semiconductor, which means the conducting properties can be tailored by introducing impurities to the crystal structure. As illustrated in Figure 1.4, the transistors in a CPU are microscopic and are

manufactured with high precision with machines on thin wafers of silicon crystal that are sliced off silicon ingots.

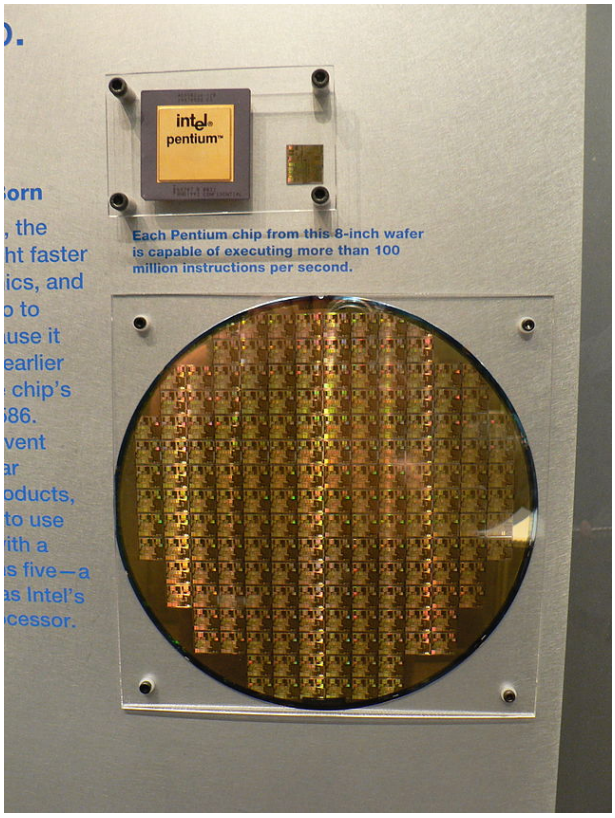

Figure 1.4 8-inch silicon wafer with multiple intel Pentium chips on it. This picture is in the public domain in the US and is taken by Naotake Murayama.

1.3 Moore's law

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles about every two years (Figure 1.5). Moore's law has been used in the semiconductor industry to guide planning and to set targets for research and development.

The first commercial computer (Figure 1.6) that used a moving head hard disk drive for secondary storage, IBM 305 RAMAC, was used at the U.S. Navy in 1956 and it weighed over a ton. The IBM hard disk drive in 1956, which needed to be lifted by a forklift into a plane, could only hold 3.75 MB with a leasing price $3200 per month. However, the minimum standard storage for an iPhone today is 64 GB and weighs around 200 grams. The largest commercially available hard disk drive can store 15 TB and the solid-state drive can offer 100 TB and weighs around 400 to 500 grams. The electronics are increasingly smaller but with higher performance, higher functional density, lower power consumption and much affordable price. The incredible advancement at an exponential rate in electronics is guided by the Moore's law. Moore's Law states that the number of transistors doubles every two years. The only way to fit more transistors into one microchip while maintain the small size is to make the transistors smaller. The shrinking of the transistors reduced the size of processors significantly. One of the first semiconductor processors, Intel's 4004 in 1971 was 10 micrometers, MIPS R14000 from SGI was 130 nanometers in 2001, Intel "Cannon Lake" was 10 nanometers in 2018 and M1 Max from Apple was 5 nanometers in 2021. While Moore's Law has been contributing to the advancement of the device scaling and providing high-functionality and high-performance electronics, the physical limitations and the increased power dissipation which results in high operating temperature might bring Moore's law to an end. Hence, apart from the quantum tunneling problem and transistor size approaching to the atom size, the most problematic of all is the thermal management issue caused by the small sized transistors.

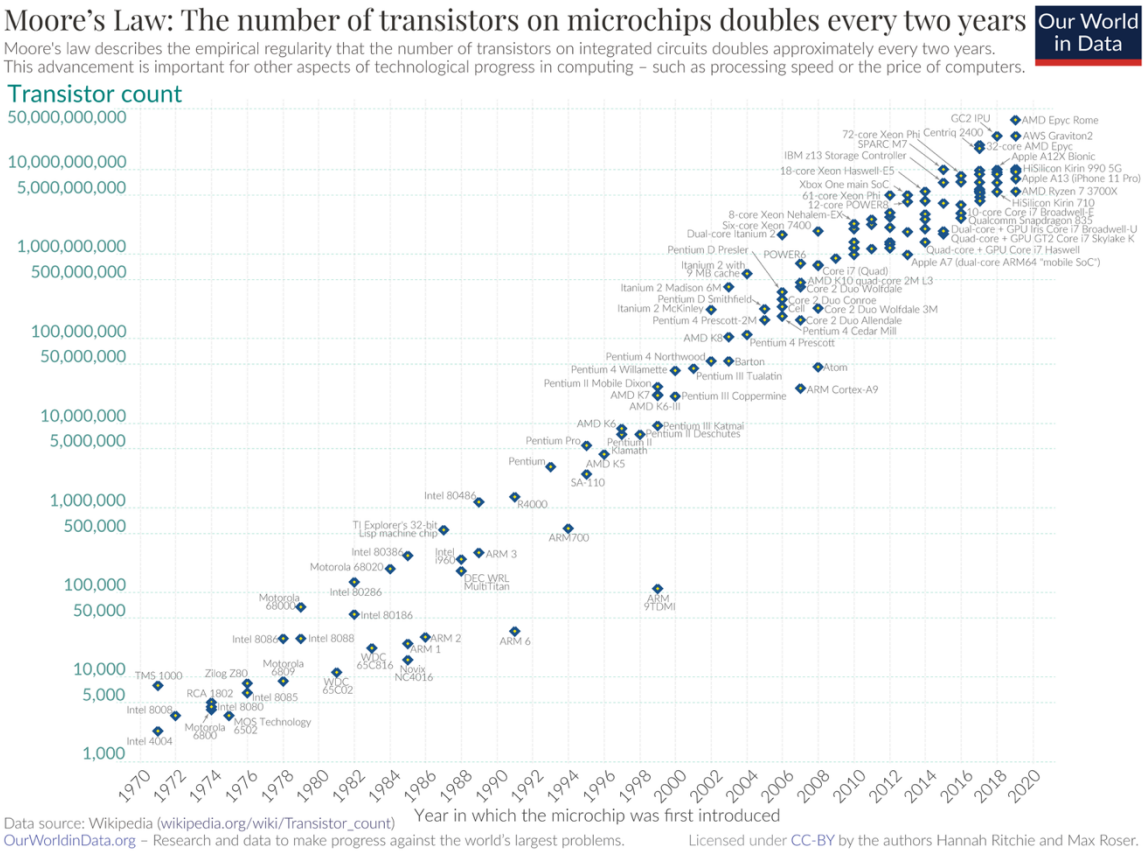

Figure 1.5 Moore's Law transistor count 1970-2020. This graph is in the public domain and created by Max Roser, Hannah Ritchie and licensed under Creative Commons Attribution 4.0 International.

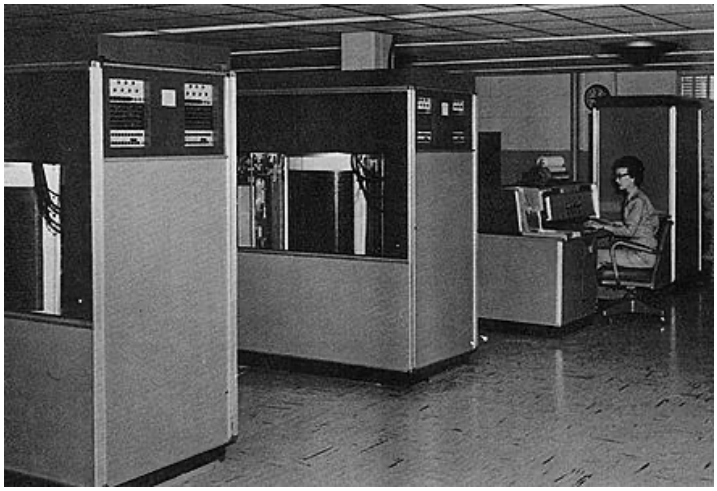

Figure 1.6 BRL61-IBM 305 RAMAC in 1956. This picture is in the public domain in the US because it is a work prepared by an officer or employee of the United States Government as part of that person's official duties.

1.4 Three-dimensional integrated circuits (3D ICs)

The issue of coming up against proper thermal management prevents these features from being produced much smaller. Hence, the industry has moved from a two-dimensional approach to a three-dimensional setup to utilize the volume more efficiently. A 3D IC (Figure 1.7) is a metal-oxide semiconductor-integrated circuit manufactured by stacking silicon wafers to dies and interconnecting them vertically using through-silicon vias (TSVs), such that they behave as a single integrated device to achieve higher performance, lower transistor packaging density, and a smaller from factor than conventional two-dimensional integrated circuits.

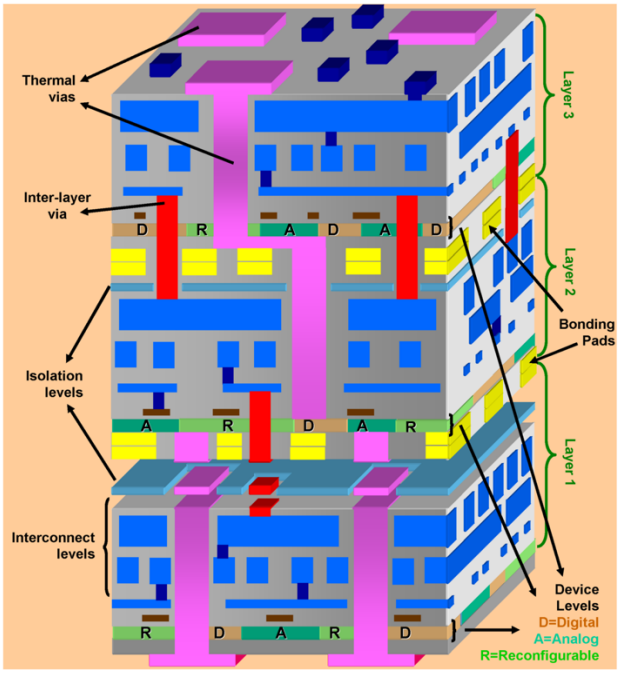

Figure 1.7 DARPA Strategic Plan (2005) Schematic of 3-D circuit employing advanced functionality in each layer and reducing the length of critical signal paths. This image is in the public domain in the US and is a work of Defense Advanced Research Projects Agency (DARPA), an agency of the United States Department of Defense, employee, taken or made as part of that person's official duties.

Despite all these benefits, heat built up within the stacks must be removed. 3D ICs pack an extraordinary amount of complexity into an extremely small space, which creates a substantial amount of heat, resulting in damage to the device's reliability. Thermal hotspots in 3D ICs can exacerbate failure mechanisms such as junction leakage and electromigration, resulting in degradation of the device's performance. It is increasingly important to have effective and efficient thermal management in order to optimize the design characteristics of 3D ICs.

1.5 Thermal Management

The thermal management is required to improve reliability and prevent the failure mechanisms in all electronic devices and integrated circuits. The high-power input in the modern graphic cards and CPUs produced the equal amount of heat output. The innovative and efficient cooling techniques are critical in order to maintain the optimal functionality and performance of the electronics. Discussions regarding various cooling techniques have dominated research and industry in recent years, including heat sinks, thermoelectric coolers, fin-stacks, forced air systems and fans, heat pipes, vapor chambers, single-layer microchannels, double-layer microchannels, thermal interface materials, boiling cooling techniques and others.

The heat pipe (Figure 1.8) is a vacuum sealed metal tube that contains a working fluid that changes from liquid to vapor when heat is applied at one end of the tube. The heated vapor moves quickly to the other end of the tube where it condenses then travels through the wick material (sintered copper) back to the end of the heat source. This design allows heat pipe to transfer heat much more efficiently than a solid piece of metal with benefits of much lighter weight and performing well in any orientation. It has been well established in many applications, such as spacecraft thermal control, electronic systems cooling and many commercial thermal devices. However, the traditional heat pipes have some limitations, for instance, they only transfer heat in one direction and the round shape makes it physically difficult to get close to a very small heat source. Vafai et.al [11-15] investigated flat-shape heat pipes that can overcome the limitations of the traditional heat pipes. The flat-shape heat pipes with secondary feeding mechanism, substantially better

geometric adoptability for complex applications and ability to fully handle asymmetrical heat load, will offer the solution for the high heat generation of 3D ICs and have far-reaching impact on the thermal management of 3D ICs.

Figure 1.8 Heat Sink with heat pipes. This picture is in the public domain in the US and taken by Hustvedt under the license of Creative Commons Attribution-Share Alike 3.0

Microchannels were first introduced by Tuckerman and Pease [16]. Microchannel heat sinks (Figure 1.9) maximize the surface area, minimize the thermal resistance, thus increase the heat transfer from the component into the surroundings while offering a compact cooling system. The majority of the microchannels studies in the literature are based on the single-layer microchannels (SLMCs). The disadvantage of the SLMCs is the relatively high streamwise temperature rise which can have an adverse influence on the equipment. The high streamwise temperature rise is caused by heat released by the

equipment and carried out by a relatively small amount of coolant, which results a high streamwise temperature. Hence the undesired high temperature rise causes larger thermal stress, for example, in chips and electronic packages due to the coefficient of thermal expansion mismatch among different materials thus undermining device reliability. One way to reduce the undesired temperature rise in the single layered microchannels is to increase the pumping power, which can generate more noise and require bulk packaging. The other way is to use two-phase microchannels which can solve the large temperature variation problem by using the latent heat. But the structure of the device is complicated and require much more pressure drop for the gas-liquid mixture flowing into the small and compact device. However, the double-layered microchannels (DLMCs), first established by Vafai and Zhu [17-20], reduce the undesired temperature gradient in the streamwise direction. The design concept it based on a two-fold microchannel structures, one atop another. For the schematic diagram of the concept, see Figure 1.10. For such an arrangement, streamwise temperature rise for the coolant and the substrate in each layer are remunerated through conduction between the two layers. Since the temperature gradient is much smaller than the SLMCs, the required pressure drop can be substantially smaller than SLMCs, which can require a significantly smaller pumping power. With reduced thermal resistance and streamwise temperature rise and higher heat removal ability, DLMCs will significantly contribute to the heat removal of 3D ICs.

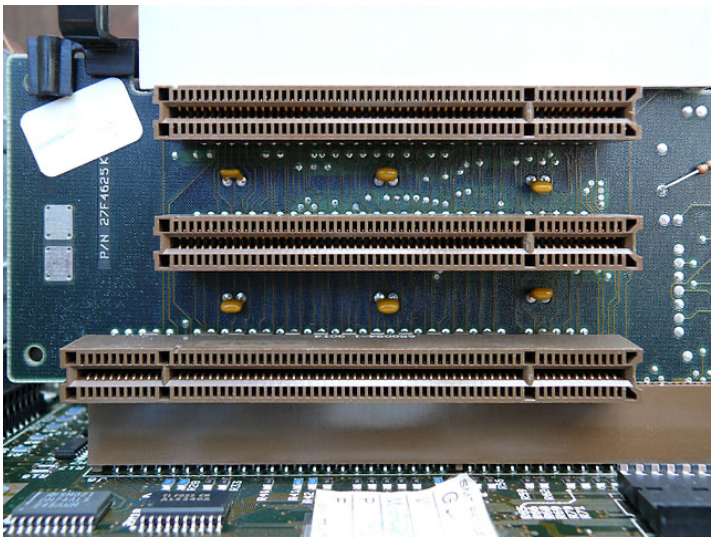

Figure 1.9 Microchannel Architecture. This picture is in the public domain and is taken by K. Reichert under the license of Creative Commons Attribution-Share Alike 3.0

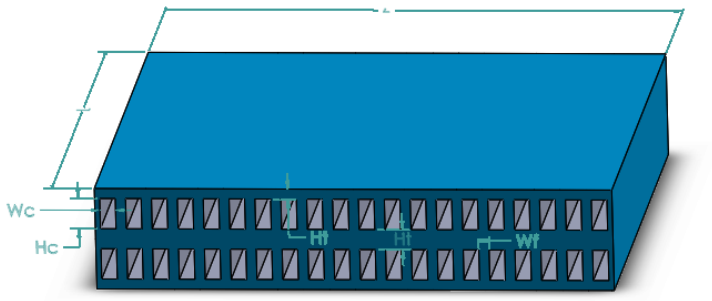

Figure 1.10 The schematic of a double-layer microchannel.

1.6 Dissertation Outlines

Three-dimensional integrated circuit (3D IC) is a promising solution for modern technology as 2D integrated circuits and embedded system are not able to meet the increasing need for smaller, thinner but more powerful electronic systems. 3D ICs have the advantages of superior performance, higher bandwidth, shorter interconnect, higher package density, condensed footprint but reduced power consumption and accommodating homogeneous and heterogeneous packaging. However, the bottleneck of heat built up within 3D ICs is still a challenge in the industries.

This work addresses the thermal issues by utilizing the flat-shape heat pipes and double-layer microchannels. Heat sinks have a significant impact on the overall thermal performance of 3D ICs and the junction temperature. To optimize the performance of a heat sink will contribute to the thermal performance of the whole device. Chapter 2 focuses on the numerical analysis of the thermal performance of the innovative 3D IC structures by utilizing the rectangular-shaped heat pipes and disk-shaped heat pipes. The optimization and innovations of the thermal performance are discussed and studied in details. Chapter 3 is on the analysis of the integrated chip-size double-layer and multi-layer microchannels. The reductions of the hotspot temperatures in various structures are presented and weight and size reductions compared with the nominal copper heat sinks are displayed. In addition, two integrated chip-size double-layer microchannels are investigated to optimize the thermal performance of the 3D IC. Finally, the effect of the nanofluids within the microchannels are discussed in this chapter. Chapter 4 is on the additional work in this

dissertation, which paved the way to have the accurate and meaningful results for chapter 2 and 3. Chapter 5 is on the summary and conclusions of the dissertation, and opportunities for future work.

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Chapter 2

Optimization of the Thermal Performance of Three-Dimensional Integrated Circuits (3D ICs) Utilizing Rectangular-shaped and Disk-shaped Heat Pipes

2.1 Abstract

Rectangular-shaped and disk-shaped heat pipes, as innovative heat sinks, are investigated to optimize the thermal performance of three-dimensional integrated circuits (3D ICs) in this work. Finite volume numerical analysis is employed to carry out the simulation of the thermal performance of 3D ICs. Both rectangular-shaped and disk-shaped heat pipes substantially improved the overall thermal performance and reduced the hotspot temperatures by 7 K and 11 K on average, respectively. Furthermore, utilizing the rectangular-shaped or the disk-shaped heat pipe as the heat spreader in place of a solid copper heat spreader further optimizes the thermal performance by reduction of the junction temperatures 14 K and 16 K on average, respectively. These reductions are achieved while the weight of the set-up is also significantly reduced. The results indicate that the innovative flat-shaped heat pipes significantly optimize the thermal performance of 3D ICs. The model and results presented in this work aim to pave the way to markedly alleviate the thermal issues of the 3D ICs.

2.2 Introduction

Moore's law has been applicable for many of the electronics advancements. The issue of coming up against proper thermal management prevents these features from being produced much smaller. Hence, the industry has moved from a two-dimensional approach to a three-dimensional set-up to utilize the volume more efficiently. A three-dimensional integrated circuit (3D IC) is a metal-oxide semiconductor integrated circuit manufactured by stacking silicon wafers or dies and interconnecting them vertically using through-silicon vias (TSVs), such that they behave as a single integrated device to achieve higher performance, lower power consumption, higher functional density, lower transistor packaging density, and a smaller formfactor than conventional two-dimensional integrated circuits.

Despite all these benefits, heat built up within the stacks must be removed. 3D ICs pack an extraordinary amount of complexity into an extremely small space, which creates a substantial amount of heat, resulting in damage to the device's reliability. Thermal hotspots in 3D ICs can exacerbate failure mechanisms such as junction leakage and electromigration, resulting in degradation of the device's performance. It is increasingly important to have effective and efficient thermal management in order to optimize the design characteristics of 3D ICs. Discussions regarding this topic have dominated research in recent years. Santos et al. [1] demonstrated that non-thinned stacked dies may act as heat spreaders to alleviate hotspot issues. It was also proposed in that study that graphite-based heat spreaders can be used as an alternative to compensate the poor heat dissipation

exhibited in 3D ICs. Zhang et al. [2] concluded that the embedded microfluidic cooling shows significant junction temperature reduction compared to air-cooling by evaluating the hotspot temperature of different architectures of 3D ICs experimentally. Chiang et al. [3] discussed the thermal performance with various integration schemes of 3D ICs and showed that the effects of vias are crucial in analyzing the thermal performance. Tavakkoli et al. [4, 5] performed a comprehensive thermal analysis of 3D high performance chips using numerical simulations. The effect of parametric changes in the geometrical configuration on the temperature distribution and hotspot temperature were extensively highlighted, such as size, number and spacing, TSV arrangements (nominal TSVs, uniform TSVs and core-concentrated TSVs). The investigation also sufficiently outlined the impact of the thermophysical properties of the chip and cooling fluid on the flow and heat transfer. Their results presented the key features to be used for establishing optimized design and setup of 3D ICs. And it was established that a core-concentrated TSV arrangement is the foremost emplacement of the optimized TSV arrangement in varied cases. Wang et al. [6] performed the heat transfer computational fluid dynamic analysis to study the effects of geometric and thermal properties of multilayer nominal 3D IC chips on the temperature hotspots with different distributions of processors (overlapped cores and staggered cores). They found that the larger the number of the chip layers, the higher the hotspot temperature is; but having a large Reynolds number can help decrease the hotspot temperature. And with core-concentrated thermal TSVs, the staggered cores have better thermal performance at a lower number of layers (2-8) while the overlapped core structure performed better at a higher number of layers (10-18). Xiao et al. [7] performed the FEA and 3D CFD analysis

under a natural convection environment on the thermal performance of 3D stacked ICs and proposed a fast and accurate approach to estimate equivalent thermal conductivity of interposer with various TSV parameters. They advocated that a smaller TSV diameter and SiO_2 thickness and a greater TSV pitch will increase the equivalent thermal conductivity in the x-y direction but a smaller TSV pitch and SiO2 thickness and a larger TSV diameter will raise the equivalent thermal conductivity in the z direction. It was also mentioned that the maximum junction temperature difference between each layer of stacked chips is negligible for the uniform heat source setting, while the thinner chip would result in noticeable hot spots. However, this conclusion is based on 3D ICs without heat sinks. With heat sinks, Tavakkoli et al. [4, 5] concluded that the device layer that is farthest from heat sink is exposed to a higher temperature compared to the device layer that is closer to the heat sinks. Jain et al. [8] developed analytical and finite-element models of heat transfer in stacked 3D ICs to investigate the impact of various geometric parameters and thermophysical properties on the thermal performance. This investigation established that package and heat sink thermal resistances play a more important role in determining the rise in temperature compared to inter-die bond thermal resistances.

Heat sinks are essentially heat dissipation devices for removing heat from a heat source, such as processors and GPUs, to keep the source at a proper operating temperature. Heat sinks are crucial in optimizing the thermal performance of 3D ICs. Heat pipes can be excellent heat sinks and have been contributing to the thermal management in existing integrated circuit technology. A heat pipe is a vacuum sealed metal tube that contains a working fluid that changes from liquid to vapor when heat is applied to one end of the tube.

The heated vapor moves quickly to the other end of the tube where it condenses then travels through the wick material (sintered copper) back to the heat source section. This design allows heat pipes to transfer heat much more efficiently than a solid piece of metal with the added benefits of being much lighter weight and performing well in any orientation. It has been well established in many applications, such as spacecraft thermal controls, electronic systems cooling and many commercial thermal devices. However, the traditional heat pipes have some limitations; for instance, they only transfer heat in one direction and the round shape makes it physically difficult to get close to a very small heat source. Vafai et al. [9-13] had established and analyzed comprehensively flat-shaped heat pipes that can overcome the limitations of the traditional heat pipes. The flat-shaped heat pipes offer an effective solution for the high heat generation of 3D ICs and have far-reaching impact on the thermal management of 3D ICs with unrivaled advantages, such as a secondary feeding mechanism, substantially better geometric adoptability for complex applications and ability to fully handle the asymmetrical heat load.

In this research, the utilization of the flat-shaped heat pipes as heat sinks and heat spreaders on the thermal performance of 3D ICs with core-concentrated TSVs arrangement are thoroughly investigated. The significant effect of flat-shaped heat pipes on the reduction of junction temperature and the overall thermal performance of the 3D IC structure is established in this work.

2.3 Modeling and Analysis

2.3.1 3D IC model and analysis

The schematic of the nominal 3D IC structure is shown in Figure 1.1 as shown in Tavakkoli et al. [4, 5]. As can be seen, the 3D IC structure incorporates a substrate, a thermal interface material (TIM) layer with C4 bumps, three layers of dies, device layers and thermal interface materials with microbumps, a heat spreader and a flat-shaped heat pipe as the heat sink. Device layers, bonded between TIM with microbumps and die, comprises four processors which are the main heat. Table 1 displays the nominal values for different components of the 3D IC structure, including materials, length and width, and thickness.

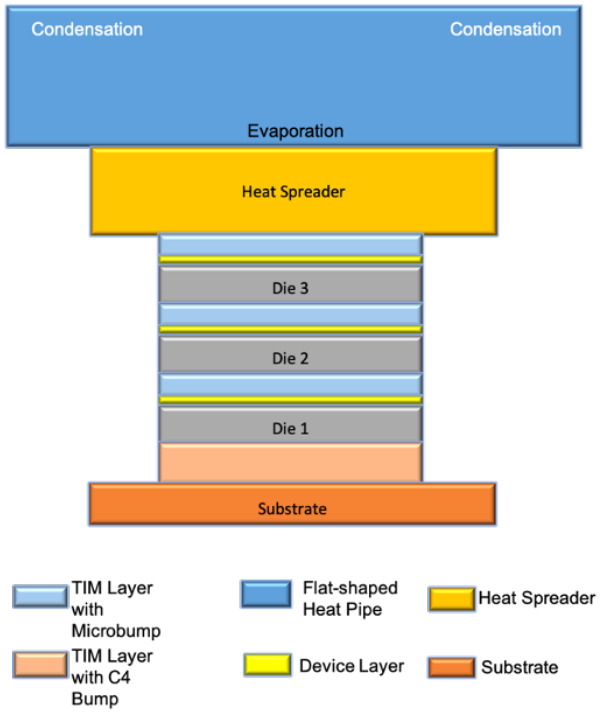


Figure 2.2.1 The Schematic of a nominal 3D IC structure

The nominal heat dissipation (30W each layer) produced by the transistors in the processors, are conducted through the layers to the substrate downward and to the heat spreader, and subsequently dissipated to the heat sink upward and eventually to the ambient air through convective heat transfer.

Table 2.1 Nominal Value for various parameters within the 3D IC structure

Layer	Parameter	Nominal Value	Unit	References
Heat sink	Material	Cu		
	Length & Width	50	mm	[4,5], [15-17]
	Thickness	4	mm	
Rectangular-shaped heat pipe	Material	Cu		
	Length & Width	50	mm	[4,5], [9-13]
	Thickness	29.4	mm	
Disk-shaped heat pipe	Material	Cu		
	Radius	28	mm	[4,5], [9-13]
	Thickness	29.4	mm	
Heat spreader	Material	Cu		
	Length & Width	30	mm	[4,5], [15], [16], [18]
	Thickness	2-3	mm	
Chip	Length & Width	10	mm	[4,5], [18], [19]
	Number of layers	3		
TIM layer with microbump	TIM material	Thermal grease		
	Thermal conductivity	5	W/m·K	[4,5], [15], [16], [24]
	Thickness	15	µm	
TIM layer with C4 bump	TIM material	Thermal grease		
	Thermal conductivity	5	W/m·K	[4,5], [15], [16], [24]
	Thickness	100	µm	
Die	Material	Si		[4,5], [15], [16], [20]
	Thickness	100	µm	
Device layer	Material	Si		[4,5], [18], [20]
	Thickness	2	µm	
Core processor	Material	Si		
	Total power within the 3D IC	90	W	
	Cores per layer	4		[4,5], [15], [16], [18], [19], [21], [22], [23]
	Length & Width	2	mm	
	Thickness	2	µm	
Substrate	Material	Si		
	Length & Width	30	mm	[4,5], [23], [24]
	Thickness	1	mm	

Conductive heat transfer through the solid, and isotropic layers of the 3D IC are governed by:

$$\frac{\partial^2 \Theta_s^+}{\partial x^{+2}} + \frac{\partial^2 \Theta_s^+}{\partial y^{+2}} + \frac{\partial^2 \Theta_s^+}{\partial z^{+2}} + q_g^+ = 0 \qquad (2.1)$$

Where q_g^+ denotes the dimensionless volumetric heat generation in the central processing units and the nondimensionalized temperature and coordinates are set up as:

$$x^+ = \frac{x}{h}, \qquad y^+ = \frac{y}{h}, \qquad z^+ = \frac{z}{h}, \qquad \Theta^+ = \frac{T - T_e}{qh/k_f}$$

The natural convective heat transfer is replayed at the bottom surface of the substrate, whereas the forced convection is administered at the top surface of the flat-shaped heat pipes. The convective boundary conditions are:

$$\frac{\partial \Theta_s^+}{\partial n} = -Bi \cdot \Theta_s^+ \qquad (2.2)$$

Where n is the normal coordinate and Bi is the dimensionless Biot number.

The heat transfer and fluid flow are based on the Navier-stokes equations. The cooling fluid enters into the 3D IC package at ambient temperature with a specified Reynolds number and exits the package at atmospheric pressure with negligible streamwise temperature change. The dimensionless Navier-Stokes equations in Cartesian coordinates are:

Mass conservation:

$$\frac{\partial u^+}{\partial x^+} + \frac{\partial v^+}{\partial y^+} + \frac{\partial w^+}{\partial z^+} = 0 \tag{2.3}$$

x-Momentum equation:

$$Re_h \left(u^+ \frac{\partial u^+}{\partial x^+} + v^+ \frac{\partial u^+}{\partial y^+} + w^+ \frac{\partial u^+}{\partial z^+} \right) = -\frac{\partial p^+}{\partial x^+} + \left(\frac{\partial^2 u^+}{\partial x^{+2}} + \frac{\partial^2 u^+}{\partial y^{+2}} + \frac{\partial^2 u^+}{\partial z^{+2}} \right) \tag{2.4}$$

y-Momentum equation:

$$Re_h \left(u^+ \frac{\partial v^+}{\partial x^+} + v^+ \frac{\partial v^+}{\partial y^+} + w^+ \frac{\partial v^+}{\partial z^+} \right) = -\frac{\partial p^+}{\partial y^+} + \left(\frac{\partial^2 v^+}{\partial x^{+2}} + \frac{\partial^2 v^+}{\partial y^{+2}} + \frac{\partial^2 v^+}{\partial z^{+2}} \right) \tag{2.5}$$

z-Momentum equation:

$$Re_h \left(u^+ \frac{\partial w^+}{\partial x^+} + v^+ \frac{\partial w^+}{\partial y^+} + w^+ \frac{\partial w^+}{\partial z^+} \right) = -\frac{\partial p^+}{\partial z^+} + \left(\frac{\partial^2 w^+}{\partial x^{+2}} + \frac{\partial^2 w^+}{\partial y^{+2}} + \frac{\partial^2 w^+}{\partial z^{+2}} \right) \tag{2.6}$$

Energy conservation for the fluid domain:

$$Pe_h \left(u^+ \frac{\partial \Theta_f^+}{\partial x^+} + v^+ \frac{\partial \Theta_f^+}{\partial y^+} + w^+ \frac{\partial \Theta_f^+}{\partial z^+} \right) = \frac{\partial^2 \Theta_f^+}{\partial x^{+2}} + \frac{\partial^2 \Theta_f^+}{\partial y^{+2}} + \frac{\partial^2 \Theta_f^+}{\partial z^{+2}} \tag{2.7}$$

The nondimensionalized terms in the above equations are:

$$u^+ = \frac{u}{u_m}, \qquad v^+ = \frac{v}{v_m}, \qquad w^+ = \frac{w}{w_m}, \qquad p^+ = \frac{ph}{\mu_f u_m},$$

$$Re_h = \frac{\rho_f u_m h}{\mu_f}, \qquad Pe_h = \frac{\rho_f \, c_{p,f} u_m h}{k_f}$$

2.3.2 Flat-shaped heat pipe model and analysis

The design and set up of a rectangular-shaped or disk-shaped heat pipe in previous works of Vafai et al. [9-13] are deployed in this work. The cross-sectional view of the heat pipe is displayed as Fig. 2. The assumptions made in this model are: (1) Vapor and liquid flow are steady, laminar and subsonic. (2) Transport properties for the vapor and liquid are taken as constant. (3) The vapor injection and suction rate are uniform in the evaporator and condenser sections. (4) The vapor velocity component in the z direction is negligible since there is no injection or suction on vertical wicks.

The analytical solution for the vapor pressure distribution, liquid pressure distribution and temperature distribution for the rectangular-shaped heat pipe and disk-shaped heat pipe are documented in Vafai et al. [9-13]. Based on the analysis given in these works, we can obtain the rectangular and disk-shaped vapor and liquid pressure and temperature distributions, as given in eqs. (1.8) to (1.14) which are used to validate our model.

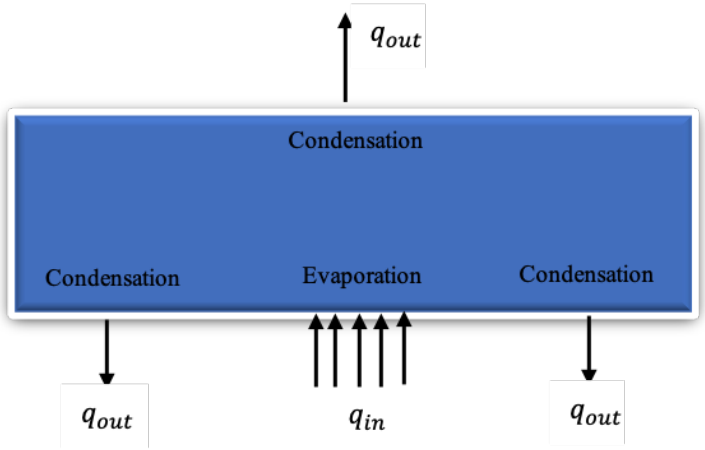


Figure 2.2.2 The cross-sectional view of a rectangular-shaped or disk-shaped heat pipe

2.3.2.1 Rectangular-shaped heat pipe's vapor pressure distribution

$$\Delta p_v^+(x^+) = \tag{2.8}$$

$$\begin{cases} -\dfrac{4(1-\varphi)}{(2-\varphi)}\, Re_h \left\{\left[\dfrac{16(1-\varphi)}{25\,\varphi}\, Re_h + \dfrac{1}{2(h_b^+)^2}\right](x^+)^2 + \displaystyle\int_0^{x^+} \frac{x^+}{f^+(x^+)\left(1-f^+(x^+)\right)}dx^+\right\} \\ \qquad (0 \le x^+ \le \varphi\, l^+) \\ \Delta p(\varphi l^+) \\ -\dfrac{4\varphi}{(2-\varphi)}\, Re_h \left\{\left[\dfrac{16\,\varphi}{25(2-\varphi)}\, Re_h - \dfrac{1}{2(h_b^+)^2}\right][(x^+ - l^+)^2 - (\varphi\, l^+ - l^+)^2] \right. \\ \left. -\displaystyle\int_0^{x^+} \frac{x^+ - l^+}{f^+(x^+)\left(1-f^+(x^+)\right)}dx^+\right\} \\ \qquad (\varphi\, l^+ \le x^+ \le l^+) \end{cases}$$

Where $f^+(x^+)$ can be found from:

$$\frac{df^+(x^+)}{dx^+} = \tag{2.9}$$

$$\begin{cases} \left[-\dfrac{9}{2}(1-\varphi)f^+(x^+) + 5\dfrac{(2-\varphi)}{Re_h}\dfrac{1}{f^+(x^+)} - \dfrac{5}{2}\varphi\right]\dfrac{1}{(1-\varphi)x^+} & (0 \le x^+ \le \varphi\, l^+) \\ \left[-\varphi f^+(x^+) + 10\dfrac{(2-\varphi)}{Re_h}\dfrac{1}{f^+(x^+)}\right]\dfrac{1}{7\,\varphi(l^+ - x^+)} & (\varphi\, l^+ \le x^+ \le l^+) \end{cases}$$

1.3.2.2 Rectangular-shaped heat pipe's liquid pressure distribution

$$\Delta p_l^+(x^+) = \tag{2.10}$$

$$\begin{cases} \Delta p_v^+(l^+) - \frac{h_w^+\mu^+(1-\varphi)\,Re_h}{2(2-\varphi)K^+}\{\varphi(1-\varphi)(l^+)^2 + [(\varphi l^+)^2 - (x^+)^2]\} \\ \qquad (0 \le x^+ \le \varphi\, l^+) \\ \Delta p_v^+(l^+) - \dfrac{h_w^+\mu^+\varphi\, Re_h}{2(2-\varphi)K^+}(l^+ - x^+)^2 \qquad (\varphi\, l^+ \le x^+ \le l^+) \end{cases}$$

1.3.2.3 Rectangular-shaped heat pipe's temperature distribution

$$\Delta T_v^+(x^+) = (T_{ov}^+)^2 \left[\frac{\ln p_v^{+2}(x^+) - \ln p_{ov}^+}{1 - T_{ov}^+(\ln p_{ov}^+ - \ln p_v^+(x^+))}\right] \tag{2.11}$$

1.3.2.4 Disk-shaped heat pipe's vapor pressure distribution

$$p_v^+(r^+) = \tag{2.12}$$
$$\begin{cases} p_v^+(0) - \frac{24}{25}\left(\frac{1-\varphi^2}{2-\varphi^2} Re_h R^+\right)^2 \left(\frac{r^+}{R^+}\right)^2 & (0 \le r^+ \le \varphi R^+) \\ p_v^+(0) - \frac{8}{25}\left(\frac{\varphi^2}{2-\varphi^2} Re_h R^+\right)^2 \left[3\left(\frac{r^+}{R^+}\right)^2 + \left(\frac{R^+}{r^+}\right)^2 - 4\ln\frac{r^+}{R^+} - 2\left(3 - 2\ln\varphi - \frac{1}{\varphi^2}\right)\right] & (\varphi R^+ \le r^+ \le R^+) \end{cases}$$

1.3.2.5 Disk-shaped heat pipe's liquid pressure distribution

$$p_l^+(r^+) = \tag{2.13}$$
$$\begin{cases} p_v^+(0) + \frac{\nu^+ Re_h (R^+)^2}{4K^+(h_w^+)^3}\frac{1-\varphi^2}{2-\varphi^2}\left[\left(\frac{r^+}{R^+}\right)^2 + \frac{2\varphi^2}{2-\varphi^2}\ln\varphi\right] \\ -\left(\frac{4}{5}\frac{\varphi^2 Re_h}{2-\varphi^2}R^+\right)^2\left(2\ln\varphi + \frac{1}{\varphi^2} - 1\right) & (0 \le r^+ \le \varphi R^+) \\ p_v^+(0) + \frac{\nu^+ Re_h (R^+)^2}{4K^+(h_w^+)^3}\frac{\varphi^2}{2-\varphi^2}\left[1 - \left(\frac{r^+}{R^+}\right)^2 - 2\ln\left(\frac{R^+}{r^+}\right)\right] \\ -\left(\frac{4}{5}\frac{\varphi^2 Re_h}{2-\varphi^2}R^+\right)^2\left(2\ln\varphi + \frac{1}{\varphi^2} - 1\right) & (\varphi R^+ \le r^+ \le R^+) \end{cases}$$

1.3.2.6 Disk-shaped heat pipe's temperature distribution

$$\Delta T_v^+(r^+) = (T_{ov}^+)^2 \left[\frac{\ln p_v^+(r^+) - \ln p_{ov}^+}{1 - T_{ov}^+(\ln p_{ov}^+ - \ln p_v^+(r^+))}\right] \tag{2.14}$$

Once the vapor pressure distribution is found, the vapor temperature distribution within the heat pipe can be obtained from equations (2.11) and (2.14). The temperature difference across the heat pipe may be employed to calculate the effective thermal conductivity of the rectangular-shaped heat pipe and disk-shaped heat pipe with the Eqs. (2.15) and (2.16) [14].

$$k_{eff} = \frac{QL_{eff}}{A\,\Delta T} \tag{2.15}$$

$$L_{eff} = \frac{L_{evaporator} + L_{condenser}}{2} + L_{adiabatic} \tag{2.16}$$

Where k_{eff} is the effective thermal conductivity; Q is the power transported; L_{eff} is the effective length; A is the cross-sectional area; ΔT is the temperature difference between evaporator and condenser sections. In this study, the evaporator section is on the bottom surface of the heat pipe and the rest of the heat pipe's external area acts as the condenser section. Once the effective thermal conductivity is obtained, the heat pipe employed for the 3D IC structure will be modeled as a solid flat plate in the system. It should be noted that the rectangular shaped and disk-shaped heat pipes not only possess the extraordinary heat transfer capacity and rate, but also lighter in weight when compared

to solid copper of the same size. This makes their use even more appealing. The nominal dimension of the heat pipe is 50×50×29.4 mm^3 in this investigation, in which the total height of the wick structure is 4 mm. The rest of the volume is a vapor channel, which is negligible in weight. Compared to the same sized solid copper plate, the weight of the heat pipe is over 7 times lighter.

2.4 Modeling Validation

COMSOL Multiphysics is utilized to set up the simulations. For model validation, a grid independence study was executed for all investigated geometries and the junction temperature for each geometry was evaluated using computational meshes for different cell distributions. Figure 1.3 presents the grid independence study for the nominal cases applying customized coarser, coarse, normal and fine mesh distributions. It can be concluded that there is no advantage to further increasing the number of grid cells after coarse mesh distribution. The last refined mesh gives a relative difference of %0.02 for the hotspot temperature in comparison with the prior mesh. To minimize the computational cost while maintaining the accuracy of the simulation, the coarse mesh distribution is applied in this study.

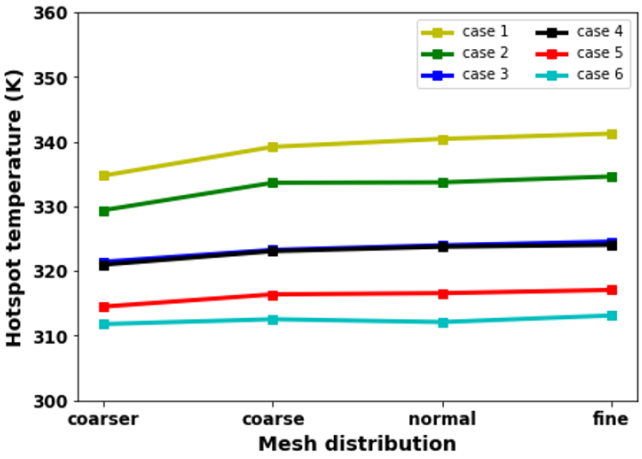
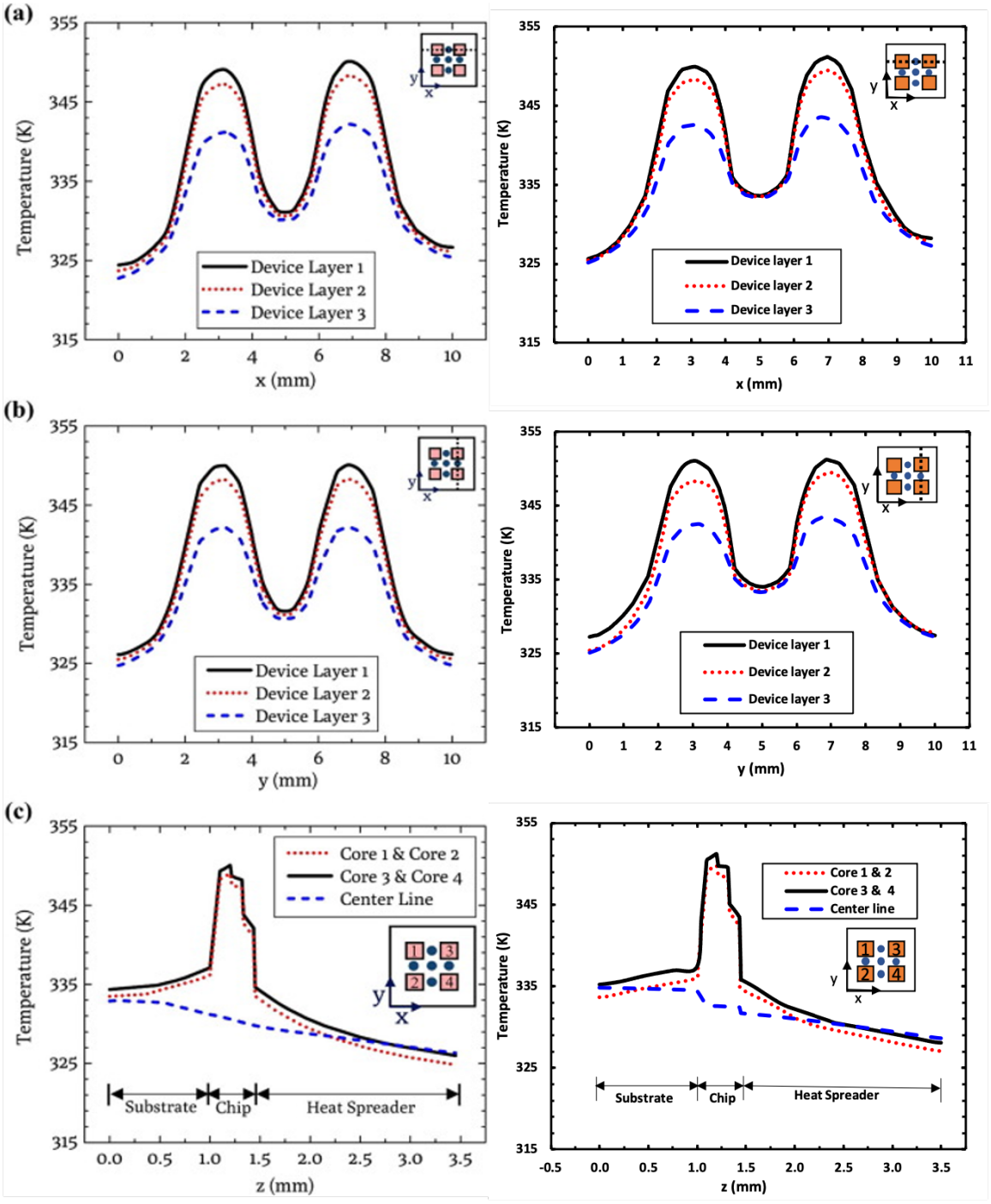


Figure 2.2.3 Grid independence study for the investigated geometries

To ratify the model, the temperature distribution of the 3D IC is validated with both the previous simulation work of Tavakkoli et al. [4] and the experimental results from Zhang et al. [2]. The vapor pressure distribution, liquid pressure distribution and temperature distribution within the rectangular-shaped heat pipe is compared with the comprehensive analytical solution of Vafai and Wang [9]. Figure 2.4 illustrates the resemblance of the temperature distribution for the nominal benchmark 3D IC along the x, y, and z directions for each device layer between the work of Tavakkoli et al. [4] and the present work. Figure 2.5 displays the comparison of the effect of different TSV arrangements on the temperature distribution of the 3D IC structure along the x, y and z directions in the device layer 1. It should be recognized that the z direction is at the vertical center line of the core processor 3. The comparisons between these two works show very good agreement.

The model is further validated by the experimental results obtained by Zhang et al. [2], where the setup model is similar with our simulation model. Zhang et al. [2] set up the

air-cooled 3D IC stack with two layers of stacked processors instead of three for the current simulation model. For the validation purpose, the simulation of two layers of stacked processors is implemented to compare the hotspot temperature in the simulation model with the experimental results. Figure 2.6 substantiates the validation of the 3D IC model setup used in the research work. Figures 2.7 and 1.8 exhibit a comparison of our results for the flat-shaped heat pipes with the comprehensive analytical results acquired by Vafai & Wang [9].



Tavakkoli et al. (2016) Present work

Figure 2.2.4 Comparison of the Temperature distribution for the nominal benchmark 3D IC with Tavakkoli et al. [4,5] (a) along the x direction for each device layer (b)along the y direction for each device layer (c) along the z direction at the vertical center line of each core and the center line of chip

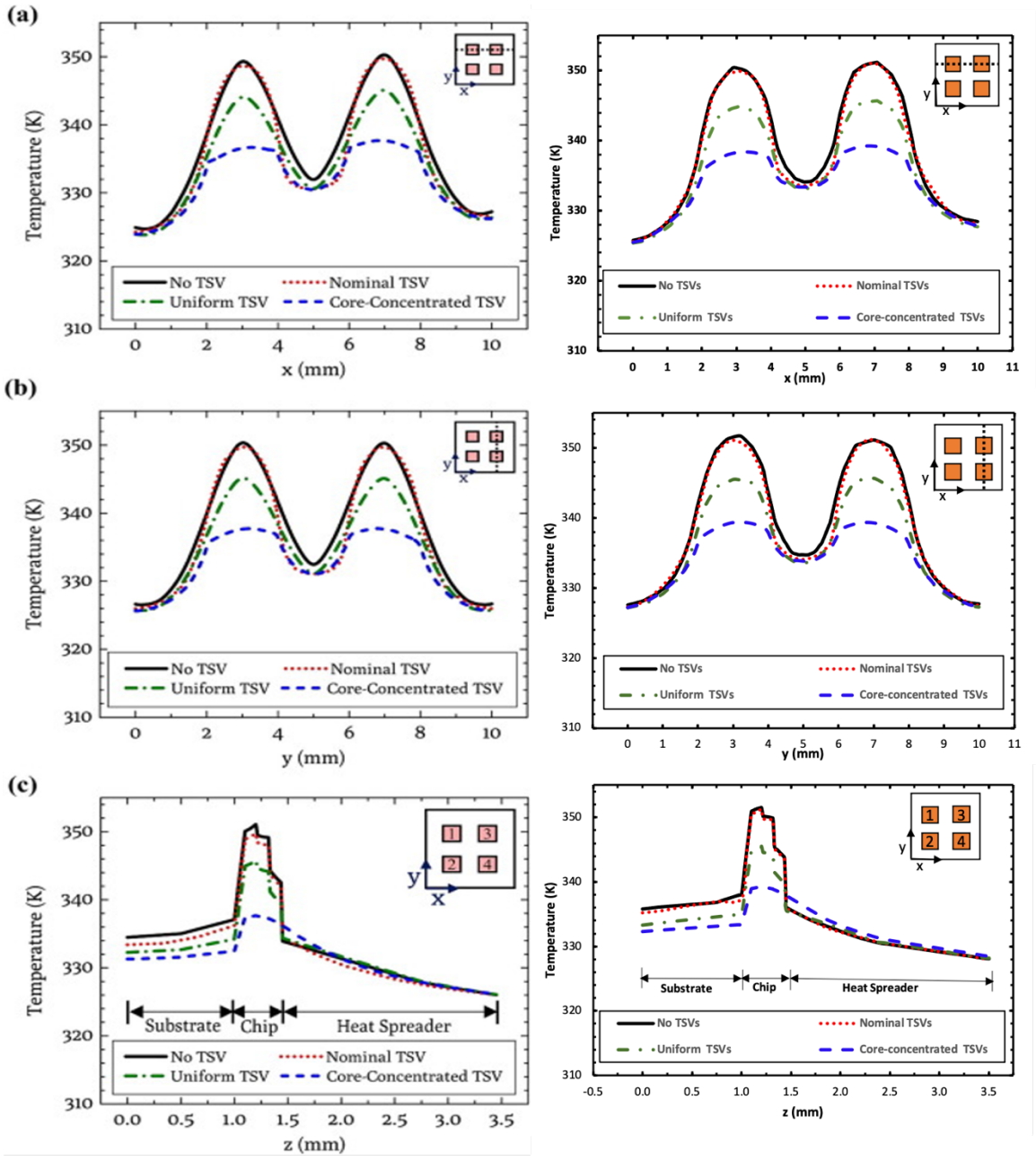


Figure 2.2.5 Comparison of the Effects of different TSV arrangements on the temperature distribution of the 3D IC structure with Tavakkoli et al. [4,5] (a) along the x direction in the device layer 1 (b) along the y direction in the device layer 1 (c) along the z direction at vertical center line of the core processor 3

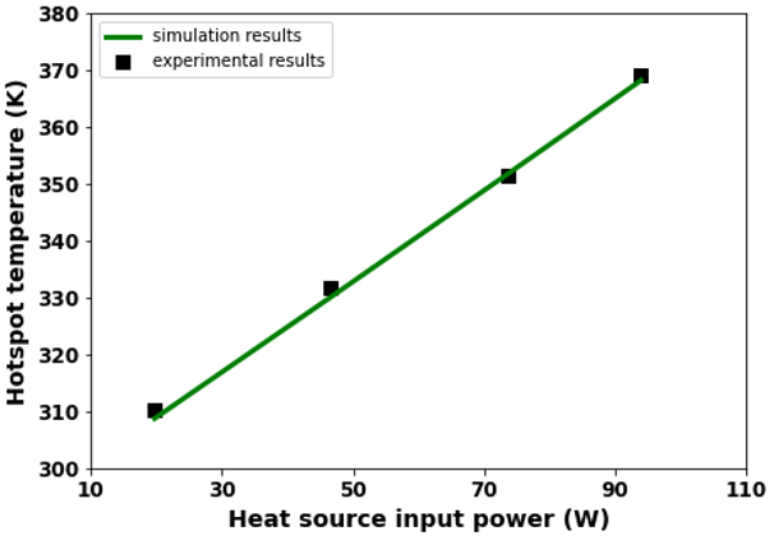
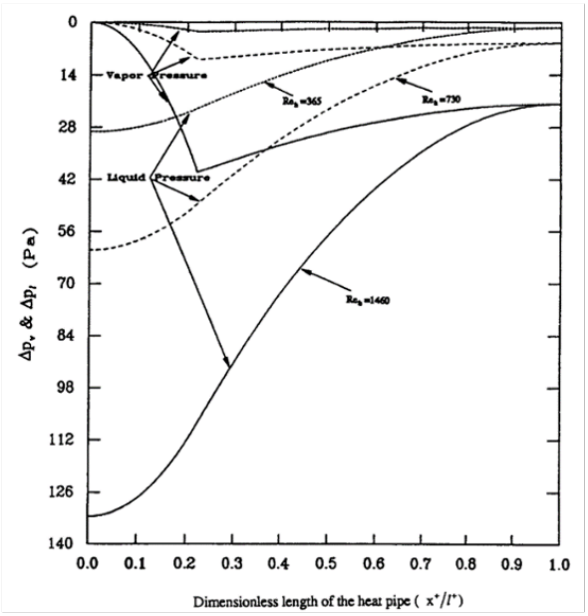


Figure 2.2.6 Comparison of the hotspot temperature with the experimental results



Vafai & Wang [9]

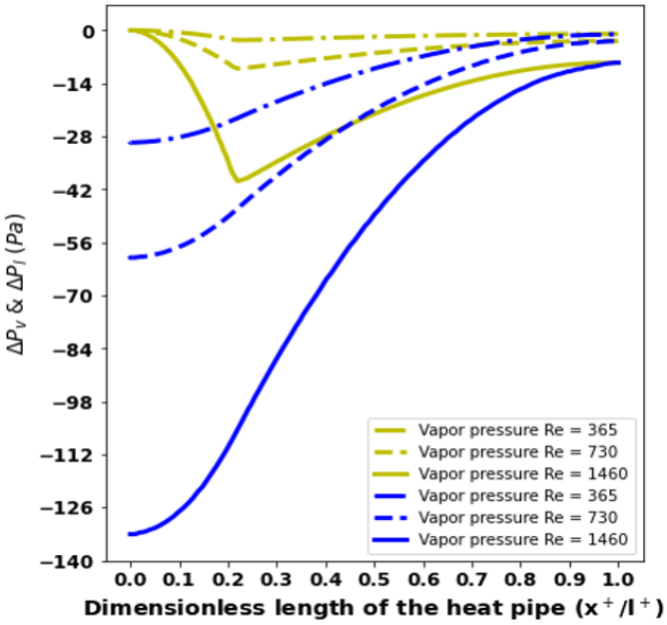


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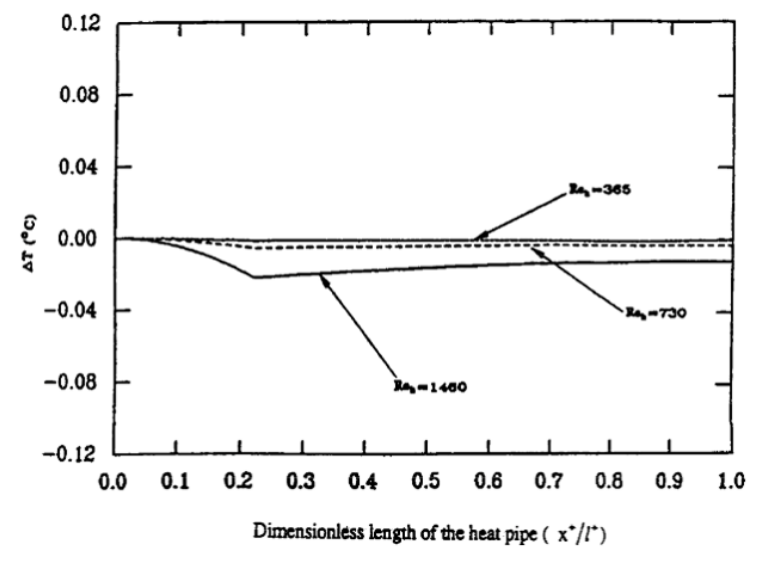
Figure 2.2.7 Comparison of the vapor and liquid pressure distributions along the heat pipe



Vafai & Wang [9]

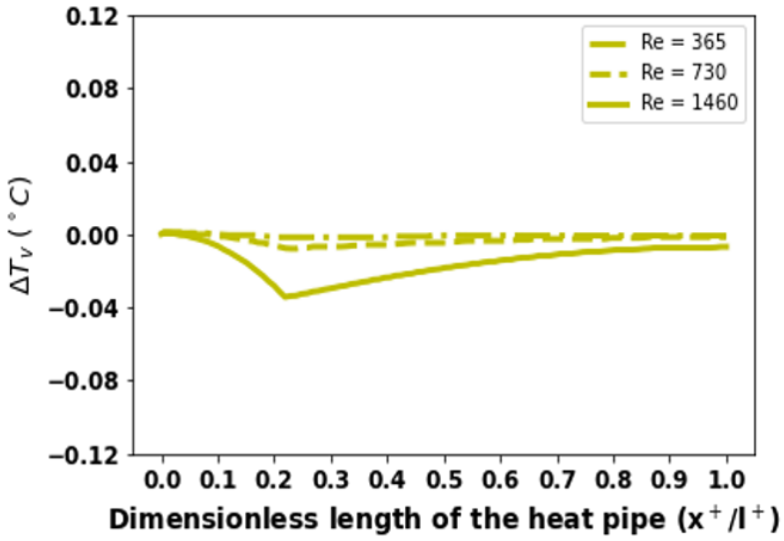


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Figure 2.2.8 Comparison of the vapor temperature profiles for different injection Reynolds numbers

2.5 Results and Discussions

The temperature distribution of a 3D IC deploying a copper heat sink, a rectangular-shaped heat pipe and a disk-shaped heat pipe with different heat sink lengths for device layer 1 is investigated. It was concluded in the work of Tavakkoli et al. [4] that the junction temperature is manifested in device layer 1. It should be emphasized that the core-concentrated TSV arrangement is employed throughout the study. The same study from Tavakkoli et al. [4] unveiled that the core-concentrated TSV is superior to the other employments of the optimized TSV arrangement. The current investigation is aimed to optimize the thermal performance based on the foremost employment with the preeminent performance in the previous work. As seen from Figure 2.9, as the length of the heat sinks increases, the temperature decreases for all three heat sinks. It is evident that the temperature of the 3D IC drops significantly when the heat sink length increases from 50 mm to 100 mm. The rate of temperature deduction is slower as the length increases further. Figure 2.9 (b) and (c) highlights the substantial effect of the rectangular-shaped and disk-shaped heat pipe on the performance of a 3D IC. The rectangular-shaped heat pipe improved the thermal performance by reducing the temperature by 8 degrees in all lengths compared to the copper heat sink. As it was strengthened in Vafai et al. [9-13] investigations, the disk-shaped heat pipe showed more advanced performance than the rectangular-shaped heat pipe. With the fixed contact surface area, Figure 2.9 (c) demonstrated a 16 degrees reduction in temperature when the length of the heat sink is 50 mm (R = 28 mm for the disk-shaped heat pipe) and an average 10 degrees in other lengths

compared to the copper heat sink. These findings reveal that both the rectangular-shaped and disk-shaped heat pipe contribute to the optimization of the thermal performance of the 3D IC by maximizing the heat conduction and minimizing the temperature rise in the 3D ICs.

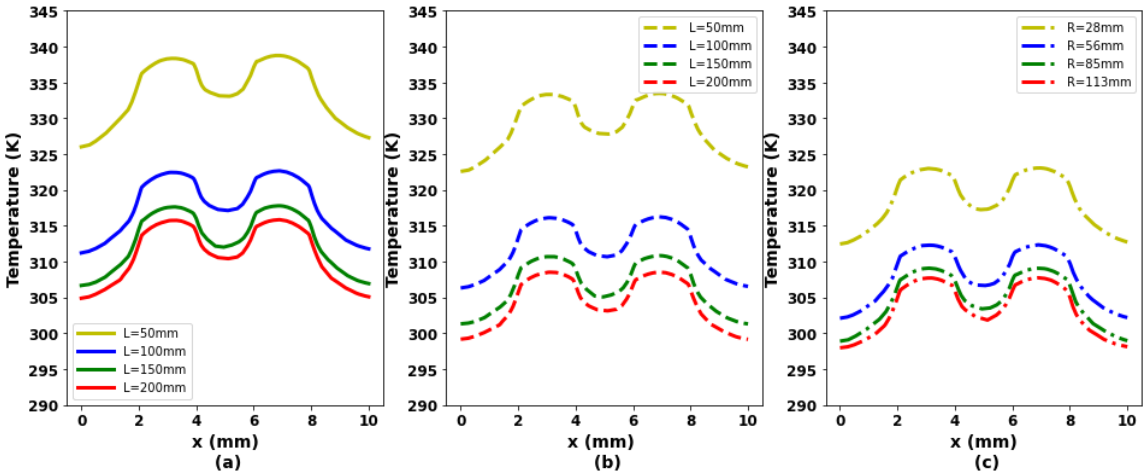

Figure 2.2.9 Device layer 1 temperature distribution for different lengths of the heat sinks (a) Copper heat sink (b) rectangular-shaped heat pipe (c) disk-shaped heat pipe

Figure 2.10. further unveils a comparison of different lengths of a flat-shaped heat pipe and a copper heat sink on the hotspot temperature of the 3D IC. The hotspot temperature declines remarkably when the rectangular-shaped heat pipe and disk-shaped heat pipe are implemented in the 3D IC structure. As anticipated, the disk-shaped heat pipe performs superior to rectangular-shaped one at all lengths. There is considerable drop in the hot spot temperature when using a flat shaped heat pipe as compared with a copper heat sink. In addition, as mentioned earlier we also have the advantage of a substantial reduction in the weight when using the flat-shaped heat pipes for the 3D IC set up.

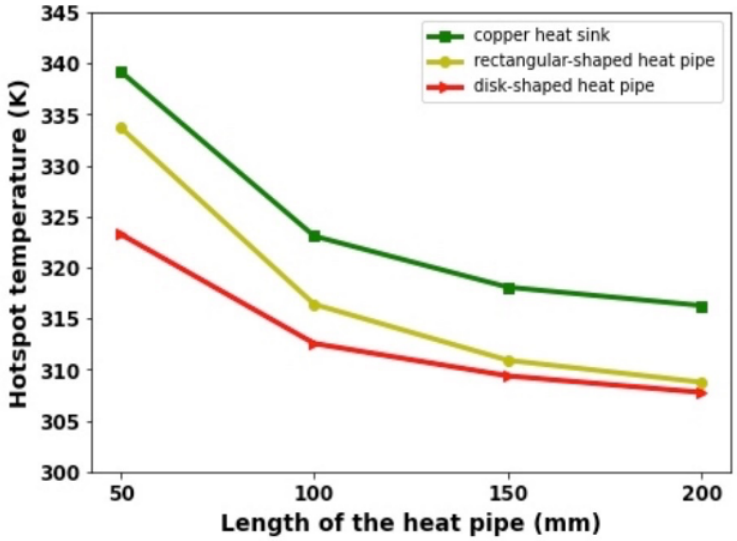

Figure 2.2.10 Effect of the lengths of the heat sink and flat-shaped heat pipes on the hotspot temperature for a nominal 3D IC structure

Figure 2.11. demonstrates the effect of increasing the heat dissipation on the hotspot temperature of a typical 3D IC utilizing a flat-shaped heat pipe compared with a copper heat sink. The allowed operating temperature for 11th Gen Intel $Core^{TM}$ i7 & i9 is 373 K. The 3D IC with a copper heat sink is heated up to 393.45 K at a power of 300 W resulting in the termination of the 3D IC, while the 3D IC with a rectangular flat-shaped heat pipe can operate under 300 W heat dissipation and the one executed with a disk-shaped heat pipe can reach nearly 400 W. These data establish the powerful effect of both the rectangular-shaped and disk-shaped heat pipes on the junction temperature for high-power processors.

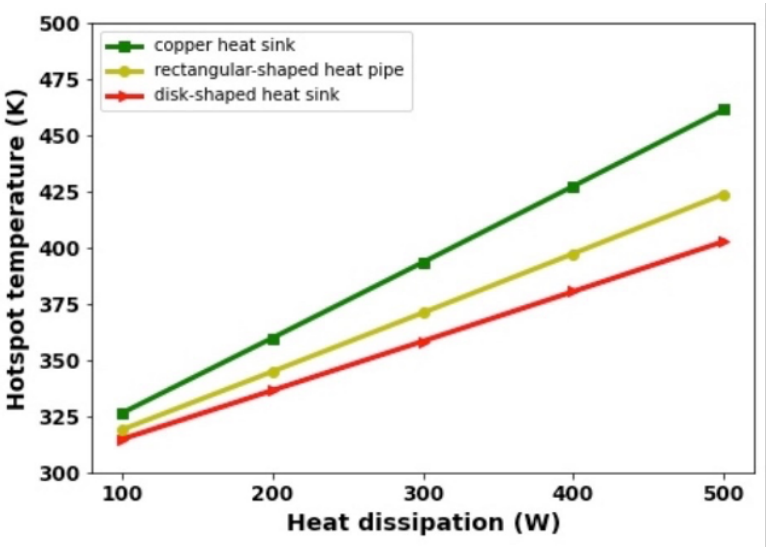

Figure 2.2.11 Effect of the flat-shaped heat pipe on the hotspot temperature of a typical 3D IC for different heat dissipation powers

For a typical fixed contact surface area 10,000 mm^2, the hotspot temperature for different configurations of a rectangular-shaped heat pipe is investigated ($50\times200\ mm^2$, $60\times167\ mm^2$, $70\times143\ mm^2$, $80\times125\ mm^2$, $90\times112\ mm^2$, $100\times100\ mm^2$). Figure 2.12 illustrates a moderate temperature drop of 2 K when using a square shaped flat-shaped heat pipe. That is the square shaped heat pipe ($100\times100\ mm^2$) carries the premier thermal performance for 3D IC.

The thermal resistances of the three different heat sinks are probed. As it can be observed from Figure 2.13, the average thermal resistance for the copper heat sink is about 0.104 K/W, while it is 0.0004 K/W for rectangular shaped heat pipe and almost zero for the disk-shaped heat pipe, respectively. These details authenticated the outstanding performance of the flat-shaped heat pipes compared to a copper heat sink.

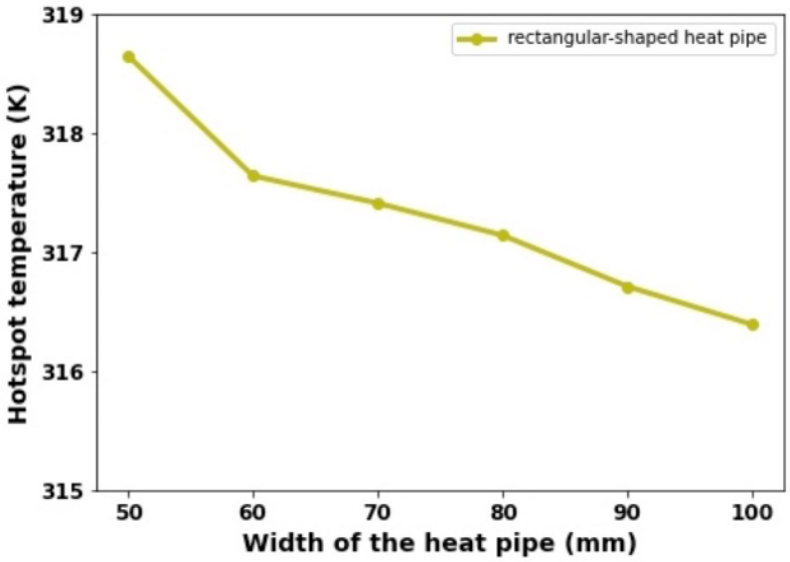

Figure 2.2.12 The effect of different configurations of the rectangular-shaped heat pipe on the hotspot temperature of a typical 3D IC configuration

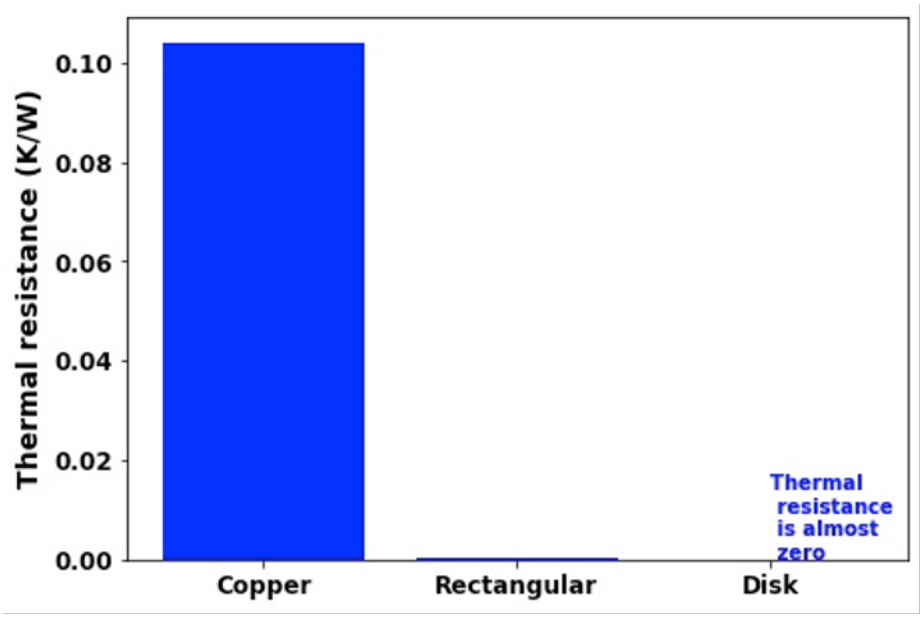

Figure 2.2.13 Thermal resistance of different heat sinks implemented in the 3D IC

Figure 2.14. presents the effects of the flat-shaped heat pipe as a heat spreader on the hotspot temperature. The size of the flat-shaped heat pipe as the heat spreader employed in the simulation is $50\times50\times 3\ mm^3$(R = 28 mm for disk-shaped one) with the effective thermal conductivity of 5000 W/m·K. The copper heat sink, rectangular-shaped heat pipe heat sink and disk-shaped heat pipe heat sink are administered on top of the copper heat spreader, rectangular-shaped heat pipe heat spreader and disk-shaped heat pipe heat spreader, respectively. It is seen that using a much lighter weight flat-shaped heat pipe as the heat spreader has a very substantial effect on the hotspot temperature of 3D ICs as opposed to a copper heat spreader of the same size. For a 3D IC with the heat sink length and width $100\times100\ mm^2$, the hotspot temperature using the copper heat sink with the copper heat spreader reaches 321.48 K, while the one applying rectangular heat pipes as the heat sink and the heat spreader reduces the hotspot temperature by over 13 K and the one utilizing the disk-shaped heat pipes as the heat sink and the heat spreader further enhances the thermal performance by decreasing the hotspot temperature by almost 17 K.

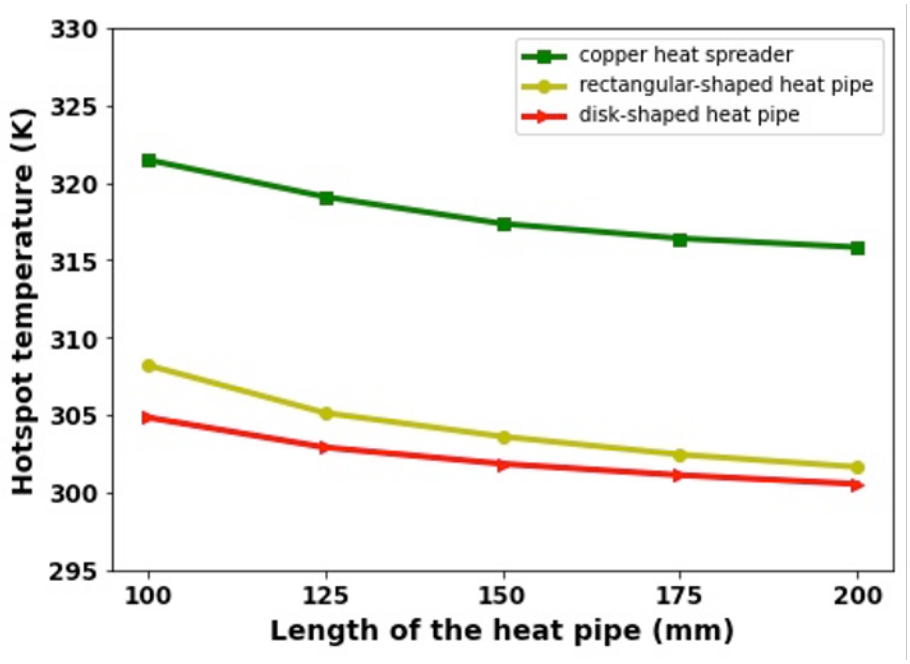

Figure 2.2.14 Effect of a flat-shaped heat pipe as the heat spreader on the hotspot temperature of a 3D IC

2.6 Summary and Conclusions

The optimization and the thermal performance and management of 3D ICs utilizing the innovative rectangular-shaped and disk-shaped heat pipes is investigated in this work. The effects of these innovative flat shaped heat pipes on the temperature distribution and hotspots are explored in detail. All the models investigated in this work were rigorously validated with established analytical and experimental results. The thermal performance and management of the rectangular-shaped and disk-shaped heat pipe as heat sinks and heat spreaders for usage in 3D IC structures were analyzed in detail and their effectiveness were compared with the current use of copper heat sinks and copper heat spreaders. We have established that the flat-shaped heat pipes substantially reduce the temperature

distribution and the hotspot temperature. The following conclusions were corroborated in the present work:

(1). Both the rectangular-shaped and disk-shaped heat pipes substantially lower the hotspot temperatures. The rectangular-shaped heat pipe brought down the hotspot temperature by 8 ℃, the disk-shaped heat pipe can lower it by about 16 ℃. They offer this sizeable advantage while the 3D IC structure's weight at the same time becomes markedly lighter.

(2). For high-power processors, flat-shaped heat pipes play a vital role in reducing the hotspot temperature. The most prominent solution is to deploy the disk-shaped heat pipe to reduce the hotspot temperature due to the high-power consumption.

(3). The square-shaped heat pipe ($100\times100\ mm^2$) has the superior thermal performance compared with other rectangular-shaped heat pipe configurations. However, the impact of the change in the configuration from square to rectangular is not that significant.

(4). A copper heat spreader in the 3D IC structure can be replaced by the rectangular-shaped or disk-shaped heat pipe to further optimize the thermal performance. Within the scope of the current study, this replacement reduces the hotspot temperature by 13 K or 17 K, respectively.

NOMENCLATURE

c_p	Specific heat at constant pressure $[J\ (kg \cdot K)^{-1}]$	**Greek symbols**	
$f(x)$	Position of the maximum value of vapor velocity in y direction [m]	φ	Ratio of the evaporator length to the pipe length
h	Height [m]	ν	Kinematic viscosity of the vapor $[m^2$
h_b^+	Dimensionless half width of any of the vapor channels, b/h	Θ	Dimensionless temperature
h_w	Thickness of the wick [m]	ρ	Density $[kg \cdot m^{-3}]$
k	Thermal conductivity $[W\ (m \cdot K)^{-1}]$	μ	Dynamic viscosity $[(N \cdot s)m^{-2}]$
K	Permeability $[m^2]$		
k_{eff}	Effective thermal conductivity $[W\ (m \cdot K)^{-1}]$		
l	Length of the heat pipe [m]		
L_{eff}	Effective length [m]		
L_c	Characteristic length [m]		
n	Normal coordinate	**Subscripts**	
p	Pressure $[Pa]$	f	Fluid
Δp_l	Overall liquid pressure drop along the heat pipe [Pa]	m	Mean
Δp_v	Overall vapor pressure drop along the heat pipe [Pa]	e	Evaporator
Pe_h	Peclet number	c	Condenser
q	Heat flux $[W \cdot m^{-2}]$	l	Liquid phase
$\dot{q}_g$	Volumetric heat generation rate $[W \cdot m^{-3}]$	v	Vapor phase
r	coordinate	w	Wick
R	Radius of the disk-shaped heat pipe [m]	0	Initial
Re_h	Reynolds number		
T	Temperature [K]		
u	x-component of velocity $[m \cdot s^{-1}]$		
v	y-component of velocity $[m \cdot s^{-1}]$		
w	z-component of velocity $[m \cdot s^{-1}]$	**Superscripts**	
x, y, z	Cartesian coordinates	+	Dimensionless quantities

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Chapter 3

Optimization of the Thermal Performance of the 3D ICs Utilizing the Integrated Chip-size Double-layer or Multi-layer Microchannels

3.1 Abstract

The chip-size integrated double-layer microchannels (DLMC) and multi-layer microchannels (MLMC) are investigated to optimize the thermal performance of three-dimensional integrated circuits (3D ICs). The chip-size integrated DLMC without a heat spreader and a heat sink reduced the hotspot temperature by almost 15 K for a nominal 3D IC structure. Meanwhile, the size is significantly smaller than the copper heat sinks and the weight of the chip-size integrated DLMC was reduced by 99.9 %. Furthermore, two chip-size integrated DLMC lowered the hotspot temperature by another 6.77 K compared with utilizing just one integrated DLMC on top of the chip structure. The results also show that the multi-layer microchannels (MLMC) have a great effect on reducing the hotspot temperature. We have established that the optimal layout is 4 layers. The hotspot temperature is reduced by 21 K and 102 times lighter in weight compared to nominal 3D IC structure. The proposed structure and results presented in this study pave the way for major innovations in resolving the thermal issues for the 3D ICs.

3.2 Introduction

A three-dimensional integrated circuit (3D IC) is a metal-oxide semiconductor-integrated circuit manufactured by stacking silicon wafers or dies and interconnecting them vertically using through-silicon vias (TSVs), such that they behave as a single integrated device to achieve higher performance, lower power consumption, higher functional density, lower transistor packaging density, and a smaller form factor than conventional two-dimensional integrated circuits. Due to drastically increased integration density of 3D ICs, the task of removing a large amount of dispersed heat from a constrained space is beyond the capability of conventional cooling techniques. The accumulated heat within the device and the hotspot temperature are undesirable for the electrical performance since many electrical parameters are adversely affected by a substantial temperature rise [1-3]. As such effective heat removal from the 3D structure is extremely crucial.

Tavakkoli et al. [4, 5] performed a comprehensive thermal analysis of 3D high performance chips using numerical simulations. The effect of parametric changes in the geometrical configuration on the temperature distribution and hotspot temperatures were extensively highlighted, such as size, number and spacing, TSV arrangements (nominal TSVs, uniform TSVs and core-concentrated TSVs). The investigation also sufficiently outlined the impact of the thermophysical properties of the chip and cooling fluid on the flow and heat transfer. Their results presented the key features to be used for establishing optimized design and setup of 3D ICs. Wang et al. [6] performed an analysis to study the effects of geometric and thermal properties of multi-layer nominal 3D IC chips on the

temperature hotspots with different distributions of processors (overlapped cores and staggered cores). They found that the larger the number of the chip layers, the higher the hotspot temperature is; but having a large Reynolds number can help decrease the hotspot temperature. Tavakoli, Salimpour and Vafai [7] investigated the optimization of the heat spreader by inserting the boron arsenide structures, including radial, one level of paring and two-level paring structures. Their results have shown that the two-level paring boron arsenide structures in the heat spreader achieved the superior performance by reducing the hotspot temperature up to 14%. Tavakoli and Vafai [8] also established a numerical investigation of the optimal distribution of a limited amount of high thermal conductivity material to enhance the heat removal from 3D ICs. Single-layer and double-layer ring shape inserts were studied and optimized for the thermal performance. Their results show that the maximum temperature of the 3D IC is reduced up to 10% for the optimal condition and the size of the heat sink and heat spreader can be 200% smaller compared to the conventional ones. Lu and Vafai [9] had established that rectangular-shaped heat pipes (RSHP) and disk-shaped heat pipes (DSHP) heat sinks substantially improved the overall thermal performance and reduced the hotspot temperatures by 7 K and 11 K on average, respectively. Furthermore, utilizing these innovative RSHP or DSHP as the heat spreader underneath the RSHP or DSHP heat sink further optimizes the thermal performance by reducing the junction temperatures by 14 K and 16 K on average, respectively. While RSHP and DSHP possess an excellent ability to removing the generated heat, microchannels have also been implemented in the electronic cooling systems to improve the thermal performance [10].

Microchannel heat sinks which were first proposed by Tuckerman and Pease [11], have been investigated and tested as high performance and compact cooling schemes. Both the industry and research communities have investigated the use of high performance microchannels on 3D IC structures. The works from IBM *(Armonk, NY)* [12-13] illustrate the structure and fabrication process of the integrated single-layer microchannel (SLMC) for 3D ICs. The SLMCs are distributed among device layers. Cooling fluid is delivered to the 3D ICs by employing fluidic through silicon vias (TSVs) and fluidic pipes [13]. With this configuration, Mizunuma et al. [14] developed a fast and accurate thermal-wake model for integrated SLMC 3D IC structure which shows that the integrated SLMC 3D IC reduces the junction temperature significantly. Lu et al. [15] investigated a Multiphysics-based co-simulation technique for the performance of 3D IC structure with integrated SLMC cooling. The integrated SLMC effectively reduced the hotspot temperature and achieved a more uniform temperature distribution. Feng et al. [16] focused on the fast and accurate GPU-based solver development and they showed that integrated SLMC cooling is effective in improving the thermal performance of 3D ICs.

One drawback of SLMC heat sink is the relatively higher streamwise temperature rise. This undesirable temperature gradient produces thermal stresses in IC packages and undermines both the thermal performance and the electrical performance [1-3]. Double-layer or multi-layer microchannels (DLMC or MLMC) can contribute to resolve these problems. DLMC and MLMC were first introduce by Vafai and Zhu [17-19]. DLMC and MLMC are not only excellent in reducing the undesired temperature variation in the streamwise direction thus enhancing the overall cooling capacity compared to the SLMC,

but also have lower pressure drop and require less pumping power [17-20]. It should be noted that the counter-flow layout was implemented in Vafai and Zhu's works [17-19]. Following Vafai and Zhu [17-19], Xie et al. [21-24] explored straight and wavy rectangular DLMC with parallel-flow and counter-flow layouts. Their results show that the counter-flow DLMC has superior thermal performance, more uniform temperature rise and lower overall thermal resistance for various scenarios. The other limitation of the integrated SLMC on 3D ICs studied in [12-16] is the significant increased risk of water permanently damaging the 3D IC structure due to the fact that the integrated SLMCs among the device layers requires the fluidic TSVs and pipes to deliver the water into the structure.

To resolve the above problems, this work introduces the integrated chip-size DLMC and MLMC on top and bottom of the 3D IC structures to avoid the fluidic TSVs and pipes within the dies and improve the overall cooling performance. The hotspot temperature reductions and the substantial weight and size reduction of the heat sink equipment in diverse configurations of integrated DLMC and MLMC are thoroughly illustrated. In addition, optimization of the integrated DLMC and MLMC is discussed, including adding a heat sink on top of the structure, the change of the dimensions of the DLMC and investigation of nanofluids within the DLMC.

3.3 Modeling and Analysis

The schematics of the nominal 3D IC structures are shown in Figures 3.1 and 3.2. The nominal 3D IC structure is comprised of a substrate, thermal interface material (TIM)

with C4 bumps, three layers of dies, device layers and TIM with microbumps, a heat spreader and a heat sink on top. Four core processors, fabricated on each device layer, are the main heat sources. Table 3.1 displays the nominal values for different components of the 3D IC structure for nominal cases. The chip-size DLMC structure fabricated with copper [10, 15, 25-31], as illustrated in Figure 3.3 (a) and (b), is $10 \times 10\, mm^2$ and the dimensions for channel width, channel height, fin width, and base and cover thickness are presented in Table 3.2.

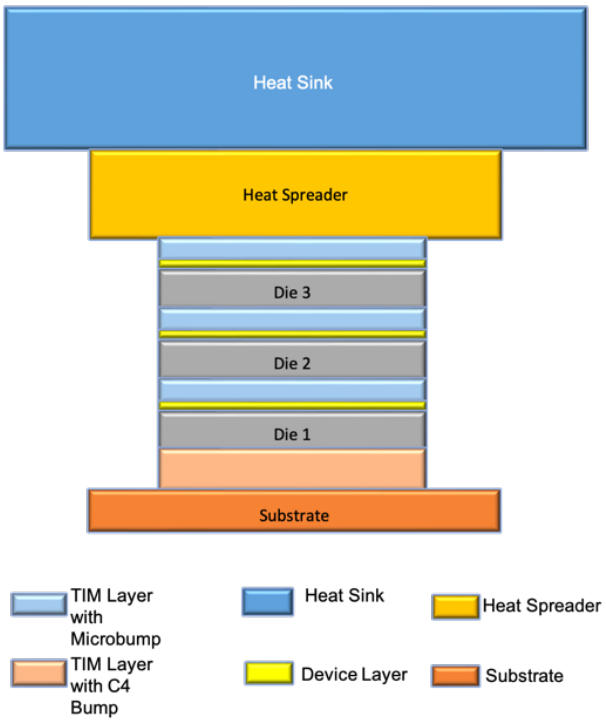


Figure 3.3.1 The schematic of the nominal 3D IC structure

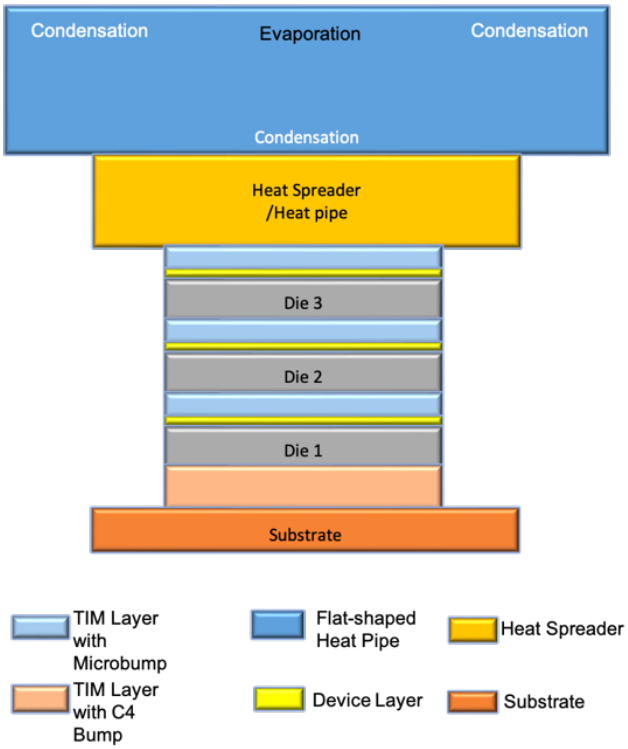
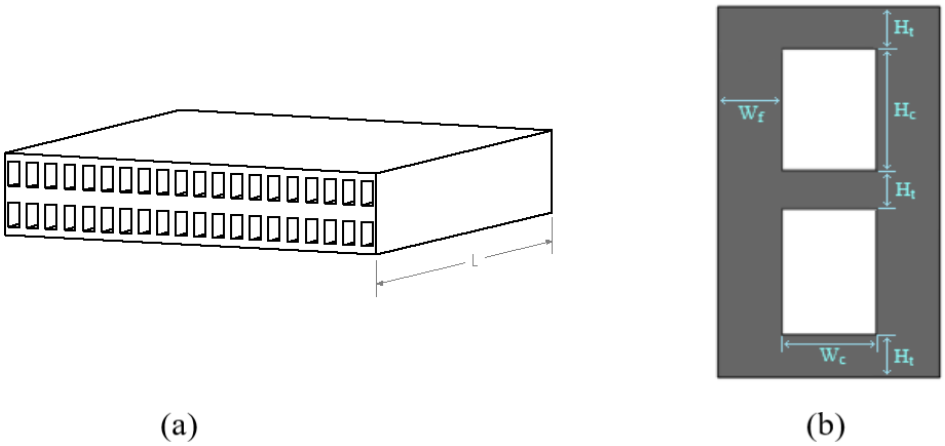


Figure 3.3.2 The schematic of 3D IC structure with heat pipe as the heat sink or heat spreader

Table 3.1 Nominal values for various parameters within the 3D IC structure [9]

Layer	Parameter	Nominal Value	Unit
Heat sink	Material	Cu	
	Length & Width	50	mm
	Thickness	4/29.4	mm
Rectangular-shaped heat pipe	Material	Cu	
	Length & Width	50	mm
	Thickness	29.4	mm
Disk-shaped heat pipe	Material	Cu	
	Radius	28	mm
	Thickness	29.4	mm
Heat spreader	Material	Cu	
	Length & Width	30	mm
	Thickness	3	mm
Chip	Length & Width	10	mm
	Number of layers	3	mm
TIM layer with microbump	TIM material	Thermal grease	
	Thermal conductivity	5	$W/m \cdot K$
	Thickness	15	µm
TIM layer with C4 bump	TIM material	Thermal grease	
	Thermal conductivity	5	$W/m \cdot K$
	Thickness	100	µm
Die	Material	Si	
	Thickness	100	µm
Device layer	Material	Si	
	Thickness	2	µm
Core processor	Material	Si	
	Total power within the 3D IC	90	W
	Cores per layer	4	
	Length & Width	2	mm
	Thickness	2	µm
Substrate	Material	Si	
	Length & Width	30	mm
	Thickness	1	mm



(a) (b)

Figure 3.3.3 (a) Schematic of the chip-size integrated DLMC structure; (b) the magnified view of one set of channels

Table 3.2 Nominal Values within DLMC structure test

Structure	Channel Length L (mm)	Channel Width W_c (μm)	Channel Height H_c (μm)	Channel fin width W_f (μm)	Channel base/cover thickness H_t (μm)	Number of Channels N
	10	290	400	200	50	20×2
References	[13, 15, 16, 21, 24-28]					

The heat source is uniformly distributed [9] in each layer (30 W each layer and 7.5 W each processor). The heat is conducted through the layers down to the substrate and up to the spreader and the heat sink, and eventually to the ambient air through forced convective heat transfer above the heat sink and natural convective heat transfer under the substrate.

Conductive heat transfer through the solid, and isotropic layers of the 3D IC is governed by

$$\frac{\partial^2 \Theta_s^+}{\partial x^{+2}} + \frac{\partial^2 \Theta_s^+}{\partial y^{+2}} + \frac{\partial^2 \Theta_s^+}{\partial z^{+2}} + q_g^+ = 0 \tag{3.1}$$

Where q_g^+ denotes the dimensionless volumetric heat generation in the central processing units and the nondimensionalized temperature and spatial coordinates are set up as:

$$x^+ = \frac{x}{h}, \qquad y^+ = \frac{y}{h}, \qquad z^+ = \frac{z}{h}, \qquad \Theta^+ = \frac{T - T_e}{qh/k_f}$$

The convective boundary conditions are

$$\frac{\partial \Theta_s^+}{\partial n^*} = -Bi \cdot \Theta_s^+ \tag{3.2}$$

Where n^* is the normal coordinate and Bi is the dimensionless Biot number.

Nominally, the heat flow occurs mainly normal to the device layers. The heat transfer and fluid flow for the DLMC needs to be accounted for. It is governed by the Navier-Stokes equation. The water as the coolant within the microchannel is pumped into the channel at 1m/s [13]. The dimensionless Navier-Stokes equations in Cartesian coordinates are:

Mass conservation:

$$\frac{\partial u^+}{\partial x^+} + \frac{\partial v^+}{\partial y^+} + \frac{\partial w^+}{\partial z^+} = 0 \tag{3.3}$$

x-Momentum equation:

$$Re_h\left(u^+\frac{\partial u^+}{\partial x^+}+v^+\frac{\partial u^+}{\partial y^+}+w^+\frac{\partial u^+}{\partial z^+}\right)=-\frac{\partial p^+}{\partial x^+}+\left(\frac{\partial^2 u^+}{\partial x^{+2}}+\frac{\partial^2 u^+}{\partial y^{+2}}+\frac{\partial^2 u^+}{\partial z^{+2}}\right) \quad (3.4)$$

y-Momentum equation:

$$Re_h\left(u^+\frac{\partial v^+}{\partial x^+}+v^+\frac{\partial v^+}{\partial y^+}+w^+\frac{\partial v^+}{\partial z^+}\right)=-\frac{\partial p^+}{\partial y^+}+\left(\frac{\partial^2 v^+}{\partial x^{+2}}+\frac{\partial^2 v^+}{\partial y^{+2}}+\frac{\partial^2 v^+}{\partial z^{+2}}\right) \quad (3.5)$$

z-Momentum equation:

$$Re_h\left(u^+\frac{\partial w^+}{\partial x^+}+v^+\frac{\partial w^+}{\partial y^+}+w^+\frac{\partial w^+}{\partial z^+}\right)=-\frac{\partial p^+}{\partial z^+}+\left(\frac{\partial^2 w^+}{\partial x^{+2}}+\frac{\partial^2 w^+}{\partial y^{+2}}+\frac{\partial^2 w^+}{\partial z^{+2}}\right) \quad (3.6)$$

Energy conservation for the fluid domain:

$$Pe_h\left(u^+\frac{\partial \Theta_f^+}{\partial x^+}+v^+\frac{\partial \Theta_f^+}{\partial y^+}+w^+\frac{\partial \Theta_f^+}{\partial z^+}\right)=\frac{\partial^2 \Theta_f^+}{\partial x^{+2}}+\frac{\partial^2 \Theta_f^+}{\partial y^{+2}}+\frac{\partial^2 \Theta_f^+}{\partial z^{+2}} \quad (3.7)$$

The nondimensionalized terms in the above equations are:

$$u^+=\frac{u}{u_m},\qquad v^+=\frac{v}{v_m},\qquad w^+=\frac{w}{w_m},\qquad p^+=\frac{ph}{\mu_f u_m},$$

$$Re_h=\frac{\rho_f u_m h}{\mu_f},\qquad Pe_h=\frac{\rho_f\, c_{p,f} u_m h}{k_f}$$

This work also investigates Al_2O_3 nanofluids within the DLMC to further optimize the thermal performance with higher thermal conductivity. The thermal conductivity,

dynamic viscosity, density and specific heat of Al_2O_3 nanofluids are calculated as follows [32-35]:

$$k_{nf} = \left[\frac{k_p + (n-1)k_{bf} - (n-1)\varphi(k_{bf} - k_P)}{k_p + (n-1)k_{bf} + \varphi(k_{bf} - k_P)}\right] k_{bf} \tag{3.8}$$

$$\mu_{nf} = (1 + 2.5\,\varphi)\mu_{bf} \tag{3.9}$$

$$\rho_{nf} = (1 - \varphi)\rho_{bf} + \varphi\rho_P \tag{3.10}$$

$$c_{p,nf} = (1 - \varphi)c_{p,bf} + \varphi c_{p,P} \tag{3.11}$$

Where k_{nf}, k_{bf} and k_P are the thermal conductivities of Al_2O_3 the nanofluid, base fluid and solid particles, respectively. φ is the volumetric concentration of nanoparticles and n is solid particle shape factor (n = 3 with the assumption of spherical particles). μ_{nf} and μ_{bf} are the viscosities of the nanofluid and base fluid, respectively; ρ_{nf}, ρ_{bf} and ρ_P are the densities of nanofluid, base fluid and solid particles, respectively; $c_{p,nf}$, $c_{p,bf}$ and $c_{p,P}$ are the specific heat of the nanofluid, base fluid and solid particles, respectively. The calculated results for the above-mentioned properties are listed in Table 3.3.

Table 3.3 Al_2O_3 nanofluid properties

	$\varphi = 0\%$	$\varphi = 2\%$	$\varphi = 5\%$
k_{nf} (W/m· K)	0.603	0.638	0.693
ρ_{nf} (kg/m^3)	995.7	1047.7	1125.9
μ_{nf}($kg/m \cdot s$)	7.977×10^{-4}	8.376×10^{-4}	8.974×10^{-4}
$c_{p,nf}$ ($kJ/kg \cdot K$)	4.183	4.115	4.012

3.4 Model Validation

The simulation and modeling of the thermal performance is carried out through COMSOL Multiphysics. The grid independence study was performed for all investigated structures (Figure 3.4 – Figure 3.9) and the junction temperature for each structure was evaluated using computational meshes for different cell distributions. The grid independence study for various cases applying physics-based coarse, fine, finer, normal and extra fine mesh distributions is shown in Figure 3.10. The overall temperature varies within 1 K. In order to reduce the computational time and gain accurate simulation results, the normal mesh distribution is sufficient to obtain accurate results and is employed in this work.

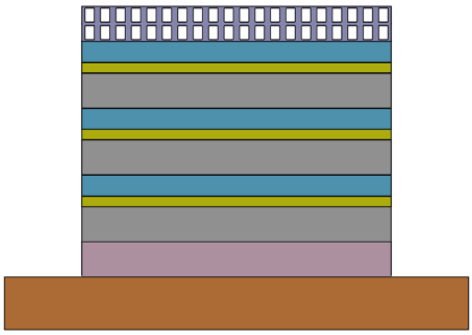


Figure 3.3.4 The schematic of chip-size integrated DLMC on top of the 3D IC structure

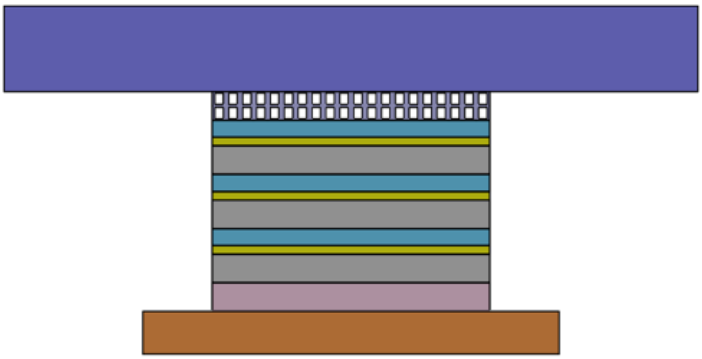


Figure 3.3.5 The schematic of chip-size integrated DLMC on top of the 3D IC structure with heat sink above

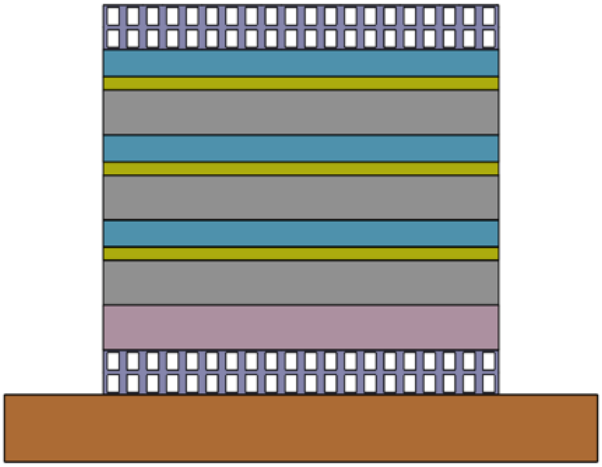


Figure 3.3.6 The schematic of two chip-size integrated DLMC on top and at the bottom of the 3D IC structure

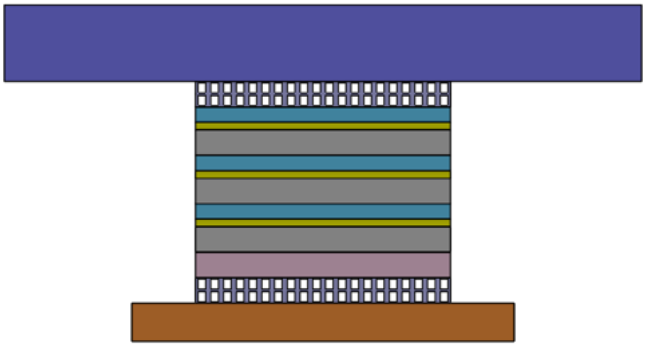


Figure 3.3.7 The schematic of two chip-size integrated DLMC on top and at the bottom of the 3D IC structure with heat sink above

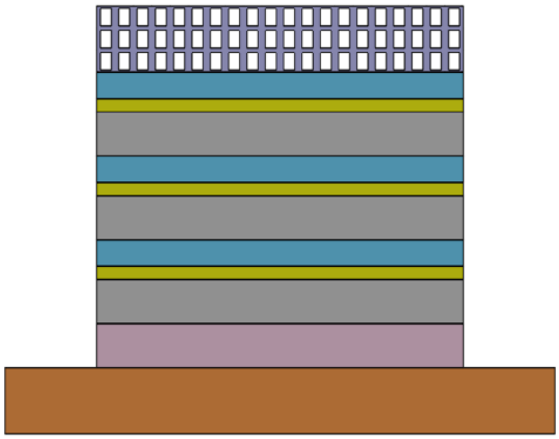


Figure 3.3.8 The schematic of chip-size integrated three-layer microchannel on top of the 3D IC structure

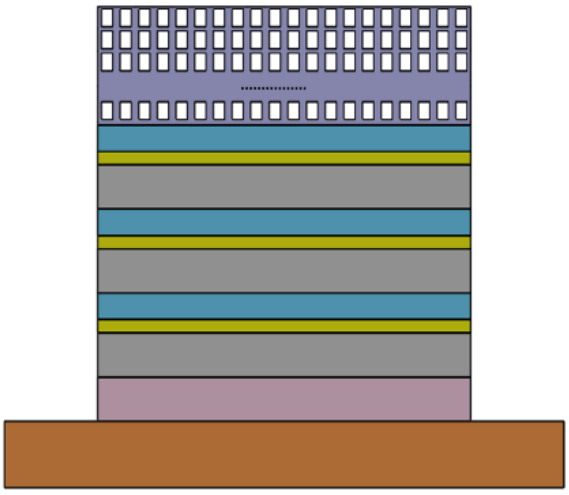


Figure 3.3.9 The schematic of chip-size integrated MLMC on top of the 3D IC structure.

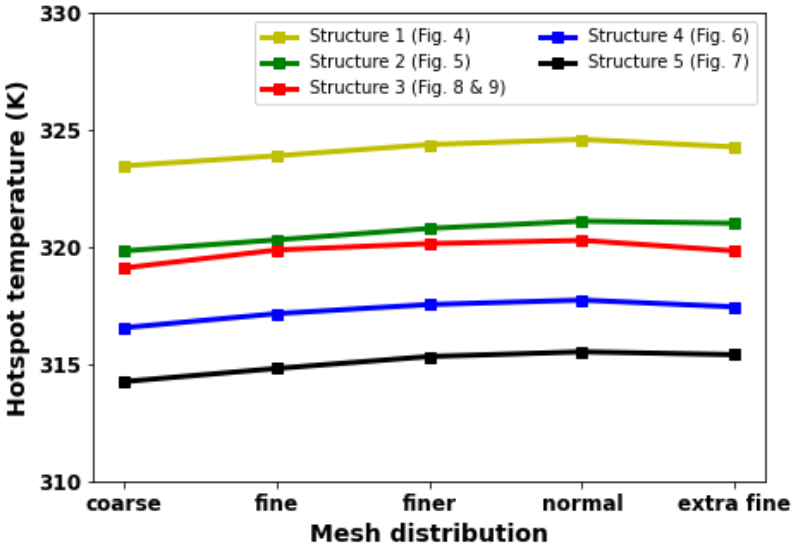


Figure 3.3.10 Grid independence study for the investigated structures

In addition, the main feature of the 3D IC structure model was validated earlier [9] both experimentally and numerically. The DLMC model was compared with the work of Xie et al. [21] in Figure 2.11. Figure 2.11 illustrates an excellent agreement for the temperature distribution for a DLMC for both parallel-flow and counterflow structure between the present work and reference [21].

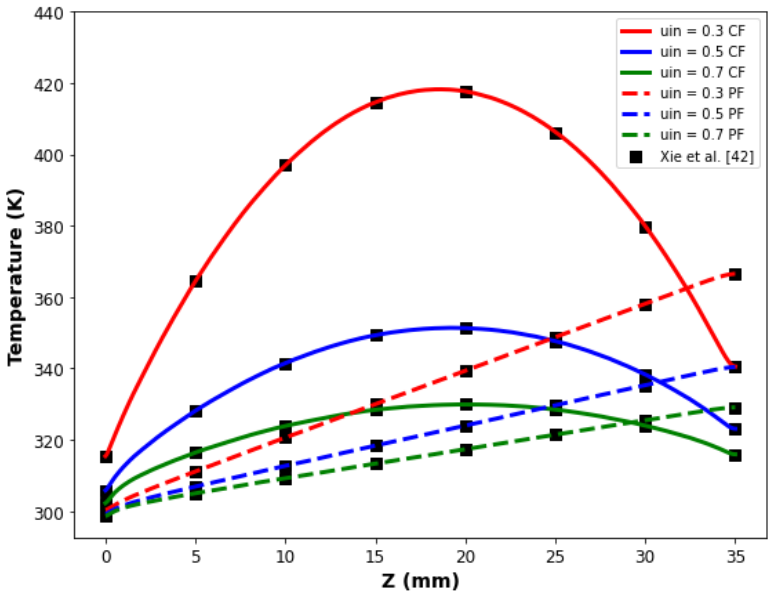


Figure 3.3.11 The temperature distribution of the bottom surface of a DLMC with both counter-flow and parallel-flow layout – comparison with Xie et al. [21]

2.5 Results and Discussions

Table 3.4 displays the thermal performance and weight comparison among nominal copper heat sink (Figure 3.1), RSHP and DSHP (Figure 3.2) and integrated chip-size DLMC (Figure 3.4). It should be noted that the height for the nominal copper heat sink in this scenario is 29.4 mm in order to be consistent with the height of RSHP and DSHP. Compared with the nominal 3D IC structure with copper heat sink and heat spreader (Figure 3.1), RSHP as the heat sink reduced the hotspot temperature by 6K and DSHP reduced the hotspot temperature by 16K while reducing the weight by 7.35 times. As it can be seen from Table 3.4, the chip-size integrated DLMC without a heat spreader and a heat sink, as illustrated in Figure 3.4, reduced the hotspot temperature by almost 15 K.

Meanwhile, the weight of the chip-size integrated DLMC is 1288 times lighter and the size is significantly smaller than the copper heat sink.

Table 3.4 Comparison of the Thermal Performance among different heat sinks

	Copper heat sink/ Reference (Figure 2.1)	RSHP as the heat sink (Figure 2.2)	DSHP as the heat sink (Figure 2.2)	Integrated DLMC without a heat spreader and heat sink (Figure 2.4)
Hotspot Temperature (K)	339.2	333.7	323.3	324.5
Reduction on Hotspot Temperature (K)	0	5.5	15.9	14.7
Weight Reduction	0	7.35 times lighter	7.35 times lighter	1288 times lighter

As shown in Table 3.5, the heat sink with a nominal height of 4 mm on top of the chip-size integrated DLMC (Figure 3.5) can further optimize the thermal performance of the 3D IC structure. Next, we have employed the effect of combining a heat sink (copper heat sink, RSHP and DSHP as illustrated in Figures 3.1 and 3.2) and a chip-size integrated DLMC on the hotspot temperature. Integrated DLMC with a copper heat sink, RSHP and DSHP reduced the hotpot temperature by 18 K, 14 K and 3 K respectively compared with the combination of a heat sink and a heat spreader. It should be noted that the weight of the integrated DLMC is 51 times lighter in weight and 9 times smaller in volume than the heat spreader employed in Figures 3.1 and 3.2.

Table 3.5 The Combination of heat sinks with Integrated DLMC

	Copper heat sink with copper heat spreader (Fig. 1)	Integrated DLMC with a copper heat sink (Fig. 5)	Integrated DLMC with a RSHP heat sink (Fig. 5)	Integrated DLMC with a DSHP heat sink (Fig. 5)
Hotspot Temperature (K)	339.2	321	320	320
Reduction on Hotspot Temperature (K)	Reference	18.2	19.2	19.2
Weight Reduction	Integrated DLMC is 51 times lighter than the copper heat spreader and 9 times smaller in volume			

Finally, we analyzed the effect of two chip-size integrated DLMC on top and at the bottom of the 3D IC structure, as displayed in Figures 3.6 and 3.7, on the hotspot temperauter. The results shown in Figures 3.12 clarify the substantial effect of this structure. Two chip-size integrated DLMC lowered the hotspot temperature by another 6.77 K in comparison with employing just one integrated DLMC for 3D IC regardless of having a heat sink on top or not. But having a heat sink on top can definitely improve the thermal performance even further and the setup can still remain lighter weight compared with the nominal strucutres (Figures 3.1 and 3.2).

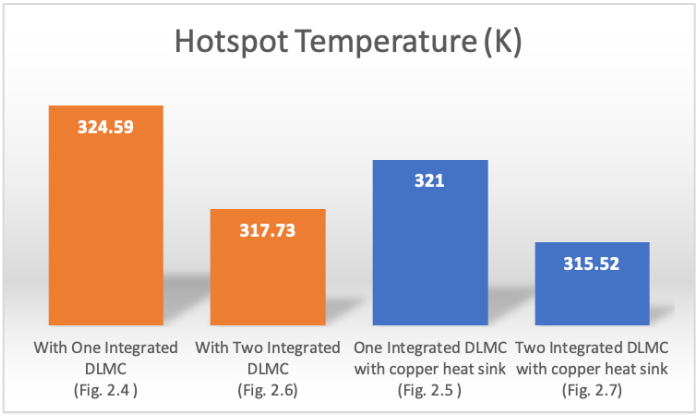


Figure 3.3.12 The effect of two integrated DLMC on the hotspot temperature of the 3D IC.

The effect of multi-layer microchannels on the hotspot temperature of the 3D IC structure (Figures 3.8 and 3.9) is illustrated in Table 3.6. As it can be seen the optimal layout is 4 layers. The hotspot temperature is reduced by 21 K and the setup is 102 times lighter in weight compared to the nominal 3D IC structure with a nominal height of 7 mm (Figure 3.1). Meanwhile, the total height of the integrated 4-layer microchannel is only 1.9 mm while the nominal 3D IC (Figure 3.1) is 7 mm. After 4 layers, the decrease in the hotspot temperature is not significant while the weight and size increase significantly.

Table 3.6 Multilayer micorchannel hotspot temperatures

	Hotspot Temperature (K)	Total height (mm)	Weight Reduction
Coper heat sink with a heat spreader (Figure 2.1)	339.2	7	0
2 layers (Figure 2.4)	324.5	1	228 times lighter
3 layers (Figure 2.8)	320.28	1.45	133 times lighter
4 layers (Figure 2.9)	317.85	1.9	102 times lighter
5 layers (Figure 2.9)	316.91	2.35	84 times lighter
6 layers (Figure 2.9)	316.27	2.8	71 times lighter

To further optimize the thermal performance of the 3D IC structure, more narrower channels were utilized with the same chip-size integrated DLMC. Figure 3.13 shows that when the number of channels increased from N = 40 to N = 50, the hotspot temperature is lowered by 2 K. The effect is not significant. The effect of nanofluids (Al_2O_3) within the integrated DLMC on the hotspot temperature of the 3D ICs was also explored. Three cases were selected to show the impact of the nanofluids. Case 1 is the integrated DLMC with 40 channels and cases 2 is for 50 channels. Case 3 was based on the two integrated DLMC with a copper heat sink above while increasing the volume fraction of the nanofluids. Figure 3.13 shows that the influence of nanofluids also is insignificant. The hotspot temperature was reduced by 1 K when the volume fraction was increased from 2% to 5% for all three cases.

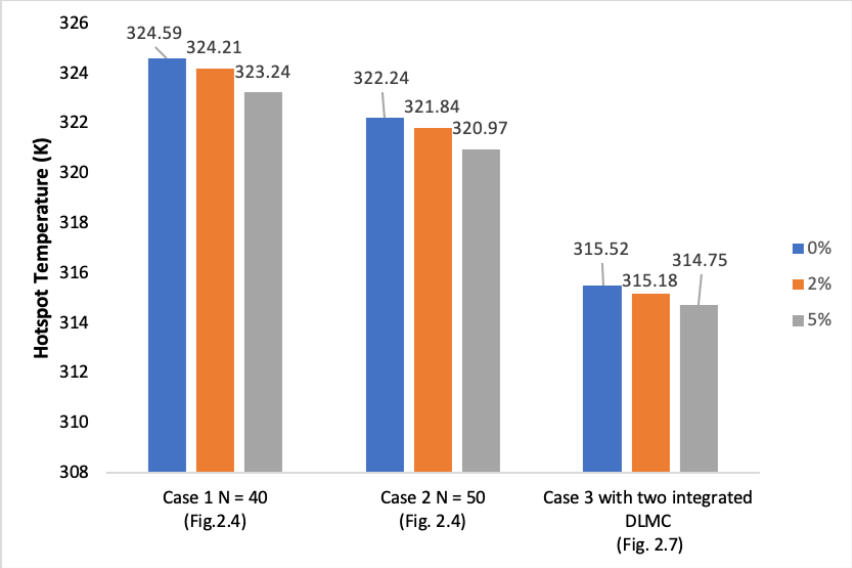


Figure 3.3.13 The effect of the nanofluids within the integrated DLMC on the hotspot temperature

3.6 Summary and Conclusions

A thorough analysis and optimization of the thermal performance of the 3D ICs utilizing the chip-size integrated DLMC and MLMC is presented in this work. The results demonstrate that the integrated DLMC and MLMC not only substantially contribute to improve the thermal performance of the 3D ICs and reduce the hotspot temperature but also greatly reduce the overall packaging size and weight, which is in high demand for the electronic devices in the industry. The main contributions for an integrated DLMC and MLMC are as follows:

(1). The chip-size integrated DLMC without a heat spreader and a heat sink reduce the hotspot temperature by almost 15 K compared with the nominal structure. Meanwhile, the weight of the chip-size integrated DLMC is 1288 times lighter and

the size is significantly smaller than the combination of copper heat sinks and heat spreaders.

(2). Two chip-size integrated DLMC on top and bottom of the chip lowered the hotspot temperature by another 6.77 K in comparison of only one integrated DLMC on top of the IC structure. The total temperature reduction in this case was 21 K and the weight was reduced by 99%.

(3). The MLMC has a pronounced effect on reducing the hotspot temperature. The optimal layout was demonstrated to be 4 layers. The hotspot temperature was reduced by 21 K and the structure was 102 times lighter in weight compared to the nominal 3D IC structure.

(4). Integrating a heat sink on top of the DLMC or MLMC without a heat spreader further reduced the hotspot temperature by another 4 K for a total hot spot temperature reduction up to 25 K. Compared to the heat spreader in the nominal structure, a chip-size DLMC is 51 times lighter in weight and 9 times smaller in volume.

(5) The effect of utilizing nanofluids for the 3D IC structure was also investigated and the results were presented. It was shown that the nanofuids did not create a significant reduction within the analyzed proposed innovative 3D IC structure.

NOMENCLATURE

L	Channel length [mm]	**Greek symbols**	
W_c	Channel width [µm]	φ	Volumetric concentration of nanoparticles
H_c	Channel height [µm]	Θ	Dimensionless temperature
W_f	Channel fin width [µm]	ρ	Density $[kg \cdot m^{-3}]$
h_t	Channel cover and base thickness [µm]	µ	Dynamic viscosity $[(N \cdot s)m^{-2}]$
N	Number of channels		
k	Thermal conductivity $[W\ (m \cdot K)^{-1}]$		
n^*	Normal coordinate		
Bi	Biot number		
p	Pressure $[Pa]$		
u	x-component of velocity $[m \cdot s^{-1}]$		
v	y-component of velocity $[m \cdot s^{-1}]$	**Subscripts**	
w	z-component of velocity $[m \cdot s^{-1}]$	f	Fluid
x, y, z	Cartesian coordinates	s	Solid
Re_h	Reynolds number	m	Mean
c_p	Specific heat at constant pressure $[J\ (kg \cdot K)^{-1}]$	nf	nanofluid
Pe_h	Peclet number	bf	Base fluid
q	Heat flux $[W \cdot m^{-2}]$	P	nanoparticle
q_g	Volumetric heat generation rate $[W \cdot m^{-3}]$		
T	Temperature [K]	**Superscripts**	
n	Solid particle shape factor	+	Dimensionless quantities

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Chapter 4

Additional Work

4.1 The effect of a heat sink on the 3D IC structures.

Figure 4.1 presents the effect of a heat sink on the thermal performance of the 3D IC structure. As it can be seen, a heat sink is indispensably necessary for a 3D IC structure. For a 3D IC without a heat sink, the hotspot temperature can reach up to 405 K, which is not acceptable for all the CPUs in the industry, whose operating temperature is 373K. However, a heat sink on top of the 3D IC structure reduced the hotspot temperature to as low as 340 K. Hence, improving the thermal performance of a heat sink can significantly contribute to optimize the thermal performance of a 3D IC.

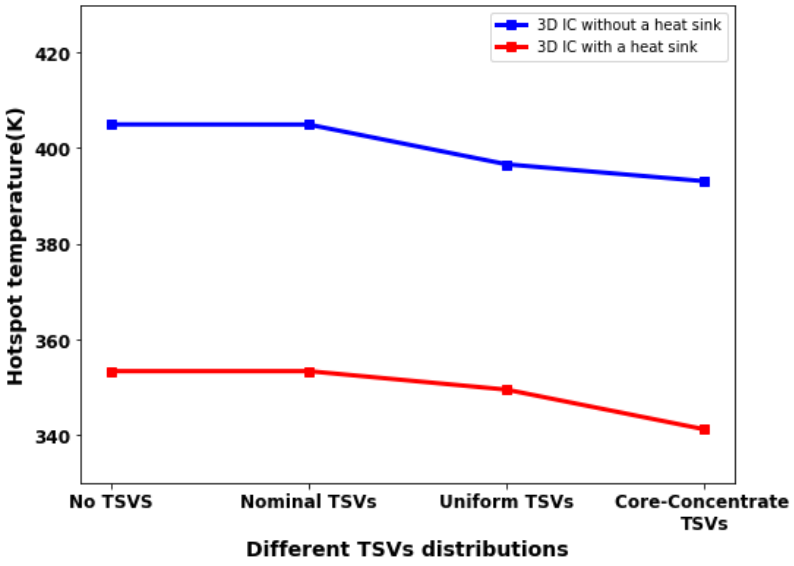

Figure 4.1 The effect of a heat sink on the thermal performance of a 3D IC structure.

4.2 Additional investigations on the RSHPs and DSHPs as the heat spreader

The additional work is done on the analysis of the effect of RSHP and DSHP heat spreader dimensions on the 3D IC hotspot temperatures. The hotspot temperatures for both $30\times30\times$ 3 mm^3(R = 28 mm for DSHP heat spreader) and $50\times50\times$ 3 mm^3(R = 56 mm for DSHP heat spreader) are presented in Figure 4.2. It should be noted that the heat sinks are RSHP and DSHP in this investigation. Figure 4.2 shows that the effect of the enlarged RSHP and DSHP heat spreaders are not significant.

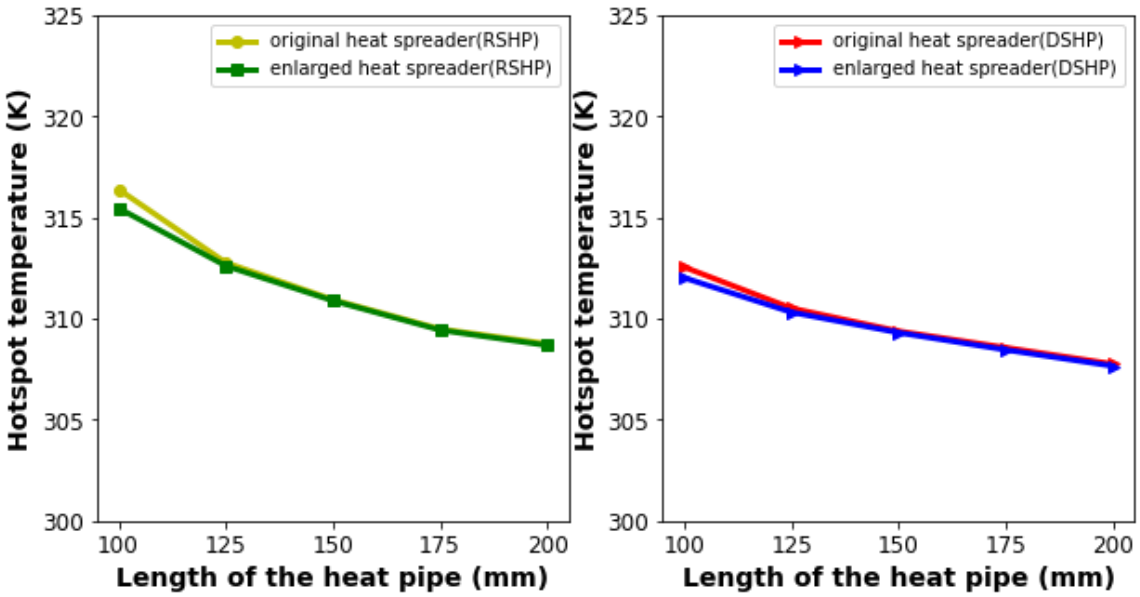

Figure 4.2 The effect of the enlarged RSHP and DSHP heat spreader on the hotspot temperature of a 3D ICs

The impacts of the combination of DSHP heat spreader with RSHP heat sink and the combination of RSHP heat spreader with DSHP heat sink are studied, as illustrated in Figure 4.3. As seen from Figure 4.3, the combinations are not reducing the hotspot temperatures to improve the thermal performance of the 3D ICs. Hence, this dissertation investigated the original configurations, which are RSHP heat spreaders with the RSHP heat sinks and DSHP heat spreaders with the DSHP heat sinks.

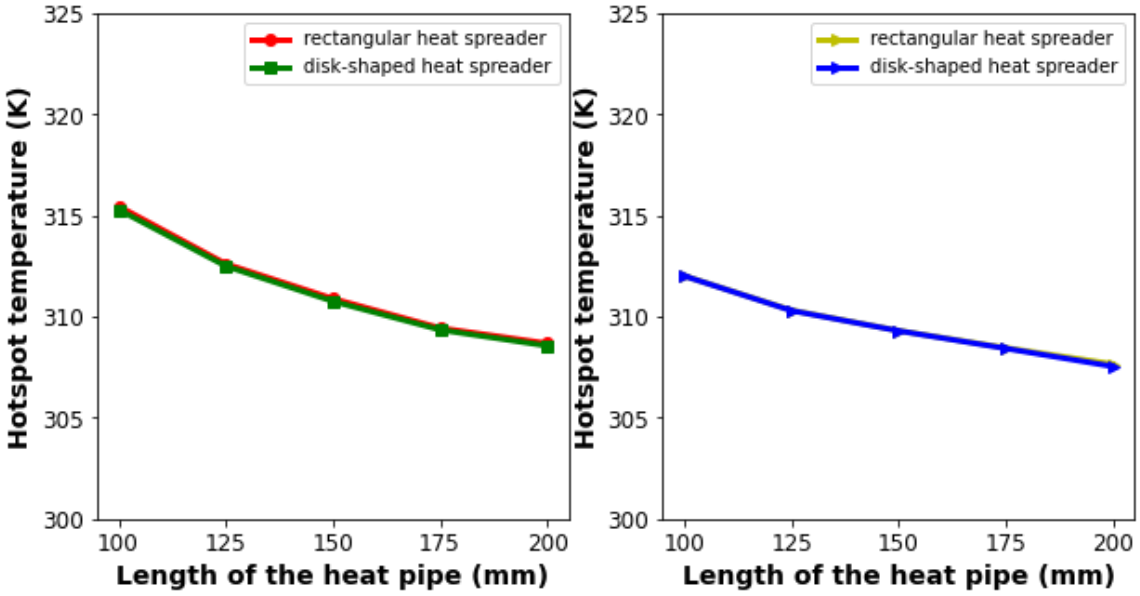

Figure 4.3 The effect of the combination of DSHP heat spreader or RSHP heat spreader with RSHP heat sink or DSHP heat sink, respectively. (Left: RSHP heat sink; Right: DSHP heat sink)

The height of RSHPs and DSHPs investigated in this dissertation is 29.4 mm. In order to make the comparison, the height of the copper heat sink is also 29.4 mm instead of the 4 mm. However, additional work of comparison with the effect of copper heat sink with the height of 4 mm is also investigated. It should be noted that the total height of

RSHP is 29.4 mm but the actual copper solid part is only 4 mm, which is the same height with the copper heat sink. Figure 4.4 shows that the flat-shaped heat pipe is superior to the nominal copper heat sink at all length and reduced the hotspot temperature by up to 17 K.

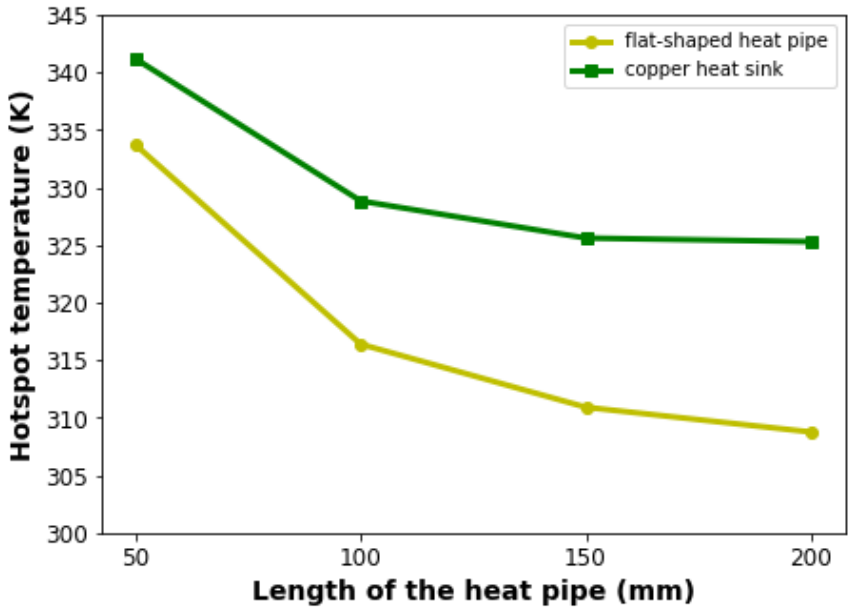

Figure 4.4 The hotspot temperature of the 3D IC with copper heat sink (h = 4mm) and the flat-shaped heat pipe.

With the 4 mm height of copper heat sink, the hotspot temperature of the 3D IC with copper heat sink and RSHP with different heat dissipation is discussed. The result in Figure 4.5 indicates the RSHP possess high heat removal capability with the reduction of the hotspot temperature up to 70 K at 500 W compared with the copper heat sink.

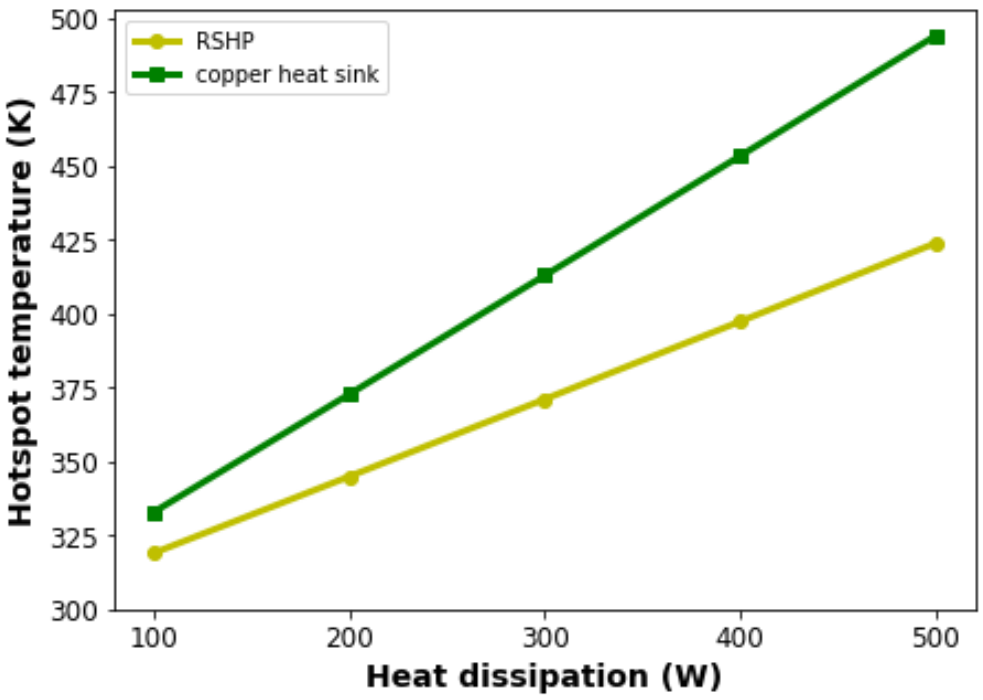

Figure 4.5 The hotspot temperature of the 3D IC with copper heat sink (h = 4mm) and RSHP.

4.3 Additional work on the integrated chip-size DLMCs and MLMCs

The three-dimensional schematics of integrated chip-size DLMC or MLMC on the 3D IC structure are created.

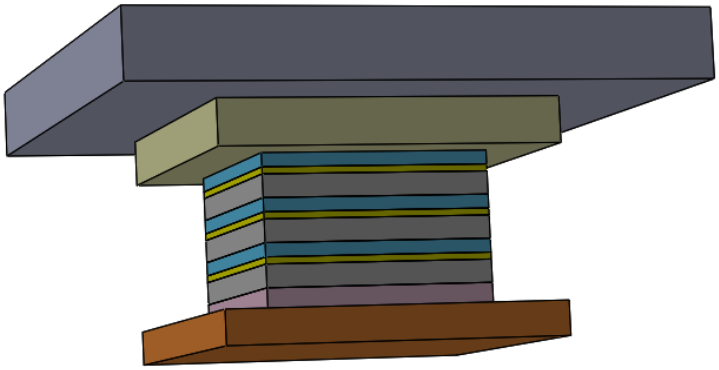

Figure 4.6 The 3D schematic of the nominal 3D IC structure.

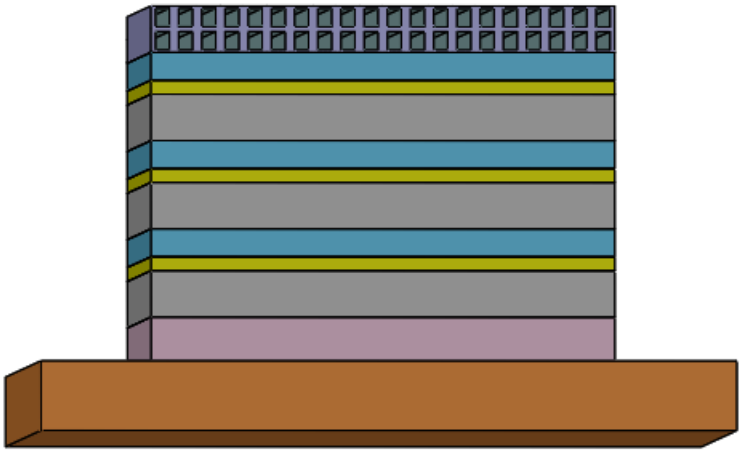

Figure 4.7 The 3D schematic of the integrated DLMC on a 3D IC structure.

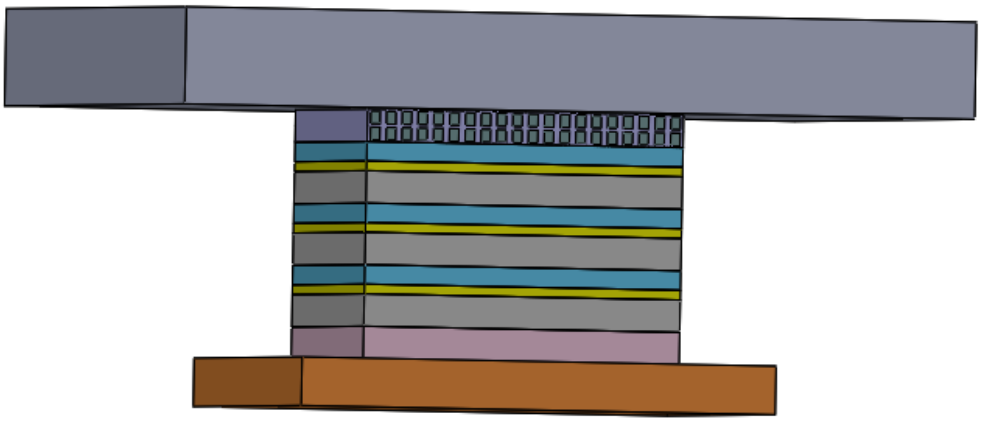

Figure 4.8 The 3D schematic of the integrated DLMC and a heat sink on top of a 3D IC structure.

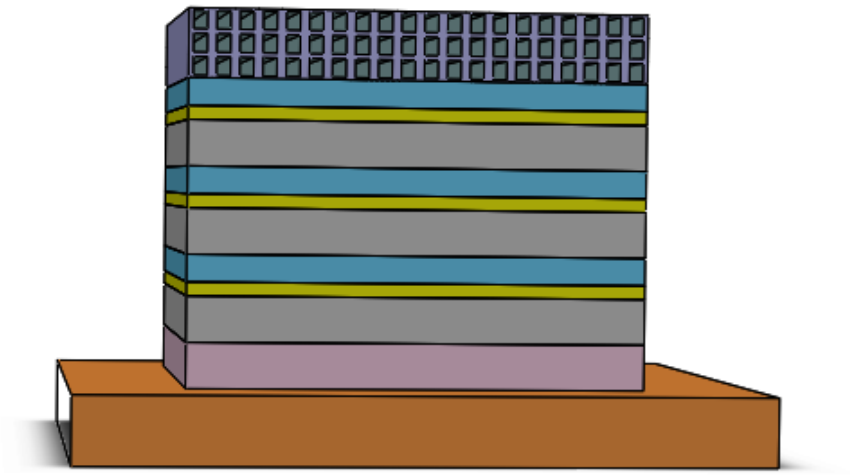

Figure 4.9 The 3D schematic of the integrated three-layer microchannel on a 3D IC structure.

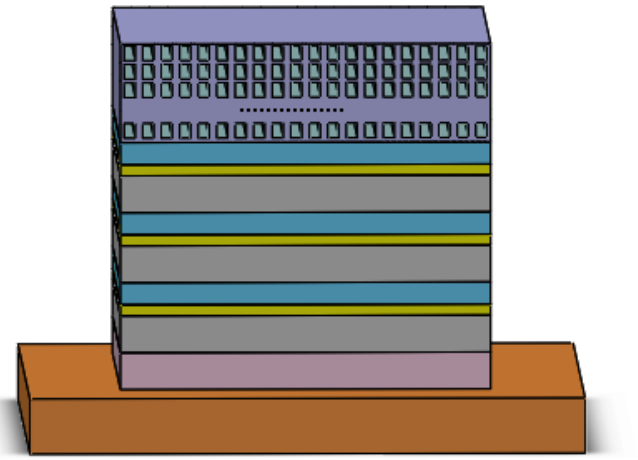

Figure 4.10 The 3D schematic of the integrated MLMC on a 3D IC structure.

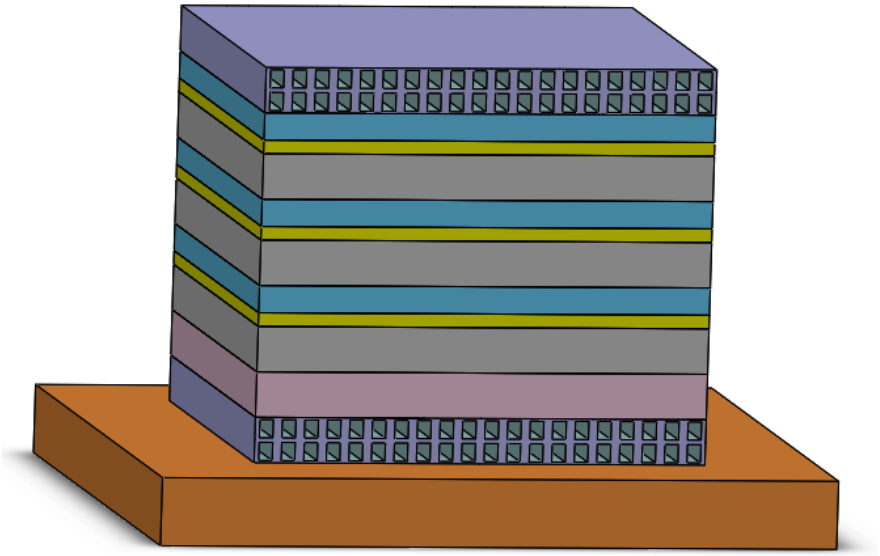

Figure 4.11 The 3D schematic of two integrated DLMCs on a 3D IC structure.

Chapter 5

Conclusions and Future Work

This chapter presents a summary of the crucial findings. Recommendations regarding the continuations of research work in this topic are discussed.

5.1 Conclusions

Three-dimensional integrated circuit (3D IC) is a promising solution for modern technology as 2D integrated circuits and embedded system are not able to meet the increasing need for smaller, thinner but more powerful electronic systems. 3D ICs have the advantages of superior performance, higher bandwidth, shorter interconnect, higher package density, condensed footprint but reduced power consumption and accommodating homogeneous and heterogeneous packaging. However, the bottleneck of heat built up within 3D ICs is still a challenge in the industries. This work provided innovative and efficient cooling techniques to optimize the thermal performance of the 3D IC structures by utilizing the rectangular-shaped and disk-shaped heat pipes as well as the integrated chip-size double-layer and multi-layer microchannels. The key findings and conclusions are as follows:

(1). Both the rectangular-shaped and disk-shaped heat pipes substantially lower the hotspot temperatures. The rectangular-shaped heat pipe brought down the hotspot temperature by 8 ℃, the disk-shaped heat pipe can lower it by about 16 ℃. They offer this sizeable advantage while the 3D IC structure's weight at the same time becomes markedly lighter.

(2). For high-power processors, flat-shaped heat pipes play a vital role in reducing the hotspot temperature. The most prominent solution is to deploy the disk-shaped heat pipe to reduce the hotspot temperature due to the high-power consumption.

(3). The square-shaped heat pipe ($100\times100\ mm^2$) has the superior thermal performance compared with other rectangular-shaped heat pipe configurations. However, the impact of the change in the configuration from square to rectangular is not that significant.

(4). A copper heat spreader in the 3D IC structure can be replaced by the rectangular-shaped or disk-shaped heat pipe to further optimize the thermal performance. Within the scope of the current study, this replacement reduces the hotspot temperature by 13 K or 17 K, respectively.

(5). The chip-size integrated DLMC without a heat spreader and a heat sink reduce the hotspot temperature by almost 15 K compared with the nominal structure. Meanwhile, the weight of the chip-size integrated DLMC is 1288 times lighter and the size is significantly smaller than the combination of copper heat sinks and heat spreaders.

(6). Two chip-size integrated DLMC on top and bottom of the chip lowered the hotspot temperature by another 6.77 K in comparison of only one integrated DLMC on top

of the IC structure. The total temperature reduction in this case was 21 K and the weight was reduced by 99%.

(7). The MLMC has a pronounced effect on reducing the hotspot temperature. The optimal layout was demonstrated to be 4 layers. The hotspot temperature was reduced by 21 K and the structure was 102 times lighter in weight compared to the nominal 3D IC structure.

(8). Integrating a heat sink on top of the DLMC or MLMC without a heat spreader further reduced the hotspot temperature by another 4 K for a total hot spot temperature reduction up to 25 K. Compared to the heat spreader in the nominal structure, a chip-size DLMC is 51 times lighter in weight and 9 times smaller in volume.

(9). The effect of utilizing nanofluids for the 3D IC structure was also investigated and the results were presented. It was shown that the nanofluids did not create a significant reduction within the analyzed proposed innovative 3D IC structure.

5.2 Future Work

(1). Boiling is the rapid vaporization of a liquid, which occurs when a liquid is heated to boiling point. There is nucleate boiling, critical heat flux, transition boiling and film boiling. The opportunity for future work is to investigate the boiling technique for cooling by making use of the critical heat flux characteristic. Before film boiling occurs, the liquid is capable of absorbing heat from the surroundings without the requirement of

large temperature difference. This can be applied to the heat sink equipment to improve the thermal performance of 3D IC structure.

(2). Thermal-structural analysis of the 3D IC structures is another opportunity for future work. High operating temperatures and hotspot temperatures in 3D IC structures cause thermal stress on the structures, which gives rise to the thermal expansions among different materials, and may affect the performance of the entire structure due to the failure of the mechanism.

(3). This dissertation employed the thermal grease as thermal interface material and hasn't put work on the effect of different thermal interface materials on the performance of 3D ICs. There is thermal paste, thermal adhesive, thermal gap filler, thermally conductive pad, thermal tape, phase-change materials, and metal thermal interface materials. It is worthwhile to put effort for the future work on the analysis of the effects of different thermal interface materials on the thermal performance and overall performance of 3D IC structures.

(4). 3D IC structures may be explored in the future work. 3D IC structures is flexible to have various configurations and the innovative cooling techniques in this project can be investigated on these configurations.