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A Low-Power 28-GHz Beamforming Receiver with On-Chip Frequency Synthesizer

A dissertation submitted in partial satisfaction
of the requirements for the degree
Doctor of Philosophy in Electrical and Computer Engineering

by

Pawan Kumar Khanna

2023

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2023

ABSTRACT OF THE DISSERTATION

A Low-Power 28-GHz Beamforming Receiver with On-Chip Frequency Synthesizer

by

Pawan Kumar Khanna
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2023
Professor Behzad Razavi, Chair

The 5G New-Radio standard includes bands in the millimeter-wave spectrum that provide channel bandwidth of up to 400 MHz. When compared to the maximum bandwidth of lower frequency (sub-7-GHz) bands of the same standard, millimeter-wave bands can provide four times the bandwidth, yielding faster data rates. Within the millimeter-wave spectrum, many transceiver implementations targeting the 26.5 GHz - 29.5 GHz band have been reported recently. The use of millimeter-wave communications in 5G radios becomes viable if (1) extensive beamforming is employed to overcome the high path loss and (2) the power consumption is sufficiently low to afford frequent high-throughput connections for mobile devices.

Recent beamforming receivers in the vicinity of 28 GHz draw, per element, 27.5 mW to 50 mW. A key observation in the design of beamforming receivers (RXs) is that the phase shift network typically consumes high power whether it appears in the receive path or the local oscillator (LO) path. This work introduces a new phase shifting technique that avoids the loss, power consumption, and phase shift resolution trade-offs of conventional topologies. In addition, several other new concepts are presented that reduce the power with no noise figure penalty. To demonstrate the efficacy of the proposed concepts, an eight-element direct-conversion RX with on-chip LO generation has been realized in 28-nm CMOS technology. The RX draws 156 mW, achieving a minimum noise figure of 3.7 dB, a phase resolution of

10°, and an LO jitter of 155 $\mathrm{fs_{rms}}$.

The dissertation of Pawan Kumar Khanna is approved.

M.C. Frank Chang

Danijela Čabric

Gregory J. Pottie

Behzad Razavi, Committee Chair

University of California, Los Angeles

2023

To my parents and to Parikshit

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Curriculum Vitae

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CHAPTER 1

Introduction

1.1 Motivation

The 5G New-Radio (NR) standard includes bands in the millimeter-wave (mmWave) spectrum that provide channel bandwidth of up to 400 MHz. When compared to the maximum bandwidth of lower frequency (sub-7-GHz) bands of the same standard, mm-Wave bands can provide four times the bandwidth, yielding faster data rates [1]. However, mmWave links suffer from large path loss. Friis' transmission equation expresses the free-space path loss experienced during line-of-sight transmission as a function of carrier frequency and other parameters as follows [2]:

$$P_r = P_t + G_t + G_r + 20log\left(\frac{c}{4\pi Rf}\right)[dBm] \tag{1.1}$$

where P_r is the received power, P_t is the isotropic transmitted power, G_t and G_r are the transmit and receive antenna gain respectively, c is the speed of light in free space, R is the transmission distance, and f is the carrier frequency. As can be seen from the above expression, the path loss increases with the square of the frequency. To counteract this extra loss at higher frequencies, beamforming is commonly used. Beamforming involves transmitting and receiving directive beams by utilizing an array of antennas. For such an array, the antenna gain is proportional to the square of the number of antennas present in the array. Since the size of a single antenna is inversely proportional to the frequency, the number of antennas within the same physical aperture, increase proportionally with the frequency. The resultant array gain in fact, results in the received power to increase proportionally with the frequency [3].

Within the mm-Wave spectrum, many transceiver implementations targeting the 26.5 GHz - 29.5 GHz band have been reported recently. These transceivers typically employ beamforming to realize directive beams thereby, raising the transmit antenna gain and improving the receiver sensitivity in order to overcome the high path loss at 28 GHz [4]. Multiple receiver (RX) elements, required to implement beamforming, raise the power consumption of the overall receiver underscoring the importance of having low power consumption per element.

The contrast in power consumption of cellular receivers for lower frequency bands and the 28-GHz band can be seen by comparing recent works in the literature. The RX in [5] supports various cellular bands between 0.5 GHz to 2.7 GHz and consumes 17.6 mA current whereas, the 28-GHz RX in [6] consumes 340 mA current, which is the lowest power consumption for an eight-element RX reported in the literature. It is worth noting that despite consuming higher power, the single element noise figure (NF) for the RX in [6] is 7.3 dB, significantly worse than the 2.5 dB NF achieved in [5].

Beamforming functionality makes the RX architecture more complex because each element needs to introduce a phase shift before the signals are combined. Additionally, until the signals are combined, every element has a separate receive path, adding to the total power consumption.

1.2 Architectural Choices for Beamforming Receivers

Beamforming RX architectures can be divided into three categories based on the method employed for phase shifting. The advantages and challenges associated with each architecture are as follows:

1. **Phase shifting in baseband**

   Phase shifting in baseband is realized by multiplying the quadrature baseband signals with programmable weights and then combining them as shown in Fig. 1.1. Since it is possible to implement programmable gain amplifiers with high resolution at baseband

frequencies, this architecture provides high phase shift resolution. For instance, phase shift resolution realized in [7] is 6 bits. The receiver in [8] downconverts the RF signal to 1 GHz and digitizes it before performing quadrature mixing, phase shifting, and signal combining in digital domain, achieving a phase shift resolution of 10 bits.

The downside of this architecture is the high power consumption as each element requires a separate low-noise amplifier (LNA), quadrature mixer, and set of programmable gain amplifiers. The local oscillator (LO) distribution also becomes complex because the LO signal has to be routed to multiple mixers.

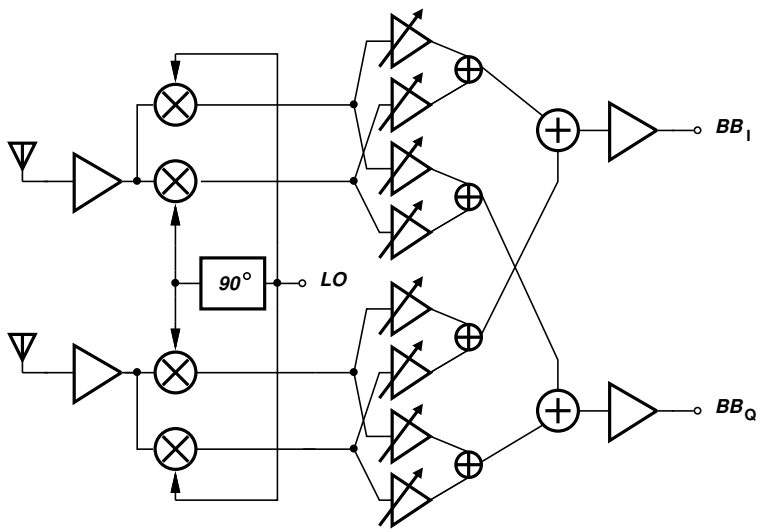


Figure 1.1: Phase shifting in baseband

2. **Phase shifting in LO path**

   The phase shifting operation can be implemented in the LO path rather than the receive path as shown in Fig. 1.2 [9] [10]. This architecture eliminates the programmable gain amplifiers needed to implement phase shifting in baseband. However, high-frequency phase shifters are required in the LO path. Since high-frequency phase shifters invariably are lossy, additional power is needed for the LO distribution.

3. **Phase shifting in RF path**

   Performing phase shifting and signal combining in the RF path, as shown in Fig. 1.3, allows sharing of a single mixer between all the elements and the LO routing is simpli-

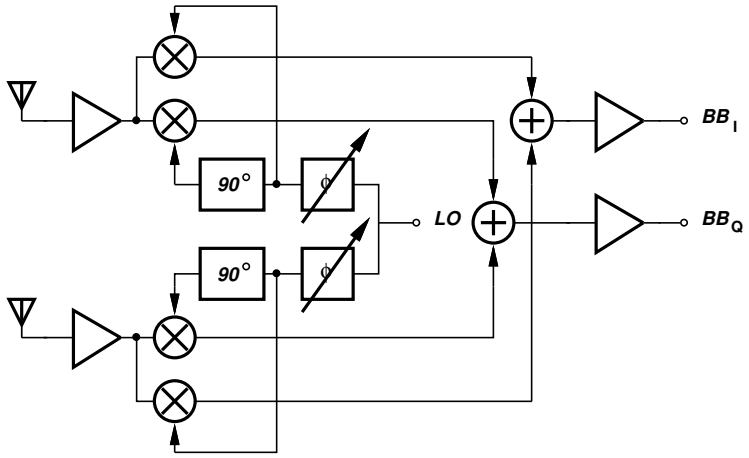


Figure 1.2: Phase shifting in LO path

fied as a result. The downside of this architecture is the presence of RF phase shifters which often add loss to the signal path, necessitating higher power consumption in the LNA. RF phase shifters can be implemented in a number of ways [11] [12] [13] [14]. These are discussed in detail in the next section.

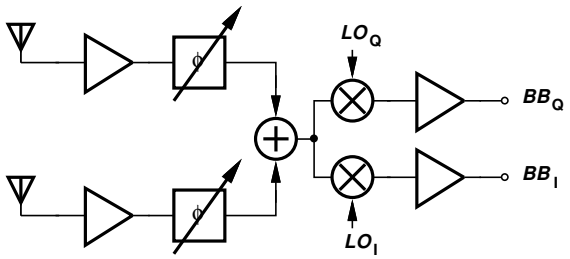


Figure 1.3: Phase shifting in RF path

Table 1.1 lists the performance summary of recently published receivers for the 28-GHz band. Comparing the power consumption per element specification of different types of phase shifting architectures, it can be concluded that from the perspective of power consumption, RF phase shifting techniques appear more favorable than LO or baseband ones. It is also worth noting that amongst RF phase shifting architectures, the best phase resolution (5°) is obtained by [13]. However, their power consumption is also significantly higher than other works based on RF phase shifting.

Work [9] implements LO phase shifting and achieves an impressive phase shift resolution of 0.3° but has a very high power consumption of 148 mW per element. Similarly, [8]

achieves a phase shift resolution of 3° but again has a very high power consumption of 177 mW per element. There is an indication that existing phase shifting techniques have a trade-off between phase shift resolution and power consumption. The next section delves deeper into the RF phase shifting architectures demonstrated in the literature and the phase shift resolution-power consumption trade-off present in them.

	Phase shifting arch.	**Tech.**	**RF Freq. (GHz)**	**No. of RX elements**	**NF_{min} (dB)**	**Gain (dB)**	**Total RX pwr (mW)**	**RX pwr /element /stream**	**Phase Res. (°)**
[6] **Mondal JSSC'18**	RF	65-nm CMOS	25 - 30	8	7.3	34 (1 element)	340	27.5	-
[15] **Kim JSSC'18**	RF	28-nm CMOS	25.8 - 28	8	6.7	69 (8 elements)	400	50	45
[16] **Dunworth ISSCC'18**	RF	28-nm CMOS	25.8 - 30.2	24	4.4	34 (4 elements)	167 (4 element)	42.5	45
[17] **Yoon RFIC'19**	RF	28-nm CMOS	26.5 - 29.5	16	3.5	60 (16 elements)	539	33.7	22.5
[13] **Sadhu JSSC'17**	RF	130-nm SiGe	27.3 - 28.8	32	6^{α}	35 (1 element)	3299	103.1	5
[9] **Pang JSSC'19**	LO	28-nm CMOS	26.5 - 29.5	4	4.1	12 (1 element)	592	148	0.3
[10] **Garg JSSC'21**	LO	65-nm CMOS	28	4	6	≥16 (1 element)	450	28.1^{*}	22.5
[8] **Lu JSSC'21**	Baseband (Digital)	40-nm CMOS	28	16	7	-	2800	177	3

$^{\alpha}$NF measured for LNA, switch, and off-mode PA.

*Total power, including the power consumption of LNAs and RF mixers, has been normalized by no. of elements x no. of output streams, even though the bifurcation of the signal path into four output streams happens after RF mixing. This method of computing the contribution of a single element's single output stream power to the total power is misleading.

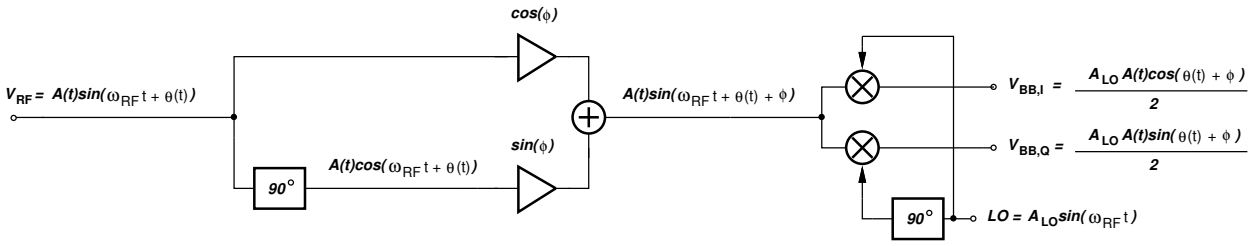
Table 1.1: Recent state-of-art 28-GHz beamforming receivers

1.3 RF phase shifting Architectures and Challenges

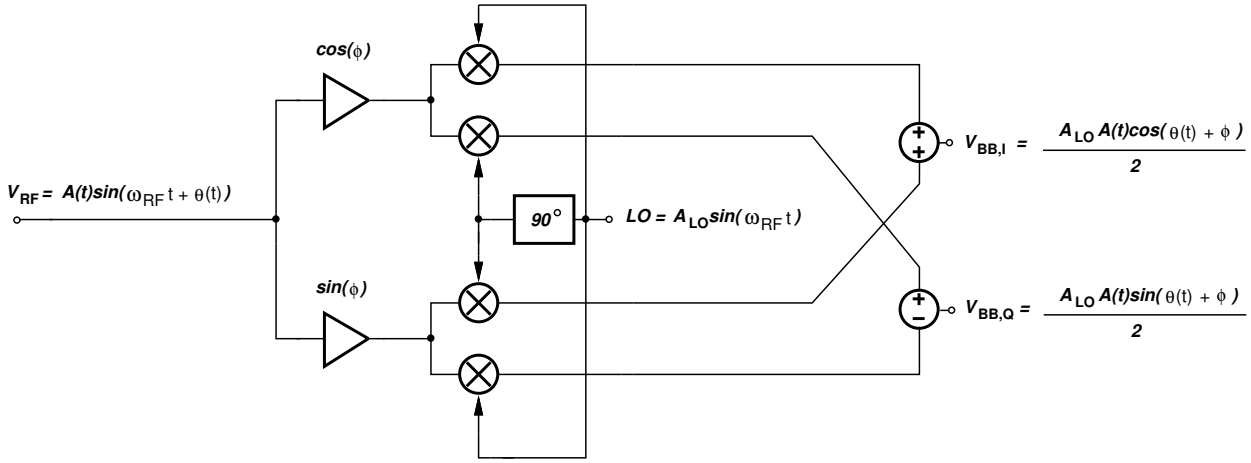
1.3.1 Quadrature-combining-based phase shifting

The quadrature-phase shifted signal can be combined with the original signal after applying appropriate weighting to both, to obtain an arbitrary phase shift. The quadrature signal generation, weighting, and combining can be done in RF domain as shown in Fig. 1.4a. The work in [18] implements this technique for beamforming and uses quadrature-all-pass filter to generate the quadrature phase shifted signal. Another way to generate quadrature signals is through quadrature mixing. However, unlike baseband phase shifting, the multiplication of the signal by programmable weights is done in RF domain as shown in Fig. 1.4b [11] [6]. This allows combining the signals in RF domain thereby merging the receive path of all the elements into two paths even though, the actual phase shift happens after downconversion.

Generating phase shift at RF through quadrature combining avoids lossy true-time-delay-based phase shifters. However, it must be noted that a single receive path is split into two branches, one carrying the in-phase signal and the other carrying the quadrature-phase signal. Depending on the phase shift required, the amplifiers implementing the programmable weighting of the signals in these two branches, are only partially on. For instance, consider the case where a 0° phase shift is required. The in-phase branch amplifier is programmed for maximum gain whereas, the quadrature-phase branch amplifier is kept completely off. However, the quadrature-phase branch amplifier still loads the preceding stage necessitating extra power consumption in that stage. In addition, the amplifiers generating programmable weights are designed with the constraint that they should be phase invariant for all gain setting. The phase invariance constraint typically requires gain control techniques that have the same current consumption across all gain settings [18] [6] leading to extra power consumption without a commensurate reduction in the NF.



(a) Quadrature signal generation in RF domain



(b) Quadrature signal generation by quadrature mixing

Figure 1.4: Quadrature-combining-based phase shifting.

1.3.2 True-time-delay-based phase shifting

Advantages of true-time-delay-based phase shifting:

A lossless transmission line (T-line) introduces a time delay to the signal passing through it as shown in Fig. 1.5. The time delay results in a phase shift that increases proportionally with frequency. The signals received by the antennas of a phased-array receiver also experience a time delay with respect to each other. To make the time delay in all the receiver elements equal, so that they combine coherently, it is desirable to introduce a true-time delay in the circuit as opposed to introducing a constant phase shift over frequency.

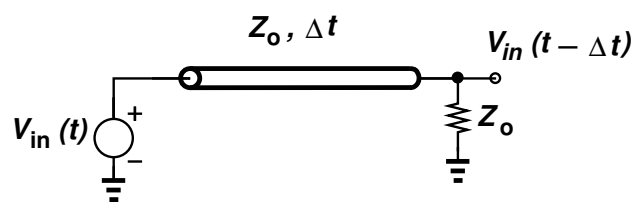


Figure 1.5: True-time delay through lossless T-line

As an example, consider a two-element beamforming receiver having a $\lambda/2$ separation between the two antennas. The receiver receives an amplitude-and-phase-modulated signal incident at an angle α. Figure 1.6 depicts the case when the receiver introduces true-time delay to make the signals of the two elements perfectly coherent. Figure 1.7 depicts the case when the receiver introduces a constant phase shift to correct for the time delay between the signals of the two elements. The signal of the two elements, $A(t)\cdot\sin(\omega_{RF}t - \omega_{RF}\tau + \theta(t))$ and $A(t-\tau)\cdot\sin(\omega_{RF}t - \omega_{RF}\tau + \theta(t-\tau))$ respectively, are not perfectly coherent because the amplitude modulation and phase modulation terms are not affected by the constant phase shift. Suppose the combined signal of the two elements is now downconverted to baseband by means of an IQ mixer. The I and Q outputs are $A(t)\cos(\theta(t))+A(t-\tau)\cos(\theta(t-\tau))$ and $A(t)\sin(\theta(t))+A(t-\tau)\sin(\theta(t-\tau))$ respectively. The extra time delay τ, present in one of the terms of the baseband outputs, is given by:

$$\tau = \frac{\sin\alpha}{2f_c} \tag{1.2}$$

where f_c is the carrier frequency equal to $\omega_{RF}/2\pi$. For an n-element array, the maximum delay between the baseband outputs of the first and the last element occurs for $\alpha = 90°$ and is given by:

$$\tau_{\text{max, n-element array}} = \frac{n-1}{2f_c} \tag{1.3}$$

As long as $\tau_{\text{max, n-element}} \ll$ symbol period of the baseband signal, the delay τ causes negligible inter-symbol interference (ISI). To determine the bound on the channel bandwidth, we can express the symbol period in terms of the channel bandwidth. Suppose the channel bandwidth is denoted by BW, then the symbol period is given by $2/BW$. To maintain negligible ISI:

$$\frac{n-1}{2f_c} \ll \frac{2}{BW} \implies BW \ll \frac{4f_c}{n-1} \tag{1.4}$$

The above expression indicates that ISI introduced due to having a constant phase shift instead of true-time delay in the receiver only becomes a problem for a large number of receiver elements and wide channel bandwidths.

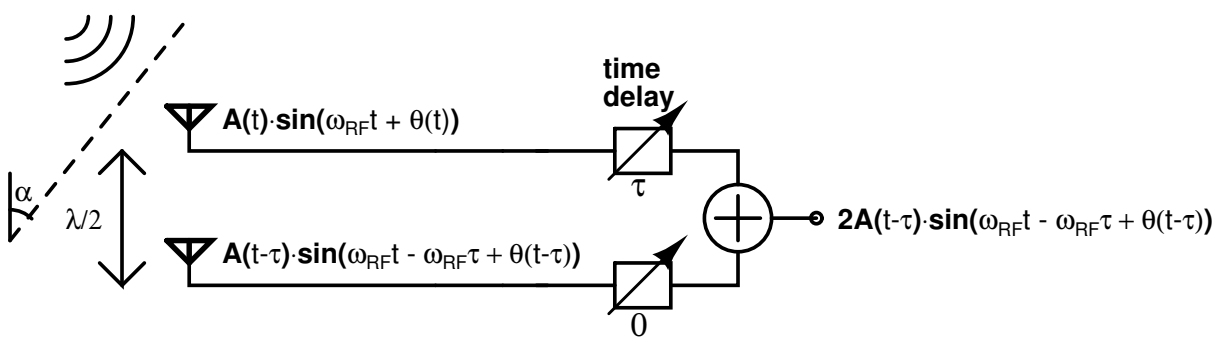


Figure 1.6: Beamforming by applying true-time delay

The second issue arising due to constant phase shift beamforming is beam squinting [19]. Since a constant phase shift translates to a different time delay at different carrier frequencies, the direction at which the receiver array points, changes with the carrier frequency. For example, Fig. 1.8a depicts an eight-element receiver array programmed for a reception angle of 43.4°. The phase shift within each element is set accordingly. However, these phase shift settings are done for a specific carrier frequency, 28 GHz. Figure 1.8b

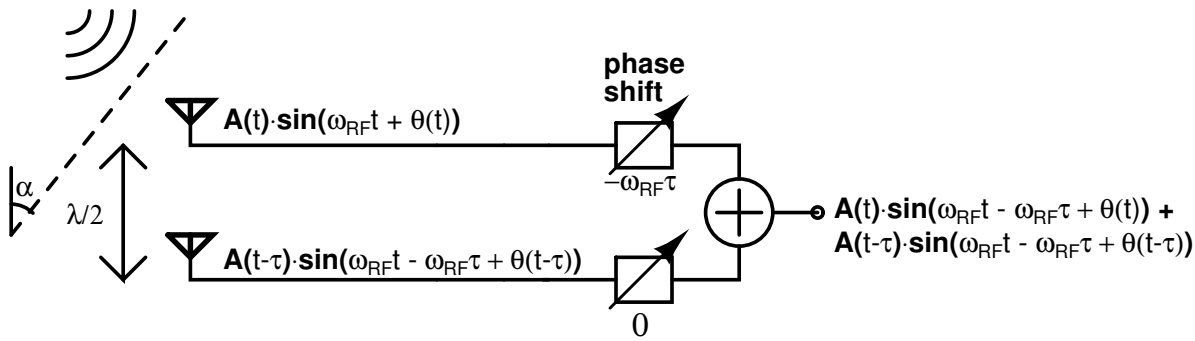
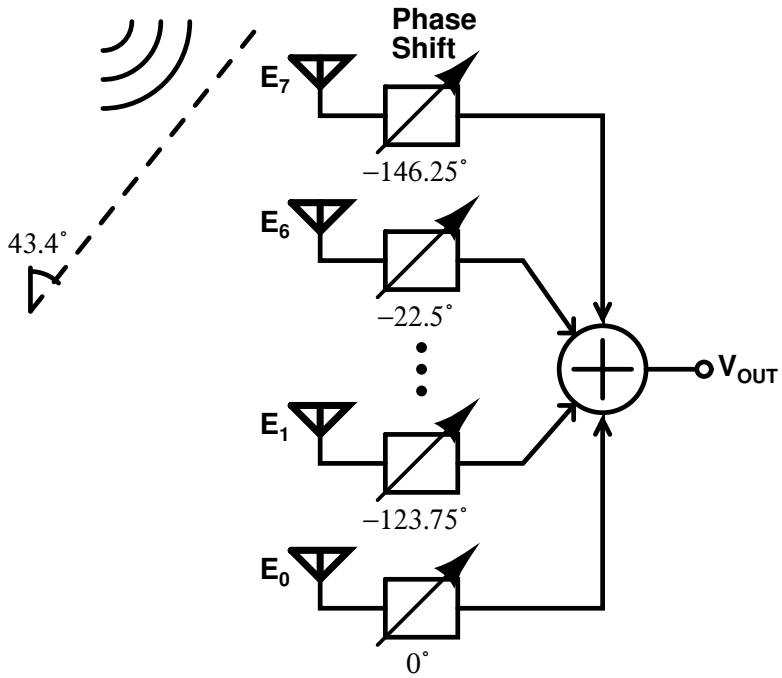
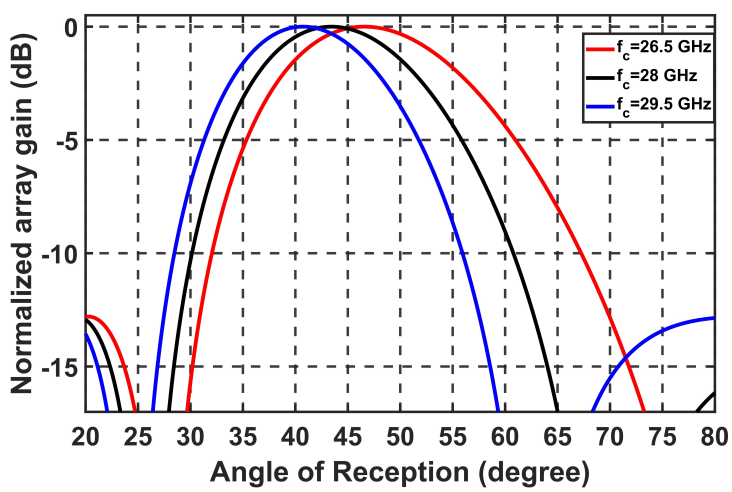


Figure 1.7: Beamforming by applying constant phase shift over frequency

shows how the beam pattern changes when the carrier frequency changes from 28 GHz to 26.5 GHz and 29.5 GHz. The reception angle changes based on the carrier frequency from 43.4° at 28 GHz to 46.6° at 26.5 GHz, and 40.7° at 29.5 GHz. Beam squinting causes variation in array gain across the frequency band of interest and these variations become larger for larger arrays as the 3-dB beamwidth is smaller for larger arrays. Beam squinting does not occur for RXs employing true-time-delay-based beamforming. For example, the eight-element RX shown in Fig. 1.9a employs true-time-delay in every element and the resultant beam patterns for different carrier frequencies don't show beam squinting [Fig. 1.9b].

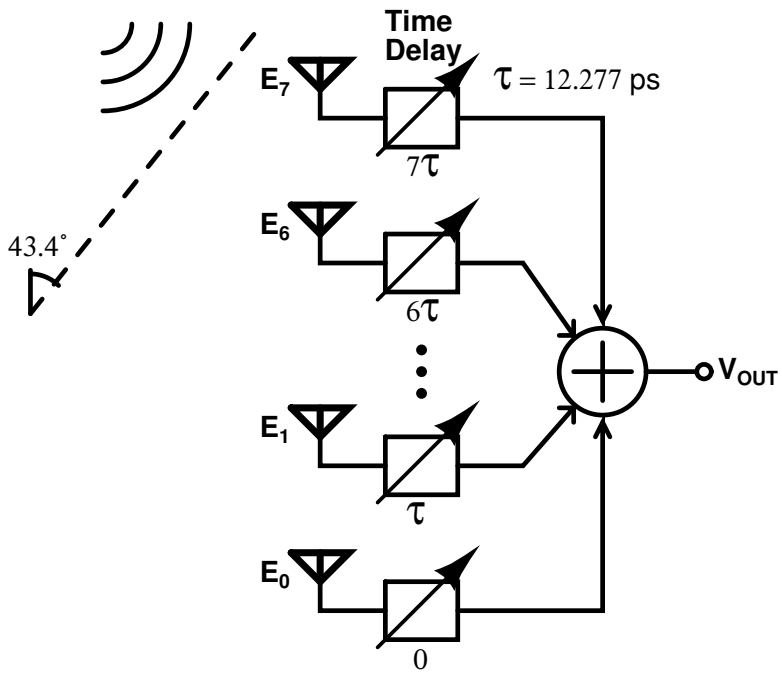


(a)

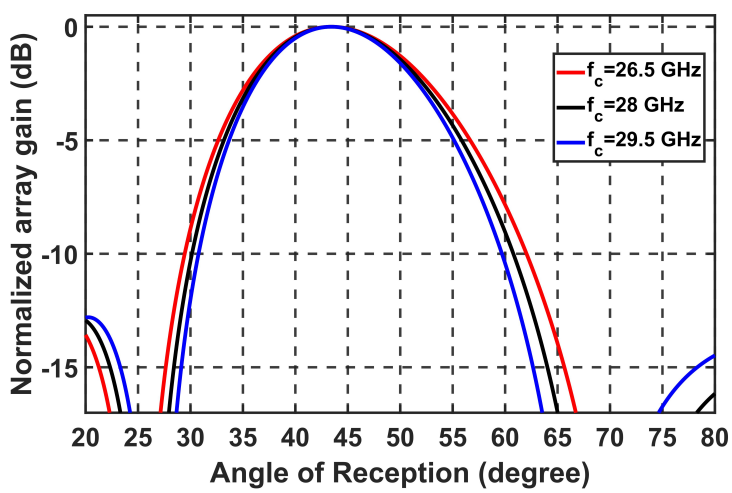


(b)

Figure 1.8: (a) Beamforming receiver with phase shift, (b) Beam pattern variation with carrier frequency shows beam squinting.



(a)



(b)

Figure 1.9: (a) Beamforming receiver with true-time delay, (b) Beam pattern variation with carrier frequency does not show beam squinting.

True-time-delay-based phase shifter architectures:

In literature, true-time delay has typically been implemented through T-lines. The T-line can be implemented in a conventional structure like microstrip, coplanar waveguide, etc., or by a lumped LC model. The previously reported true-time delay-based phase shift approaches are as follows:

1. **Bypassing sections of lumped T-line**

   The basic idea is to implement a lumped T-line using multiple LC π sections where each section can be bypassed with a switch as shown in Fig. 1.10. This approach was reported in [12] and later implemented for 28 GHz in [15]. In the bypass state, the shunt capacitors C1 and C2 are disconnected from ground by means of switches. The purpose of the inductors L2 and L4 is to resonate with the off-state parasitic capacitance of these switches to present a high impedance to the shunt capacitors. The challenge associated with this technique of phase shifting is that a trade-off exists between the phase shift resolution and the loss of the phase shifter. To increase the resolution, more LC sections are required to be cascaded, and since each section requires bypass switches, the signal passing through these extra switches experiences more attenuation. For example, the phase shifter implemented in [15] has a phase shift range of 325° with a resolution of 45° and loss of 8-9 dB across different phase shift settings.

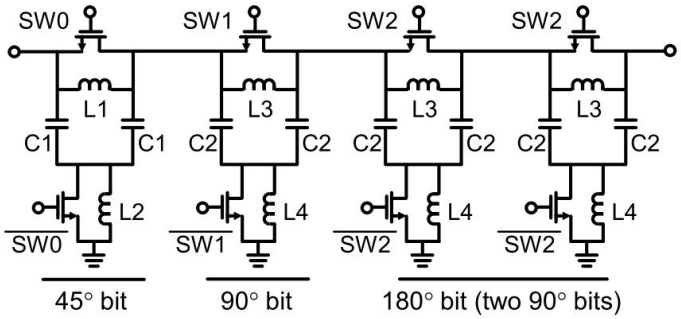


Figure 1.10: [Kim et al, JSSC, May 2018] Bypassing sections of T-line to get programmable phase shift.

2. **Tapping phase from lumped T-line**

   This approach involves tapping different phase shifted points on a lumped T-line using common-source transistors as shown in Fig. 1.11. The gate capacitance of the transistors contributes to the shunt capacitance of the LC π sections that form the T-line [14]. The trade-off between phase resolution and power consumption is present in this approach as well. Increasing phase resolution requires constructing the T-line with smaller LC π sections and each section being tapped with a common-source transistor to sense the phase shifted signal. The increase in the number of phase-tapping transistors loads the T-line capacitively, bringing down its characteristic impedance (Z_0). Consequently, the stage driving the T-line requires higher power to achieve moderate gain and noise figure (NF).

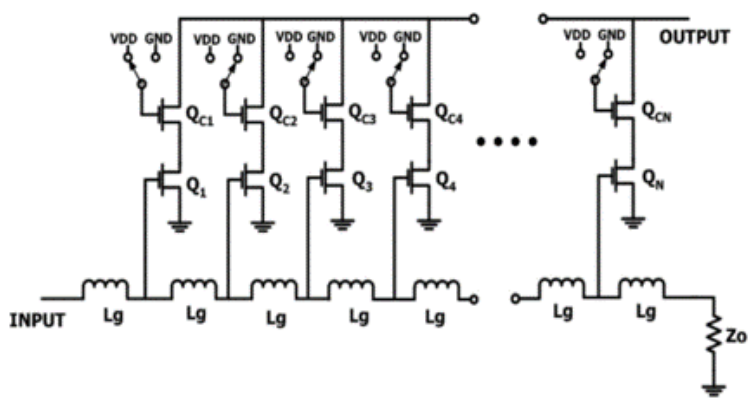


Figure 1.11: [Kang and Hong, TMTT, July 2007] Tapping phase from lumped T-line.

3. **Digitally changing the delay of a T-line section**

   This technique, adopted in [13], implements programmable phase shift by breaking a T-line into smaller sections. Each section can either be set to a low-delay mode [Fig. 1.12(a)] or a high-delay mode [Fig. 1.12(b)]. In the low-delay mode, the signal-return paths adjacent to the forward-signal path, are enabled by switches labeled 'L' which short these return paths to the previous T-line section. The resultant coplanar-waveguide section has a certain delay, and Z_0. In the high-delay mode, the T-line structure undergoes two changes. Firstly, the adjacent return paths are

disabled which means that the return paths farther away (marked with backward arrows in Fig. 1.12(b)) carry the return current. The return path moving away from the forward path increases the effective inductance per section of the T-line and reduces the capacitance per section. Secondly, a MIM capacitor is connected between the forward path and return path by means of switch labeled 'C'. This capacitor increases the capacitance per section of the T-line. The cumulative effect of the two changes made to the T-line is that the Z_0, given by $\sqrt{L_2/C_2}$ (L_2 and C_2 represent the per section inductance and capacitance of the T-line in the high-delay mode, respectively) remains the same as $\sqrt{L_1/C_1}$ (L_1 and C_1 represent the per section inductance and capacitance of the T-line in the low-delay mode, respectively). However, the delay in the high-delay mode, given by $\sqrt{L_2C_2}$, is larger than the delay in the low-delay mode, given by $\sqrt{L_1C_1}$.

This technique results in an impressive phase shift resolution of 5°, and a low rms error in the phase resolution of 0.81°. However, the addition of switches in series with the return path in the high-delay mode, and in series with the MIM capacitor in the low-delay mode, introduces losses. Infact, to equalize the loss between the two modes, the switch labeled 'S' is connected between the forward path and return path in the low-delay mode to introduce additional loss. This results in a 9.3 dB loss across the T-line, providing 210° of total phase shift. The comparatively large loss across the phase shifter results in a 103 mW power consumption per receive element. The trade-off between phase resolution and power consumption is once again evident.

4. **Digitally Controlled Artificial Dielectric (DiCAD) [20]**

   This technique also involves digitally modifying the structure of a T-line to change its properties, including delay. The basic idea is to digitally realize a T-line that can switch between structures shown in Fig. 1.13. In the T-line in Fig. 1.13(b), the horizontal metal strips below the T-line do not have any role to play as they can neither carry the signal current nor do they appreciably affect the electric field lines between the differential T-line segments. However, in the T-line shown in Fig.

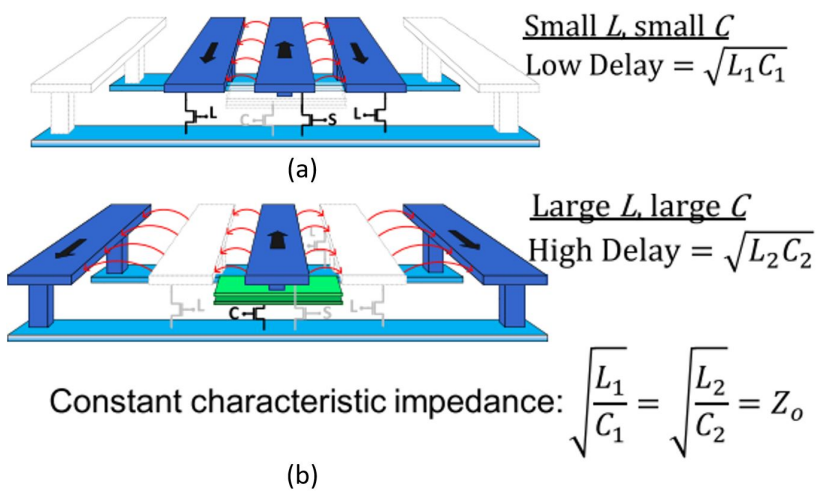


Figure 1.12: [B. Sadhu et al, JSSC, Dec 2017] T-line section for the phase shifter operating in two modes: (a) low-delay mode, (b) high-delay mode.

1.13(a), the metal strips behave as dipoles, opposing the electric field between the differential T-line segments. This effect translates to a larger effective capacitance between the T-line segments. Since the inductance is still unaffected, the delay across the T-line increases. The Z_0 of the T-line is also expected to drop which can be an issue for certain applications. In practice, a π switch placed between the metal bars, as shown in Fig. 1.14 is responsible for switching the T-line between the above two modes. Another drawback of this approach is that the π switch leads to increased loss. For instance, [21] reports that when the switch is on, the loss of the T-line increases from 4 dB/mm to 14 dB/mm.

To gauge the performance of this phase shifter architecture, we design a DiCAD T-line section in our technology (TSMC 28-nm CMOS with 9-metal stack) [Fig. 1.15]. The 119 μm long section is operated in two extreme modes: when all the π switches connecting the horizontal strips are turned on and when all the switches are turned off. When all the switches are off, the T-line provides a phase shift of 12.8° and when all the switches are on, the T-line provides a phase shift of 22.9°. Since there are a total of 30 strips, each controlled by a separate π switch, the phase resolution is expected to be less than 1°. While such a fine phase resolution translates

to certain advantages related to beamforming, for user equipment applications, where the number of receiver elements are typically of the order of eight or 16, such a fine phase resolution is generally not required, as will be shown in the next section. Once again, a fine phase resolution comes at the cost of low characteristic impedance, 56 Ω in the low-delay mode and 32 Ω in the high-delay mode. Also, a lumped T-line implementation occupies a relatively large area. For instance, for a 180° phase shift range, the T-line will occupy an area of 0.15 mm^2. For an eight-element receiver, the total area consumed by the T-line phase shifter would be 1.2 mm^2.

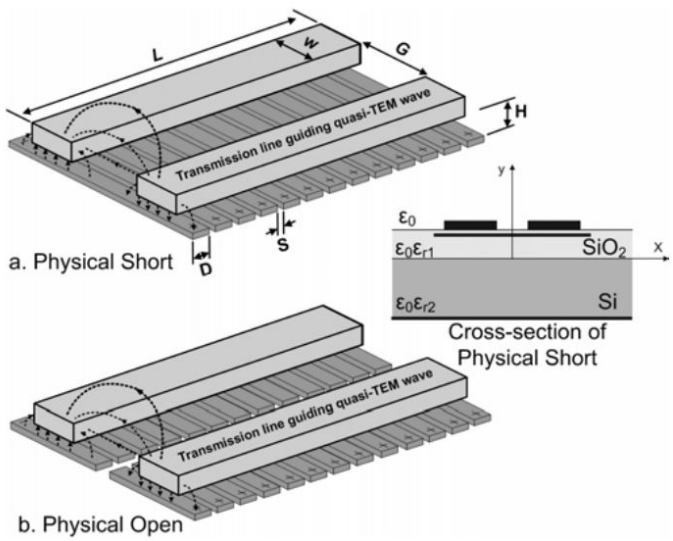


Figure 1.13: [T. LaRocca et al, IMS, June 2008] T-line structure with different configurations of metal strips placed beneath (a) high-capacitance and high-delay mode, (b) low-capacitance and low-delay mode.

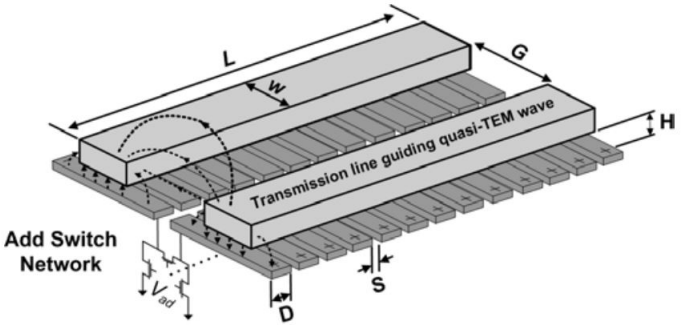


Figure 1.14: [T. LaRocca et al, IMS, June 2008] T-line with π switches controlling the delay.

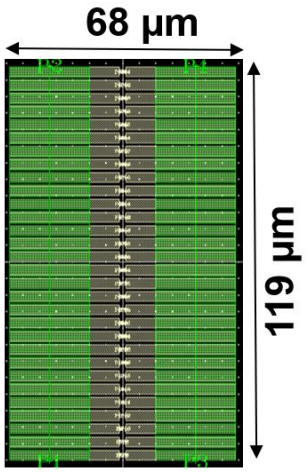


Figure 1.15: DiCAD T-line section adopted in our technology for performance evaluation.

1.4 Design Goals

1.4.1 Number of RX elements and phase shift resolution

The number of receiver elements and the phase shift resolution determine the array gain degradation, beam steering resolution, beam width, and side lobe levels. Beam pattern plots depict these effects. Figure 1.16 shows the beam patterns for uniform phase shift applied between adjacent elements. The angle of reception of the beam is measured from the axis perpendicular to the antenna array. Three cases are considered, (i) number of elements = 4 and phase shift resolution = 22.5°, (ii) number of elements = 4 and phase shift resolution = 11.25°, and (iii) number of elements = 8 and phase shift resolution = 11.25°. The specific beam patterns for 0° and 40° angle of reception are plotted in black and red colors. Table 1.2 lists the array gain degradation, beam-steering resolution, 3-dB beam width, and side-lobe level for each case.

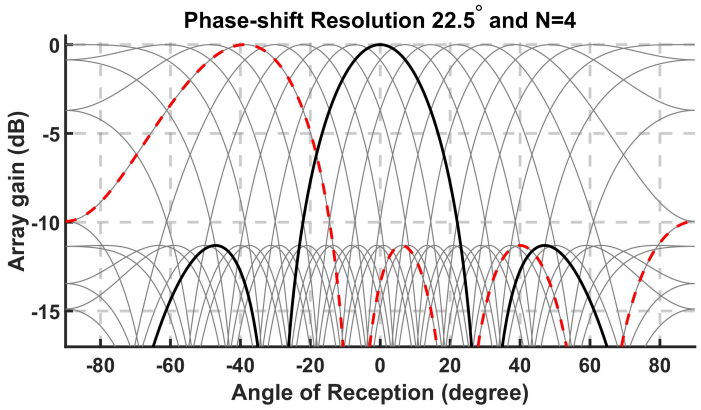
Number of elements	4	4	8
phase shift resolution	22.5°	11.25°	11.25°
Array gain degradation	0.21 dB	0.05 dB	0.22 dB
Beam-steering resolution*	7.2°	3.6°	3.6°
3-dB beam width*	26°	26°	13°
Side-lobe level*	-11.3 dB	-11.3 dB	-12.8 dB

*For angle of reception = 0°

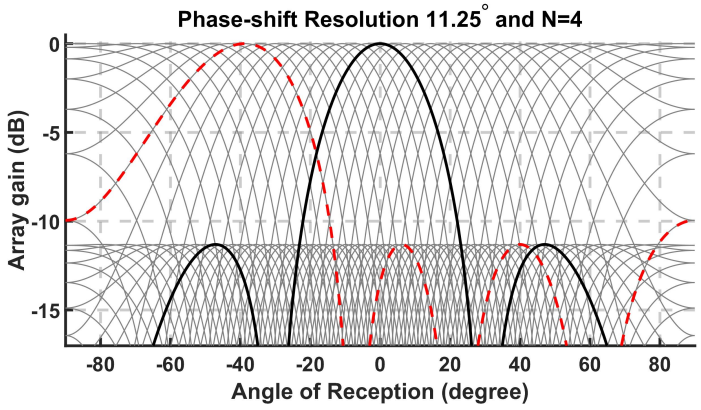
Table 1.2: Variation of beam pattern parameters with number of elements and phase shift resolution

From these results, the following conclusions can be drawn:

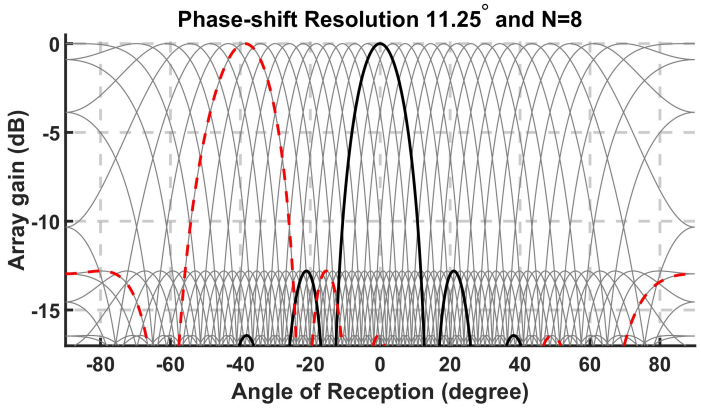
1. The array gain degradation reduces by increasing the phase shift resolution. For instance, the array gain degradation reduces from 0.21 dB to 0.05 dB on increasing the phase shift resolution from 22.5° to 11.25°.



(a)



(b)



(c)

Figure 1.16: (a) Beam patterns for N=4 and phase resolution = 22.5°, (b) Beam patterns for N=4 and phase resolution = 11.25°, and (c) Beam patterns for N=8 and phase resolution = 11.25°

2. The array gain degradation increases by increasing the number of elements as the beam becomes narrower with increase in the number of elements. For instance, for a fixed phase resolution of 11.25°, if the number of elements are increased from four to eight, the 3-dB beam width reduces from 26° to 13°. As a result, the array gain degradation also increases from 0.05 dB to 0.22 dB.

3. The beam steering resolution is determined by the phase shift resolution only and improves with increase in phase shift resolution. For instance, the beam steering resolution for phase shift resolution of 22.5° is 7.2° whereas, for a phase shift resolution of 11.25°, the beam steering resolution is 3.6°.

4. The side-lobe levels depend on the number of elements only, reducing, albeit only slightly, by increasing the number of elements from four to eight from -11.3 dB to -12.8 dB.

The first two conclusions suggest that receivers with a larger number of elements require a larger phase shift resolution as well to keep the array gain degradation to a negligible level. Eight elements for the user equipment are sufficient to realize 5G communication links with the base station [9]. Since these eight elements are likely to be arranged in a 4x2 array structure [15], we focus our attention on the beam pattern for four elements to derive the phase shift resolution requirement. A phase shift resolution of 11.25° gives negligible array gain degradation of 0.05 dB at all angles of reception. Since the array gain degradation is equal to the error-vector-magnitude (EVM) degradation for beamforming RX (proved later in the section), the degradation in array gain due to finite phase resolution should be kept minimal. So a phase shift resolution of 11.25° is sufficient for an eight-element RX.

Relationship between array gain and EVM for beamforming RX:

To find the relationship between array gain and EVM, we consider a four-element beamforming RX model [Fig. 1.17]. Each element introduces additive noise, which is uncorrelated to the noise introduced by the other elements. The phase shifter present in every element introduces an appropriate phase shift to make the signals of all the elements

coherent. The signals are then combined and downconverted by means of a quadrature mixer. We find the EVM of the downconverted I and Q baseband signals.

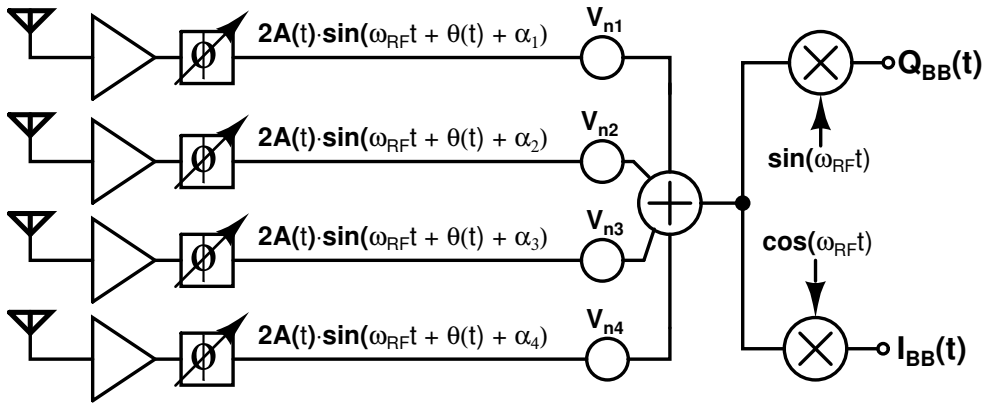


Figure 1.17: Four-element beamforming RX model.

The A(t) and θ(t) terms represent the amplitude and phase modulation in the received signal, respectively. Each element has a finite resolution phase shifter to correct for the phase mismatch between the received signal of each element. The residual phase mismatch of each element is represented by α_1, α_2, α_3, and α_4 terms. The additive noise of each element is represented by the V_{n1}, V_{n2}, V_{n3}, and V_{n4} random variables. The I_{BB}(t) and Q_{BB}(t) signals are given by the following expressions:

$$Q_{BB}(t) = A(t)\cos(\theta(t)+\alpha_1) + V_{n1}\sin(\omega_c(t)) + A(t)\cos(\theta(t)+\alpha_2) + V_{n2}\sin(\omega_c(t)) \\ + A(t)cos(\theta(t)+\alpha_3) + V_{n3}\sin(\omega_c(t)) + A(t)\cos(\theta(t)+\alpha_4) + V_{n4}\sin(\omega_c(t)) \quad (1.5)$$

$$I_{BB}(t) = A(t)\sin(\theta(t)+\alpha_1) + V_{n1}\cos(\omega_c(t)) + A(t)\sin(\theta(t)+\alpha_2) + V_{n2}\cos(\omega_c(t)) \\ + A(t)sin(\theta(t)+\alpha_3) + V_{n3}\cos(\omega_c(t)) + A(t)\sin(\theta(t)+\alpha_4) + V_{n4}\cos(\omega_c(t)) \quad (1.6)$$

To find the EVM we need to find the mean error vector magnitude and normalize it to the mean symbol magnitude. This averaging is done assuming that the same signal is being transmitted, or in other words, θ(t) and A(t) remain constant. The mean symbol magnitude is given by:

$$\Big(E\Big(I_{BB}(t)\Big)\Big)^2+\Big(E\Big(Q_{BB}(t)\Big)\Big)^2=$$
$$\Big(A(t)\cos\Big(\theta(t)+\alpha_1\Big)+A(t)\cos\Big(\theta(t)+\alpha_2\Big)+A(t)\cos\Big(\theta(t)+\alpha_3\Big)+A(t)\cos\Big(\theta(t)+\alpha_4\Big)\Big)^2+$$
$$\Big(A(t)\sin\Big(\theta(t)+\alpha_1\Big)+A(t)\sin\Big(\theta(t)+\alpha_2\Big)+A(t)\sin\Big(\theta(t)+\alpha_3\Big)+A(t)\sin\Big(\theta(t)+\alpha_4\Big)\Big)^2 \tag{1.7}$$

The above expression is exactly similar to the magnitude square of the sum of the following four phasors: $A(t)e^{j(\theta(t)+\alpha_1)}$, $A(t)e^{j(\theta(t)+\alpha_2)}$, $A(t)e^{j(\theta(t)+\alpha_3)}$, and $A(t)e^{j(\theta(t)+\alpha_4)}$. This same expression is also equal to: array gain of the beamforming receiver $\times$ $A^2(t)$. For the case where the outputs of the four elements do not have any phase mismatch between them, α_1, α_2, α_3, and α_4 are equal to 0. The mean symbol magnitude, in that case, comes out to be $16 \times A^2(t)$ as expected, where the array factor is 16 because of perfectly coherent signal combining. So the mean symbol magnitude can be rewritten as:

$$\Big(E\Big(I_{BB}(t)\Big)^2+E\Big(Q_{BB}(t)\Big)^2\Big)=A^2(t)\times AG \tag{1.8}$$

where AG denotes the array gain. Now, to find the mean error vector magnitude we use the following expression:

$$E\Big(I_{BB}(t)-E\Big(I_{BB}(t)\Big)\Big)^2+E\Big(Q_{BB}(t)-E\Big(Q_{BB}(t)\Big)\Big)^2=$$
$$E\Big(V_{n1}^2\sin^2\Big(\omega_c(t)\Big)\Big)+E\Big(V_{n2}^2\sin^2\Big(\omega_c(t)\Big)\Big)+E\Big(V_{n3}^2\sin^2\Big(\omega_c(t)\Big)\Big)+E\Big(V_{n4}^2\sin^2\Big(\omega_c(t)\Big)\Big)+$$
$$E\Big(V_{n1}^2\cos^2\Big(\omega_c(t)\Big)\Big)+E\Big(V_{n2}^2\cos^2\Big(\omega_c(t)\Big)\Big)+E\Big(V_{n3}^2\cos^2\Big(\omega_c(t)\Big)\Big)+E\Big(V_{n4}^2\sin^2\Big(\omega_c(t)\Big)\Big)$$
$$=E(V_{n1}^2)+E(V_{n2}^2)+E(V_{n3}^2)+E(V_{n4}^2)=4E(V_{n1}^2) \tag{1.9}$$

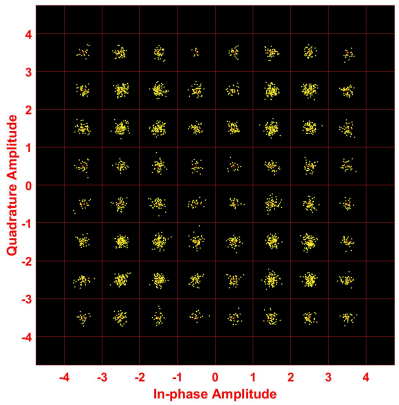
Now, the EVM is given by:

$$EVM=\frac{\text{mean error vector magnitude}}{\text{mean symbol magnitude}}=\frac{4\cdot E(V_{n1}^2)}{AG\cdot A^2(t)} \tag{1.10}$$
$$EVM_{dB}=10\log\left(\frac{E(V_{n1}^2)}{A^2(t)}\right)+6\,dB-AG_{dB}$$
$$EVM_{dB}=EVM_{single-element,dB}+6\,dB-AG_{dB} \tag{1.11}$$

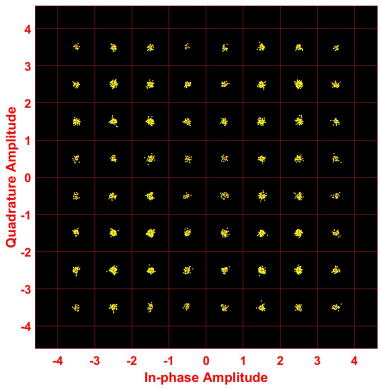
This expression proves that any degradation in the array factor directly degrades the EVM as well. In order to depict this result, we simulate the receiver model by sending a 64-QAM signal to the four-element receiver. The noise added by each element is modeled by independent Gaussian random variables. If only one of the elements is activated, the resultant received constellation is depicted in Fig. 1.18a and shows an EVM of -27.82 dB. If the four elements are all activated and the four elements don't have any phase mismatch between them then the resultant constellation, depicted in Fig. 1.18b, shows an EVM of -33.83 dB. Now we mimic the conditions for maximum array gain degradation for a four-element RX with 45° phase shift resolution, i.e. beam directed at -7.14°. The theoretical array gain degradation in this case is 0.87 dB. The constellation for this case is depicted in Fig. 1.18c and shows an EVM of -32.98 dB which is 0.85 dB lower than the case where there was no phase mismatch between all the four elements.

1.4.2 Design goals based on prior art

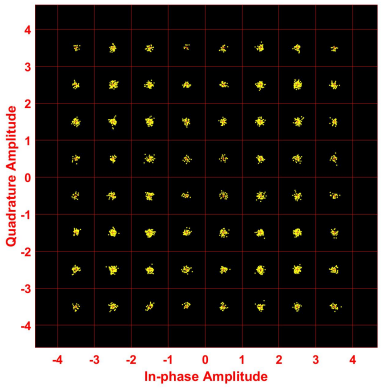
Table 1.3 lists the performance summary of the recent state-of-art 28-GHz beamforming receivers. Based on the performance achieved by the prior art, and the analysis presented in this section, we fix our design goals as shown in the last column of the table. We aim to design an eight-element beamforming RX that matches prior art in terms of NF but consumes two times lesser power. We note that none of the prior work implements complete on-chip LO synthesis. References [6], [15], and [17] require an off-chip clock to generate the LO. Considering the low-jitter requirement on the external clock, if it were to be generated on-chip, the synthesizer would require an appreciable amount of power consumption. A similar argument also holds for [16] as the output of the RX is at 6.5 GHz intermediate frequency (IF). We aim to have complete on-chip LO synthesis for our RX including quadrature phase generation to implement direct downconversion.



(a) RX constellation with no beamforming



(b) RX constellation with ideal beamforming (perfectly coherent addition of signals)



(c) RX constellation with realistic beamforming (phase shifter resolution = 45° and angle of reception = -7.14°)

Figure 1.18: Simulated 64-QAM constellations for the four-element RX model

	[6] Mondal JSSC 18	[15] Kim JSSC 18	[16] Dunworth ISSCC 18	[17] Yoon RFIC 19	Design Goals
Input Frequency (GHz)	25 - 30	25.8 - 28	25.8 - 30.2	26.5 - 29.5	26.5 - 29.5
No. of RX Elements	8	8	24	16	8
NF_{min} (dB)	7.3	6.7	4.4	3.5	3.5
Gain (dB)	34 (1 element)	69 (8 elements)	34 (4 elements)	60 (16 elements)	30 (1 element)
On-Chip LO Synthesis?	f_{ext} = 20 - 24 GHz	f_{ext} = 3.11 GHz	IF out = 6.5 GHz	f_{ext} = 5.67 GHz, IF Out = 11 GHz	Yes
Total Power[1] (mW)	223	400	334	270	110
Phase Resolution	N.A.	45°	45°	22.5°	11.25°

[1]For 8 elements

Table 1.3: Recent state-of-art 28-GHz beamforming receivers employing RF phase shifting

CHAPTER 2

Receiver design

2.1 Phase Shifter

2.1.1 The LC π network

A lossless T-line introduces a time delay to the signal passing through it as shown in Fig. 2.1. Assuming an on-chip T-line is used to provide a phase shift of 180° at 28 GHz, its length would be of the order of a few millimeters. To reduce the area overhead, the lumped LC π network shown in Fig. 2.2 can be used as an approximation of a physical T-line [15] [12].

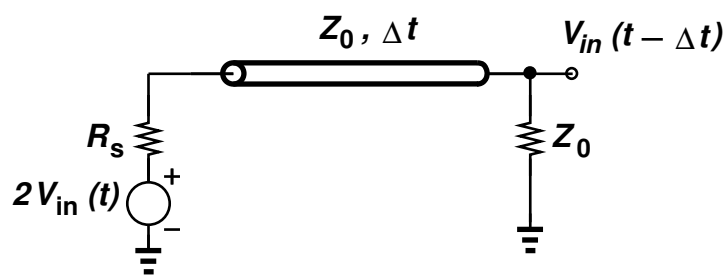


Figure 2.1: Lossless T-line introducing delay

To analyze the LC π network, its ABCD matrix is listed below:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + Z_L Y_C & Z_L \\ Y_C(2 + Y_C Z_L) & 1 + Z_L Y_C \end{bmatrix} \tag{2.1}$$

where $Z_L = jX_L = j\omega L$, $Y_C = jB_c = j\omega C$, and ω is the angular frequency of operation. The condition for matching dictates $S_{11} = 0$ which translates to the following condition:

$$\frac{Z_L}{Z_0} = Y_C Z_0 (2 + Y_C Z_L) \tag{2.2}$$

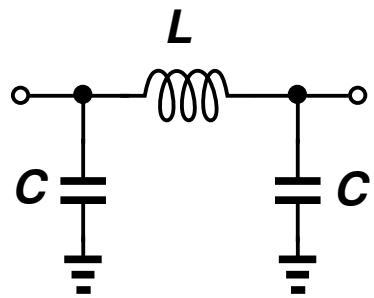


Figure 2.2: LC π network

$$\implies Z_0^2 = \frac{L}{2C(1-\omega^2\frac{LC}{2})} = \frac{L}{2C(1-\frac{\omega^2}{\omega_B^2})} \tag{2.3}$$

where ω_B is the Bragg's frequency given by [22]:

$$\omega_B = \sqrt{\frac{2}{LC}} \tag{2.4}$$

At frequencies above the Bragg frequency, the characteristic impedance of the network becomes imaginary implying that it cannot deliver power to the load. To ensure that the network mimics a T-line closely, its characteristic impedance should be real and stay nearly constant over the frequency range of operation. This condition requires: $\omega \ll \omega_B$. Under the constraint, $\omega \ll \omega_B$, Eq. 2.3 can be approximated as:

$$Z_0 \approx \sqrt{\frac{L}{2C}} \tag{2.5}$$

Now, the S_{21} of the network is analyzed to gauge the phase and magnitude frequency response. The S_{21} is given by the following expression:

$$S_{21} = \frac{2}{(1+Z_LY_C)+\frac{Z_L}{Z_0}+Y_CZ_0(2+Y_CZ_L)+1+Z_LY_C} \tag{2.6}$$

Using Eq. 2.2 to simplify the expression:

$$S_{21} = \frac{1}{1+Z_LY_C+\frac{Z_L}{Z_0}} \tag{2.7}$$

To further simplify the expression, Eq. 2.2 is re-written as:

$$Z_L = \frac{2Y_CZ_0^2}{1-Y_C^2Z_0^2} \tag{2.8}$$

Substituting for Z_L from Eq. 2.8 in Eq. 2.7:

$$S_{21} = \frac{1 - Y_C Z_0}{1 + Y_C Z_0} = \frac{1 - j\omega C Z_0}{1 + j\omega C Z_0} \tag{2.9}$$

$$\implies |S_{21}| = 1 \tag{2.10}$$

The insertion phase, or in other words, the phase shift of the network is given by:

$$\phi = -2\tan^{-1}(\omega C Z_0) \tag{2.11}$$

The above expression can be approximated to a simpler form under the constraint, $\omega \ll \omega_B$ as shown below:

$$\phi \approx -2\tan^{-1}(\omega\sqrt{\frac{LC}{2}}) \tag{2.12}$$

Equation 2.3 and Eq. 2.11 together give the value of L and C for a given Z_0, ω, and ϕ. Next, these expressions are used to design LC π networks as lumped approximations of physical T-lines of different lengths at 28 GHz. S-parameter simulations are used to compare the two and show the limitations of the approximation.

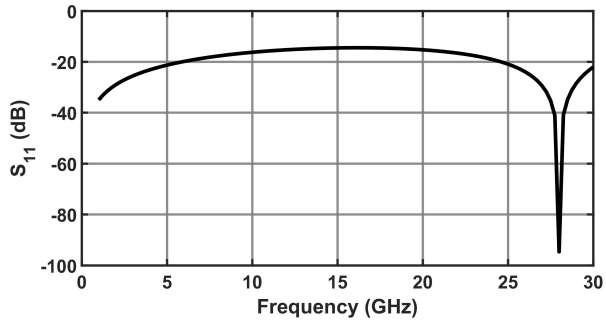
The following three T-lines (having $Z_0 = 50\ \Omega$) and their corresponding LC π networks are simulated and compared:

(a) $\lambda/4$ T-line and LC π network with 90° phase shift at $\omega = 28$ GHz.

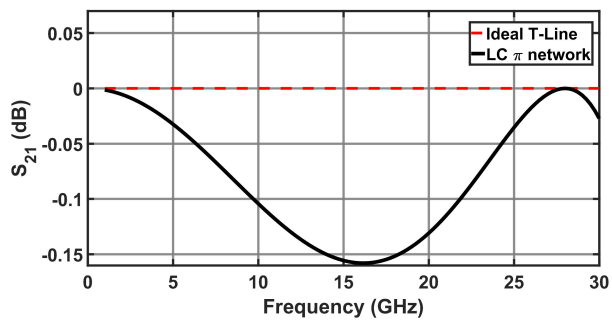
(b) $\lambda/3$ T-line and LC π network with 120° phase shift at $\omega = 28$ GHz.

(c) $5\lambda/12$ T-line and LC π network with 150° phase shift at $\omega = 28$ GHz.

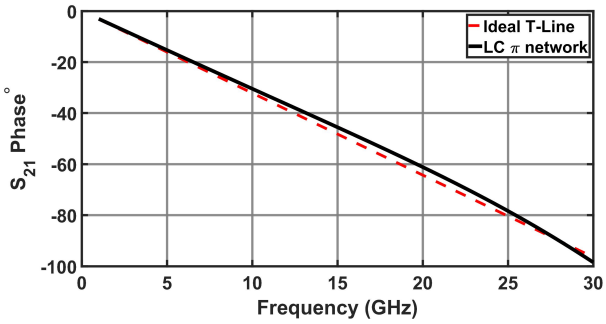
The S_{11} and S_{21} plots for the three cases are shown in Fig. 2.3. The plots illustrate that the matching in the frequency range of interest (26.5 GHz - 29.5 GHz) degrades as the length of the T-line implemented by the network increases. The S_{21} magnitude and phase also show larger deviations from the ideal T-line characteristics for larger lengths. Therefore, in our design of the phase shifter, we limit the phase shift obtained from a single LC π network element to be lesser than 90°. The subsequent section addresses the challenges associated with implementing a low-power beamforming RF front-end employing LC π networks as phase shifters.



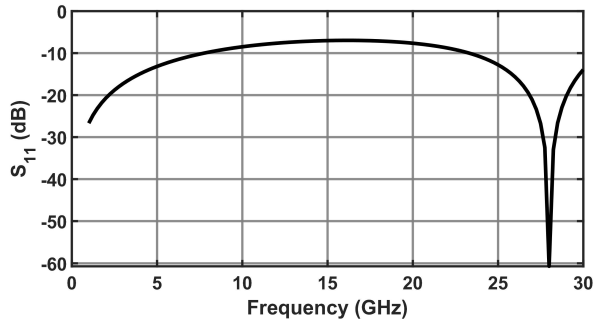
(a) $|S_{11}|$ for 90° phase shift LC π network



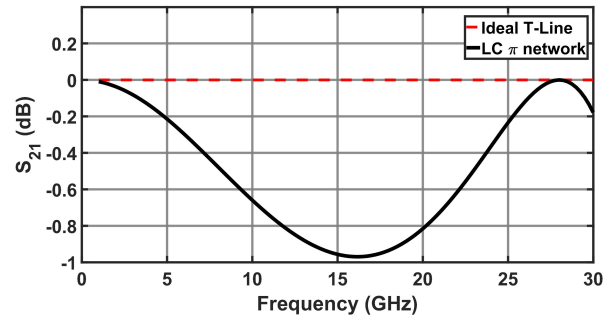
(b) $|S_{21}|$ for 90° phase shift LC π network



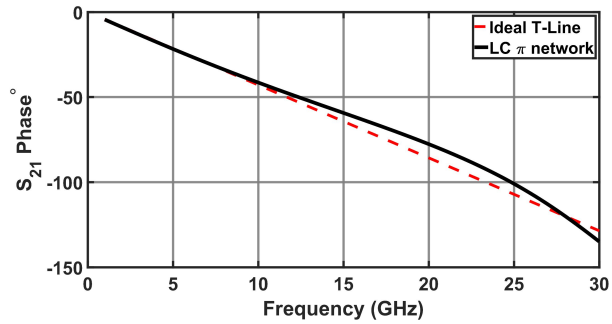
(c) $\angle S_{21}$ for 90° phase shift LC π network



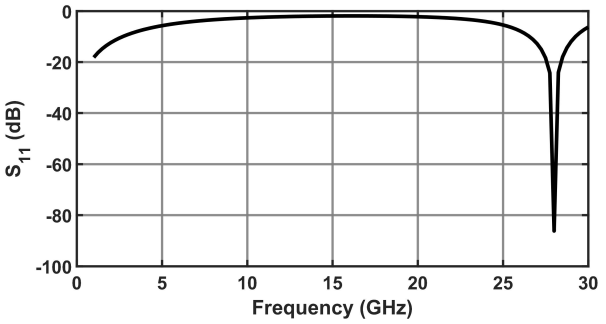
(d) $|S_{11}|$ for 120° phase shift LC π network



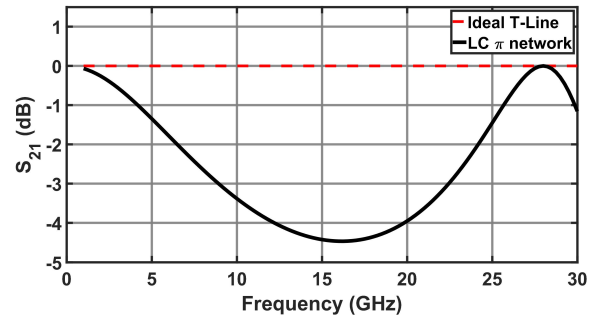
(e) $|S_{21}|$ for 120° phase shift LC π network



(f) $\angle S_{21}$ for 120° phase shift LC π network

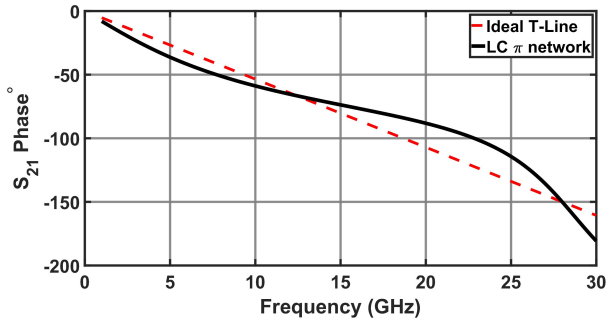


(g) $|S_{11}|$ for 150° phase shift LC π network



(h) $|S_{21}|$ for 150° phase shift LC π network

Figure 2.3: Simulated S-parameters for LC π networks



(i) $\angle S_{21}$ for 150° phase shift LC π network

Figure 2.3: Simulated S-parameters for LC π networks (continued)

The T-line, comprised of multiple LC π network elements, needs to be driven by the LNA, implying that the power consumption of the LNA depends on the characteristic impedance of the T-line. As an example, Fig. 2.4 depicts a common-source transistor behaving as a current source and driving the T-line. The T-line must exhibit a high characteristic impedance, Z_0, so that the stage achieves a reasonable voltage gain, $g_{m1}R_L = g_{m1}Z_0$, with moderate input capacitance and power consumption. The T-lines used to implement phase shifters in the literature typically have a low characteristic impedance, close to 50 Ω [15] [12]. Figure 2.5 depicts a single-stage LNA driving a T-line with 50 Ω characteristic impedance. Due to the low characteristic impedance, even with a current consumption of 4.2 mA, the gain of the LNA is only 9.1 - 8 dB.

The need to have a higher Z_0 suggests that the C per section of the T-line should be minimized. This line of thought leads to a T-line made of LC π network elements which do not have any explicit capacitances. For such a T-line [Fig. 2.6], the characteristic impedance and phase shift are determined by the parasitic capacitance of the inductor, $C_U/2$. To check the validity of this approach, we consider a single spiral drawn on metal 9 having dimensions 50 μm x 50 μm, as shown in Fig. 2.7. The spiral has an inductance of 704 pH. When used as an LC π network element to build the T-line, it possesses a high value of characteristic impedance equal to 260 Ω. However, the phase shift at 28 GHz is only 28.4°, implying that a total of seven such spirals are needed to realize a 180° phase

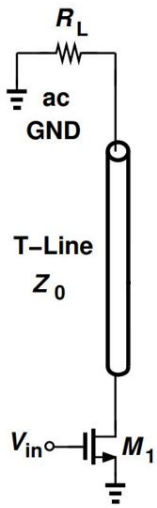


Figure 2.4: T-line driven by current source.

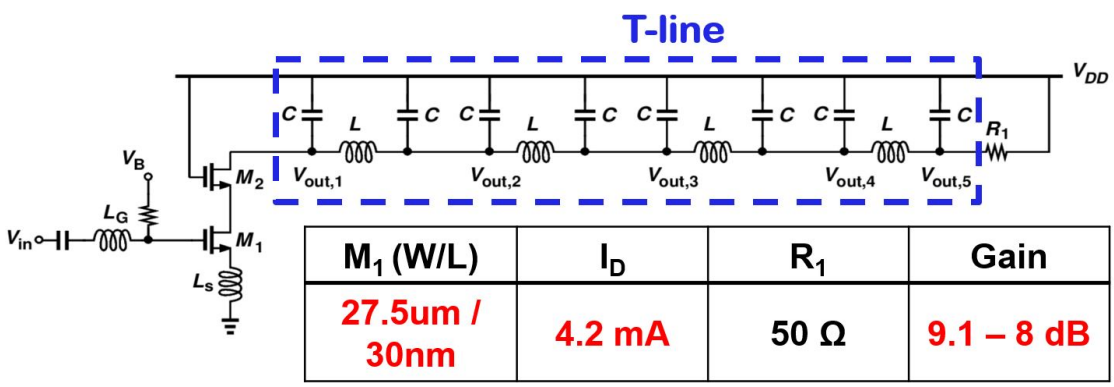


Figure 2.5: LNA driving 50 Ω characteristic impedance T-line.

shift, occupying a total area of 350 μm x 50 μm. The large area of the phase shifter is a result of removing explicit capacitors from the LC π network element. Equation 2.12 predicts that removing the explicit capacitor will reduce the phase shift provided by the LC π network element. Ideally, to make up for the reduced capacitance, we would like to increase the inductance of the spiral within the same footprint. Among various spiral inductor structures, the stacked geometry proves particularly useful in this regard as it affords an inductance increase proportional to the square of the number of layers [23]. Consequently, the phase shift, given by Eq. 2.12, also increases. In the next section, we take a closer look at stacked inductors as candidates to implement the T-line.

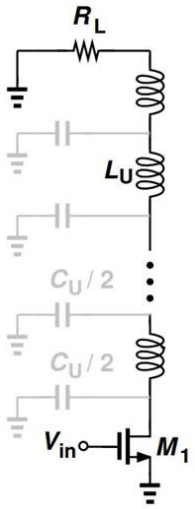


Figure 2.6: T-line made of LC π network elements without any explicit capacitances, relying on the parasitic capacitance of the inductor, $C_U/2$.

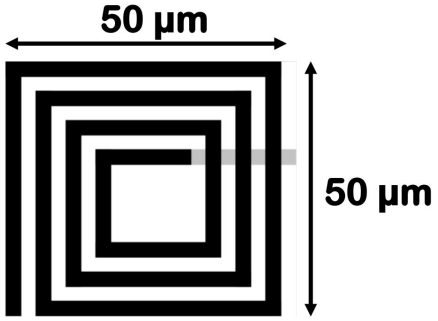


Figure 2.7: Spiral measuring 50 μm x 50 μm having L = 704 pH.

2.1.2 Stacked Inductors as LC π Network Elements

Multiple spirals can be connected in series by placing them on adjacent metal layers, as shown in Fig. 2.8. The resulting stacked inductor has a high value of inductance due to the strong magnetic coupling between the multiple spirals, as a result of which, the inductance increases proportionally to the square of the number of layers, compared to a single-layer spiral. The increased inductance suggests that stacking multiple spirals can increase the characteristic impedance of the LC π network element formed by these inductors. Additionally, the increased inductance is also likely to provide a greater amount of phase shift. To validate these advantages, an estimate of the capacitance to the substrate needs to be made for the stacked inductors. For the purpose of this analysis, the lumped model, shown in Fig. 2.9 [24], is used to represent the inductors. For the lumped model, we ignore substrate losses and trace resistance to simplify the analysis. Next, we focus on determining the C_{s1} and C_{s2} values for the stacked inductors.

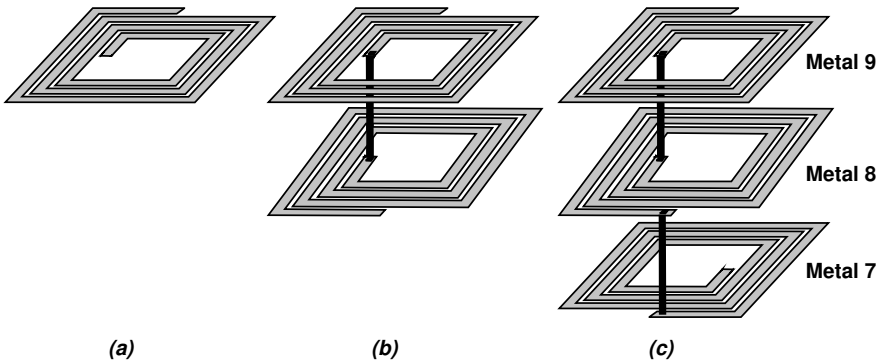


Figure 2.8: (a) Single-layer spiral, (b) two spirals stacked, and (c) three spirals stacked.

Prior work on the parasitic capacitance estimation for stacked inductors has focused on the self-resonance frequency (SRF) estimation [23]. Since the SRF calculation involves connecting one terminal of the inductor to ground, it is useful to find the value: $C_{s1} + C_{BR}$ or $C_{s2} + C_{BR}$, as shown in Fig. 2.10. These two equations are insufficient to estimate the value of the C_{s1} and C_{s2}. In the absence of any analytical method, we resort to electromagnetic (EM) simulations to estimate the substrate capacitance of stacked inductors. The procedure followed is detailed below:

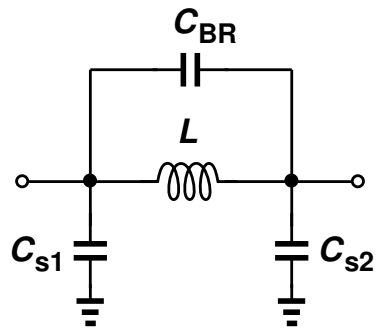


Figure 2.9: Lumped inductor model.

1. The inductance value (L) for the inductor being analyzed is obtained from EM simulations.

2. The SRF is found from simulations for the two cases depicted in Fig. 2.10(a), and Fig. 2.10(b). The SRF values together with L are used to calculate $C_{s1} + C_{BR}$, and $C_{s2} + C_{BR}$.

3. The characteristic impedance (Z_0) and the phase shift (ϕ) of the inductor, behaving as an LC π network element, is found from simulations. However, we cannot equate them to eq. 2.11 directly because i) the stacked inductor could have unequal capacitance to substrate on the two terminals ($C_{s1} \neq C_{s2}$), and ii) eq. 2.3 does not account for C_{BR}. The first issue is resolved by solving for the characteristic impedance and phase shift of an "asymmetric LC π network element". The analysis carried out in Appendix A shows that for small difference between C_{s1} and C_{s2} values (less than 20%) and the phase shift of the LC π network element less than 60°, the following value of characteristic impedance:

$$Z_0 = \sqrt{\frac{L}{(C_{s1} + C_{s2})\left(1 - \omega^2 \frac{LC_{s1}C_{s2}}{C_{s1}+C_{s2}}\right)}} \tag{2.13}$$

guarantees the return loss to be less than -20 dB. Also, the phase shift can be approximated by:

$$\phi = 2\tan^{-1}\left(\omega \cdot \frac{C_{s1} + C_{s2}}{2} \cdot Z_0\right) \tag{2.14}$$

Since, for the stacked inductors considered in this work, both the above-mentioned constraints hold as will be shown later, we can replace values of Z_0 and ϕ found from simulations in expressions eq. 2.14 to obtain the value of $C_{s1} + C_{s2}$. The effect of C_{BR} has still not been considered in the expressions given by eq. 2.13 and eq. 2.14. To include the effect of C_{BR}, we note that since C_{BR} appears in parallel with L, its effect can be captured by replacing L with $L/(1 - LC_{BR}\omega^2)$, where ω is the frequency of operation. Doing so complicates the expressions used to derive C_{s1} and C_{s2} values. Instead, we ignore the effect of C_{BR} because, for the inductors considered in this work, it has been ensured that the SRF is above 2 x frequency of operation, implying that: $L/(1 - LC_{BR}\omega^2) < 1.33L$. Consequently, the error incurred by neglecting C_{BR} is small.

4. Finally, since the values of $C_{s1} + C_{BR}$, $C_{s2} + C_{BR}$, and $C_{s1} + C_{s2}$ are known, the value of C_{s1} and C_{s2} can be solved for.

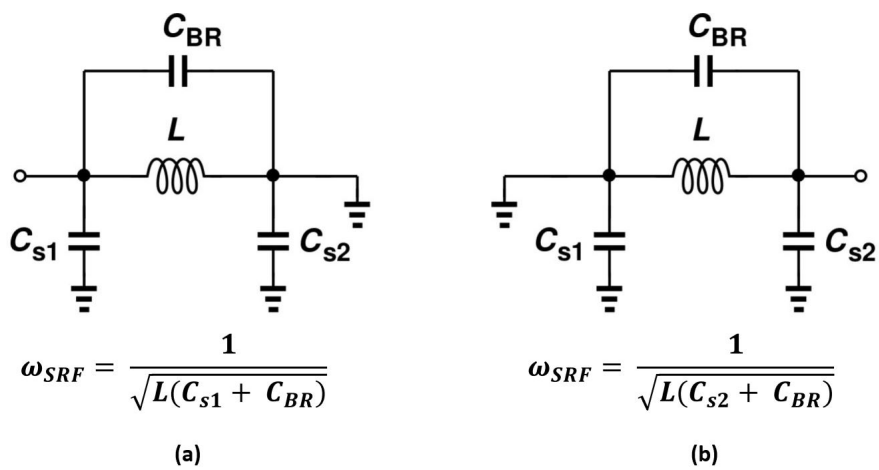


Figure 2.10: Inductor SRF values when one terminal is connected to ground.

We apply the procedure detailed above to the three cases depicted in Fig. 2.11. In each case, the inductor occupies the same footprint, measuring 20 μm x 20 μm. The first case is a single-layer spiral on metal 9. The second case consists of two stacked spirals on metal 9 and metal 8. The third case consists of three stacked spirals on metal 9, metal 8, and the third spiral is made of metal-7, metal-6, and metal-5 spirals connected in parallel. Metal-6

and metal-5 spirals are placed in parallel with the metal-7 spiral as the lower metals (metal 7, metal 6, and metal 5) have 17 times the sheet resistance of metal 9 and metal 8. The results obtained by solving the lumped model of the inductors are listed in Table 2.1. From these results we can draw the following conclusions:

1. Stacking two inductors increased the inductance by a factor of 3.3, and stacking three inductors increased the inductance by a factor of 6.7. Stacking also increases the characteristic impedance as a result.

2. The C_{BR} capacitance increases drastically for the case of stacked inductors compared to the single-layer inductor. However, the C_{s1} and C_{s2} values do not increase by a large factor. For eg. the C_{BR} capacitance for the stack-of-two inductor is almost 8 times the single-layer inductor whereas, the $(C_{s1} + C_{s2})/2$ value increases by only 1.2 times. Since the C_{s1} and C_{s2} capacitance controls the Z_0 along with the inductance, there is an increase in Z_0 with stacking.

3. Stacking also provides a greater amount of phase shift within the same footprint compared to a single-layer inductor.

4. Finally, for the two-stack and three-stack inductors, C_{s1} and C_{s2} values differ by less than 20%, which validates the use of eq. 2.14 in their calculation.

Now that the advantages of stacking for inductors functioning as LC π network elements have been established, we take a closer look at finding the optimal inductor geometry for building the T-line.

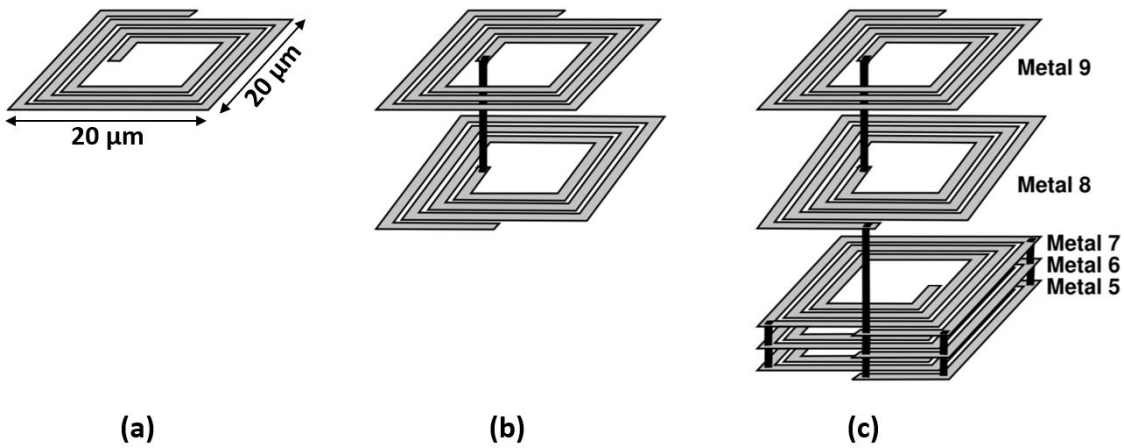


Figure 2.11: The substrate capacitance of the three cases are compared: (a) single-layer spiral, (b) two spirals stacked, (c) three spirals stacked.

	Single layer spiral **Fig. 2.11(a)**	**Two spirals stacked** **Fig. 2.11(b)**	**Three spirals stacked** **Fig. 2.11(c)**
L	116 pH	387 pH	775 pH
$\mathbf{C_{BR}}$	0.5 fF	3.9 fF	4.1 fF
$\mathbf{C_{s1}}$	1.5 fF	2.1 fF	2.3 fF
$\mathbf{C_{s2}}$	2.3 fF	2.5 fF	2.9 fF
$(\mathbf{C_{s1}} + \mathbf{C_{s2}})/\mathbf{2}$	1.9 fF	2.3 fF	2.6 fF
$\mathbf{Z_0}$	170 Ω	290 Ω	410 Ω
Phase shift	6.7°	13.5°	21°

Table 2.1: Lumped model parameters calculated for the three inductors in Fig. 2.11.

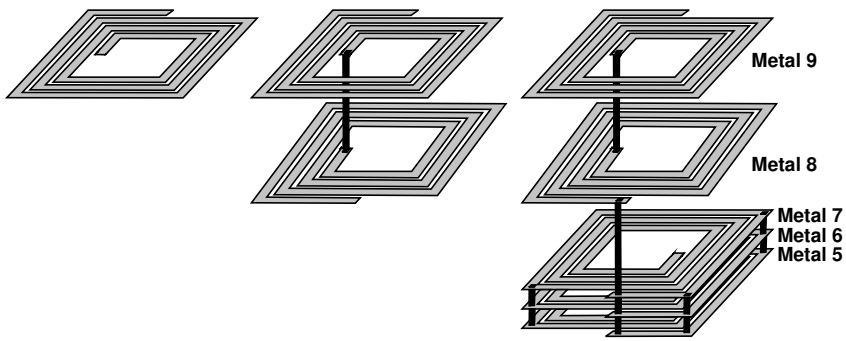
2.1.3 The Optimal Inductor to Build the T-line

The design of the unit inductor and hence the T-line is governed by four parameters: unit inductance, characteristic impedance (Z_0), loss, and total area; the last one is important because we shall use two T-lines for differential operation and 180° phase reversal. To arrive at an optimal geometry, we consider single-layer, two-stacked, and three-stacked inductors [Fig. 2.12a]. Since metal 9 and metal 8 have roughly 1/17th the sheet resistance of metal 7, we place metal-6 and metal-5 spirals in parallel with the latter for the case of the stacked inductors. Next, we iterate the length of all the three types of inductors starting from 20 μm up until the point where the SRF of the inductors drops to 30 GHz - 40 GHz. Increasing the length further, causes the Bragg's frequency of the spiral to reduce to values close to 28 GHz. Since beyond the Bragg's frequency, the inductor no longer functions as a T-line, we limit the inductor size to values for which the Bragg's frequency is sufficiently far away from the frequency of operation. To quantify the loss and area, we cascade a sufficient number of sections to obtain a 180° phase shift [Fig. 2.12b]. Simulated in Cadence's EMX at 28 GHz, these designs yield the results depicted in Fig. 2.12c and Fig. 2.12d.

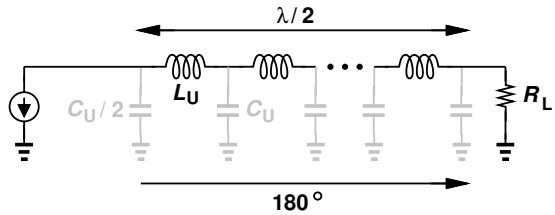
The inductance plot [Fig. 2.12c] indicates that an inductance value of around 1500 pH translates to a lateral dimension of 26 μm x 26 μm for the three-stacked inductor and a remarkably high Z_0 of 630 Ω. However, Fig. 2.12d reveals a loss of 6.9 dB. A smaller footprint for the three-stacked inductor still gives similar loss. With the two-stacked inductor, we achieve L = 1.43 nH and Z_0 = 690 Ω in a slightly larger footprint of 35 μm x 35 μm and a loss of 5.6 dB. In order to have a lower loss, we instead choose the two-stacked inductor measuring 26 μm x 26 μm, having a loss of 4.7 dB, at the cost of lower Z_0 = 390 Ω. The chosen inductor geometry is illustrated in Fig. 2.13 and the characteristics are listed in Table 2.2. The T-line area reduction, when using a two-stacked inductor, compared to a single-layer inductor is almost twofold.

Dimension	L	Z_0	Phase shift	Loss of $\lambda/2$ T-line
26 μm x 26 μm	759 pH	390 Ω	23.5°	4.7 dB

Table 2.2: Characteristic of the optimal spiral shown in Fig. 2.13.

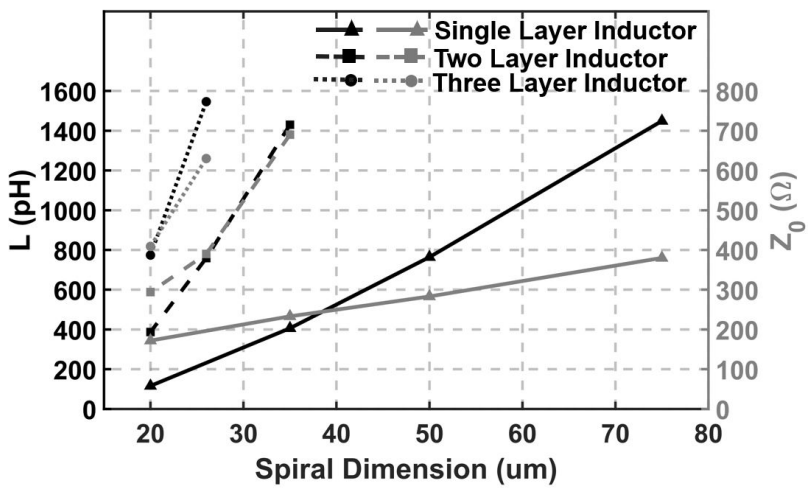


(a)

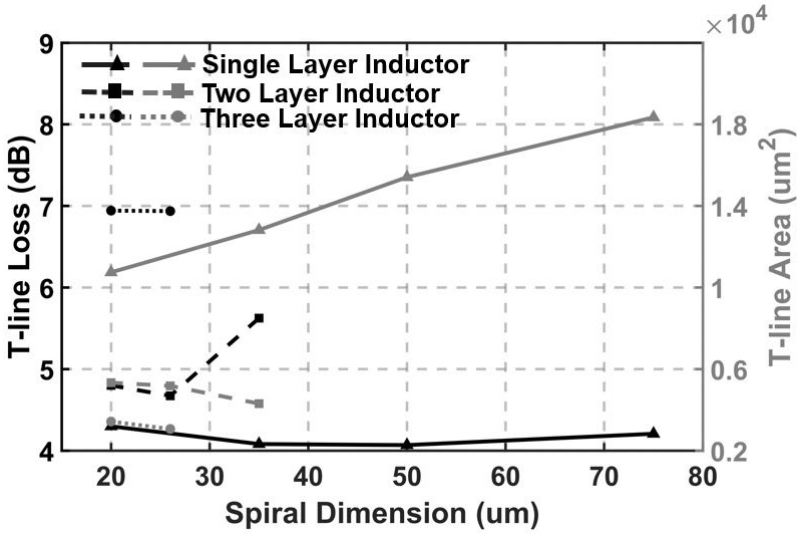


(b)

Figure 2.12: (a) The inductor geometries considered, (b) Inductors cascaded to form $\lambda/2$ T-line, (c) L and Z_0 plots, (d) Loss and area plots.



(c)



(d)

Figure 2.12: (a) The inductor geometries considered, (b) Inductors cascaded to form $\lambda/2$ T-line, (c) L and Z_0 plots, (d) Loss and area plots (continued).

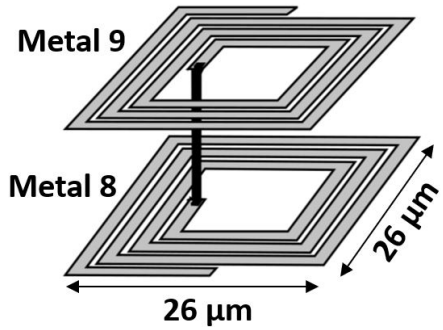
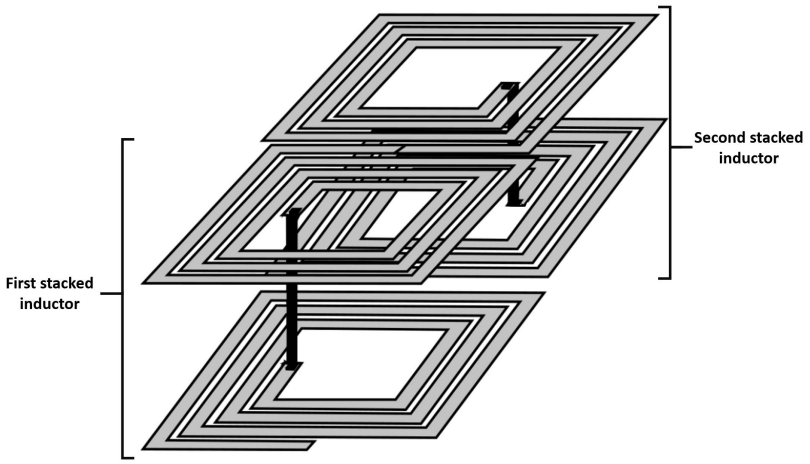


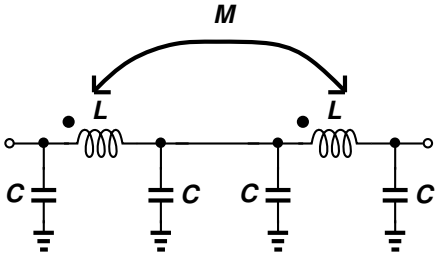
Figure 2.13: Optimal inductor geometry chosen to implement the T-line.

Having decided the optimal inductor structure to build the T-line, the next step is to determine how to connect the stacked inductors together, to form the T-line giving 180° of phase shift. From the perspective of minimizing the area of the T-line, it is desirable to place the stacked inductors as close as possible, as shown in Fig. 2.14a. Placing the inductors next to each other introduces coupling between the two, as shown in Fig. 2.14b, where the inductance of each inductor is represented by L, the mutual inductance between adjacent inductors is represented by M, and the capacitance to the substrate of each inductor is represented by C. In Appendix B we show that the coupling between the inductors, with the polarity as shown in Fig. 2.14b, results in an increase in the characteristic impedance as well as the phase shift provided by the T-line.

The complete structure of the T-line involves cascading nine stacked inductors as shown in Fig. 2.15. The resultant characteristic impedance of the T-line is 550 Ω and the phase shift at 28 GHz is 185°. The simulated S-parameters for the T-line are depicted in Fig. 2.16. The T-line loss is 7.5 dB. The loss value is higher than our prediction based on the simulations for a standalone stacked inductor (4.7 dB). Also, the characteristic impedance is higher than that of a standalone stacked inductor (390 Ω). The rise in characteristic impedance can be partially explained by the coupling between adjacent inductors. In the next section, we describe the design of the stage sensing the phase shift from the T-line.



(a) Placing two stacked inductors next to each other.



(b) LC π model of two coupled inductors

Figure 2.14: Constructing T-line by placing stacked inductors next to each other.

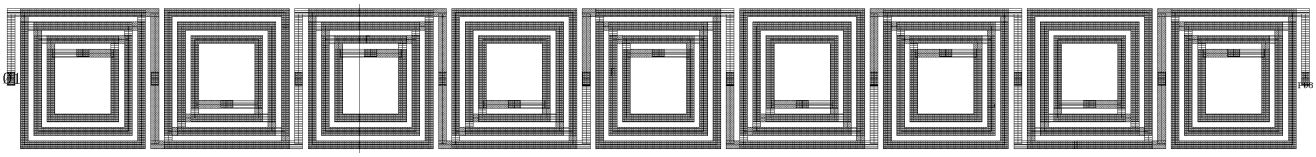
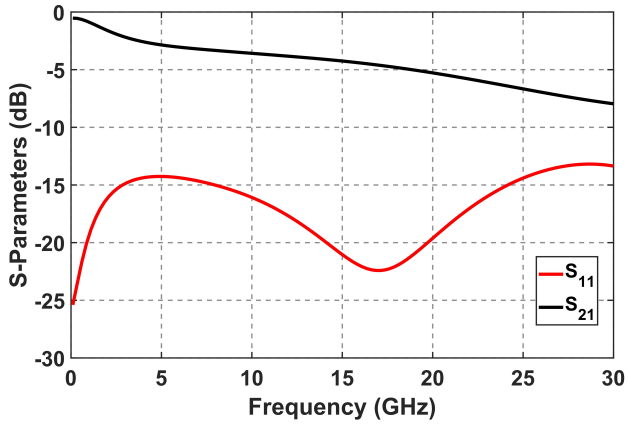
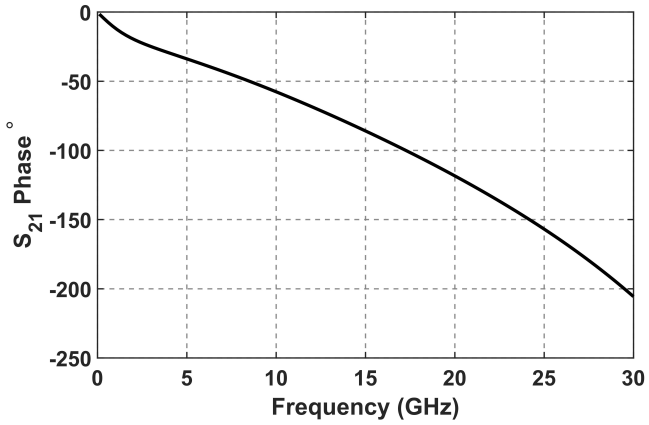


Figure 2.15: T-line made by nine stacked inductors (top view) measuring 245 μm x 26 μm.



(a) S_{11} and S_{21} magnitude results.



(b) S_{21} phase.

Figure 2.16: Simulated S-parameter results of the T-line.

2.1.4 Sensing Phase Shift from the T-line

Section 1.3.2 provides a summary of the previously reported approaches to derive phase shift from T-line and the associated challenges. While phase shifters made from actual T-lines afford a fine phase shift resolution, they have the drawbacks of having low characteristic impedance value, and large length of the T-line [13] [20]. The phase shifters made from LC π section T-lines have an undesirable trade-off between the characteristic impedance and the phase shift resolution [15] [14] in addition to having a low value of characteristic impedance. While the T-line design described in the previous section addresses the issue of low characteristic impedance and large area consumption, the challenge of achieving high phase resolution still remains to be addressed.

We follow the approach of tapping phase shifted points from the T-line, described in [14] to extract phase shift. However, in [14] each LC π network element is considered as a unit phase shift element, and the phase shift is tapped only at the endpoints of the inductor. We propose two new ideas to obtain higher phase shift resolution. We would ideally like to view the artificial T-line made of discrete inductors as an actual T-line that can be tapped at any desired phase as shown in Fig. 2.17.

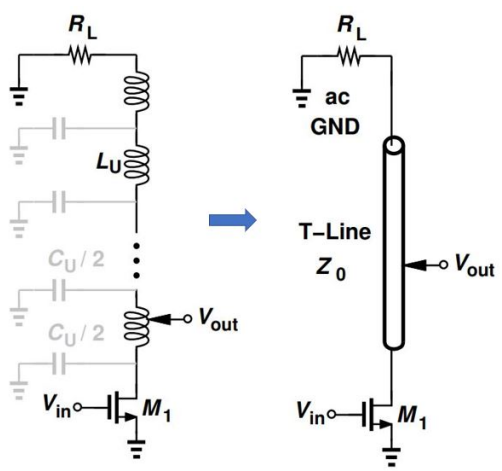


Figure 2.17: Tapping T-line made from inductors at arbitrary points like an actual T-line.

For the stacked inductors used in the design of the T-line, the above premise necessitates tapping any point within the inductor to obtain arbitrarily high phase shift resolution as

shown in Fig. 2.18. To check the efficacy of this approach, we take a stacked inductor and tap it at nine uniformly spaced points along the inductor [Fig. 2.19a], one at a time, using an NMOS transistor ($W/L = 4\ \mu$m/30 nm) in common-source configuration. Due to the additional capacitance introduced by the transistor, the Z_0 of the inductor drops from 390 Ω to 317 Ω. Regardless of the tap to which the transistor is connected, the S_{11} of the inductor remains below -22 dB as shown in Fig. 2.19b. Figure 2.19c depicts the phase shift profile for the different tap points and shows that the phase shift across the different tap points is almost uniform.

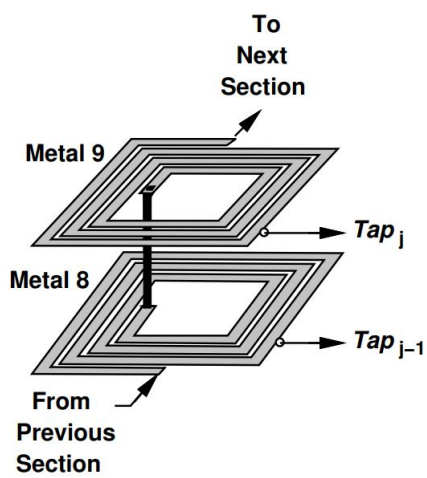
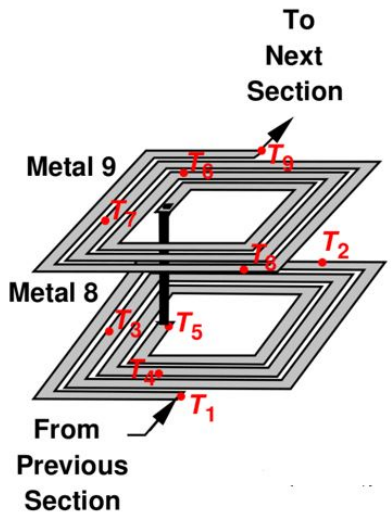
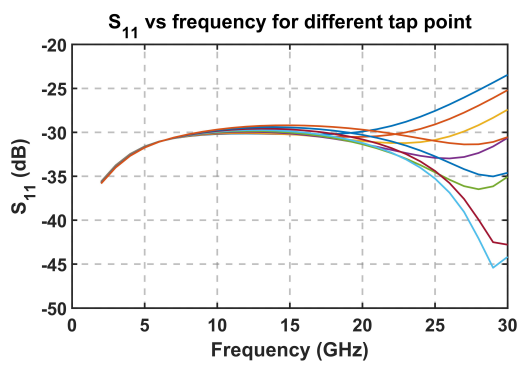


Figure 2.18: Tapping points *within* the inductor.

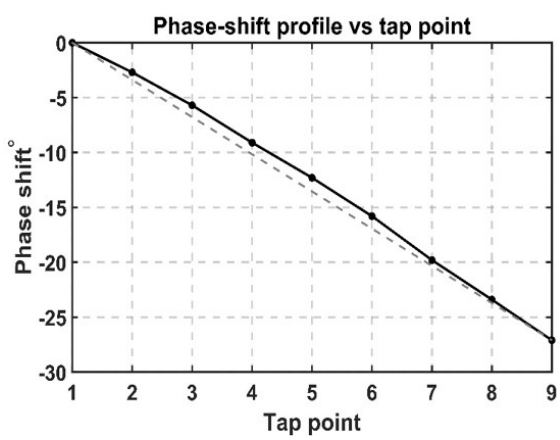
Next, we construct the T-line by connecting five stacked inductors with 21 uniformly spaced taps placed along the T-line as depicted in Fig. 2.20a. Each tap point is connected to a G_m stage consisting of common-source transistor M_j that can be turned on or off by means of a source switch S_j. The total phase shift given by the T-line is 226° at 28 GHz. The Z_0 of the T-line drops from 550 Ω in the untapped condition, to 210 Ω. Also, the phase shift provided by per inductor increases as can be seen by the reduction in the number of inductors required to build the T-line. The reason for the drop in Z_0 and increase in phase shift is the extra capacitance introduced between the T-line and the ground due to the gate capacitance C_G of the G_m stages as depicted in Fig. 2.20b. Since the output of all the G_m stages are shorted, the capacitive loading at the output, denoted by C_A, is large (= 100 fF), leading to low gain which is another drawback of having a large number of taps.



(a) Tapping nine uniformly spaced points *within* the inductor.

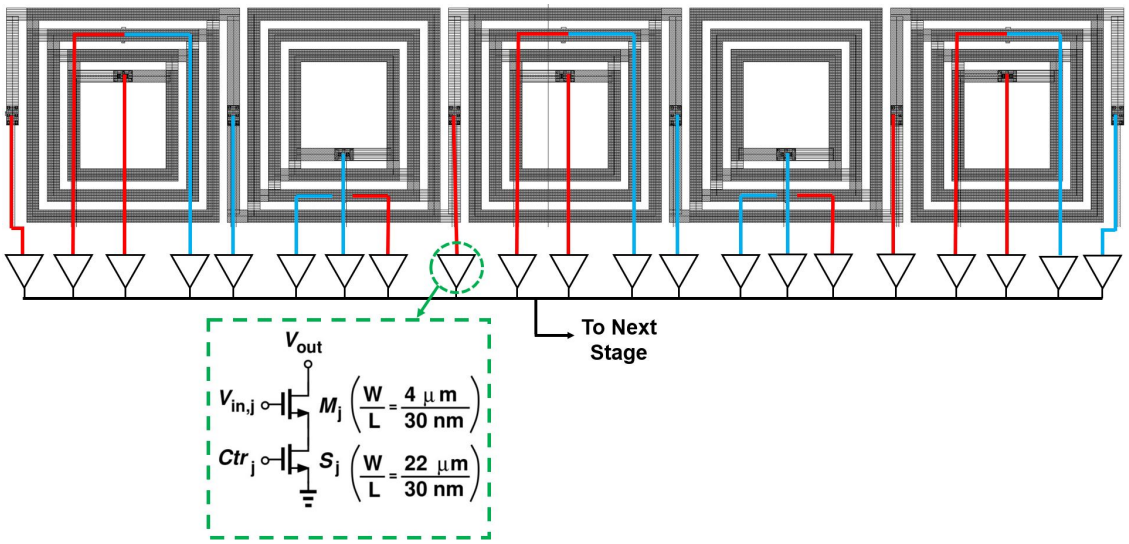


(b) S_{11} for common-source transistor connected to the different tap points.

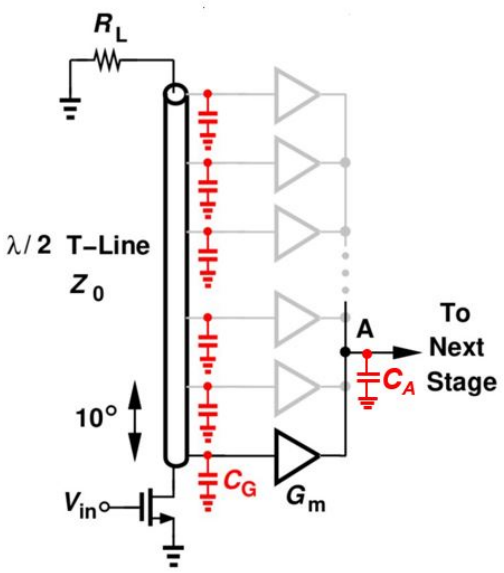


(c) phase shift profile vs tap points.

Figure 2.19: Tapping uniformly spaced points *within* the inductor.



(a) Tapping T-line with 21 G_m stages (red and blue connections represent tap points on Metal 9 and Metal 8, respectively).



(b) G_m stages tapping the T-line introduce C_G.

Figure 2.20: Tapping T-line with 21 G_m stages to get a 10° phase resolution.

To address the two issues identified above, we propose employing phase interpolation technique. The principle of phase interpolation is to take two phase shifted signals from the T-line and then interpolate them to get an intermediate phase shift value. The interpolation happens by scaling the two outputs before combining them. For instance, Fig. 2.21 depicts two unit magnitude phasors X and Y that are separated by 40° phase. After applying the appropriate weights α and β to the two vectors, they are combined. The interpolated phase, ϕ, as a function of the weights α and β, and the phase between X and Y, θ, is expressed as:

$$\phi = \tan^{-1}\left(\frac{\beta \sin\theta}{\beta \cos\theta + \alpha}\right) \tag{2.15}$$

The magnitude of the resultant phase, $|\alpha\mathrm{X} + \beta\mathrm{Y}|$ is expressed by:

$$|\alpha X + \beta Y| = \sqrt{\alpha^2 + \beta^2 + 2\alpha\beta\cos\theta} \tag{2.16}$$

If $\theta \ll 1$ radian, we can approximate θ by:

$$\phi \approx \tan^{-1}\left(\frac{\beta\theta}{\beta + \alpha}\right) \tag{2.17}$$

$$\approx \frac{\beta\theta}{\beta + \alpha} \tag{2.18}$$

Similarly, the magnitude of the resultant phasor can be approximated by:

$$|\alpha X + \beta Y| \approx \alpha + \beta \tag{2.19}$$

While $\theta = 40°$ for the two phasors on the T-line which are going to be interpolated and the condition $\theta \ll 1$ radian does not hold true, we still would like to use the eq. 2.18 to obtain an interpolated phase resolution of 5°. By doing so, we incur errors, both on the magnitude and phase of the resultant phasor, which are recorded in Table 2.3. These errors are very small: the maximum magnitude error is -0.5 dB and the maximum error in the interpolated phase is 0.3°. So, a nine-level resolution for the weights α and β is sufficient to realize a phase resolution of $\theta/8$ i.e. 5°.

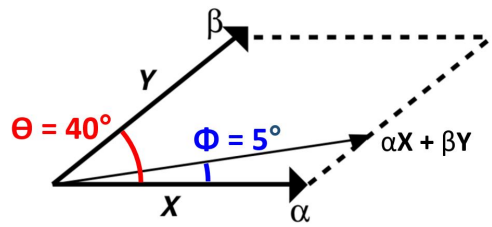


Figure 2.21: Principle of phase interpolation.

α	β	$\tan^{-1}\left(\frac{\beta \sin\theta}{\beta\cos\theta+\alpha}\right)$	$\frac{\beta\theta}{\beta+\alpha}$	$\lvert\alpha X + \beta Y\rvert$
0	1	40°	40°	1
0.125	0.875	35.3°	35°	0.97
0.25	0.75	30.3°	30°	0.96
0.375	0.625	25.2°	25°	0.94
0.5	0.5	20°	20°	0.94
0.625	0.375	14.8°	15°	0.94
0.75	0.25	9.7°	10°	0.96
0.875	0.125	4.7°	5°	0.97
1	0	0°	0°	1

Table 2.3: Error incurred in phase interpolation by using Eq. 2.18 and Eq. 2.19.

To implement phase interpolation, we tap the T-line at 40° phase shift intervals with G_m stages that have been segmented into eight sections, to implement the weighting factors α and β [Fig. 2.22]. The total number of taps on the T-line reduce to six which results in a Z_0 of 350 Ω and the total capacitance at node A, denoted by C_A, is now only 30 fF. Due to lesser phase shift per inductor, the T-line now consists of eight inductors.

The phase shifter design, depicted in Fig. 2.23a, now has six uniformly spaced taps along the T-line. The G_m stage tapping these points has a gate-to-drain capacitance of 1.4 fF, both in the on and off states. The capacitance between the gate and ground, which is a sum of the C_{gb} and C_{gs} component is 2.2 fF in the off state and rises to 3 fF when the G_m

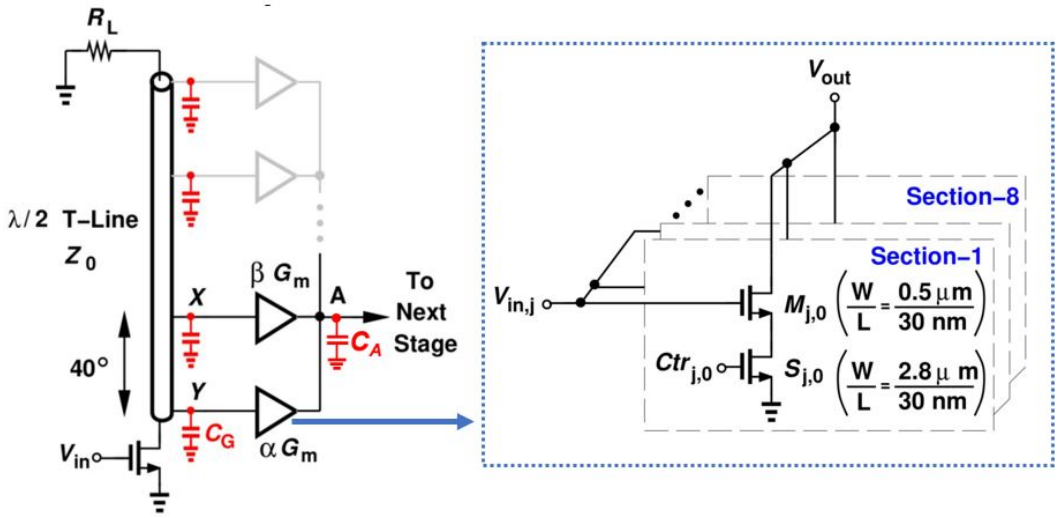
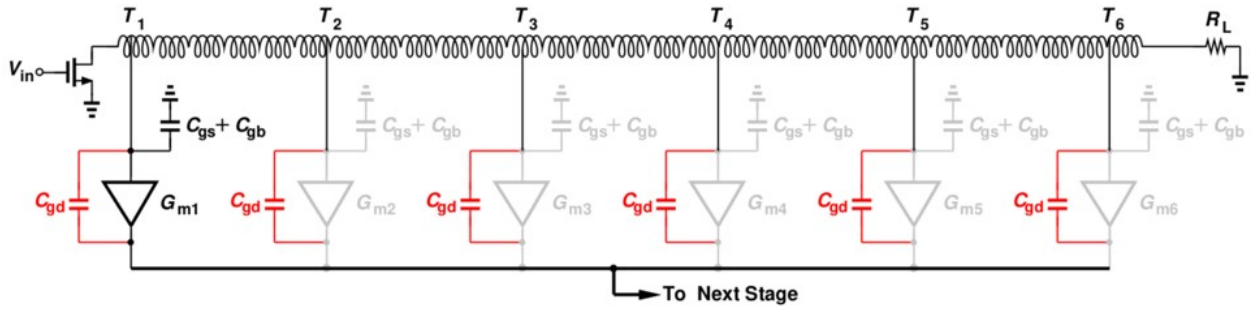
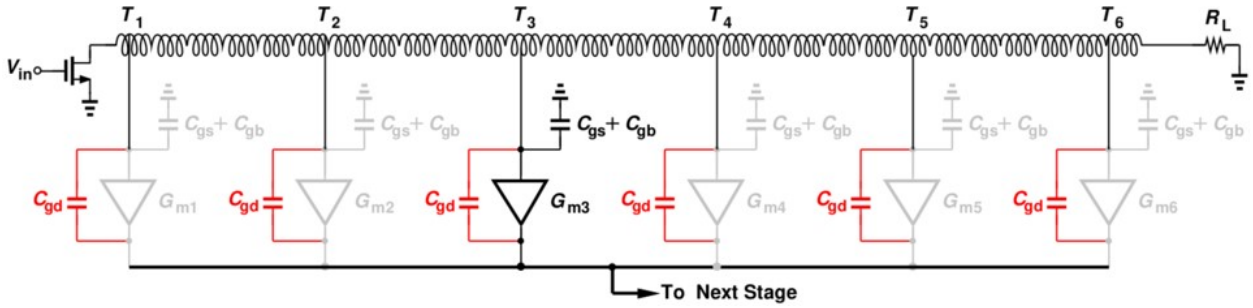


Figure 2.22: Phase interpolation by a factor of 8 to obtain a phase resolution of 5°.

stage is turned fully on. Both these capacitive components, C_{gd} and C_{gb}+C_{gs}, play a role in creating phase shift non-uniformity. The C_{gd} of the off-state G_m stages provides a capacitive feedthrough path that causes the output phase characteristics to differ from the phase characteristics of the tapped points T_1, T_2, till T_6. To understand the effect which the C_{gb}+C_{gs} component has, we consider two scenarios, one in which the tap point T_1 is active [Fig. 2.23a] and the other in which the tap point T_3 is active [Fig. 2.23b]. In the two scenarios, the capacitive loading on the T-line changes which causes non-uniformity in phase shift. Another mechanism contributing to the phase shift non-uniformity is the magnetic and capacitive coupling between the output trace and the T-line as both are physically near each other and span a distance of around 200 μm. Due to the above three factors, the phase shift characteristics, shown in Fig. 2.24a, display considerable non-uniformity. The INL plot [Fig. 2.24b] show larger than 2 LSB INL.

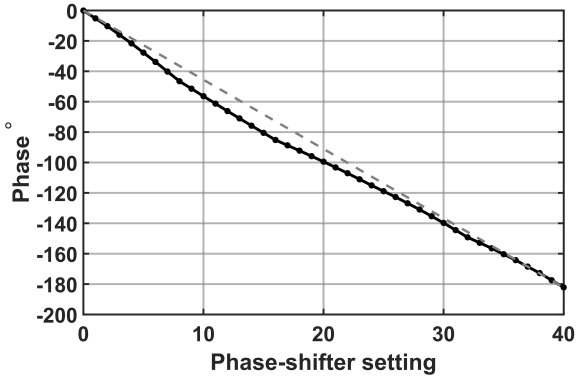


(a) T_1 tap point active.

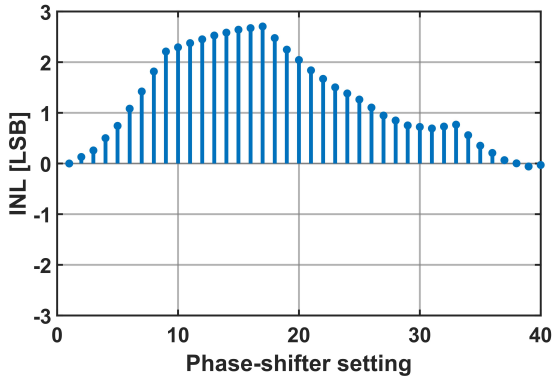


(b) T_3 tap point active.

Figure 2.23: Phase non-uniformity mechanisms.



(a) phase shift characteristics.



(b) INL plot for the phase shift characteristics.

Figure 2.24: Non-uniformity in phase shift characteristics.

To correct for the errors in the phase shift, a special property of the T-line can be used. Theoretically, a T-line can provide any arbitrary amount of phase shift. This allows for appropriate "predistortion" of the tap points on the T-line. The process is carried out by observing the output phase characteristics and then moving the tap points on the T-line to correct for the errors in the phase shift characteristics as shown in Fig. 2.25. The new simulated phase shift characteristics, shown in Fig. 2.26a, have a full-scale phase shift of 204.7° over 41 codes and display an INL of less than 0.5 LSB as depicted in Fig. 2.26b. The normalized gain for different phase shifter settings is also shown in Fig. 2.27b and merits an important remark. When compared to the loss across the different T-line tap points, shown in Fig. 2.27a, the gain profile at the output of the G_m stages shows different behaviour. For instance, the loss at the end of the T-line, which corresponds to the sixth tap point, is 5.4 dB, whereas, at the output of the G_m stages, the gain drops by only 1.3 dB relative to the phase shifter setting at which the first tap point is active. This suggests that the mechanisms identified earlier which caused phase non-uniformity, result in an advantage in terms of the gain, as the loss across the T-line doesn't get manifested to the same degree when looking at the output of the G_m stages.

To check for the variability of the phase shift characteristics with process variations, which will cause variations in the termination resistor of 350 Ω, we compare the simulated phase shift characteristics for the TT, SS, and FF corners in Fig. 2.28. The load resistor values in the TT, SS, and FF corners are 350 Ω, 397 Ω, and 303 Ω. The maximum variation across different phase shifter settings is 7.5°.

Signal Combining and Additional 180° phase swap:

In the signal path, after the phase shifter applies the appropriate phase shift to the signals of every element, the signals from multiple elements can be combined. However, since the T-line provides a phase shift range of 180°, an additional 180° phase shift is needed before the signal combining to cover the entire 360° range. To this end, we implement a differential structure for the phase shifter that includes differential T-lines. Next, we add cascode devices at the drain terminals of the G_m stages as shown in Fig. 2.29. These

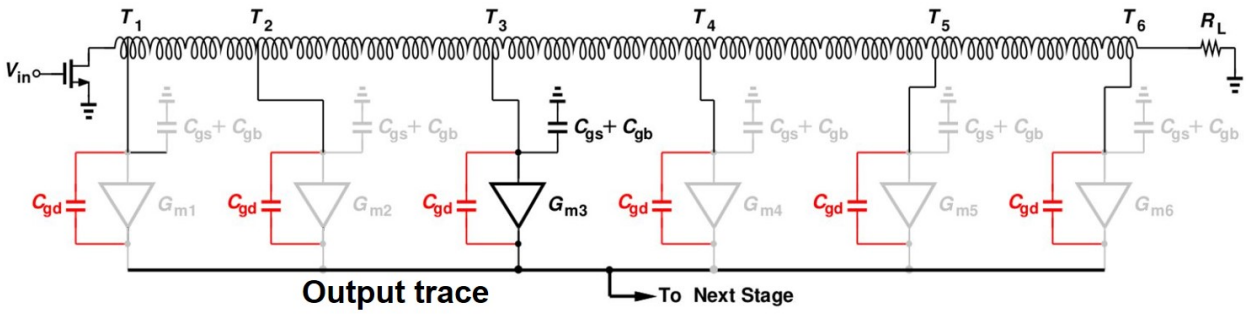
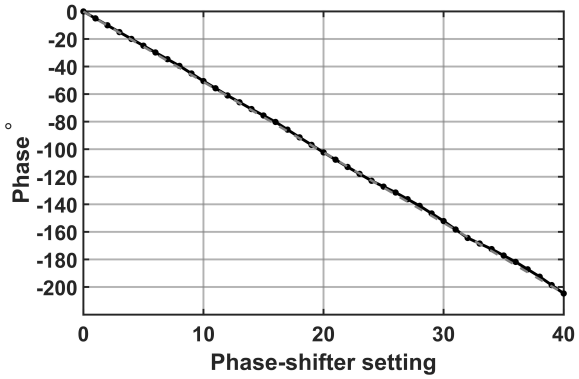
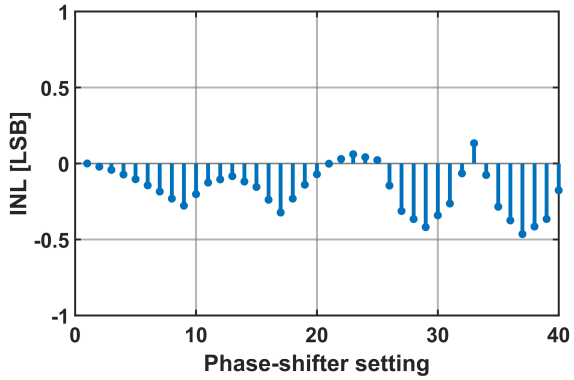


Figure 2.25: Predistortion of tap points to correct phase non-uniformity.

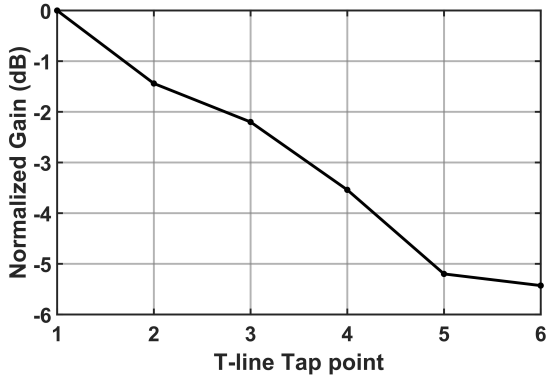


(a) phase shift characteristics.

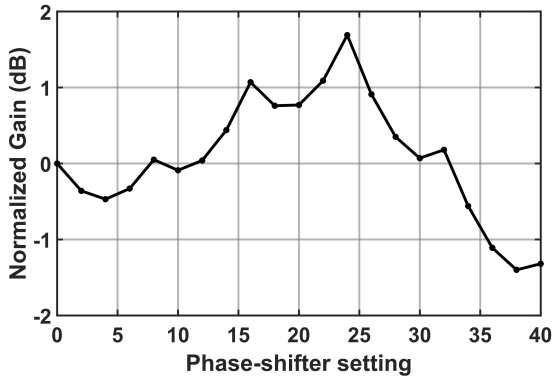


(b) INL plot for the phase shift characteristics.

Figure 2.26: Predistortion results in uniformity in phase shift characteristics.



(a) Loss across different T-line tapping points.



(b) Normalized gain at the output of G_m stages for different phase shift settings.

Figure 2.27: Gain characteristics across T-line tap points and at the output of G_m stages.

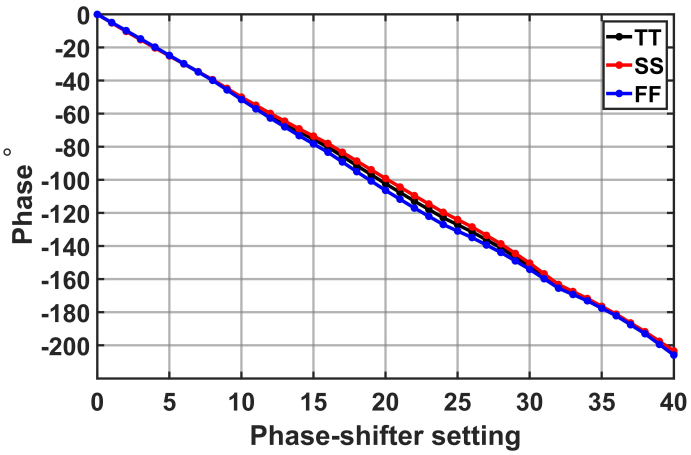


Figure 2.28: Variation in the phase shift characteristics across different corners.

cascode devices can implement a 180° phase swap under the command of the V_1 signal. The differential outputs of the cascode devices are connected to the combining network that consists of a differential load inductor. The load inductor is responsible to resonate with the capacitance introduced by the long traces carrying the output current of the different elements along with the input capacitance of the next stage. We combine the outputs of four elements at a time. The cascode devices also improve the isolation amongst multiple elements. The floor plan of the phase shifter of four elements consisting of differential T-lines along with the combining traces and the load inductor at the output of the combining network is shown in Fig. 2.30.

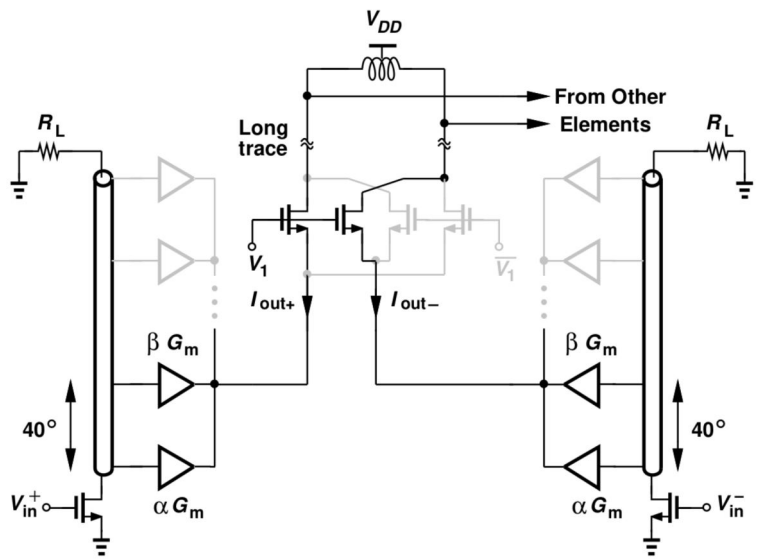


Figure 2.29: Cascode devices (W/L = 4 μm/30 nm) for 180° phase swap.

The next stage in the signal path is the mixer. A double-balanced passive mixer emerges as the natural choice to be connected to the combined output of the four elements. An active mixer is ruled out owing to the headroom required to place the additional switching transistor and load resistors. Before moving to the design details of the mixer, we model the phase shifter G_m stage along with the cascode transistors, and the capacitance contributed by the combining traces of the four elements as the small-signal Thevenin equivalent. Since we want to capture the single-element gain and NF, while finding the Thevenin equivalent, the G_m stage of only one of the elements is kept on while the other

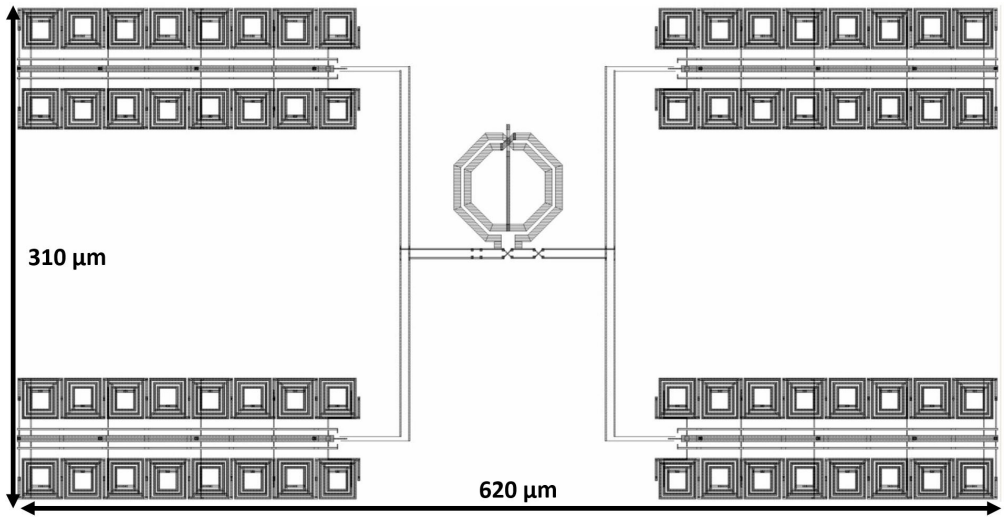


Figure 2.30: Floor plan of phase shifters of four elements along with the combining network.

three elements are off. The half-circuit Thevenin equivalent is shown in Fig. 2.31. The next section describes the mixer design in detail.

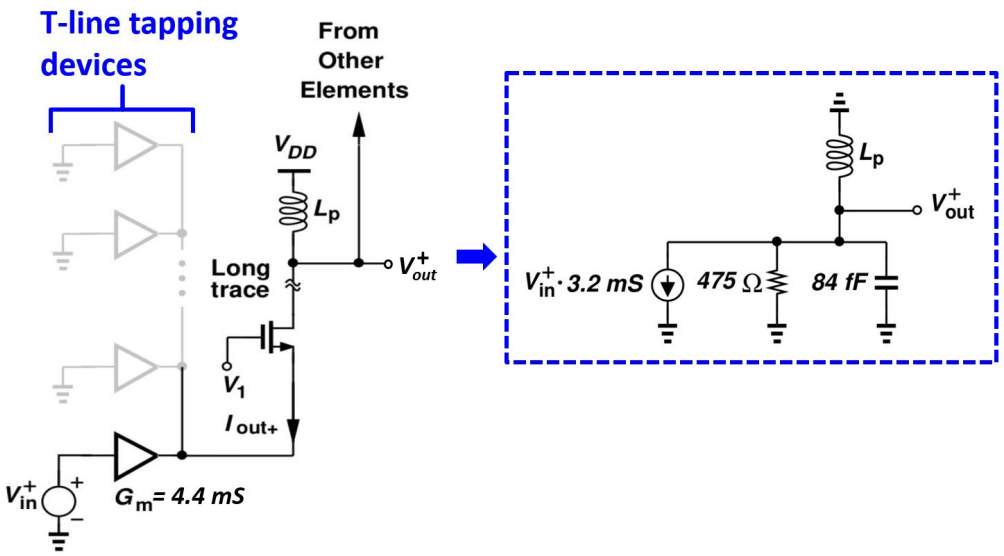


Figure 2.31: Half-circuit Thevenin equivalent of the phase shifter and the combining network.

2.2 Mixer

The considerations leading to the choice of a passive mixer over an active mixer were described in the previous section. There are two choices further to be made with regard to the passive mixer architecture. The first is the choice of duty cycle. It is well known that passive mixers driven by 25% duty-cycle LO give better performance in terms of I and Q channel isolation, gain, and NF [25] [26]. However, due to the fanout-1-rise-time of CMOS logic gates being limited to around 8 ps, it is not possible to generate rail-to-rail 25% duty-cycle LO waveforms so we instead generate 50% duty-cycle LO. The second choice to be made is whether to choose a purely capacitive load at the baseband or a low-impedance resistive load. The advantage of using a low-impedance resistive load is that the mixer transistors' contribution to noise and nonlinearity reduces [25]. However, this is under the assumption that the resistance of the mixer transistors in the on-state is much lower than the impedance of the current source driving the mixer. To ensure that this condition is met, the width of the mixer transistors required is quite large which further presents certain issues. For instance, a transistor having W/L = 8.8 μm/30 nm, has an on resistance of around 50 Ω, which is about nine times lower than the current source impedance shown in Fig. 2.31. However, the same transistor has an estimated gate-to-source capacitance of 4.8 fF and a total gate capacitance of 9.7 fF. The gate-to-source capacitance of four mixer transistors loads the input of the mixer, thereby degrading the performance. The total gate capacitance requires significant power in the LO distribution network to obtain rail-to-rail swings. These two issues limit the advantages realized by opting for a low-impedance resistive load. We instead choose a capacitive load at the baseband and describe its design process next.

2.2.1 Passive Mixer Design Optimization

The general model for a 50% duty-cycle-driven-quadrature-passive mixer is shown in Fig. 2.32. The analysis of the mixer for a resistive load at baseband is done in [27]. We adopt a

similar analysis for a capacitive baseband load.

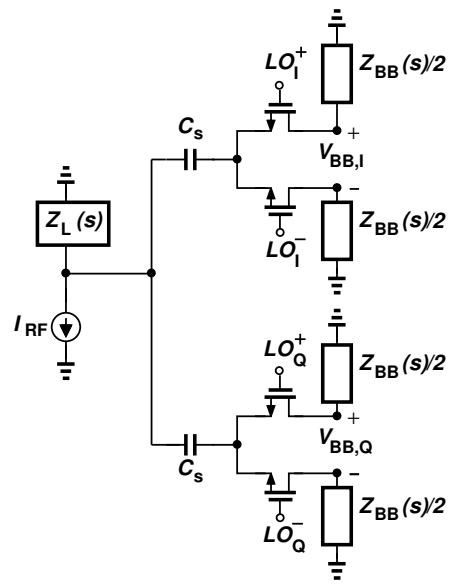


Figure 2.32: Passive mixer model.

The RF current source at the input excites the mixer at a frequency $\omega_{LO} + \omega_m$, where ω_m represents the baseband frequency of interest at which, the output voltage is calculated. The expression for the gain is as follows:

$$\frac{V_{BB,I}(\omega_m)}{I_{RF}(\omega_{LO}+\omega_m)} = -\frac{1}{\pi}\cdot\frac{Z_L(\omega_{LO}+\omega_m)[Z_C^*(\omega_{LO}-\omega_m)+R_{SW}]\cdot Z_{BB}(\omega_m)}{[2Z_L(\omega_{LO}+\omega_m)+Z_C(\omega_{LO}+\omega_m)+R_{SW}+\frac{1}{\pi^2}Z_{BB}(\omega_m)][Z_C^*(\omega_{LO}-\omega_m)+R_{SW}+\frac{1}{\pi^2}Z_{BB}(\omega_m)]-[\frac{1}{\pi^2}Z_{BB}(\omega_m)]^2} \tag{2.20}$$

where $Z_C(\omega)$ denotes the impedance of the capacitor C_S, and R_{SW} represents the on-state resistance of the mixer transistors. The multiplication of the phasor frequencies by j has been omitted for brevity. The above expression can be simplified by assuming $Z_L(\omega_{LO}+\omega_m)$ to be constant over the channel bandwidth and equal to $Z_L(\omega_{LO})$. A similar assumption is made for $Z_C(\omega_{LO}+\omega_m)$ as well. With these assumptions, the gain is simplified to the following expression:

$$\frac{V_{BB,I}(\omega_m)}{I_{RF}(\omega_{LO}+\omega_m)} = -\frac{1}{\pi}\cdot\frac{Z_L(\omega_{LO})[-Z_C(\omega_{LO})+R_{SW}]\cdot Z_{BB}(\omega_m)}{[2Z_L(\omega_{LO})+Z_C(\omega_{LO})+R_{SW}][-Z_C(\omega_{LO})+R_{SW}]+\frac{2}{\pi^2}[Z_L(\omega_{LO})+R_{SW}]\cdot Z_{BB}(\omega_m)} \tag{2.21}$$

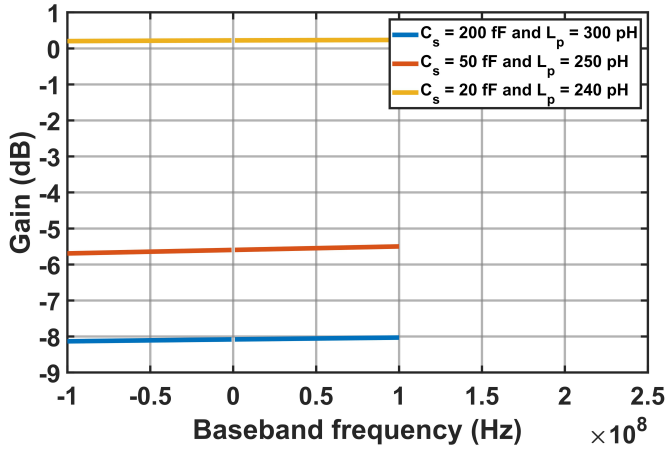


Figure 2.33: Gain vs baseband frequency based on expression 2.21 for different C_S and L_P values.

To derive design guidelines and decide on the optimum values of R_{SW}, $Z_L(s)$, and $Z_{BB}(s)$ for obtaining maximum gain, we plot the gain expression for different cases.

From the simulations done on the T-line tapping G_m stages and the subsequent signal combining traces, we know the effective G_m and the output impedance driving the mixer [Fig. 2.34]. Firstly, to capture the effect of C_S, we fix the values of $R_{SW} = 95\ \Omega$ and $C_{BB} = 60$ fF, and iterate for $C_S = 200$ fF, 50 fF, and 10 fF. For each case, the optimum value of L_P to get maximum gain is found. The resulting gain vs baseband frequency ($2\pi\omega_m$) for the three cases is plotted in Fig. 2.35. These plots clearly suggest that a smaller value of C_S gives a higher gain, for the particular source impedance shown in Fig. 2.34.

To verify the results obtained from the gain expression 2.21, we simulate the mixer using Cadence's PSS/PAC analysis. The switches are replaced by NMOS switches that are sized to give the desired on resistance. These switches are driven by realistic LO waveforms having 4-ps rise and fall time. Once again we iterate for $C_S = 200$ fF, 50 fF, and 10 fF. For each case, the optimum value of L_P to get maximum gain is found. The resulting gain vs baseband frequency for the three cases is plotted in Fig. 2.36.

From these plots, we conclude that while a smaller value of C_S improves gain, the predictions made by expression 2.21 are optimistic. For instance, the gain predicted for $C_S = 200$ fF by the gain expression is -8.1 dB whereas, the simulated value is -9.8 dB. The discrepancy between the

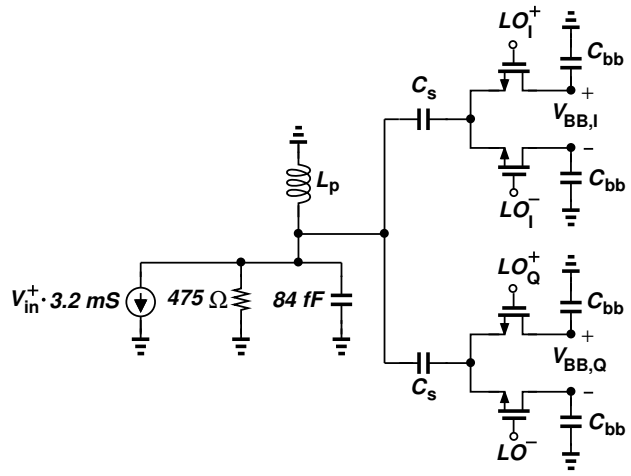


Figure 2.34: Effective G_m and source impedance driving the mixer.

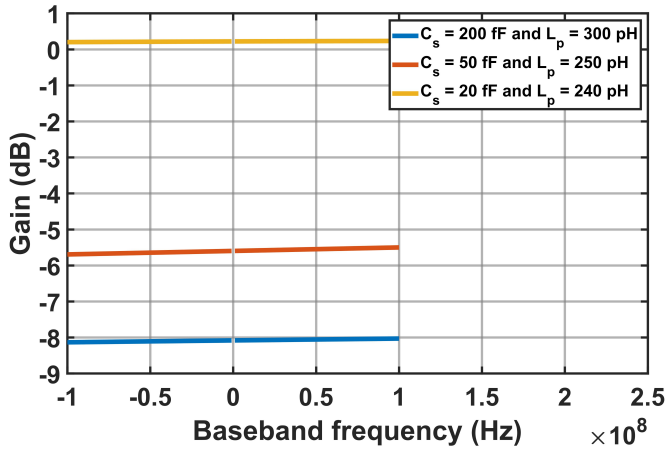


Figure 2.35: Gain vs baseband frequency based on expression 2.21 for different C_S and L_P values.

two values is likely caused by the non-ideal LO waveforms used in the simulations. It must be noted that the optimum value of L_P for the above case, predicted by the gain expression is 300 pH whereas simulations predict an optimum value of 230 pH. The reason for this discrepancy is the capacitance of the switch devices (measuring 4.4 μm in width and 30 nm in length) which has not been included in the gain expression. We fix the value of C_S to be 50 fF and proceed with the rest of the optimization for C_{BB} and R_{SW} values.

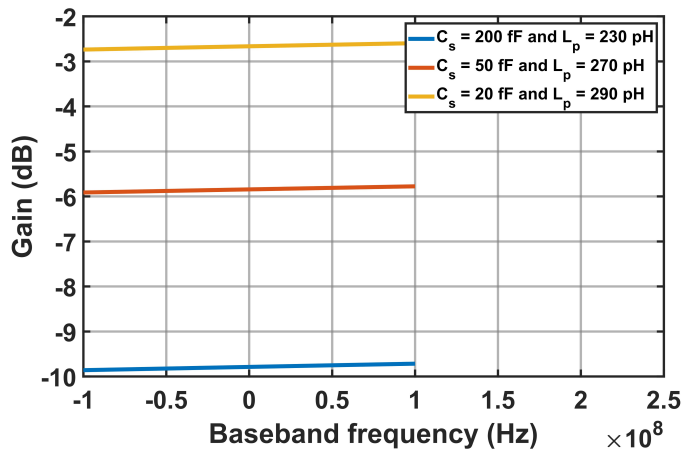


Figure 2.36: Gain vs baseband frequency based on SPICE simulations for different C_S and L_P values.

We iterate for C_{BB} = 60 fF, 120 fF, 240 fF, 480 fF, 1pF, 2 pF, and 4 pF. Again, for each case, the optimum value L_P for maximum gain and the correct center frequency is found using the gain expression. The resulting gain vs baseband frequency for the three cases is plotted in Fig. 2.37. The same iteration is carried out in SPICE simulations and the results are depicted in Fig. 2.38. It can be observed that the gain is a strong function of C_{BB}, especially for C_{BB} lesser than 480 fF. We fix C_{BB} to be 60 fF as a compromise between large gain and small clock-feedthrough from the switches.

Next we iterate for R_{SW} = 48 Ω, 95 Ω, and 190 Ω. The results for the gain expressions are plotted in Fig. 2.39. For all three cases, the optimum L_P is 250 pH. The results suggest that the gain changes negligibly for different R_{SW} values. The same iteration is carried out using SPICE simulations and the results are depicted in Fig. 2.40.

Before deciding on the optimal value of R_{SW}, the noise added by the switches also needs to be

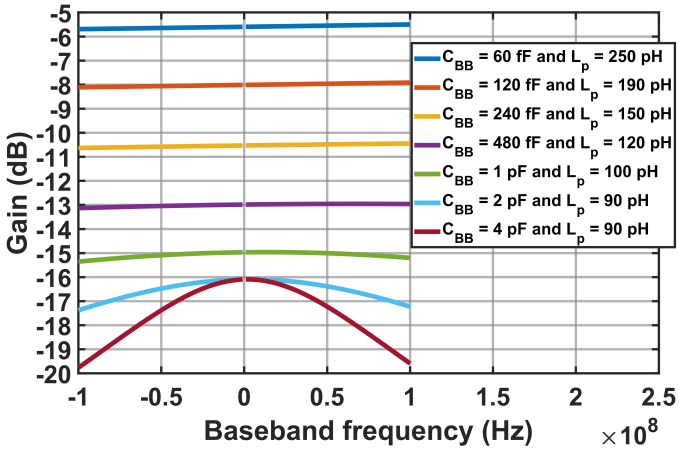


Figure 2.37: Gain vs baseband frequency based on expression 2.21 for different C_{BB} and L_P values.

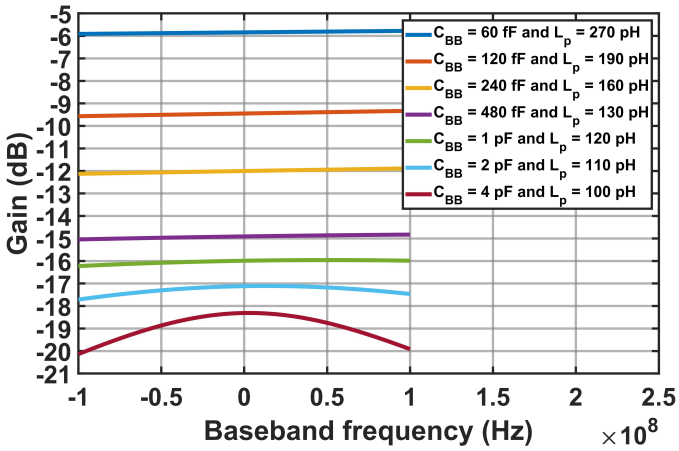


Figure 2.38: Gain vs baseband frequency based on SPICE simulations for different C_{BB} and L_P values.

considered. Intuitively, a larger R_{SW} should add more noise, however, to account for the effect of the switch capacitance, simulations are performed where only the effect of the switch noise is considered, and the transconductance at the input of the mixer [Fig. 2.34] is driven by a 50 Ω source. The resultant NF of the mixer for different values of C_S, C_{BB}, L_P, and R_{SW} considered in the preceding analysis are listed in Table 2.4. From the simulated NF results, we conclude that smaller values of C_S and C_{BB} result in smaller NF. Keeping the value of C_S to be 50 fF, and C_{BB} to be 60 fF, we iterate for R_{SW} = 48 Ω, 95 Ω, and 190 Ω. The NF results reveal that having a lower R_{SW} results in a lower NF. As a compromise between higher gain, lower NF, and ease of designing LO buffers, we fix the value of R_{SW} to be 95 Ω.

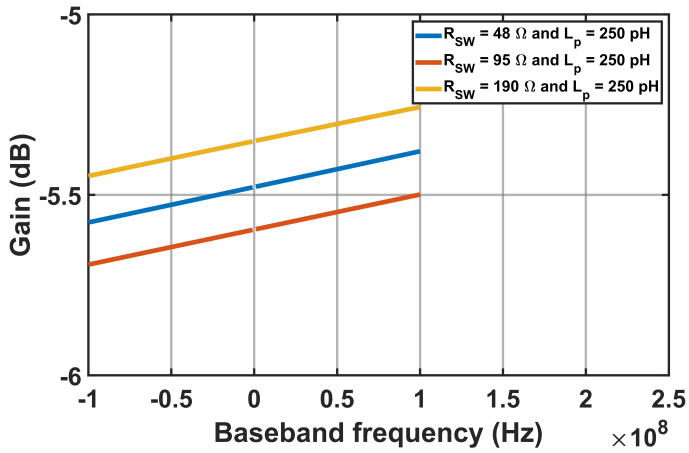


Figure 2.39: Gain vs baseband frequency based on expression 2.21 for different R_{SW} and L_P values.

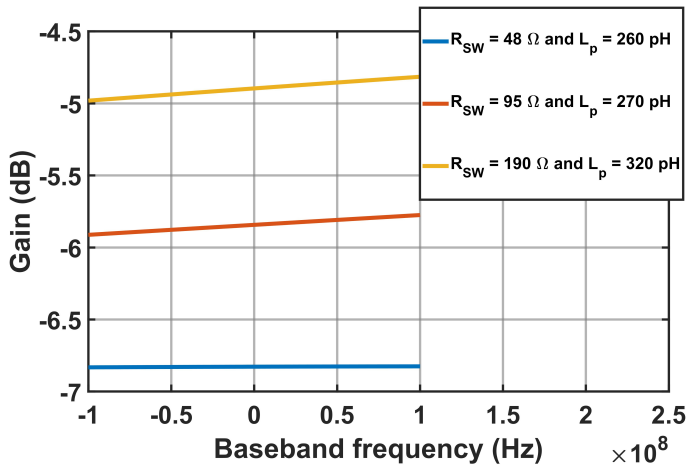


Figure 2.40: Gain vs baseband frequency based on SPICE simulations for different R_{SW} and L_P values.

C_S	C_{BB}	L_P	R_{SW}	NF
20 fF	60 fF	290 pH	95 Ω	7.49 dB
50 fF	60 fF	270 pH	95 Ω	9.19 dB
200 fF	60 fF	230 pH	95 Ω	11.8 dB

(a) NF variation with C_S

C_S	C_{BB}	L_P	R_{SW}	NF
50 fF	60 fF	270 pH	95 Ω	9.19 dB
50 fF	120 fF	190 pH	95 Ω	11.65 dB
50 fF	240 fF	160 pH	95 Ω	14.38 dB
50 fF	480 fF	130 pH	95 Ω	17.62 dB
50 fF	1 pF	120 pH	95 Ω	18.76 dB
50 fF	2 pF	110 pH	95 Ω	19.99 dB
50 fF	4 pF	100 pH	95 Ω	21.3 dB

(b) NF variation with C_{BB}

C_S	C_{BB}	L_P	R_{SW}	NF
50 fF	60 fF	260 pH	48 Ω	8.04 dB
50 fF	60 fF	270 pH	95 Ω	9.19 dB
50 fF	60 fF	320 pH	190 Ω	11.84 dB

(c) NF variation with R_{SW}

Table 2.4: NF variation with C_S, C_{BB}, and R_{SW}

The final design of the combining network and the mixer and component values are depicted in Fig. 2.41 and Table 2.5, respectively. The design merits two remarks. Firstly, unlike the conventional design of a double-balanced passive mixer, the outputs $V^{+}_{BB,I,P}$ and $V^{-}_{BB,I,N}$ are not shorted together. Similarly, the outputs $V^{-}_{BB,I,P}$ and $V^{+}_{BB,I,N}$ are not shorted together. Instead, we combine these signals with a differential amplifier [Fig. 5.6b]. For the conventional case, the capacitors do not enter hold mode as they are always connected to either the positive-side input or the negative-side input. Whereas, for our design, for about 50% of the time, the capacitors are in the hold mode, where they are not connected to any input. It can be shown that the hold mode provides an additional gain of 5.5 dB [28]. Simulations confirm that the gain for our design is higher by 6.8 dB, however, the NF for the two cases is similar. Secondly, since the mixing happens after the signal combining of four elements, while calculating the NF of the mixer, the noise contribution of the mixer devices has to be divided by four, i.e. equally among the four elements. The proof of this conjecture is provided in Appendix C. The single-element conversion gain and NF of the mixer are -11.9 dB and 18.5 dB, respectively. Finally, the L_P value chosen is somewhat sub-optimal. A value of 220 pH would give 3.7 dB higher gain and 2.4 dB lower NF. However, the reason for choosing lower L_P is to shift the resonance frequency of the combining network to a value slightly greater than 28 GHz. This is done to stagger the center frequency of the three different resonant loads present in the signal chain to get a wider bandwidth.

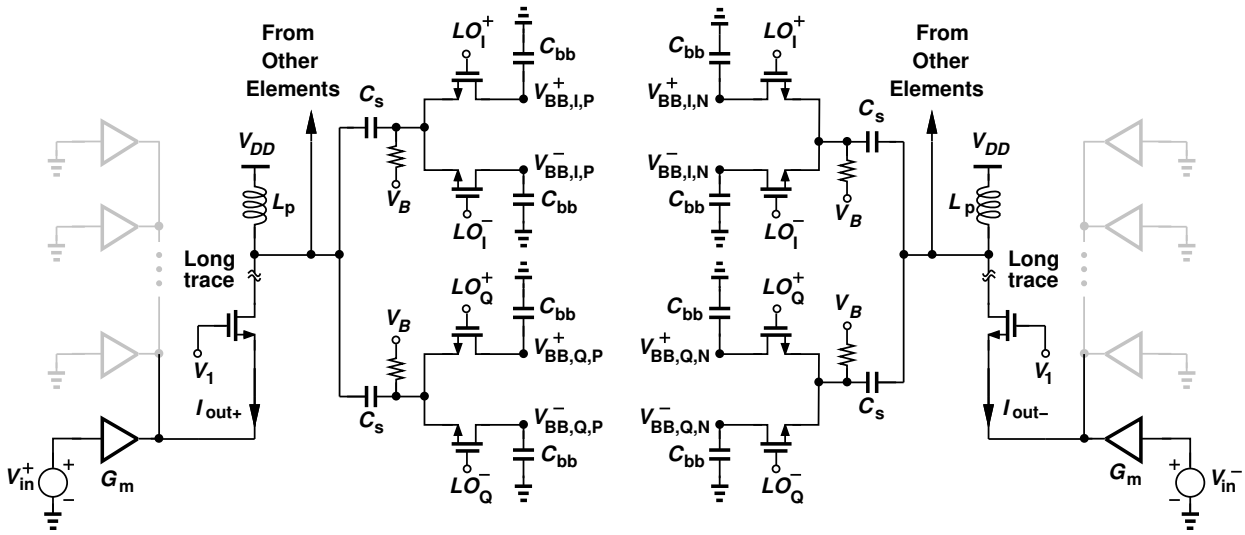


Figure 2.41: Design of the combining network and the mixer.

Mixer Transistor Size	L_P	C_S	C_{BB}
W/L = 4.4 μm/30 nm	160 pH	50 fF	60 fF

Table 2.5: Component values in Fig. 2.41.

At the output of the mixer, a baseband differential amplifier is connected which provides combining of the $V^{+}_{BB,I,P}$ and $V^{-}_{BB,I,N}$ signals, and $V^{-}_{BB,I,P}$ and $V^{+}_{BB,I,N}$ signals by means of the input transistor which is split into two segments with separate inputs [Fig. 2.42]. The amplifier gives a gain of 6.2 dB and has an NF of 15.4 dB at 10 MHz.

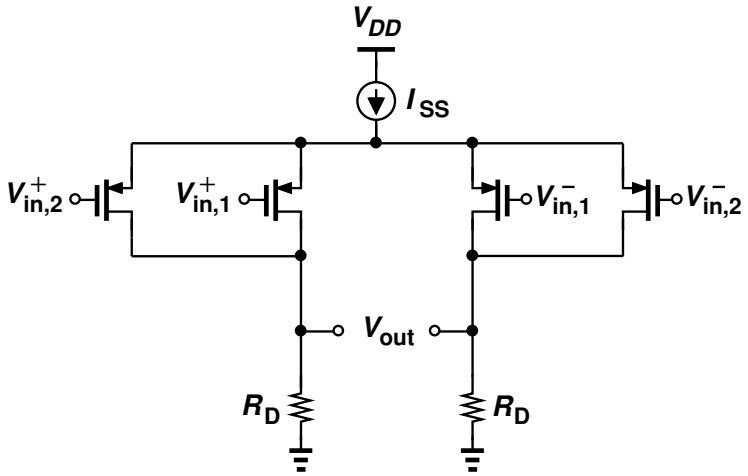


Figure 2.42: Baseband differential amplifier.

Input Transistor Size	R_D
W/L = 15 μm/110 nm	400 Ω

Table 2.6: Component values in Fig. 2.42.

Based on the NF of the mixer and the baseband amplifier, the front-end driving the T-line needs to have a gain greater than 36 dB and NF lesser than 3 dB to limit the overall NF of the RX to 3.5 dB. The next section describes the design of the LNA and the rest of the front-end.

2.3 LNA

2.3.1 Design Details

A common source topology with inductive degeneration provides low NF without high power consumption. The design of the LNA is depicted in Fig. 2.43. The component values are listed in Table 2.7. The input network consists of the L_g and L_s inductors that have coupling between them. Such a structure, presented in [29], has advantages in terms of area reduction required to implement the L_g and L_s inductors and the associated reduction in the NF of the LNA.

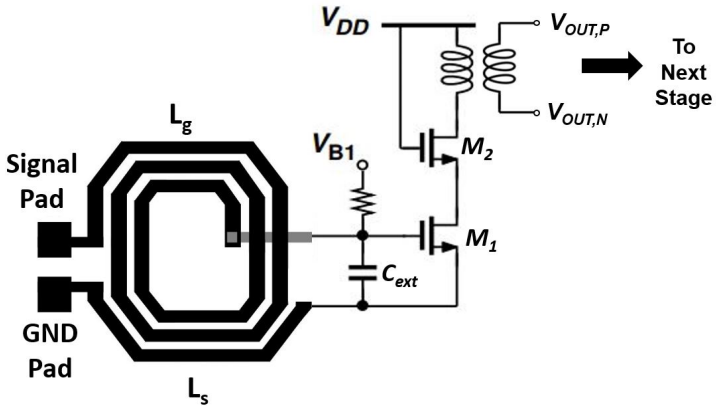


Figure 2.43: LNA circuit realization.

L_g	L_s	$k_{L_g-L_s}$	C_{ext}	M_1	M_2	Balun Primary	Balun Secondary	k_{Balun}
555 pH	94 pH	0.27	18 fF	W/L = 14 μm/30 nm	W/L = 14 μm/30 nm	389 pH	692 pH	0.7

Table 2.7: Component values in Fig. 2.43.

To understand the above points, first, we note that the L_g and L_s have associated trace resistance that can be modeled as R_{L_g} and R_{L_s}, in series with the two inductors, as shown in Fig. 2.44. The sum of these resistances is close to 10 Ω which is comparable to the source resistance of 50 Ω and so cannot be neglected while calculating the NF. The expression for the input impedance of the

LNA is as follows (where only the C_{gs} component of the transistor capacitances is considered):

$$Z_{in} = \frac{1 + g_m R_{L_s}}{s(C_{gs} + C_{ext})} + s(L_g + L_s + 2M) + R_{L_s} + R_{L_g} + \frac{g_{M_1}(M + L_s)}{C_{gs}} \tag{2.22}$$

$$\approx \frac{1}{s(C_{gs} + C_{ext})} + s(L_g + L_s + 2M) + R_{L_s} + R_{L_g} + \frac{g_{M_1}(M + L_s)}{C_{gs}} \tag{2.23}$$

M in the above expression denotes the mutual inductance between L_g and L_s. For matching to 50 Ω source, the imaginary component cancels by resonating at the frequency of interest, and the real part is equated to 50 Ω. As can be seen from Eq. 2.23, the required L_g and L_s values for resonance reduce due to the mutual inductance term. This translates to lesser R_{L_g} and R_{L_s} values which in turn reduces the NF. The NF of the LNA, considering the noise contribution of M_1, R_{L_g}, and R_{L_s} only, can be expressed as:

$$NF = 1 + \frac{R_{L_g} + R_{L_s}}{R_s} + \gamma_{M_1} \cdot g_{M_1} \cdot R_s \cdot \left(\frac{\omega}{\omega_T}\right)^2 \cdot \left(1 + \frac{R_{L_g} + R_{L_s}}{R_s}\right)^2 \tag{2.24}$$

where R_s is the source resistance, γ_{M_1} is the excess noise coefficient of M_1 transistor, ω_T is the transit frequency of M_1 given by $g_{M_1}/(C_{gs} + C_{ext})$. Simulations show that the area reduction in L_g and L_s due to their mutual inductance, reduces the $(R_{L_g} + R_{L_s})/R_s$ term from 0.19 to 0.15, which results in a 0.4 dB improvement in NF of the LNA. Simulation results predict a voltage gain of 24.4 dB from V_{in} to the differential output $V_{out,p} - V_{out,n}$, and an NF of 2.7 dB, with a power consumption of 3.8 mW.

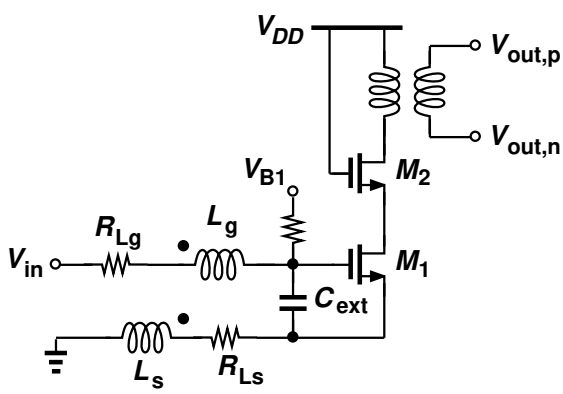


Figure 2.44: LNA circuit including R_{L_g} and R_{L_s}.

The balun at the output of the LNA is connected to a differential common source G_m stage with cascode devices, as shown in Fig. 2.45. The component values are listed in Table 2.8. The G_m stage has gain control functionality implemented through the cascode devices $M_{5,1-4}$, $M_{6,1-4}$,

$M_{7,1-4}$, and $M_{8,1-4}$. These devices can be switched on or off by means of control signals V_1-V_4. Turning the devices $M_{6,1-4}$ and $M_{8,1-4}$ on reduces the gain by diverting some of the signal current to the supply. The gain control provides 3-dB range in four steps. The gain control is used to correct for the variation in gain for the different phase shifter settings that occurs because of the loss of the T-line.

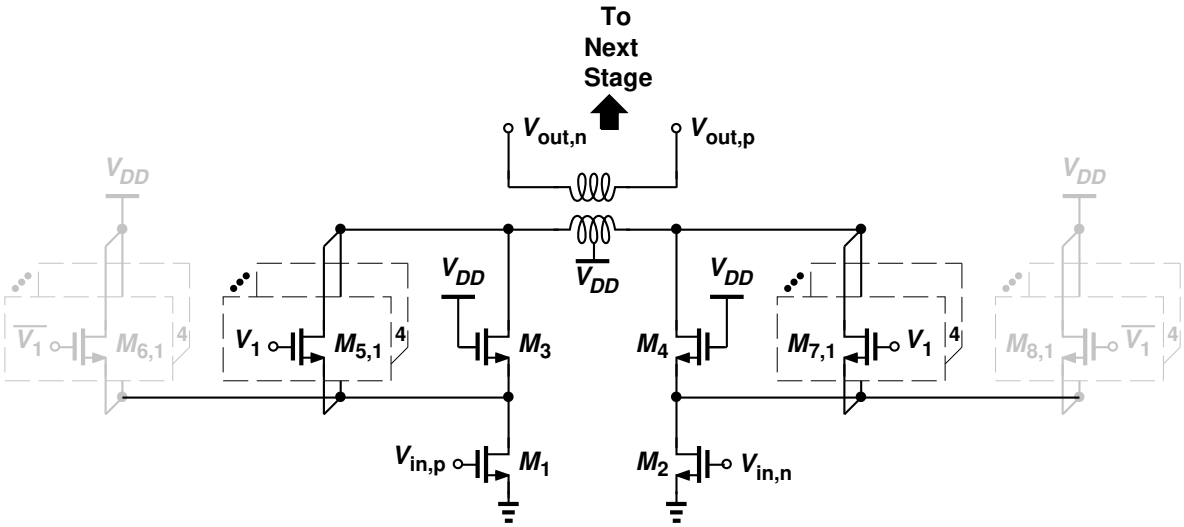


Figure 2.45: G_m stage following the LNA with gain control functionality.

M_1	M_3	$M_{5,1-4}$	$M_{6,1-4}$	Load Transformer Primary	Load Transformer Secondary	$k_{Transf.}$
W/L = 14.4 μm/30 nm	W/L = 11.2 μm/30 nm	W/L = 0.8 μm/30 nm	W/L = 0.8 μm/30 nm	849 pH	493 pH	0.72

Table 2.8: Component values in Fig. 2.45.

The G_m stage drives the T-lines through the transformer as shown in Fig. 2.46. The programmable cross-coupled pair is used to provide additional gain. Boosting the gain with the cross-coupled pair instead of raising the transconductance of the G_m stage, leads to lesser power consumption. Measurements show that the cross-coupled pair provides a 5.7 dB boost in the gain with just 1.2 mA current consumption when all branches of the cross-coupled pair are active. The dimensions of the cross-coupled pair devices and the switches which turn each section on or off

are listed in Table 2.9. The LNA and the G_m stage, depicted in Fig. 2.46, together provide a simulated voltage gain of 32 dB, measured from the LNA input to the last tapping point of the T-line, i.e. $V_{out,6}$. While measuring the gain till the last tapping point of the T-line, the G_m stage is programmed to give maximum gain. The simulated NF of the depicted part of the front-end is 3.0 dB and the power consumption is 13 mA.

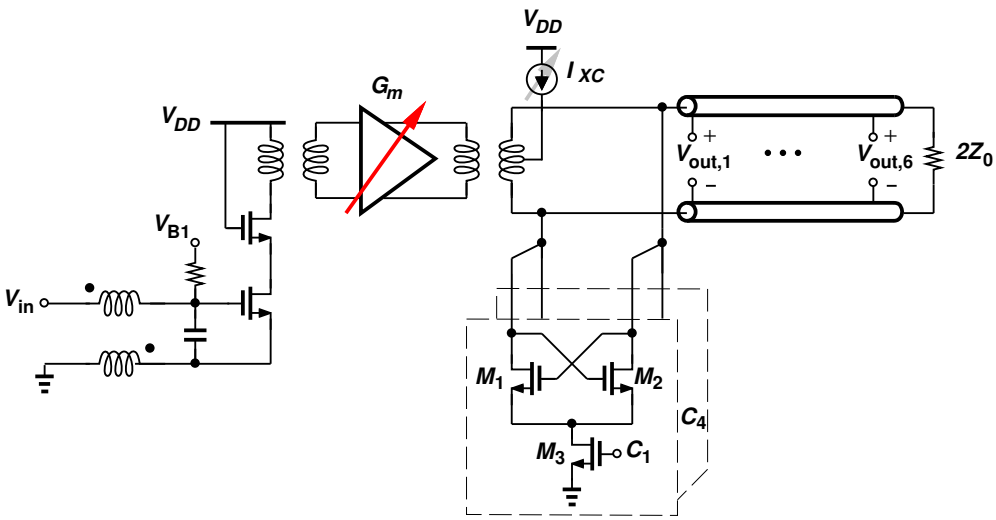


Figure 2.46: LNA and the G_m stage driving the T-lines.

M_1	M_3	Z_0
W/L = 0.75 μm/30 nm	W/L = 8.3 μm/30 nm	350 Ω

Table 2.9: Component values in Fig. 2.46.

2.3.2 Floorplan Considerations

The area of the RX is dominated by the inductors and transformers used in the signal path. A key factor in determining the floorplan is the magnetic coupling between physically nearby inductors. Due to the presence of two gain stages, even a small coupling factor between adjacent inductors like 0.01 can lead to significant amount of feedback. While a positive feedback is desirable because of the resultant increase in gain, it must be sufficiently weak to ensure that

stability is maintained and input impedance of the LNA is not severely modified. The spacing between different inductors is set keeping this consideration in mind. The RX floorplan of a single element's front-end is shown in Fig. 2.47. Shown in the figure are the L_g and L_s inductors at the input of the LNA, the balun at the LNA output, the transformer at the output of the G_m stage, and the differential T-lines.

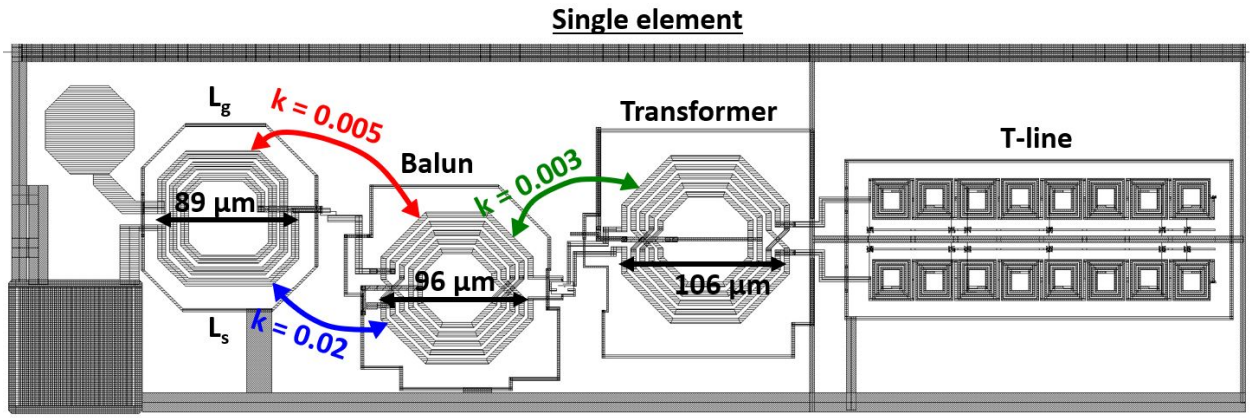


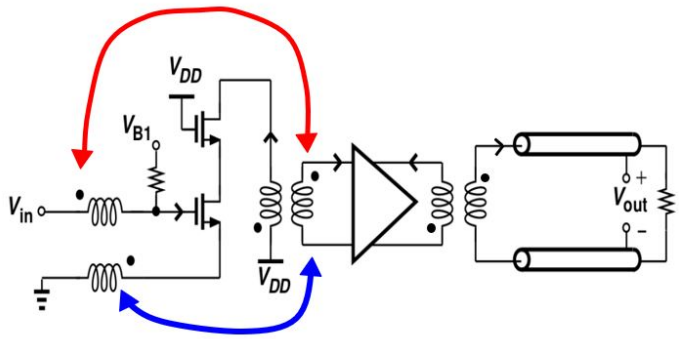
Figure 2.47: Single-element front-end floorplan.

Amongst the numerous coupling mechanisms present between every pair of inductors, we identify the three most significant ones and then set their direction in a way that translates to positive feedback. We start with the coupling direction between L_g and the secondary of the balun. Setting the direction of this coupling also automatically fixes the direction of coupling between L_s and the secondary of the balun since the direction of coupling between L_g and L_s is already fixed as described in the previous section.

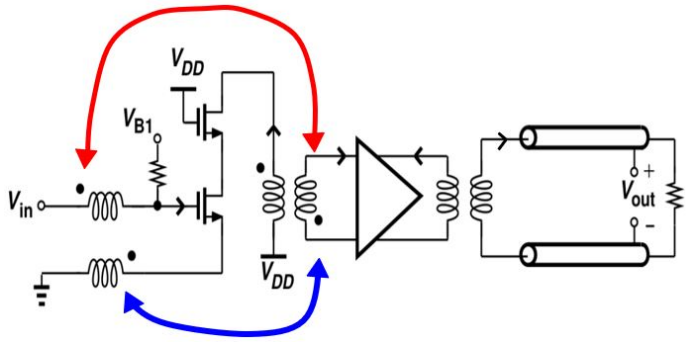
Deciding direction of coupling between $\mathbf{L_g}$ and secondary of balun, and $\mathbf{L_s}$ and secondary of balun:

Figure 2.48 depicts the two possible scenarios of coupling directions. The case depicted in Fig. 2.50a results in a positive voltage feedback due to the coupling between the secondary of the balun with L_g and L_s. It must be noted that for the same case, the coupling between the primary of the balun with L_g and L_s results in a negative feedback, however, since the coupling with the secondary is stronger, the net feedback still remains positive. The second case, depicted in Fig. 2.50b represents negative feedback. Either of the two cases can be implemented depending on

which terminal of the balun primary is connected to the supply and which one is connected to the output of the LNA. The gain from V_{in} to V_{out} as a function of the frequency is shown in Fig. 2.49b for both the cases. The positive feedback case provides 1.3 dB higher gain. Also shown in Fig. 2.49a is the input impedance for the two cases. The positive feedback results in a reduction of real part of input impedance as is expected. However, since the simulated S_{11} is still better than -10 dB, we choose the positive feedback case and set the direction of coupling accordingly.



(a) Positive feedback case.

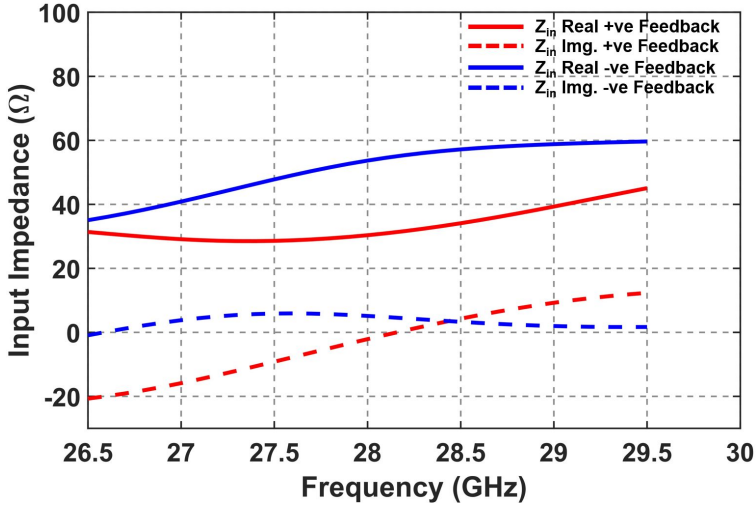


(b) Negative feedback case.

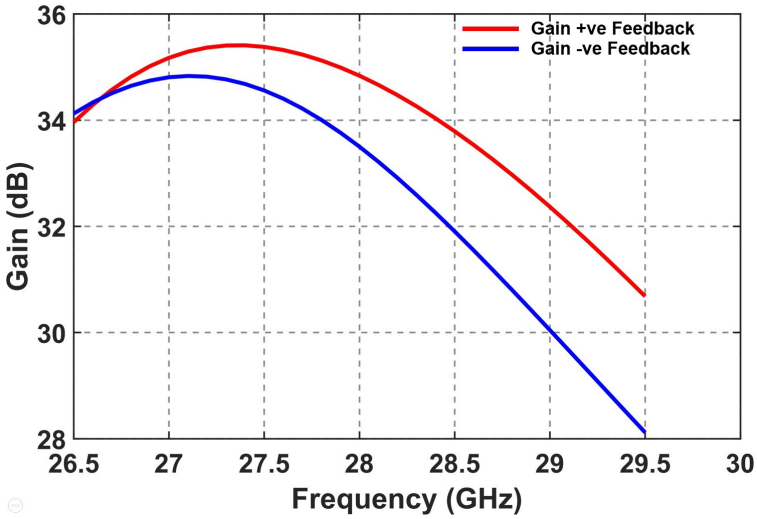
Figure 2.48: Different directions of coupling between secondary of balun with L_s and L_g.

Deciding direction of coupling between the secondary of balun and primary of transformer:

The next choice to be made is about the direction of coupling between the secondary of the balun and the primary of the transformer. The two different choices are depicted in Fig. 2.50. The gain for the two cases is depicted in Fig. 2.51. Again, we choose the positive feedback case which gives 1.8 dB increase in gain and set the direction of coupling accordingly.

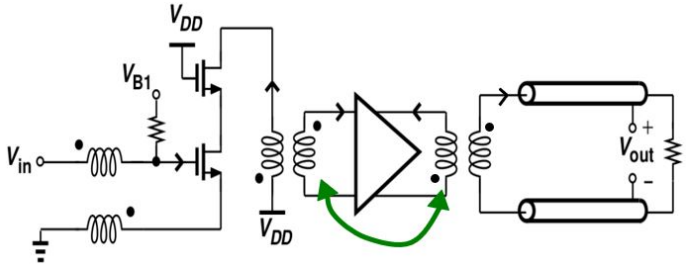


(a) LNA input impedance for the two cases.

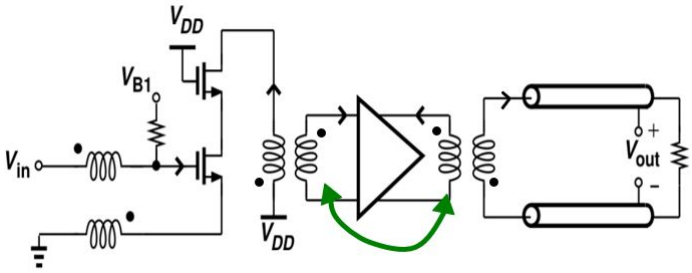


(b) Gain for the two cases.

Figure 2.49: Input impedance and gain for the two directions of coupling shown in Fig. 2.48.



(a) Positive feedback case.



(b) Negative feedback case.

Figure 2.50: Different directions of coupling between the secondary of balun with the primary of the transformer.

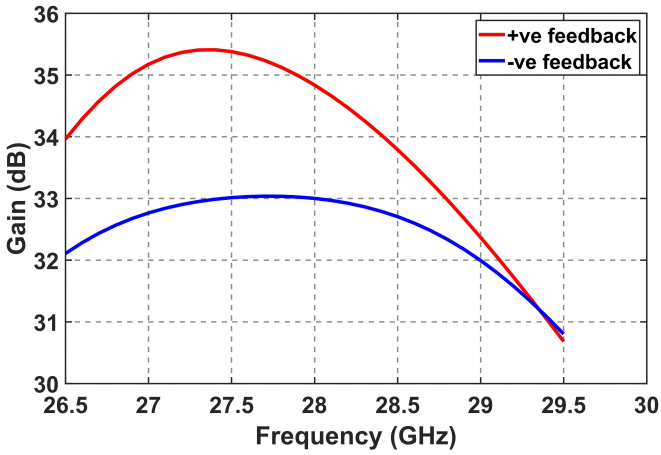


Figure 2.51: Gain for the two directions of coupling shown in Fig. 2.50.

2.3.3 Problem of Inter-Element Coupling

The preceding analysis described how the coupling between inductors of the same element can be utilized to improve the single-element performance. However, any coupling between adjacent elements of the RX proves to be detrimental to the performance. As an example, Fig. 2.52 depicts two adjacent elements separated by 236 μm. Depending on the direction of arrival of the beam, in extreme cases, the two elements receive signals that can have a phase shift of 0°, for boresight beam direction, or 180°, for the beam direction perpendicular to the antenna array. The second element changes the response of the first element due to the magnetic coupling present between them. This change in the response depends on the relative phase between the two elements and so, for the two extreme cases considered above, the gain and phase response measured at the T-line tapping point of the first element varies. Figure 2.53 shows the gain and phase response for the two cases considered and reveals that the gain and phase change by 2.1 dB and 18°, respectively.

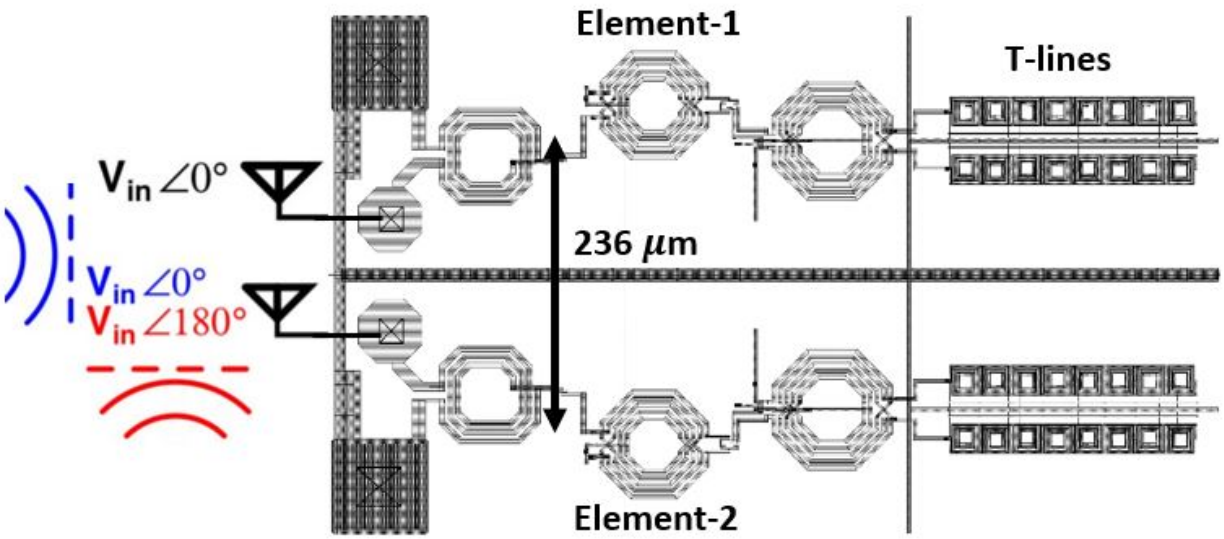
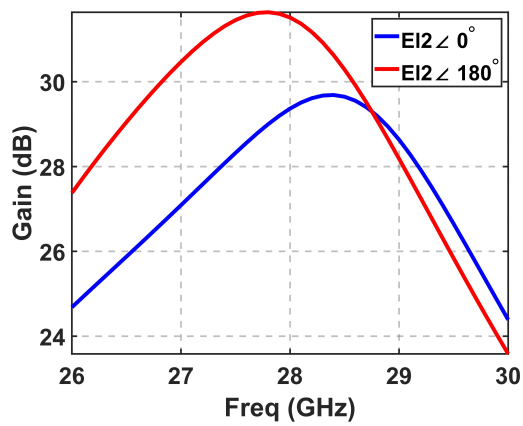
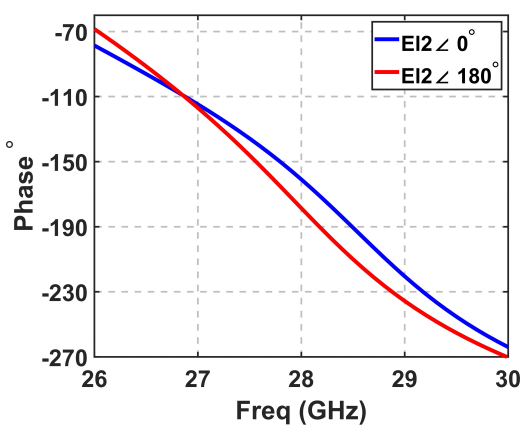


Figure 2.52: Adjacent elements receiving signals with different relative phase.

To mitigate the issue of inter-element coupling, we add guard rings around each inductor and the T-lines of the two elements. A guard ring is also added around each element [Fig. 2.54]. These rings increase the magnetic isolation between the different inductors and as a result, the gain and phase response of the first element changes to a lesser degree depending on the second element's phase. Figure 2.55 shows the gain and phase response of the first element and reveals that by



(a) Gain response of the first element changes due to the relative phase of the second element.



(b) Phase response of the first element changes due to the relative phase of the second element.

Figure 2.53: Affect of the second element phase on the first element's output.

adding guard rings, the gain and phase changes for the two cases considered are limited to 0.8 dB and 5° only.

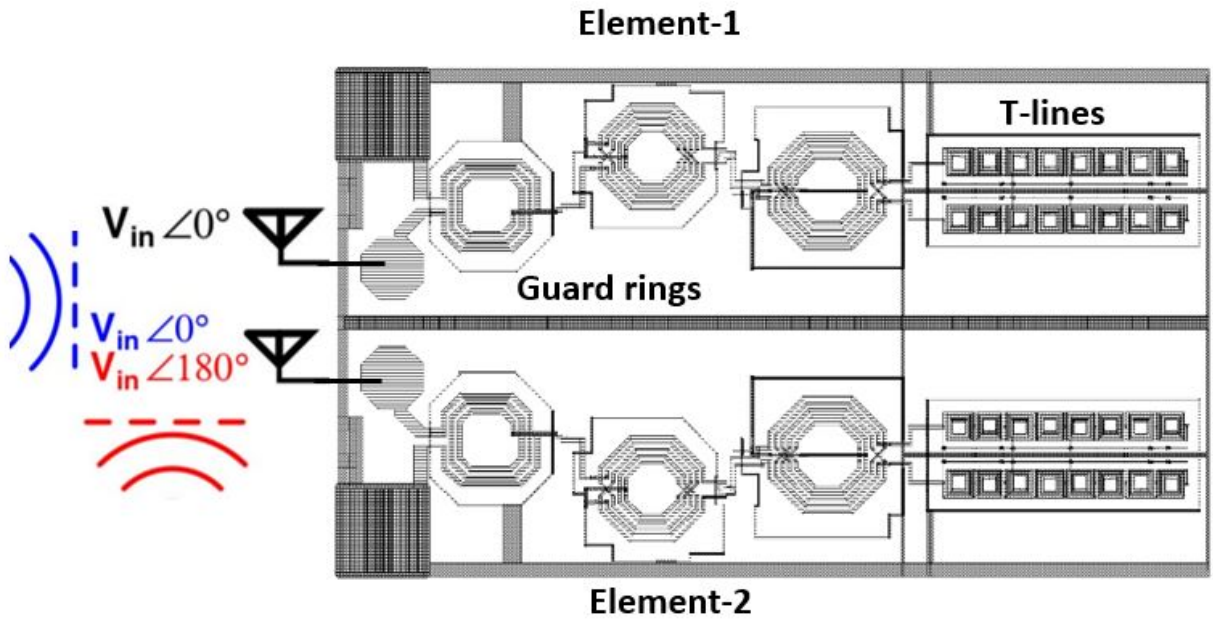
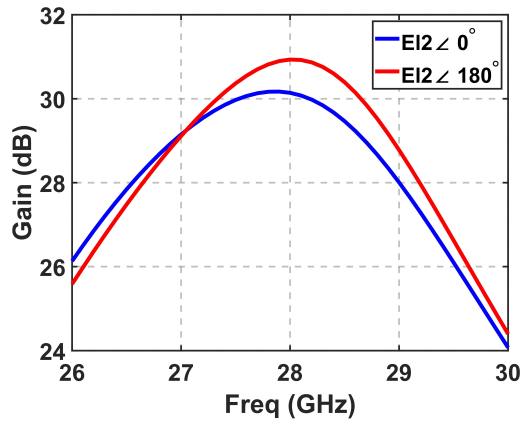
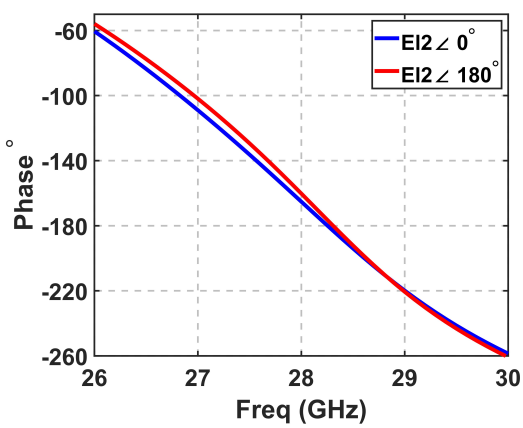


Figure 2.54: Adjacent elements with guard rings.



(a) Gain response of the first element changes to a lesser extent due to the relative phase of the second element.



(b) Phase response of the first element changes to a lesser extent due to the relative phase of the second element.

Figure 2.55: Affect of the second element phase on the first element's output reduces by adding guard rings.

2.4 Performance Breakdown of Signal Path

The overall eight-element RX architecture is shown in Fig. 2.56. The outputs of the top four and the bottom four elements are not combined to maintain flexibility in testing and characterization. We describe the LO synthesis in the next section. The simulated power consumption, voltage gain, NF, IP_{1dB}, and IIP_3 of all the components constituting the signal path are listed in Table 2.10.

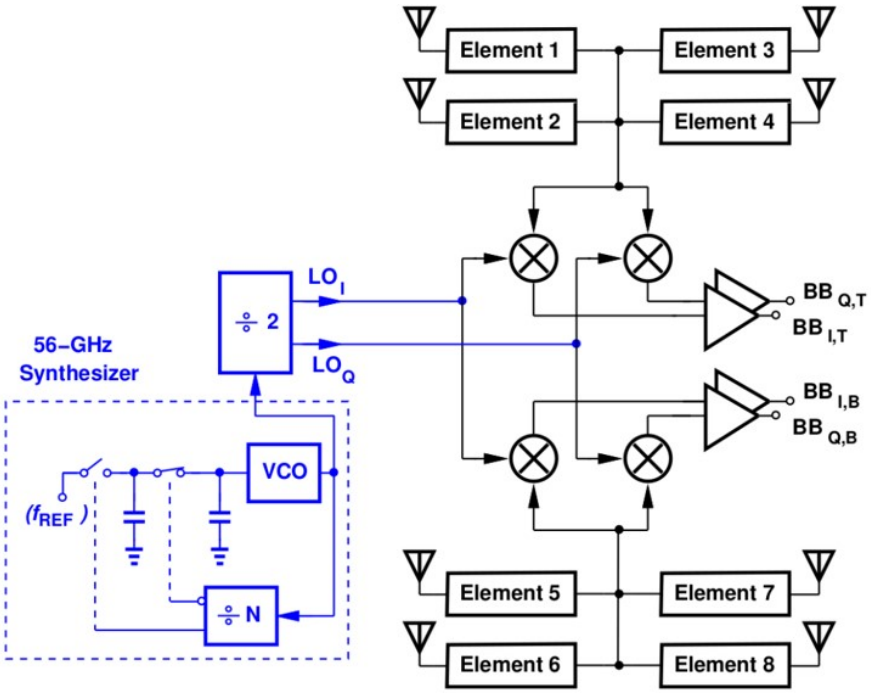


Figure 2.56: Overall eight-element RX architecture.

	LNA and G_m stage driving the T-lines	**T-line tapping G_m devices and mixer**	**Baseband Amplifier**
Power consump.	12.8 mA (single element)	2.4 mA (single element)	4.6 mA
Voltage Gain	32.2 dB (single element)	-11.9 dB (single element)	6.2 dB
NF	3.0 dB (single element at 28 GHz)	18.5 dB (single element at 10 MHz)	15.4 dB (at 10 MHz)
IP_{1dB}	-29 dBm (single element)	4 dBm (single element)	-2.9 dBm
IIP_3	-22.9 dBm (single element)	11.9 dBm (single element)	7.6 dBm

Table 2.10: Simulated performance breakdown of the signal path.

2.5 LO Synthesis[1,2]

The 28-GHz I and Q signals are generated on-chip through a 56-GHz synthesizer followed by a divide-by-two circuit. The circuit realization of the complete LO synthesis is depicted in Fig. 2.57. The phase-locked loop (PLL) consists of a sampling phase detector followed by a loop filter. The component values for the phase detector and loop filter are listed in Table 2.11. The design details about the rest of the building block of the PLL can be found in [30]. The PLL has a loop bandwidth of 10.7 MHz. The PLL consumes 10.4 mW of power.

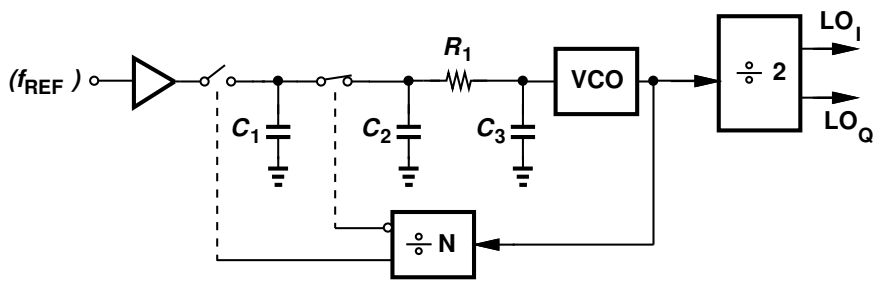


Figure 2.57: PLL Design.

f_{REF}	C_1	C_2	C_3	R_1
250 MHz	520 fF	130 fF	1.2 pF	320 Ω

Table 2.11: Component values in Fig. 2.57.

The design of the divide-by-2 following the PLL is taken from [31]. The divider has to divide 56-GHz clock down to 28 GHz. At such a high frequency of operation, two principal challenges need to be addressed. Firstly, the delay of the latches used within the divider should be less than half of the clock period. Secondly, the divider should rely on perfectly differential operation to generate complimentary outputs because the fanout-1 delay of an inverter for the technology is around 8 ps, which is a significant fraction of the time period of the output 28-GHz clock. The C^2MOS implementation, shown in Fig. 2.58 addresses these issues. The cross-coupled pair added

[1]**PLL proposed and designed by Yu Zhao**

[2]**Divide-by-2 proposed and designed by Mahdi Forghani**

between D and $\overline{Q}$, and $\overline{D}$ and Q ensure differential operation. The extra bypass inverters aid high-speed operation by preemptively charging or discharging the outputs of the latches before the latches become transparent. These bypass inverters adversely affect the low-speed operation causing the divider to fail at lower frequencies. As a result, the divider has a maximum as well as minimum frequency of operation as depicted in Fig. 2.59. Extensive simulations are done to ensure that the divider operates at 56-GHz across corners. The divider draws only 4.7 mW.

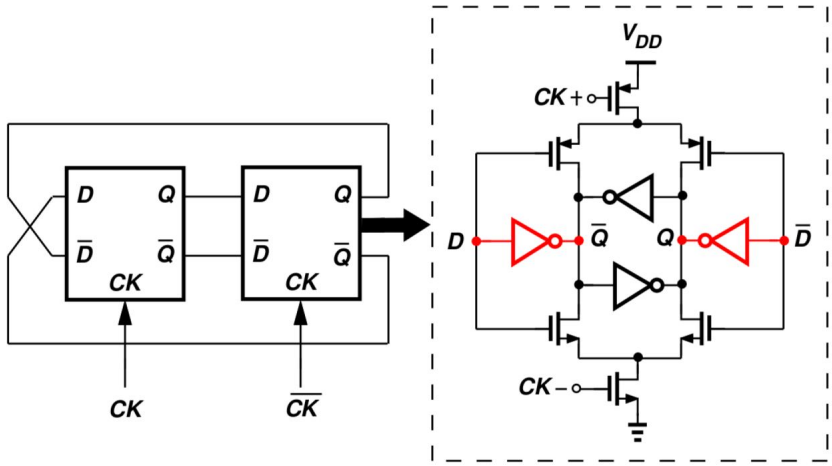


Figure 2.58: Proposed divide-by-2

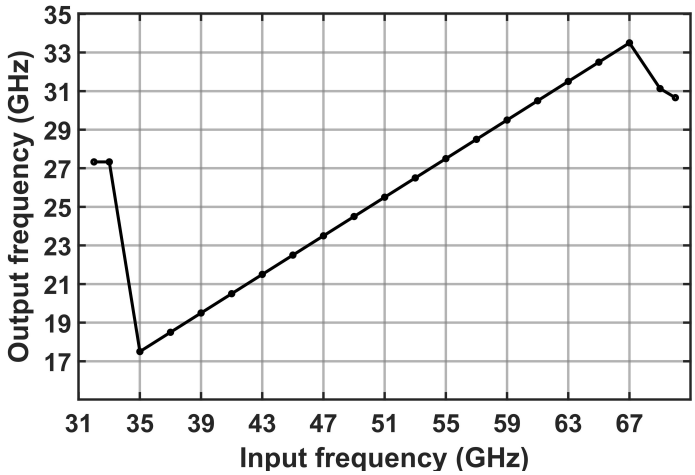


Figure 2.59: Proposed divide-by-2 output frequency vs input frequency profile

2.6 LO Leakage Cancelation

Another concept proposed here relates to the carrier leakage to the RF path, a severe issue at 28 GHz leading to possible desensitization and/or large dc offsets in the baseband. We present in Fig. 2.60 an active LO cancellation method that reduces the dc offsets. The I and Q phases of the LO are scaled, interpolated, and injected into nodes A and B by means of differential amplifiers with programable tail current sources as shown in Fig. 2.61, and the component values are listed in Table 2.12. The optimum settings are determined by observing and minimizing the offsets in each of the baseband outputs. The noise added to the signal path by the LO injectors raises the overall noise figure by only 0.02 dB. The Experimental Results chapter contains the measured performance results for the LO leakage cancelation scheme.

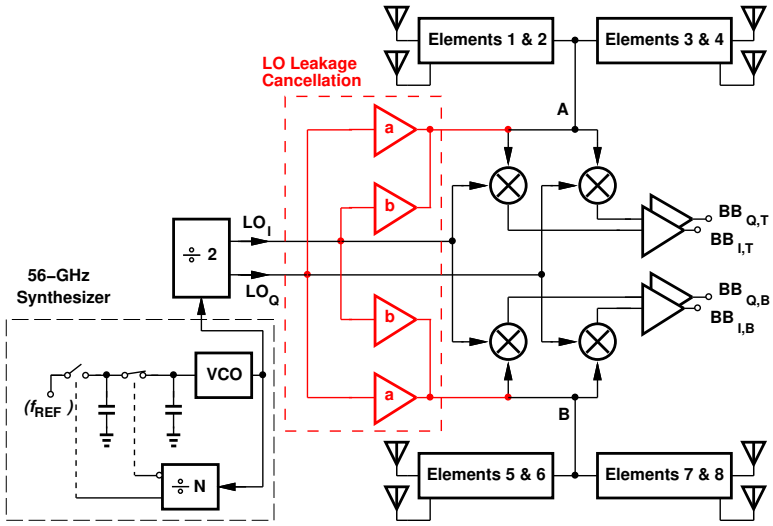


Figure 2.60: LO leakage cancellation architecture.

LO Transistors Size	$I_{SS,I/Q}$ Full Scale
W/L = 2 μm/30 nm	250 μA (Nominal) to 600 μA (in steps of 50 μA)

Table 2.12: Component values in Fig. 2.61.

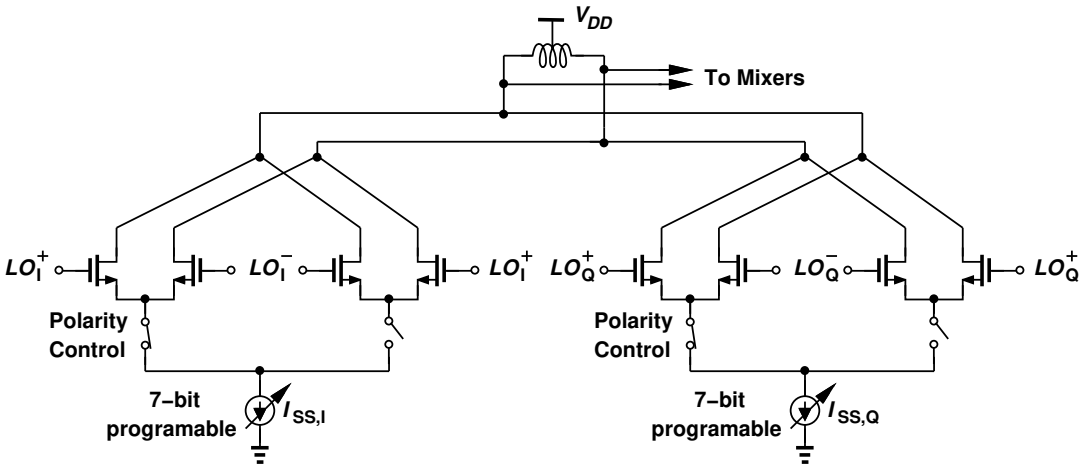


Figure 2.61: LO leakage cancellation circuit realization.

CHAPTER 3

Experimental Results

The eight-element RX has been fabricated in TSMC's 28-nm technology and tested with a 1-V supply. Figure 3.1 shows the photograph of the die, which measures 1.38 mm × 1.71 mm. The RX draws a total of 156 mW in the low-NF mode and 109 mW in the low-power mode, of which 38 mW are drained by the synthesizer and the LO distribution network and the rest by the eight receive paths. The RF input is applied through GS probes. The measured results are recorded for the RX operating in two modes: low-NF mode, and low-power mode. In the low-NF mode, the bias currents of the LNA and the G_m stage following the LNA are set to the maximum. Also, all four sections of the cross-coupled pair present at the input of the T-lines are turned on. Whereas, in the low-power mode, the bias currents of the LNA and the G_m stage are set to the minimum and only one section of the cross-coupled pair is turned on. The breakdown of the power consumption of the RX in the two modes is given in Table 3.1.

	Low-NF Mode	**Low-power Mode**
Front-end	110 mW	63 mW
LO generation and distribution	38 mW	38 mW
Baseband Amplifiers	8 mW	8 mW
Total	156 mW	109 mW

Table 3.1: Measured power consumption breakdown.

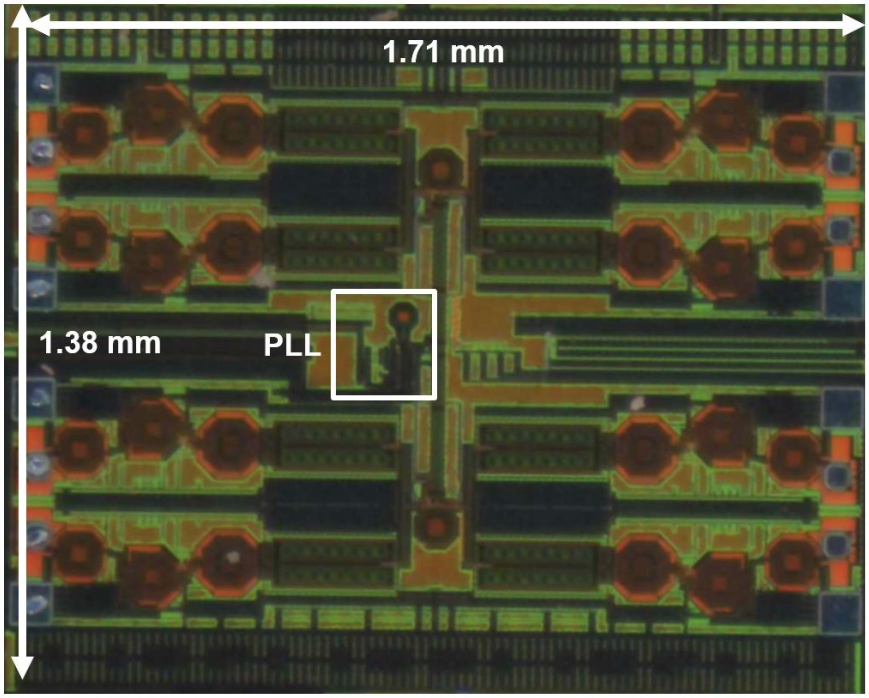


Figure 3.1: Die photograph.

3.1 Return Loss, Gain, NF, and P_{1dB}

The S_{11} measured across 10 MHz to 67 GHz for the two operating modes is depicted in Fig. 3.2. The close-up of the S_{11} in the frequency range of interest is depicted in Fig. 3.3, and shows that the S_{11} remains below -7.7 dB across the frequency range of interest.

The gain of a single element operating in the low-NF and low-power mode is shown in Fig. 3.4. The maximum gain for both modes occurs at an input frequency of 28.2 GHz. The gain for the low-NF mode is 31.3 dB and the 3-dB bandwidth is 1.6 GHz. The gain for the low-power mode is 23.4 dB and the 3-dB bandwidth is 1.7 GHz.

The NF is measured for the combined output of the four elements of the RX. For carrying out the measurement, four Keysight 346C-K01 noise sources are connected to the four elements and their combined output is connected to the Noise-Figure meter, which performs a Y-factor NF measurement [Fig. 3.5a]. Such a measurement correctly captures the true single-element NF of the beamforming RX as is shown in Appendix C. We compare the NF results with another measurement where the NF is measured by enabling only a single element [Fig. 3.5b]. The results

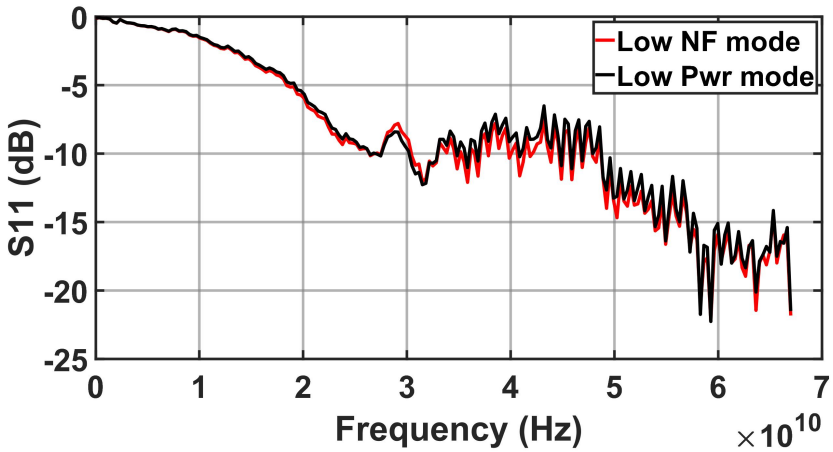


Figure 3.2: Measured S_{11} from 100 MHz to 67 GHz.

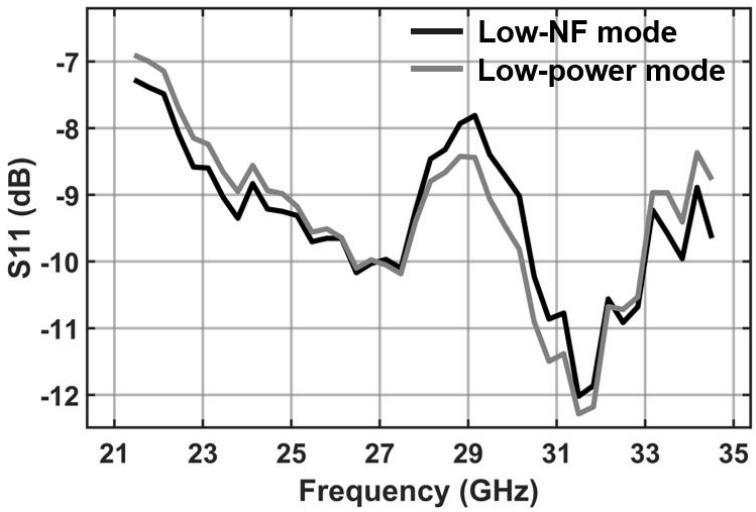


Figure 3.3: Measured S_{11} from 21.4 GHz to 34.5 GHz.

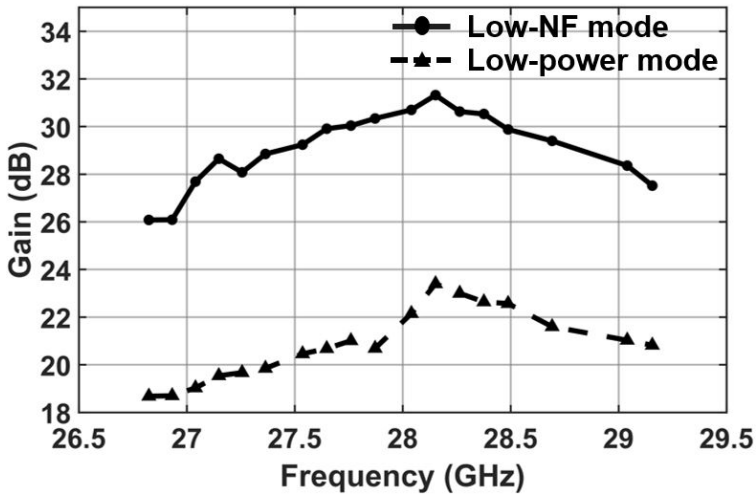


Figure 3.4: Measured single-element gain across frequency.

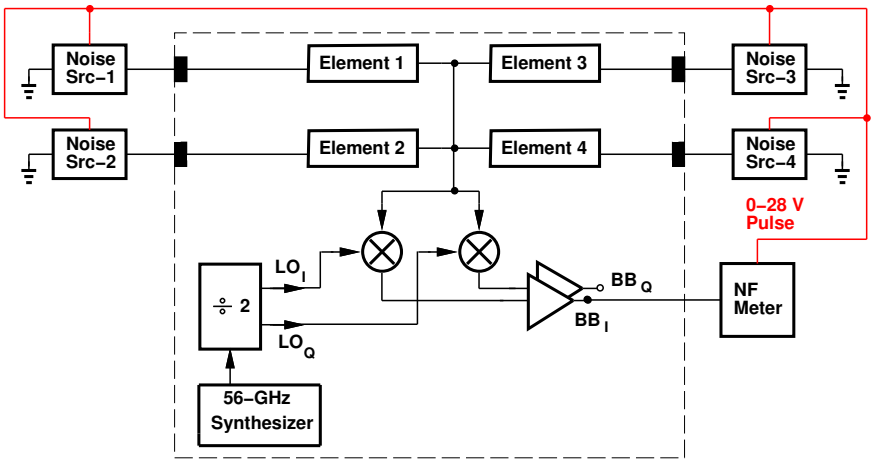
of both these measurements, for the low-NF mode operation, are shown in Fig. 3.6. The NF at 28 GHz is 3.7 dB and remains below 4 dB for frequencies between 26.9 GHz and 29.1 GHz. The NF for the case where only a single element is enabled is higher than the case where the outputs of the four elements are combined, as is expected. The measured NF for the low-power mode is shown in Fig. 3.7. The four-element combined NF is 6.8 dB at 28 GHz input.

The single element 1-dB compression characteristics of the RX in the two modes are shown in Fig. 3.8. The IP_{1dB} in the low-NF mode is -39 dBm and for the low-power mode, it is -31 dBm.

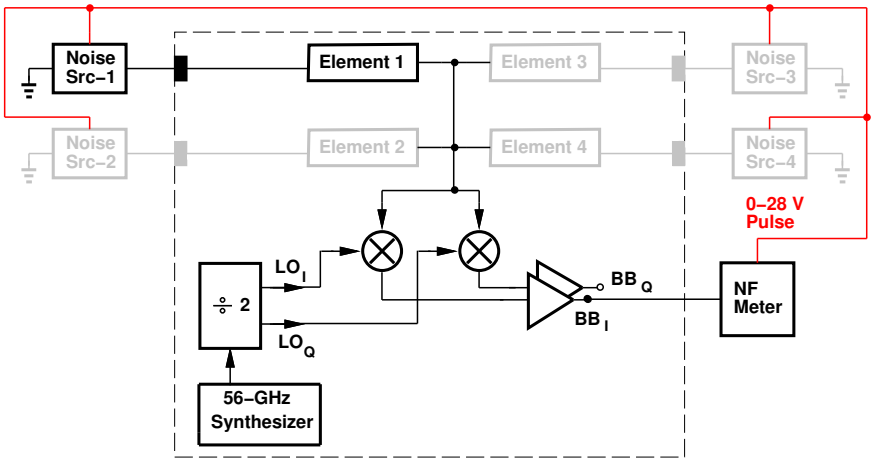
3.2 Phase Shift Characteristics

The measured phase shift characteristics at 28 GHz input for all the different codes are compared with the simulated results in Fig. 3.9. The match between simulations and measurements is very good till $-100°$, which corresponds to the first 19 codes. Thereafter, the measured results show a larger phase shift step than simulations for higher codes. Since we want a phase shift range of close to 180° only, we only consider the first 36 codes which give us a total phase shift of 202°, and discard the codes between 37 to 41. The selected codes provide an average phase shift resolution of 5.8° with an rms error of 5.9° as depicted in Fig. 3.10. The INL for the phase shift characteristics is plotted in Fig. 3.11.

To measure the variability across the phase shift characteristics of different elements on the same



(a)



(b)

Figure 3.5: (a) NF measurement for the combined outputs of four elements, (b) NF measurement for only one element.

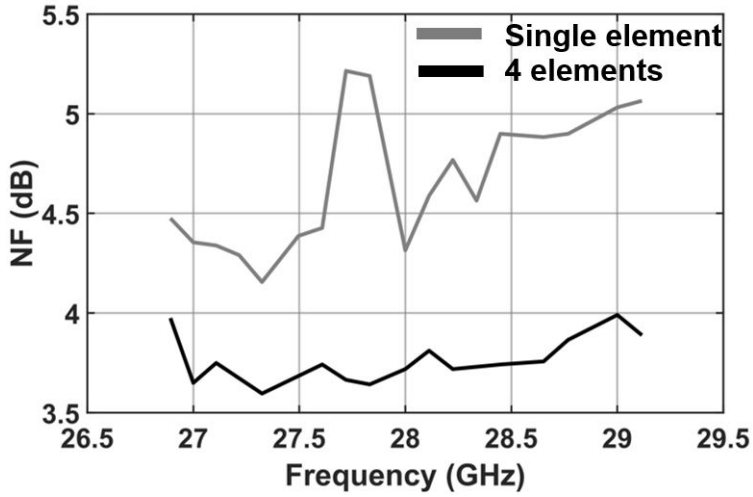


Figure 3.6: Measured NF for outputs of four elements combined and for single element (low-NF mode).

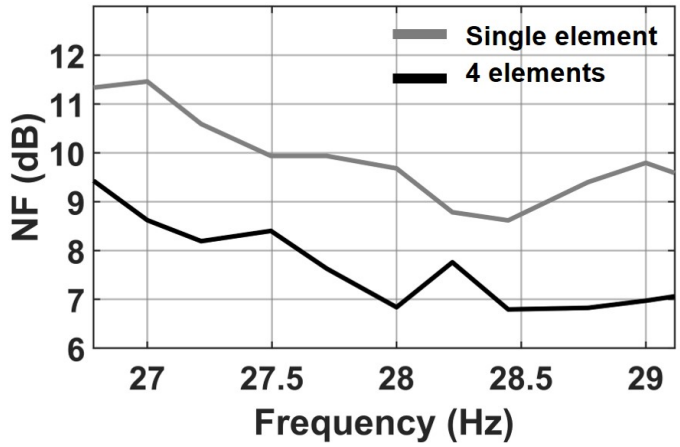


Figure 3.7: Measured NF for outputs of four elements combined and for single element (low-power mode).

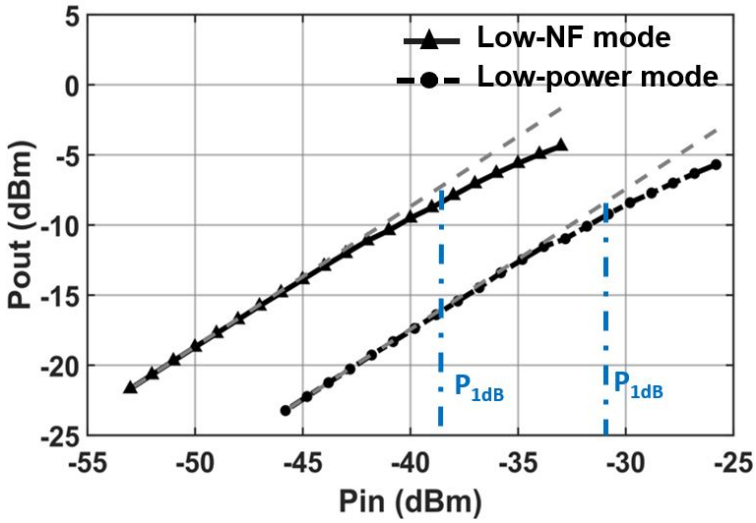


Figure 3.8: Measured 1-dB compression characteristics for single element.

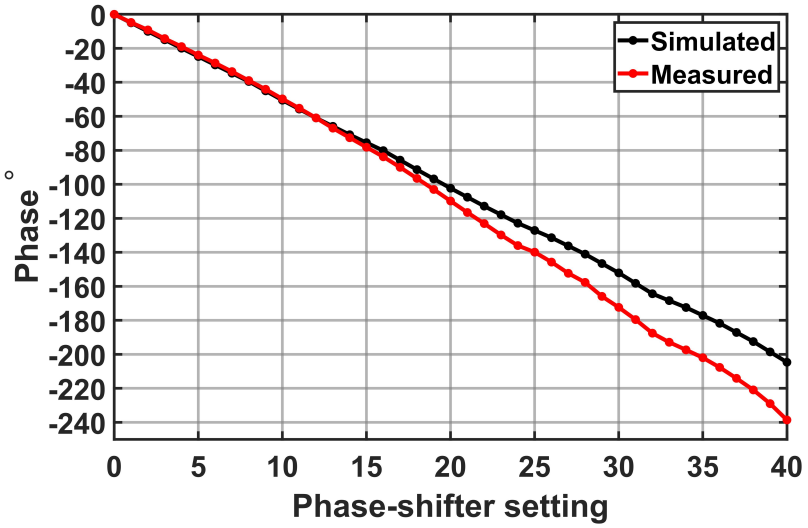


Figure 3.9: Measured phase shift characteristics compared with the simulated results.

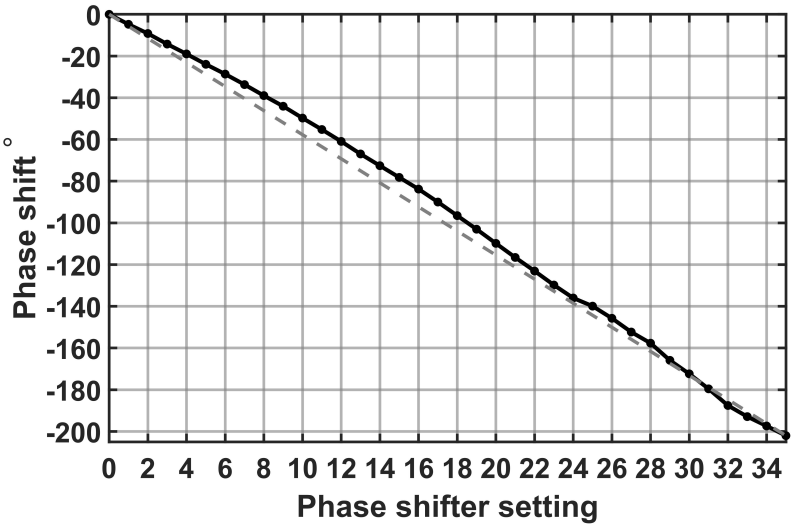


Figure 3.10: Measured phase shift characteristics for the first 37 codes.

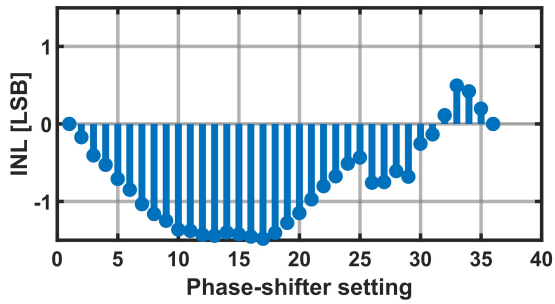


Figure 3.11: Measured INL for the phase shift characteristics.

chip, we plot the measured phase shift characteristics for three elements in Fig. 3.12. The maximum variation in phase shift for any code across the three elements is 1.6°.

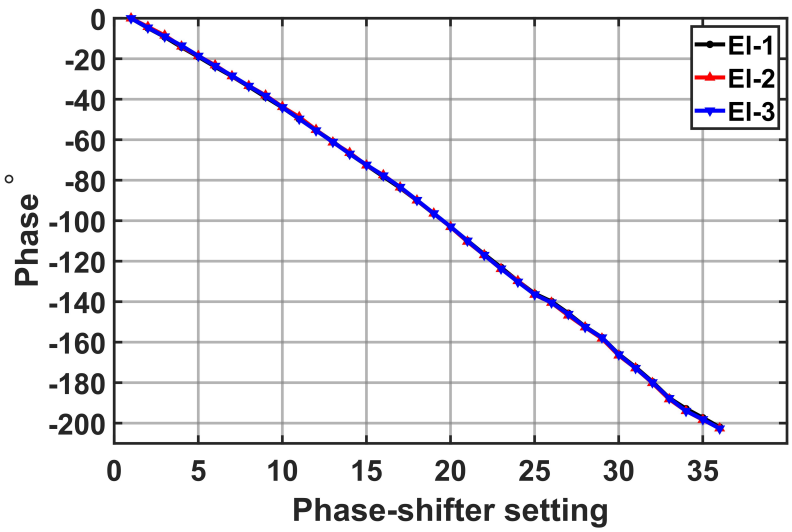


Figure 3.12: Measured phase shift characteristics for three different RX elements.

The gain variation across different phase shifter settings after applying gain correction is plotted in 3.13. The maximum variation in gain is 2.6 dB. To test the efficacy of signal combining, the two-element patterns for the RX are measured. The phase shift of one element is varied with respect to the other by applying different phase shifter settings to that element. The two-element patterns shown in Fig. 3.14 depict the combined output of the two elements vs the phase shifter settings. The amplitude level at 180° phase shift with respect to the 0° level is -25 dB, which is an indicator of the fine phase shift resolution achieved.

Shown in Fig. 3.15 are the phase shift characteristics for different codes as a function of the input frequency. For this measurement, we only consider alternate phase shift codes i.e. the codes 0, 2, 4, and so on till 34. The total phase shift rises with the input frequency. For instance, for all the 35 codes, the total phase shift rises from 178.7° at 27 GHz to 199.2° at 28 GHz, and to 205.1° at 29 GHz. This behavior indicates that the phase shift is close to true-time-delay phase shift since it is derived from a T-line. The nonlinearity in phase shift as a function of frequency occurs due to the factors mentioned in section 2.1.4, namely the change in capacitive loading of the T-line as the phase shifter settings are changed, the feedthrough from the C_{gd} of off-state G_m stages, and the coupling between the output trace of the G_m stages and the T-line.

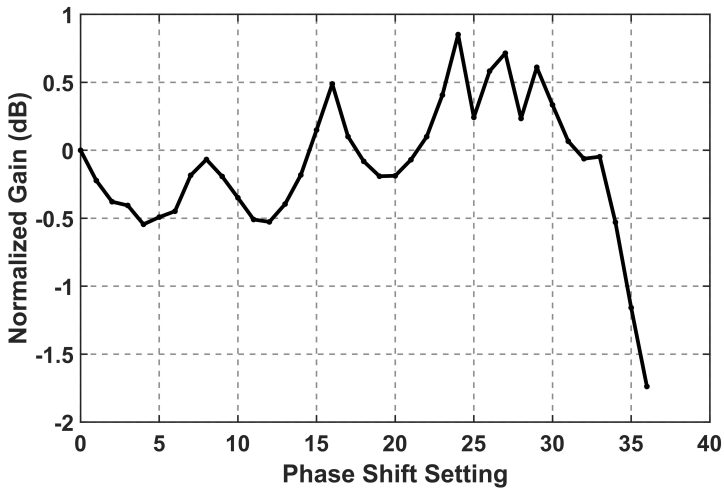


Figure 3.13: Measured gain variation across different phase shift settings.

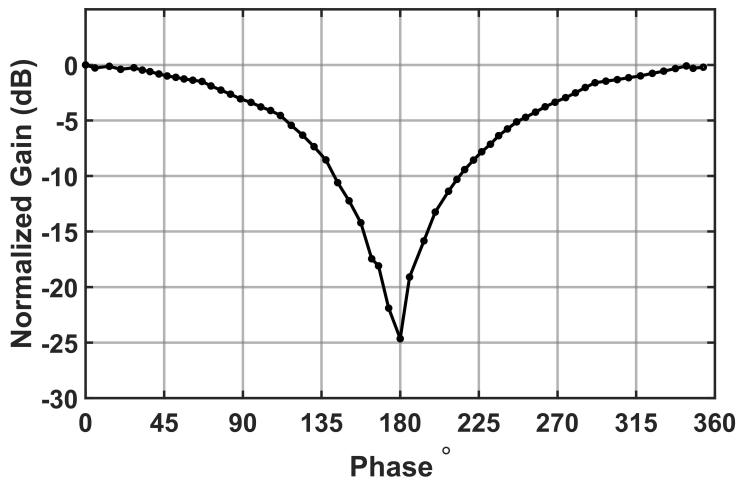


Figure 3.14: Measured two-element pattern.

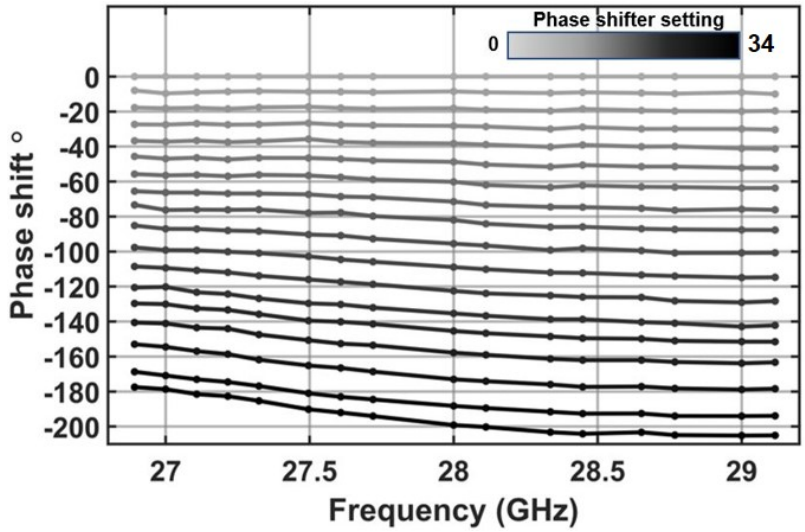


Figure 3.15: Measured phase shift characteristics as a function of frequency.

In order to reduce the rms error in the phase shift resolution, we can pick the 21 best-fit codes that give phase shifts in multiples of 10° and drop the rest of the codes. This amounts to treating the dropped codes as redundancies in the phase shifter that are added to improve the phase shift accuracy. The 21 best-fit codes result in the phase shift characteristics shown in Fig.3.16. The average phase shift resolution is 10° and the rms error is reduced to 1.7°.

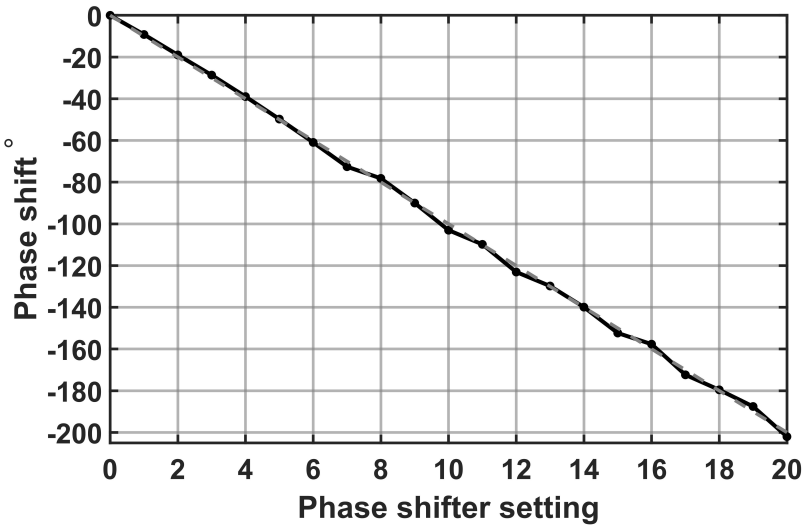


Figure 3.16: Phase shift characteristics for 21 best-fit codes.

3.3 Synthesizer Phase Noise

Figure 3.17 shows the measured phase noise of the synthesizer after frequency division to 7 GHz. The integrated jitter from 1 kHz to 40 MHz is 155 fs. Also shown is the output spectrum of the synthesizer after frequency division to 7 GHz. The reference spur level is -58 dBC at -250 MHz offset. When translated to 56 GHz, i.e. the output frequency of the synthesizer, the estimated spur level should be -40 dBC.

As an indicator for the correct operation of the 56-GHz divide-by-2, the baseband I/Q outputs display amplitude and phase mismatches of 0.7 dB and 8.5°, respectively.

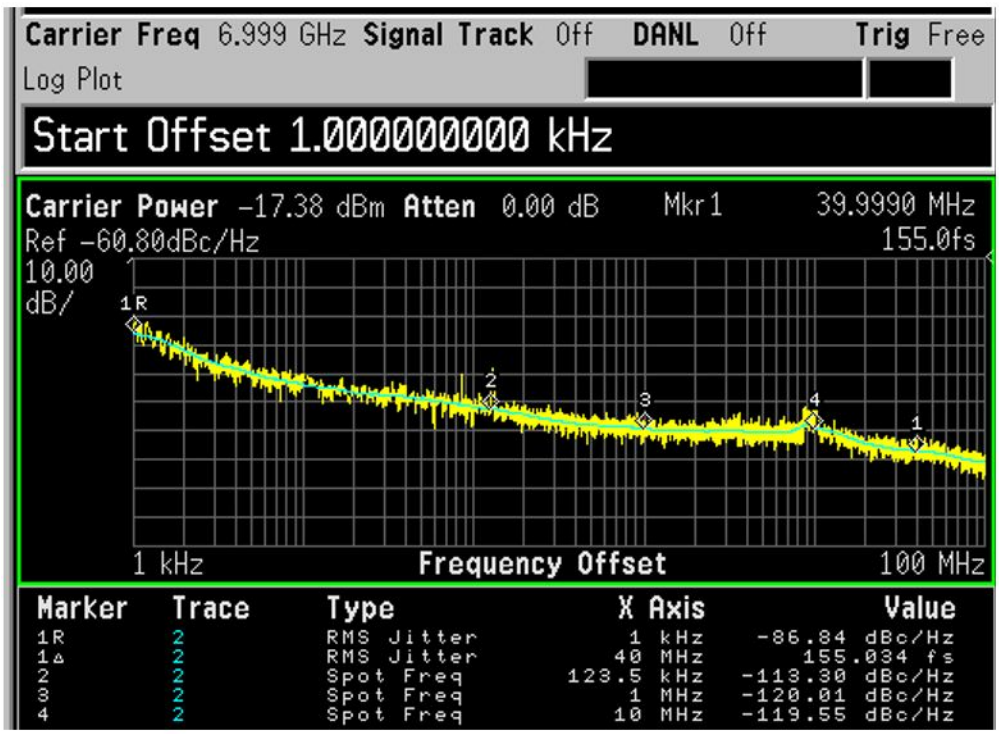


Figure 3.17: Synthesizer phase noise after ÷ 8.

3.4 LO Leakage Cancellation

The LO leakage cancellation circuit is shown in Fig. 3.19. The weight and polarity of a is set by observing the Q channel offset and then setting the value of a appropriately to cancel the Q component of the LO leakage. Similarly, the value of b is set to cancel the I component of the LO

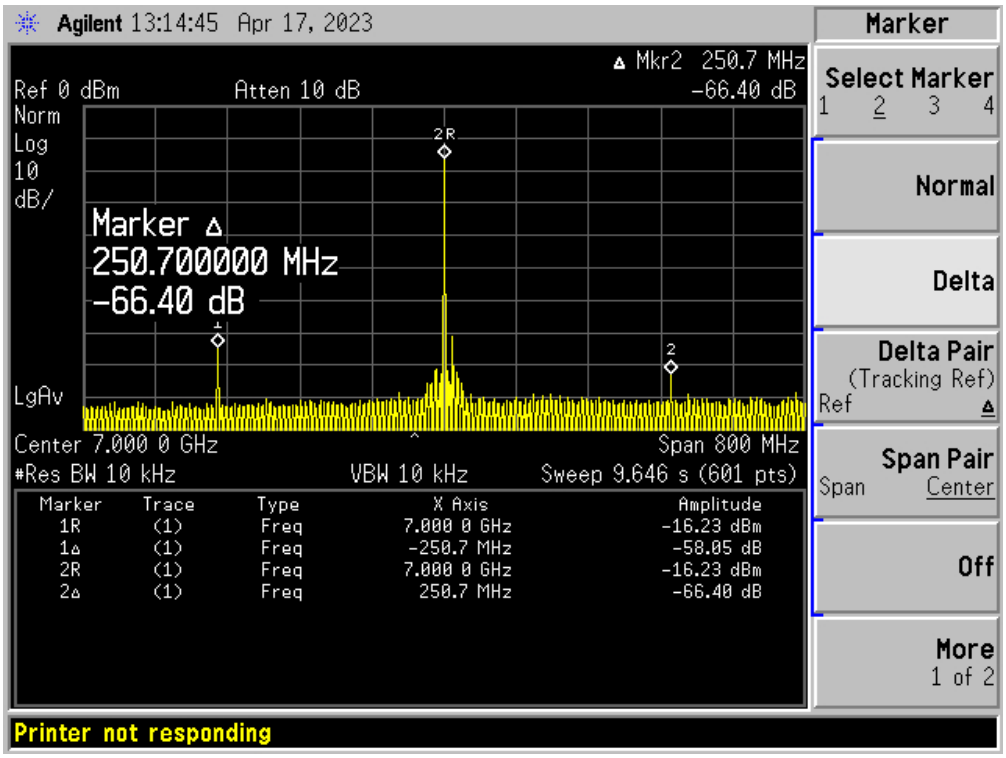


Figure 3.18: Synthesizer spectrum after ÷ 8.

leakage. The offset introduced in the I channel is measured as a function of digital control of b and is depicted in Fig. 3.20. The offset introduced ranges from −151 mV to 148 mV and can be controlled with an eight bits word. Introducing an offset of 148 mV in the I channel only introduces 18 mV offset in the Q channel.

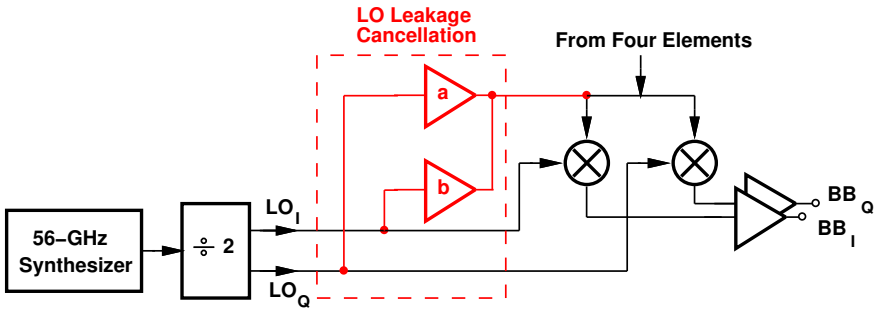


Figure 3.19: LO leakage cancelation circuit.

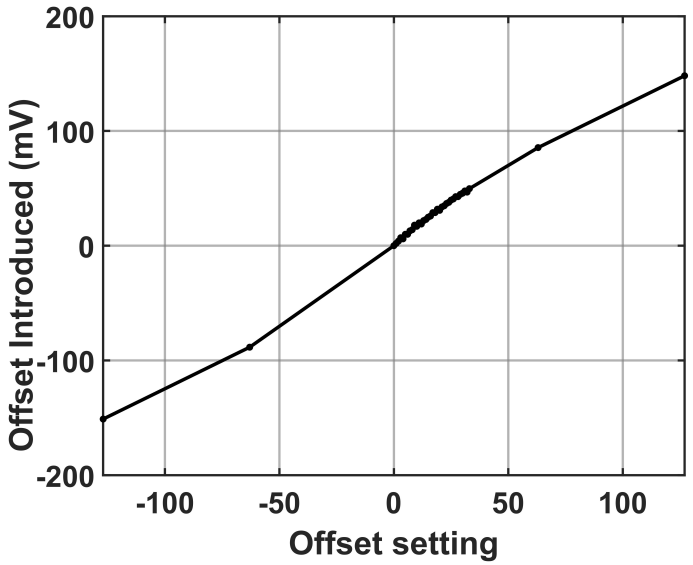


Figure 3.20: Measured I channel offset introduced for different settings of a.

CHAPTER 4

Conclusion

Table 4.1 compares the performance of our prototype RX with the recent state-of-the-art 28-GHz beamforming receivers. For a fair comparison of power consumption, we note that, unlike our RX the references listed in the table do not have complete on-chip LO synthesis. As a result, we also list the power consumption of our RX by subtracting the power consumption of the synthesizer in a separate row. Compared to [6], our RX achieves a factor 2.4x lesser power consumption when operated in the low-power mode in addition to achieving better NF. Compared to [17], our design draws 1.9x lesser power and achieves twice the phase resolution.

	This Work		[6] Mondal JSSC 18	[15] Kim JSSC 18	[17] Yoon RFIC 19
	Low NF	Low Power			
Input Frequency (GHz)	27.3 – 29	27.5 – 29.2	25 – 30	25.8 – 28	26.5 – 29.5
No. of Rx elements	8		8	8	16
NF_{min} (dB)	3.7	6.8	7.3	6.7	3.5
Gain (dB)	31.3 (1 element)	23.4 (1 element)	34 (1 element)	69 (8 elements)	60 (16 elements)
IP_{1dB} (dBm)	-39 (1 element)	-31 (1 element)	-29[a] / -21[b] (1 element)	-68.9[a] / -34.8[b] (8 elements)	-
On-Chip LO Synth.	Yes		No	No	No
Total Power (excl. synth.)(mW)	141*	94*	223*	400*	270*
Total Power (incl. synth.)(mW)	156*	109*	N.A.	N.A.	N.A.
Phase Resolution	10°		N.A.	45°	22.5°
CMOS Technology	28-nm		65-nm	28-nm	28-nm

*For 8 elements [a]High-gain mode [b]Low-gain mode

Figure 4.1: Comparison with state-of-the-art 28-GHz beamforming receivers.

We summarise the key contribution of this work:

1. A new low-power beamforming technique has been proposed that avoids the trade-off between power consumption and phase resolution.

2. The prototype eight-element RX achieves more than 2x reduction in power consumption compared to state of the art.

3. The RX provides phase resolution of 10° with an rms error of 1.7°.

4. We demonstrate complete on-chip LO synthesis.

CHAPTER 5

Appendices

5.1 Appendix A: LC π network with asymmetric capacitances

Figure 5.1 depicts an LC π network where $C_{s1} \neq C_{s2}$. The ABCD matrix for the network is as follows:

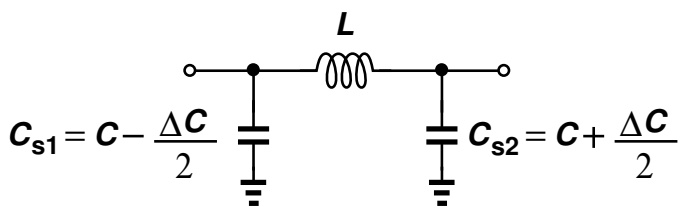


Figure 5.1: LC π network with asymmetric capacitances ($C_{s1} \neq C_{s2}$).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + Z_L Y_{C1} & Z_L \\ Y_{C1} + Y_{C2} + Y_{C1} Y_{C2} Z_L & 1 + Z_L Y_{C1} \end{bmatrix} \tag{5.1}$$

where $Z_L = jX_L = j\omega L$, $Y_{C1} = jB_{C1} = j\omega C_1$, and $Y_{C2} = jB_{C2} = j\omega C_2$, and ω is the angular frequency. The S_{11} is given by:

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} \tag{5.2}$$

Since A and D are unequal, no real-valued Z_0 can make S_{11} equal to 0. However, under the assumption that $\Delta C/C \ll 1$, S_{11} can still be made much smaller than 1 by choosing Z_0 that satisfies: $B/Z_0 = CZ_0$. For such a Z_0 value, S_{11} reduces to:

$$S_{11} = \frac{A - D}{A + 2BZ_0 + D} \tag{5.3}$$

replacing the values of A and D we get:

$$S_{11} = \frac{-\omega^2 L \Delta C}{2 - \omega^2 L \cdot 2C + 2j\frac{L\omega}{Z_0}} \tag{5.4}$$

Since we are interested in the magnitude of S_{11} being low enough to guarantee good matching, the maximum bound on the magnitude of the above expression for S_{11} is calculated as follows:

$$|S_{11}| = \frac{|\omega^2 L\Delta C|}{|2 - 2\omega^2 LC + 2j\frac{L\omega}{Z_0}|} \leq \frac{|\omega^2 L\Delta C|}{|2 - 2\omega^2 LC| + |\frac{2L\omega}{Z_0}|} \leq \frac{|\omega^2 L\Delta C|}{2|1 - \omega^2 LC|} = \frac{|\omega^2 LC|}{2|1 - \omega^2 LC|} \cdot \frac{|\Delta C|}{C} \quad (5.5)$$

The term $\omega^2 LC$ in the above expression, has a special significance. Going back to the case where $C_{s1} = C_{s2} = C$, and replacing for Z_0 from eq. 2.3 in the phase shift expression given by eq. 2.11, the phase shift of the symmetric LC π network can be represented by the following expression:

$$\phi = -2\tan^{-1}\left(\frac{\omega\sqrt{LC}}{\sqrt{2\left(1 - \frac{(\omega\sqrt{LC})^2}{2}\right)}}\right) \quad (5.6)$$

Clearly, $\omega^2 LC$ is a measure of the phase shift. A higher value of $\omega^2 LC$ translates to a greater amount of phase shift. For instance, a phase shift value of 22.5°, 45°, and 90° requires $\omega^2 LC =$ 0.28, 0.54, and 1, respectively. While the above expression is applicable for LC π networks having symmetric capacitances, we would, for now, assume that it holds for asymmetric LC π networks as well under the assumption that $\Delta C/C \ll 1$, and, the assumption will be justified later in this section. Since the LC π networks considered in this work, provide a phase shift lesser than 60° (for reasons discussed in Chapter 2, section 2.1.3), $\omega^2 LC < 0.5$ for such LC π networks. Next, we make another assumption that holds true for the LC π networks considered in this work. The mismatch between C_{s1} and C_{s2} is limited to 20%, implying that $\Delta C/C \leq 0.2$. Under these two assumptions, eq. 5.5 indicates that S_{11} is lesser than -20 dB, for the following value of Z_0:

$$Z_0 = \sqrt{\frac{B}{C}} = \sqrt{\frac{L}{2C\left(1 - \omega^2 L\frac{C^2 - \Delta C^2}{2C}\right)}} \quad (5.7)$$

Next, we turn our attention to the S_{21} of the network given by the following expression:

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \quad (5.8)$$

The above expression is reduced by following steps similar to Chapter 2, section 2.1.1:

$$S_{21} = \frac{1 + \omega^2(C^2 - \Delta C^2)Z_0^2}{1 - \omega^2 Z_0^2(C^2 + \Delta C^2) + 2j\omega Z_0 C} \quad (5.9)$$

If $\Delta C = 0$, S_{21} reduces to the symmetric LC π network element value of $(1 - j\omega Z_0 C)/(1 + j\omega Z_0 C)$. For the asymmetric network, we first find the magnitude of S_{21} which

can be written as:

$$|S_{21}| = \sqrt{\frac{1+\omega^4 Z_0^4(C^4+\Delta C^4-2C^2\Delta C^2)+2\omega^2 Z_0^2(C^2-\Delta C^2)}{1+\omega^4 Z_0^4(C^4+\Delta C^4+2C^2\Delta C^2)+2\omega^2 Z_0^2(C^2-\Delta C^2)}} \tag{5.10}$$

which is clearly only slightly lesser than 1 provided $\Delta C/C \ll 1$. The phase shift provided by the network is given by:

$$\phi = -\tan^{-1}\left(\frac{2\omega Z_0 C}{1-\omega^2 Z_0^2 C^2(1+\Delta C^2/C^2)}\right) \tag{5.11}$$

which is slightly larger in magnitude than the case where $\Delta C = 0$.

The analysis presented is verified by simulations. The S-parameters of a symmetric LC π network [Fig. 5.2(a)] are compared with that of an asymmetric LC π network [Fig. 5.2(b)] having the same mean value of capacitances. The results shown in Fig. 5.3 confirm that the asymmetric network shows very low return loss. The S_{21} for the two cases match very closely.

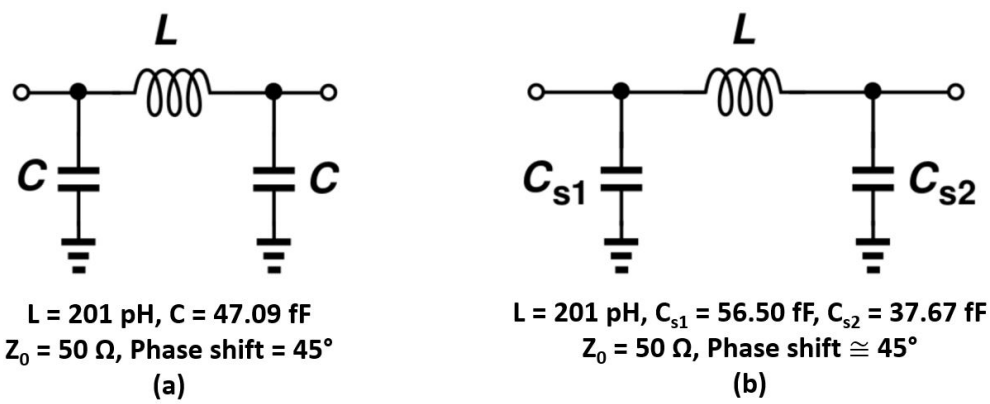


Figure 5.2: Two LC π networks having similar Z_0 and phase shift with (a) symmetric capacitances, and (b) with asymmetric capacitances.

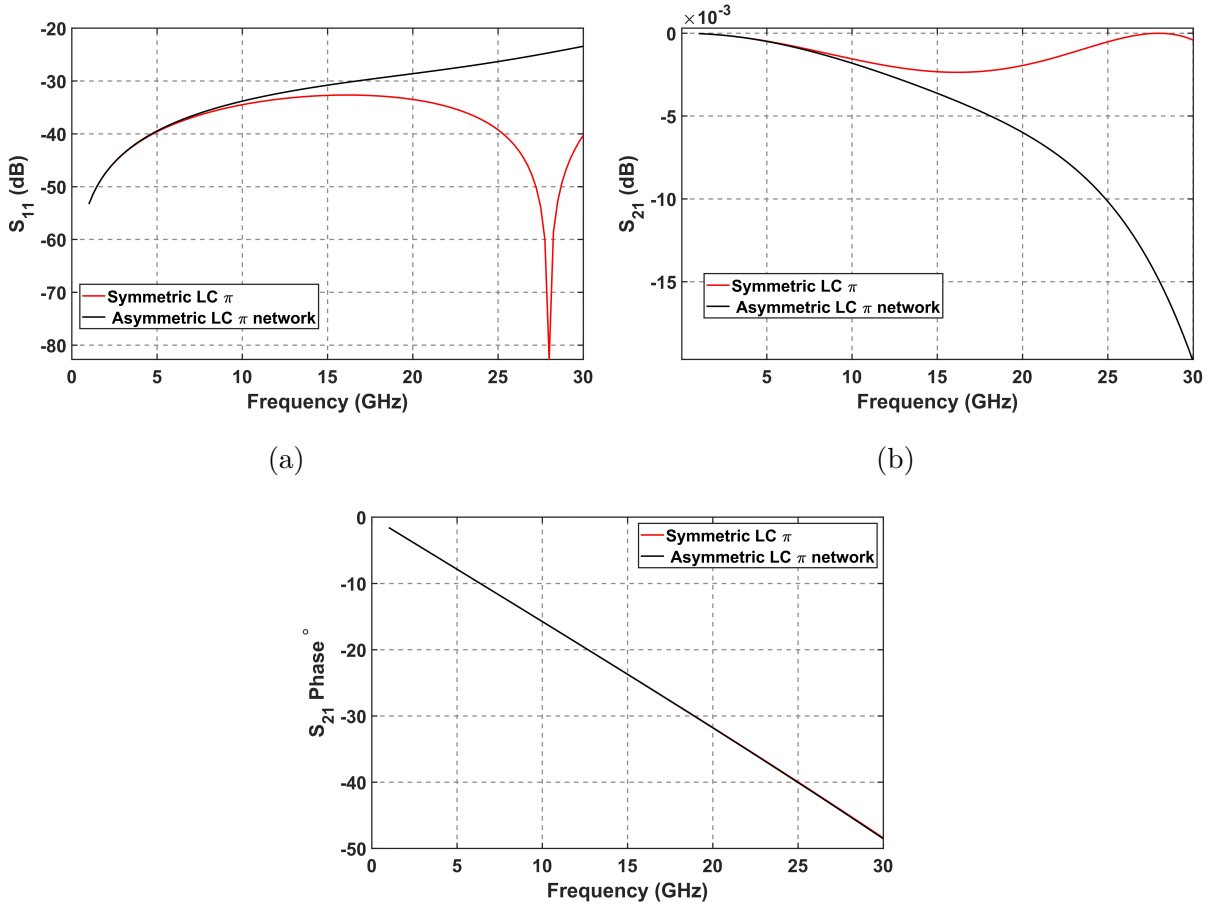


Figure 5.3: Simulated S-parameters for symmetric and asymmetric LC π networks

5.2 Appendix B: LC π network with coupling between adjacent inductors

Figure 5.4 depicts two LC π networks connected in series and with mutual coupling present between the two inductors. The ABCD matrix of the network is as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} Y_C(Z_L+Z_M)+\frac{2Y_C^2 Z_L(Z_L+Z_M)+3Y_C Z_L+Y_C Z_M+1}{1-2Y_C Z_M} & (Z_L+Z_M)\Big(1+\frac{1+2Z_L Y_C}{1-2Z_M Y_C}\Big) \\ Y_C\Big(1+Y_C(Z_L+Z_M)+\frac{2Y_C^2 Z_L(Z_L+Z_M)+5Z_L Y_C+3Y_C Z_M+3}{1-2Y_C Z_M}\Big) & Y_C(Z_L+Z_M)+\frac{2Y_C^2 Z_L(Z_L+Z_M)+3Y_C Z_L+Y_C Z_M+1}{1-2Y_C Z_M} \end{bmatrix}$$

where $Y_C = j\omega C$, $Z_L = j\omega L$, $Z_M = j\omega M$, and ω is the angular frequency. To ensure matching, $S_{11} = 0$, implying that $Z_0^2 = B/C$. Z_0 in terms of L, C, M, and ω is given by:

$$Z_0 = \sqrt{\frac{(L+M)}{C} \cdot \frac{(1-\omega^2 C(L-M))}{(2-\omega^2 C(L-M))(1-\omega^2 C(L+M))}} \tag{5.12}$$

The above expression can be shown to be always greater than the case where M=0, provided (i) $M > 0$, and (ii) $\omega^2 LC < 3$. The second condition is always true as, if $\omega^2 LC \geq 3$, then Z_0 becomes imaginary, implying that the network is no longer capable of transferring power to the load. The preceding analysis proves that positive coupling increases the characteristic

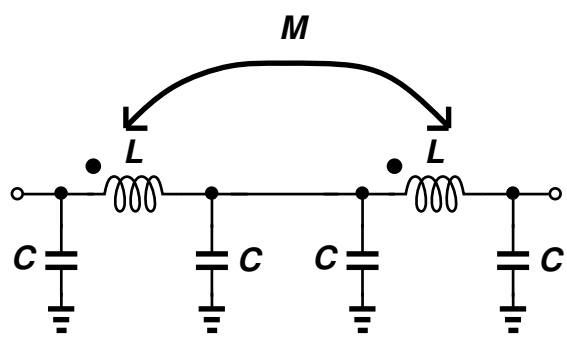


Figure 5.4: LC π network with coupling between adjacent inductors.

impedance of the network. Analyzing the S_{21} is more challenging because of the complicated expressions so we instead resort to simulations. We consider two LC π networks, one without any coupling between adjacent inductors [Fig. 5.5(a)], and the other, with coupling (coupling factor, k = 0.1) between adjacent inductors [Fig. 5.5(b)]. From the expressions for the characteristic impedance, we know that the characteristic impedance for the no coupling case is 50 Ω, whereas, for the case of coupled inductors, the characteristic impedance increases to 53.07 Ω. Figure 5.6 depicts the S_{11}, S_{21}, and also the phase at the intermediate node between the two inductors for both the cases. It can be seen that the phase shift across the network rises by around 2.5° for the case where coupling is present. These results establish the benefits of having coupling, namely, rise in the characteristic impedance value, and rise in the amount of phase shift.

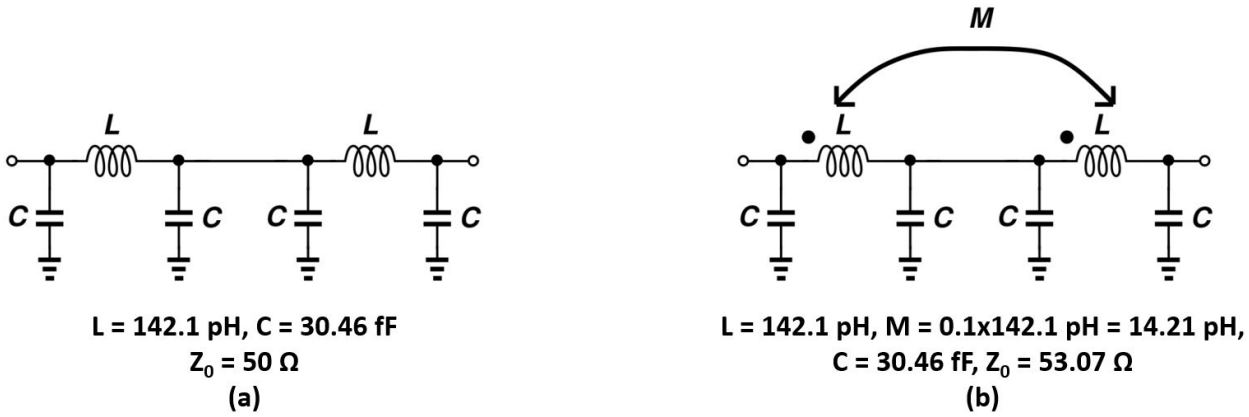
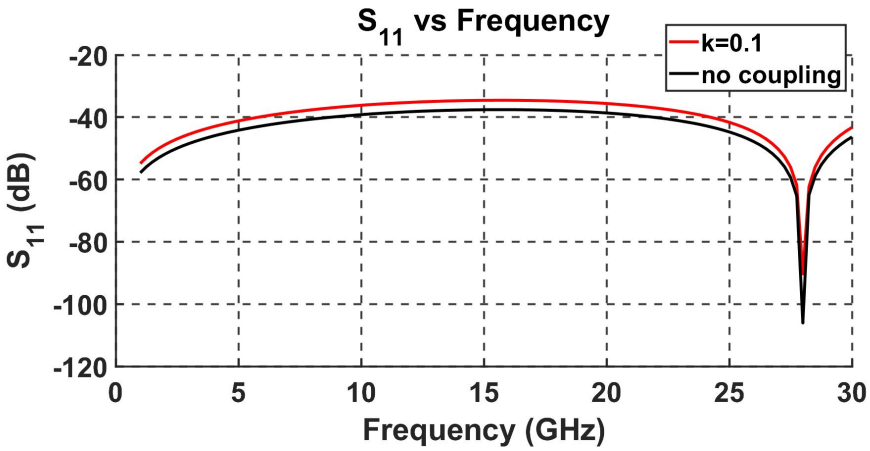
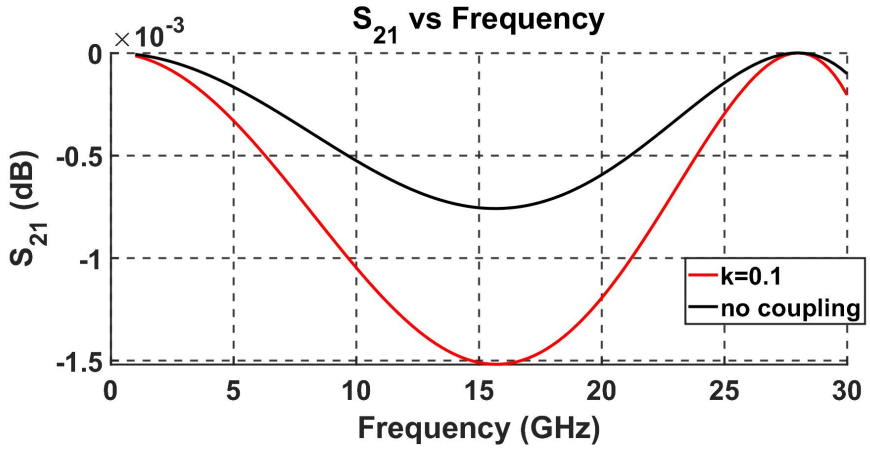


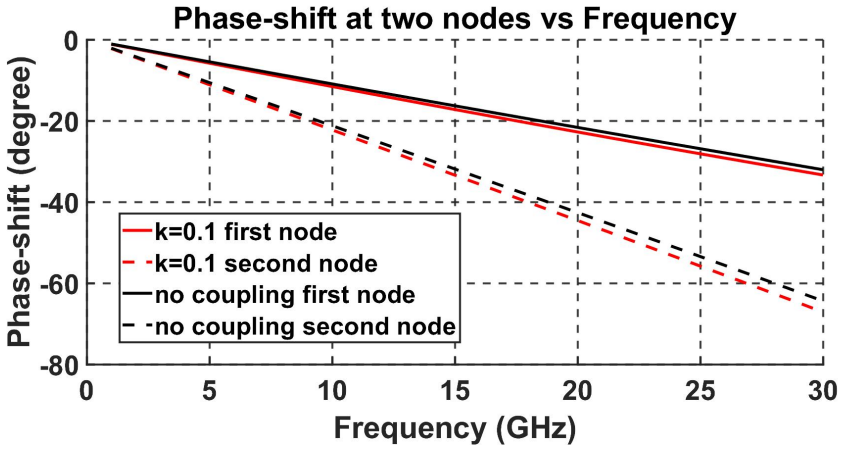
Figure 5.5: Two LC π networks (a) without coupling, and (b) with coupling between adjacent inductors.



(a)



(b)



(c)

Figure 5.6: Simulated S-parameters for LC π networks with and without coupling between adjacent inductors

5.3 Appendix C: NF Measurement for Beamforming RX

The straightforward way to measure the single-element NF of a beamforming RX is to enable only one of the elements and connect it to a noise source. However, instead, if the NF of the RX is measured by connecting a separate noise source to each of the elements, an accurate result for the single-element NF is obtained. We validate this claim by considering a four-element beamforming RX depicted in Fig. 5.7. Each element has a separate LNA. The output signals of the four LNAs are combined. The combined output signal is downconverted by a mixer. The square of the signal voltage level at the input of each element is denoted by S^2. The noise contributed by the antenna at the input of the ith element is denoted by $4kTR_{s,i}\ V^2/Hz$. The voltage gain of the LNA is G_{LNA} and the output thermal noise of the ith element LNA is $\overline{V^2_{LNA,i}}\ V^2/Hz$. The voltage gain and the output thermal noise of the mixer are denoted by G_{Mix} and $\overline{V^2_{Mix}}\ V^2/Hz$ respectively. The NF of the RX is given by the ratio of the SNR at the input of a single element to the SNR at the output:

$$NF = \frac{S^2}{4kTR_sB} \div \frac{n^2 \cdot S^2 \cdot G^2_{LNA} \cdot G^2_{Mix}}{n \cdot 4kTR_sB \cdot G^2_{LNA} \cdot G^2_{Mix} + n \cdot \overline{V^2_{LNA}} \cdot B \cdot G^2_{Mix} + \overline{V^2_{Mix}} \cdot B}, \quad (5.13)$$

where n denotes the number of elements (four for this example), B denotes the signal bandwidth, and the noise level of all the antennas is denoted by $4kTR_s\ V^2/Hz$, and similarly, the output noise level of all the LNAs is denoted by $\overline{V^2_{LNA}}\ V^2/Hz$. On simplifying:

$$NF = \frac{1}{n}\left(1 + \frac{\overline{V^2_{LNA}}}{4kTR_s \cdot G^2_{LNA}} + \frac{\overline{V^2_{Mix}}}{n \cdot 4kTR_s \cdot G^2_{LNA} \cdot G^2_{Mix}}\right) \quad (5.14)$$

Noting that the NF of the standalone LNA is given by $\overline{V^2_{LNA}}\ /\ 4kTR_s \cdot G^2_{LNA}$ and that of the mixer is $\overline{V^2_{Mix}}\ /\ 4kTR_s \cdot G^2_{Mix}$, we denote these expressions as NF_{LNA} and NF_{Mix}. The expression for the RX NF simplifies to:

$$NF = \frac{1}{n}\left(1 + (NF_{LNA} - 1) + \frac{NF_{Mix} - 1}{n \cdot G^2_{LNA}}\right) \quad (5.15)$$

The $1/n$ term in the above expression accounts for the reduction in NF due to n-element beamforming. The rest of the expression, within the brackets, can be defined as the NF of a single element. Interestingly, while calculating a single-element NF, the contribution of the mixer's NF gets divided by $n \cdot G^2_{LNA}$. This suggests that when the output noise of any block in the signal path, that is placed after signal combining, gets referred to the input of a single element, it gets divided by n. It is important to recognize the reduction by a factor of n in the mixer's noise contribution when referred to the input of a single element as this leads to a lower gain requirement from the LNA, allowing a reduction in its power consumption.

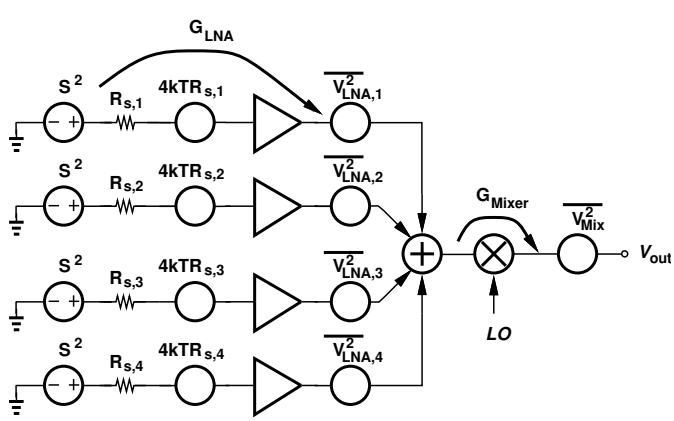


Figure 5.7: A four-element RX model for NF calculation

We now show that if the NF of the above RX is measured by connecting four independent noise sources to the four elements, as shown in Fig. 5.8, we get the NF of a single element as defined above. The Y-factor method measures the NF by dividing the output noise density due to the DUT and the noise sources, with the output noise density only due to the noise sources. The NF calculated by this method is given by the following expression and is equal to the single-element NF:

$$\begin{aligned} NF &= \frac{n \cdot 4kT_cR_s \cdot G_{LNA}^2 \cdot G_{Mix}^2 + n \cdot \overline{V_{LNA}^2} \cdot G_{Mix}^2 + \overline{V_{Mix}^2}}{n \cdot 4kT_cR_s \cdot G_{LNA}^2 \cdot G_{Mix}^2} \\ &= 1 + (NF_{LNA} - 1) + \frac{NF_{Mix} - 1}{n \cdot G_{LNA}^2}, \end{aligned} \tag{5.16}$$

where T_c is the cold temperature of the noise source. On the other hand, the conventional setup for measuring NF, shown in Fig. 5.9, results in the following measured NF which does not account for the 1/n factor in the noise contribution of the mixer referred to the input of a single element.

$$NF = 1 + (NF_{LNA} - 1) + \frac{NF_{Mix} - 1}{G_{LNA}^2}, \tag{5.17}$$

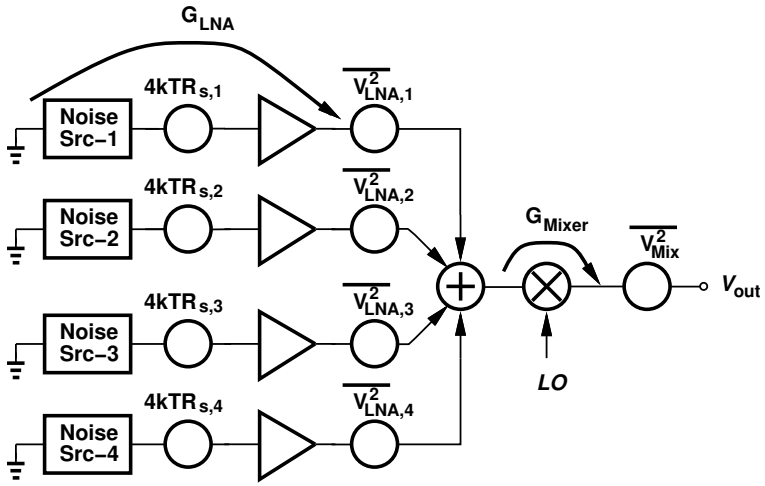


Figure 5.8: Proposed measurement setup for single-element NF

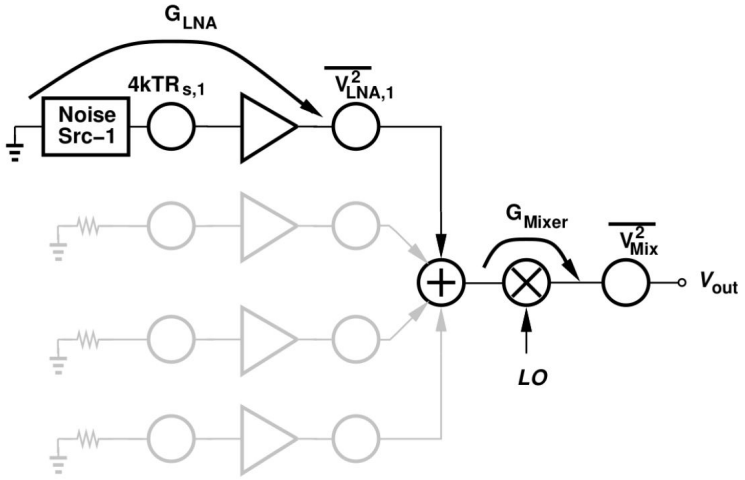


Figure 5.9: Conventional measurement setup for single-element NF

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