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Amplitude-to-RF and Phase-to-RF Time Alignment in Microwave Outphasing Modulators

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by

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The thesis of Jinous Valizadeh is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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University of California, San Diego

2016

DEDICATION

To my parents - Mrs. Tohfeh Samandary and Mr. Mehran Valizadeh

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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ABSTRACT OF THE THESIS

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Many phase modulation schemes generally rely on phase-to-RF and amplitude-to-RF modulation alignment. Splitting a signal into amplitude and phase components and feeding them into separate paths potentially has major advantages. While theoretically achievable, amplitude and phase modulation time alignment remains a challenge.

One of the phase modulation schemes is outphasing. Outphasing, also known as linear amplification with nonlinear components (LINC), improves the efficiency while maintaining linearity. To do so, any arbitrary signal splits into amplitude and phase. Then outphasing modulator generates two constant enve-

lope phase modulated vectors also known as outphasing signals. Since outphasing signals are constant envelope, they can be fed into high-efficiency switching mode power amplifiers (PAs). Therefore, efficiency improves without degrading the linearity. Recombining the amplified outphasing signals after PAs, restores the phase and amplitude of the desired output signal. In this scheme, splitting the input signal into amplitude and phase is handled in digital domain thus reducing the risk of time mismatch between amplitude-to-RF and phase-to-RF modulation. However, outphasing modulator requires four digital-to-analog converters (DACs).

In this thesis an alternative approach is proposed that requires only two DACs, similar to envelope tracking, however it does not suffer from time mismatch. Also, a digital phase modulator based on coupled oscillator outphasing modulator is designed. In this design, varactor inside the oscillators is replaced with an 8-bit cap bank, therefore there is no need for any additional DACs.

A 10-GHz modulator is designed in 45-nm CMOS SOI and output vectors demonstrate close to 360 degrees of phase coverage.

Chapter 1

Introduction

Large volume of wireless communication has increased the demand for high-speed modulations since there is an increasing demand for large volume real-time data transfer. There are two ways to increase the data-rate in a wireless communication. Firstly, by operating at a higher bandwidth (BW). Fig. 1.1 compares the output spectrum of a narrowband application with a wideband modulation. There are many applications at lower frequencies, therefore not much available spectrum. In order to increase the BW, designers are forced to move up to higher frequencies. For example, around 2 to 3GHz designers are limited to channels with only 20MHz BW, while it can increase to 500MHz at higher frequencies.

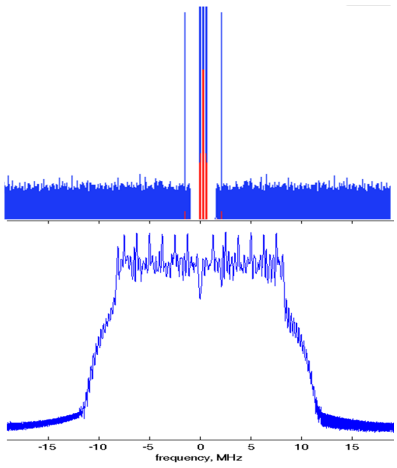

Figure 1.1: Narrowband versus wideband spectrum.

This thesis focuses on X-band (8GHz - 12GHz) at 10GHz frequency. As it was mentioned earlier, higher BW is available at this frequency range which means higher data-rate communications is achievable. Fig. 1.2 shows two of the main applications of this band, namely radar and satellite communications [5].

Figure 1.2: Radar and satellite communications.

A second method to increase the data-rate is to use the available BW more efficiently. In other words, there is an ongoing effort to increase the number of symbols in constellation in order to have higher data-rate for high speed communications. Fig. 1.3 demonstrates the constellations for QPSK, 16-QAM, and 64-QAM waveforms.

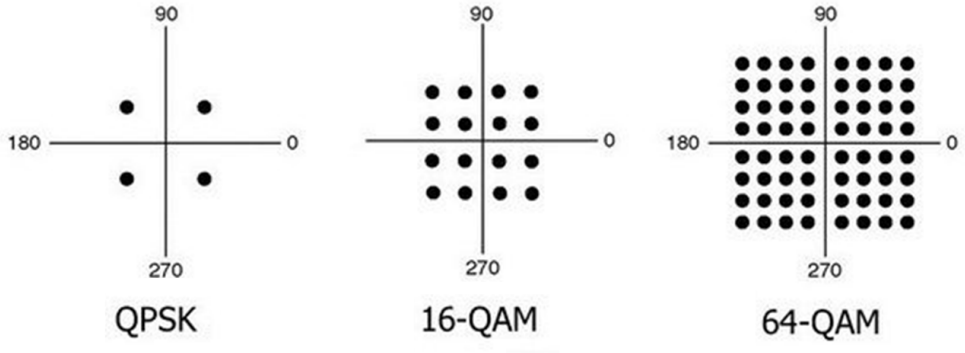

Figure 1.3: QPSK, 16-QAM, and 64-QAM constellations.

Higher order modulation results in a larger peak-to-average power ratio (PAPR), and high PAPR modulation requires high linearity PAs. In modern wireless communications PAPR sometimes exceeds 8 dB, which imposes strict restrictions on linearity. It forces the power amplifiers (PAs) to operate in back-off region

and as a result the system efficiency will be low [6]. There is also a well-known trade-off between linearity and efficiency in PAs. On one side there are linear PAs, such as class A and Class AB with low efficiency, and on the other side there are switching mode PAs such as class E and class F with high efficiency and poor linearity. While switching mode PAs are good candidates for phase and frequency modulations, due to their low linearity, it can be a challenge to use them for amplitude modulations such as QAM. There are a couple of techniques to utilize high efficiency switching mode PAs while maintaining linearity for phase modulation such as envelope tracking and outphasing modulator. Table. 1.1 shows the trade-off between linearity and efficiency for different PA classes of operation.

Table 1.1: Trade-off between linearity and efficiency in PAs.

$PA-Type$	$Linearity$	$Efficiency$	$Modulation$
Linear (A, AB,...)	high	low	Amplitude
Switching (E,F,...)	low	high	Phase, Frequency

As was mentioned earlier, envelope tracking is one of the techniques to improve the efficiency while maintaining the linearity [7–17]. An envelope tracking approach contains two paths from input to output. One path is for the RF signal itself and another one for the amplitude of the input signal. Block diagram of an envelope tracking PA is shown in Fig. 1.4 [1].

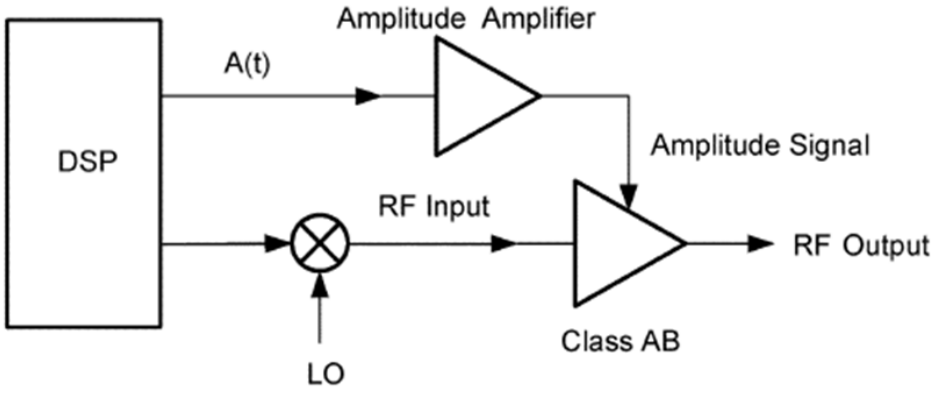

Figure 1.4: Block diagram of an envelope tracking power amplifier [1].

The main path includes a linear power amplifier and the second path is dedicated to set the supply voltage of the PA based on the input signal. The second path also detects the envelope of the signal and adjusts the supply voltage to increase the voltage only when it is necessary, therefore ensuring the high efficiency. So, this technique utilizes a linear PA and a controlled supply voltage which tracks the signal envelope. Therefore, voltage supply of the power amplifier dynamically changes with the input signal envelope and the RF transistor operates with a higher efficiency over a wide dynamic range of the output power [18]. Time alignment between these two paths is critical especially at higher bandwidths, and it is one of the important challenges of this technique. In envelope tracking, calibration is required to make sure RF amplification and Vdd modulation are synced. Also, this structure requires only two DACs, one for the envelope and another for the signal itself, which is an advantage of this technique compare to other techniques that require more DACs such as outphasing modulator.

Another technique to improve the efficiency while maintaining the linearity is outphasing modulation, which is also known as linear amplification with nonlinear components (LINC) [19–32]. Outphasing is an alternative to envelope tracking technique with some advantages and disadvantages. Block diagram of an outphasing system is shown in Fig. 1.5 [2].

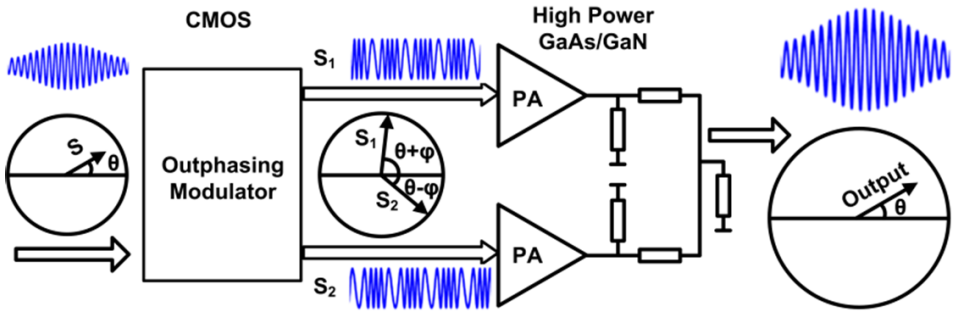

Figure 1.5: Block diagram of an outphasing modulator [2].

In an outphasing modulator, a complex signal splits into two constant-envelope, phase-modulated signals by separating the input signal into amplitude and phase components in a digital domain. As a result, high-efficiency switching mode PAs can be used to amplify the generated RF signals with constant

envelope and different phase to improve the efficiency without degrading the linearity [33], [34], [35–38], [39–41]. Then, to generate the desired output signal, the amplified signals are recombined to restore the amplitude and phase components of the output signal. One advantage of the outphasing modulation technique over envelope tracking is that phase and amplitude information travel the same paths from baseband to RF. This happens due to the fact that signal decomposition is handled in digital domain, therefore timing requirements at baseband and RF are relaxed, which means time alignment between amplitude-to-RF and phase-to-RF modulation is not an issue anymore. However, the downside of an outphasing approach compared to envelope tracking is that it requires four DACs, thus contributing to greater area and power consumption.

In this thesis a phase modulator based on injection-locking coupled-oscillators is discussed offering the same phase-to-RF and amplitude-to-RF timing while only requiring two DACs. Chapter 2 presents the background of this work and includes phase modulator based on injection-locking coupled-oscillators. Chapter 3 presents the proposed approach to relax the phase and amplitude time alignment in baseband and RF. In chapter 4 it is shown that varactor in oscillators can be replaced with cap bank to incorporate DACs into the phase modulator. Finally, chapter 5 concludes the thesis.

Acknowledgment

Some parts of this chapter are adopted from [3] and [18].

Chapter 2

Coupled Oscillator Outphasing Modulator with Analog Phase Modulation

2.1 Outphasing Modulation and Injection Locking

2.1.1 Outphasing Modulation

Outphasing modulation is a technique to generate a pair of constant envelope signals and allows PAs to operate at their peak efficiency while still generating complex waveforms (as shown in Fig. 2.1).

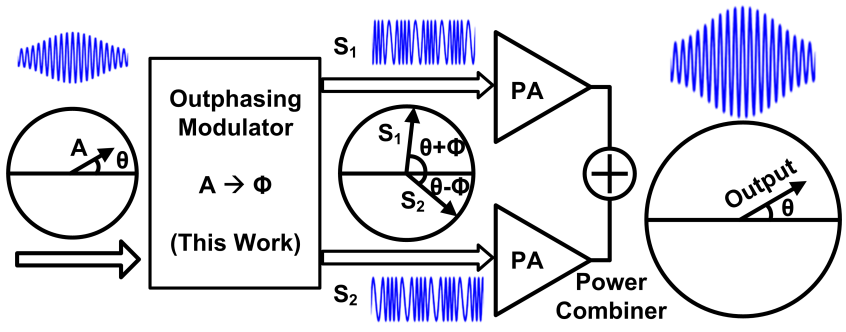

Figure 2.1: Outphasing modulation [3].

This technique increases the transmit efficiency and requires the transformation of a cartesian (I and Q) message to polar coordinates (A and θ) as well as the additional transformation of the amplitude to an outphasing angle (A-to-ϕ) [3]. Conventional outphasing generates outphasing signals using a dual channel I/Q modulator. Each of the channels requires two DACs and a quadrature upconverter to generate one of the outphasing signals. Therefore, it generates S_1 with I_1+Q_1 and S_2 with I_1+Q_1, as shown in Fig. 2.2. Since all of the 4 signals are applied to the system simultaneously and they travel similar paths from baseband to RF, time alignment here is not a challenge for outphasing modulator technique.

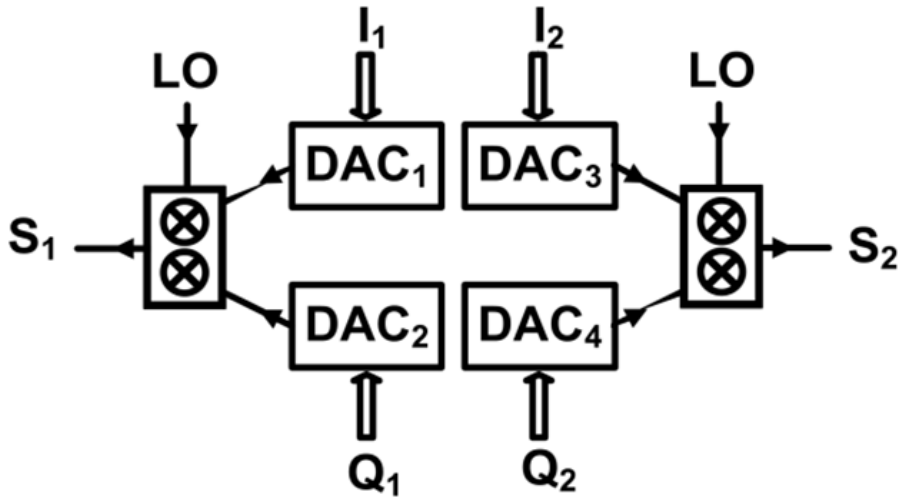

Figure 2.2: Dual channel I/Q modulator [4].

In outphasing modulator a complex waveform with amplitude and phase modulations can be represented as $S(t) = A(t)\cos(\omega t + \theta(t))$ which can be transformed to a pair of outphasing signals such as $S_1(t)$ and $S_2(t)$ with constant envelope and outphasing angle of ϕ as $S_1(t) = \frac{1}{2}A_{max}\cos(\omega t + \theta(t) + \phi(t))$ and $S_2(t) = \frac{1}{2}A_{max}\cos(\omega t + \theta(t) - \phi(t))$ as shown in Fig. 2.1. The outphasing angle can be calculated

$$\phi(t) = \arccos\left(\frac{A(t)}{A_{max}}\right), \tag{2.1}$$

where $A_{max} = \max(A(t))$ and $-90^\circ \leq \phi \leq +90^\circ$ [4]. The delivered Output power changes as the maximum amplitude of the input signal changes since the signal power is proportional to the $A^2(t)$. Output signals of the two PAs are out-of-phase when the amplitude is minimum. In this case since the outphasing angle is $\pm 90^\circ$, it results in a complete cancellation of the output signals of $S_1(t)$ and $S_2(t)$. On the other hand, the output signal from two PAs are in-phase when the amplitude of the input signal is at the maximum, since the outphasing angle is zero, $S_1(t)$ and $S_2(t)$ combine in-phase and the power from the two channels add together. Delivered output power is

$$P_O = P_{max} \frac{1 + \cos 2\phi}{2}, \tag{2.2}$$

where P_{max} is the maximum output power [4]. As the outphasing angle changes from 0° to 90°, the output power drops from the maximum power to the minimum power. If we substitute (2.1) into (2.2), the output power is dependent on $A^2(t)$. Notably, the efficiency of outphasing modulation depends on the load modulation that is performed through the output power combiner.

2.1.2 Injection Locking

The goal of injection locking is to lock an oscillator to a source by injecting signal from the source to the oscillator so that the frequency of the oscillator locks to the source which results in a phase shift. In order to generate phase shift, the frequency detuning $\Delta\omega$ between the injected frequency ω_i and the natural frequency of the oscillator ω_n should be within the locking range. When $\Delta\omega$ is within the locking range of the oscillator ω_L, then oscillator frequency locks to the injected frequency with a phase shift of

$$\psi = \arcsin\left(\frac{\omega_n - \omega_i}{\omega_L}\right) = \arcsin\left(\frac{\Delta\omega}{\omega_L}\right). \tag{2.3}$$

Therefore, a maximum $\pm 90^\circ$ of phase shift will be produced if the frequency detun-

ing is within the locking range of the oscillator. The locking range of the oscillator is $\omega_L = \frac{2}{Q}\frac{I_{inj}}{I_{osc}}\omega_o$, and to derive (2.3) I_{inj} is assumed to be considerably smaller than I_{osc} [42–44]. ω_L is directly related to the circuit parameters af Q which is the quality factor of the resonator, I_{inj} is the injected current, and I_{osc} is the oscillator current swing.

There are two main reasons that make locking range an important parameter: Firstly, it clearly controls the range of the frequency detuning over which the oscillator will remain locked. Secondly, the locking range determines the time constant for the response of the oscillator to an external perturbation. This means that the locking range determines the bandwidth of the modulator. So, injected current can be used to control the locking range which will lead to also controlling the bandwidth when the Q of the tank is fixed. Typically, the locking range is around 10% of the oscillation frequency. Voltage controlled oscillators (VCOs) are tuned over a certain frequency range. Output frequency of VCOs varies linearly over a limited range of applied control voltage V_{tune}. Since $\omega n = \omega_o + K_V V_{tune}$ and $\omega_o = \omega_i$ then the frequency detuning will be $\Delta\omega = K_V V_{tune}$. In this case two voltage controlled oscillators (VCOs) are coupled through a resistive network while VCOs are tuned differentially through a differential control voltage $\pm V_{tune}$ as shown in Fig. 2.3.

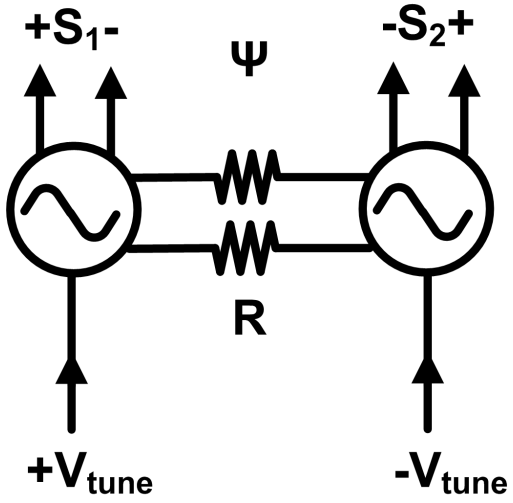

Figure 2.3: Coupling two VCOs through resistors [3].

If the resistive network is large enough to guarantee $I_{inj} \ll I_{osc}$, then phase between the two oscillators will be

$$\psi = \arcsin\left(\frac{K_V V_{tune}}{\omega_L}\right). \tag{2.4}$$

given that $V_{max} = \frac{\omega_L}{K_V}$, then phase shift between two coupled VCOs produces an arcsine function

$$\psi = \arcsin\left(\frac{V_{tune}}{V_{max}}\right). \tag{2.5}$$

There are two major differences comparing (2.1) and (2.5) that need to be considered to get the same results as outphasing modulation technique. First, the range of phase variations for two coupled VCOs is half of the required phase variations in an outphasing modulator. Second, the outphasing angle is an arccosine function of the amplitude while coupled VCOs provide an arcsine function of the injection locking amplitude. In order to overcome the first issue, three VCOs are coupled to double the phase variation range so that the edge VCOs can cover the $\pm 180^\circ$ range which maps to the $\pm 90^\circ$ range of outphasing angle. Phase between the two edge VCOs will be

$$\measuredangle S_{1+} - \measuredangle S_{2+} = 2\psi = 2\arcsin\left(\frac{V_{tune}}{V_{max}}\right). \tag{2.6}$$

Fig. 2.4 shows three coupled VCOs block diagram.

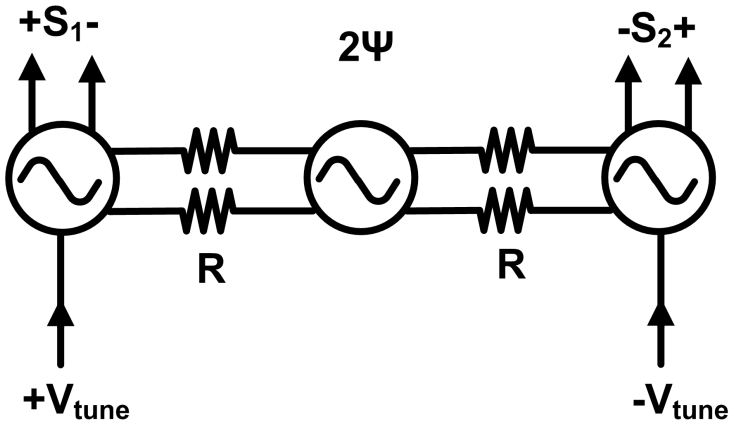

Figure 2.4: Coupling three VCOs through resistive network to double the phase range [3].

Second problem can be solved by combining the differential output signals from the edge VCOs with the opposite sign. In other words, $\measuredangle S_2-$ can be defined as a function of $\measuredangle S_2+$ by defining $\measuredangle S_2- = \pi + \measuredangle S_2+$ and by substituting $\measuredangle S_2-$ into (2.6) it can be shown that

$$\measuredangle S_{2-} - \measuredangle S_{1+} = \pi - 2\arcsin\left(\frac{V_{tune}}{V_{max}}\right) = 2\arccos\left(\frac{V_{tune}}{V_{max}}\right). \tag{2.7}$$

Therefore, by taking advantage of the nonlinear characteristics of the injection locked oscillator, and combining the right sign of the edge VCOs, differential output signals of the outphasing angle can be produced without the need for digital signal processing. This results in much lower power outphasing modulation for high bandwidth signals [3].

2.2 Circuit Implementation of the Injection Locking Outphasing Modulator

In the previous section application of injection locking to produce outphasing signals was introduced. In this section block diagrams of the implemented proposed outphasing modulator, and critical building blocks of the design are demonstrated. Block diagram of the proposed coupled oscillator outphasing modulator has shown in Fig. 2.5.

Block diagram of the coupled oscillator outphasing modulator consists of three VCOs which are coupled through a resistive network in series. A central VCO is coupled to an external oscillator which provides frequency control that locks the central VCO to the external source as well as θ of the input signal by injecting the common mode phase modulation reference signal into the central VCO. Then, conversion of the amplitude to outphasing angle is provided by detuning the edge VCOs differentially. Differential tuning signals $A(t)$ and $-A(t)$ are applied to the edge VCOs and results into the phase difference between the edge VCOs which is a function of the amplitude of the input signal. Edge oscillators are followed

by doublers to double the frequency and also the phase range. This removes the stress from the edge VCOs and there will be no need to push them to the edge of instability to get $\pm 180^\circ$ phase shift.

This structure, similar to the envelope tracking, requires only two DACs. This is an advantage compared to the conventional outphasing modulator. However, this structure does not offer a synced amplitude-to-RF and phase-to-RF modulation unlike the conventional outphasing modulator. In other words, similar to the envelope tracking, calibration needs to be done to make sure envelope and phase (θ) reach the output simultaneously.

As Fig. 2.5 shows, critical blocks of the coupled oscillator outphasing modulator are oscillators, doublers, and single-ended-to-differential converters. Designs of these blocks are discussed in the following sections.

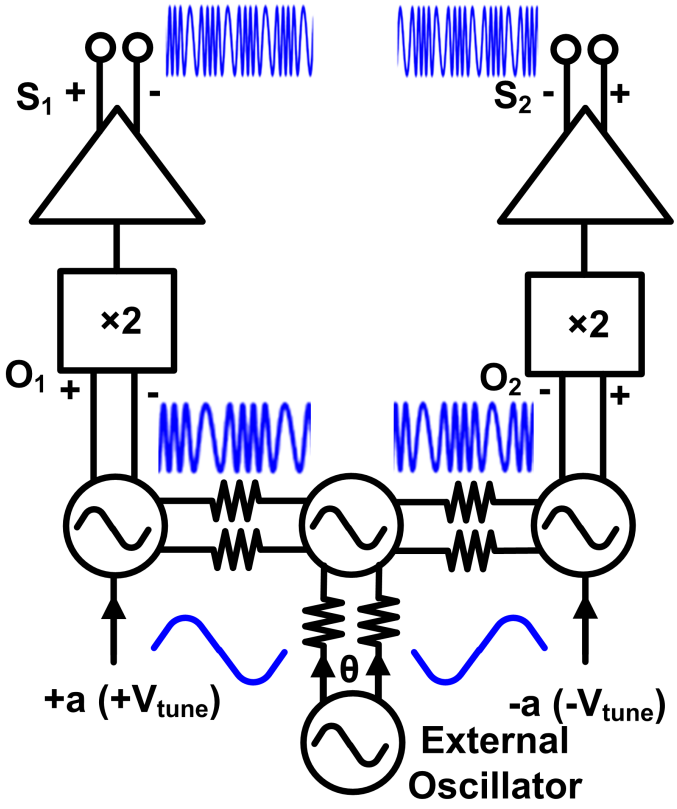

Figure 2.5: Block diagram of the proposed coupled oscillator outphasing modulator [3].

2.2.1 Frequency Multiplication

Even though the outphasing angle is being produced by using injected coupled oscillators, it is still difficult to cover the full 180 degrees of phase shift by coupling three VCOs. Sensitivity of the circuit to noise could cause cycle-slipping behavior near the edge of the locking range [44] which then causes the edges of the injection locked oscillator tuning range not to be practical regions of the operation. So, to solve this issue and prevent the outphasing limitation angle as it has been presented in previous work on coupled oscillators, the use of multiplier to increase the phase variation was suggested [45]. Given that V_{tune} the phase shift can be found as (2.8) where M is the frequency multiplication factor, and in this case a factor of 2 is needed to provide the required margin for an outphasing modulator.

$$\phi = M \arccos\left(\frac{V_{tune}}{V_{max}}\right), \tag{2.8}$$

One of the down sides of using a frequency multiplier is that not only the phase and frequency will be multiplied, but also the phase noise from oscillators will be multiplied. However, this issue can be solved with a low phase noise external reference which also helps to make sure that the phase noise of the edge oscillators is suppressed within the locking bandwidth [46].

Doubler output signal is single-ended. However, as it was shown in the previous section, differential output is required to convert the arcsine function to arccosine function. Therefore, in this design doublers are followed by single-ended-to-differential active balun circuits which are designed to provide enough gain since the frequency doubler is lossy and therefore active balun will compensate the loss of the frequency doubler. As shown in Fig. 2.6, adding the doubler has increased the phase range, however, simulations shows it is less than double and that is because as soon as doublers are loading the oscillators then the locking range reduces.

From simulation results as shown in Fig. 2.6, even the phase range has not been doubled after adding doublers, but required phase variation needed for full outphasing has been provided by frequency detuning.

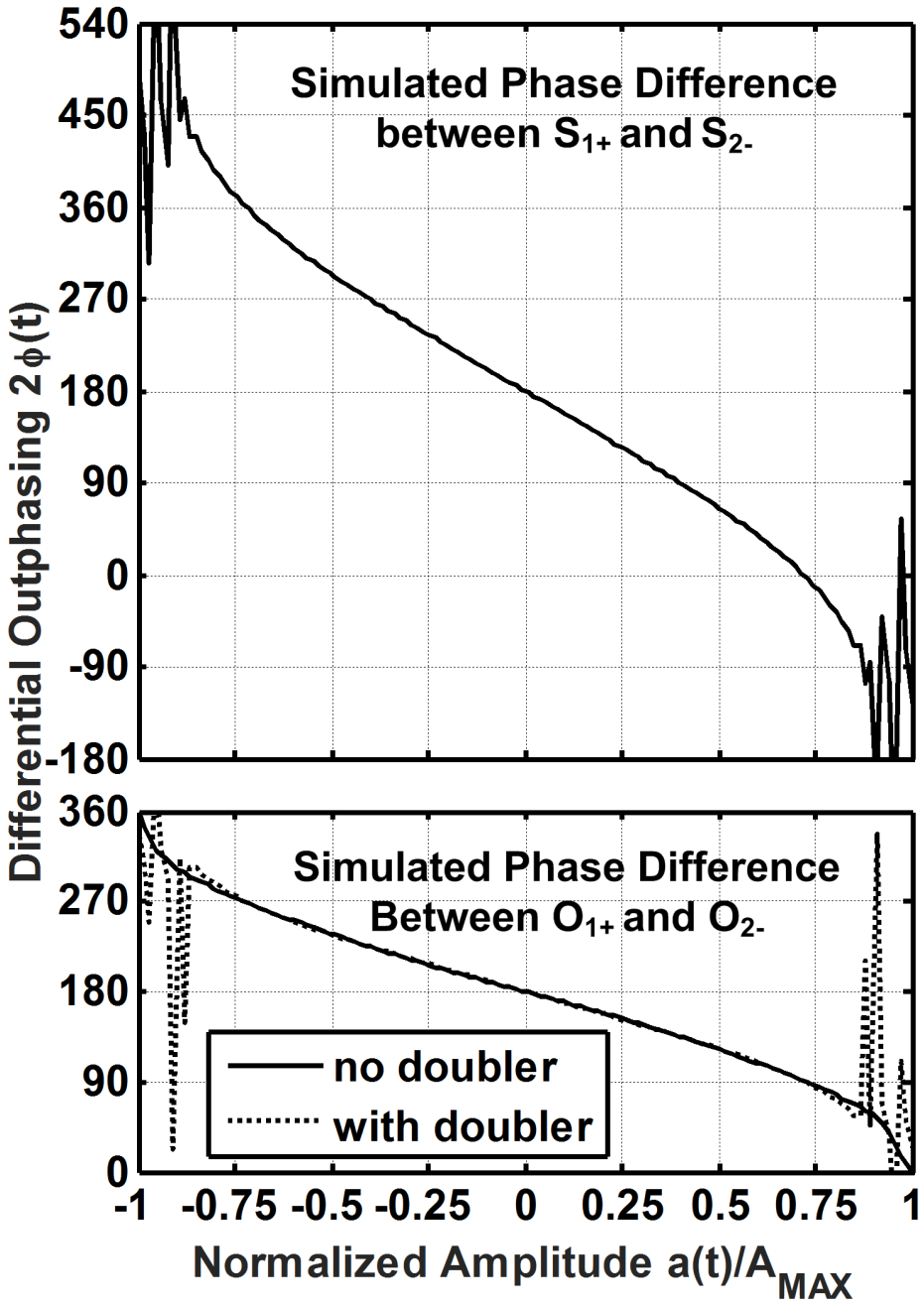

Figure 2.6: Simulated phase at the output of the coupled oscillators as well as doublers. [3]

2.2.2 Oscillator

A cross-coupled LC oscillator is designed as shown in Fig.2.7.

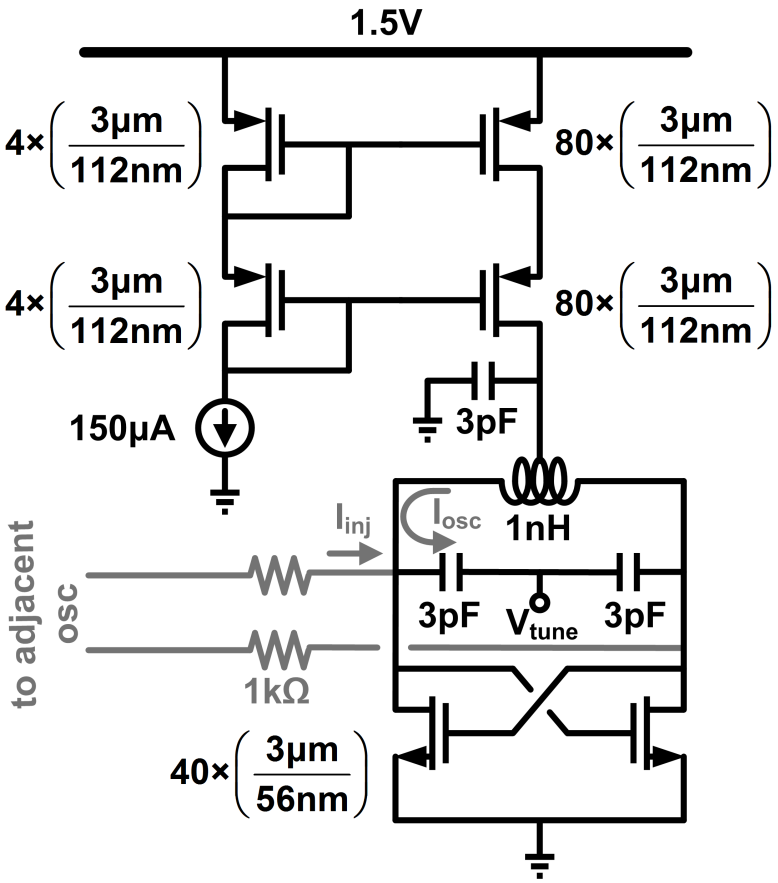

Figure 2.7: Schematic of the designed cross-coupled LC oscillator at 5GHz. [3]

To improve the Flicker noise, a PMOS current source is used and to increase its output resistance a cascode structure is used. Typically, metal-insulator-metal (MIM) capacitors are used since they have a high quality factor Q. In that case, a cap bank with discrete tuning steps would be designed. In this design, however, due to the analog nature of the phase modulation, an analog approach is pursued with the use of varactors. Metal-Oxide-Semiconductor (MOS) capacitors are used in the tank of the oscillator to tune the frequency. As shown, resistive coupling network used to connect oscillators.

2.2.3 Frequency Doubler

After each oscillator there is frequency doubler that its schematic is shown in Fig. 2.8.

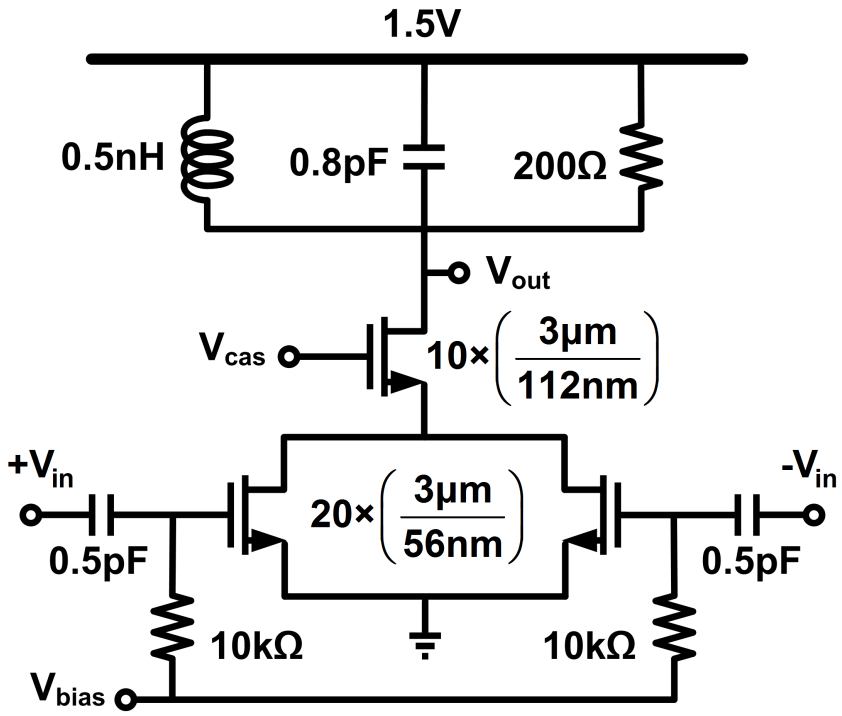

Figure 2.8: Schematic of the designed frequency doubler with differential 5GHz input and signle-ended 10GHz output. [3]

The doubling pair is biased to maximize the second order nonlinearity [47] since the edge oscillators are followed by doublers to double the frequency and also the phase range. To improve the output-to-input isolation a cascode device is placed on top of the input pair. An LC resonator with 10 GHz resonant frequency is placed at the output to filter out the unwanted harmonics. However, the narrow-band nature of the LC load can result in swing variation within the oscillator tuning range. To solve that, a parallel 200 Ω resistor is placed in parallel with the tank to reduce the quality factor and increase the bandwidth.

2.2.4 Single-Ended-to-Differential Converter

Fig. 2.9 shows the active balun that amplifies the 10 GHz single-ended signal at the doubler output while converting it into the differential form.

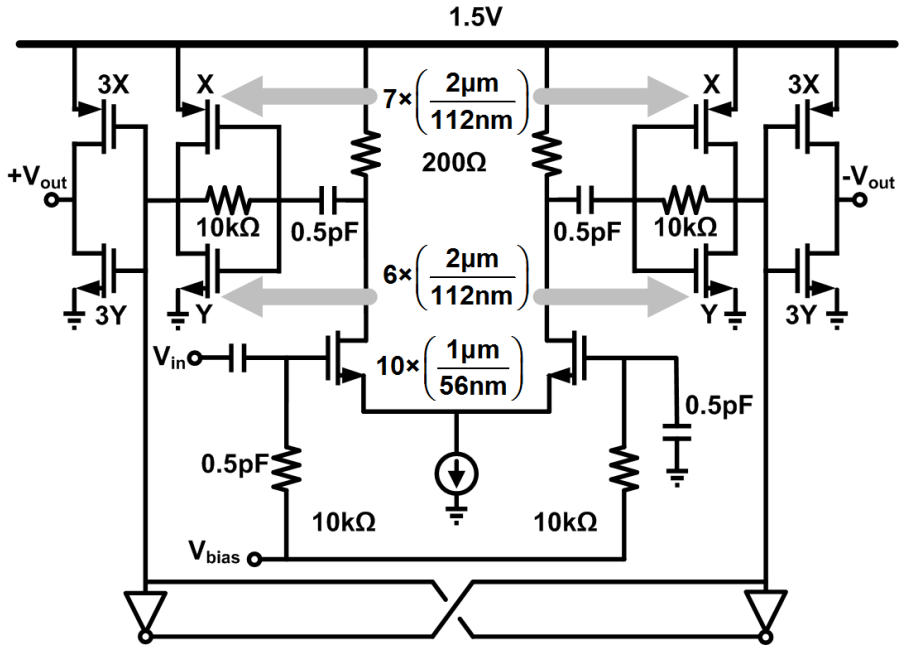

Figure 2.9: Schematic of the designed single-ended-to-differential converter followed by a two-stage CMOS buffer. [3]

No inductors are used at this block to save the area. Following the active balun, there is a two-stage CMOS buffer for more amplification and to produce rail-to-rail swing. The first stage of the CMOS buffer has a resistive feedback to provide bias. Buffers are scaled up for generating a high slew-rate signal and consequently to minimizes the power consumption. Minimum-size cross-coupled inverters are implemented between the two stages of CMOS buffer to guarantee a differential signal pair and also drives the load.

Acknowledgment

Some parts of this chapter are adopted from [3] and [18].

Chapter 3

Phase-to-RF and Amplitude-to-RF Time Alignment

Previous chapter introduced a phase modulator based on injection locking coupled-oscillators. In that design phase of the input signal is injected into the center oscillator and amplitude of the input signal detunes the edge oscillators to generate the outphasing angle. One key challenge in that approach is the amplitude-to-RF and phase-to-RF time alignment. This chapter presents an outphasing analog approach to deliver a synced amplitude-to-RF and phase-to-RF with using only two DACs. Modulator is designed in 45-nm CMOS SOI process and operates at 10 GHz.

3.1 Injection Locking Coupled Oscillator versus Outphasing Modulator

Injection locking coupled oscillator presented in the previous chapter requires two DACs, one for phase and another one for amplitude. In that regard, it is similar to envelope tracking structures. These two approaches have a common disadvantage. In both envelope tracking and presented injection locking coupled

oscillator, time alignment between amplitude-to-RF and phase-to-RF modulation remains a challenge. This is due to the fact that phase information is injected into the center oscillator, whereas amplitude information is applied to the edge oscillators. In other words, phase and amplitude travel different paths from baseband to RF. To solve this challenge, referring to conventional outphasing modulator is helpful. In conventional outphasing systems phase and amplitude are inherently synced in baseband and RF. This is due to the fact that amplitude and phase decomposition is handled in digital domain where it is considerably easier to handle any time mismatches. Then, based on amplitude and phase four vectors are generated in digital domain. Each pair of them represents the in-phase (I) and quadrature-phase (Q) for one of the two outphasing vectors (S1=I1+Q1, S2=I2+Q2). Since these four signals are introduced to the similar baseband-to-RF paths, inherently amplitude-to-RF and phase-to-RF are time aligned. This is a major advantage of the conventional outphasing compared to envelope tracking and injection locking coupled oscillator outphasing modulator. However, in a conventional outphasing modulator four DACs are required. Here the goal is to design a system to benefit from a relaxed amplitude-to-RF and phase-to-RF time alignment and at the same time only requires two DACs.

3.2 Independent Detuning of Coupled-Oscillator

Outphasing system presented in the previous chapter introduces two different paths to phase and amplitude. Phase information rotates the center oscillator while amplitude information triggers the edge oscillators. Amplitude information controls the tank varactor and detunes the edge oscillators deferentially. In the previous approach final phase of the outphasing vectors is generated in two steps where edge oscillators were being detuned differentially to generate $\phi(t)$ while in a separate step center oscillator was rotated with $\theta(t)$ to rotate edge oscillators with theta. Another approach could be to land the outphasing vectors to their final location at once. This can happen by injecting both amplitude and phase information to the oscillator simultaneously. Given that it is easier to handle time

mismatch in digital domain compared to baseband or RF, $\phi(t)$ can be calculated in digital domain. Also, in digital domain $\theta(t)+\phi(t)$ and $\theta(t)-\phi(t)$ can be calculated and by using an LUT calculated $\theta(t)+\phi(t)$ and $\theta(t)-\phi(t)$ can be mapped to individual tuning voltages. Finally these tuning voltages will need to get converted from digital to analog and get fed to each of the oscillators independently. Therefore, with this approach each oscillator will land to its final phase directly unlike the previous approach.

In other words, each of the two edge oscillators can be rotated for $\theta(t)+\phi(t)$ and $\theta(t)-\phi(t)$. That way edge oscillators are detuned independently and as a result amplitude-to-RF and phase-to-RF information travel the exact same path and there wont be any need for additional time alignment technique for this approach. Fig. 3.1 shows the system block diagram of this architecture.

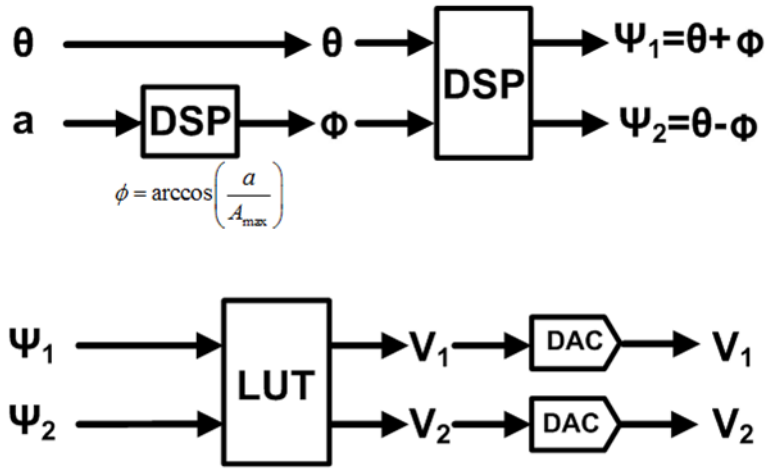

Figure 3.1: System block diagram of the outphasing modulator with two oscillators.

3.2.1 Block Diagram

Fig. 3.2 illustrates the block diagram of the proposed scheme. Unlike the previous design with three oscillators, in this design only two oscillators are required and there wont be a need for the center oscillator since $\theta(t)$ and $\phi(t)$ both

are applied to the left and right oscillator directly.

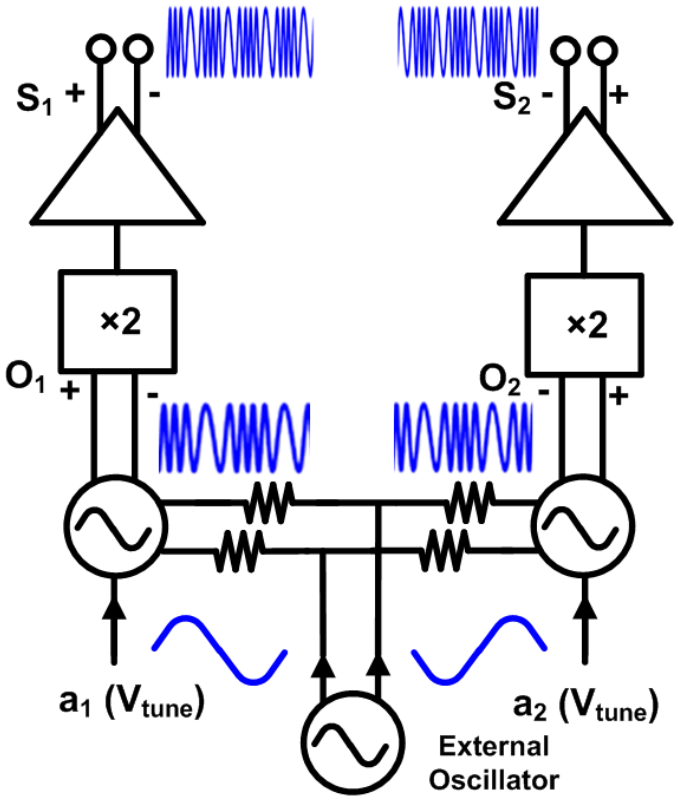

Figure 3.2: Block diagram of the outphasing modulator with two oscillators.

Since the left and right oscillators should be detuned independently, then there is no need for center oscillator. As shown in 3.2, the external oscillator is tapped to the middle of the coupling resistive network, and similar to the previous design coupled oscillators are followed by frequency doublers and single-ended-to-differential converters. This approach benefits from requiring only two DACs similar to the original coupled oscillator outphasing modulator. But, unlike that design, there is no need to take any extra steps to ensure the time alignment between amplitude-to-RF and phase-to-RF modulator.

3.2.2 Simulation Results

The key in this design is to generate two outphasing vectors independently so that each oscillator will land to its final phase directly. Therefore, by taking advantage of the nature of the conventional outphasing system and using digital domain to handle any time mismatches the phase and amplitude can be synced in baseband and RF. In this case, left oscillator should be detuned with the proper detuning voltage for S_1 to land on $\theta(t) + \phi(t)$ and the right oscillator should be detuned to make sure S_2 is located at $\theta(t) - \phi(t)$. To demonstrate that oscillators can be detuned independently several cases are simulated.

Fig. 3.3 shows the simulation result of the output phase of both channels when only oscillator 1 is detuned and the tuning voltage of oscillator 2 is fixed. Fig. 3.3 shows that oscillator 1 produces different phase as tuning voltage is changing, while the phase of the oscillator 2 remains constant. It can be seen that oscillator 1 covers a phase range of 351 degrees before it is pushed into the unstable region.

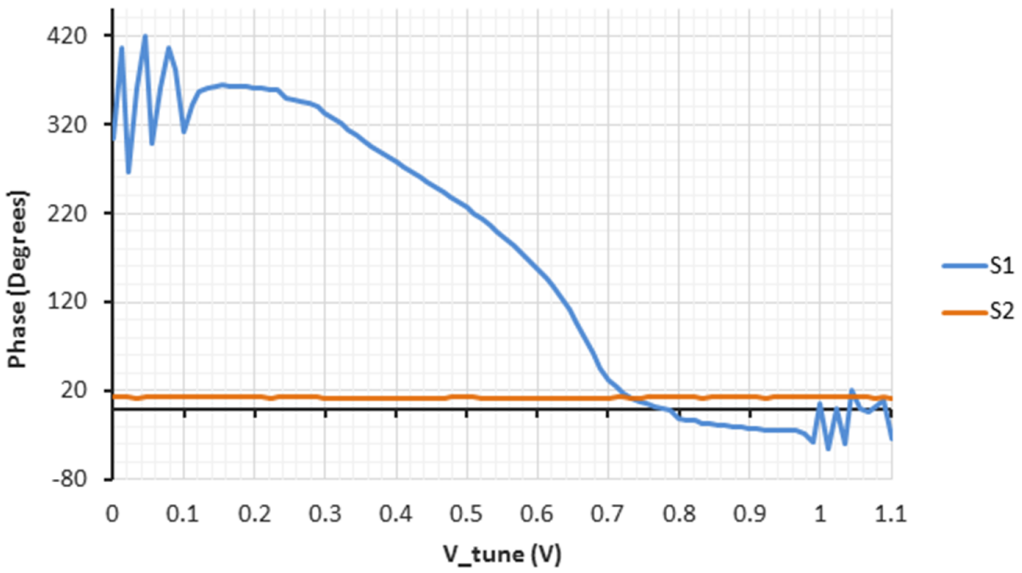

Figure 3.3: Oscillator 1 is detuned and oscillator 2 is fixed.

Next simulation, studies the case when the tuning voltage of oscillator 1

is fixed and oscillator 2 is detuned. Fig. 3.4 shows the simulation result of the output phase of both vectors when oscillator 2 produces different phase as tuning voltage is changing, while the phase of oscillator 1 remains constant. It can be seen that oscillator 2 covers a phase range of 350 degrees before it is pushed into the unstable region.

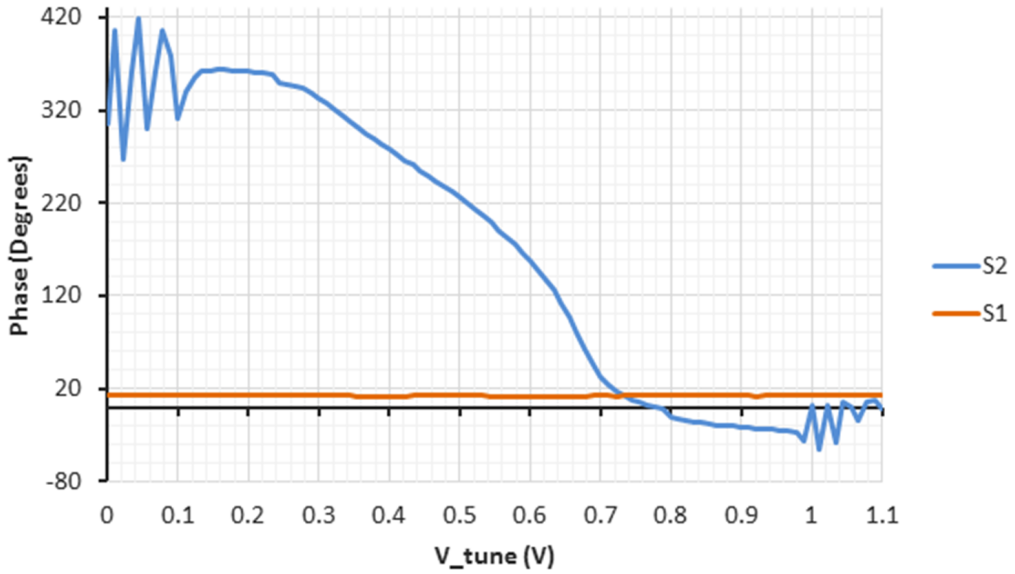

Figure 3.4: Oscillator 2 is detuned and oscillator 1 is fixed.

Another case that was simulated, represents vector S_1 following vector S_2. In this case, both oscillators were detuned in the same direction. Fig. 3.5 shows the simulation result of this case where the output phase of oscillator 1 is following oscillator 2. For that, there is a 0.1V offset in detuning voltage for oscillator 1 and oscillator 2. It can be seen that both vectors cover a phase range of 355 degrees before they are pushed into the unstable region.

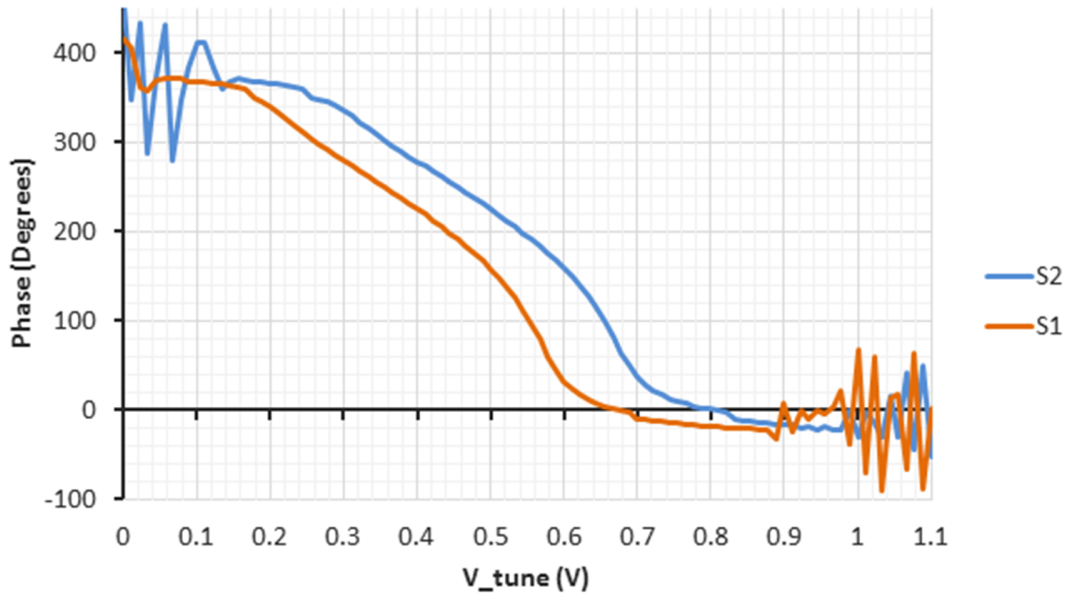

Figure 3.5: Both oscillator 1 and oscillator 2 are detuned with 0.1V offset in their detuning voltage.

3.3 Weak Coupling versus Strong Coupling

In this section the effect of coupling strength is discussed. In the original design that was presented in previous chapter, coupling network was built with $1k\Omega$ resistors. That was to make sure that coupling is weak and injected current is much smaller than the oscillator current to guarantee that phase variation is an arccosine function of the tuning voltage. In the current approach presented in this chapter, there is no need to generate an arccosine function and therefore we can design for a strong coupling. To increase the coupling strength delivered power from external source can be increased. However, there is a practical limitation with the maximum swing that an external source can generate and here, it is assumed to be 0.5V amplitude. Next step to increase the coupling strength is to reduce the coupling network resistance. Simulation results show that more detuning is required for phase modulator with strong coupling compared to a phase modulator with weak coupling to get the same phase variation.

Fig. 3.6 shows the phase variation versus detuning voltage for a phase modulator with a $1k\Omega$ coupling resistor. It can be seen than the phase modulator can offer a +/-172 degrees of phase coverage for detuning voltage from .465V to .532V. As shown in Fig. 3.6 by detuning oscillators for less than 0.1V oscillators can almost cover the whole phase range. This happens because there is no strong coupling between oscillators, therefore a small change in capacitor of the tank will result in large phase steering. That means phase is sensitive to tuning voltage, and to reduce the sensitivity we should provide stronger coupling.

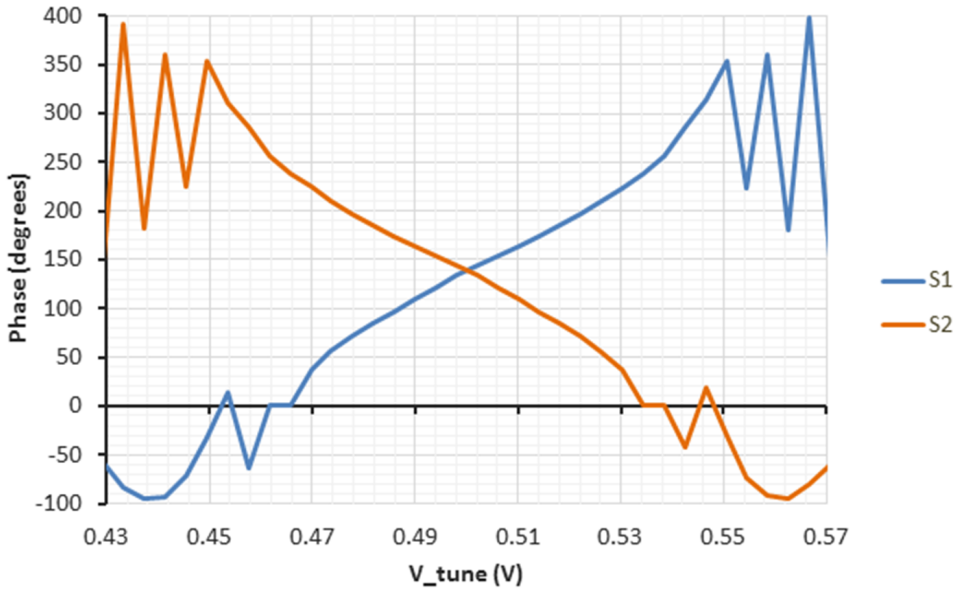

Figure 3.6: Phase variation versus detuning voltage for a phase modulator with a $1k\Omega$ coupling resistor.

Same simulation is performed for a coupling resistance of 100Ω. Fig. 3.7 shows the phase variation versus tuning voltage for strong coupling case. From Fig. 3.7 it can be seen that with a detuning voltage from .185V to .737V, a +/-176 degrees of phase variation can be achieved. Therefore, to cover the whole phase range oscillators need to get detuned about 0.7V. This means phase variation is less sensitive to the cap variation and therefore the tuning voltage variation.

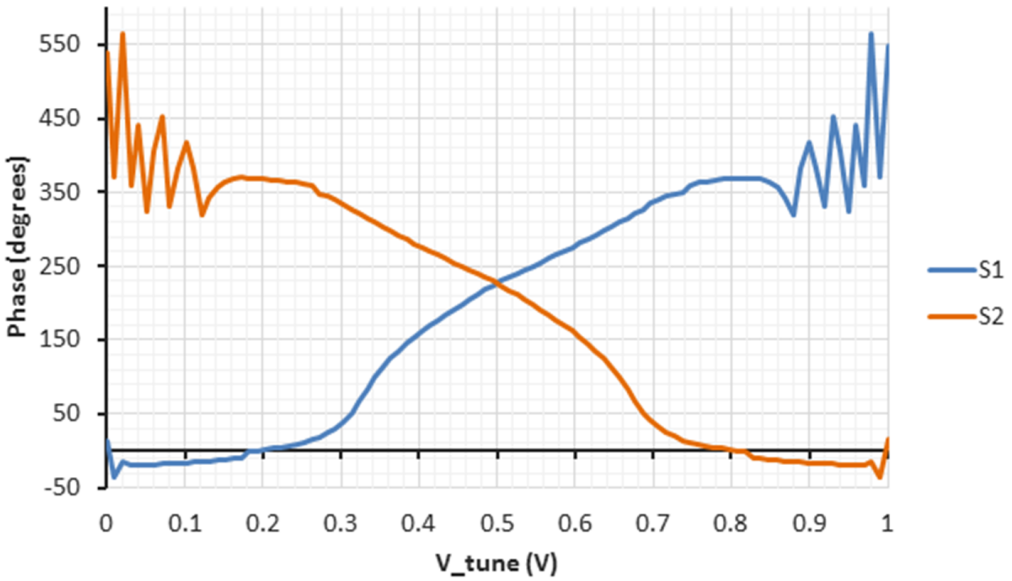

Figure 3.7: Phase variation versus tuning voltage for a phase modulator with a 100Ω coupling resistor.

A wider range of detuning voltage translates to more capacitance variations. Reducing coupling resistance reduces the sensitivity of phase versus cap variation (and therefore tuning voltage variation). This will be beneficial if an accurate control on the cap value is required. However, reducing the coupling resistance will result in a higher current consumption and increase the power consumption. Table. 3.1 compares the current consumption of the phase modulator with $1k\Omega$ and 100Ω.

Table 3.1: Comparison between current consumption of the phase modulator with $1k\Omega$ and 100Ω.

	R = $1k\Omega$	R = 100Ω
Phase Range (degrees)	344	351
Current Consumption (mA)	14.5	15.2

According to this table current consumption increases from 14.5mA to 15.2mA for using 100Ω resistor instead of $1k\Omega$. This change is not a consider-

able increase in current consumption and will provide a finer capacitance control. So, if less sensitivity is highly desired, it can be achieved by paying a low price on current consumption. Also, not surprisingly, there is no meaningful phase range difference between these two cases. In the next chapter it will be discussed that how this increase in capacitance range can help with linearity

3.4 Comparison Between Techniques

In this section, Table. 3.2 presented to summarize the advantages and disadvantages of different techniques that has been reviewed and presented so far based on their required number of DACs, and whether time alignment is an issue for them. From Table. 3.2 it is clear that the presented design of independently detuned coupled oscillators phase modulator in this section has eliminated amplitude-to-RF and phase-to-RF time alignment challenge, while it only requires to use two DACs.

Table 3.2: Comparison between different phase modulator techniques.

Technique	# of DACs	Time Alignment
Envelope Tracking	2	Challenge
Conventional Outphasing	4	Not a Challenge
Coupled Oscillators Outphasing	2	Challenge
Independent Coupled Oscillators Outphasing	2	Not a Challenge

Acknowledgment

Blocks that are used in this modulator are adopted from [3]

Chapter 4

Outphasing Modulator with Digitally Voltage Controlled Oscillator

This chapter describes a proposed digitally voltage controlled oscillator (DVCO) to be utilized in the outphasing modulator. To implement the DVCO, varactor is replaced with a cap bank. In the following sections cap bank design is discussed step by step. First, the required cap bank range is studied. Then, cap bank resolution is decided based on linearity of the modulator. Finally, switches are designed to meet the varactor quality factor. At the end of this chapter, outphasing modulator performance is simulated with the designed cap bank. Similar to the previous chapter, this circuit is designed in a 45-nm CMOS SOI process.

4.1 Capacitance Range

To determine the demanded capacitance range, described VCO from previous chapter is used. Sweeping capacitance and monitoring frequency can define the required cap bank range. In this test one of the VCOs is locked to the external source and the other one is free running. Fig. 4.1 shows that for the free running oscillator S_1, sweeping capacitor changes the oscillation frequency. However, in case of the locked oscillator S_2, frequency remains similar to the external source

over the locking range. Mapping this locking range into capacitance range defines the targeted range of cap bank in this design. As, Fig. 4.1 demonstrates a capacitance range of 1.1 pF to 2.3 pF is required.

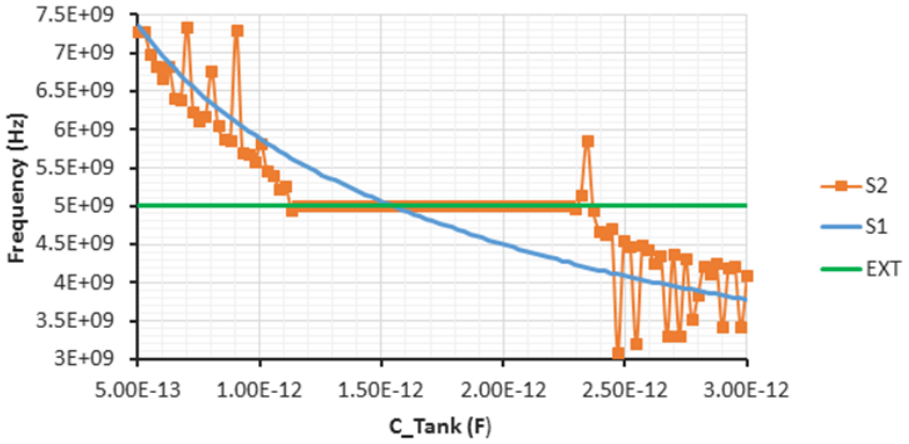

Figure 4.1: Frequency of free running and locked oscillators versus capacitance.

Fig. 4.2 shows the phase variation for the locked S_2 and free running oscillators S_1 versus capacitance. Over the locking range, phase of the locked oscillator can be defined as a function of the capacitance.

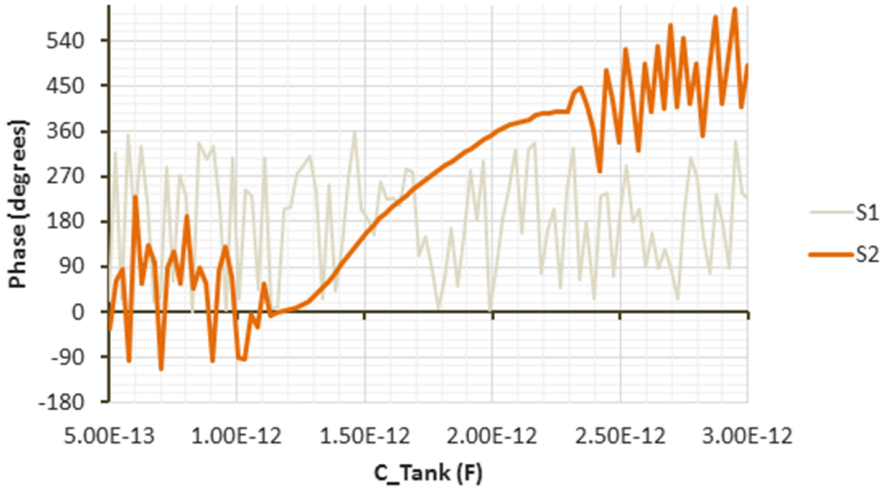

Figure 4.2: Phase variation for locked and unlocked oscillators versus capacitance.

4.2 Number of Bits

Number of bits should be decided based on linearity since cap bank resolution affects the linearity of the modulator. Error Vector Magnitude (EVM) is a function of amplitude and phase error as shown below

$$EVM = \sqrt{\left(\frac{a}{2}\right)^2 + \left(\frac{\theta}{2}\right)^2} \tag{4.1}$$

where (a) is amplitude error and (θ) represents the phase error. In outphasing modulator since output vectors are constant envelope, only phase error will be relevant. Therefore, EVM equation will be simplified to $EVM = \frac{\theta}{2}$ which is only function of phase error. Phase resolution is a function of number of bits, so $\theta = \frac{2\pi}{2^N}$, where N is the number of bits, Table. 4.1 summarize the EVM versus number of bits.

Table 4.1: EVM versus number of bits.

EVM	Number of bits
1%	9
2%	8
5%	6
10%	5
20%	4

In this work an EVM of 2% is being considered and therefore an 8-bit cap bank is designed. Cap range and resolution will define the capacitor unit cells.

4.3 Quality Factor

Cap bank unit cells are metal-insulator-metal (MIM) cap which inherently has a higher quality factor compared to varactor. However, in cap bank, these MIM caps are placed in series with switch devices to form the cap bank and provide the control over the capacitance. Adding switches degrades the quality factor, but

it can't become worse than quality factor of the original varactor. Series on-resistance of these switches degrades the quality factor of cap bank. Increasing device sizes helps to reduce the series on-resistance. However, it increases the parasitic capacitance of the device as well, which leads to nonlinearity specially at higher data rates. In this design, our goal is to select device sizes to make sure quality factor of the cap bank is similar to quality factor of varactor that was designed and described in chapter two.

Fig. 4.3 shows the simulated quality factor of the varactor at operation frequency (5 GHz), that was used in the original design, versus tuning voltage. As Fig. 4.3 shows varactor has a quality factor of 87.

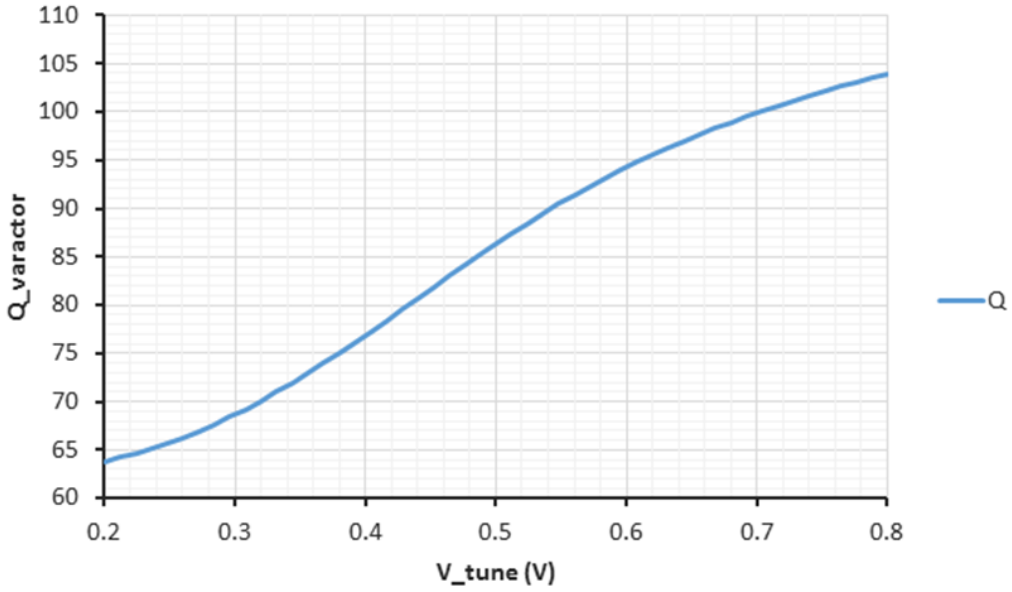

Figure 4.3: Simulated quality factor of varactor.

As it is mentioned earlier in this section quality factor of the MIM caps are higher than quality factor of the varactors. To quantify quality factor of MIM cap, a MIM cap with the value of the maximum required capacitance (2.3 pF) is simulated. Fig. 4.4 shows the simulation results over frequency. As it shows MIM cap has a quality factor of 880 at 5 GHz.

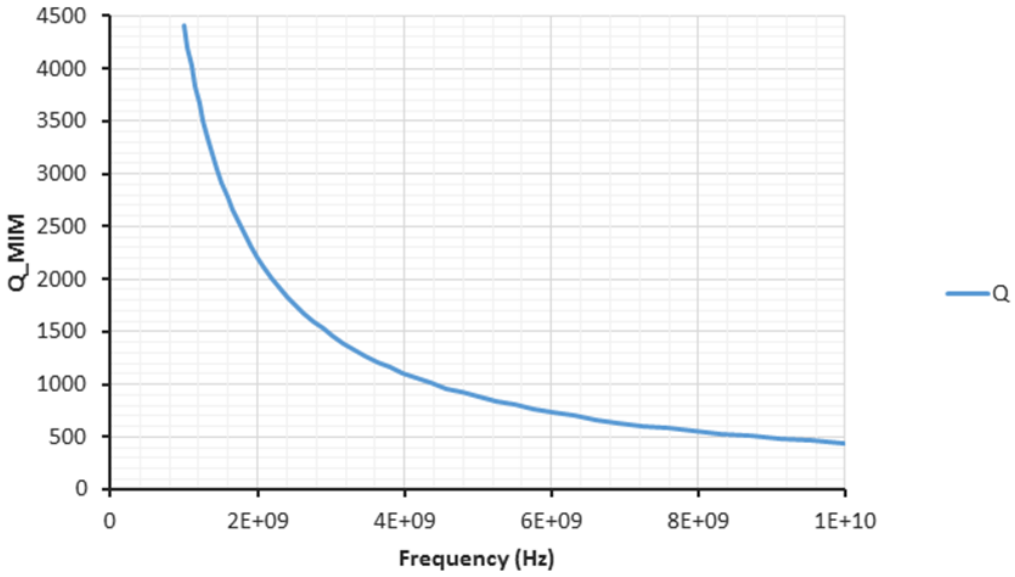

Figure 4.4: Simulated quality factor of 2.3 pF MIM cap.

To design for a cap bank that has quality factor similar to the Q of the varactor (87), parallel resistor should be calculated. From $Q = \frac{R_p}{X_P}$ where $X_p = \frac{1}{j\omega C}$, R_p can be calculated at total capacitance of 2.3 pF and 5 GHz frequency. To match the Q of varactor, it should be considered that some portion of the cap bank is fixed. In this case as it was mentioned before, given that capacitance range is 1.1 pF to 2.3 pF, 1.1 pF is fixed and only 1.2 pF is variable. Since cap bank is formed by placing a 1.1 pF MIM cap with a quality factor of 880 in parallel with the variable 1.2 pF capacitance, Q of the variable portion can be much lower than 87. To calculate the Q of the cap bank variable portion ($Q_{variable}$), it would be a fair assumption to consider the fixed portion ideal and pair R_p with $Q_{variable}$. Given that $Q_{variable} = \frac{R_p}{X_{P,variable}}$ where $X_{p,variable} = \frac{1}{\omega \times 1.2pF}$, $Q_{variable}$ is equal to 45.

In the next step, maximum series resistance with the variable portion of the cap bank should be calculated ($R_{s,variable}$). From $R_{s,variable} = \frac{R_p}{\left(1+Q^2_{variable}\right)}$ and by substituting quality factor of the variable portion, $R_{s,variable}$ will be equal to 0.58Ω. That means the on-resistance of the MSB bit should be limited to 1.2Ω. Simulation results show that a switch device with finger width of 3 um and a total

number of fingers of 4 and multiplicity of 32 provides a 1.2Ω on-resistance.

Fig. 4.5 shows the schematic of the designed 8-bit cap bank. Unit cells are scaled down from MSB to LSB.

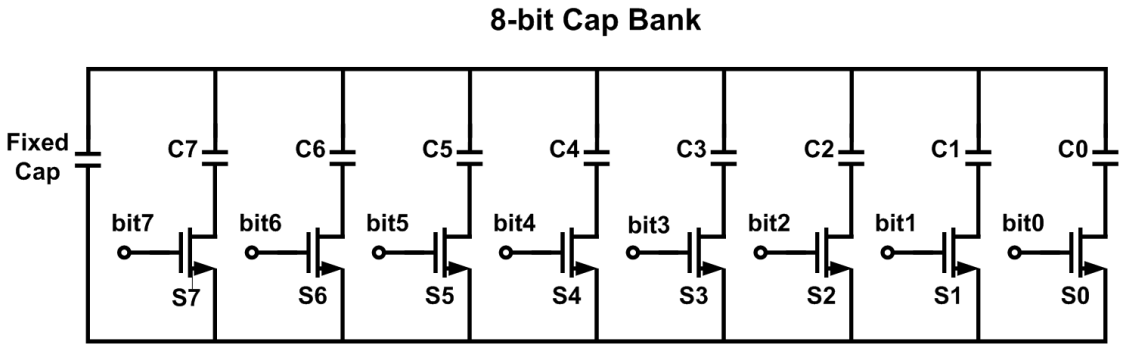

Figure 4.5: Designed 8-bit cap bank.

Table. 4.2 mesmerizes the capacitor's sizes in the cap bank. To get the best matching, unit cells are the same across the cap bank and larger caps designed by adding more unit cells in parallel.

Table 4.2: Cap bank series capacitor sizes.

Bit	M	$W[uM]$	$L[nM]$	$Unit-Cell-Cap[fF]$	Total Cap [fF]
7(MSB)	128	2.9	3.43	5.46	698.9
6	64	2.9	3.43	5.46	349.5
5	32	2.9	3.43	5.46	174.72
4	16	2.9	3.43	5.46	87.36
3	8	2.9	3.43	5.46	43.68
2	4	2.9	3.43	5.46	21.84
1	2	2.9	3.43	5.46	10.92
0(LSB)	1	2.9	3.43	5.46	5.46

Table. 4.3 summarizes the switch device sizes. MSB switch is designed to offer no more than 1.2Ω on-resistance, to guarantee a Q of grater than 87 which was available in the original varactor design.

Table 4.3: Cap bank switch sizes and on resistances.

Bit	M	$W[uM]$	$L[nM]$	On ResistanceΩ
7(MSB)	32	$4x3$	56	1.2
6	16	$4x3$	56	2.1
5	8	$4x3$	56	4
4	4	$4x3$	56	7.8
3	2	$4x3$	56	15.5
2	1	$4x3$	56	30.9
1	1	$4x1.5$	56	61.6
0(LSB)	1	$4x.750$	56	123.1

Fig. 4.6 shows the simulated capacitance versus control bit. It shows that the cap bank covers the 1.15pF to 2.3pF range in a monotonic fashion.

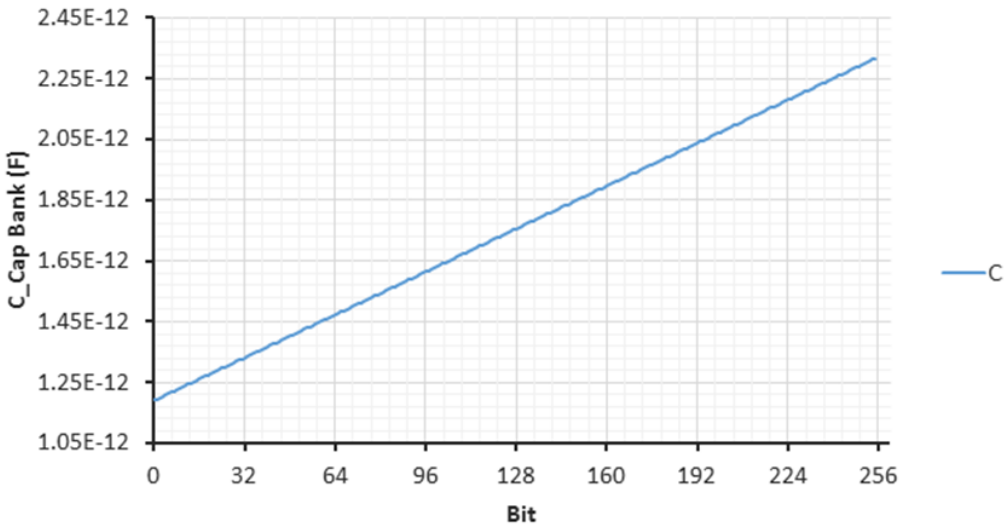

Figure 4.6: Capacitance of the designed 8-bit cap bank versus bit.

Quality factor of the fixed and variable portion of the cap bank are shown in Fig. 4.7 and Fig. 4.8.

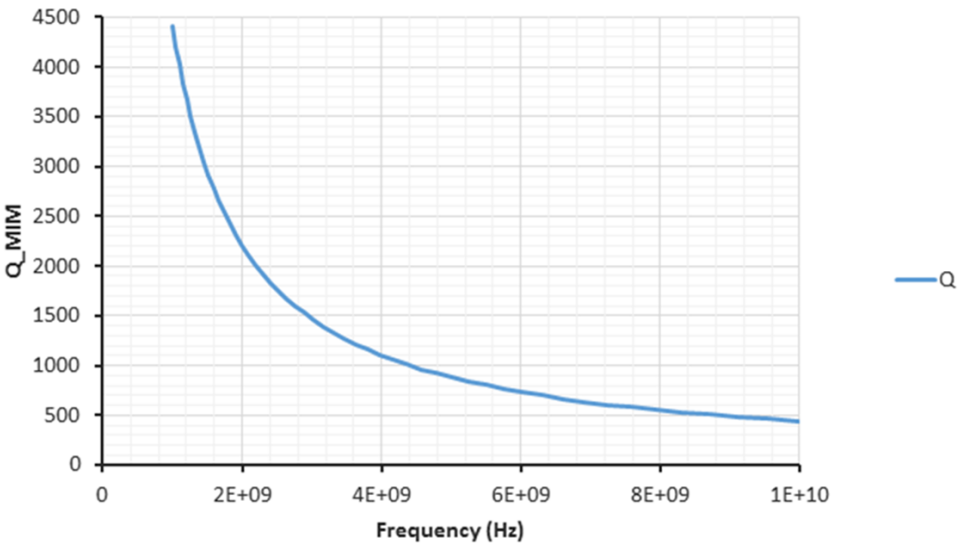

Figure 4.7: Quality factor of the fixed portion of the designed 8-bit cap bank versus bit.

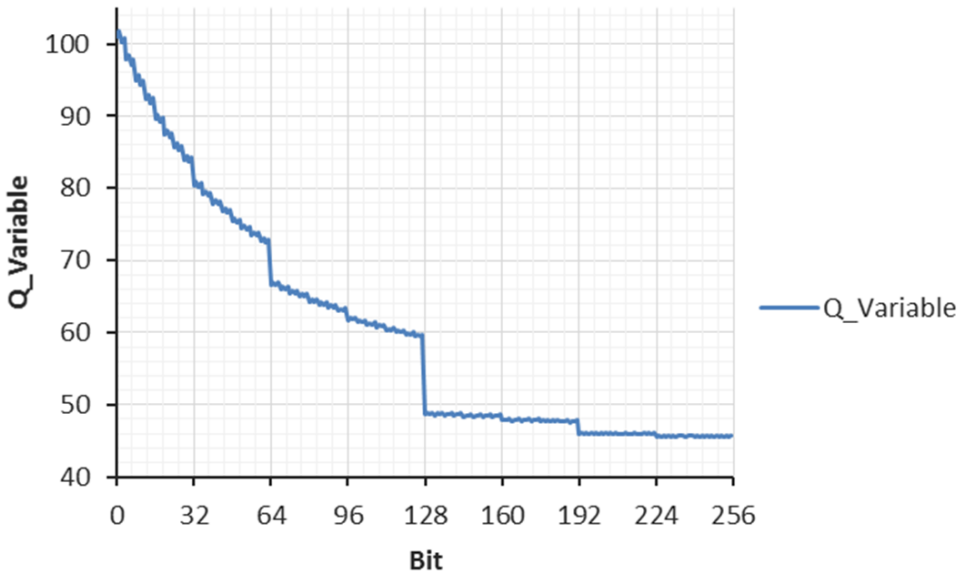

Figure 4.8: Quality factor of the variable portion of the designed 8-bit cap bank versus bit.

Quality factor of the cap bank is the combination of the quality factor of the fixed and variable portion and Fig. 4.9 demonstrates the simulated quality factor of the cap bank versus bits. Fig. 4.9 shows that quality factor of the designed cap bank is better than 90 over the whole code range which is better than the 87 offered by the original varactor.

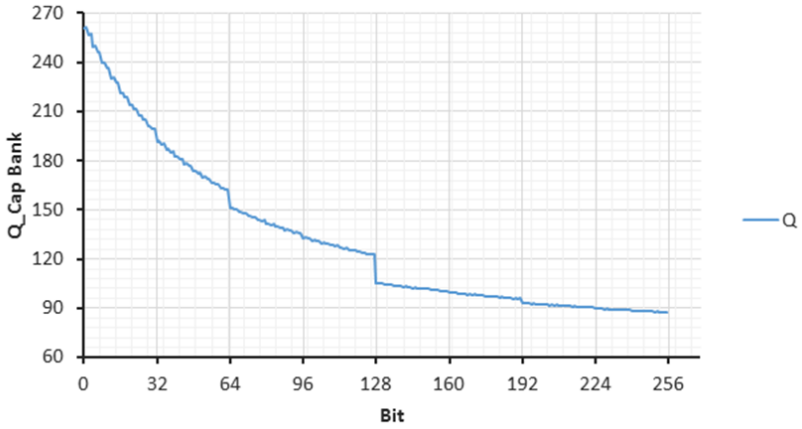

Figure 4.9: Quality factor of the designed 8-bit cap bank versus bit.

Now that cap bank is designed cap DNL can be captured from a 200-points Monte Calrlo simulation result as shown in Fig. 4.10. Cap DNL shows cap steps as cap bank code changes from 0 to 255. Fig. 4.10 shows that MSB has the maximum error since it has the maximum cap variation. Maximum cap error is 20 times larger than capacitance LSB=5.46 fF.

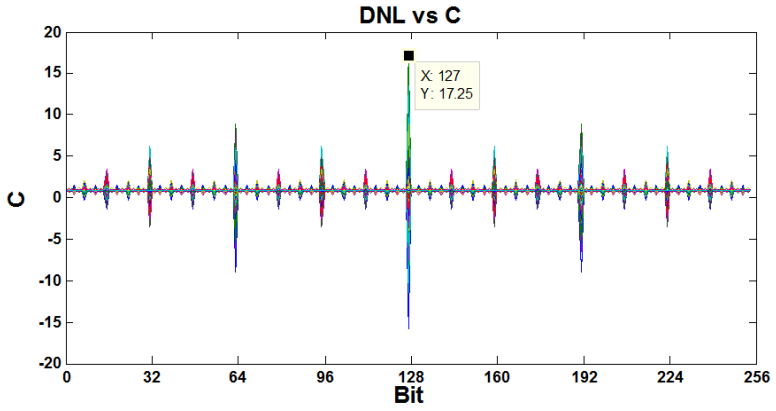

Figure 4.10: Cap DNL versus cap bank code.

4.4 DVCO Simulation Results

At this step cap bank is incorporated into the oscillator, and Fig. 4.11 demonstrates schematic of the designed oscillator using an 8-bit cap bank. This way there wont be a need for external DAC anymore.

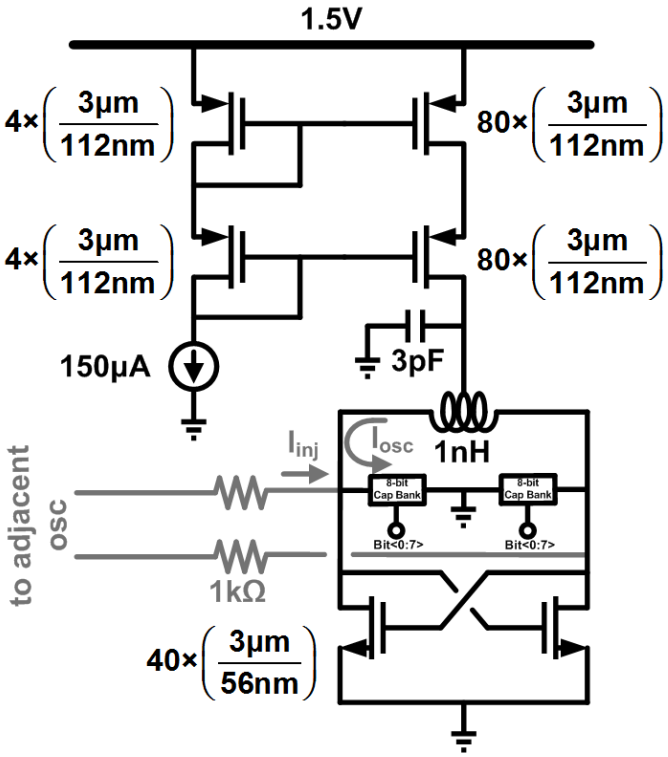

Figure 4.11: Digitally voltage controlled oscillator with 8-bit cap bank.

To evaluate the performance of the phase modulator with cap bank, one of the oscillators is tied to the external source while the other one is free running. In this case, oscillator 1 is on free running mode. So, as shown in Fig. 4.12 frequency of oscillator 1 is changing versus the code number. On the other side, oscillator 2 is locked to the external source so, it's frequency is fixed and equal to the external source. Fig. 4.12 shows the frequency versus cap bank code.

It can be seen that changing the cap bank code results in a change in frequency for the free running oscillator from 4.2 GHz to 5.6 GHz, whereas the one locked to the external source has a fixed frequency. Instead, as it was discussed in previous chapter, it is expected that phase of the locked oscillator should change

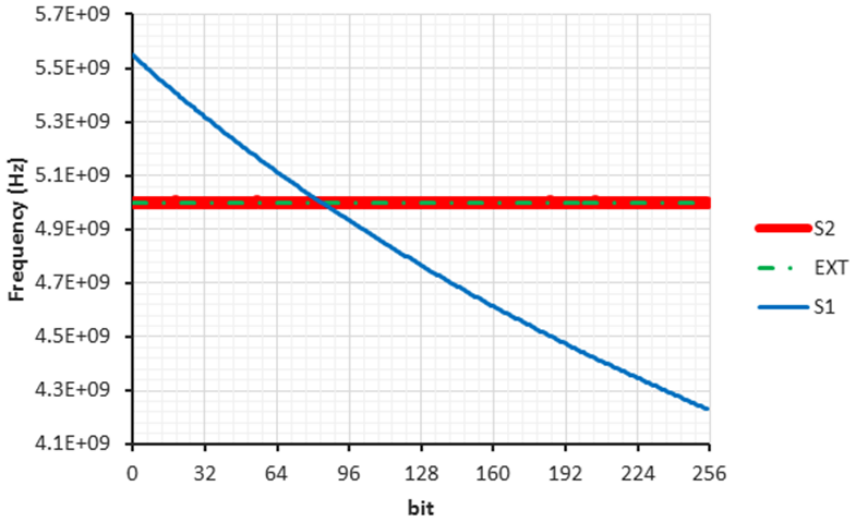

Figure 4.12: Frequency of the locked and free running oscillators versus cap bank code.

as cap bank code is changing. This is shown in Fig. 4.13. Phase of the locked oscillator covers the range of +/-166 degrees which means 336 degrees of phase coverage, whereas the free running oscillator represents a random phase.

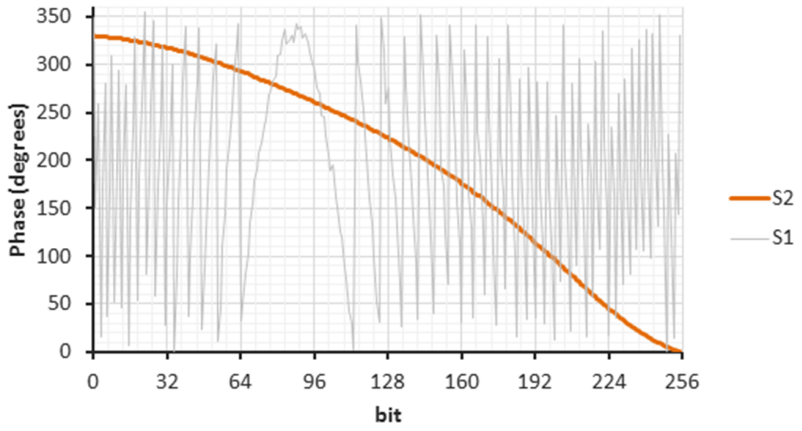

Figure 4.13: Phase of the locked and free running oscillators versus bit.

At the end, to demonstrate the performance under mission mode, previous simulations are repeated when both oscillators are locked to the external source, and they are differentially detuned. Fig. 4.14 shows the output phase of both

channels when oscillators are detuned differentially.

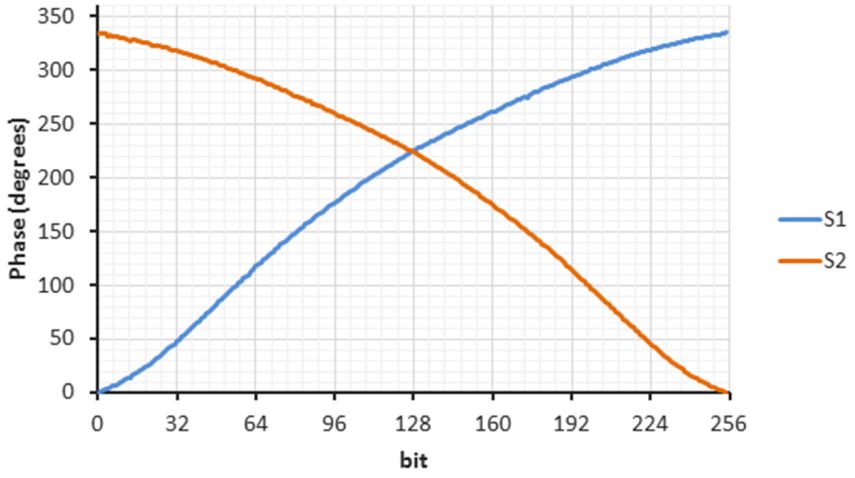

Figure 4.14: Phase of the locked oscillators versus cap bank code.

Finally, after capturing the phase simulation results Fig. 4.15 shows the phase DNL from a 200-points Monte Calrlo simulation result that captures phase steps as cap bank code changes from 0 to 255. Phase DNL result shows that MSB has the maximum error since it has the maximum cap variation. Maximum phase error is 20 times larger than phase LSB=1.4.

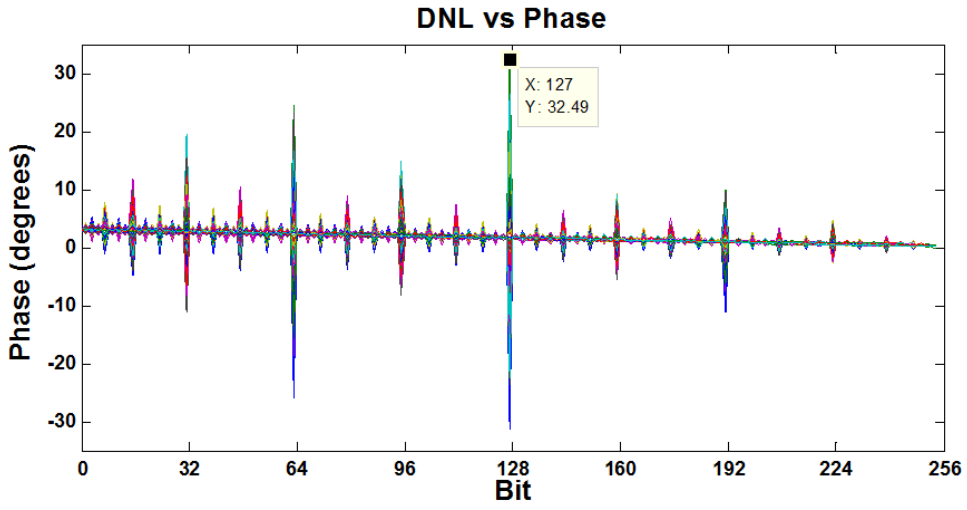

Figure 4.15: Phase DNL versus cap bank code.

4.5 Acknowledgment

For the phase modulator presented in this chapter, cap bank is designed and the rest of the oscillator is adopted from [3] with modification.

Chapter 5

Conclusions

This thesis presents the analysis, design and simulation results in the area of injection locking phase modulators for x-band wireless communication. First, previous techniques for efficiency improvement such as envelope tracking and outphasing are reviewed. It has been discussed that in envelope tracking scheme, two DACs are required. One for envelope information and another one for phase. It should be considered that these two information have two different baseband-to-RF paths and therefore amplitude-to-RF and phase-to-RF time alignment remains a challenge. On the other side in a conventional outphasing modulator amplitude-to-RF and phase-to-RF are inherently time aligned. The reason is that there are four independent signals and bounding them in two pairs, forms the outphasing angles. While there is no need for additional steps to have time aligned signals, the fact that there are going to be four signals, imposes having four DACs in system. Later it has been discussed that how to overcome this trade-off.

Second, an outphasing modulator based on injection locking coupled oscillators is presented. In this system there are three oscillators coupled to each other to form a phase modulator. Center oscillator is locked to the external source. phase information is injected to the center oscillator as a common mode signal that rotate all the oscillators in the same direction. Amplitude information detunes the edge oscillators differentially to form the two outphasing vectors with appropriate outphasing angle between them. This approach requires two DACs but amplitude-to-RF and phase-to-RF time alignment remains a challenge.

Then, it was proposed that tuning edge oscillators independently could land the outphasing vectors at their final angles $\theta + \phi$ and $\theta - \phi$. In this case there is only a need for two DACs and amplitude-to-RF and phase-to-RF time alignment has been taken cared of. This is the advantage of the proposed structure over previous generation [3].

Finally, varactor is replaced with an 8-bit cap bank in oscillator to implement the digitally controlled oscillator. As a result there wont be a need for external DACs and this design still benefits from the amplitude-to-RF and phase-to-RF time alignment. Cap bank is designed to cover the required capacitance range for the phase modulation as well as to meet the quality factor of the varactor that was being used in the previous generation. All the circuits presented here are designed in 45-nm CMOS SOI.

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