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EXCESS NOISE IN SELECTED FIELD-EFFECT TRANSISTORS

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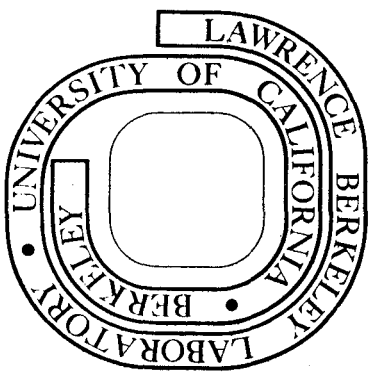

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EXCESS NOISE IN SELECTED FIELD-EFFECT TRANSISTORS*

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ABSTRACT

The origin of excess noise in high-quality FETs is investigated in the frequency domain. It is found that, for use in opto-feedback systems, generation-recombination noise through deep traps is important. It is shown that best initial characterization of transistors for that use can be done in a grounded gate configuration. The activation energy of the principal traps responsible for the g-r noise is calculated and tentative identification of the responsible impurities or defects is made. It is also shown that the basic low temperature limit of Si FET operation is set by majority carrier freeze out at chip temperatures well above 100K and that boron nitride mounts at temperatures above 77K can contribute 10 to 15 eV of 1/f noise.

INTRODUCTION

In a previous paper,[1] it was shown that the basic FET parameters determining the noise behavior of ultra-low noise opto-feedback spectrometer systems can best be measured in the frequency domain. It was found that for high-quality 2N4416 FETs, the noise voltage spectrum at the output of a charge sensitive preamplifier contains, in general, four terms:

$$V(f) = \left\{ (a_1/f^2) + (a_2/f) + a_3 + \left[a_4 \, \tau_g/(1 + \omega^2 \, \tau_g^2) \right] \right\}^{\frac{1}{2}} \left(\frac{\text{volt}}{\text{Hz}^{\frac{1}{2}}} \right) \qquad (1)$$

where $a_1 = 2q \, I_L'/(2\pi C_{fb}^2)$ (parallel component),

$a_2 = 2 \, A_\alpha / C_{fb}^2$ (1/f),

$a_3 = 4 \, kT \, r_s \, C_{in}^2 / C_{fb}^2$ (series),

$a_4 = K_g \, C_{in}^2 / C_{fb}^2$. (generation-recombination)

In terms of the customary noise equivalent circuit, I_L' corresponds to detector plus FET gate leakage current, $2 A_\alpha$ is the value of the power spectrum of the 1/f noise at f = 1 Hz, r_s is the equivalent resistance in series with the FET gate which generates noise equivalent to the white noise in the channel, and K_g is a proportionality constant for the observed FET gate junction generation-recombination noise. τ_g is a characteristic generation-recombination (g-r) time which is temperature dependent. Please see Ref. 1 for a more detailed description of the parameters.

The results obtained by fitting Eq. (1) to experimental measurements in the frequency domain can be used to calculate noise line width (NLW) FWHM in a typical spectrometer by the expression:

$$NLW(FWHM) = \frac{2.35 \, \bar{e}}{q} \left\{ q \, I_L' \langle N_s^2 \rangle + A_\alpha \langle N_{-1s}^2 \rangle + 2 \, kT \, r_s \, C_{in}^2 \langle N_\Delta^2 \rangle + \frac{1}{2} K_g \langle N_g^2 \rangle \right\}^{\frac{1}{2}} \qquad (2)$$

where $\langle N_s^2 \rangle \propto \tau_o$ (peaking time) (parallel component),

$\langle N_{-1s}^2 \rangle \simeq 6.9$ for all τ_o (1/f),

$\langle N_\Delta^2 \rangle \propto 1/\tau_o$ (series),

and $\langle N_g^2 \rangle \simeq [(2 \, \tau_g/\tau_o) + (\tau_o/2 \, \tau_g)]$. (g-r)

$\langle N_s^2 \rangle$ and $\langle N_\Delta^2 \rangle$ depend on the shape of filter response function, while $\langle N_{-1s}^2 \rangle$ is quite insensitive to it, at least for time invariant filters. Parameter $\langle N_g^2 \rangle$ has been evaluated numerically by integration in the frequency domain and it also is found to be quite insensitive to filter response shape. It can be approximated by the function given above.

This paper reports on the detailed results obtained from an analysis of the noise behavior of selected 2N4416 FETs at low temperatures by the use of frequency domain techniques as a first step toward the possible elimination of excess noise by improved FET fabrication and/or handling. The study is divided into three temperature regions, depending on the noise source that is dominant:

Region I, at very low temperatures, dominated by series noise which is white up to very high frequencies.

Region II, just below the optimum temperature, dominated by g-r noise.

Region III, at optimum temperature and just above, dominated by 1/f noise.

As an illustration of the relative importance of the different noise sources, please consider Fig. 1. The measured NLW vs approximate case temperature for a typical 'good' 2N4416 transistor in its standard header is shown. A feedback resistor of 10^9 Ω was used at peaking times of 1.6 and 6.4 μs. The NLW calculated from frequency domain measurements is also shown. Lags in FET chip temperature and errors in evaluating the feedback resistor noise and the 1/f contribution in the presence of g-r noise are probably responsible for most of the discrepancies between the measured and calculated results, particularly at τ_o = 6.4 μs. In Region I, the high series noise component is prominent, particularly at short τ_o. Its temperature dependence is very steep. In Region II a 'bump' due to g-r noise is quite evident. Since the magnitude of $\langle N_g^2 \rangle$ is independent of τ_o at its

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maximum ($\langle N^2_{g_{max}} \rangle$ = 0.47), the g-r 'bump' is most noticeable at longer τ_o, where the series component is small. In this respect, g-r noise behaves like 1/f noise, although its position in temperature shifts with τ_o due to the temperature sensitivity of τ_g. In Region III, NLW is dominated by a high 1/f component due to header losses, although at short τ_o, the series component can become dominant.

Figure 1 also shows an estimate of NLW at τ_o = 35 μs for the tested transistor if it were removed from its header and mounted in a boron nitride support. The measured values of series and g-r noise parameters for the transistor tested, scaled down to C_{in} = 3 pfd, are used in the calculation. Parallel noise is assumed to be negligible and an estimate of 1/f noise (decreasing at lower temperatures) is included, based on the findings of Ref. 1 and the present work. Removal of the g-r noise bump and/or the 1/f contribution clearly would reduce the NLW substantially.

A detailed analysis of noise behavior in the three regions indicated above will be given after a brief exposition of the nature of g-r noise and of measurement methods.

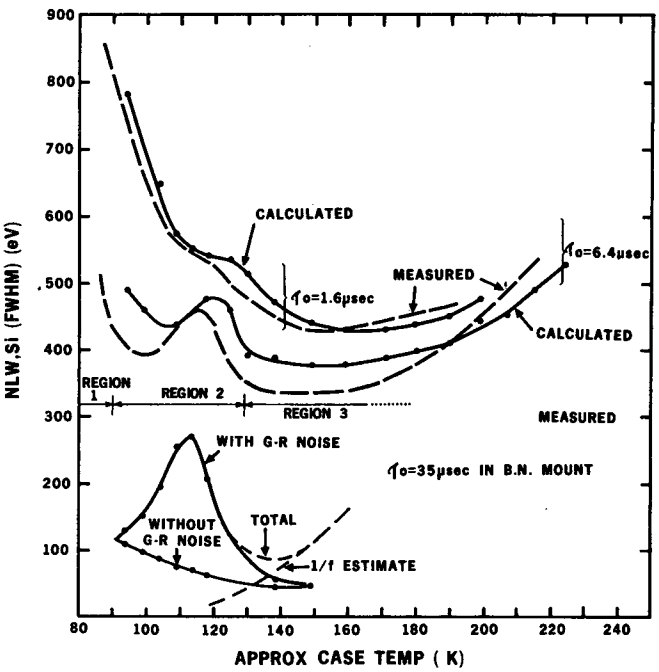

Fig. 1. Measured NLW at τ_o = 1.6 and 6.4 μs vs FET case temperature compared to point-by-point calculations from frequency domain measurements on the same transistor. Three main regions of noise behavior are defined. At bottom, extrapolation to a decanned transistor operated at τ_o = 35 μs.

THE NATURE OF THE G-R NOISE

Low-frequency generation-recombination noise has been studied in detail in the literature. Perhaps the simplest and most useful theoretical study is that of Sah[2] in 1964. Measurement of g-r noise parameters are as recent as 1975, by Hiatt, van der Ziel and van Vliet.[3] Basically, the noise arises from fluctuations in gate width due to generation and/or recombination at traps in the gate-junction depletion layer or from fluctuations in the channel charge density due to those traps. For single level traps, g-r noise can be characterized by a generation time τ_g, which is sensitive only to temperature, and by a proportionality constant K_g whose magnitude depends on trap density and depth, and on device geometry and operating conditions. K_g can only be related to external variables in an approximate manner. The generation time τ_g can be described by

$$\tau_g \simeq 1/[c_p p_1 + c_n n_1] = 1/[e_p + e_n] \qquad (3)$$

for traps in the transition region of a reversely biased p-n junction, where c_p, c_n, e_p and e_n are respectively the hole and electron capture and emission rates at equilibrium, and $n_1 = n_i \exp(E_t - E_i)/kT$, $p_1 = n_i \exp(E_i - E_t)/kT$. E_t is the trap Fermi level and E_i is the energy level for intrinsic material.

For traps which are not near the center of the band gap, either the electron or hole term in Eq. (3) will dominate, so that, for example,

$$\begin{aligned} \tau_g &\simeq 1/c_n n_i \exp[(E_t - E_i)/kT] \\ &\simeq 1/c_n (N_c N_v)^{\frac{1}{2}} \exp[(E_t - E_c)/kT] \end{aligned} \qquad (4)$$

The activation energy E_t can then be obtained by realizing that the temperature variation of $c_n(N_c N_v)^{\frac{1}{2}}$ is slow compared to the exponential in Eq. (4) and by then using the result:

$$\frac{d(\ln \tau_g)}{d(1/T)} = \frac{1}{k}(E_c - E_t) \qquad (5)$$

A similar equation holds for dominant hole emission.

The voltage spectrum of the g-r noise has the form given by the fourth term of Eq. (1). For the 'depletion approximation', the simplest FET model considered by Sah[2], the proportionality parameter K_g for gate junction noise is given by

$$K_g = 4\left(\frac{q}{C}\right)^2 \frac{N_t AW}{3} f_t f_{tp} \qquad (6)$$

where C is the gate capacitance, N_t is trap density, AW is the volume of the gate transition region, f_t is the fraction of occupied traps and $f_{tp} = 1 - f_t$. Equation (6) will be used later in a determination of the order of magnitude of the number of traps active in generating the observed g-r noise in Region II of Fig. 1.

For g-r noise due to fluctuations of carrier density in the channel due to trapping at the shallow donors (carrier freeze out), the equivalent noise resistance is found by Sah[2] to be proportional to $\exp[2(E_C - E_D)/kT]$, where E_D is the donor level, so that approximately

$$\frac{d(\ln r_s)}{d(1/T)} = \frac{1}{k} 2(E_C - E_D). \qquad (7)$$

This expression can then be used to check on the possibility of carrier freeze out being responsible for the high series noise in Region I, Fig. 1.

EXPERIMENTAL METHODS

The measurement of the noise parameters of Eq. (1) as a function of temperature has been carried out in two different configurations: 1) ac grounded gate for the series components of the noise spectrum, and 2) normal high impedance gate mode of operation which adds the parallel components of noise.

Measurements in the first mode can be carried out with the FET in its header, as parallel insulation losses are shorted out. As will be shown below, this method allows accurate measurement of equivalent r_s and of the g-r parameters K_g and τ_g. No 1/f series component has been observed in our measurements. The FET configuration is shown schematically in Fig. 2.

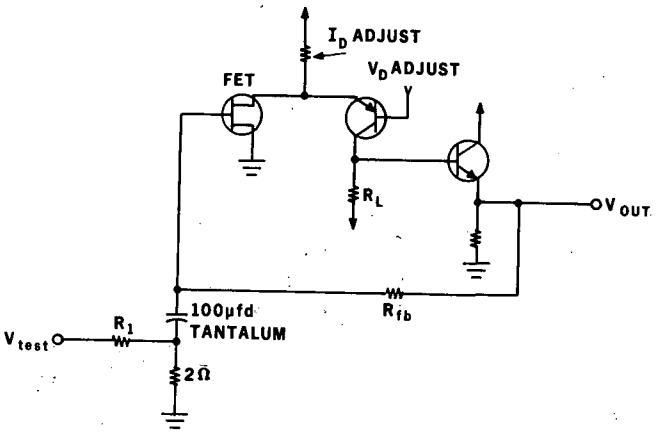

Fig. 2. Simplified circuit for grounded gate tests on FETs.

With R_{fb} large enough (1 MΩ, for example) the input cascode operates virtually as an ac open loop. Measurement of the gain from FET gate to preamplifier output allows us to refer the output noise voltage spectrum to equivalent source voltages at the input. Equation (1) becomes

$$V_{in}(f) = [4kT\, r_s + K_g\, \tau_g/(1 + \omega^2\, \tau_g^2)]^{\frac{1}{2}} \qquad (8)$$

For the measurements, FETs in their normal package were placed in an evacuated cryostat, with the can heat-sunk to an aluminum block whose temperature was servo-controlled from approximately 85K to 200K. Block temperature was measured with a copper-constantan thermocouple calibrated with a Pt resistor at liquid N_2 temperature. It is estimated that block temperatures are accurate to ± 0.5K.

Noise spectra were obtained by using a Nicolet UA-500 real time spectrum analyzer, which allows the collection of as many as 1500 data points from 10 Hz to 100 KHz in ~ 5 min with good statistics. The instrument was under control of a Hewlett-Packard Model 9830A desk calculator which selected 80 evenly spaced data points in a logarithmic scale and carried out function fittings to determine the desired noise parameters. Figure 3 shows a set of data for a typical 'good' 2N4416 in the temperature region in which g-r noise would be dominant at long τ_o (Region II, Fig. 1). The vertical scale is RMS noise voltage ($V/\sqrt{Hz}$) referred to the input. The white (series noise) part of the spectrum is evident at high frequencies, while the characteristic g-r step appears at low frequencies added to the white noise.

If one assumes that the thermal conductivity of the materials in the cooling path from the FET chip to the aluminum block is constant within the narrow range of temperature of one measurement, it is evident that the difference between chip and block temperatures will be proportional to the FET power dissipation. Furthermore, τ_g is a very sensitive function of chip temperature, so that lines of constant τ_g are lines of constant chip temperature. It follows that an extrapolation to zero power of lines of constant τ_g will yield data points corresponding to τ_g vs chip temperature. Equation (5) can then be applied to obtain (E_c-E_t) or (E_t-E_v), the trap activation energy. Figure 4 shows a set of results for τ_g vs 1000/T at three current levels, while Fig. 5 shows the lines of constant τ_g from the same measurement. The FET was operated at V_D = 4.5 V, I_D = 0.87, 2.37 and 3.87 mA.

Grounded gate measurements have also been used in a fast cycling cryostat for preselection of FETs for mounting on boron nitride, instead of the more conventional operation with high impedance gate. Since 1/f noise from the header losses dominates over the series and g-r components at medium to long τ_o, and these losses cannot be expected to have any relationship to the final 1/f behavior of the transistor once it is removed from the header, it is evident that preselection in the header can only be done on the basis of the series and g-r components of noise. We have also observed that leakage current is substantially correlated with g-r noise, as might be expected since I_L' arises at Shockley-Read centers, although the ultimate test for leakage current noise has to be carried out in a cryostat with a very good detector and the FET out of its header.

The calibration of the NLW (eV/pfd) vertical scale of the fast cycling cryostat measurement is very simple. With a 'good' transistor (not excessive g-r noise) in the grounded gate configuration of Fig. 2, a short τ_o is selected so that series noise dominates over any g-r noise present at a convenient temperature (e.g. room temperature if the FET is a 'good' one for operation at that temperature). The voltage step gain S, defined as peak voltage at the output of the main amplifier-filter divided by magnitude of voltage step at the gate of the FET, is next obtained.

The output noise voltage $V_{out}(RMS)$ is then given by

$$V_{out}(RMS) = \left[2kT\, r_s \int_{-\infty}^{\infty} |H(f)|^2 df\right]^{\frac{1}{2}} = \left[2kT\, r_s \langle N_\Delta^2 \rangle\, S^2\right]^{\frac{1}{2}} \qquad (9)$$

from the definition of $\langle N_\Delta^2 \rangle$.[1] Then, from Eq. (2) (third term) we find

$$NLW(eV/pfd) = \frac{2.35\, \bar{\varepsilon}}{q} \frac{V_{out}(RMS) \times 10^{-12}}{S} \qquad (10)$$

independent of τ_o and of the filter used. Once a calibration is obtained at short τ_o, it can be maintained at any other τ_o by changing the main amplifier gain to keep S constant.

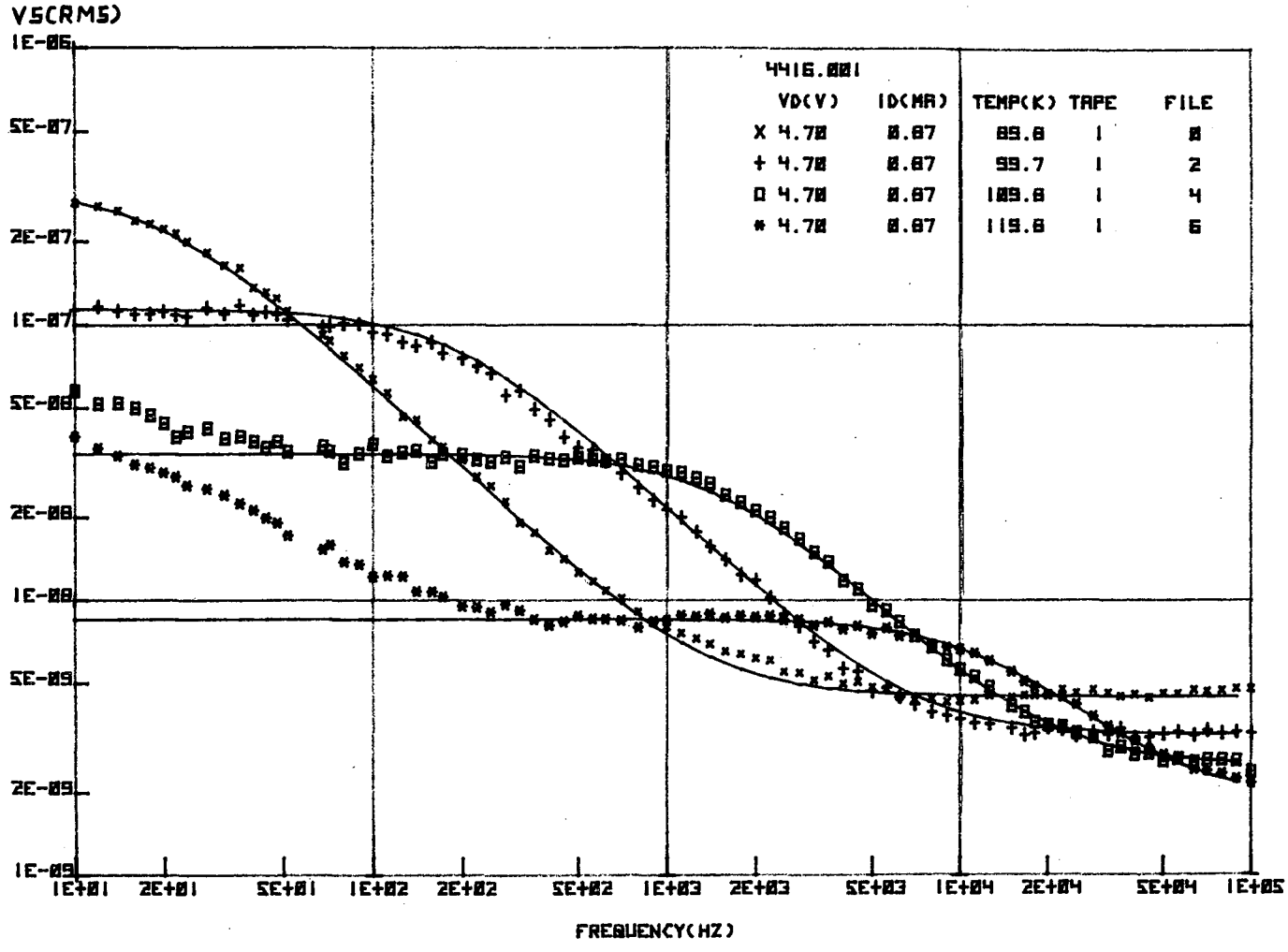

Fig. 3. Frequency domain data for the determination of g-r noise parameters from a grounded gate transistor. Solid lines are theoretical fittings of Eq. (8).

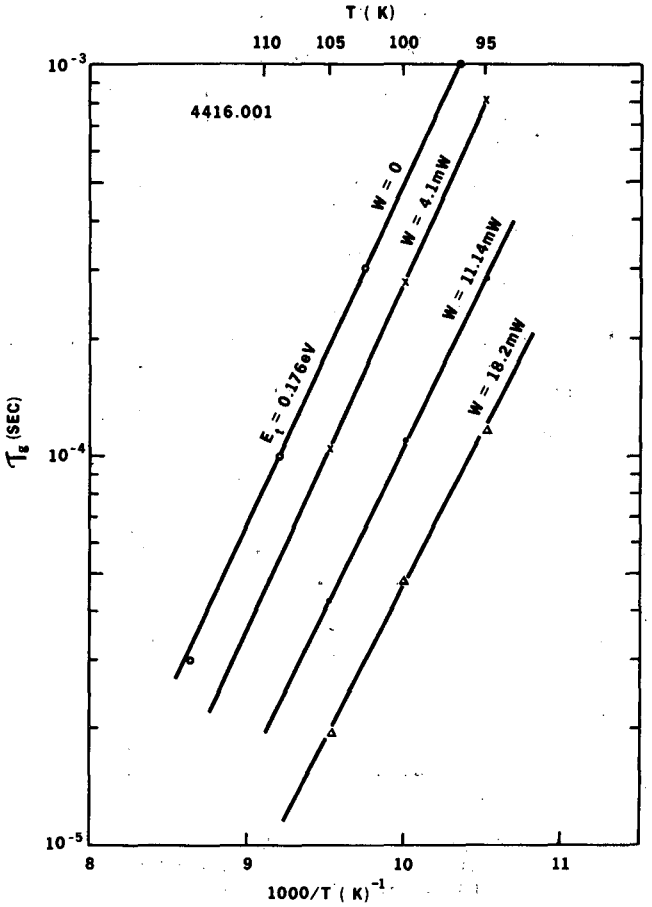

Fig. 4. Generation characteristic time τ_g vs 1000/T at three different FET power dissipations. Extrapolation to zero power gives the curve of τ_g vs chip temperature.

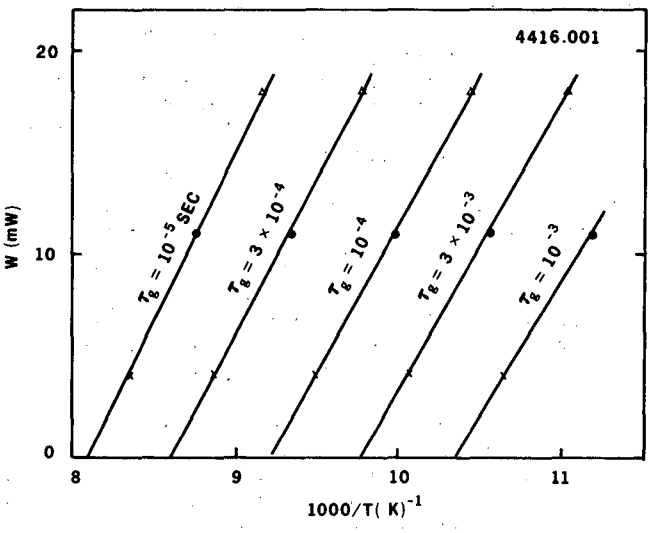

Fig. 5. Lines of constant τ_g (constant chip temperature) for the determination of zero power extrapolation.

Figure 6 shows NLW(FWHM) per pfd measured in three 2N4416s as a function of approximate cold finger temperature at τ_o = 16 μs. At the lowest temperature recorded the transistors are near the top of the g-r bump of Region II. (Note Fig. 1 records case temperature while Fig. 6 uses the cold finger temperature.) The curve for transistor 4416.002 shows no significant g-r noise as the temperature is increased above the point of minimum noise, while transistor 4416.005 exhibits a second bump at higher temperatures. The curve for transistor 4416.011 is an example of a transistor with three recognizable g-r bumps which would have good series noise at room temperature, but would be useless when cold.

As the transistors warm up their g_m decreases, so that true NLW series figures have to be divided by the relative gain vs temperature curve also shown in Fig. 6. It is found that all transistors of the same type follow this normalized gain curve.

Measurements with the gate at high input impedance have been done in a conventional opto-feedback cryostat with a Si(Li) detector of 0.3 pfd capacitance, a vacuum dielectric feedback capacitor of approximately 0.06 pfd, with the FET mounted on the boron nitride mounts described by Goulding, Walton and Malone.[4]

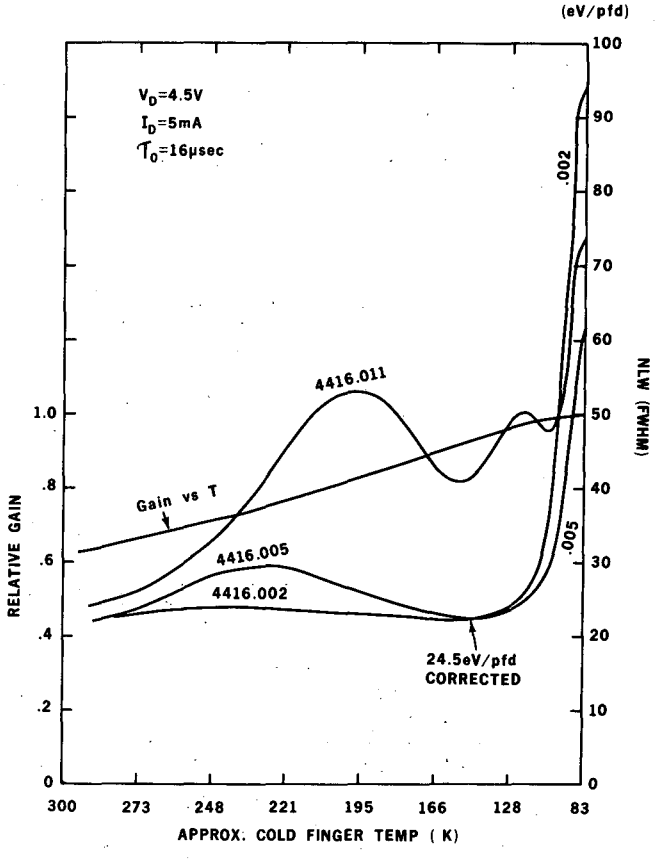

Fig. 6. Grounded gate noise measurements on three 2N4416s in which the series components of noise are shown as a capacitance noise slope. Normalized FET gain (g_m x R_L, open loop) is also shown.

RESULTS OF MEASUREMENTS

A. Region I

All 2N4416s which have been tested at low enough temperatures exhibit high series noise with a white spectrum in the frequency region measured. Churchill and Lauritzen[5] have investigated this region of operation with commercial devices and have concluded that the excess noise is due to carrier density fluctuation in the channel due to trapping and detrapping in the shallow donors or acceptors. The theory for this mechanism was initially given by Van der Ziel[6] and measurements indicating a flat spectrum up to at least 2×10^7 Hz have been carried out by Hiatt, et al.[3]

The simplest test that can confirm the correctness of the above explanation consists in applying Eq. (7) to measurements of r_s vs chip temperature in grounded gate mode and obtaining the activation energy of the responsible trap. In order to ascertain that the results were not due to carrier multiplication phenomena, three separate measurements were made at V_D = 3.7, 4.7 and 5.7 V, keeping power dissipation constant. The results are shown in Fig. 7 (r_s referred to the correct chip temperature), which give a value of $E_t = 0.041 \pm 0.005$ eV for the responsible trap at the three values of V_D tested. This result is a good agreement with the ionization energies of donors P and Sb[7] (0.045 and 0.043 eV respectively) and leaves little doubt about the basic nature of this noise source. It must be indicated that the g_m of the tested 2N4416s changes only by 3% (lower at low T) in the temperature region covered in Fig. 7, so that the excess noise observed is distinct from the thermal channel noise[8] and much higher. The characteristic g-r noise step in the frequency domain for this noise source is estimated to occur in the neighborhood of 54 MHz at 80K.[3]

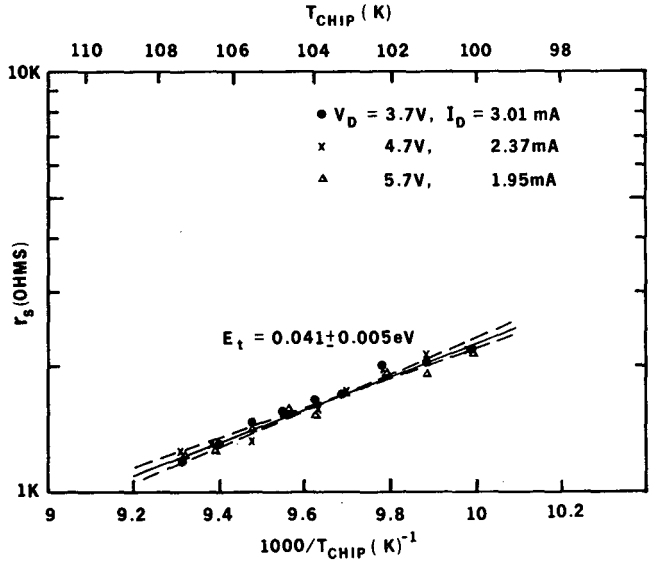

Fig. 7. Values of r_s vs 1000/T in Region I, showing the slope characteristic of shallow donor carrier freeze out.

B. Region II

In this region, noise is dominated by g-r noise caused by a trap with an activation energy of approximately 0.18 eV. Grounded gate noise plots like those of Fig. 6 obtained from more than 200 2N4416s of different batches and dates (spanning a few years), manufactured by Texas Instruments, have shown the same trap level existing with variable numbers of active traps in all transistors. Hiatt, et al[3] have also identified this level in their specially made transistors (0.19 eV) and we have also identified it in FETs made at the University of California School of Engineering, Berkeley, from high quality epitaxial material and low temperature processing.

The determination of energy level by the zero power extrapolation described above has given the results of Table 1. Slightly different values are obtained depending on the transistor mounting configuration.

TABLE I

FET	RUN NO.	E_t
4416.001	1	0.176 eV
	2	0.177 eV
	3	0.189 eV
4416.002	1	0.186 eV
	2	0.178 eV

The fitting of the experimental results by the theory for a single level trap is very good (Fig. 3) in all cases tested in detail.

The values of K_g, r_s and $1/g_m$ for transistor 4416.001 are shown as a function of chip temperature and I_D in Fig. 8, as obtained from grounded gate measurements. In order to estimate the number of active traps, we use Eq. (6). The factor N_tAW is the total number of traps in the depletion layer modified by f_t which as to be calculated from a knowledge of the potential in the reverse biased gate junction and the use of the quasi-Fermi levels. One can make a rough approximation by assuming no applied bias, with the Fermi level just below the donor levels at the n-side of the junction. The traps (assumed at the upper half of the band gap) will be filled only until the Fermi level crosses E_t, and that should occur roughly at $|(E_t-E_F)/E_{bi}| \simeq (0.18-0.05)/0.7 \simeq 0.2$ of the depletion layer thickness. For an order of magnitude calculation only, we take then $f_t = 0.2$, and $f_{tp} = 0.8$. For $K_g = 1.5 \times 10^{-11}$ and $C = 3 \times 10^{-12}$ pfd, N_tAW becomes 2.5×10^4 traps active in generating noise. The depletion layer volume can be estimated from a photomicrograph of the 2N4416 structure to be 10^{-7} cm^3, leaving $N_t = 2.5 \times 10^4/10^{-7} = 2.5 \times 10^{11}$ (cm^{-3}).

In this temperature region, the equivalent r_s due to carrier freeze out continues dropping as the temperature increases (Fig. 8) with a small dependence on I_D. On the other hand $1/g_m$ is fairly independent of temperature and quite sensitive to I_D, as expected.

As the chip temperature is increased so that the characteristic g-r step decreases in magnitude and shifts to frequencies at the high end of the filter response, (right side of g-r 'bump' in Fig. 1) we approach the optimum region of FET operation.

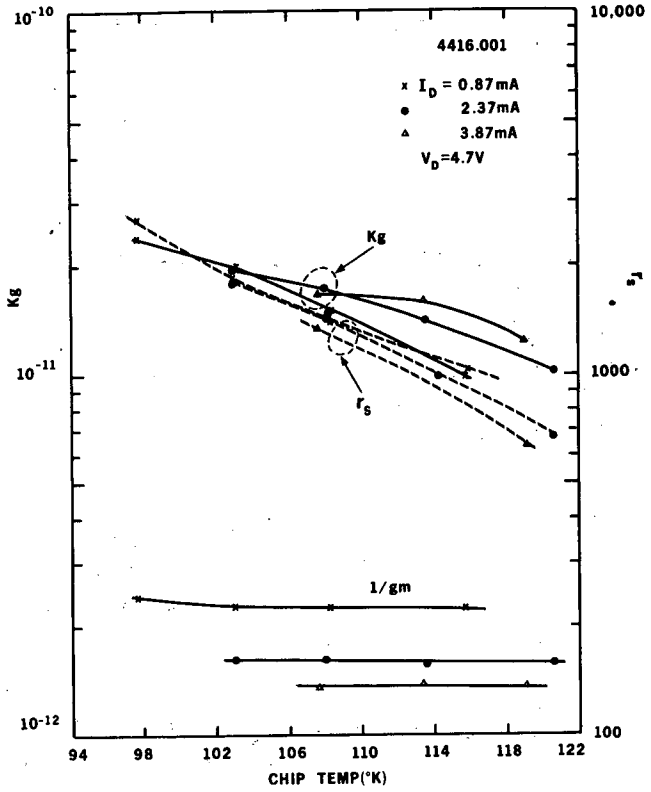

Fig. 8. Comparing r_s vs $1/g_m$ in Region II, dominated by g-r noise. Proportionality parameter K_g is also shown.

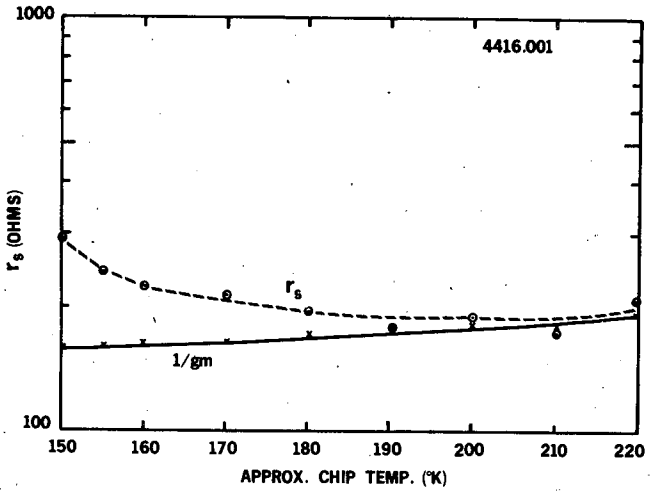

Fig. 9. Comparing r_s vs $1/g_m$ in Region III.

C. Region III

This region is characterized by a series component r_s with a value approaching $1/g_m$ at the higher temperatures, by the possible appearance of a secondary g-r bump corresponding to a deeper level and by the dominance of a parallel 1/f component which is sensitive to temperature.

Figure 9 shows the behavior of r_s and $1/g_m$ as a function of approximate chip temperature. The values of r_s are referred to the correct T. It would appear that the tail of the high noise due to carrier freeze out extends to very high temperatures, but this interpretation is in error. In fact, the excess r_s above the value of g_m is principally due to the low frequency side of the main g-r step which has shifted to frequencies above the range of measurement.

The majority of reasonably good transistors exhibit a secondary g-r bump at temperatures higher than the first bump already discussed (Fig. 6, transistors 4416.002 and .005), so that, from the noise capacitance slope (eV/pF) point of view, the optimum point (the valley between bumps) is determined by a combination of the magnitudes of the primary and secondary g-r bumps, the tail from the low-temperature carrier freeze out noise and the g_m of the FET.

The energy level of the second bump has been measured carefully for a transistor which exhibited a healthy, clean bump. The result was E_t = 0.25 eV, not as deep as a second bump reported by Hiatt, et al[3] (0.36 eV) in their transistors. The initial appearance of the secondary bump can be observed on the low frequency side of Fig. 2 for the two higher temperatures.

When the FET is operated in the normal high impedance gate mode, a strong 1/f parallel noise contribution is added. The effect of I_L' is usually negligible for good systems, except at very long τ_o.

The 1/f parallel component is temperature sensitive. Figure 10 shows the magnitude of A_α vs power delivered to a resistive heater for the FET-boron nitride package of the test opto-feedback system. Three 2N4416s were measured, two exhibiting a moderate secondary bump (4416.005 and .007) and one almost flat (4416.002). The data at a heater power of 32 mW correspond to a temperature at which the effect of the primary g-r bump at τ_o = 16 μs has just about disappeared. The overall optimum for these FETs was found to be at a point with heater power of 57 to 100 mW at I_D = 2.4 mA, V_D = 4.5 V. From Eq. (2), the contribution to total noise from this 1/f component is found to be 70 to 75 eV (FWHM) at the overall optimum point. Since FET 4416.002 exhibits practically no secondary bump, it is clear that the observed 1/f noise and its temperature dependence are not caused by g-r effects. This result and the fact that g-r effects are 'series', while all the observed 1/f is parallel, directs the search for the source of 1/f noise towards dielectric losses, as described by Radeka,[9] the first suspect being the boron nitride mount.

The dissipation factor D = G/ωC of three boron nitride parallel plate capacitors machined from actual FET mounts has been measured as a function of power delivered by the heater which is normally used to warm up the FET package. The capacitors were made in such a manner that their temperature should be near that of the FET packages at similar heater powers. The results are shown in Fig. 10. As pointed out by Radeka,[9] the 1/f noise power due to lossy dielectrics is proportional to the dissipation factor (i.e. A_α is proportional to D). The results of Fig. 10 bear out this proportionality relatively well and are a very strong indication that the temperature dependence of the 1/f parallel component of noise in Region III is due to losses in the boron nitride insulator. Furthermore, it was found earlier[1] that A_α was independent of whether vacuum dielectric or a boron nitride bulk feedback capacitor was used, and we have recently also found that surrounding the b.n. package tightly with aluminum at ground potential did not alter A_α in

any substantial way (A_α should be proportional to C_d, the dielectric capacitance from gate to ground).[9] These observations appear to indicate that we are dealing with a surface effect in the b.n. rather than a bulk effect.

The effect of the boron nitride package has been further studied by mounting three FETs directly suspended from the detector holder with no boron nitride. In this arrangement, the Si detector is held in place by a Teflon button at liquid nitrogen temperature through whose center a thick gold wire acts as the n^+ terminal of the detector and as support and heat sink for the FET. A length of 1.4 cm of the normal Kovar gate wire of the 2N4416 is adequate thermal resistance to attain optimal temperature with the FET providing its own self heating. The use of a detector with thick red paint as surface protection allows the operation of the opto-feedback LED without increasing I_L excessively. A substantial amount of microphonics is generated by the suspended FET, but measurements in frequency domain allow us to disregard unwanted points in the parameter fitting procedures.

Figure 11 shows the comparative results for transistor 4416.002, as typical of a FET mounted in boron nitride at its optimum temperature for τ_o = 16 μs, and for transistor 4416.015, as typical of the three FETs tested in the suspended arrangement. Table II shows a summary of the results of this comparison. All the measurements were carried out with the same detector.

It is evident from Table II that boron nitride adds 10 to 15 eV of 1/f noise when it is in contact with the gate at temperatures above liquid nitrogen. The source of the remaining 55 to 60 eV of 1/f noise has not been determined at this time. There is some preliminary evidence that the cold Teflon detector support is relatively noiseless and that the size of the Si detector or its surface coating has an effect on A_α.

In the process of studying the 1/f noise another peculiar noise source has been observed for which no explanation is evident at this time. Figure 12 shows the frequency domain data obtained from FET 4416.002 corresponding to the runs in Table II. As I_D is increased, the low frequency power noise spectrum takes a dependence steeper than $(1/f)^2$, which would correspond, for example, to a current source at the input with a 1/f power spectrum. This effect has been observed to a certain degree in all FETs tested in the high impedance gate configuration and it probably is responsible for the observation[10] that FETs optimized for long τ_o work best at low currents.

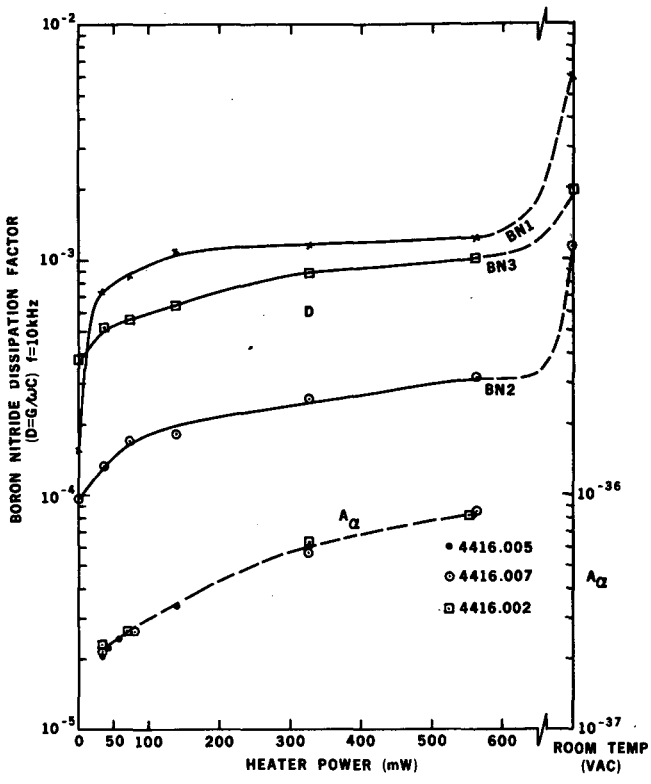

Fig. 10. Dissipation factor D for three boron nitride parallel plate capacitors, and 1/f noise parameter A_f at similar temperatures in Region III, high impedance gate operation.

TABLE II

FET	Mount	I_D (mA)	A_α	1/f Noise Contribution eV (FWHM)
4416.002	b. n.	1.99	2.49×10^{-37}	73.3
		2.40	2.32	70.6
		2.89	2.41	72.0
		3.44	2.32	70.7
		4.05	2.49	73.2
		4.74	2.35	71.1
4416.014	Suspended	2.89	1.48×10^{-37}	54.8
4416.015	Suspended	1.99	1.65	59.5
		2.41	1.72	60.8
		2.89	1.76	61.5
4416.016	Suspended	3.44	1.56	57.9
		4.05	1.46	56.0

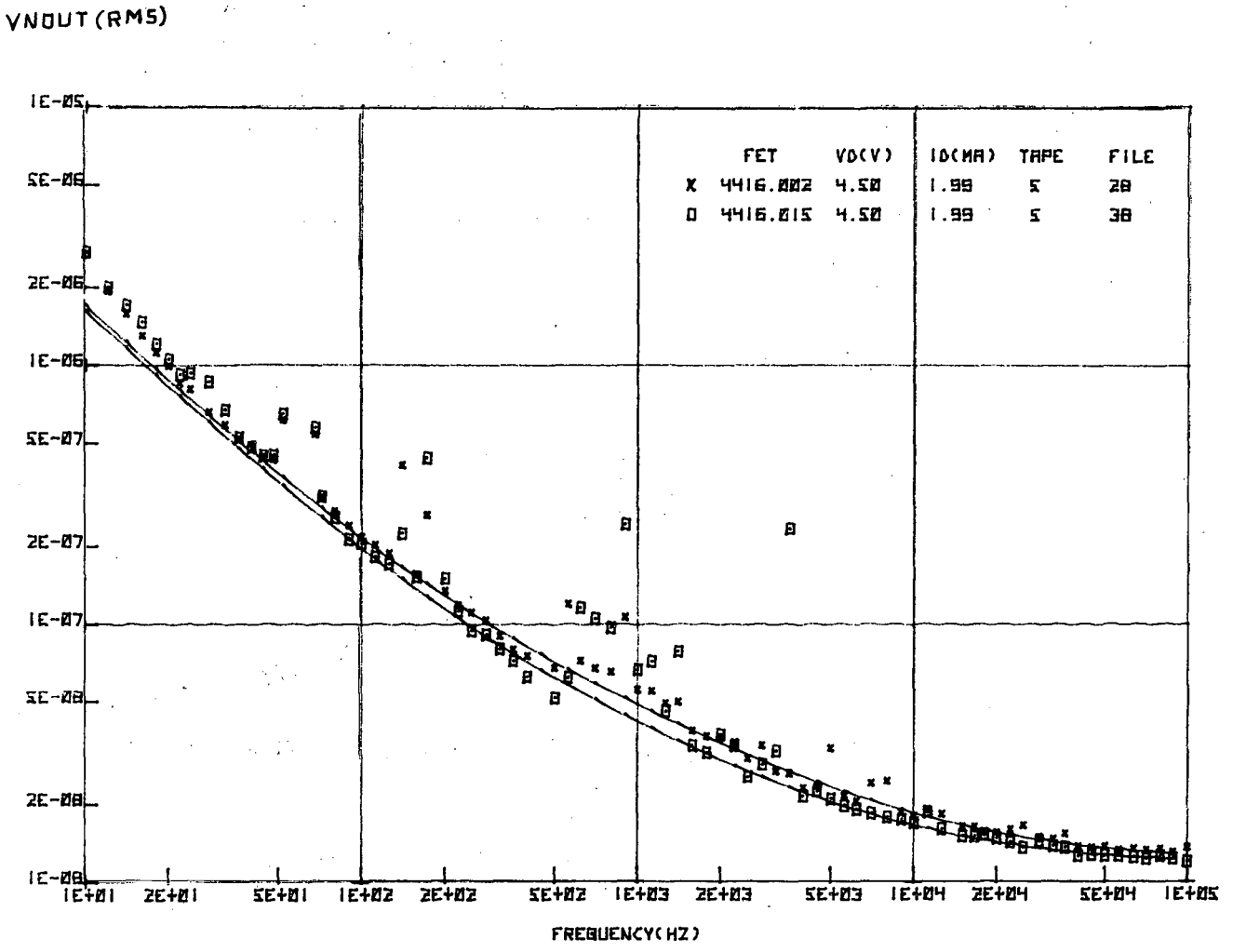

Fig. 11. Frequency domain data comparing typical spectrum of FET in boron nitride mount (4416.002) and typical one for FET suspended from detector support (4416.015). Solid lines are mathematical fittings to Eq. (1) (first three terms). Points substantially above fittings are due to 60 Hz hum and harmonics, and considerable microphonics in both cases.

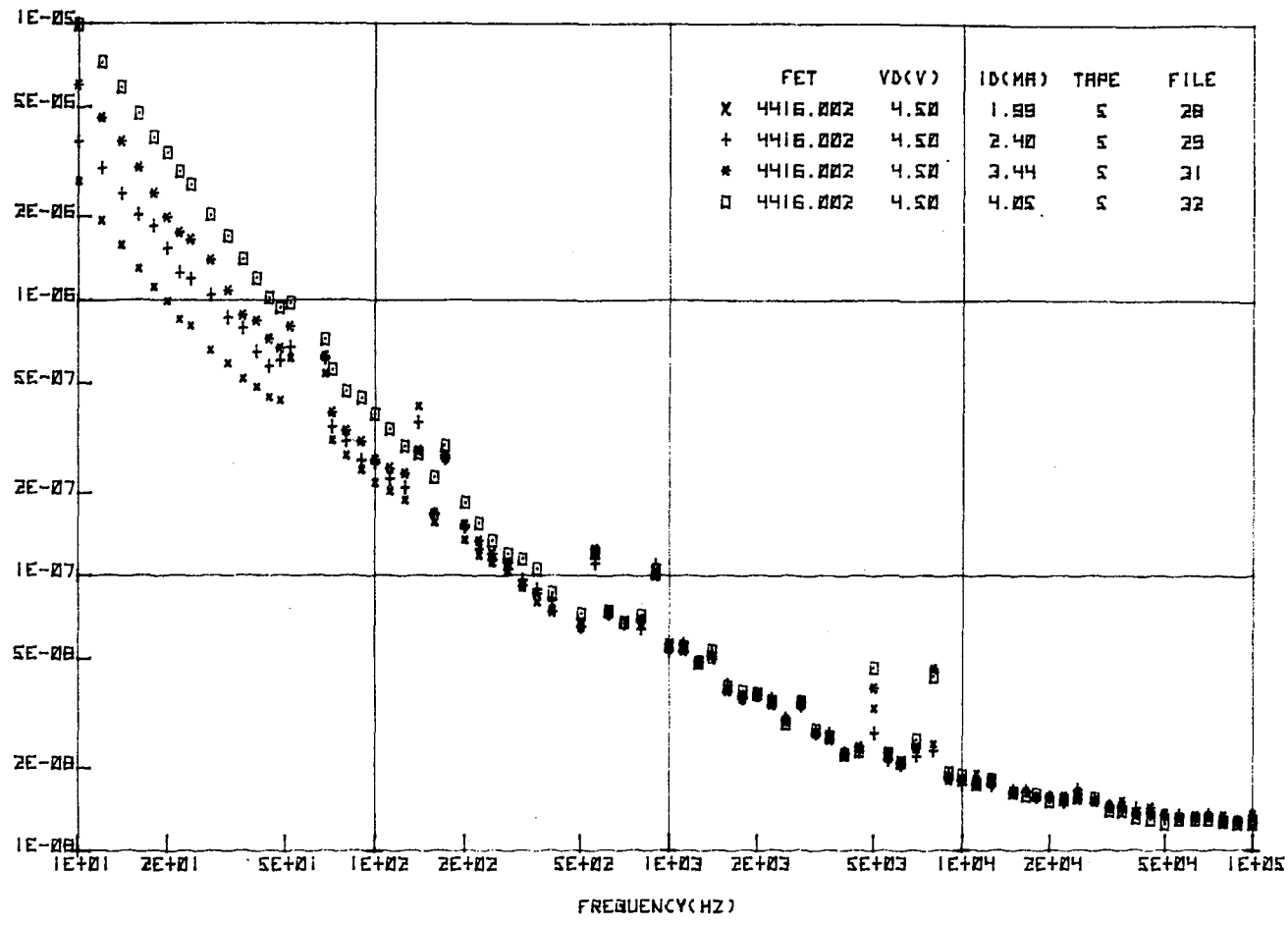

Fig. 12. Frequency domain data showing low frequency noise steeper than $(1/f)^2$ in power spectrum when I_D is increased.

DISCUSSION AND CONCLUSIONS

It is felt that the analysis presented above begins to give a coherent picture of the complex noise behavior of FETs operated at low temperatures with high impedance gate input circuits, and particularly in the case of the Texas Instruments 2N4416 FET. The interplay of the four terms of Eq. (2) in yielding a particular figure for the NLW can be followed term by term as a function of temperature. With reference to the qualitative picture of the lower graph of Fig. 1, and Figs. 7 to 9, we have shown that there exists a series channel noise contribution which is very high at low temperatures and has a white spectrum up to very high frequencies. As the FET temperature is increased this noise drops rapidly at first, with its contribution to NLW having an inverse exponential temperature dependence with shallow donor activation energy. At higher temperatures where the g-r noise becomes strong in the bandpass of a filter with long peaking time, the series white component continues dropping more slowly and it blends with the low-frequency residual effect of of the g-r noise step and the thermal channel noise as the FET temperature rises above the overall optimum operating point.

The g-r noise gives a 'bump' in the NLW characteristics due to the passing of the characteristic step of Fig. 3 through the bandpass of a filter (Fig. 1, bottom). 'Good' transistors show only one of these 'bumps', or perhaps also a second bump (Fig. 6), which could become important at higher temperatures if it is large enough. The g-r noise sources are series sources and the 'bump' shown in Fig. 1 had been interpreted in the past as series 1/f noise.

Parallel 1/f noise due to boron nitride and other insulator losses (perhaps detector surfaces, SiO_2 in FET) also appears (Fig. 1, bottom) in FETs and the substantial temperature dependence observed in FETs mounted in boron nitride has been shown to be due to surface losses in that material.

We see, therefore, that the optimum working point of a transistor, leaving aside leakage currents, is determined by a minimum of the sum of at least four different effects: 1) basic carrier freeze out noise, 2) thermal channel noise ($1/g_m$), 3) g-r noise and 4) 1/f parallel noise. At the optimum operating temperature at moderately long τ_o (16 μs, for example), the first three effects appear in one single parameter r_s, since the characteristic step of the g-r noise has moved to frequencies higher than the bandpass of the filter and is also above the range of the spectrum analyzer used inthe present measurements.

For transistors 4416.002 and 4416.015 (with and without boron nitride mount) operated at the optimum temperatures for τ_o = 16 μs, the frequency domain fittings of Fig. 11, and an assumed input capacity of 3.3 pfd yield a value for r_s of ~ 550 Ω, which places the chip temperature at about 145K, from grounded gate data on FET 4416.002. The carrier freeze out contribution at that temperature can be calculated to be equivalent to 130 Ω, and $1/g_m$ to be approximately 200 Ω, leaving 220 Ω as the residual g-r noise effect, a substantial contribution.

Then, in order to place the g-r noise in the proper perspective one has to observe, along with Fig. 1, that without g-r noise, the series contribution could drop quite substantially at the same operating temperature, or one could operate the FET at a lower temperature so that some of the temperature sensitive 1/f noise may be reduced. The lowest temperature of operation is still limited by carrier freeze out noise.

It is evident that the search for a transistor structure with higher g_m/C ratio is worthwhile to the extent that $1/g_m$ contributes to r_s, but the results presented here indicate that $1/g_m$ is only one component of r_s, to which one must add the g-r and carrier freeze out noise effects.

From the point of view of manufacturing good FETs with consistency and also for the improvement of the few which are good at present, the elimination of g-r noise becomes very important. The large majority of unselected 2N4416s exhibit very large g-r noise contributions, not only from the 'bumps' which have been called primary and secondary here, but from many other ones. The curve for 4416.011 in Fig. 6 is a relatively 'mild' one. FETs like 4416.005 in the same figure is representative of FETs which show only the primary and secondary 'bump', while all FETs tested show the primary g-r center in widely varying amounts. The identity of the centers causing g-r noise in the bad transistors cannot be established at this time. The level causing the secondary bump at E_t = 0.25 eV could very well be caused by the lower acceptor level of Cu (0.24 eV) or that of Ni (0.23 eV).[7] The energy level of the primary g-r level (see Table I) might well be the one reported by Mordkovich[11] as belonging to the SiO_4 complex. That author found an energy level of 0.16 ± 0.03 eV for the donor complex. The quantity of centers and trapping effects (and noise generation) are very dependent on details of the temperature cycle of the FET in manufacture.

The next point that needs further elucidation is that of finding the source of the remaining parallel 1/f noise, with careful experiments to separate insulator, detector and FET contributions. The appearance of the approximately 1/f current source at the gate depending on I_D is another source of noise which must be investigated.

In trying to maintain an overall perspective on the progress made in this investigation and on possible future courses of action towards the goal of FET improvement, it becomes clear that a closer relationship between the device physicist and the manufacturer will be needed if any substantial progress is to be made. Access to material handling, diffusion temperatures, etc. to check on the appearance of g-r centers, for example, is a necessity.

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