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Design of Control Systems and Topologies for High-Performance DC-DC Converters

A dissertation submitted in partial satisfaction of the requirements
for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and System)

by

Wen-Chin Brian Liu

Committee in charge:

Professor Patrick P. Mercier, Chair
Professor Gert Cauwenberghs
Professor Hanh-Phuc Le
Professor Chunting Chris Mi

2024

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University of California San Diego

2024

DEDICATION

To My Family

My Parents: Yu-Shing Liu and Chiung-Chu Chen

My Sister: Yu-Jun Liu

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- W. -C. Liu, C. -H. Cheng, P. P. Mercier and C. C. Mi, "Small-Signal Analysis and Design of Constant On-Time Controlled Buck Converters With Duty-Cycle-Independent Quality Factors," in *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 8379-8393, July 2023, doi: 10.1109/TPEL.2023.3268613.

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- W. -C. B. Liu and P. P. Mercier, "A Merged Backside Series Parallel Hybrid Piezoelectric-Resonator-Based DC-DC Converter," *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2024, pp. 2130-2135, doi: 10.1109/APEC48139.2024.10509428.
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ABSTRACT OF THE DISSERTATION

Design of Control Systems and Topologies for High-Performance DC-DC Converters

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2024

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Amid the surge in advanced technologies such as consumer electronics, the Internet of Things (IoTs), and data centers, the demands on DC-DC converters have become unprecedentedly stringent, driven by the need for miniaturized converters with enhanced performance. This requirement for high performance in a compact design presents significant challenges to current technologies, necessitating novel control strategies, materials, and topologies. For instance, voltage regulator modules (VRMs) in recent data center applications require outputs of several hundred amperes at sub-1V scales, with stringent load transient requirements where the slew rate can be as fast as 1A/ns. This demands the implementation of fast-transient, multiple-phase control strategies to support system operations. On the other hand, for miniature DC-DC converters, the

strategy typically involves increasing the operation frequency with zero-voltage switching (ZVS) technique to reduce the size of passive components, particularly magnetic components, which are recognized as the major obstacle in miniaturizing converters. However, magnetic components exhibit sub-linear volume/frequency scaling, implying limitations in minimizing converter size. Thus, the development of new materials for energy storage/processing devices, which act like magnetic components, with favorable scaling properties is desired.

This thesis introduces a novel constant on-time (COT) control strategy based on the conventional step-down converter, specifically Buck converter, for which supports multi-phase operation and delivers a fast load transient response without the need for additional ramp compensation, unlike traditional COT control schemes. Subsequently, the uses of piezoelectric materials, particularly piezoelectric resonators (PRs) are explored. The piezoelectric materials have been widely used in ultrasonic sensors, actuators, and energy harvesting applications and have recently been incorporated into power converters due to their excellent volume/frequency scaling properties, which facilitate compact DC-DC converter designs. Following the introduction of the materials, this thesis proposes and compares various hybrid PR-based DC-DC topologies across both discrete and integrated circuit (IC) implementations.

Chapter 1 Introduction

1.1 Introduction of DC-DC Converters

Power electronics, especially DC-DC converters, play a pivotal role in a wide array of applications, ranging from industrial to consumer electronics. The burgeoning of advanced technologies such as data centers and the Internet of Things (IoTs) has led to exponential growth in power demands, as depicted in Figure 1.1. According to this figure, the market size of power management ICs is projected to surge from \$34.63 billion to \$59.74 billion, nearly doubling in just a few years. Within this market expansion, voltage regulators represent the largest segment, accounting for about a quarter of the market, highlighting the importance of voltage regulators in future technological developments.

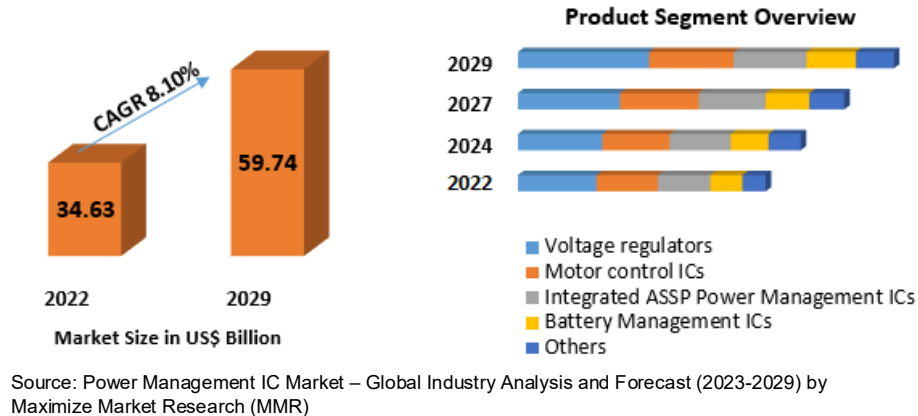


Figure 1.1 Power management IC market forecast by applications.

The development of high-performance, compact-designed voltage regulators is rapidly becoming a primary focus within the industry. Given this growing interest, the design of voltage regulators can be categorized into three main components that contribute to the final system: 1) control strategy, 2) material design, and 3) topology selection. Each plays a vital role in

engineering a voltage regulator that is both high-performing and compact. This thesis will address each aspect in detail, examining their individual contributions to the overall effectiveness of the voltage regulators.

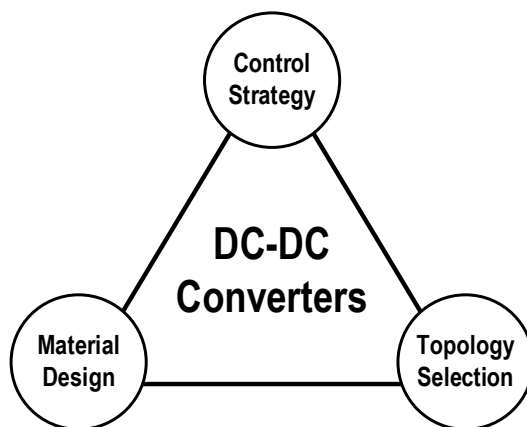


Figure 1.2 Design aspects of a high performance and compact size voltage regulator.

Conventional voltage regulators typically operate with an input voltage range of 3.3-19V, sourced from batteries, adapters, or grid-connected AC/DC converters, and deliver a sub-1V to ~3V output to power loads such as CPUs, GPUs, and peripheral I/Os. However, recent development [1] suggests that employing a 48V input voltage in regulators can reduce wire mass and size and simplify thermal management because of the reduced current required from the front-end to the regulator input given the enhanced voltage level. Consequently, there is a growing interest in 48V voltage systems.

1.2 Current Challenges for High Performance DC-DC Converters

1.2.1 Increasing Power Demands for Voltage Regulators

The dynamic power demands of central processing units (CPUs) and neural network processors continue to increase, putting increasing pressure on DC-DC-converting voltage

regulators (VRs) to supply a clean, low-ripple voltage at high efficiency across a wide dynamic range of wildly varying current loads. A representative CPU load profile is shown in Figure 1.3, illustrating that while the CPU is often in a light load condition consuming only a few watts (or less), it does occasionally, in the span of a few microseconds (or less), transition to a turbo mode where it consumes a few hundred watts. As a result of this typical operation, VRs need to have high efficiency at light-load for idle operation, fast transient response for the short transition between idle and turbo modes, and high current capability at high efficiency for turbo mode power requirements. Simultaneously being nimble to varying loads over a large dynamic range, while keeping efficiency high and voltage regulation stable is a known difficult challenge in the power electronics community.

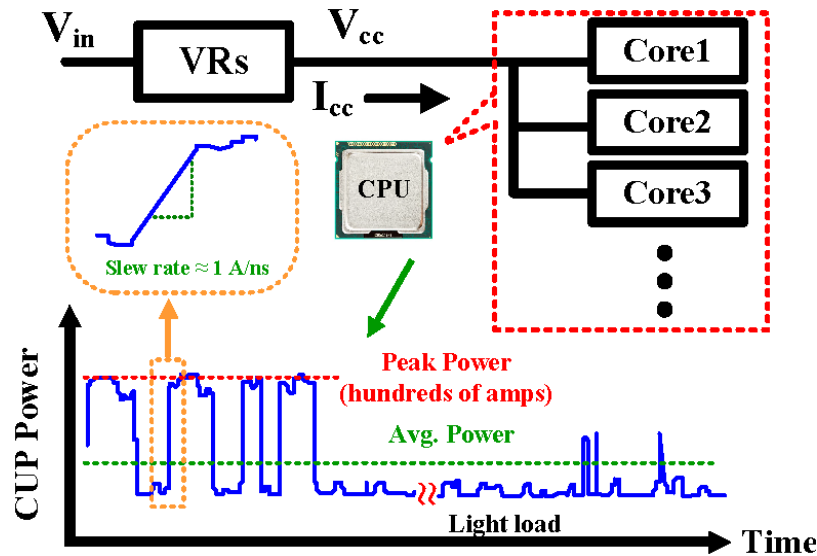


Figure 1.3 Representative transient power demands of modern CPUs.

One of the more popular control technique to attempt to deal with this problem is the constant on-time (COT) technique. Under light load operations, COT control inherently reduces its switching frequency, hence increasing overall conversion efficiency at such loads. For example, the conversion efficiency of COT-controlled buck converter can be as high as 80% at light-load

compared to around 30% with equivalent constant frequency control [3], [4]. Consequently, COT control has been widely adopted in consumer electronic devices.

COT-based control techniques also offer advantageous operation in response to high slew rate load steps (e.g., up to 1000 A/ μ s) due to its high-bandwidth design achievability, and in some cases, ultra-low susceptibility to load transient. While there are multiple COT variants [4], [5], ripple-based COT (RBCOT) control schemes have captured the most attention due to their simplicity and inherent high-load-transient immunity. However, RBCOT control schemes suffer from subharmonic oscillations if multilayer ceramic capacitors (MLCCs) are used as output capacitors, and hence, external ramp generators [6]-[8] are typically required to stabilize the system, sacrificing droop and response time to load steps.

In addition to light-load efficiency and large load step control concerns, simply operating buck converters at high output power is challenging. To help, multi-phase operation, where power is delivered through a network of time-interleaved inductors, can increase the total output power capabilities while simultaneously leveraging the multi-phase operation for reduced ripple. However, ripple reduction can be a double-edged sword if COT control is desired, since most COT control schemes rely on the current/voltage ripple to achieve modulation. As a result, multi-phase COT schemes again typically require an external ramp waveform for stable control, increasing design complexity and sacrificing performance.

1.2.2 Stability and Design Challenge across Wide-Input-Output Range

For a COT-controlled voltage regulator, the input supply voltage - either from a battery or another power rail - is typically between 4V and 24V, while the CPU and SoC loads generally require 0.5V to 3.3V. A wide input-to-output voltage range requires a wide duty-cycle range in a

COT-based Buck converter controller, which can lead to concerns regarding stability, especially when a high-bandwidth, rapid response time design is desired.

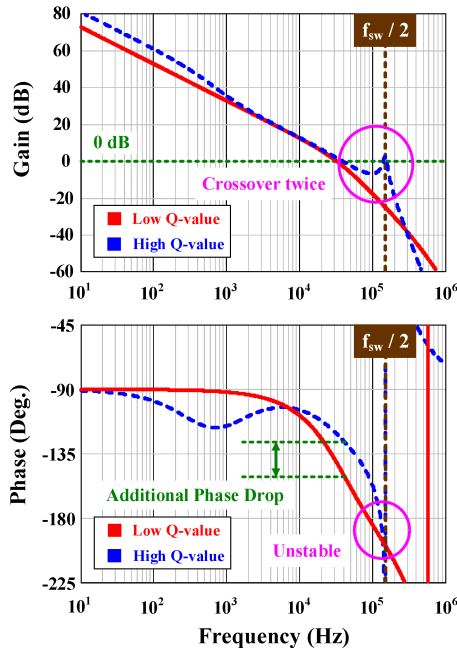
Since the location of high-frequency complex poles in a COT system is usually a function of duty cycle[5]-[10], it is possible that duty-cycle variation can move these poles to the right-hand plane (RHP), resulting in system instability. During stable operation, the duty cycle and the output voltage operate normally; however, in an unstable condition, the duty cycle shows a subharmonic oscillation, making the output voltage ripple significantly larger than in the stable condition. Due to the large potential dynamic range of duty cycle in consumer electronics applications, additional attention is thus required when designing a COT-controlled Buck converter.

A wide input-to-output voltage range also presents increased challenges towards a high bandwidth COT design because, again, the location of poles, especially the high-frequency conjugate poles, are a function of duty cycle. For a pair of conjugate poles, the location can be represented by the frequency and the quality factor, Q , where the value of Q indicates the damping ratio of a system (i.e., $Q = \frac{1}{2\xi}$), implying the poles' distance toward the real and the imaginary axis in the B-plane. Combining the statements above, Q is thus also a function of duty cycle because the poles, whose locations are highly related to duty cycle, can be partially represented by Q [5]-[11].

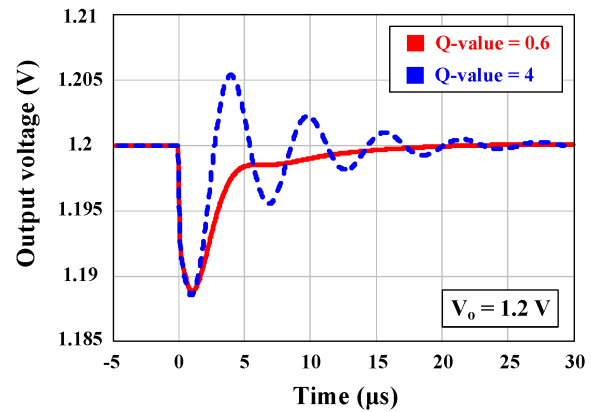
A design example of an ultra-fast transient COT (UFTCOT) control [12] with simple type II compensation is shown in Figure 1.4(a) to illustrate the challenges when Q varies due to changes in duty cycle. Under a low- Q , low duty cycle, situation (the solid line), the complex poles split into two real poles, which move toward the low-frequency and the high-frequency regions, respectively. This can add some additional phase drop near the unity gain bandwidth, potentially presenting stability issues. On the other hand, in the high- Q , high duty cycle, situation (the dashed line), the

gain at high frequencies may cross 0 dB twice for a high bandwidth design, as highlighted by the solid pink lines, resulting in instability. From this example, it should be clear that either a low or high Q can be detrimental to a system. Unfortunately, most COT-controlled buck converters suffer from the Q -value issue. Hence, to avoid this issue, a well-controlled and duty-cycle-independent Q -value is desired for a wide-duty-cycle-range operation in a COT controller.

In addition to stability and high bandwidth challenges, load transient performance is also affected by the wide-duty-cycle-range operation since the duty-cycle variation affects system behavior yet again. Specifically, the output impedance of a converter, which is often used to evaluate load transient response, also has a dependence on Q [5],[6]. As is well known in control theory, if a step response is applied to a high Q -value system, ringing can become significant, which is not desirable in a well-designed system. Thus, a high Q -value should be prevented under a wide-duty-cycle-range operation.



(a) High bandwidth design challenge



(a) Load transient design challenge

Figure 1.4 Wide-input-output range design challenges.

To further explore the effect of Q -value on load transient performance, a step response simulation can be performed on the closed-loop output impedance. Here, the closed-loop output impedance, Z_{oc} , is defined as $Z_o(s)/[1 + T(s)]$, and $T(s)$ is the loop gain, which is defined as the sum of gain around the feedback loop (i.e., $T(s) = G_{vc}(s) \times H_v(s)$). For the closed-loop compensation, $H_v(s)$, a simple type II compensation with pole/zero cancellation is applied. The step-response results with Q -values of 0.6 and 4 are shown in Figure 1.4(b). It can be seen that the ringing effect is exacerbated as the Q -value is increased. Therefore, a well-controlled Q -value is typically required to optimize the load transient behavior and prevent excessive undershoot/overshoot in a wide-duty-range operation.

Table 1.1 Literature review for COT-controlled Buck converter in a wide-range operation.

Literature	Specific control	Implementation	Limitation
S. Bari <i>et al.</i> [10]	Inverse-charge COT	An adaptive threshold voltage proportional to the output voltage.	Q -value variation is reduced but still varies with duty ratios. Load transient is not optimized.
K. Cheng <i>et al.</i> [13]	Ripple-based COT	An internally adaptive ramp generated by high-pass filter.	Enhanced stability and transient response but Q -value variation is not discussed.
T. Qian <i>et al.</i> [14]	Ripple-based COT	An adaptive ramp achieved by off-time sensing	Only discussed stability issue, Q -value appears to vary with duty ratios.
W. Liu <i>et al.</i> [15]	Ripple-based COT	An adaptive ramp controlled by input/output voltage and duty signal	Stability and transient response is improved but Q -value only nearly constant; namely, it still varies with duty ratios.
Y. Lin <i>et al.</i> [16]	Ripple-based COT	A virtual inductor current ramp generated from low-pass filter	Q -value varies significantly over a wide-duty-cycle range to ensure stability a large ramp typically required, sacrificing transient performance.
K. Kong <i>et al.</i> [17]	Ripple-based COT	An adaptive ramp generated by duty signal feedback and sample-and-hold circuit	A constant Q -value is achieved to improve both stability and transient response, but the system exists low-frequency poles, limiting high-bandwidth design. Besides, the Q -value exists a minimum value, confining the design flexibility.

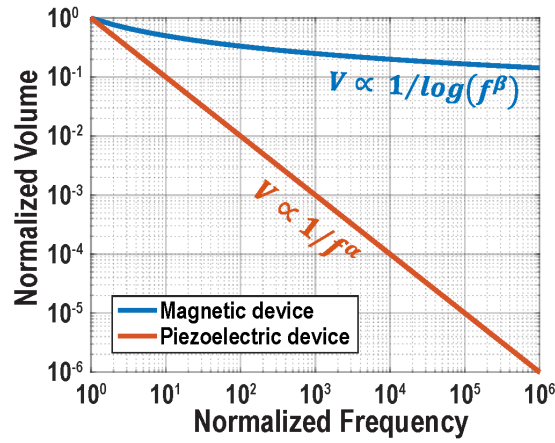
In summary, duty-cycle variation, as expected in many consumer electronics applications, poses significant challenges to stability, bandwidth, and response time, largely due to corresponding variations in Q . Unfortunately, most of the COT-controlled Buck converters suffer from the exact same difficulties mentioned above because the Q shows up at the half-switching frequency in the small-signal models. [10],[13]-[17] reported different adaptive methods to reduce Q variation over the wide-duty-cycle-range operation, improving stability and transient response performance while alleviating difficulties in bandwidth design, as illustrated in Table 1.1, most of them (e.g.,[10], [13]-[16]) cannot entirely remove the variation caused by the change of duty ratios. Though the method proposed in [17] can achieve an invariant Q -value, the developed system has a pair of low-frequency ($< f_{sw}/2$) conjugate poles, limiting high-bandwidth design. Besides, there is a lower limit for the Q -value design in [17], confining the design flexibility. Instead, a simple, well-controlled, and duty-cycle-independent Q -value, also known as constant Q -value, is desired for COT-controlled Buck converters.

1.2.3 Sublinear Properties of Inductors and Potential Alternative:

Piezoelectric Resonators

The increasing demands for high-efficiency, lightweight, and low-cost miniaturized power converters are starting to highlight the limitations posed by magnetic passive elements. While conventional electromagnetic-based converters are renowned for their fast response, ease of control, and high-power capability, the sublinear scaling property of magnetic components [18], where the magnetic size reduces nonlinearly with an increase in frequency, limits the pathway towards converter miniaturization, as shown in Figure 1.5(a). Consequently, there is a growing interest in exploring alternative energy storage forms, materials, and devices to replace magnetic

components [19], encompassing diverse manifestations such as kinetic, elastic, and electrostatic energy storage.



(a)



(b)

Figure 1.5 (a) Volume versus frequency scaling of magnetics and PRs, (b) Planar form-factor of the PR compared to an inductor and 5 cents USD.

Piezoelectric devices are one of the prospective candidates, as they can be easily batch fabricated at low cost, offer thin planar form factors, and, importantly, offer linear frequency/volume scaling properties as shown in Figure 1.5. These devices store energy in the form of elastic energy and can be implemented in multi-port or single-port forms: piezoelectric transformers (PTs) and piezoelectric resonators (PRs), respectively. PTs were previously found applications in push-pull [20], class E [21], [22], and half/full-bridge [23] converters implemented along with magnetic components. To eliminate the use of magnetics, magnetic-less PT-based

converters have also been explored [24], [25] However, due to efficiency limitations [26], [27] and zero voltage switching constraint [25], PTs have not gained widespread adoption yet. PRs, on the other hand, have emerged as particularly promising alternatives to inductors in DC-DC converters. Recent works demonstrated both step-up and step-down magnetic-free converters with promising gains in efficiency [28]-[30] and power density [31], [32], thereby affirming the effectiveness of PRs.

1.2.4 Challenges in Adopting Piezoelectric Resonators to Existing DC-DC Converters

Though PRs are identified as good alternatives to inductors, they do not serve as direct replacements. The Butterworth Van-Dyke (BVD) model [33], as depicted in Figure 1.6, is a commonly adopted electrical equivalent model for PRs, where the model is comprised of mechanical components, R , L , and C , and a piezo-static capacitor, C_P . Notably, the equivalent model functions as a DC block component, making PRs unsuitable for conventional inductor-based converters. Hence, modified topologies and modulation laws are required to achieve optimal operation of PR-based converters.

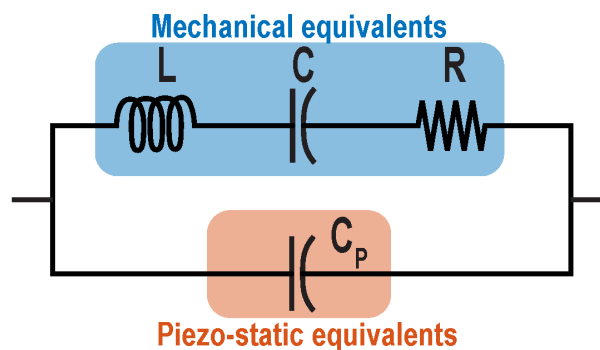


Figure 1.6 Butterworth Van-Dyke equivalent model for piezoelectric resonators.

1.2.5 Reduced Efficiency at Low Voltage Conversion Ratio for PR-based Converter

There are a variety of inductor-less PR-based DC-DC converters reported [28]-[30] for step-up or step-down conversion. This work specifically focuses on step-down conversion with voltage conversion ratios (VCRs), denoted as $VCR = V_o/V_{in}$, less than 0.25. Among the high-step-down topologies, the baseline PR-based DC-DC converter, as shown in Figure 1.7, was reported to be one of the most efficient topologies [26] for $VCRs \leq 0.5$ scenarios. By operating the PR in the inductive resonating region, zero-voltage switching (ZVS) across all switches and soft-charging of the piezo-static capacitor, C_p , can be achieved, leading to low overall losses.

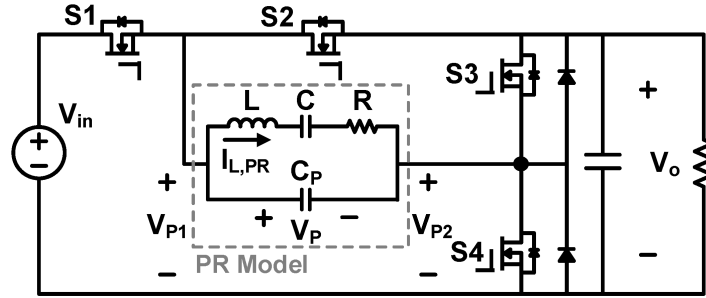


Figure 1.7 Baseline PR-based converter.

However, the baseline PR-based converter achieves its optimal efficiency at a VCR of 0.5, with performance degrading as the operations deviate from the optimal point, as shown in Figure 1.8. At a VCR of 0.5, the efficiency of the baseline PR-based converter reaches an impressive 97%, but decreases dramatically as VCR decreases, reducing to 90% and 80% at 0.2 and 0.1 VCR, respectively. Unfortunately, a great number of step-down DC-DC applications require a much larger conversion ratio (i.e., $VCRs \leq 0.2$ or even more $VCRs \leq 0.1$), and the efficiency degradation limits the appeal of the baseline PR-based converter adoption in such applications.

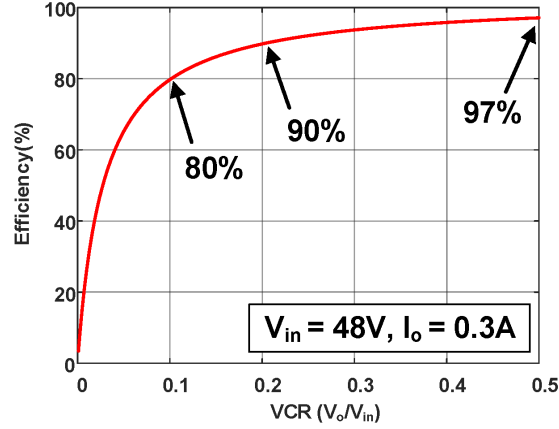


Figure 1.8 Efficiency curve example of baseline PR-based converter.

1.2.6 Lack of Integrated-Circuit-Implemented PR-based DC-DC Converters

Though there are a variety of PR-based converters proposed [20]-[32], none has been implemented in integrated circuit design, nor have they been designed for low VCR scenarios ($VCRs \leq 0.1$). Hence, there is a clear need for an integrated-circuit-implemented PR-based converter, moving toward the miniature scale yet high performance DC-DC design.

1.3 Thesis Contributions

This thesis presents multiple strategies in designing high-performance and compact DC-DC converter that can potentially be utilized in future consumer electronics, cloud computing, automotive, and aerospace applications. As illustrated in Figure 1.2, there are three main aspects of DC-DC converter design: 1) control strategies, 2) materials, and 3) topologies where each of them will be introduced in this thesis.

Chapter 2 delves into the conventional voltage regulator design with a novel constant on-time (COT) control scheme. Here, an ultra-fast transient constant on-time (UFTCOT) control is proposed to improve load transient performance while enabling simple multi-phase operation,

demonstrating 6x faster transient response than conventional inverse-charge constant on time (IQCOT) control. Moreover, the small-signal models for UFTCOT control are also derived, providing system design guidelines, and verifying its transient performance. In addition, a generalized strategy to design a well-controlled and duty-cycle-independent quality factor for COT-controlled Buck converters is proposed with a design example under a baseline UFTCOT control scheme presented. The proposed design strategy can be easily extended and applied to several other state-of-the-art COT control schemes.

Chapter 3 focuses on the hybrid piezoelectric-resonator-based (PR-based) DC-DC converters with the new 48V system, which is introduced in Chapter 1.1. In this chapter, the piezoelectric resonators (PRs) and novel hybrid PR-based DC-DC converter topologies are presents. Here, the Frontside Series/Parallel PR-based (FSPPR) and Backside Series/Parallel PR-based (BSPPR) DC-DC converters are proposed to improve the performance of conventional PR-based converters at low voltage conversion ratios (VCRs), i.e., $VCR \leq 0.25$. These hybrid PR-based converters leverage the concept of switched capacitor hybridization, popularized by inductor-based DC-DC converters in recent years, to enable optimal operation of the PRs while all while maintaining an overall compact size and all of the advantages of PR-based converters, i.e., ZVS and soft-charging of capacitors. Finally, the converter prototypes are built with a disk-shaped PZT piezoelectric resonator operating in a radial vibration mode and can be reconfigured as a co-designed baseline PR-based converter for fair comparisons.

Chapter 4 introduces the integrated circuit design for the dual-side series/parallel PR-based (DSPPR) converter implemented in 180 nm BDC technology, striving to improve efficiencies at low VCRs, ($VCR \leq 0.1$), while minimizing the silicon and PR area. Incorporating a hybrid approach, popularized in hybrid buck converters, two SCs are merged to the frontside and backside

of the baseline PR-based converter, respectively. This configuration enables an optimal efficiency point of 0.125VCR while placing the PR at the high voltage/low current side, thereby reducing the current stress over PR as well as the current-related losses. Finally, the system is designed and tested under 16-20/ 1.1-2.2V conditions, revealing a peak efficiency of 92.9%, making a 13%-20% efficiency enhancement, a 13x-23x active area reduction, and a 1.7x-2.5x output capability improvement compared to co-designed PR-based converters.

Chapter 5 review the state-of-the-art hybrid PR-based converters and the baseline PR-based converter by analyzing their PR operation and utilization. Then, a device modeling framework for PRs is proposed along with active switches and capacitors models revisited. This PR framework incorporates the geometrical dimensions and piezoelectric constants to develop a size-ratio-to-loss model, serving as a powerful tool in optimizing PR size and comparing different PR-based topologies. Subsequently, comprehensive comparisons of hybrid PR-based converters are performed, focusing on power density and maximum achievable efficiency. These comparisons assess PR current amplitude, operating frequency, active/passive footprint, and total loss, offering insights into various PR-based converter designs. A discrete reconfigurable prototype capable of configuring as DSPPR, BSPPR, FSPPR, and baseline PR-based converters is built using PIC181 disk-shaped radial mode PRs in different size ratios (20/0.2 mm, 20/1 mm, and 20/2 mm in diameter and thickness).

Chapter 6 proposes a new control strategy, demonstrating the first closed-loop control for the hybrid PR-based converters. Each control timing is illustrated in detail and, accordingly, the driving strategy is concluded. By examining the out-of-phase waveforms of PR, a state machine is designed for PLL control. In addition, the regulation and loss minimization loops are enabled to achieve ideal operation with regulation. Finally, a prototype is built featuring a disk-shaped PIC

181 PR with dimensions of (20/0.2)mm in radius and thickness where the closed-loop control is realized by a digital controller. The measurement results validate the proposed control strategy and demonstrate the regulation ability.

Chapter 2 A Novel Ultra-Fast Transient Constant On-Time Buck Converter with Duty-Cycle-Independent Quality

Factors Design for Multi-Phase Operation

2.1 Review of Constant-On Time Control Schemes for Multi-Phase Operations

In this section, three different multi-phase control schemes will be discussed: current-mode COT (CMCOT), inverse-charge COT (IQCOT), and ripple-based COT (RBCOT). The small-signal models for each approach will be derived, facilitating direct comparison of the control-to-output transfer functions and of the output impedances.

2.1.1 Control Laws for CMCOT, IQCOT, and RBCOT

2.1.1.1 Current Mode Constant-On Time (CMCOT) Control Scheme

The CMCOT control scheme, shown in Figure 2.1(a) possesses two feedback loops: 1) the inner loop is the current sensing loop, converting the summed current, I_{sum} , from the two inductor phases, into a voltage signal via, R_i , fed to the negative terminal of the comparator; and 2) the outer loop is a voltage feedback loop, converting the error signal between the output voltage and a reference voltage into a control voltage, V_c , fed to the positive terminal of the comparator. Once the sensed $I_{sum} \times R_i$ reaches V_c , the phase manager is triggered and determines the turn-on instance of each phase. That is, this control utilizes the sum current ripple in modulation. However, as shown in Figure 2.1(a), the sum current ripple is eliminated at the ripple cancellation point (i.e., when both inductors are perfectly out of phases), and hence the modulation cannot be achieved

merely by the current ripple, leading to system instability at this important operating point. To prevent an unstable condition and to improve noise immunity at the ripple cancellation point, an external ramp which is purposefully added to V_c to avoid this issue is required under multi-phase operation.

2.1.1.2 Inverse-Charge Constant-On Time (IQCOT) Control Scheme

Compared to CMCOT control, IQCOT control is inherently suitable for multi-phase operation because the ramp generation process is built directly into the feedback loop design. As shown in Figure 2.1(b), the control voltage, V_c is generated from error amplifier, which is then subtracted by sensed inductor current. The voltage difference between the control signal and the sensed current is fed into a transconductor that generates a proportional current used to charge capacitor C_q . Then, the voltage across C_q is fed to the positive terminal of the comparator and compared with a constant threshold voltage, $V_{th,const.}$, to determine the turn-on instance for each phase. Owing to the charging process in the modulation loop, the system can properly operate in a multi-phase circuit, even when the two inductors are operating perfectly out of phase for maximum ripple reduction, as shown in Figure 2.1(b). Besides, the inverse charge method supports better noise immunity than conventional charge control [10].

2.1.1.3 Ripple-Based Constant-On Time (RBCOT) Control Scheme

The RBCOT control scheme is illustrated in Figure 2.1(c). Its modulation law is very similar to CMCOT, in the sense that the output voltage is compared to a reference voltage, generating an error control signal V_c , to which an external ramp signal is added prior to reaching the positive terminal of the comparator. Unlike CMCOT, however, instead of sensing the summed

current, the output voltage is directly driven to the negative terminal of the comparator. A major benefit of voltage sensing is that the modulator can respond to load transient immediately, and as a result, RBCOT can have the best load transient response performance. However, since the output voltage consists of the capacitor voltage ripple and the equivalent series resistor (ESR) voltage ripple, the phase delay issue between the capacitor voltage and the output voltage might result in subharmonic oscillations. Moreover, similar to CMCOT control, the interleaving operation further degrades stability due to ripple cancellation, as shown in Figure 2.1(c), which is why an external ramp is again required to address stability concerns.

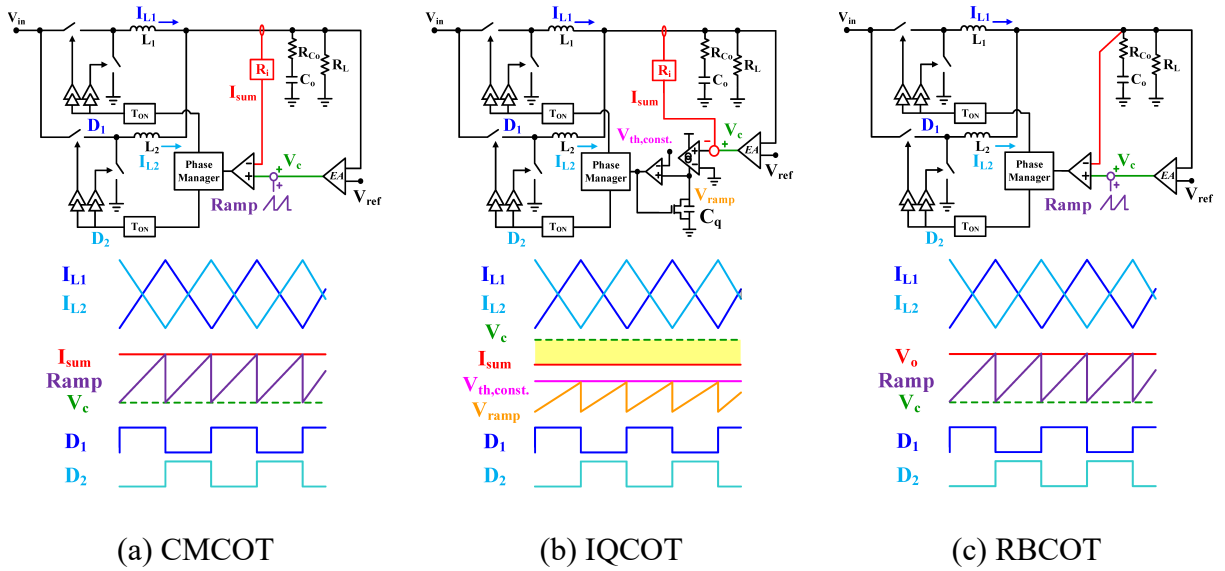


Figure 2.1 Circuit diagrams and modulation waveforms.

2.1.2 Control-to-Output Transfer Function of the COT schemes

The control-to-output transfer function, $G_{vc}(s)$, of CMCOT control with an external ramp is shown in equation (2.1), while the plots can be found in [34],[35]. From equation (2.1), it can be seen that an additional pair of conjugate zeros and poles are introduced due to external ramp compensation. Since $Q_1 = 2/\pi$, $\omega_1 = \pi/T_{on}$, and $\omega_2 = \pi/T_{sw}$, the frequency and Q -value of the

conjugate zeros are constant and independent of the external ramp's slope. In contrast, the Q -value of the additional conjugate poles vary with the slope of the external ramp. In practice, the slope of the external ramp should not be large in order to prevent extra low-frequency phase drop caused by the split poles. As a result, the complex poles and zeros can approximately cancel each other, and thus the loop gain can be efficiently designed to achieve a high bandwidth because only a single pole dominates. Besides, unlike other COT-based controls (i.e., RBCOT and IQCOT) whose conjugate poles at $\omega_2 = \pi/T_{sw}$ in $G_{vc}(s)$ might move to right-half plane (RHP) because of a negative Q -value, causing system instability, there are no stability concerns even when an external ramp is applied in CMCOT because the Q -value of the conjugate poles at $\omega_2 = \pi/T_{sw}$ is always a positive value.

The $G_{vc}(s)$ of the IQCOT control [10], described in (2.2), is similar to CMCOT but without the conjugate zeros. Besides, the quality factor, Q_3 , at ω_2 in IQCOT control is different from the quality factor, Q_2 , in CMCOT control where ω_2 is equal to half-switching frequency, $f_{sw}/2$. Here, the complex pole at $f_{sw}/2$ may cause the stability issue if Q_3 , becomes a negative value, and thus the stability of this control technique depends strongly on the control stage parameters. In addition, owing to the complex poles, there is an extreme phase drop that appears at $f_{sw}/2$. Consequently, compared to CMCOT, the design of the loop gain bandwidth will be limited. Yet, this control does not require an external ramp; hence, $G_{vc}(s)$ for multi-phase will have the same $G_{vc}(s)$ as a single-phase design, which is a appealing benefit. Note that the plot for $G_{vc}(s)$ for IQCOT control is available in [10]

Equation (2.3) shows the $G_{vc}(s)$ of RBCOT control, and its graphical illustration is shown in [6]. As shown, $G_{vc}(s)$ here is by far the most complicated one, and since it is not easy to separate the poles and zeros, it is difficult to analyze and design well. According to [35], if a large external

ramp is applied to this control technique, it will cause gain peaking at both low and high frequencies, which seriously degrades the achievable bandwidth. Conversely, a small external ramp causes an unstable condition. Hence, a proper external ramp design is essential in this control scheme to achieve high bandwidth and stable performance. Generally, the external ramp design is recommended as 2-6 times falling slope of the sensed inductor current[35].

$$\frac{\hat{v}_o(s)}{\hat{v}_{c,CM}(s)} \approx K_c \frac{(R_{Co}C_o s + 1)}{s/\omega_a + 1} \frac{1}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \left(\frac{1 + \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2}}{1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}} \right) \quad (2.1)$$

$$\frac{\hat{v}_o(s)}{\hat{v}_{c,IQ}(s)} \approx K_c \frac{(R_{Co}C_o s + 1)}{s/\omega_a + 1} \frac{1}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \frac{1}{1 + \frac{s}{Q_3\omega_2} + \frac{s^2}{\omega_2^2}} \quad (2.2)$$

$$\frac{\hat{v}_o(s)}{\hat{v}_{c,RB}(s)} \approx \frac{(R_{Co}C_o s + 1)}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \frac{1 + \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2}}{\left(1 + \frac{s}{Q_4\omega_2} + \frac{s^2}{\omega_2^2}\right) \left(1 + \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2}\right) + \frac{S_e}{S_f} R_{Co}C_o T_{sw} s^2} \quad (2.3)$$

Where,

$$K_c = \frac{R_L}{R_i(1 - R_L \times k_2)}, \omega_a = \frac{1 - R_L \times k_2}{(R_L + R_{Co})C_o - R_L R_{Co}C_o \times k_2}$$

$$k_{2(CMCOT)} = -\frac{1}{2} \frac{T_{on} R_i}{L_s}, k_{2(IQCOT)} = -\frac{C_T}{g_m} \frac{V_{th,const.}}{V_{in} R_i T_{on}}$$

$$\omega_1 = \pi/T_{on}, \omega_2 = \pi/T_{sw}, Q_1 = 2/\pi$$

$$Q_2 = \frac{1}{\pi \left(\frac{1}{2} + \frac{S_e}{S_f} \right)}, Q_3 = \frac{2S_f T_{on}}{\pi D \left(\frac{2C_T V_{th,const} D}{g_m T_{on}} - S_f T_{on} \right)}, Q_4 = \frac{T_{sw}}{\pi \left(R_{Co}C - \frac{T_{on}}{2} \right)}, S_f = R_i \frac{V_o}{L_s}$$

2.1.3 Output Impedance of the COT Schemes

The output impedance, $Z_o(s)$, between CMCOT and IQCOT control approaches are fairly similar because both of them are current-mode-based control and affected by the k_2 term, where the k_2 term is defined as a transfer function from the output voltage to the inductor current. Because the inductor current can be viewed as an ideal current source under current-mode-based control, the output impedance will be equal to the impedance converting the inductor current into an output voltage. Hence, the output impedance can be obtained from the output network and k_2 . Finally, the output impedance is the output network in parallel with the negative reciprocal of k_2 [36], as shown in equation (2.4). In RBCOT control, the feedback loop is slightly different compared to the others because the feedback signal is not a current but a voltage. The output impedance $Z_o(s)$ is shown in equation (2.5), where $G_{vc}(s)$ is illustrated in equation (2.3).

$$Z_{o1}(s) = \left(\frac{-1}{k_2} // \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1} \right) \quad (2.4)$$

$$Z_{o2}(s) \approx (G_{vc}(s) - 1) \frac{R_{Co}C_o s + 1}{C_o s} \quad (2.5)$$

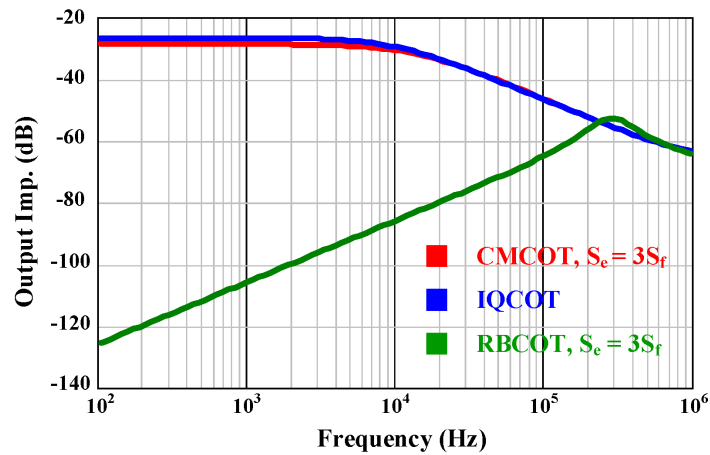


Figure 2.2 Output impedance comparison for CMCOT, IQCOT, and RBCOT

Figure 2.2 shows the frequency response of $Z_o(s)$ with different control schemes, where the external ramp magnitude in CMCOT and RBCOT control is set to three times the falling slope of the sensed inductor current. From Figure 2.2, it can be seen that CMCOT and IQCOT are almost overlapped with each other, and RBCOT is far lower than the others. Thus, RBCOT control has by far the best load transient performance amongst them.

2.1.4 Comments on State-of-the-art Constant On-Time Control Schemes

In multi-phase operation, both CMCOT and IQCOT control are easier to design than RBCOT control. However, these conventional current-mode-based control schemes suffer from fairly slow transient response due to inductor current sensing. On the other hand, RBCOT has the best transient response capability due to ultra-low output impedance. Yet, the system design for RBCOT is a daunting task because of the ramp compensation required. Considering all the pros and cons in this section, a novel COT control is proposed to simultaneously enable inherent multi-phase operation and fast transient response.

2.2 Proposed Ultra-Fast Transient Constant On-Time Control Scheme

Figure 2.3 shows the circuit diagram of the proposed control scheme for a single-phase and multi-phase (two-phase as an example) buck converter. There are three feedback loops at work to perform modulation: 1) the first loop directly feeds the output voltage, which is also noted as output-voltage-threshold voltage, $V_{th,out}$, back to the negative terminal of the comparator; 2) the second loop senses the capacitor current, converts it to a voltage and feeds it to a subtractor; and

3) the last loop feeds the output voltage into a high-gain compensator. The reasons for each of these loop revisions will be discussed in the following paragraphs.

The detailed modulation waveforms under single-phase and two-phase interleaving conditions are illustrated in Figure 2.4. In modulation, the control signal, V_c , is generated from the error between the output voltage and the reference voltage, V_{ref} . The control signal is then subtracted by the sensed capacitor current signal, V_{ic} . Then, the difference will be converted into a ramp current, I_{ramp} , through a transconductor, which is used to charge capacitor C_T , generating a ramp voltage, V_{ramp} . This ramp voltage is fed into the positive terminal of the comparator, and thus once it reaches the output-voltage-threshold voltage, $V_{th,out}$, the phase manager is triggered, determining turn-on instance, and a local feedback loop is temporarily activated to purge the charge on C_T , resetting V_{ramp} back to zero.

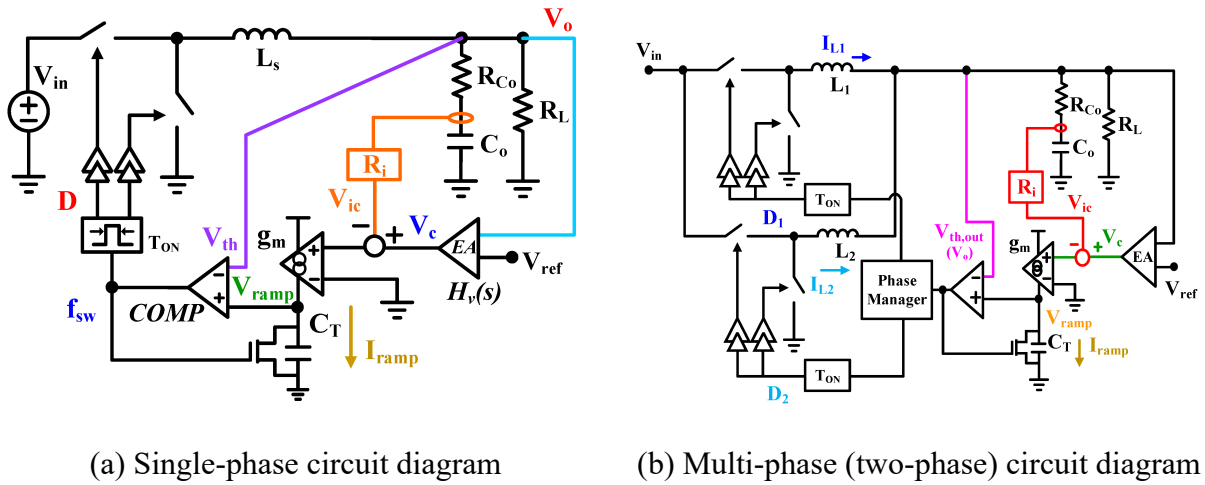


Figure 2.3 Circuit diagram of the proposed control scheme for a buck converter.

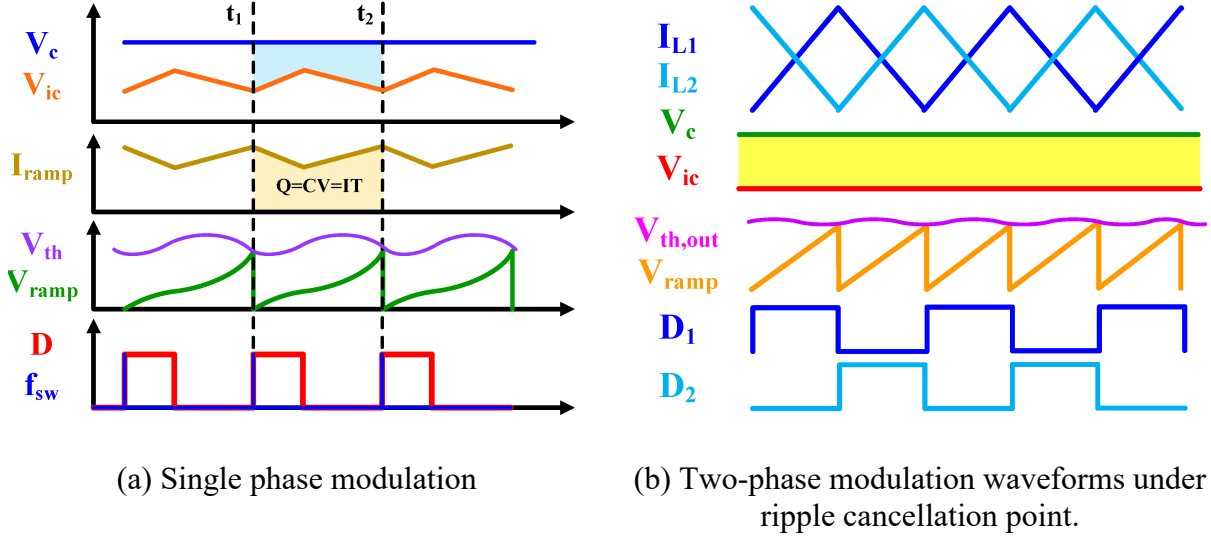


Figure 2.4 Modulation waveforms of the proposed UFTCOT control scheme.

The quintessence of the modulation is the voltage difference between the control voltage and sensed capacitor current used to charge the threshold capacitor, C_T , forming a self-generated ramp. By providing feedback in this manner, the total charge built up on C_T in each cycle will be equal to the threshold voltage multiplied by C_T . According to the above idea, the current ripple in the capacitor current becomes insignificant since the control voltage, V_c , will adjust its value automatically to ensure that the total charge is constant over each cycle. One of the benefits of this charge control is that the converter can naturally operate at the ripple cancellation point in the multi-phase application while maintaining normal operation without stability concerns or the need for an external ramp generator.

The difference between the inductor current and capacitor current feedback loop in COT-controlled Buck converters is extensively discussed in [37], [38]. The literature uses frequency-domain analyses to show that the capacitor current sensing has a lower output impedance than traditional inductor current sensing. In the time domain, the load current equals the inductor current minus the capacitor current. Therefore, when a load step-up transient occurs, the extra required load current will be provided by the capacitor since the inductor's current cannot change

instantaneously. Instead, the capacitor current is capable of reflecting load transient instantaneously, which is why it is a favorable parameter to use for the purposes of load regulation. This is illustrated in Figure 2.5, which shows the modulation waveform when a large load step-up transient occurs. Immediately after the load step-up, the sensed capacitor current, V_{ic} , drops, while the control voltage, V_c , increases simultaneously, causing the internally-generated ramp current, I_{ramp} , to correspondingly increase. Then, according to the charge equation ($Q = C \times V = I \times T$), the time to reach the threshold voltage becomes shorter due to a larger voltage difference, significantly reducing response delay compared to inductor current sensing.

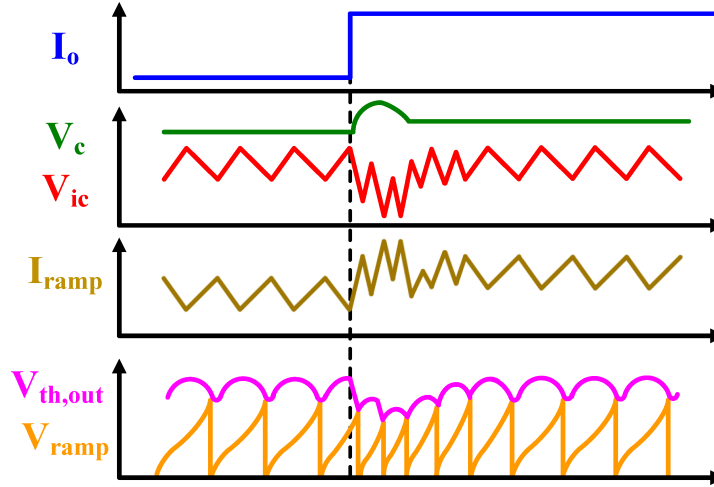


Figure 2.5 Modulation waveform during load step-up transient.

2.3 Small-Signal Model and Frequency-Domain Analysis

The small-signal model (SSM), and stability criteria for the proposed control scheme will be derived and illustrated in this section. To simplify the derivation, a single-phase condition is considered, and it can be easily extended to multi-phase through the work in [39]. A describing function (DF) method [4], [5], will be applied for accurate modeling because, during SSM

derivation, this approach considers the side-band components created by modulation. The developed SSM can be accurate all the way up to half the switching frequency.

2.3.1 Control-to-Output Transfer Function

To obtain a correct SSM, a complete current mode model can be first illustrated in Figure 2.6 according to [39], which is composed of three blocks at work: 1) factor 1 represents the transfer function from the control voltage, V_c , to the inductor current, $i_L(s)$; 2) factor 2 represents the transfer function from the inductor current, $i_L(s)$, to the output voltage, $v_o(s)$; 3) factor 3 represents the transfer function from the output voltage, $v_o(s)$, back to the inductor current, $i_L(s)$. These blocks will be derived separately in the following paragraphs, and then the final SSM of the proposed control scheme can be derived through Mason's gain formula (MGF) and Figure 2.6.

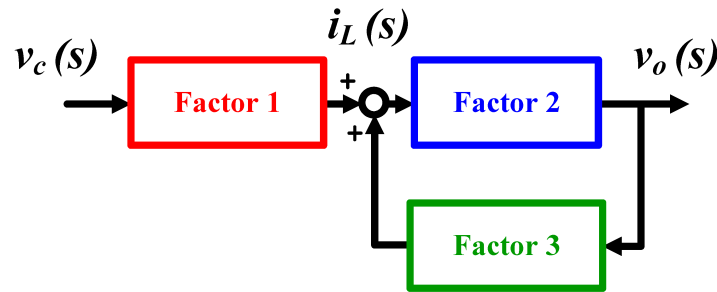


Figure 2.6 Block diagram of control-to-output transfer function in current mode control scheme.

To obtain an accurate factor 1 and reduce complexity during derivation, the DF method is applied and simplified into few steps as follow: 1) assumptions, 2) off-time calculation from modulation waveforms, 3) Fourier analysis of duty cycle and inductor current, and 4) describing function derivation.

Step 1: Assumptions

There are three basic assumptions required before performing DF as follow: i) the slope of the inductor current is constant during on-time and off-time intervals; ii) the amplitude of

perturbation is much smaller than the perturbed signal (i.e., $v_c(t)$); iii) the switching frequency, f_{sw} , and the perturbation frequency, f_m , are commensurable.

Step 2: Off-time calculation from modulation waveform

To illustrate how the perturbation affects the modulation, the modulation law of the proposed control scheme is first developed via Figure 2.7. Here, the control voltage, v_c , is perturbed by a small sinusoidal perturbation with frequency, f_m , which can be expressed as equation (2.6).

$$v_c(t) = r_o + \hat{r} \sin(2\pi f_m t), \quad \hat{r} \ll r_o \quad (2.6)$$

It can be seen that the modulation points are varied with perturbation, namely, the turn-on and turn-off instances change with the sinusoidal perturbation, where PWM is the steady-state duty ratio; PWM' is the duty ratio after being perturbed; $T_{off(i)}$ is the off-time in the i_{th} cycle and $T_{off(i)} = T_{off} + \Delta T_{off(i)}$, where T_{off} is the steady-state off-time and $\Delta T_{off(i)}$ is the off-time perturbation in the i_{th} cycle; T_i is the accumulated time from the first end of the on-time to the end of the on-time in i_{th} cycle, which can be calculated as: $T_i = (i - 1)(T_{on} + T_{off}) + \sum_{k=1}^{i-1} \Delta T_{off(k)}$.

With the modulation waveforms in place, the equation of the inverse charge modulation is shown in equation (2.7). Then, the perturbed control voltage, equation (2.6), can be substituted into equation (2.7) to derive the off-time perturbation, as shown in equation (2.8).

$$\int_{t_{i-1}+T_{off(i-1)}}^{t_i+T_{off(i)}} [v_c(t) - i_c(t)R_i] dt = \frac{C_T V_{th,out}}{g_m} \quad (2.7)$$

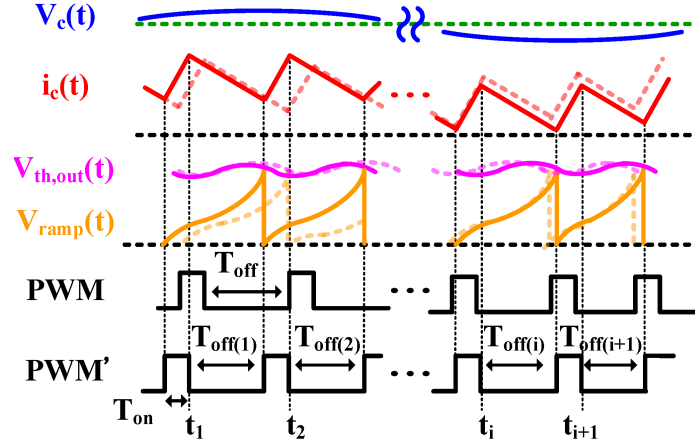


Figure 2.7 Modulation law for the proposed control scheme.

$$\begin{aligned}
 & \left(\frac{C_T V_{th,out}}{g_m T_{sw}} + \frac{1}{2} s_f T_{off} \right) \Delta t_{off(i)} + \left(T_{sw} s_f - \left(\frac{C_T V_{th,out}}{g_m T_{sw}} + \frac{1}{2} s_f T_{off} \right) \right) \Delta t_{off(i-1)} \\
 &= \frac{\hat{r}}{\pi f_m} \sin \left(\pi f_m (T_{on} + T_{off}) \right) \\
 & \times \left[\sin \left(2\pi f_m \left[(i-2)(T_{on} + T_{off}) - \frac{T_{on} - T_{off}}{2} \right] - \theta \right) \right. \\
 & \left. - \sin \left(2\pi f_m \left[(i-1)(T_{on} + T_{off}) - \frac{T_{on} - T_{off}}{2} \right] - \theta \right) \right]
 \end{aligned} \tag{2.8}$$

Step 3: Fourier analysis of duty cycle and inductor current

According to the modulation waveforms, the perturbed duty cycle and inductor current can be derived as equation (2.9) and equation (2.10), respectively. Thereafter, Fourier analysis can be performed to derive the Fourier coefficient, C_m , of the inductor current at the perturbation frequency, f_m . By substituting equation (2.9) into equation (2.10), C_m of the inductor current can be found as equation (2.11).

$$d(t)|_{0 \leq t \leq t_M + T_{off(M)} + T_{on}} = \sum_{i=1}^M [u(t - t_i - T_{off(i)}) - u(t - t_i - T_{off(i)} - T_{on})] \quad (2.9)$$

$$i_L(t)|_{0 \leq t \leq t_M + T_{off(M)} + T_{on}} = \int_0^t \left[\frac{V_{in}}{L_s} d(t) - \frac{V_o}{L_s} \right] dt + i_{L0} \quad (2.10)$$

$$c_{m(i_L)} = \frac{1}{N\pi} \frac{V_{in}}{L_s} e^{-j2\pi f_m T_{off}} (e^{-j2\pi f_m T_{on}} - 1) \left[\sum_{i=1}^M \left(e^{-j2\pi f_m (i-1) T_{sw}} \sum_{k=1}^i \Delta T_{off(k)} \right) \right] \quad (2.11)$$

Step 4: Describing function derivation

Eventually, the perturbed off-time equation (2.8) can be substituted into equation (2.11) to obtain factor 1, as shown in equation (2.12).

$$\frac{i_L(s)}{v_c(s)} = \frac{V_o}{sL_s} \frac{1}{sT_{on}} \frac{(1 - e^{-sT_{on}})(1 - e^{-sT_{sw}})}{x + (T_{sw}s_f - x)e^{-sT_{sw}}} \quad (2.12)$$

Where,

$$x = \frac{C_T V_{th,out}}{g_m T_{sw}} + \frac{1}{2} s_f T_{off}$$

The factor 2 is the output impedance looking from the inductor side, given by equation (2.13), which is just the output capacitor with ESR in parallel with the output resistor.

$$Factor2(s) = \frac{R_L(R_{Co}C_o s + 1)}{(R_L + R_{Co})C_o s + 1} \quad (2.13)$$

Factor 3, also known as k_2 , represents the effect of the output voltage on inductor current, as the slope of inductor current will vary with the value of the output voltage. Hence, it can be modeled as a feedback loop. Based on the result in [39], factor 3 can be obtained through an average derivation because factor 3 usually affects the low-frequency behavior (i.e., the low-frequency pole) only. The average derivation is described in equation (2.14).

$$\left. \frac{\partial \langle i_L \rangle}{\partial V_o} \right|_{V_{in}=constant} = -\frac{C_T}{g_m} \frac{2V_{th,out}}{V_{in}R_i T_{on}} + \frac{1}{R_L} \quad (2.14)$$

Now, by applying Mason's gain formula (MGF) and padé approximation, the control-to-output transfer function can be derived as shown in equation (2.15).

$$\frac{\hat{v}_o(s)}{\hat{v}_{c,IQ}(s)} \approx \frac{K_c}{s/\omega_a + 1} \frac{(R_{Co}C_o s + 1)}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \frac{1}{1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}} \quad (2.15)$$

Where,

$$K_c = \frac{R_L}{R_i(1 - R_L \times k_2)}, \omega_a = \frac{1 - R_L \times k_2}{(R_L + R_{Co})C_o - R_L R_{Co} C_o \times k_2}, k_2 = -\frac{C_T}{g_m} \frac{V_{th,out}}{V_{in}R_i T_{on}} + \frac{1}{R_L}$$

$$\omega_1 = \pi/T_{on}, \quad \omega_2 = \pi/T_{sw}, \quad Q_1 = 2/\pi$$

$$Q_2 = \frac{2s_f T_{on}}{\pi D \left(\frac{2C_T V_{th,out} D}{g_m T_{on}} - s_f T_{on} \right)}, \quad s_f = R_i \frac{V_o}{L_s}$$

Here, s_f represents the sensed falling slope of the inductor current; R_i is the sensing gain; R_L is the load resistance; C_o and R_{Co} are the output capacitance and ESR respectively; C_T is the threshold capacitor for the inverse charge process; g_m is the transconductance, converting voltage difference into ramp current, I_{ramp} ; and D denotes the duty cycle.

The control-to-output transfer function, as shown in equation (2.15), shows a low-frequency pole, two pairs of conjugate poles, an ESR-based zero, and a dc gain of K_c . It should be noted that the poles located at the half-switching frequency may move to the right-half plane (RHP) if Q_2 becomes negative. Thus, the stability criteria can be expressed as equation (2.16).

$$\frac{C_T L_s}{R_i g_m T_{sw}} > \frac{T_{on}}{2} \quad (2.16)$$

Figure 2.8 shows the calculation, and the simulation results of $G_{vc}(s)$ with duty cycles of 0.1, 0.5, and 0.9. The simulation results are obtained from SIMPLIS. As can be seen, the

calculation results are well-matched with the simulation results, indicating the validity of the mathematical model represented by equation (2.15). In Figure 2.8, the Q -value at the half-switching frequency increases with the increase of the duty cycle, which verifies that the Q -value varies as the duty ratio varies. Note that Figure 2.8 is calculated at a given condition that C_T is 700pF, R_i is 0.05V/V, G_m is 1.5mA/V, L_s is 250nH, and f_{sw} is 500kHz.

2.3.2 Output Impedance Transfer Function

To simplify the output impedance derivation[40], the capacitor current loop can be decomposed into a inductor current loop and a load current loop based on equation (2.17), and then the equivalent circuit can be redrawn as shown in Figure 2.9. It can be noted that the circuit is analogous to the IQCOT control scheme if the load current loop is excluded. Thus, the output impedance of proposed control technique can be derived based on IQCOT control with the load current loop closed.

$$I_c = I_L - I_{load} \quad (2.17)$$

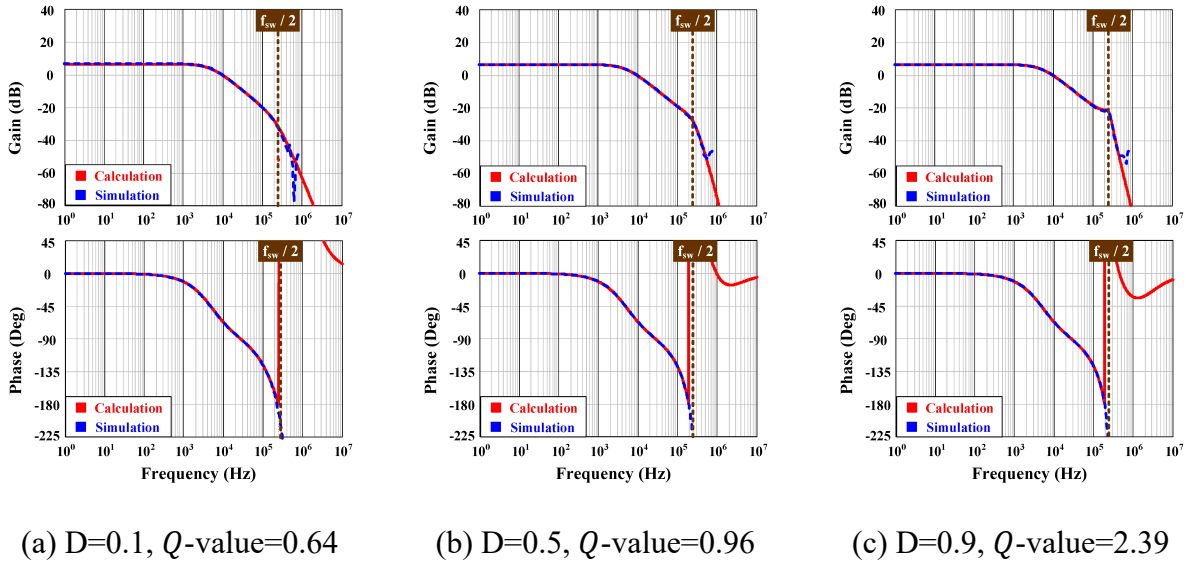


Figure 2.8 Control-to-output transfer function validation.

To include effects caused by the load current loop, a small-signal current perturbation can be injected into the output terminal of the Buck converter, and the equivalent block diagram is found as Figure 2.10. In the figure, the red lines are the effects of the inductor current loop, and the blue lines are the effects of the load current loop. If the load current loop is omitted (i.e., considering the red lines only), the output impedance is $Z_{o(iL)}(s)$ since v_c is a constant value, which is zero in the small-signal analysis. Then, the load current loop can be taken into consideration, creating two additional paths, a forward path and a feedback path, to the block diagram. The forward path is from the sensing network, which directly feeds sensed load current to the modulator, while the feedback path is from the local feedback caused by the load resistance, which is also sensed by sensing gain, R_i and fed back to the modulator.

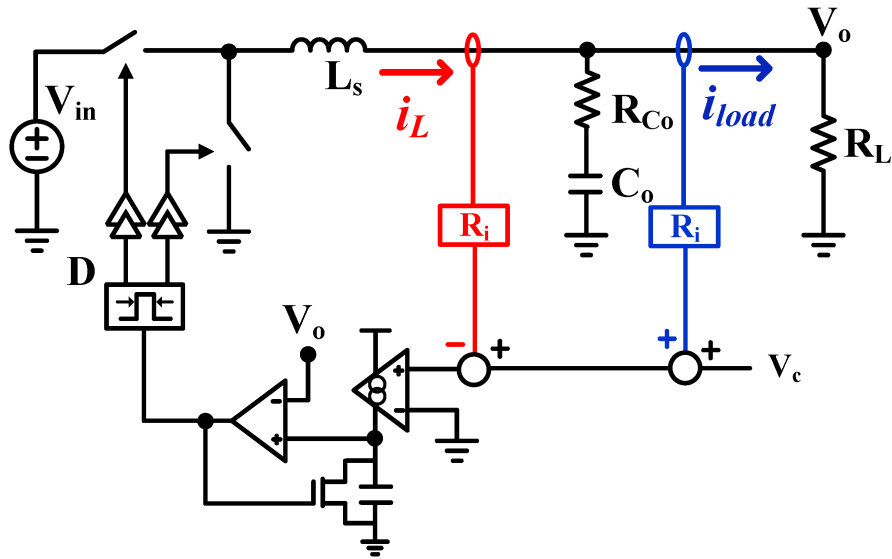


Figure 2.9 Capacitor current loop decomposition.

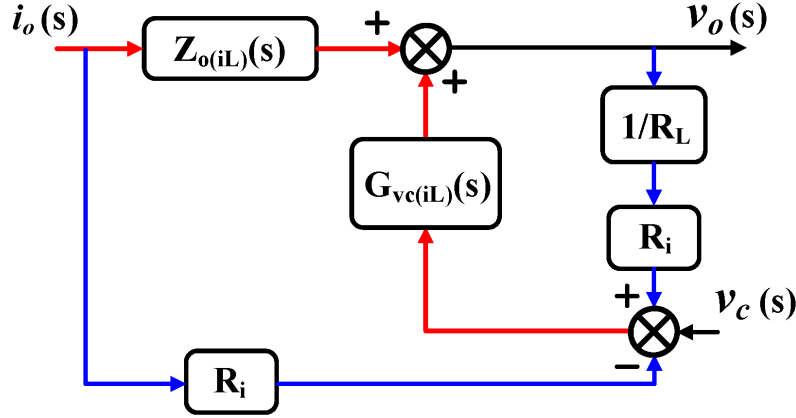


Figure 2.10 Output impedance block diagram for the proposed control scheme.

With the block diagram in place, the output impedance of the proposed control technique can be derived in equation (2.18) via Figure 2.10 and MGF where $G_{vc(iL)}(s)$, and $Z_{o(iL)}$ are small-signal models only considering the inductor current loop. The expressions for $G_{vc(iL)}(s)$ and the $Z_{o(iL)}$ are shown in equation (2.2) and (2.4), while k_2 is shown in equation (2.19).

$$Z_o(s) \equiv \frac{v_{out}(s)}{i_o(s)} \approx \frac{R_i \cdot G_{vc(iL)}(s) - Z_{o(iL)}(s)}{\frac{R_i}{R_L} \cdot G_{vc(iL)}(s) - 1} \quad (2.18)$$

$$k_2 = -\frac{C_T}{g_m} \frac{2V_{th,out}}{V_{in}R_iT_{on}} \quad (2.19)$$

According to equation (2.18), the output impedance transfer function can be further simplified as equation (2.20)

$$Z_o(s) \approx K_z \frac{1}{s/\omega_a + 1} \frac{1}{1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}} \frac{1}{1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}} \quad (2.20)$$

Where,

$$K_z = \frac{L_s C_T R_L}{g_m T_{sw} R_i (1 - R_L k_2)}$$

Figure 2.11 shows the calculation, and the simulation results of $Z_o(s)$ with duty cycles of 0.1, 0.5, and 0.9. As can be seen, the calculation results are again well-matched with simulation results, and Q -value clearly changes with the duty cycle. Note that Figure 2.11 is calculated at a given condition that C_T is 700pF, R_i is 0.05V/V, G_m is 1.5mA/V, L_s is 250nH, and f_{sw} is 500kHz.

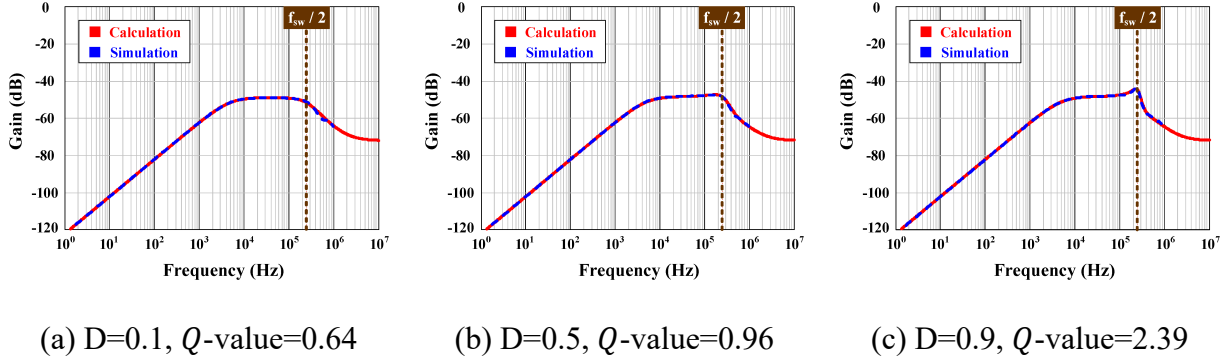


Figure 2.11 Output impedance transfer function validation.

2.3.3 Transfer Function Comparison

In this subsection, both the control-to-output transfer function and output impedance of IQCOT and the proposed control scheme will be discussed to verify the stability and load transient response performance. Since CMCOT and IQCOT control schemes are extensively discussed in Section II, which share similar forms in transfer function, CMCOT can be easily extended, and therefore, CMCOT is omitted in this subsection.

2.3.3.1 Control-to-Output Transfer Function

The main differences between IQCOT and the proposed control are the threshold voltage and current sensing, where the former adopts a constant threshold voltage and inductor current sensing method, while the latter control scheme employs an output-voltage-threshold voltage and capacitor current sensing approach. To investigate the effects of the feedback loop on the overall

control of the circuit, the control-to-output transfer function, $G_{vc}(s)$, should be discussed, which is a metric for designers to evaluate stability and design compensation circuits.

$G_{vc}(s)$ of IQCOT and proposed control technique is shown in equation (2.2) and (2.15) separately. The two expressions are very similar to each other, with the main differences being the value of k_2 and the quality factor at frequency ω_2 . According to the SSM derivation of $G_{vc}(s)$ and k_2 , it can be concluded that the quality factor difference mainly comes from the difference of threshold voltages, while the k_2 difference results from both current sensing and threshold voltage differences. Also, the difference in k_2 leads to different DC gain, k_c , and the low-frequency pole, ω_a . In contrast, the difference in the quality factor results in stability concerns. That is, when the quality factor becomes negative, the system becomes unstable. In summary, the capacitor current sensing feedback affects the DC gain and the low-frequency pole; on the other hand, the output-voltage-threshold voltage affects the DC gain, the low-frequency pole, and stability.

The bode plot of the control-to-output transfer function is shown in Figure 2.12. As shown, the DC gain and the low-frequency pole are different in both control schemes. As for the quality factor at ω_2 , if the DC value of the constant threshold voltage, which is IQCOT's threshold, and the output-voltage-threshold voltage, which is UFTCOT's threshold, are the same, the quality factor will be the same since the only difference in the quality factor expression is the threshold voltage. Therefore, the peaking at $f_{sw}/2$ is the same in Figure 2.12.

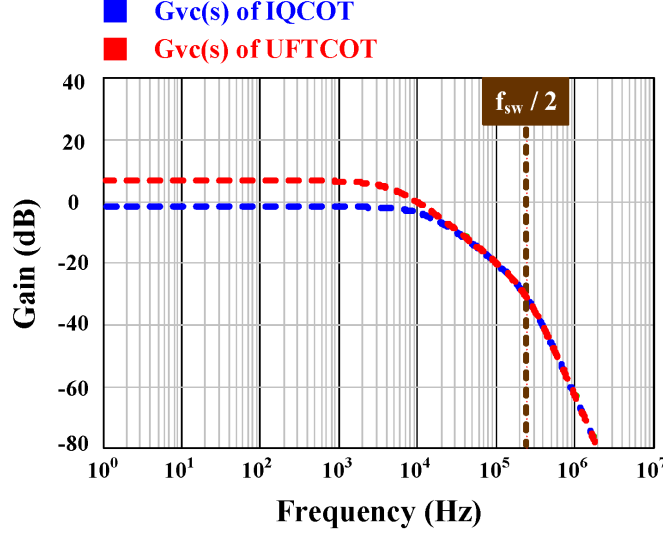


Figure 2.12 Control-to-output transfer function comparison.

2.3.3.2 Output Impedance

Apart from the loop effect on controls, the output impedance, $Z_o(s)$, is also of interest for evaluating the load transient performance in the frequency-domain. Figure 2.13 shows the impacts caused by the different feedback loops. As illustrated in Chapter 2.3.2, capacitor current sensing can be decomposed into inductor current feedback and load current feedback. Figure 2.13 firstly shows $Z_o(s)$ with only the voltage regulation loop closed in the red solid line. Then, $Z_o(s)$ with the inductor current loop closed in the blue dashed line, which is the same as IQCOT control. When both the inductor current and load current loops are closed, as shown in the green dashed line, $Z_o(s)$ at low frequencies shows an ultra-low impedance. This is a result from the capacitor current sensing, which behaves as a differentiator, reducing low-frequency impedance significantly. Finally, the orange dashed line shows $Z_o(s)$ with all loops closed, which is the $Z_o(s)$ of proposed control technique. With the additional output-voltage threshold loop, the impedance is further reduced. Hence, the proposed control can achieve an ultra-fast load transient response.

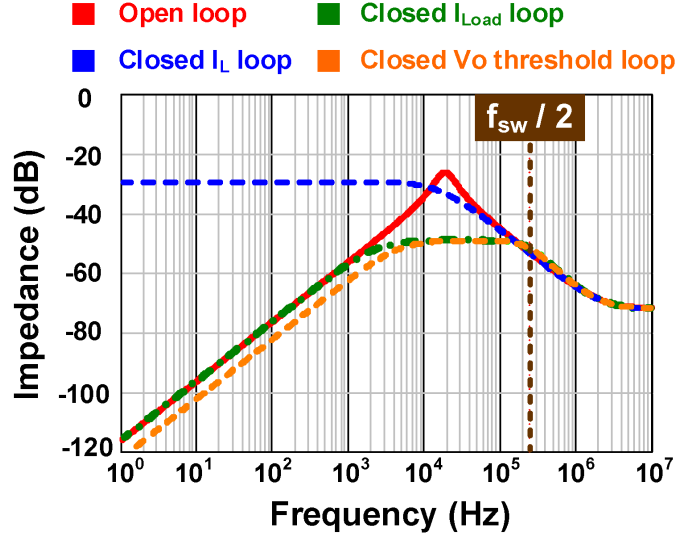


Figure 2.13 Output impedance comparison.

2.4 Proposed Duty-Cycle-Independent Quality Factors Design

From the analysis conducted in Chapter 2.3, it is clear that Q_2 varies with the employed duty cycle, which can lead to stability issues in wide input-to-output voltage range applications. In this section, a generalized approach is presented, enabling a duty-cycle-independent Q -value (constant Q -value) design. Then, a constant Q -value circuit is proposed based on the UFTCOT control scheme.

2.4.1 Constant Q -Value Analysis

The stability criteria in equation (2.16) can be rearranged as follows, equation (2.21), to investigate the effect of duty cycle on Q -value:

$$\frac{C_T L_S}{R_i g_m T_{sw}} > \frac{DT_{sw}}{2}. \quad (2.21)$$

Here, the key variables at play are duty cycle and switching frequency since the other variables can be viewed as constants once the controller is designed. To reduce frequency variation caused by wide input/output voltage range in commercial products, an adaptive on-time (AOT) technique, which automatically adjusts the on-time according to input/output voltage, can be employed [41]. In this case, a fixed frequency can be presumed during steady-state operation. Consequently, the Q -value only varies with duty cycle. Figure 2.14 shows this Q -variation versus duty cycle under baseline UFTCOT control scheme with AOT. Once the Q -value becomes negative, the system becomes unstable, as highlighted in the cyan-colored region. Note that Figure 2.14 is calculated at a given condition that C_T is 700pF, R_i is 0.05V/V, G_m is 1.5mA/V, L_s is 250nH, and f_{sw} is 500kHz.

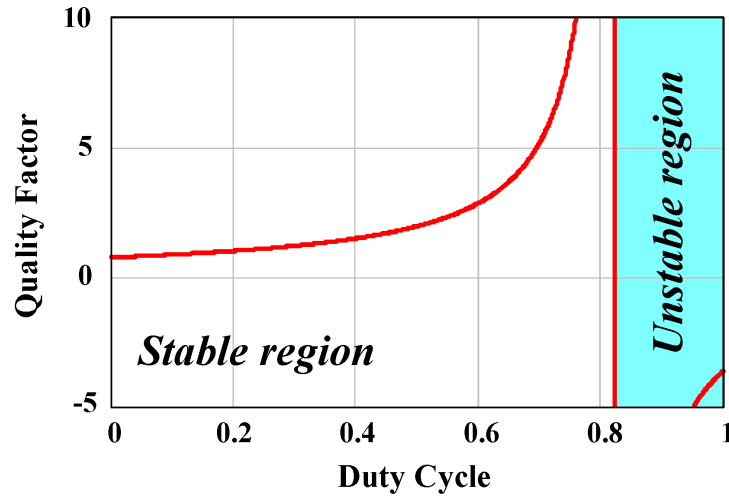


Figure 2.14 Q -value variation without constant Q -value control.

As aforementioned, the key parameter at play in setting the Q -Value is the duty cycle, which varies in wide input-to-output voltage applications. Hence, to achieve a constant Q -value, there should be another variable, that is capable of eliminating the effect caused by a wide input-to-output voltage range. To make the forthcoming discussion more clear, the variables that vary as

the operation condition changes are defined as control inputs (i.e., duty cycle, D , output voltage, V_o , and input voltage, V_{in}). Finally, a generalized analysis is developed, involving the following three steps:

- 1) Simplify the Q -value expression and identify which variable(s) can be deliberately designed to vary as control inputs changes.
- 2) Evaluate the relationship between the targeted variable(s) and the control inputs.
- 3) Design the targeted variable(s) to compensate for the effect caused by the control inputs.

Based on this, the following steps are performed to design a constant Q -value circuit for UFTCOT control. First, the expression for Q -value can be simplified to equation (2.22). Here, the variable that can be manipulated is the threshold voltage, V_{th} , since the other variables, including C_T , g_m , L_S , and R_i , are typically determined once the system is designed and they cannot be easily designed to vary as the operation point varies. Second, with V_{th} identified as a target variable, its relationship with the control inputs, namely duty cycle and V_o in this case, can be examined. The denominator of equation (2.22) is a function of V_o multiplied by the threshold voltage, which is then subtracted by a constant multiplied by the duty cycle. Therefore, V_{th} should also vary at the same rate as the duty cycle and V_o vary. Third, by observation, V_{th} should be a function of V_o to compensate for the Q -variation affected by V_o . However, if V_{th} is merely a function of V_o , the Q -value still varies with duty ratio. Hence, V_{th} should also be a function of duty cycle. Thus, V_{th} can be designed as $(\alpha + \beta D) \times V_o$. This gives a new Q -value, Q_2'' , which can be expressed as equation (2.23), where α decides the exact Q -value, and β helps achieves a duty-independent Q -value.

$$Q_2 = \frac{T_{sw}}{\pi} \frac{1}{\left(\frac{C_T L_S}{g_m R_i T_{sw}} \frac{V_{th}}{V_o} - \frac{T_{sw}}{2} D \right)} \quad (2.22)$$

$$Q_2'' = \frac{T_{sw}}{\pi} \frac{1}{(Q_{init} + a_1 D - a_2 D)} \quad (2.23)$$

Where,

$$Q_{init} = \frac{C_T}{g_m} \frac{L_s}{R_i} \frac{\alpha}{T_{sw}}, \quad a_1 = \frac{C_T}{g_m} \frac{L_s}{R_i} \frac{\beta}{T_{sw}}, \quad a_2 = \frac{T_{sw}}{2}$$

There are several advantages to designing V_{th} as $(\alpha + \beta D) \times V_o$:

- 1) The output voltage is eliminated in equation (2.23), since the output voltage in V_{th} reduces the fraction in equation (2.22).
- 2) It is easy to achieve a constant Q -value. Once a_1 equals a_2 , the effect of duty cycle is canceled out; namely, once equation (2.24) holds, the constant Q -value condition holds.
- 3) The Q -value can be simplified as equation (2.25) when equation (2.24) holds. That is, the exact value of the quality factor can be designed by the gain α when other parameters are determined. The lower the gain α is, the higher the Q -value will be.

In this way, the constant Q -value over the whole duty-cycle range can be achieved, and the exact value of Q is well-controlled.

$$\alpha = Constant, \quad \beta = \frac{g_m R_i T_{sw}^2}{2 C_T L_s} \quad (2.24)$$

$$Q_2'' = \frac{T_{sw}^2 R_i g_m}{\pi C_T L_s} \frac{1}{\alpha} \quad (2.25)$$

Figure 2.15 shows a plot of Q -value versus duty cycle of the UFTCOT control with constant Q -value activated where the Q -value is designed to be 0.774 with $\alpha=1$, and $\beta=1.216$. It can be seen that with proper α and β design, a constant Q -value can be achieved.

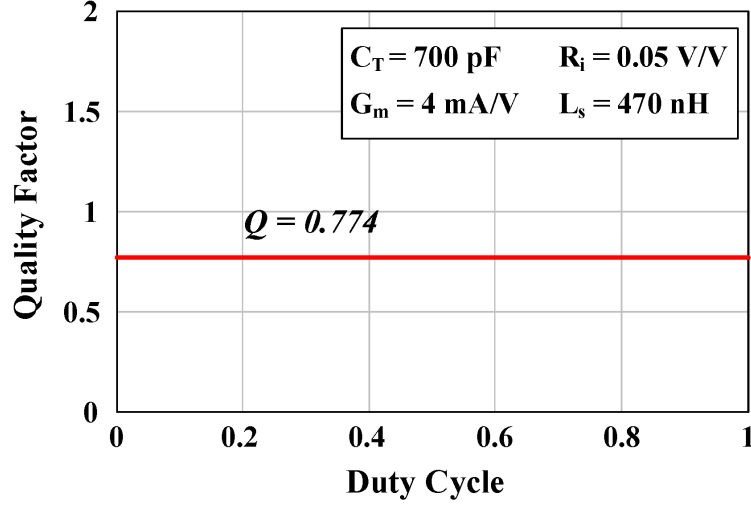


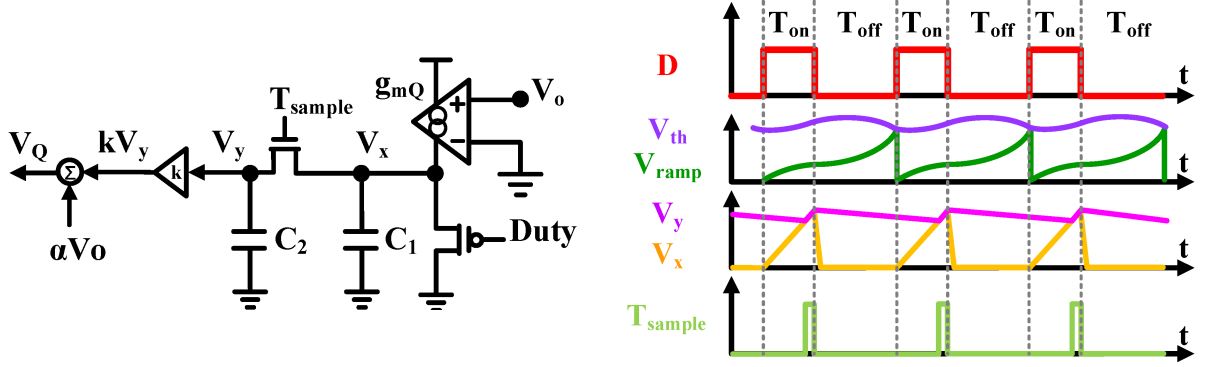
Figure 2.15 Q -value variation with constant Q -value control.

2.4.2 Constant Q -Value Circuit Design

One potential circuit to generate $(\alpha + \beta D) \times V_o$ and achieve the constant Q -value is shown in Figure 2.16(a), with key waveforms shown in Figure 2.16(a). When the duty signal is high, the capacitor, C_1 , is charged by a current generated from the output-voltage-controlled transconductor, generating voltage, V_x , which is then sampled by the sampling signal, T_{sample} , and stores the value to the capacitor, C_2 . The sampled voltage, V_y , is connected to a gain stage with a gain of k , and then adds to αV_o to create a constant Q -value control voltage V_Q . When the duty signal is low, the switch in parallel with C_1 is activated and purges the charge stored in C_1 , resetting and clamping V_x to zero. At the same time, C_2 holds the sampled voltage, V_y .

Eventually, the final output, V_Q , of the proposed circuit is found as $(\alpha V_o + kV_y)$. To ensure $V_{th} = (\alpha + \beta D) \times V_o$, kV_y should be equal to $\beta D V_o$, where kV_y can be found as equation (2.26) by the charging equation ($Q = C \times V = I \times T$), and $\beta D V_o$ can be written as equation (2.27). Then,

$(k \times g_{mQ})/C_1$ can be designed to be equal to $\beta \times f_{sw}$ to make V_Q equal $(\alpha + \beta D) \times V_o$, achieving a constant Q -value. Note that β is shown in equation (2.24).



(a) Circuit for $(\alpha + \beta D) \times V_o$ generation (b) Waveforms for $(\alpha + \beta D) \times V_o$ generation

Figure 2.16 $(\alpha + \beta D) \times V_o$ circuit and waveforms.

$$kV_y \approx k \frac{g_{mQ}}{C_1} T_{on} V_o \quad (2.26)$$

$$\beta D V_o = \beta f_{sw} T_{on} V_o \quad (2.27)$$

Figure 2.17 shows the Q -value variations with different threshold voltages along with the Q -value with constant Q -value circuit enabled. Figure 2.18 shows $G_{vc}(s)$ of UFTCOT with the constant Q -value circuit enabled under different duty-cycle conditions in both calculation and simulation where Q -value is designed to be approximately 0.77, where the parameters used are the same as in Figure 2.15. It can be seen that the Q -value at the half-switching frequency is well-controlled and duty-cycle-independent under different duty-ratio conditions. It should be noted that the phase difference at high frequencies (i.e., around the half-switching frequency) is caused by the high-frequency complex poles at ω_1 , as shown in equation (2.15).

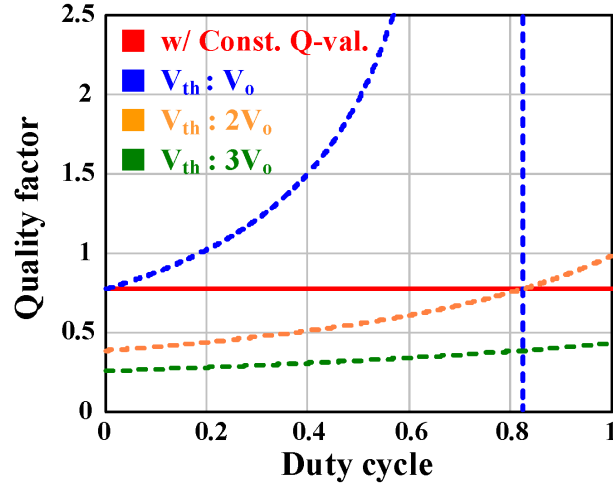


Figure 2.17 Q -value variation of UFTCOT control scheme.

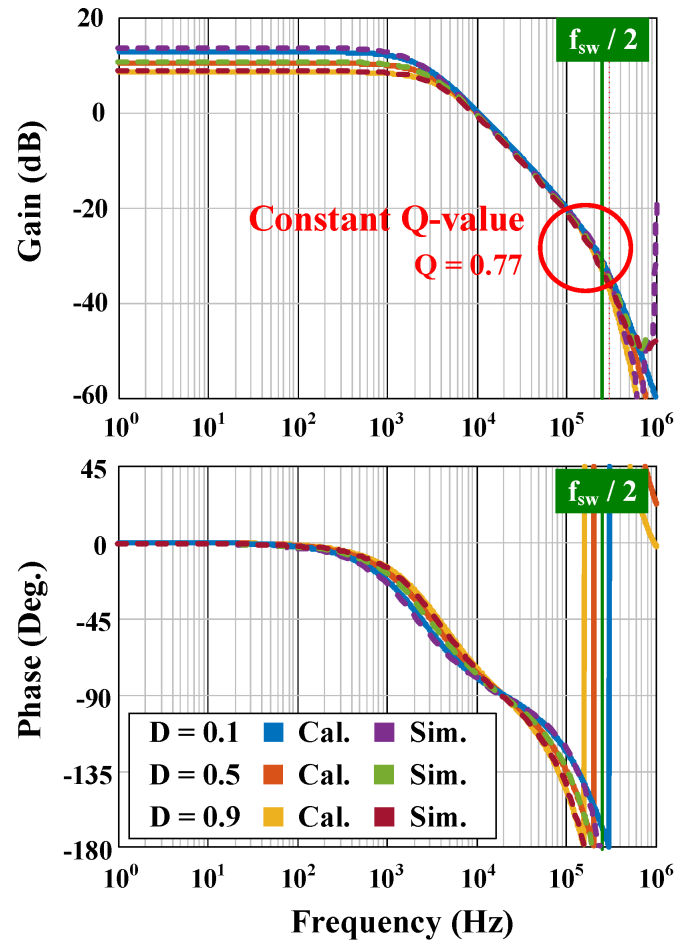


Figure 2.18 Control-to-output transfer function of UFTCOT control scheme.

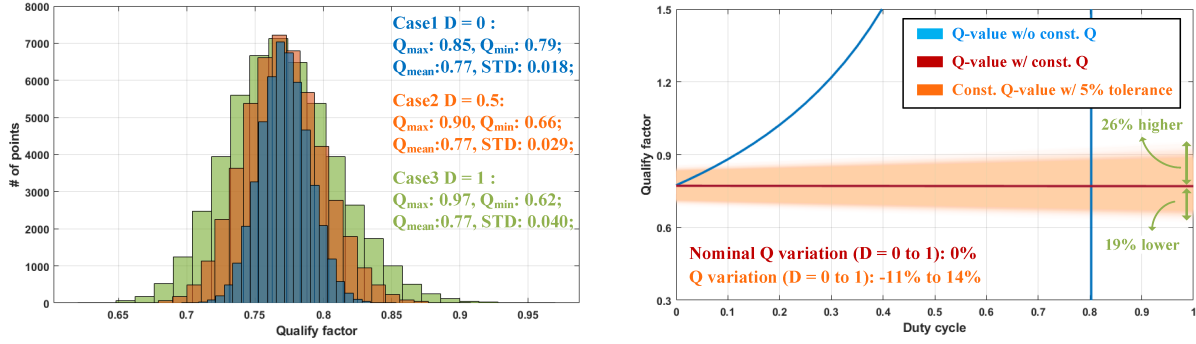
2.4.3 Effects of System Component and Constant Q -Value Voltage Tolerance on Constant Q -Value Accuracy

In the actual circuit implementation, the component tolerance and accuracy of the constant Q -value circuit often come into play and degrade the effectiveness of the constant Q -value control, even when the constant Q -value is carefully designed. In this subsection, the effect of the component and constant Q -value control voltage, V_Q , tolerance is illustrated and summarized.

2.4.3.1 Effect of Component Tolerance on Q -Variation

Here, two assumptions have been made for this analysis: (1) a perfect Q -value circuit is assumed, and the component tolerance occurs only on the power stage and modulator components, e.g., R_i , L_s , G_m , etc. (2) 5% variance in a Gaussian distribution is assumed for each component. With these two assumptions, a 50,000-point Monte Carlo simulation is performed. Note that the parameters for the calculation are the same as used in Figure 2.15. The resulting Q -value variation distribution is shown in Figure 2.19(a). Here, Q -value variations at $D=0$, 0.5, and 1 cases are plotted. It can be observed that with a larger duty cycle, a higher Q -variation is shown where the standard deviation increases from 0.018 to 0.04 as the duty cycle moves from 0 to 1. This also implies that Q -value varies to a higher/lower value at a larger duty cycle that Q_{max} moves from 0.85 to 0.97, and Q_{min} moves from 0.79 to 0.62 as D moves toward 1 from 0. The Q -value variation with duty cycle is shown in Figure 2.19(b). Here, the orange shaded area shows the potential Q -value curves where the area with a higher intensity implies a higher possibility of Q -value curve to be. It can be found that the Q -value shows a maximum and minimum of 26% and -19% deviation, respectively, toward the targeted constant Q -value when component tolerance is in play. In addition, the Q -value variation with the duty cycle is no longer constant but a value

between -11% to 14% variation due to the component tolerance. Nevertheless, compared to the original Q -variation curve without constant Q -value control, the Q -value control strategy significantly improves the system stability no matter whether there is component tolerance or not.



(a) Q -value Monte Carlo simulation with 5% component tolerance

(b) Q -value variation versus duty cycle

Figure 2.19 Component tolerance effect on Q -value variation.

2.4.3.2 Effect of V_Q Tolerance on Q -variation

Aside from the component tolerance, the constant Q -value control voltage, V_Q , generated from the constant Q -value circuit can sometimes deviate from the design value. Here, 10% V_Q tolerance and tolerance-free components are assumed. The Q -value variation with duty is shown in Figure 2.20. The V_Q tolerance shows similar trends with component tolerance, where the maximum and minimum Q -value variations are -18% and +28% compared to the design value at +10% and -10% V_Q tolerance cases, respectively, and the percentages of variations due to the duty cycle are from -9% to +16% under 10% V_Q cases. Again, even with V_Q tolerance, the constant Q -value control can stabilize the system and enable the system to be operated at a higher duty cycle range.

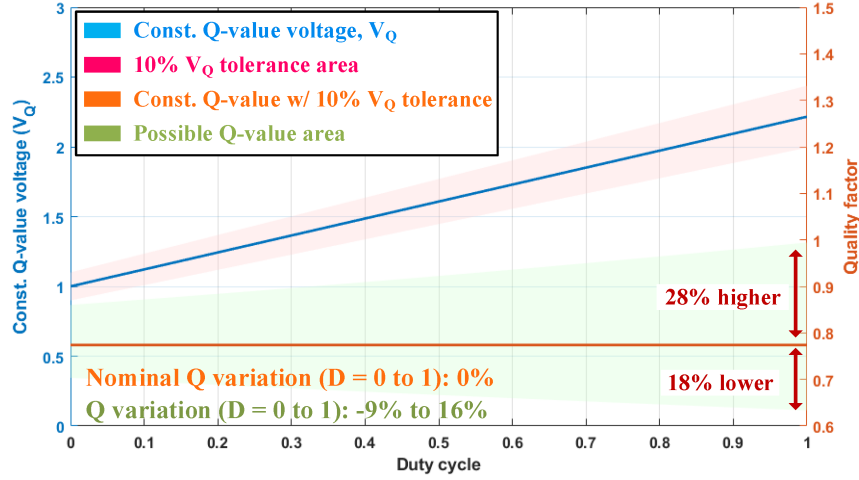


Figure 2.20 Q -value variation with 10% V_Q tolerance.

2.4.4 Extending to Other Existing Control Schemes

The constant Q -value analysis can be easily extended to a variety of COT controllers since the proposed constant Q -value method does not alter the original modulation law of a COT control scheme and, therefore, the COT models reported can be directly reused and analyzed. Three state-of-the-art COT control schemes and a general form of a ripple-based COT with continuous ramp compensation are presented and analyzed to achieve constant Q -value in this section: 1) inverse charge COT (IQCOT) control [10], 2) accurate adaptive COT (A^2 COT) control [12], 3) ripple-based COT with Virtual inductor current (RBCOT with VIC) control [11], and 4) ripple-based constant on-time control with continuous ramp compensation.

2.4.4.1 Inverse Charge Constant On-Time Control Scheme

The circuit diagram of IQCOT control scheme [10] is shown in Figure 2.21, which is very similar to UFTCOT control, but instead with inductor current sensing and a constant threshold

voltage. Therefore, the small-signal models of IQCOT control, shown in [10], is similar to UFTCOT control.

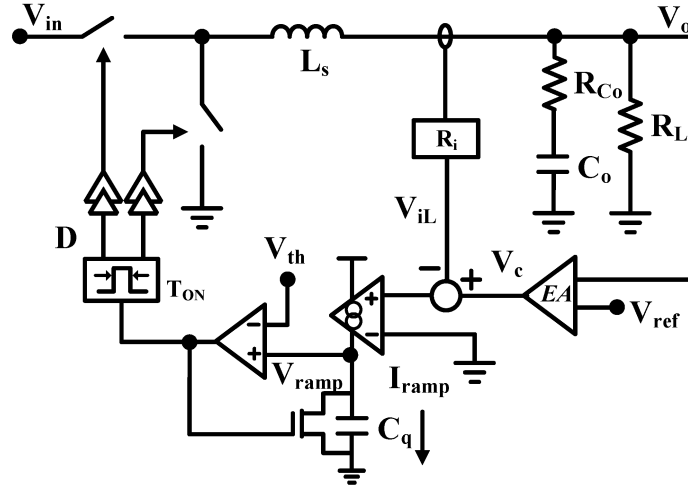


Figure 2.21 IQCOT control circuit diagram.

The Q -value expression at $f_{sw}/2$ is described as equation (2.22), which is the same as UFTCOT, shown in equation (2.15). Therefore, the same method can be applied to the IQCOT control, which designates the threshold voltage to be $(\alpha + \beta D) \times V_o$. Moreover, the constant Q -value circuit proposed in Chapter 2.4.2 can be applied as well. As a result, a constant Q -value can be realized, and the new Q -value expression is shown in equation (2.23), which is the same as UFTCOT control. The constant Q -value validation can refer to Figure 2.18 since its $G_{vc}(s)$ is similar to UFTCOT control [10] [42].

2.4.4.2 Accurate Adaptive Constant On-Time Control Scheme

For the A²COT control scheme[12], the Q -value expression at $f_{sw}/2$ is described by equation (2.28). Given this expression, the constant Q -value concept can be applied as follows: 1) The variable that can be adjusted is the ramp-slope-control voltage, V_{rsc} in the Q -value expression, since other variables are usually determined once system is designed. 2) The relationship between

V_{rsc} and the control inputs, duty ratio, and input voltage in this case, can be identified. 3) By observation, V_{rsc} should eliminate the Q -value variation caused by the input voltage and the duty cycle at the same time. Interestingly, if V_{rsc} is a function of the input voltage and output voltage such as $(\alpha V_{in} + \beta V_o)$, then the αV_{in} term can be used to eliminate V_{in} variation in equation (2.28), while the βV_o term forms a duty cycle term because of $(D = V_o/V_{in})$ and can be used to cancel out the $T_{sw}/2 \times D$ term in equation (2.28).

$$Q_2 = \frac{T_{sw}}{\pi \left[\left(R_{C_o} C_o + \frac{L_s G_{mRP} R_{C_o} C_o}{C_{RP} R_i} \frac{V_{rsc}}{V_{in}} \right) - \frac{T_{sw}}{2} D \right]} \quad (2.28)$$

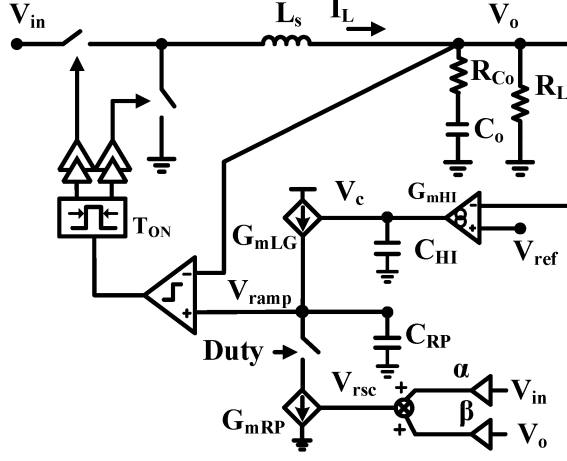
Combining the observations above, V_{rsc} can be designated to be $(\alpha V_{in} + \beta V_o)$ and the constant Q -value expression can be derived as equation (2.29), where α decides the exact Q -value, and β achieves constant Q -value. Again, the input voltage is eliminated in the new expression. Also, if a_1 is equal to a_2 , the effect of duty-cycle variation can be eliminated. Subsequently, the exact value of the quality factor can be designed via α in Q_{init} .

$$Q_2'' = \frac{T_{sw}}{\pi} \frac{1}{(Q_{init} + a_1 D - a_2 D)} \quad (2.29)$$

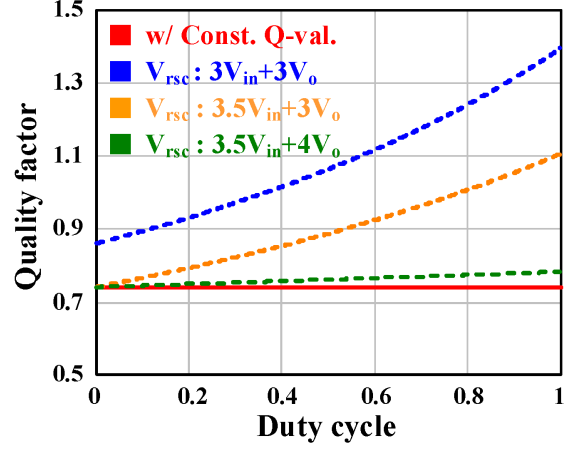
Where,

$$Q_{init} = R_{C_o} C_o + \frac{L_s G_{mRP} C_o}{C_{RP}} \alpha, \quad a_1 = \frac{L_s G_{mRP} C_o}{C_{RP}} \beta, \quad a_2 = \frac{T_{sw}}{2}$$

Importantly, the input/output controlled V_{rsc} is naturally built-in; namely, there is no additional circuit required in A²COT to achieve a constant Q -value, as shown in Figure 2.22(a).



(a) A2COT control circuit diagram with constant Q -value circuit



(b) Q -value variation of A²COT control scheme

Figure 2.22 A²COT control circuit diagram and constant Q -value variation.

Figure 2.22(b) shows the Q -value variations with different ramp-slope-control voltages, V_{rsc} , along with the Q -value with constant Q -value circuit enabled. In [12], a nearly constant Q -value is claimed, as shown in Figure 2.22(b), when V_{rsc} is $3.5V_{in} + 4V_o$; however, the constant Q -value could, in fact, be achieved by the systematic analysis proposed in equation (2.29). Figure 2.23 shows $G_{vc}(s)$ of A²COT with the constant Q -value circuit enabled under duty cycles of 0.1, 0.5, and 0.9, where the validity of $G_{vc}(s)$ is proven in [12]. It can be seen that the Q -value at the half-switching frequency is well-controlled and duty-cycle-independent, where no peaking is shown in the magnitude plot at the half-switching frequency as the duty cycle increases.

$$Q_2 = \frac{T_{sw}}{\pi \left[\left(1 + \frac{L_s M_f}{R_i V_o} \right) R_{C_o} C_o - \frac{T_{sw}}{2} D \right]} \quad (2.30)$$

Where,

$$M_f = \frac{\alpha V_o}{R_{VIC} C_{VIC}}$$

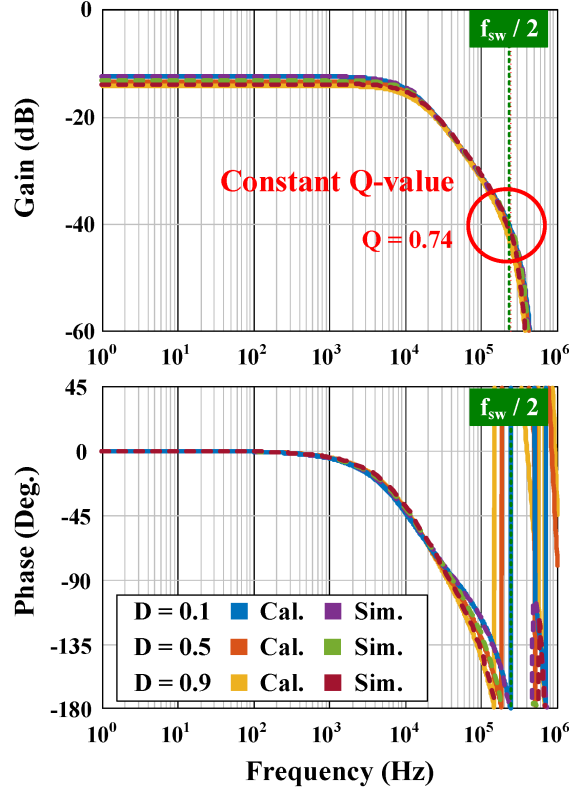


Figure 2.23 Control-to-output transfer function of A²COT control scheme with constant Q -value control.

2.4.4.3 Ripple-Based Constant On-Time with Virtual Inductor Current (VIC) Control Scheme

The Q -value of the RBCOT with VIC control scheme [7] is shown in equation (2.30). As in the previous subsections, the constant Q -value concept can be employed as follows: 1) the ramp slope, M_f , is substituted into equation (2.30), but, after simplification, there is no variable that can be controlled. Hence, going back to the original expression (2.30), it can be seen that the ramp slope, M_f , is the variable that can be modulated. 2) The relationship between M_f and the control inputs, which are duty cycle and V_o in this case, can be identified. M_f should be capable of eliminating the Q -value variations caused by duty cycle and V_o variation. 3) Then, M_f needs to be redesigned, and according to step 1, the original M_f is capable of eliminating V_o variation but

unable to compensate the duty-cycle variation. As a result, a duty-cycle compensation term should be added in to the original M_f . Finally, the new M_f can be designated as equation (2.31).

$$M_f'' = \frac{\alpha V_o}{R_{VIC} C_{VIC}} + \frac{\beta D V_o}{R_{VIC} C_{VIC}} \quad (2.31)$$

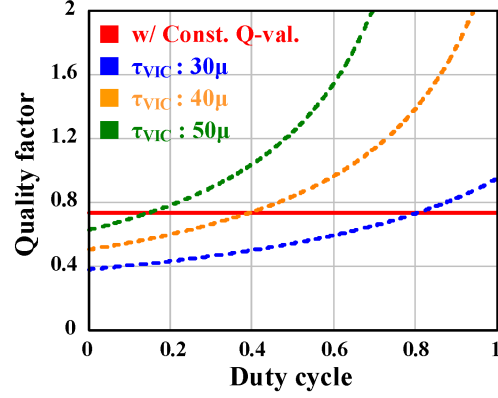
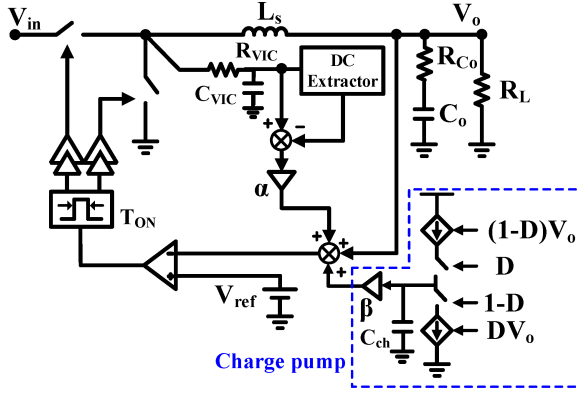
After designating M_f'' , the Q -value can be rearranged as equation (2.32), where, again, α decides the exact Q -value, and β achieves constant Q -value. Similar to other constant Q -value expressions, when a_1 is equal to a_2 , the effect of duty-cycle variation can be eliminated. Thereafter, the exact value of the quality factor can be designed via α in Q_{init} . In this way, the instability issue can be effectively addressed.

$$Q_2'' = \frac{T_{sw}}{\pi} \frac{1}{(Q_{init} + a_1 D - a_2 D)} \quad (2.32)$$

Where,

$$Q_{init} = R_{C_o} C_o + \frac{L_s C_o}{R_{VIC} C_{VIC}} \alpha, \quad a_1 = \frac{L_s C_o}{R_{VIC} C_{VIC}} \beta, \quad a_2 = \frac{T_{sw}}{2}$$

To achieve a constant Q -value in RBCOT with VIC control, an additional ramp generation is required to generate the second term in equation (2.31). A simple charge pump circuit can be applied to generate the ramp compensation, as shown in Figure 2.24(a). The charge pump circuit consists of two output-voltage-controlled current sources, which are controlled by switches that are controlled by the input duty signal and its complement, to charge and discharge a capacitor generating the ramp and then, connect to a gain stage with a gain of β . The charge and discharge time is determined by D and $1 - D$. Note that the charge pump circuit is a simplified version for functional illustration purposes only.



(a) RBCOT w/ VIC control circuit diagram with constant Q -value circuit

(b) Q -value variation of RBCOT w/ VIC control scheme

Figure 2.24 RBCOT w/ VIC control circuit diagram and constant Q -value variation.

Figure 2.24(a) shows the Q -value variations with different VIC time constant, $\tau_{VIC} = R_{VIC}C_{VIC}$, along with the Q -value with constant Q -value circuit enabled. It can be found that when the constant Q -value circuit is not enabled, quality factors vary with the duty cycle, and the variation depends on τ_{VIC} applied, which causes design difficulties as discussed in Figure 1.4(a). On the other hand, the Q -value can be well-controlled with the design rule proposed in equation (2.32).

Figure 2.25 shows the calculated and simulated $G_{vc}(s)$ of RBCOT w/ VIC with the constant Q -value circuit enabled under different duty-cycle conditions, where the validity of $G_{vc}(s)$ is proven in [7]. It can be seen that the Q -value at the half-switching frequency is well-controlled and duty-cycle-independent, that no peaking is presented with duty-cycle varying.

$$Q_2 = \frac{T_{sw}}{\pi \left[\left(1 + \frac{s_{ramp}}{s_f} \right) R_{Co} C_o - \frac{T_{sw}}{2} D \right]} \quad (2.33)$$

Where,

$$s_f = R_{Co} \frac{V_o}{L_s}, \quad s_{ramp(typ.)} = K_{ramp} V_o$$

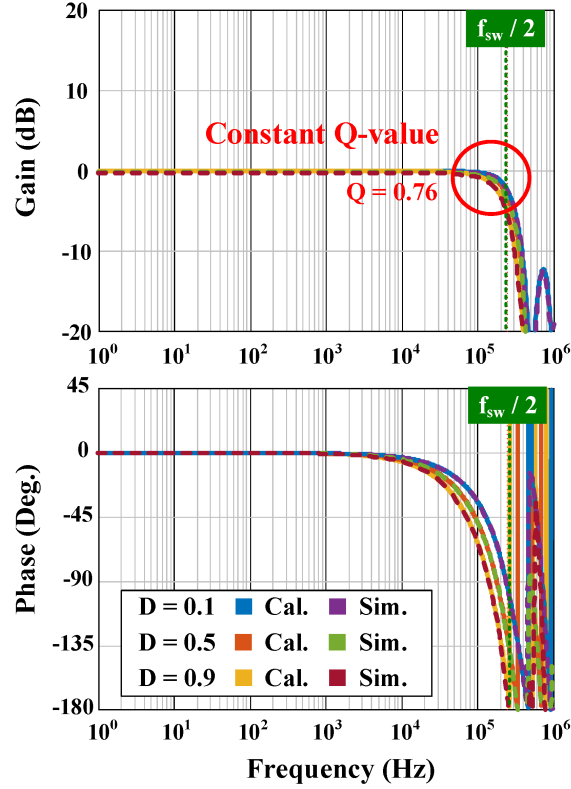


Figure 2.25 Control-to-output transfer function of RBCOT w/ VIC control scheme with constant Q -value control.

2.4.4.4 Ripple-based constant on-time control with continuous ramp compensation

In addition to the ripple-based control schemes mentioned above, the proposed constant Q -value control concept can also be applied to most other ripple-based COT-controlled Buck converters with continuous ramp compensation, where the continuous ramp refers to the type of ramp compensation without resetting the ramp to zero in a cycle [7], [11], [12], [43-46]. Note that RBCOT with discontinuous ramp compensation control schemes, [6], [17], [34], [35], [40], [47], are out of scope in this paper.

In general, the Q -value of RBCOT with continuous ramp compensation control schemes can be simplified as equation (2.33) where S_{ramp} stands for the ramp compensation slope added

to the RBCOR control that enhances to equivalent ESR, and S_f is sensed inductor current slope due to output voltage ripple in RBCOT modulation. It is worth mentioning that S_{ramp} is subject to change in different control schemes and implementations, and to make an in-phase ramp with the inductor current that enhances equivalent ESR, S_{ramp} is typically a function of V_o , i.e., equation (2.30). Hence, S_{ramp} is assumed to be a function of V_o with a constant gain, K_{rmap} , here.

With equation (2.33), the constant Q -value strategy can be applied as follow: 1) simplify the Q -value expression, as shown in equation (34), by substituting S_f into equation (2.33). 2) The relationship between S_{ramp} and the control inputs, which are duty cycle and V_o in this case, can be identified. S_{ramp} should be capable of eliminating the Q variations caused by duty cycle and V_o variation. 3) S_{ramp} , then, needs to be redesigned, and according to step 1, the original S_{ramp} is capable of eliminating V_o variation but unable to compensate the duty-cycle variation. As a result, a duty-cycle compensation term should be added to the original S_{ramp} . Finally, the new ramp slope can be designated as equation (2.35), and the Q -value expression can be rewritten as equation (36). A constant Q -value can be achieved while a_1 equals a_2 and the Q -value can be set by Q_{init} .

$$Q_2 = \frac{T_{sw}}{\pi \left[\left(1 + \frac{L_s S_{ramp}}{R_{C_o} V_o} \right) R_{C_o} C_o - \frac{T_{sw}}{2} D \right]} \quad (2.34)$$

$$S''_{ramp} = K_{ramp} (\alpha + \beta D) V_o \quad (2.35)$$

$$Q_2'' = \frac{T_{sw}}{\pi} \frac{1}{(Q_{init} + a_1 D - a_2 D)} \quad (2.36)$$

Where,

$$Q_{init} = R_{C_o} C_o + C_o L_s K_{ramp} \alpha, \quad a_1 = C_o L_s K_{ramp} \beta, \quad a_2 = \frac{T_{sw}}{2}$$

2.5 Experimental Verification

A fully discrete Buck converter with UFTCOT control is implemented in this work and designed in a way to support both a conventional IQCOT control technique, along with the proposed UFTCOT control technique to verify the behavior of the proposed control scheme and constant Q -value concept. The test setup and PCB design of the prototype are shown in Figure 2.26(a) and (b), where a detailed schematic for the implementation is illustrated in Figure 2.27, and the experimental parameters are listed in Table 2.1.

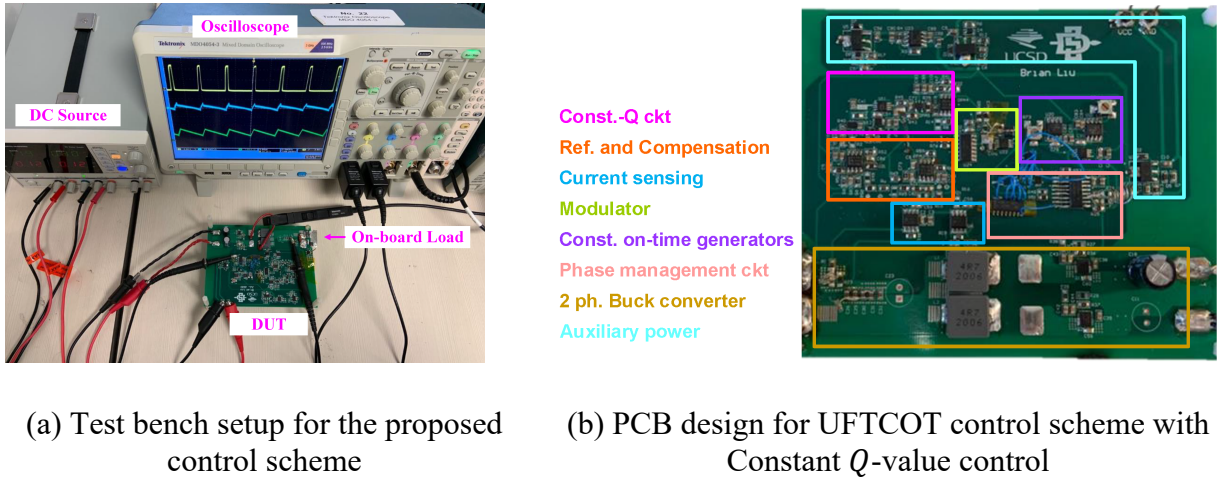


Figure 2.26 Tech Bench and PCB design.

In this work, a reconfigurable fully-discrete system is adopted for behavioral and SSM verification. An on-board load is adopted to achieve a fast load transient in order to ensure the performance of the loop is stressed under the most difficult of conditions without the effects of ringing due to the parasitics of connecting to an electronic load. Note that: the capacitor current sensing of this prototype is implemented by the resistor sensing, where a small resistor is inserted, and the capacitor current is then measured by the resistor voltage. According to the parameters listed in Table 2.1 and equation (2.23), the quality factor of the system is approximately equal to 0.6 when the constant Q -value circuit is enabled.

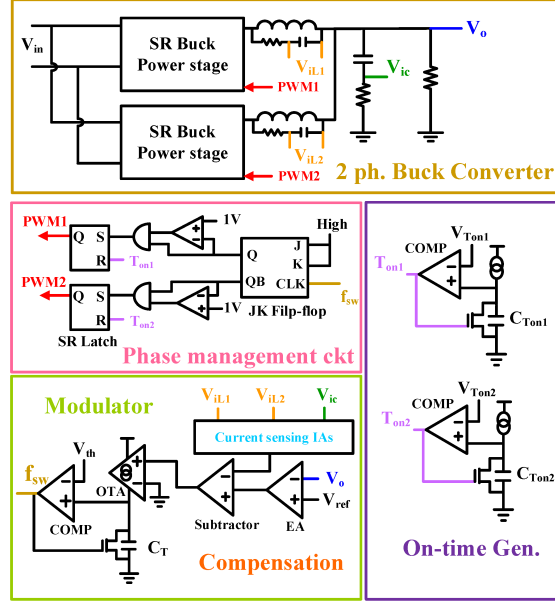


Figure 2.27 Circuit Schematic for the implementation.

Table 2.1 Experimental parameters

Parameters	Values
Input voltage range V_{in}	2.5-12 V
Output voltage range V_o	1.2 V
Output current range I_o	0-10A
Switching frequency f_{sw}	300 kHz
Output inductor L_s	4.7 μ H
Output capacitor C_o	220 μ F
Equivalent series resistance ESR	10 m Ω
Threshold capacitor C_T	1 nF
Modulator transconductance g_m	8 mA/V
Sensing gain R_i	0.1 V/A
Const. Q -value ckt. Transconductance g_{mQ}	1 mA/V
Const. Q -value ckt. capacitor 1 C_1	1 nF
Const. Q -value ckt. capacitor 2 C_2	100 pF
Const. Q -value ckt. V_y gain k	2.8 V/V
Const. Q -value ckt. V_o gain α	1 V/V

In the implemented circuit, owing to the limitation of discrete components, the switching frequency is set to 300kHz, and a 4.7 μH inductor is chosen to ensure continuous-conduction mode (CCM) operation at this frequency. A simple capacitor current sensing technique is employed, which inserts a small series resistor in the capacitor path and senses the voltage across the resistor, to simplify the implementation while verifying the behavior. This is why there is a relatively large ESR in Table 2.1. There are several other more advanced capacitor sensing techniques that could be employed in future work [48-50].

Design of the control stage parameters, i.e., g_m , R_i , and C_T , is limited by available discrete components. For example, the g_m needs a compromise between maximum source current capability and its transconductance to prevent output saturation. For the R_i , it requires a trade-off between noise and circuit performance because the series resistor method is applied. That is, a small resistance may be sensitive to noise; on the other hand, a large resistance deteriorates load transient performance. Here, g_m and R_i are chosen as 8 mA/V and 0.1 V/A, respectively. Finally, C_T can be designed based on Q_2 in equation (2.15), where the recommended Q_2 is from 0.6 to 0.9 [51] to prevent an extra phase drop at low frequencies resulting from a low- Q value and an excessive peaking following by a high- Q value. In this work, Q_2 is designed to be 0.6 and C_T is therefore around 1nF because the other variables, i.e., g_m and R_i , are already decided.

All together, both power stage and control stage design will vary depending on the implementation applied. For example, if an integrated-circuit implementation is employed, the switching frequency can be much higher, around 700kHz to 1MHz or even higher; therefore, the inductor size can be reduced significantly. Besides, an integrated current sensing technique can be used to prevent large ESR. For the control stage design, the value of g_m , R_i , and C_T will be limited

by the process and topology of OTAs and sensors adopted. Still, the control design should be based on Q_2 in equation (2.15) to ensure a stable operation.

2.5.1 Steady-State Operation Waveforms

Figure 2.28 shows the modulation waveforms of the UFTCOT control scheme at 12/1.2V, which works well and are similar to modulation law illustrated in Figure 2.4(a). When the ramp voltage, V_{ramp} , is equal to the threshold voltage, V_{th} , the duty signal is triggered and V_{ramp} is reset to zero. The two-phase modulation waveforms under different duty cycle conditions are shown in Figure 2.29(a) and (b). As analyzed, the converter works well even when it operates at the ripple cancellation point where the duty cycle equals 50%, as shown in Figure 2.29(a). Figure 2.29(b) shows a low duty cycle situation and the ramp in modulation is a non-linear ramp. It should be noted that because of the switching noise of sensed current, the V_{ramp} experiences discharging when the $Duty_{1,2}$ is turned off.

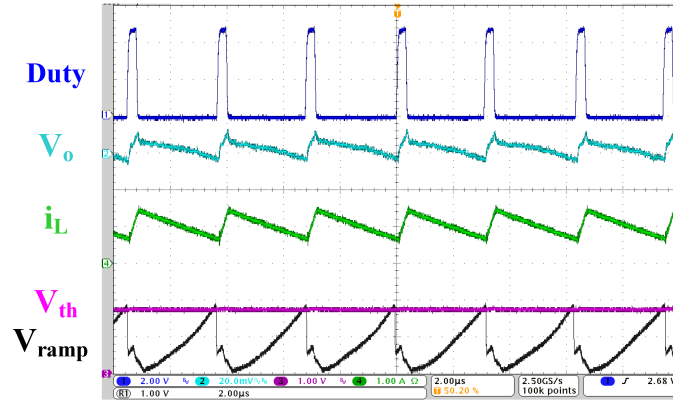
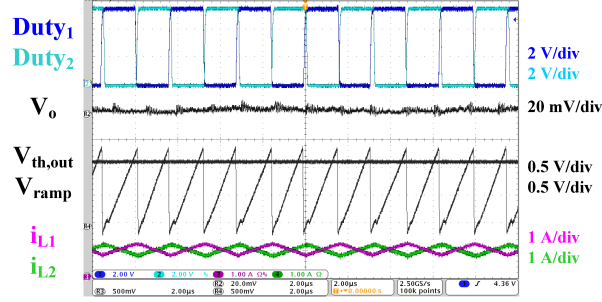
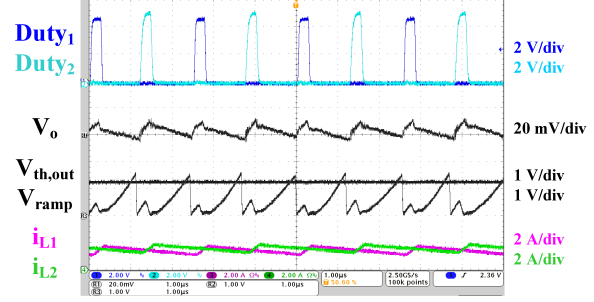


Figure 2.28 Modulation waveforms at $D \approx 0.1$, 12-1.2V, $Q \approx 0.6$.



(a) Operation waveforms at $D=0.5$

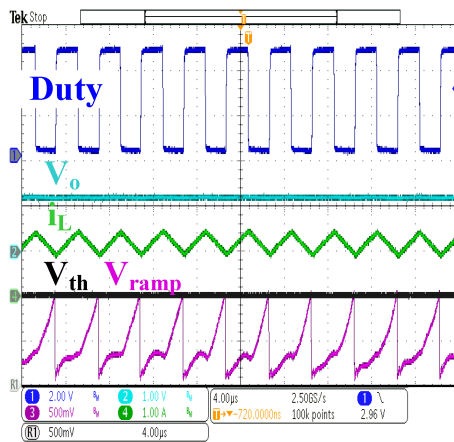


(b) Operation waveforms at $D=0.1$

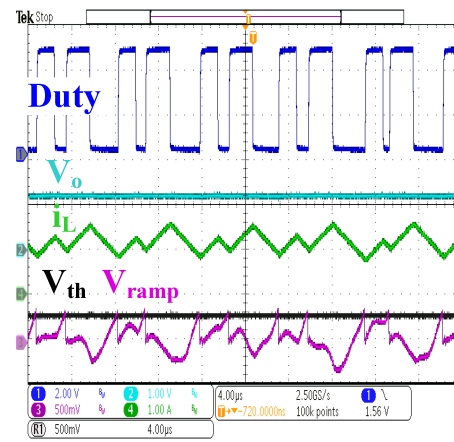
Figure 2.29 Multi-phase operation waveform of UFTCOT.

2.5.2 Constant Q -Value Circuit Verification

Figure 2.31 shows the steady-state waveforms when the duty cycle is equal to 50% with and without constant Q -value circuit. With the constant Q -value circuit, the system can operate stably, as shown in Figure 2.31(a). In contrast, the system shows subharmonic oscillations without the constant Q -value circuit, as shown in Figure 2.31(b), implying system instability. Note that to simulate the unstable condition, the circuit parameters are deliberately adjusted, which are thus not exactly the same as in Table 2.1. Still, both stable and unstable conditions in Figure 2.31 are tested under the same parameter setup.

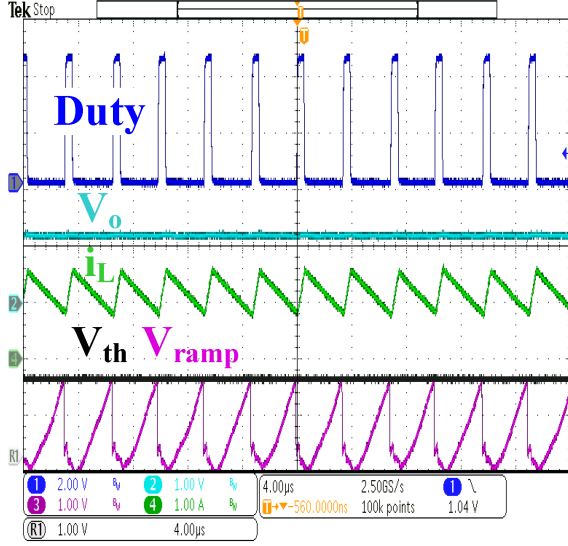


(a) Stable operation , $\alpha=0.3$, $\beta=0.93$,
(constant Q -value circuit enabled)

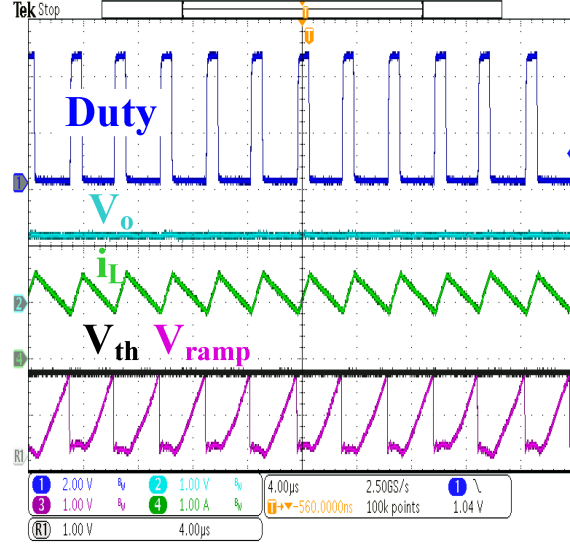


(b) Unstable operation , $\alpha=0.3$, $\beta=0$, (constant
 Q -value circuit disabled)

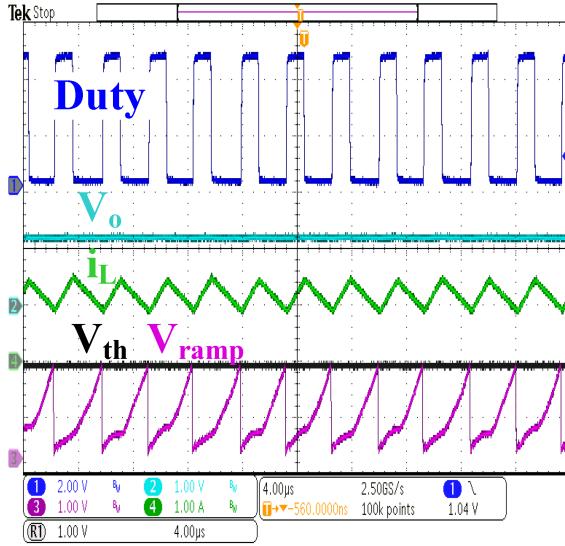
Figure 2.30 Operation waveforms at $\approx 50\%$ duty cycle, 2.5-1.2V.



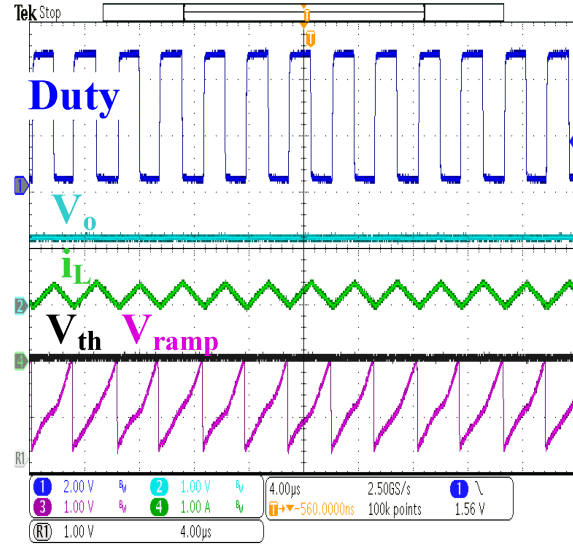
(a) $D \approx 0.15$, 8-1.2V



(b) $D \approx 0.25$, 5-1.2V



(c) $D \approx 0.38$, 3.3-1.2V



(d) $D \approx 0.5$, 2.5-1.2V

Figure 2.31 Steady-state operation waveforms at different duty cycle with constant Q -value circuit enabled ($Q \approx 0.6$).

Figure 2.31 shows the steady-state waveforms at different duty cycles to verify the modulation and proposed constant Q -value circuit. It can be seen that the threshold voltage, V_{th} , is well-matched with the $(\alpha + \beta D) \times V_o$ concept that, with a higher duty cycle, a higher V_{th} is generated to control the Q -value of the system.

The accuracy of the proposed constant Q -value circuit is essential in guaranteeing constant Q -value during operation since there are many error sources involved in V_Q generation, such as mismatch, noise, and so on. To determine how many errors are generated during sample and hold, amplifying, and summing, the accuracy of the constant Q -value is measured. In Figure 2.32, the left y-axis shows the voltage and Q -value, while the right y-axis shows the percentage of the error. The calculation and measurement results of V_Q and Q -value, labeled at the top-left corner in Figure 2.32, are shown in solid and dashed lines, respectively, referring to the left axis. On the other hand, the error of V_Q (V_Q Error) and Q -value (Q -value Error), labeled at the top-right corner in Figure 2.32, are shown in solid and dashed lines referring to the right axis. Here, the error of the constant Q -value voltage (V_Q Error) is less than 2%, and the error of the Q -value (Q -value Error) is less than 3%. Note that since the Q -value cannot be directly measured, the measured Q -value shown in Figure 2.32 is obtained from equation (2.22) using actual circuit parameters, and measured V_Q , as shown in Table 2.1, and Figure 2.32.

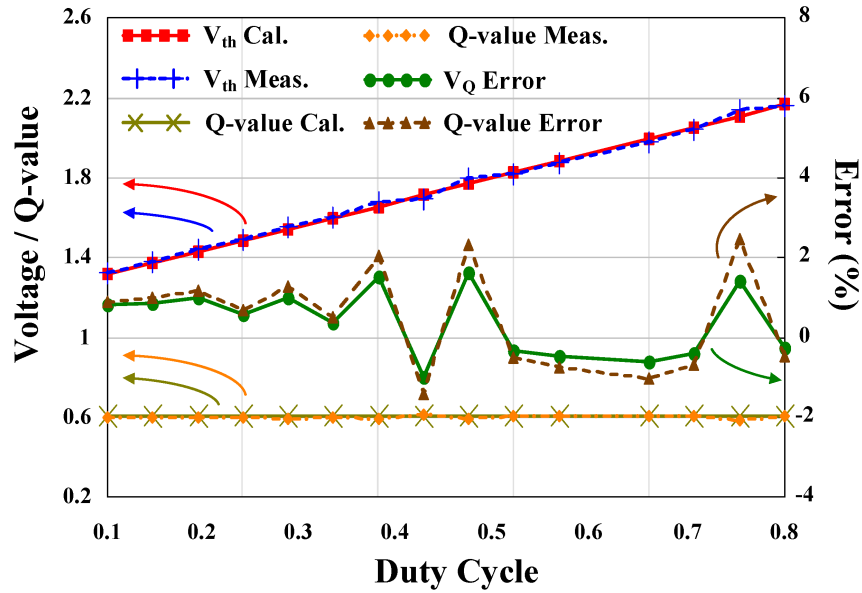


Figure 2.32 Accuracy of constant Q -value circuit.

2.5.3 Small-Signal Model Verification

To validate the small-signal model proposed in Chapter 2.3, the control-to-output transfer function is measured under different input voltage conditions (12V and 5V) while converting down to 1.2V. The measurement is performed by a lock-in amplifier, which injects a small-signal perturbation with a DC bias to the V_c terminal while disabling the error amplifier, and then measures the gain and phase from V_c to the output. Figure 2.33(a) and (b) present the measurement results of the control-to-output transfer function, where the red lines are the calculation results as derived in the previous section, while the blue lines are the measurement results. As shown, the measurement results are well-matched with the calculation results for frequencies below $f_{sw}/2$.

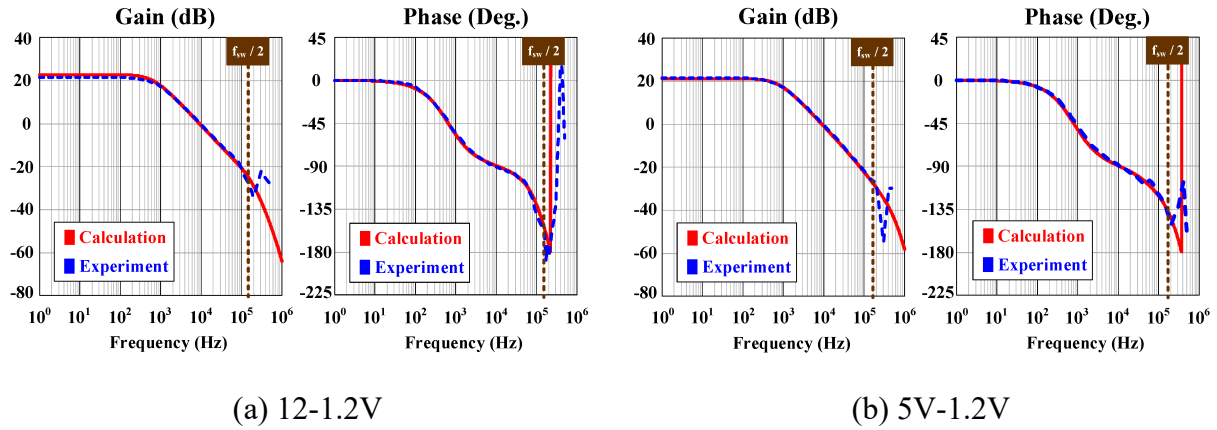


Figure 2.33 Control-to-output transfer function results for the UFTCOT control scheme with constant Q -value circuit disabled.

On the other hand, to verify the proposed constant Q -value method and circuit applied to the UFTCOT control scheme, the control-to-output transfer function of UFTCOT with the constant Q -value circuit is both calculated and measured as shown in Figure 2.34, where the transfer functions of 12V, 5V, and 3.3V to 1.2V cases are conducted. It can be seen that the measurement results are matched with the calculation results implying that the Q -value is well controlled. Another worth mentioning point from the transfer function measurement results is that since the

constant Q -value method proposed does not change the original modulation law of UFTCOT, the model introduced in equation (2.15) can be directly applied, and the same logistics can also be applied to the rest of COT control schemes.

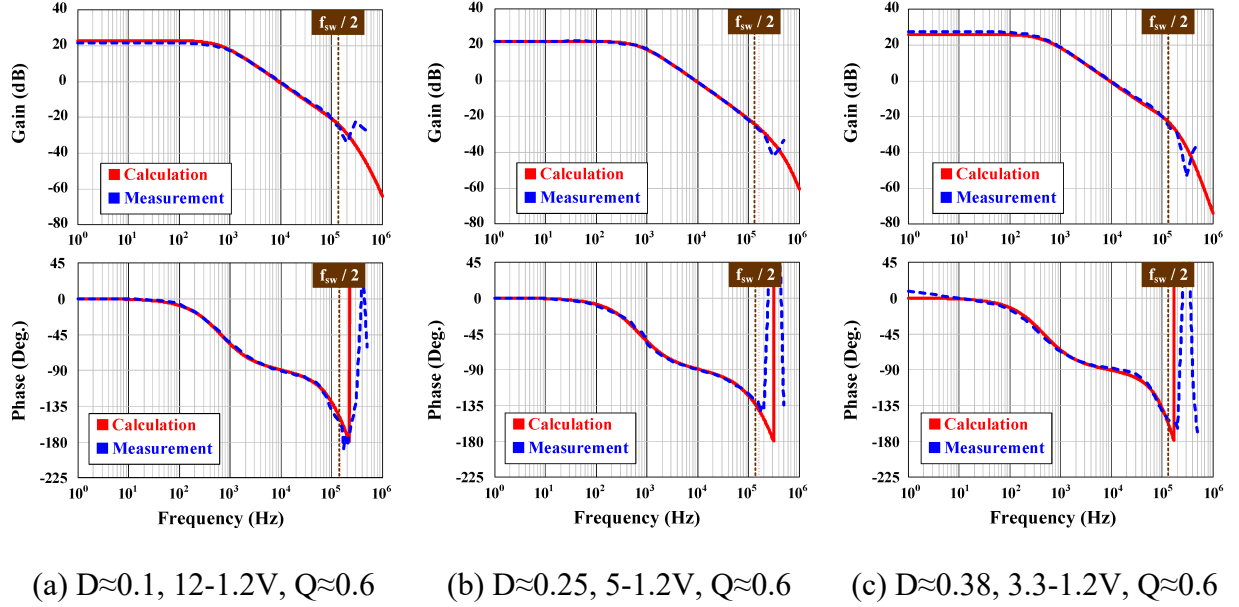


Figure 2.34 Control-to-output transfer function results for the UFTCOT control scheme with constant Q -value circuit enabled.

2.5.4 Transient Response Verification

The most significant benefit of the proposed control scheme is fast load transient response. To examine its transient performance, the following test conditions are employed: the input voltage is 12V, the output voltage 1.2V, and the output current changes from 1A to 6A. As aforementioned, the load transient is achieved by an on-board transient tool whose slew rate is as high as 50 A/ μ s to ensure the controller is properly stressed. Note that to have a fair comparison, a PI compensator is applied to make both controls have similar crossover frequency and phase margin. The

calculation result is shown in Figure 2.35, where the crossover frequency is around 15kHz and the phase margin is around 75 degrees.

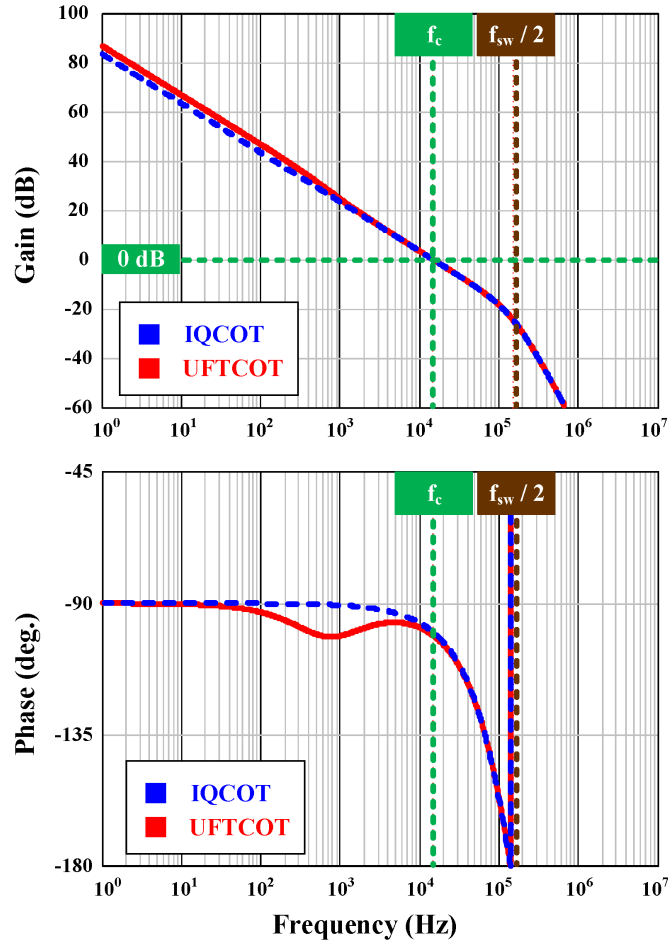


Figure 2.35 Loop gain for transient comparison.

A dynamic load transient with different frequencies is performed, and the results are shown in Figure 2.36. When the dynamic frequency is 100 Hz, both the proposed control scheme and IQCOT control can regulate the output voltage at 1.2V, but the response time of the proposed control is clearly faster than the IQCOT control. Then, as the dynamic frequency is further increased to 1 kHz, the IQCOT control is no longer capable of output voltage regulation, as shown in Figure 2.36(c). On the contrary, the proposed control still regulates the output voltage easily, as shown in Figure 2.36(d), due to its superior transient performance.

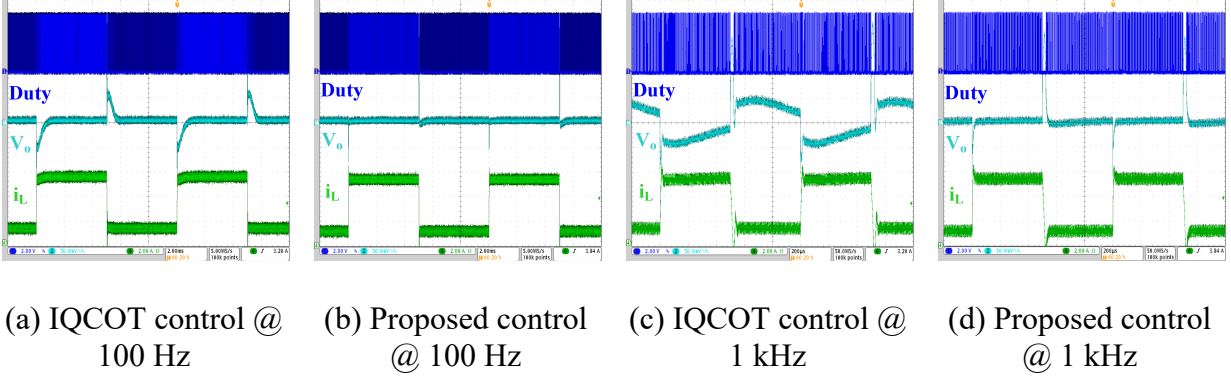


Figure 2.36 Dynamic load transient response.

To better quantify the performance, the zoomed-in load transient responses are shown in Figure 2.37. Figure 2.37(a) shows the transient response of the IQCOT control, whose voltage drop is 102 mV, response time is 6 μ s, and settles after 600 μ s. On the other hand, for the proposed control, the voltage drop is 53 mV, the response time is 1 μ s, and it settles within 20 μ s, as shown in Figure 2.37(b). Moreover, $V_{th,out}$ in Figure 2.37(b) shows a non-constant threshold voltage during load transients, which is the same as the transient illustration in Figure 2.5. Also, it should be noted that because of the internal resistance of the discharge switch, the discharging rate is limited and, hence, the V_{ramp} in Figure 2.37(b) is not reset to zero in the process of load transient. Clearly, the proposed control scheme is far faster than IQCOT control scheme.

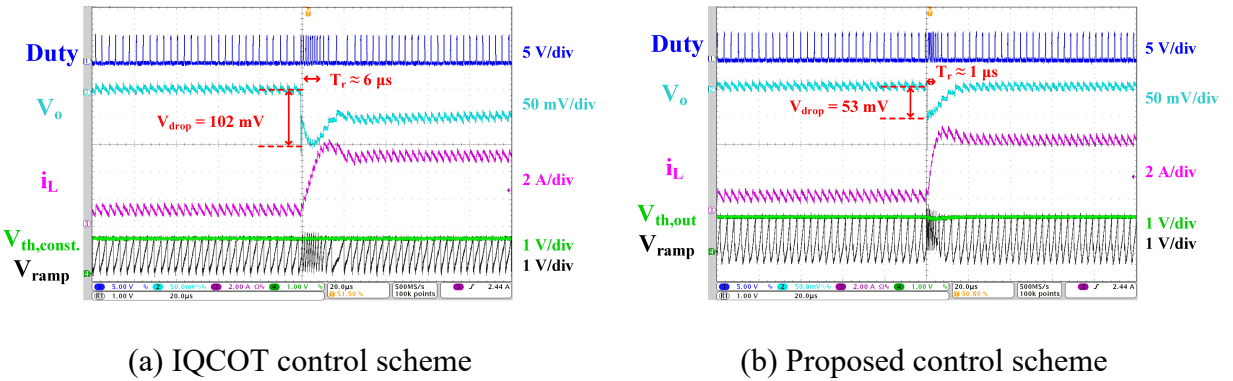


Figure 2.37 Load transient response comparison with different control scheme.

The constant Q -value circuit not only prevents the system instability in a wide-duty-range operation but also improves the load transient response. As known, the high Q -value in the output impedance will cause a ringing effect during a fast load transient. Figure 2.38 shows the load transient response for different input voltage (12V and 5V) while converting down to 1.2V with and without the constant Q -value circuit. Figure 2.38(a) shows the load transient response with a 12V input voltage which serves as a control. Figure 2.38(b), and Figure 2.38(c) shows the load transient response with a 5V input voltage with and without the constant Q -value circuit. It can be seen that the output voltage waveform in Figure 2.38(a) and Figure 2.38(b) does not exhibit ringing during the transient response. In contrast, from equation (2.15), the lower the input voltage is, the higher the Q -value will be, and therefore, Figure 2.38(c) shows a ring back phenomenon because of a higher Q -value.

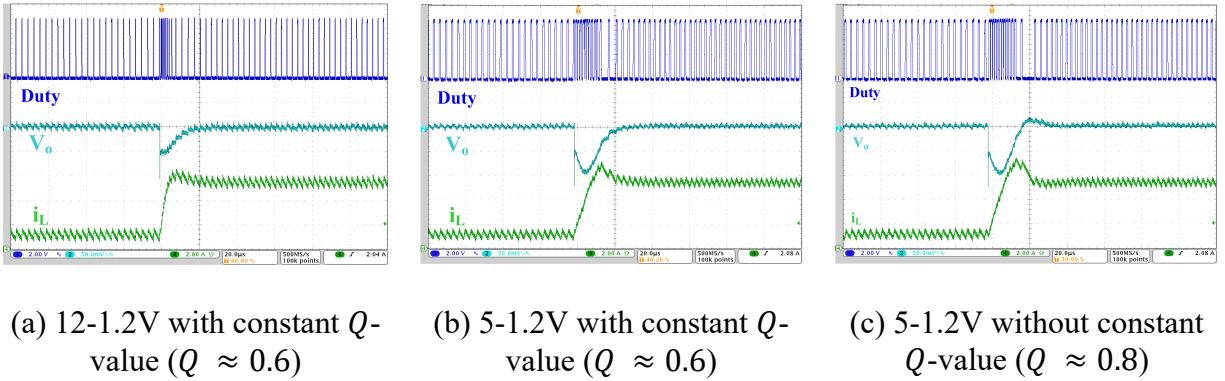


Figure 2.38 Load transient comparison with and without constant Q -value mechanism.

2.6 Conclusion

An ultra-fast transient constant on-time (UFTCOT) control is proposed in this chapter to improve stability and load transient performance while enabling simple multi-phase operation. Due to the capacitor current feedback and output voltage threshold, the response time of UFTCOT is 6x faster than IQCOT control. Importantly, thanks to the built-in charging modulation, the

instability issue in multi-phase operation is readily addressed. Moreover, the small-signal models for UFTCOT control are also derived, providing system design guidelines and verifying its transient performance. In addition, a generalized strategy to design a well-controlled and duty-cycle-independent quality factor for COT-controlled Buck converters. A design example under a baseline UFTCOT control scheme is illustrated and verified by both simulations, calculations, and experiments. The constant Q -value circuit is capable of ensuring system stability and improving load transient response, all while alleviating high bandwidth design efforts in a COT Buck controller over a wide input-output voltage range. The proposed design strategy is also extended and applied to several other state-of-the-art COT control schemes, as verified by both calculations and simulations. In summary, using the strategy presented in this chapter, a simple, well-controlled, and duty-cycle-independent Q -value (constant Q -value) can be achieved in most COT-controlled Buck converters. Finally, a series of experiments are performed to validate the proposed methods.

Acknowledgements

Chapter 2 is based on and mostly a reprint of the following publication(s):

- W. -C. Liu, C. -H. Cheng, C. C. Mi and P. P. Mercier, "A Novel Ultrafast Transient Constant on-Time Buck Converter for Multiphase Operation," in *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 13096-13106, Nov. 2021, doi: 10.1109/TPEL.2021.3076430.
- W. -C. Liu, C. -H. Cheng, P. P. Mercier and C. C. Mi, "Small-Signal Analysis and Design of Constant On-Time Controlled Buck Converters With Duty-Cycle-Independent Quality Factors," in *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 8379-8393, July 2023, doi: 10.1109/TPEL.2023.3268613.

Chapter 3 Hybrid Series/Parallel PR-based Converters with 48V Bus Voltage

3.1 Introduction

The increasing demands for high-efficiency, lightweight, and low-cost miniaturized power converters are starting to highlight the limitations posed by magnetic passive elements. While conventional electromagnetic-based converters are renowned for their fast response, ease of control, and high-power capability, the sublinear scaling property of magnetic components [18], where the magnetic size reduces nonlinearly with an increase in frequency, limits the pathway towards converter miniaturization. Consequently, there is a growing interest in exploring alternative energy storage forms, materials, and devices to replace magnetic components [19], encompassing diverse manifestations such as kinetic, elastic, and electrostatic energy storage. Piezoelectric devices, especially piezoelectric resonators (PRs), have gained significant attention as magnetics replacements in DC-DC converters due to the promising high efficiency and power density [28-32], [52-54].

Unfortunately, the most state-of-the-art PR-based converters, especially for step-down applications, exhibit peak efficiency at a 0.5 voltage conversion ratio (VCR), defined as (V_o/V_{in}) , with efficiency declining exponentially as the VCR decreases. The efficiency degradation arises from the low PR utilization factor, K , defined as the ratio of charges transferred to the output, Q_{out} , to the total charges in the PR including charges delivered to the output, Q_{out} , and charges circulated, Q_{cir} , inside the converter. That is, a lower K results from a large Q_{cir} indicating poor efficiency [29]. This characteristic restricts the usage of PR-based converters in modern electronic applications, whose conversion ratio is typically below 0.2.

To overcome the efficiency challenge under large step-down conversion scenarios popularized by many applications, i.e., computing, automotive, and consumer electronics, the hybrid Frontside Series/Parallel PR-based (FSPPR) and Backside Series/Parallel PR-based converters are introduced in this Chapter. These hybrid PR-based converters leverage the concept of switched capacitor hybridization, popularized by inductor-based DC-DC converters [55-60] in recent years, to enable optimal operation of the PRs while all while maintaining an overall compact size and all of the advantages of PR-based converters, i.e., ZVS and soft-charging of capacitors. Finally, the converter prototypes are built with a disk-shaped PZT piezoelectric resonator operating in a radial vibration mode and can be reconfigured as a co-designed baseline PR-based converter for fair comparisons.

3.2 Introduction to Piezoelectric Resonators

This section reviews the materials and vibration modes of PRs that exhibit promising performance. Subsequently, PR parameter extraction for the BVD equivalents, utilizing the PR constants from datasheets, is introduced. The effect of PR sizing is also discussed.

There are a variety of piezoelectric materials available on the market primarily designed for use in ultrasonic sensors, actuators, and energy harvesters [61-64], rather than for power conversion applications. Considering the absence of market-available, power-optimized PRs, not all piezoelectric materials are appropriate for power conversion intention.

According to prior research [30], [65], [66], three materials have demonstrated potential for power-optimized design: 1) Hard-PZT (Lead Zirconate Titanate), 2) LNO (Lithium Nickel Dioxide), and 3) AlN (Aluminum Nitride). Table 3.1 lists the key parameters of these piezoelectric materials obtained from [67]. An ideal material for power conversion shall exhibit a high

coupling/quality product, kQ , indicating excellent electric-mechanical coupling (small C_p relative to motion branch) with minimal mechanical motion loss (small R). Additionally, a high Curie temperature is advantageous, which enables 1) ease of packaging/mounting, and a broad safe operating area (SOA), ensuring that the material is resilient against high temperatures without depolarization and loss of piezoelectric properties. Note that, due to the anisotropic behavior of piezoelectric materials, different vibration modes lead to different coupling factors.

Table 3.1 Piezoelectric material properties [30], [67]

	Hard-PZT (PIC181)	LNO (Y + 36° cut)	AlN
Vibration Mode	Radial	Thickness extensional	Thickness extensional
Dielectric constant ϵ_r	1200	29.7	10.4
Mech. quality factor Q	≈ 2000	$\geq 10,000$	$\geq 4,000$
Coupling factor k_{33} or k_p	0.66	0.61	0.31
Curie temperature T_c , °C	330	1,150	$\geq 1,000$

PZT ceramics offer significant advantages due to their market availability in standard sizes and consistent production [67] with a decent kQ . Although their high dielectric constant leads to increased dielectric loss, it enables an operating frequency range from hundreds of kHz to a few MHz. This range, compared to other materials, facilitates achieving a more compact size in the low-frequency spectrum (kHz to MHz), which is a more favorable range for power applications, considering the controllability. This means a better volume/frequency scaling property within an operating range of interest. However, the relatively low quality factor, compared to others, contributes additional mechanical loss to the system, limiting power handling capability.

LNO, a monocrystalline material, features a significantly lower dielectric constant, suggesting an operational frequency from a few MHz to a hundred MHz. Its exceptionally high-

quality factor and Curie temperature facilitate low mechanical loss and high power capability. However, LNO PRs are only available on demand with predefined design, including geometry and cut ($X + 41^\circ$, $Y + 36^\circ$, $Y + 163^\circ$, Z , etc.).

AlN, a CMOS-process-compatible material, is appealing for converter integration and miniaturization. However, the reduced k_{33} implies less efficient operation, and its even lower dielectric constant shifts the operation frequency into the GHz range imposing an extremely daunting task to stably control the system, especially in DC-DC converters.

Aside from materials, piezoelectric resonators exhibit several common vibration modes, including length/width extensional, thickness shear/extensional, contour extensional, and radial modes [68]. Of these, radial and thickness modes stand out in PR-based converters. Specifically, disk-shaped PZT PRs operating in radial mode [29], [69-71] and disk/rectangular-shaped LNO PRs in thickness mode [30], [66] are prevalent. Radial mode PZT PRs are characterized by their spurious-free response, whereas thickness mode LNO PRs are characterized by their power handling capability; however, LNO PRs are prone to spurious interventions, leading to additional losses. The spurious modes can be mitigated with special geometrical design [32].

According to [65], the PIC181 material showcases excellent areal loss and mechanical loss attributes, making it an ideal candidate for this work. Another promising candidate is C213 material, but it is exclusively fabricated upon custom orders with extended lead times of several months, rendering it, strictly speaking, not commercial off-the-shelf. Hence, it is also ruled out from the list. In this study, disk-shaped radial mode PZT PRs are chosen for proof of concept owing to their commercial off-the-shelf (COTS) availability, favorable volume/frequency scaling within the desired operating range, and spurious-free response.

In addition to the materials and vibration modes, understanding the limitations associated with specific sizes and their impact on overall performance, such as efficiency, is important. To address these concerns, insights can be gained through a BVD equivalent model, which serves as a simplified behavioral model. The BVD model of PR is illustrated in Figure 3.1 where the R , L , and C represent the mechanical components related to elastic loss and mechanical vibrations. Additionally, C_p is the piezo-static capacitor attributing to electrodes [72].

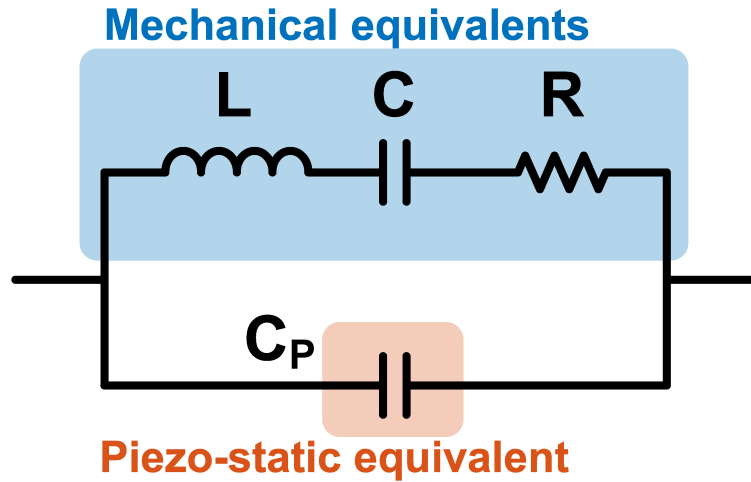


Figure 3.1 Butterworth Van-Dyke equivalent model for piezoelectric resonators.

The parameters of the BVD model for a disk-shaped PR can be found from four piezoelectric constants along with geometrical constants: 1) dielectric constant, ϵ_{33}^T , 2) quality factor, Q , 3) coupling factor, k_p , and 4) vibrating frequency constant, N_p , 5) the geometrical radius, r , and 6) thickness, l . According to the definitions of the constants, BVD model equivalents in the form of these constants can be written as equations (3.1)-(3.4) with f_r and f_{ar} representing the resonant and anti-resonant frequencies, respectively. Here, C_p is derived from its definition [68]; C is determined from f_r/f_{ar} with C_p and the definition of k_p [73]; L is found by the definition of f_r [67] with C ; Finally, R is obtained from L and C . Note that adopting different K_p definitions lead to differences in expressions.

$$C_p = \epsilon_{33}^T (1 - k_p^2) \frac{\pi r^2}{l} \quad (3.1)$$

$$C = k_p^2 C_p \quad (3.2)$$

$$L = \frac{r^2}{\pi^2 N_p^2 k_p^2 C_p} \quad (3.3)$$

$$R = \frac{1}{Q} \sqrt{\frac{L}{C}} = \frac{1}{\pi^2 Q \epsilon_{33}^T N_p (1 - k_p^2) k_p^2} \frac{l}{r} \quad (3.4)$$

Where,

$$k_p = \sqrt{\frac{f_{ar}^2 - f_r^2}{f_r^2}}, \quad Q = \frac{1}{R} \sqrt{\frac{L}{C}}, \quad f_r = \frac{N_p}{2r} = \frac{1}{2\pi\sqrt{LC}}, \quad f_{ar} = \frac{1}{2\pi\sqrt{L\frac{C_p C}{C_p + C}}}$$

The PR model in equations (3.1)-(3.4) can be verified by comparing it with the measurement results. Table. 3.2 illustrates the parameters of the piezoelectric resonator in both measurement and calculation where the measurement results are obtained from the parameter extraction of the PR's impedance measured by vector network analyzer (VNA). Here, the coefficients for the calculation are obtained from the datasheet of the PIC181 material [67]. A close correspondence between calculated and measured results is observed, with the notable exception of the mechanical resistance, R , which exhibits a significant increase. This increase is primarily attributed to the absence of appropriate packaging during measurement. The degradation of R is also reflected in the reduced quality factor, Q .

Table 3.2 Parameters of disk-shaped radial-mode piezoelectric resonator in a size of 20/0.2mm
(diameter and thickness) and PIC181 material

	C_p (nF)	C (nF)	L (μ H)	R (Ω)	f_r/f_{ar} (kHz)	Q
Calculation	10.8	3.4	578.9	0.21	113/130	2000
Measurement	13.96	4.2	468.78	0.48	113/129	696

With the equations above and the selected material under the belt, the physical parameters, e.g., the size of PRs, can be translated into the electrical representatives for further analysis, such as loss analysis. The impact of diameter and thickness on the BVD model is summarized in Table 3.3. From this table, the resonant frequency solely depends on the diameter of PRs. This implies that smaller PRs can be utilized for higher operating frequencies. In contrast, the mechanical resistor, R , which is the primary source of loss in the PR, decreases with an increase in diameter and increases with an increase in thickness. Therefore, to minimize R , the PR should have a maximized diameter and minimized thickness, respectively. However, this design imposes fabrication difficulties due to the mechanical stress limitations while introducing a large passive component area. In addition, the piezo-static capacitor, C_p becomes significant, resulting in additional loss. The size optimization will be introduced in Chapter 5.

Table 3.3 Effect of PR sizing in BVD model

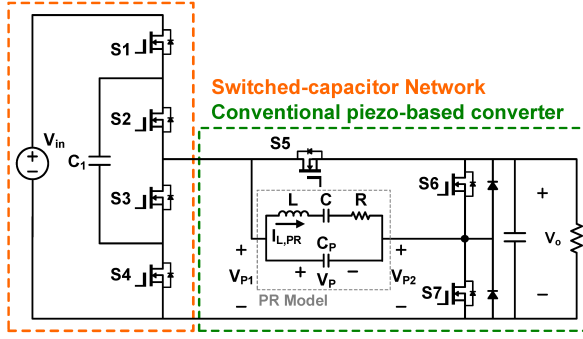
Parameter	Increase of Diameter	Increase of Thickness
f_r	Decrease(-)	No change(=)
C_p	Increase(+)	Decrease(-)
C	Increase(+)	Decrease(-)
L	No change(=)	Increase(+)
R	Decrease(-)	Decrease(-)
$V_{PR,max}$	No change(=)	Increase(+)

3.3 Frontside Series/Parallel Piezoelectric-Resonator-Based DC-DC Converter

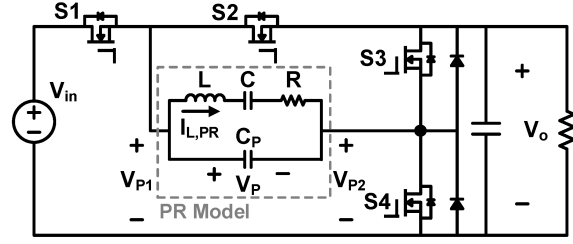
3.3.1 Circuit Diagram and Operation

The circuit diagram of the proposed Frontside Series/Parallel Piezoelectric-Resonator-Based (FSPPR) converter is shown in Figure 3.2(a), where the PR is represented by the BVD model. In the BVD model, R , L , and C refer to the mechanical vibration of the PR, while C_p is the piezo-static capacitor of the PR. From the equivalent model, the PR can be operated in either the inductive or capacitive regions, depending on the operation frequency. Here, the inductive region operation is adopted, enabling zero-voltage switching (ZVS) operation and, thereby reducing switching losses.

In front of the PR stage, a 2:1 switched-capacitor network is merged as the input stage, which can be viewed as a pre-step-down stage where switches S1-4 operate between series and parallel switched-capacitor modes to the PR stage. In the series switched-capacitor mode, S1 and S3 are turned on, placing the flying capacitor, C_1 , in series with the piezo-based stage; on the other hand, in the parallel switched-capacitor mode, S2 and S4 are turned on, placing C_1 in parallel with the piezo-based stage. In this configuration, the flying capacitor, C_1 , is clamped to half the input voltage, resulting in the reduction of voltage stress on switches in the SC network and the effective input voltage to the piezo-based stage, which is now approximately half the input voltage. This is a similar benefit that flying capacitor multi-level hybrid inductive buck converters enjoy. Therefore, the equivalent voltage seen across the PR stage is halved compared to the baseline PR-based converter.



(a) Frontside Series/Parallel PR-based converter



(b) Baseline PR-based Converter

Figure 3.2 Circuit diagram of Frontside Series/Parallel and Baseline PR-based converters.

It should be noted that switches S1-4 in the FSPPR topology effectively replace switch S1 in the baseline topology, as shown in Figure 3.2(b), and thus the SC stage is integrated into the PR stage with no additional cascaded losses presented. In addition, any control scheme applicable to the baseline converter could also be applied to the FSPPR converter. This will be explored in Chapter 6.

The operation waveforms and phases are depicted in Figure 3.3(a) and (b). The FSPPR converter operates through seven individual phases in a sequential manner, employing two alternative modes: series capacitor mode and parallel capacitor mode. Across these seven phases, the piezoelectric resonator (PR) can be in one of three connection states:

- 1) Connected PR state: In this state, the PR is connected to either the input source, the output load, or both, forming a loop in which energy is delivered to output while the PR stores or releases energy.
- 2) Shorted PR state: In this state, the PR is shorted by the external switches, and the resonant current, $I_{L,PR}$, circulates through the switches.

- 3) Opened PR state: In this state, the PR is opened, and the resonant current, $I_{L,PR}$, circulates within PR through the piezo-static capacitor, C_P , allowing soft-charging/discharging of the capacitor to achieve ZVS in the subsequent phase.

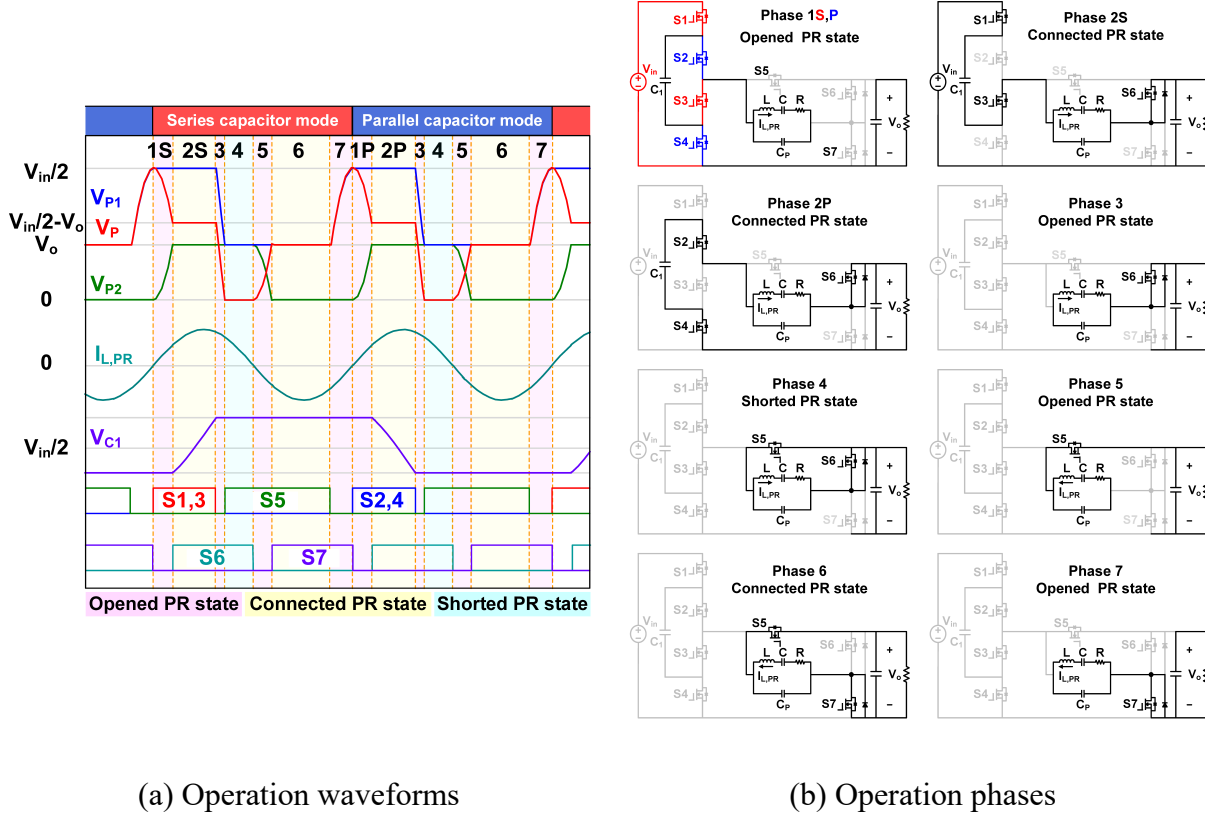


Figure 3.3 Operation waveforms and phases of Frontside Series/Parallel PR-based converter.

As illustrated in Figure 3.3(b), the PR is configured as an opened PR state in phases 1S and 1P where the piezo-static capacitor, C_P , is softly discharged by the inductive PR current, $I_{L,PR}$. The phase ends when V_{P2} reaches V_o , enabling ZVS for $S6$. In phase 1S, the flying capacitor, C_1 , is set to the up (series) configuration, while in the subsequent cycle, in phase 1P, C_1 operates in the down (parallel) configuration. In either case, $S6$ is activated once the drain-to-source voltage of $S6$ reaches zero, establishing a connection between the PR and the output and initiating phases 2S and 2P.

During phase 2S (series operation), the PR transfers energy from the input to the output while softly charging the flying capacitor (C_1), whereas phase 2P (parallel operation) involves the soft discharge of C_1 through $I_{L,PR}$ and delivers the energy to the output. Subsequently, in phase 3, switches S1-4 are all deactivated, placing the PR in an opened state, whereby $I_{L,PR}$ discharges C_P until $V_{P1} = V_o$, enabling ZVS for S5. Once $V_{P1} = V_o$, phase 4 begins, wherein both S5 and S6 are turned on, shorting the PR to maintain the continuity of the resonant current. Phase 4 ends as $I_{L,PR}$ crosses zero and reverses its polarity. At this point, S6 is switched off, returning the PR in the opened state again, and phase 5 begins. During phase 5, $I_{L,PR}$ once again softly charges C_P , causing V_{P2} to decrease until it reaches zero, enabling ZVS turn-on of S7. As soon as $V_{P2} = 0$, S7 is activated, connecting the PR to both the output and ground, releasing the stored energy to the load. Phase 7 begins with the deactivation of S5, placing the PR in the opened state, where C_P is softly charged by $I_{L,PR}$. This phase concludes when V_{P1} reaches V_{in} , thereby minimizing switching losses across S1,3/S2,4 in the following SC cycle.

3.3.2 Steady-State Analysis: PR Operation

This section includes mathematical derivations and discussions of the voltage conversion ratio (VCR), charge transfer, resonant current, and time duration approximations, with the aim of comprehending the behavior, operation, and performance of piezoelectric resonators in the proposed FSPPR converter. Finally, the loss breakdown and efficiency estimation are presented.

3.3.2.1 Voltage Conversion Ratio and PR Charge Transfer Utilization

Figure 3.4 illustrates the steady-state waveforms over a PR cycle in the proposed system. Due to the merged 2:1 SC network, the input voltage applied to the PR is half the input voltage

rather than the full input voltage in the baseline PR-based converter. During steady-state operation, the piezoelectric resonator must adhere to the principles of conservation of charge (CoC) and conservation of energy (CoE) to maintain charge and energy balance [29], [52]. Therefore, the CoC of the PR mechanical capacitor, C , and the piezo-static capacitor, C_P , must hold in equations (3.5) and (3.6), where q_n is the charge in phase n .

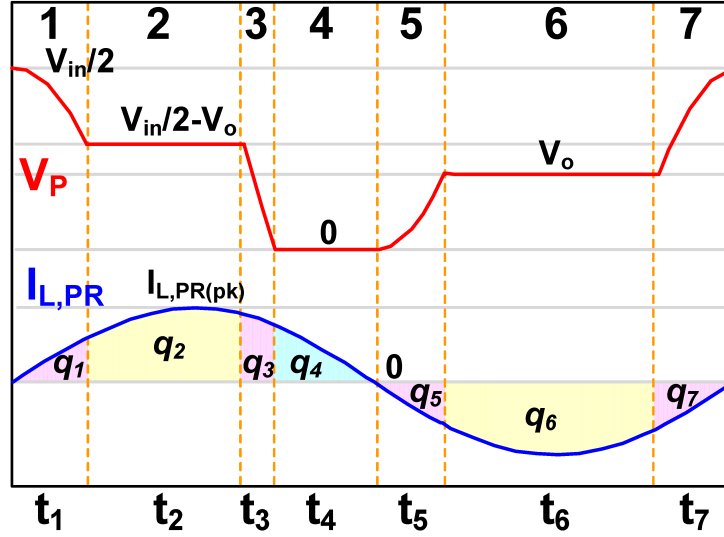


Figure 3.4 Waveforms of a PR cycle.

$$q_1 + q_2 + q_3 + q_4 + q_5 + q_6 + q_7 = 0 \quad (3.5)$$

$$q_1 + q_3 + q_5 + q_7 = 0 \quad (3.6)$$

By substituting equation (3.6) into equation (3.7), a balance in charge transfer between the connected and shorted states is revealed, yielding the following expression:

$$q_2 + q_4 + q_6 = 0 \quad (3.7)$$

On the other hand, only the connected states, phases 2 and 6, transfer energy, and hence the CoE must hold:

$$E_2 + E_6 = V_2 q_2 + V_6 q_6 = (V_{in}/2 - V_o) q_2 + V_o q_6 = 0 \quad (3.8)$$

Then, inserting equation (3.7) into equation (3.8) using $q_6 = -(q_2 + q_4)$, the voltage conversion ratio of the FSPPR converter can be found as:

$$0 \leq \frac{V_o}{V_{in}} = \frac{1}{2} \frac{q_2}{2q_2 + q_4} \leq \frac{1}{4} \quad (3.9)$$

The VCR is observed to depend on the ratio of charge in the connected state (phase 2) to the shorted state (phase 4) within the positive cycle of $I_{L,PR}$. Assuming that the charge in the opened states (phases 1 and 3) is small and negligible, a maximum VCR of 0.25 is achieved when phase 2 spans the entire positive cycle of $I_{L,PR}$, indicating the complete utilization of the positive cycle for energy transfer. Conversely, a minimum VCR of 0 is obtained when phase 4 occupies the entire positive cycle, signifying no energy is sourced from the input. Notably, the VCR range is halved compared to the baseline PR-based converter presented in [29], owing to the inclusion of the series/parallel SC network.

The PR charge transfer utilization factor (PR utilization factor, K) was first introduced in [29], and serves as an evaluation metric for how efficient the PR is used in a given topology with a specific phase sequence, regardless of materials, sizes, loss coefficients, etc. This factor is defined based on the concept of effective charge transfer, representing the portion of the charge in the connected and shorted states that ultimately contributes to the output.

Here, the PR utilization factor of the FSPPR converter can be defined as equation (3.10) and by substituting equations (3.6) and (3.7) into equation (3.10), the PR utilization factor can be rearranged in terms of V_{in} and V_o , which is shown in equation (3.11).

$$K = \frac{|q_2| + |q_6|}{|q_2| + |q_4| + |q_6|} \quad (3.10)$$

$$0.5 \leq K = \frac{V_{in}}{2(V_{in} - 2V_o)} \leq 1 \quad (3.11)$$

According to equation (3.11), K equals 1 when the VCR reaches its maximum value of 0.25, and, conversely, K equals 0 when VCR equals its minimum value, 0, implying that PR is most efficient at the maximum conversion ratio in the FSPPR converter where the duration of the resonant current circulating phase, phase 4, is minimum. In contrast, as the VCR reduces, K reduces as well, indicating inefficient utilization of the PR. Comparing to the baseline PR-based converter in [29], equations (3.9) and (3.11) show that the optimal efficiency is shifted down from the conversion ratio of 0.5 to 0.25.

3.3.2.2 Charge Transfer and PR Resonant Current

To derive the PR resonant current, $I_{L,PR}$, for the upcoming time duration and efficiency analysis, the total charger transferred and stored in the PR must be addressed first. There are two parts of charge transferred or stored in the PR: 1) the charge in connected and shorted state, Q_{CS} , and 2) the charge used to soft-charge/discharge C_P to achieve ZVS, Q_{ZVS} . The total charge can be expressed as equation (3.12) where V_{pp} is the voltage swing over C_P in a cycle and is notated as $V_{in}/2$ in the FSPPR converter.

$$Q_{total} = Q_{CS} + Q_{ZVS} = \frac{I_o}{Kf} + 2C_P V_{pp} \quad (3.12)$$

On the other hand, the total charge can also be expressed in terms of $I_{L,PR}$ as equation (3.13). By equating the equations (3.12) and (3.13), the amplitude of the PR resonant current, $I_{L,PR(pk)}$, can be derived equation (3.14).

$$Q_{total} = 2 \int_0^{\frac{1}{2f}} i_{L,PR}(t) dt \quad (3.13)$$

$$I_{L,PR(pk)} = \frac{\pi}{2} \left(\frac{I_o}{K} + f C_P V_{in} \right) \quad (3.14)$$

3.3.2.3 Steady-State Phase Duration Approximation

For an accurate estimate of the performance in the proposed converter, it is essential to determine the steady-state duration in each phase. With the PR resonant current derived above, the steady-state phase duration can be obtained by integrating the charges in each phase. In Figure 3.4, t_n represents the time duration in n-th phase. In this analysis, $V_{in,PR}$ is used to represent the effective input voltage for the PR, which is half the input voltage, $V_{in}/2$, in the FSPPR converter.

In phases 1S, and 1P, the resonant current discharges C_P from $V_{in,PR}$ to $V_{in,PR} - V_o$, and therefore, the voltage difference over C_P in phase 1 can be written as:

$$\Delta V_{C_P(t_1)} = -V_o = \frac{1}{C_P} \int_0^{t_1} -i_{L,PR}(t) dt \quad (3.15)$$

In phase 2, the PR is in the connected state, delivering energy to the output while storing energy in the PR. Based on the CoE in equation (3.8) and the loss due to the PR, the charge, q_2 , in phase 2 can be rearranged as equation (3.16) where P_{loss} represents the losses in the PR.

$$q_2 = \frac{P_o + P_{loss}}{V_{in,PR}f} = \int_0^{t_2} -i_{L,PR}(t + t_1) dt \quad (3.16)$$

In phase 3, the PR is in the opened state and discharges C_P from $V_{in} - V_o$ to 0. As a result, the voltage difference over C_P in phase 3 can be written as:

$$\Delta V_{C_P(t_3)} = V_{in,PR} - V_o = \frac{1}{C_P} \int_0^{t_3} -i_{L,PR}(t + t_1 + t_2) dt \quad (3.17)$$

In phase 4, the PR resonant current is freewheeling in a shorted loop, which ends when $I_{L,PR}$ reverses its polarity at the end of the positive cycle. Hence, the duration of phase 4, t_4 , is given by:

$$t_4 = \frac{1}{2f} - t_1 - t_2 - t_3 \quad (3.18)$$

In phase 5, again, the PR is in the opened state, and $I_{L,PR}$ charges C_P from 0 to V_o ; hence, the voltage across C_P can be written as:

$$\Delta V_{C_P(t_5)} = V_o = \frac{1}{C_P} \int_0^{t_5} -i_{L,PR} \left(t + \frac{1}{2f} \right) dt \quad (3.19)$$

In phases 6 and 7, phase 6 is a connected state that transfers energy from the PR to the output, while phase 7 is an opened state where $I_{L,PR}$ charges C_P from V_o to V_{in} . Therefore, the time duration of phase 7 can be derived in equation (3.20) by solving the voltage difference over C_P in phase 7. On the other hand, since the duration of phases 5, 6, and 7 is a half cycle, the duration of phase 6 can be found from t_5 , and t_7 in equation (3.21)

$$t_7 = \frac{1}{f} - t \quad (3.20)$$

where

$$\Delta V_{C_P(t_7)} = V_{in,PR} - V_o = \frac{1}{C_P} \int_t^{\frac{1}{f}} -i_{L,PR}(t) dt$$

$$t_6 = \frac{1}{2f} - t_5 - t_7 \quad (3.21)$$

By solving equations (3.15)-(3.21), the time duration of each phase can be expressed as:

$$\left\{ \begin{array}{l} t_1 = \frac{1}{\omega} \cos^{-1} \left(1 + \frac{-\omega C_P V_o}{I_{L,PR(pk)}} \right) \\ t_2 = \frac{1}{\omega} \cos^{-1} \left(\cos(\omega t_1) - \frac{2\pi(P_o + P_{loss})}{V_{in,PR} I_{L,PR(pk)}} \right) - t_1 \\ t_3 = \frac{1}{\omega} \cos^{-1} \left(\cos[\omega(t_1 + t_2)] + \frac{-\omega C_P (V_{in,PR} - V_o)}{I_{L,PR(pk)}} \right) - t_1 - t_2 \\ t_4 = \frac{1}{2f} - t_1 - t_2 - t_3 \\ t_5 = \frac{1}{\omega} \cos^{-1} \left(\frac{\omega C_P V_o}{I_{L,PR(pk)}} - 1 \right) - \frac{1}{2f} \\ t_6 = \frac{1}{2f} - t_5 - t_7 \\ t_7 = \frac{1}{f} - \frac{1}{\omega} \cos^{-1} \left(1 - \frac{\omega C_P (V_{in,PR} - V_o)}{I_{L,PR(pk)}} \right) \end{array} \right. \quad (3.22)$$

According to equation (3.22), it can be observed that the time duration of phase 2, t_2 , can be used to control the power delivered to the output as well as the output voltage, which matches the feedback control method in [74] where t_2 is used to achieve voltage regulation.

To have an accurate time duration calculation, the operation frequency, ω , in equation (3.22) must be known. However, due to the variable frequency operation of the PR-based converter, the actual operating frequency varies between the resonant frequency (f_r) and the anti-resonant frequency (f_{ar}), complicating the determination of an exact operating frequency beforehand. While a model for predicting the operating frequency has been reported in [75], it is not analytically solvable. Here, given that a PZT PR with a high-quality factor (ranging from 600-2000 [67]) is typically employed and the operating frequency approaches the PR resonant frequency, f_r , as output power level or losses increase, a simple and quick approximation could be made by putting f_r into equation (3.22) for early-stage analysis. It is worth noting that this assumption is made based on a good electro-mechanical coupling factor and quality factor of the

piezoelectric devices, which allows the f_r and f_{ar} to be close, and as a result, the frequency variation does not span across a large frequency range. The quality factor, Q , is defined as $\sqrt{L/C}/R$.

3.3.2.4 Loss Analysis and System Efficiency

Once the value of $I_{L,PR(pk)}$ and the time duration of each phase have been calculated, the losses of the converter can be determined accordingly. The losses in the FSPPR converter can be divided into three main categories: 1) PR losses, 2) switching losses, and 3) conduction losses. Here, switching losses are calculated from the hard-charging of the lumped output capacitance, C_{loss} , of each power switch. Note that the ESR losses of capacitors and driving losses, $P_{dri} = Q_g V_{gs} f_{sw}$, of power MOSFETs are excluded in this work.

The PR losses contain dielectric, piezoelectric, and elastic losses; however, since the dielectric and piezoelectric losses are typically much smaller than elastic losses, these two types of losses can be ignored [68]. The elastic losses are the mechanical motion losses, represented by the mechanical resistor, R , in the BVD model. Therefore, the PR losses are given by:

$$P_{loss,PR} = \frac{1}{2} I_{L,PR(pk)}^2 R \quad (3.23)$$

The switching losses occur only in switches S1-S4 of the SC network since the remaining switches achieve ZVS in steady-state operation. Here, a simplified loss estimation is used, as shown in equation 24, where $V_{ds(n)}$ represents the drain-to-source voltage in switch n (S1-S4), and C_{loss} is the lumped output capacitance at the drain-to-source nodes, which is a function of drain-to-source voltage. More accurate switching loss calculations can be found in [76].

$$P_{loss,SW} \approx C_{loss} V_{ds(n)}^2 f_{sw} \quad (3.24)$$

The conduction losses occur during the PR-connected and PR-shortcd states, specifically in phases 2, 4, and 6, as depicted in Figure 3.3. There are no conduction losses in phases 1, 3, 5, and 7 due to the internal circulation of the PR in the opened state. Assuming ideal operation conditions where the on/off timing of S1-S7 perfectly matches, and the on-resistance of switch n is consistent ($R_{on(n)}$), the total conduction losses and losses of each switch can be expressed as equations (3.25) and (3.26), respectively. Here, n represents the label of the switch (S1-S7), and the root-mean-square (RMS) current of each switch is given by equation (3.27), where $I_{rms,ph(k)}$ denotes the RMS current of each phase, k , (phases 2, 4, and 6).

$$P_{loss,cond} = \sum_{n=1}^7 P_{loss,cond(n)} \quad (3.25)$$

$$P_{loss,cond(n)} = I_{rms(n)}^2 R_{on(n)} \quad (3.26)$$

$$I_{rms(n)} = \begin{cases} I_{rms,ph2}/\sqrt{2}, & 1 \leq n \leq 4 \\ \sqrt{I_{rms,ph4}^2 + I_{rms,ph6}^2}, & n = 5 \\ \sqrt{I_{rms,ph2}^2 + I_{rms,ph4}^2}, & n = 6 \\ I_{rms,ph6}, & n = 7 \end{cases} \quad (3.27)$$

where

$$I_{rms,ph(k)} = \begin{cases} \sqrt{\frac{1}{T_{sw}} \int_0^{t_2} i_{L,PR}^2(t + t_1) dt}, & k = 2 \\ \sqrt{\frac{1}{T_{sw}} \int_0^{t_4} i_{L,PR}^2\left(t + \sum_{i=1}^3 t_i\right) dt}, & k = 4 \\ \sqrt{\frac{1}{T_{sw}} \int_0^{t_5} i_{L,PR}^2\left(t + \sum_{i=1}^5 t_i\right) dt}, & k = 6 \end{cases}$$

Finally, the system efficiency can be built based on the abovementioned losses, as shown in equation (3.28).

$$\eta = \frac{P_o}{P_o + P_{loss,PR} + P_{loss,SW} + P_{loss,Cond}} \quad (3.28)$$

3.3.2.5 Mathematical Model Verification

This section focuses on verifying and comparing the mathematical models proposed above with MATLAB SIMULINK simulations. Then, the proposed model is used for the efficiency comparison of the FSPPR and baseline PR-based converter in the following section. It should be noted that the parameters employed in both the calculation and simulation here are identical to the final implementation value, as detailed in Table 3.4.

Table 3.4 Simulation, calculation, and experiment parameters and parts

Parts/Parameters	Values	Implementation
Switches (S1-S7)	80V, 10A, 20mΩ	EPC2214
S6,7 parallel diode	40V, 2A	PMEG4020EP
Gate driver	Isolated, 2.3A	ADUM4120
Digital Controller	150MHz	TMS320F28335
Input voltage range V_{in}	36-48 V	-
Output voltage range V_o	4-10 V	-
Output current range I_o	0.05-0.3 A	-
flying capacitor C_1	4.7 μF	MLCC (0805)
Resonant frequency f_r	≈113 kHz	Piezo resonator
Anti-resonant frequency f_r	≈129 kHz	Piezo resonator
piezo-static capacitor C_p	13.96 nF	Piezo resonator
Mechanical capacitor C	4.2 nF	Piezo resonator
Mechanical Inductor L	468.78 μH	Piezo resonator
Mechanical resistor R	0.48 Ω	Piezo resonator
Quality factor Q	696	Piezo resonator

To verify the time duration model equation (3.22), the operation waveforms are calculated and simulated, as depicted in Figure 3.5. Here, the calculated waveforms are built based on the time duration model, where the time durations are individually calculated and applied to the modulation laws for the waveform representation. In addition, the calculation results based on both the accurate and approximated frequencies are presented in Figure 3.5. Here the accurate frequency is the same as the operation frequency in the simulation, f_{sim} , whereas the approximated frequency is the resonant frequency, f_r by assuming that the operation is in the vicinity of f_r . The analysis reveals that when $f_{sw} = f_{sim}$, the calculated waveforms are well-matched with the simulations, and when $f_{sw} = f_r$, there is a small phase shift over time due to the small frequency discrepancy. Nonetheless, the amplitudes of $I_{L,PR}$ in both cases closely approximate the simulation results. Therefore, the time duration model, equation (3.22), demonstrates its utility in estimating PR behavior during preliminary assessments.

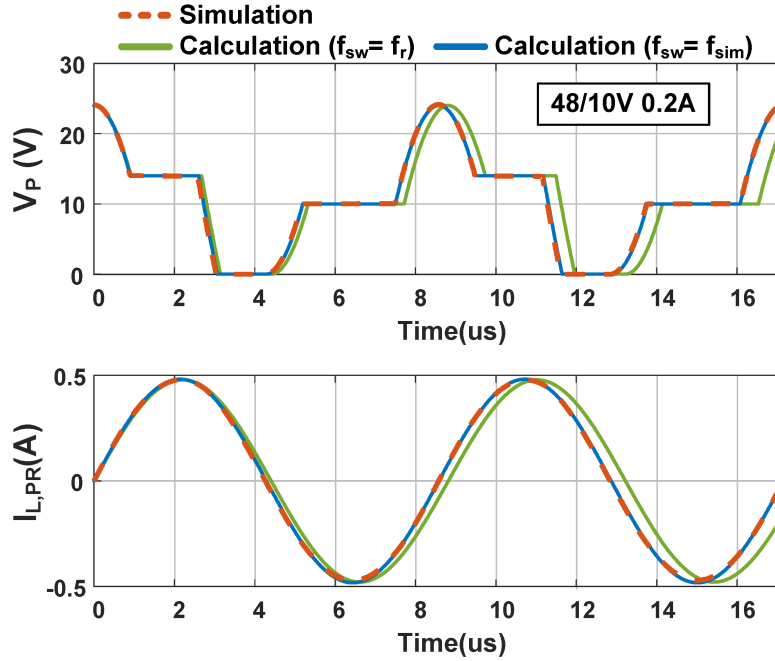


Figure 3.5 Comparison of operational waveforms in simulation and calculation.

Following the verification of equation (3.22), the system loss model, particularly the root-mean-square current for each switch derived from equation (3.22), can be further verified. The comparison of simulation and calculation results at a 48V-10V, 0.2A output scenario is shown in Table 3.5, where the frequency approximation ($f_{sw} \approx f_r$) is applied to the calculation results. This table reveals an excellent agreement between calculated and simulated results, with errors under 1%, even when the switch frequency approximation is considered. The difference in efficiencies rises from the omission of node capacitance that is being charged and discharged during the opened PR states, diode conduction loss, and frequency approximation in the calculation. It is important to note that values in the table are rounded to the nearest first and second decimal places, and the error is computed using exact values.

Table 3.5 System efficiency model verification of FSPPR converter at 48/10V, 0.2A

Parameters	Calculation (approx.)	Simulation	Error (%)
$I_{rms}(S1,3)$	137.0 mA	136.5 mA	0.32
$I_{rms}(S2,4)$	137.0 mA	136.4 mA	0.41
$I_{rms}(S5)$	235.4 mA	236.2 mA	-0.36
$I_{rms}(S6)$	210.9 mA	210.9 mA	-0.01
$I_{rms}(S7)$	220.1 mA	220.2 mA	-0.01
$I_{L,PR(pk)}$	476.4 mA	480.6 mA	-0.88
Efficiency	96.17%	96.21%	-0.04

3.3.2.6 Topological Comparison

This analysis compares the FSPPR with its precursor, the baseline PR-based converter. The voltage conversion ratio (VCR) range, PR utilization factor, and the peak PR resonant current are elaborated in Table 3.6. The variables $V_{in,PR}$ and $V_{o,PR}$ denote the equivalent PR input and output

voltages during operation, while V_{in} and V_o denote that input and output voltages of the entire converter, and V_{pp} corresponds to the peak swing over the PR.

Table 3.6 Comparison of Baseline PR-based converter and FSPPR converter

	Baseline PR	FSPPR
Voltage conversion ratio (VCR)	$0 \leq VCR \leq 0.5$	$0 \leq VCR \leq 0.25$
PR charge utilization (K)	$\frac{V_{in,PR}}{2(V_{in,PR} - V_{o,PR})}$	
Optimal PR charge utilization (K_{opt})	$K = 1$ ($VCR = 0.5$)	$K = 1$ ($VCR = 0.25$)
Peak PR resonant current ($I_{L,PR(pk)}$)	$\pi \left(\frac{P_o}{2KV_{o,PR}} + f_{sw}C_P V_{pp} \right)$	
$V_{in,PR}$	V_{in}	$V_{in}/2$
$V_{o,PR}$	V_o	V_o
$V_{o,PR}$	V_{in}	$V_{in}/2$

The PR utilization factor comparison is then plotted, as illustrated in Figure 3.6(a), based on Table 3.6. The FSPPR converter exhibits an enhanced utilization of the piezoelectric resonator throughout its operable VCR range (low VCRs), attributed to a reduced input voltage applied to the PR, implying potentially enhanced efficiencies in high step-down applications. That is, due to the SC conversion in the FSPPR converter, $V_{in,PR}$ is reduced and, as a result, the equivalent VCR of the PR itself, VCR_{PR} , is closer to 0.5, identified as its optimal efficiency point [29]. However, this is a trade-off employed for overall conversion ratios restricted to below 0.25. In other words, the baseline PR-based converter is capable of a wider operation range, and thereby the baseline PR-based converter could be used for a VCR range between 0.5 and 0.25 while the FSPPR is more beneficial at VCRs below 0.25.

Upon comparing the VCR and K with the verification of the system loss and efficiency models, Figure 3.6(b) shows the efficiency comparison of the FSPPR and baseline PR-based converters at a 48V input voltage with different output voltages and currents, where the efficiencies are calculated and simulated with the parameters shown in Table 3.4. It can be observed that, in all scenarios, the FSPPR converter outperforms the baseline PR-based converter with increasing efficiency advantages as the output current/power increases.

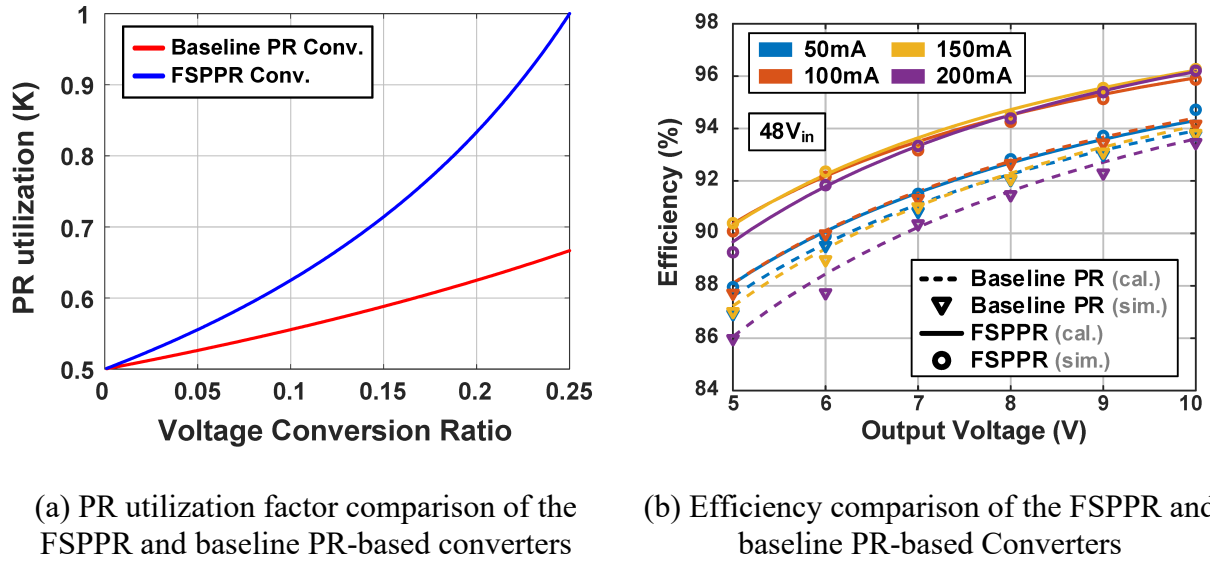


Figure 3.6 Performance comparison of the FSPPR and baseline PR-based converters.

Figure 3.7 shows the loss breakdowns of the baseline PR-based converter and the FSPPR converter at 48/10V input/output voltage with different output conditions in Figure 3.6(b). It can be seen that there is no switching loss presented in the baseline PR-based converter, while the FSPPR converter shows switching loss due to the SC network. Despite this, the FSPPR converter still presents a lower overall loss because the equivalent voltage conversion ratio of the PR stage in the FSPPR converter is much closer to its optimal operating point of 0.5; consequently, the PR current ($I_{L,PR}$) and PR losses are reduced. The benefit of the SC network becomes more advantageous as the output current/power goes to a higher level. However, it should be noted that

under extremely light load conditions, when switching losses start to dominate the overall losses, the baseline PR-based converter may exhibit higher efficiency than the FSPPR converter.

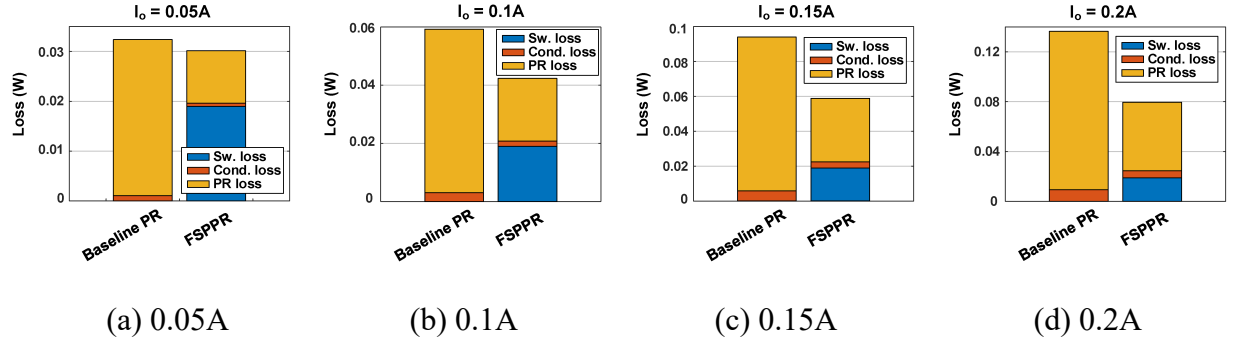


Figure 3.7 Loss breakdown comparison at 48/10V condition.

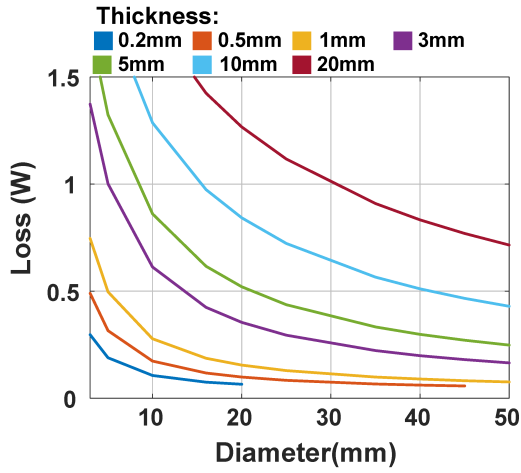
3.3.3 Piezoelectric Resonator Sizing Optimization

As analyzed in Chapter 3.2, maximized radius and minimized thickness can result in minimal R ; however, the capacitor, C_p , increases as well leading to higher $I_{L,PR(pk)}$ due to extra charges required for ZVS (Q_{ZVS}). Thus, there must exist an optimal sizing for a given operation condition and material. More optimizations will be discussed in Chapter 5.

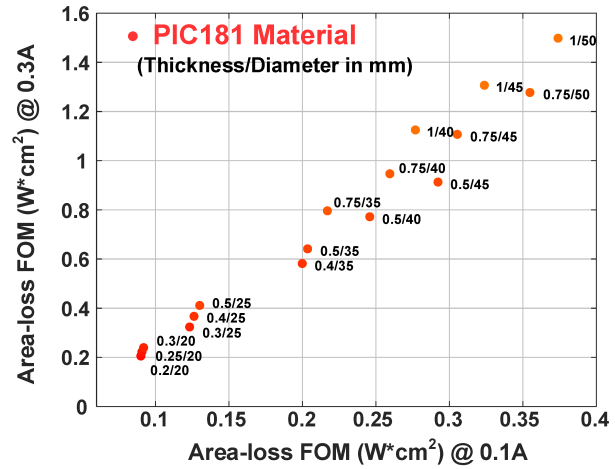
Figure 3.8(a) shows the total loss of the FSPPR converter with various PR sizes using the PIC181 material at 48/10V, 0.3A, where the available PR sizes are obtained from the standard dimension table provided by PI ceramic. It can be found that, at a given thickness, a larger diameter leads to a lower overall loss; conversely, at a given diameter, a larger thickness results in a higher overall loss. This observation perfectly aligns with the physical model discussion above, indicating that minimizing losses requires minimizing the thickness and maximizing the diameter.

It should be noted that the PR size obtained from loss minimization is not always area/volume favorable as the loss reduction often saturates beyond a certain point with an increase in size. For instance, in Figure 3.8(a), the loss of (0.5/45)mm PR size is slightly smaller than that

of the (0.2/20)mm PR size, with losses of 57mW and 65mW, respectively. However, the area is significantly increased with areas of 0.16 cm² and 0.03 cm², respectively. Therefore, an alternative optimization method should be employed when the area becomes a critical factor in PR selection. One commonly used figure of merit (FOM) is the areal-loss FOM, which is the product of losses and area, given by $FOM = loss \times Area$, with a minimal efficiency constraint. By minimizing the FOM with constraints, an optimal size can be found for the desired specification. It is important to note that apart from efficiency and area/volume considerations, there are also hard limitations to be taken into account, such as the maximum voltage limitation, where the safe operating area for PZT material typically does not exceed 1kV/mm, and the maximum current limitation, as described in [65].



(a) Overall FSPPR converter losses with different PR diameter and thickness size (PIC181 material).



(b) Area-loss FOM comparison of PIC181 material with different sizes.

Figure 3.8 PR sizing selection.

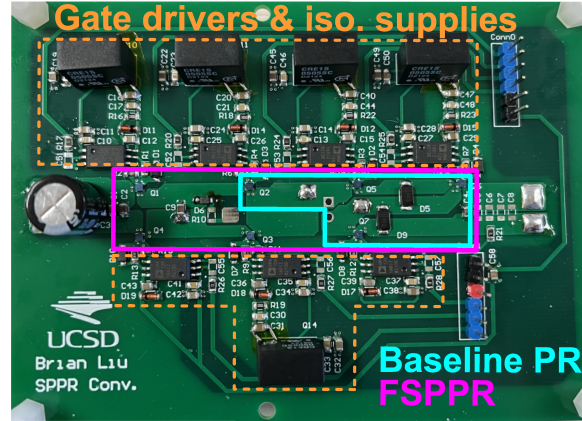
Figure 3.8(b) shows the area-loss FOM comparison for various available PIC181 PR sizes [67] at a 48/10 conversion ratio with 0.1A and 0.3A output in the x/y-axis, with an efficiency

constraint of 95%. It can be found that the size of (0.2/20)mm exhibits the most favorable area-loss performance, and hence, the size of (0.2/20)mm PR is adopted in this work.

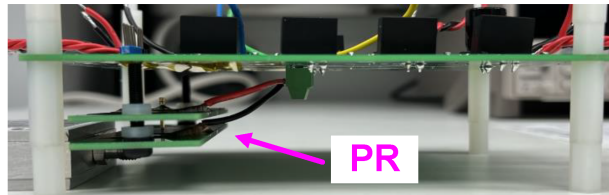
Aside from the material and sizing considerations, in practical design, thermal performance is critical for piezoelectric devices as the piezoelectric properties vary with temperature, potentially altering its behavior. However, due to the limited current density and power handling capabilities of the commercial off-the-shelf (COTS) PRs at present, which are not specifically designed for power applications, only a small amount of loss is dissipated in the PRs, given low output power, in this work. Thus, the thermal performance is not considered in this article. Nevertheless, when the COTS PRs are optimized for power electronic applications, which will involve higher output current and power in the future, the thermal behavior should be carefully considered.

3.3.4 Experiment Verification

A prototype of the FSPPR converter incorporating a piezoelectric resonator has been designed and built based on the aforementioned analysis and discussions and is shown in Figure 3.9. The prototype can function as either a FSPPR or baseline PR-based converter, specifically noted in Figure 3.9, enabling a fair performance comparison. The experimental parts and parameters are listed in Table 3.4. In the implementation, a disk-shaped, radial vibration mode PR made of PIC181 material with a thickness and diameter of (0.2/20)mm is adopted. Additionally, GaNFETs are applied to the prototype for their excellent switching/conducting characteristic, minimizing overall losses in the system. The prototype is digitally controlled by a DSP controller (TMS320F28335) operating in an open-loop configuration.

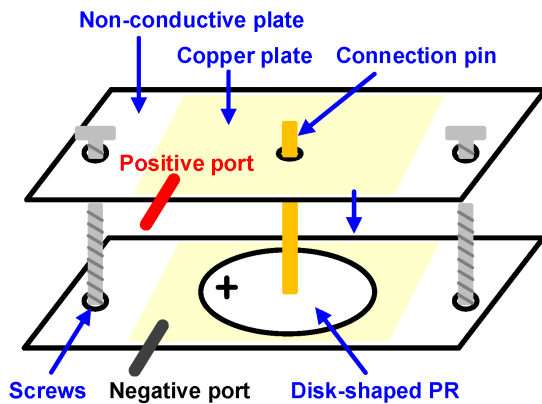


(a) Top view

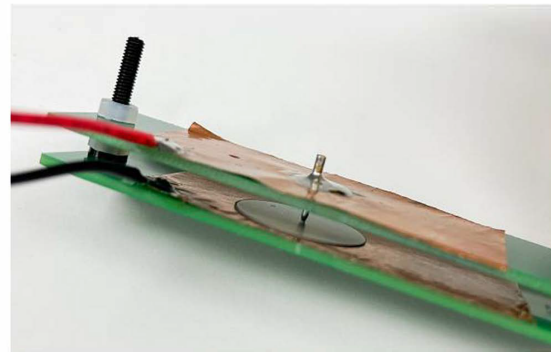


(b) Side view

Figure 3.9 Prototype of Frontside Series/Parallel Piezoelectric Resonator converter.



(a) 3D view



(b) Implementation

Figure 3.10 Sandwich mounting for piezoelectric resonators.

Due to the lack of a package and the power-electronics-optimized PRs. The mounting of PRs plays a vital role in determining the converter's overall efficiency. That is, improper mounting can result in significant efficiency degradation. Here, the sandwich-like mounting method,

illustrated in Figure 3.10(a), is applied to this prototype that involves placing the PR between two non-conductive plates, each equipped with a copper plate as a conductive surface. The positive electrode of the PR is connected via a connection pin, while the negative electrode is in direct contact with the copper plate. Screws on each side of the non-conductive plates allow for contact adjustment, ensuring unclamped contact for a clean response (minimizing the occurrence of spurious modes). Figure 3.10(b) provides an actual implementation using an FR4 PCB board as the non-conductive plate and golden micro pins as connection pins. The advantages of this sandwich mounting approach include non-destructive contact, flexibility, and protection against depolarization, aging, and damage caused by excessive heat and force during soldering and handling. Fine-tuning the PR position and screws allows for easy adjustment to the desired centered-pined and unclamped contact position, resulting in an ideal response. Figure 3.11 shows the measured impedance of the sandwich mount along with the BVD model fitting result, demonstrating a clean frequency response without spurious modes as well as a beautiful agreement between measurement and model fit results. It should be noted that mounting and packaging of PRs for use in DC-DC converters is an ongoing topic of research and development.

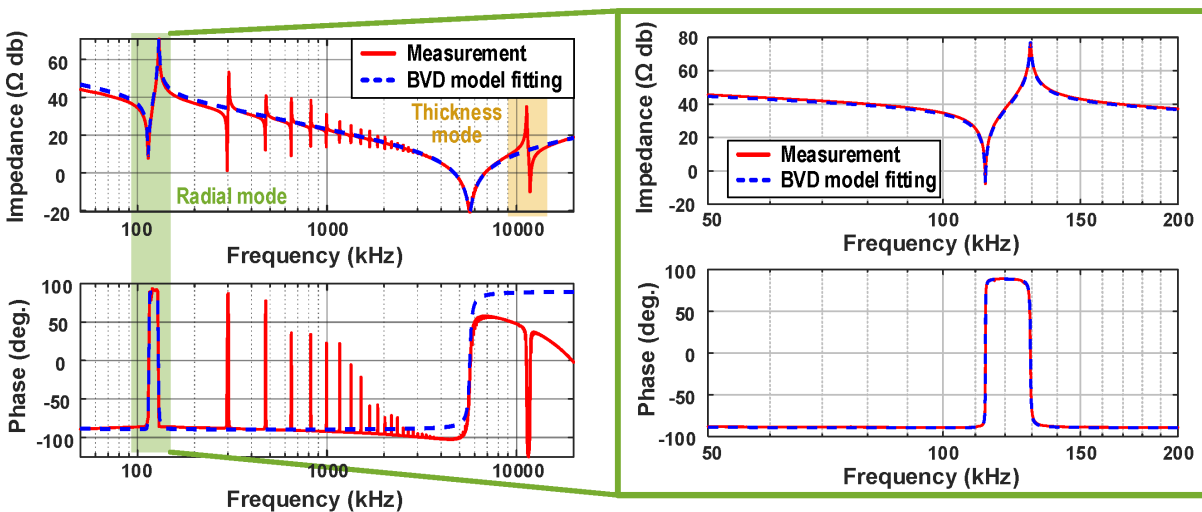
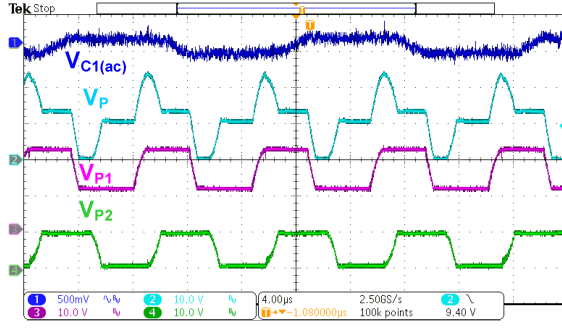
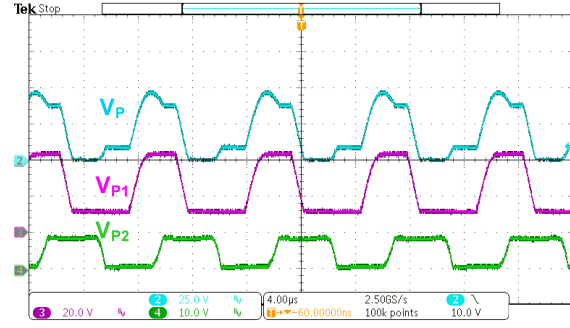


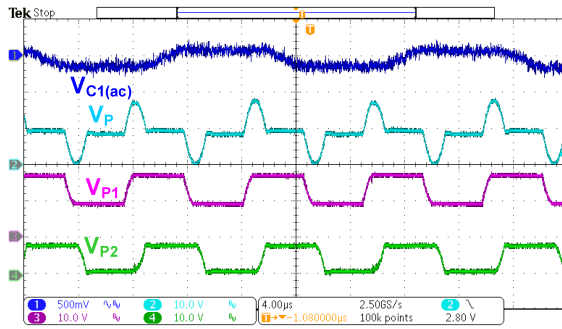
Figure 3.11 Piezoelectric resonator impedance model-fitting results.



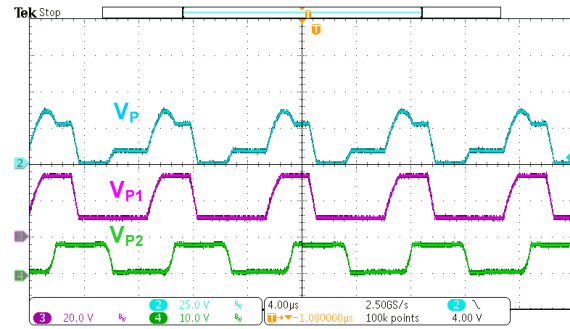
(a) 48/10V/0.25A FSPPR converter



(b) 48/10V/0.25A PR-based converter



(c) 36/8V/0.25A FSPPR Converter



(d) 36/8V/0.25A PR-based Converter

Figure 3.12 Steady-state waveforms of baseline PR-based and FSPPR Converters.

The steady-state waveforms of the baseline PR-based converter and FSPPR converter are shown in Figure 3.12. Figure 3.12(a) and Figure 3.12(b) depict the waveform comparison of FSPPR and baseline PR-based converters at a 48/10V conversion ratio, while Figure 3.12(c) and Figure 3.12(d) show the comparison at a 36/8V conversion ratio. Analysis of the waveforms reveals that a longer input-to-output connected state duration (t_2) and a shorter current circulating shorted state duration (t_4) are exhibited in the FSPPR converter than in the baseline PR-based converter, where the definitions of t_2 and t_4 are presented in Figure 3.4. This discrepancy suggests a higher utilization factor of the PR in the FSPPR converter, thereby implying the potential for higher efficiency. On the other hand, Figure 3.12(a) and (c) show the waveform comparison of the FSPPR converter at different input/output scenarios, which are 48/10V and 36/8V conversion ratio respectively. The V_{C1} waveforms in both cases present soft-charging/discharging of the flying

capacitor (C_1), eliminating capacitor hard-switching losses. Moreover, ZVS has been achieved in both baseline PR-based and FSPPR converters, except for S1-4, where minor switching noise presents at the rising edge of V_{p2} in Figure 3.12(a) and (c).

To evaluate the performance of the proposed topology and compare it with the baseline PR-based converter, multiple experiments are conducted with various operating points. Figure 13- Figure 17 show the comparisons of the baseline PR-based and FSPPR converters in terms of efficiency, input-output-connected state time duration, t_2 , and frequency variation with different input/output conditions. Here, the efficiency is defined as equation (3.28) in a similar way as [29], [30], [52]. Note that testing stops when the PR shows unstable behavior such as low-frequency oscillation and/or an output voltage drop over time. Based on the experimental stop points, the peak PR current, $I_{L,PR(pk)}$, is limited to around 0.8-1A

Figure 3.13 shows the efficiency comparison of the baseline PR-based and FSPPR converters at 48/10V and 36/8V conversion ratios. Here, the equivalent PR conversion ratio, VCR_{PR} , of the FSPPR converter is 0.42 and 0.44 at 48/10 and 36/8 input/output voltages, respectively, compared to 0.21 and 0.22 of the baseline PR-based converter at the same input/output voltage. Because of a higher VCR_{PR} , the FSPPR converter shows an enhanced performance to the baseline PR-based converter, where the peak efficiency is 95.27%, and the efficiency improvement is up to 14% at a 48/10 conversion ratio. The calculated efficiencies are also marked in the figure. As shown, compared to calculated efficiencies, the measurement results present differences in efficiency. The differences can be attributed to several factors: 1) the imperfect matching of turned-on duration in the synchronous rectifiers, S6 and S7. To prevent false action of the converter, the synchronous rectifiers are turned on/off a little bit later/earlier, compared to the ideal case, which introduces additional diode commute losses to the converter, and it becomes worse in baseline PR-

based converter cases due to a higher resonant current. 2) the in/out-of-band spurious mode excitation by the harmonics [30], [52], which is hypothesized to affect the baseline converter more strongly due to its higher resonant current limiting its ability to deliver higher output current at large conversion ratios; however, an accurate model is not currently available to predict this behavior. 3) The difference in small-signal and large-signal behaviors; here, the PR parameters are assumed to be constant but, in reality, they vary with deformation (amplitude of $I_{L,PR}$), temperature, aging, and other factors, leading to extra loss [25]. Collectively, these factors contribute to the observed deviation in measured efficiency from calculated values, particularly at higher power outputs [52] and lower PR conversion ratios [77], where $I_{L,PR}$ amplitude is more significant.

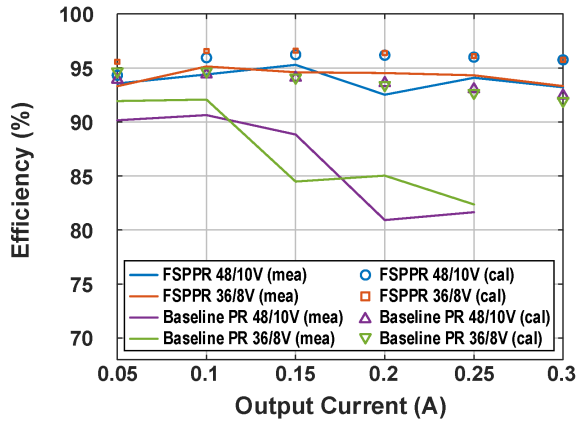


Figure 3.13 Efficiency comparison of the baseline PR-based and FSPPR converters with calculation results

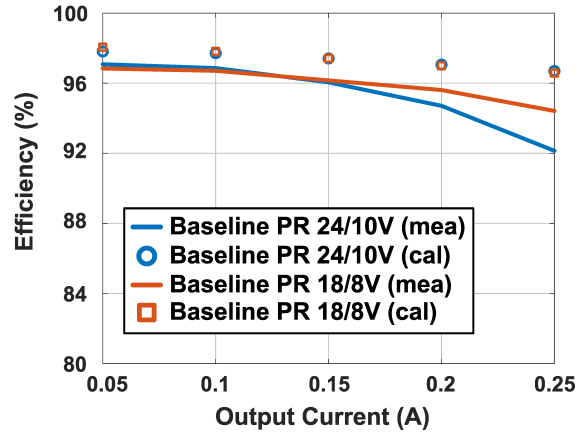


Figure 3.14 Baseline PR-based converter efficiency at the vicinity of its optimal point: $VCR \approx 0.5$.

To ensure that the baseline PR-based converter is optimally designed for comparison, the efficiencies at 24/10V ($\approx 0.42VCR$) and 18/8V ($\approx 0.44VCR$) are measured and compared with calculated results, as illustrated in Figure 3.14. The measured efficiencies closely align with the calculated projections, confirming the optimal operations. Also, consistent with previous

discussions, the discrepancy in efficiency rises with an increase in output power[52], where $I_{L,PR}$ is increased as well.

Figure 3.15 shows the input-output-connected time, t_2 , comparison of the baseline PR-based and FSPPR converters. The input-output-connected state is phase 2 in Figure 3.3(a), where the PR is connected to input and output at the same time, in which the input delivers power to the output through PR while PR stores energy in itself. As analyzed in equation (3.9) and [74], the duration of t_2 is used for the voltage regulation, and therefore, Figure 3.15 shows that with an increase of the output current, which is equivalent to an increase of output power, t_2 increases accordingly to deliver more energy requested by the output. Besides, a portion of t_2 increase is to compensate for the voltage drop due to losses, as illustrated in equation (3.16). For example, as shown in Figure 3.13, it can be seen that the efficiency of the baseline PR-based converter at a 48/10V conversion ratio shows an efficiency drop at the output current of 0.2A, and correspondingly, t_2 shows a sudden increase, as shown in Figure 3.15, to maintain output regulation. The same trend is also shown in the baseline PR-based converter at a 36/8V conversion ratio. The calculated t_2 is also marked in Figure 3.15. The measurement results follow the same trend with calculation but with differences at some points. The discrepancy could result from many factors; however, the main factors are: 1) the open-loop test, where the timings are manually tuned, 2) frequency approximation in the calculation, where the actual operation frequency is not equal to the approximated frequency.

Figure 3.16 shows the frequency variation comparison of the baseline PR-based and FSPPR converters at different output currents. It can be observed that the operation frequency ranges between resonant and anti-resonant frequency, f_r and f_{ar} , and decreases with an increase

in output current/power due to the shorter opened states and longer connected states in both the baseline PR-based and FSPPR converters.

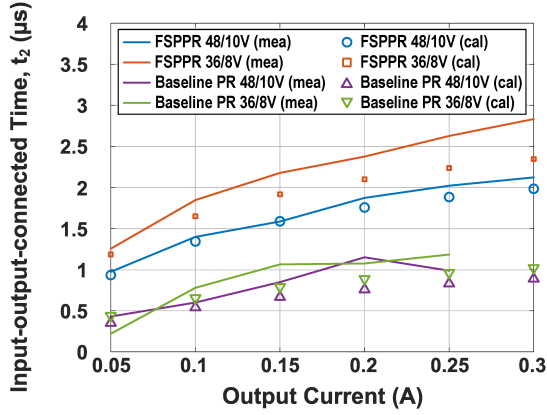


Figure 3.15 Input-output-connected time comparison of the baseline PR-based and FSPPR converters with calculation results.

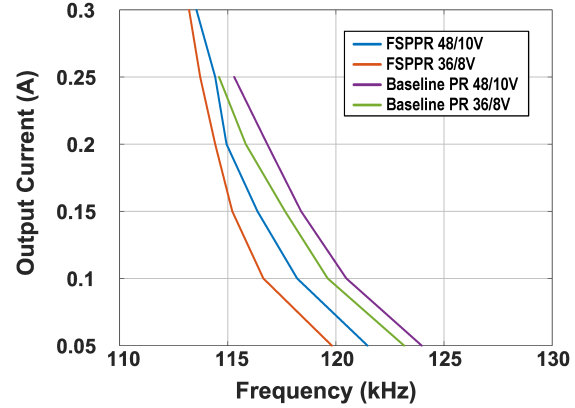
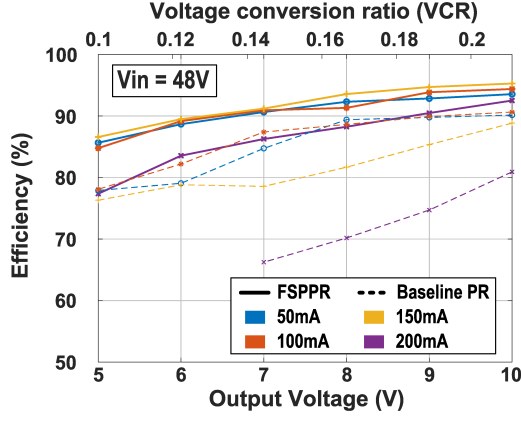


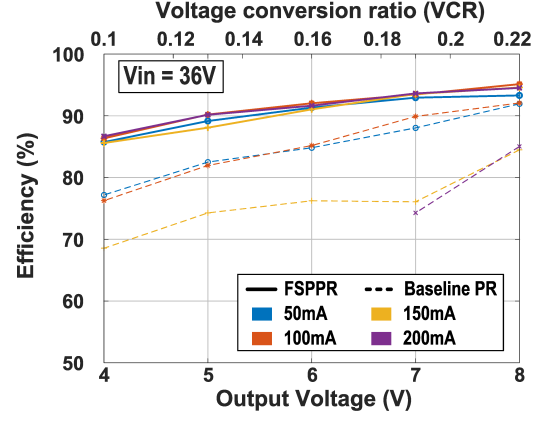
Figure 3.16 Frequency variation comparison of the baseline PR-based and FSPPR converters.

Figure 3.17(a) and (b) show the efficiencies of the FSPPR converter at the 48V and 36V input voltage with different output voltages and currents. The efficiency curves show a similar trend as in Figure 3.13, where, at a given output current, the efficiency decreases with a decrease in conversion ratio.

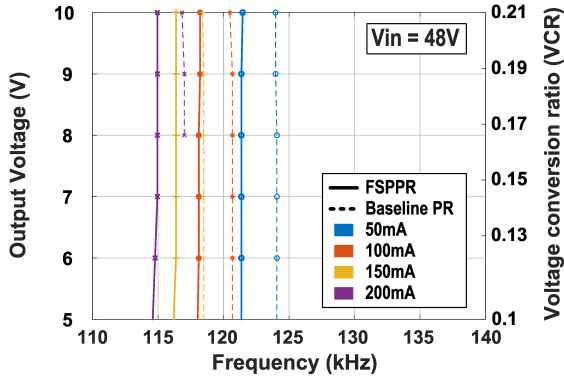
Figure 3.17(c), and (d) show the frequency variation of the FSPPR converter at 48V and 36V input voltage with different output voltages. The operating frequency is fairly constant at a given output current regardless of the output voltage level. Although fairly constant operating frequency results are presented, the t_2 of the FSPPR converter at the input voltage of 48V and 36V with different output is not constant, as shown in Figure 3.17(e), and (f). This variation arises from differences in losses, conversion ratios, and PR utilization factors. As observed, t_2 increases with an increase in the VCR or output current, agreeing with the trend observed in Chapter 3.3.2.



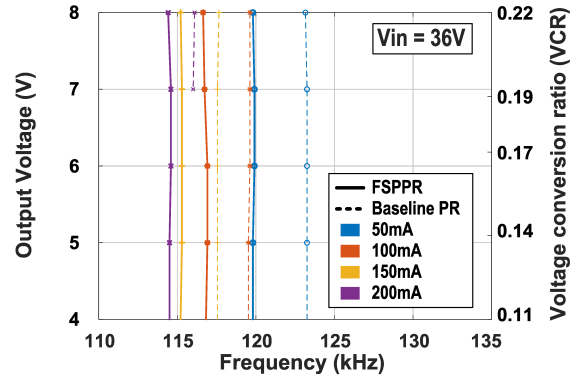
(a) Efficiencies at $48V_{in}$



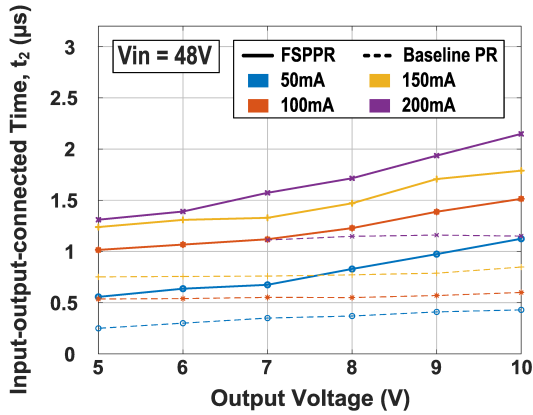
(b) Efficiencies at $36V_{in}$



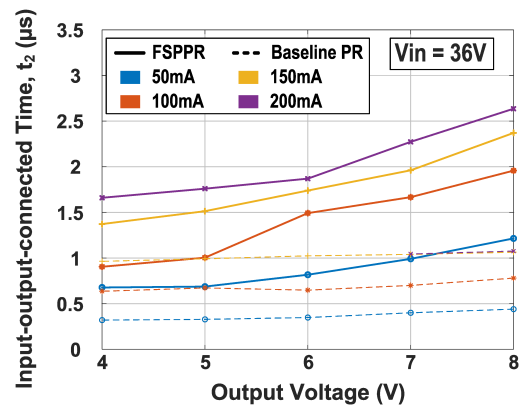
(c) Frequency variation at $48V_{in}$



(d) Frequency variation at $36V_{in}$



(e) Input-output-connected time at $48V_{in}$



(f) Input-output-connected time at $36V_{in}$

Figure 3.17 Performance comparison of FSPPR and Baseline PR-based converters at various

VCR scenarios.

Table 3.7 highlights the advantages of the FSPPR converter relative to the co-designed baseline PR-based converter. Despite the FSPPR featuring additional switches and a flying capacitor, its overall power density, denoted as $P_{o(max)}/(\text{Total footprints})$, surpasses that of the baseline PR-based at low VCR (high-step-down ratio) scenarios. This is attributed to the hybrid switched capacitor (SC), which enhanced the PR utilization factor in the FSPPR converter. Consequently, this enhancement leads to a reduction in $I_{L,PR(pk)}$, thereby facilitating a higher output capacity while maintaining a compact footprint. The FSPPR thus achieves better peak efficiency and power density.

Table 3.7 Comparison table

	Baseline PR [29]	This Work (FSPPR)
Active footprint	5.8 mm^3 (4x GaN)	10.2 mm^3 (7x GaN)
Passive footprint	62.8 mm^3 (PR only)	65.2 mm^3 (PR, 1x 0805 Cap.)
$P_{o(max)}$	2.5 W	3 W
Power density	36.4 W/cm^3	39.8 W/cm^3
Peak efficiency	92.08%	95.27%

3.4 Backside Series/Parallel Piezoelectric-Resonator-Based DC-DC Converter

3.4.1 Introduction to Backside Series/Parallel Piezoelectric-Resonator-Based DC-DC Converter

As introduced in Chapter 3.1, the state-of-the-art step-down PR-based converters, exhibit exponential efficiency declination as the VCR decreases. To address the efficiency issue, various hybrid PR-based converters have been reported[70], [71] in a similar manner to hybrid inductive buck converters[55]-[60]. Both the Frontside Series/Parallel PR-based converter (FSPPR), Figure 3.18(a), and Merged Switched Capacitor PR-based converter (MSCPR), Figure 3.18(b), leverage the advantages of switched capacitors to reduce the equivalent input voltage of PRs, thereby minimizing the PR resonant current and improving efficiency at low VCRs. However, such converters position the PR on the output side (low-voltage/high-current side), requiring the PR to process a large output current. As a result, significant PR vibration losses (I^2R losses) arise, constraining the achievable efficiency and output capability, which is limited by the maximum allowable current of PRs.

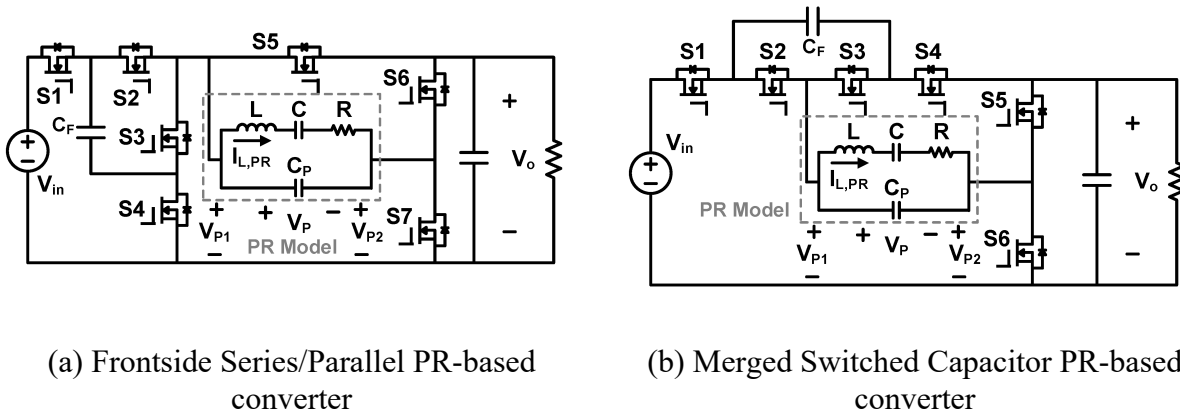
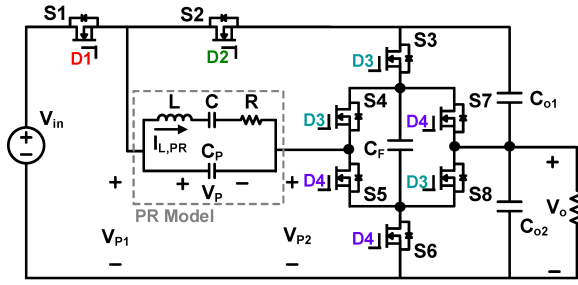


Figure 3.18 Hybrid PR-based converters.

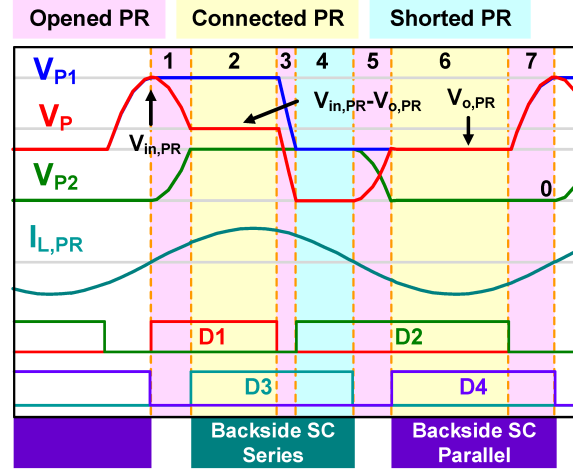
In response, a merged Backside Series/Parallel PR-based (BSPPR) converter. Unlike prior art, the proposed approach employs a switched capacitor network located on the backside (i.e., output side) of the converter, which thus places the PR on the high-voltage/low-current side. This configuration effectively reduces the PR resonant current as well as PR vibration losses, and shifts the optimal operating point to a lower VCR (from 0.5 to 0.25) while preserving all benefits of the baseline PR converter, such as ZVS for all switches. Furthermore, owing to the hybrid converter concept, similar to a hybrid Buck converter, the operation principle remains unchanged from the baseline PR converter, allowing for the direct application of the control logistics reported in [69], and [70]. In contrast, the FSPPR converter achieves ZVS on specific switches, and the MSCPR converter alters the operation principle with a more complex driving strategy.

3.4.2 Circuit Diagram and Operation

The Backside Series/Parallel PR-based (BSPPR) converter is shown in Figure 3.19(a). Following the PR-based stage, a SC network is merged into the baseline PR converter, incorporating the output half-bridge structure of the baseline PR converter, switches S3-6, and additional switches S7,8 along with a flying capacitor, C_F . This configuration forms a 2:1 series/parallel SC network to the output, where C_F is controlled by driving signals D3 and D4 that position it either in series or parallel with the output. Notably, due to its series/parallel arrangement with the output, C_F is inherently self-balanced to the output voltage, V_o , effectively reducing the control complexity. Furthermore, this configuration allows the PR to operate at the high voltage/low current side for a given output power level, thereby reducing the PR resonant current and I^2R losses within the PR. Lastly, as C_F is balanced to V_o , ZVS turn-on for S7 and S8 is enabled, further reducing the overall losses.



(a) Circuit Diagram



(b) Operation waveforms

Figure 3.19 Backside Series/Parallel PR-based (BSPPR) converter.

The operation waveforms and phases are illustrated in Figure 19(b) and 20 where $V_{in,PR}$ and $V_{o,PR}$ represent the equivalent input/output voltage for PR stage. Here, $V_{in,PR}$ is the input voltage, V_{in} while $V_{o,PR}$ is twice the output voltage, $2V_o$ in the BSPPR converter. There are 7 individual phases in a cycle, where the PR can be arranged in one of three states: (1) opened PR, (2) connected PR, and (3) shorted PR states.

At the beginning, no current loop is formed by the switches in phase 1, leading to an open PR state. In this phase, the inductive PR current, $I_{L,PR}$, discharges C_P , where V_{P2} is correspondingly increased. As V_{P2} equals $V_{o,PR}$, the body diodes of S3 and S4 become forward-biased. This allows ZVS turn-on of S3, S4, and S8, entering phase 2 and making C_F in series with the load. During phase 2, the PR is linked to both the input and output, transferring energy to the output while storing energy within the PR. The phase ends as S1 deactivates, transitioning to phase 3, an open PR state, where $I_{L,PR}$ discharges C_P until $V_{P1} = V_{o,PR}$, assuring ZVS turn-on for S2. Then, phase 4 initiates, creating a shorted loop to ensure the current continuity and this free-wheeling phase terminates when the polarity of $I_{L,PR}$ reverses, after which switches S3, S4, and S8

are opened. This puts the PR back to an open PR state, phase 5, where $I_{L,PR}$ charges C_P , discharging V_{P2} until it becomes zero where body diodes of S5 and S6 are conducted with ZVS turn-on enabled for S5-S7. This consequently puts the C_F in parallel with the load, and the PR is connected to the output and ground, entering the connected PR state, where the PR starts to release energy to the load. Phase 7 begins as S2 turns off, opening the PR. In this phase, $I_{L,PR}$ charges C_P until V_{P1} reaches $V_{in,PR}$, ensuring ZVS turn-on for S1.

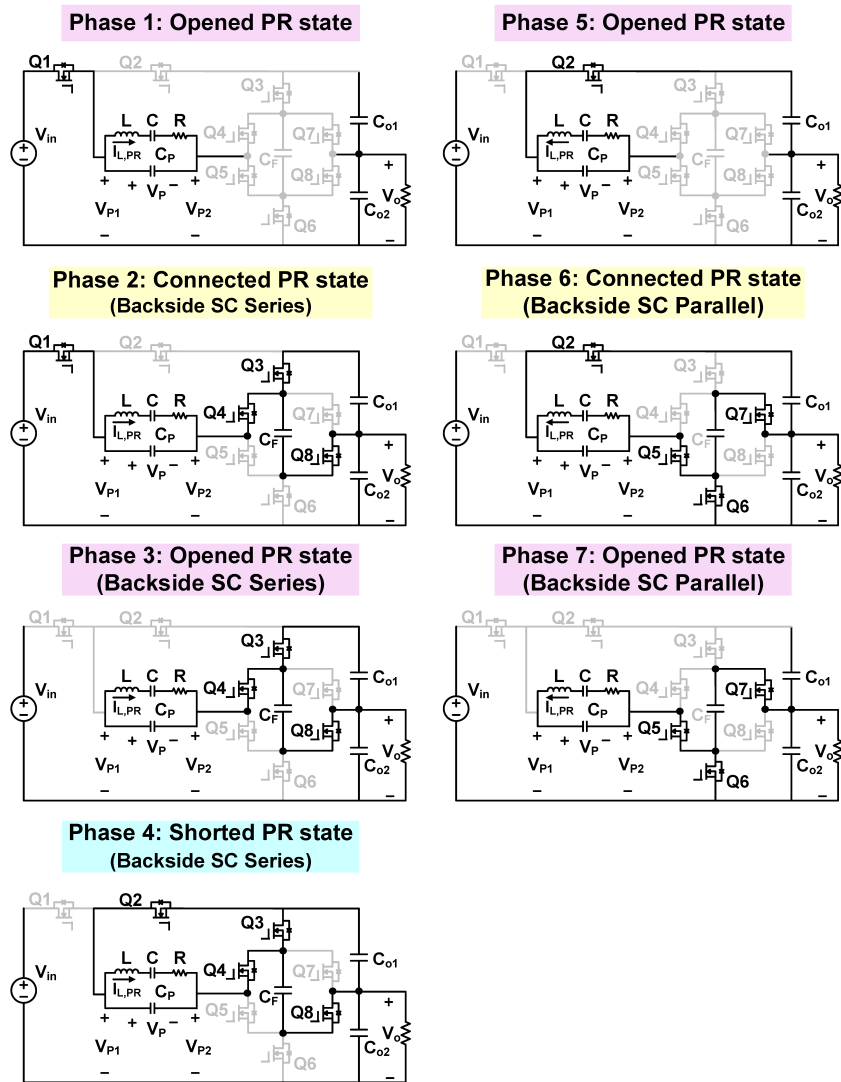


Figure 3.20 Operation phases of Backside Series/Parallel PR-based (BSPPR) converter

3.4.3 Steady-State Analysis: PR Operation

3.4.3.1 Voltage Conversion Ratio

As illustrated in Figure 3.19(b), the PR must follow the conversion of charge (Coc) and conversion of energy (CoE) principles in the steady state to keep charge and energy balanced in a similar way as the other PR-based converters. Hence, the CoC of PR mechanical capacitor, C , and junction capacitor, C_p and be expressed as equations (3.29) and (3.30) where q_n is the charge in phase n . Here, $V_{in,PR}$ and $V_{o,PR}$ are the equivalent input/output voltage viewed by the PR. In the BSPPR converter, $V_{in,PR}$ equals V_{in} and $V_{o,PR}$ equals $2V_o$.

$$q_1 + q_2 + q_3 + q_4 + q_5 + q_6 + q_7 = 0 \quad (3.29)$$

$$q_1 + q_3 + q_5 + q_7 = 0 \quad (3.30)$$

On the other hand, the CoE of the PR can be written as:

$$\begin{aligned} E_2 + E_4 + E_6 &= V_2 q_2 + V_4 q_4 + V_6 q_6 \\ &= (V_{in,PR} - V_{o,PR})q_2 + (0)q_4 + (V_{o,PR})q_6 = 0 \end{aligned} \quad (3.31)$$

By substituting equations (3.29) and (3.30) into equation (3.31) the voltage conversion ratio can be found as:

$$0 \leq \frac{V_o}{V_{in}} = \frac{1}{2} \frac{q_2}{2q_2 + q_4} \leq \frac{1}{4} \quad (3.32)$$

According to equation (3.32), it can be found that the VCR is regulated by the ratio of phases 2 (connected state) and 4 (shorted state), which can also be translated into the ratio of the input-connected time (phase 2) and the circulating time (phase 4). Therefore, an extended phase 2 interval implies a prolonged input-connected time leading to an increased VCR, and conversely, a shortened phase 2 interval leads to a reduced VCR.

3.4.3.2 PR Charge Transfer Utilization

The PR utilization factor is defined by the charge transfer utilization as a ratio of the charges delivered to the output, Q_{out} , to the total connected/shorted state charges including charges delivered to the output, Q_{out} , and the charges circulating inside the circuit in the shorted state, Q_{cir} [29]. Thus, the PR utilization factor can be written as:

$$K = \frac{Q_{out}}{Q_{out} + Q_{cir}} = \frac{|q_2| + |q_6|}{|q_2| + |q_4| + |q_6|} \quad (3.33)$$

By inserting equations (3.29), (3.30) and (3.31) into equation (33), K is expressed as

$$0.5 \leq K = \frac{V_{in}}{2(V_{in} - 2V_o)} \leq 1 \quad (3.34)$$

Based on equations (3.32) and (3.34), it can be observed that the BSPPR converter reaches its maximum K of 1 at 0.25 VCR; on the other hand, the baseline PR converter presents a K of 0.67 at the same conversion ratio indicating a higher portion of circulating interval in the baseline PR converter, and consequently, a lower efficiency.

3.4.3.3 PR Resonant Current Amplitude

The amplitude of PR resonant current, $I_{L,PR(pk)}$, can be found by the charges in connected and shorted states, and charges used to achieve ZVS as defined in [29], which can be derived as:

$$I_{L,PR(pk)} = \pi \left(\frac{P_o}{4KV_o} + f_{sw} C_P V_{in} \right) \quad (3.35)$$

The resonant current, $I_{L,PR(pk)}$, is directly correlated to the output current. However, in equation (3.35), the output-related term is written as $P_o/(4KV_o)$, contrasting with the baseline PR, FSPPR, and MSCPR converters as $P_o/(2KV_o)$. This implies that the PR resonant current in the BSPPR converter can be smaller than in others at the same output condition, leading to reduced

I^2R losses in the PR. The difference in resonant current arises because the PR is relocated to the input side (high voltage/low current side) rather than being directly linked to the output (low voltage/high current side).

3.4.4 Topology Comparisons

To better understand the performance of the proposed topology, three other PR-based converters: Baseline PR, FSPPR, and MSCPR are selected for performance comparison. Various aspects are discussed in this section including VCR, K , $I_{L,PR(PK)}$, and PR efficiency.

3.4.4.1 Voltage Conversion Ratio and PR Utilization Factor

The voltage conversion range for each PR-based converter is illustrated in Table 3.8. Here it can be seen that the hybrid PR-based converters exhibit slightly smaller voltage conversion ranges compared to the baseline PR converter, attributed to the presence of the hybrid SC mechanism.

Table 3.8 Voltage conversion range of different PR-based converters

Topology	VCR		
Baseline PR	0	$\leq \frac{V_o}{V_{in}} \leq$	1/2
FSPPR	0		1/4
BSPPR (This work)	0		1/4
MSCPR	0		1/3

Table 3.9 and Figure 3.21 show K and its relationship with VCR across various PR-based converters. As shown, the MSCPR, even with the introduction of hybrid conversion, exhibits the same utilization as the baseline PR converter due to its asymmetrical energy delivery between cycles[71]. In contrast, both the FSPPR and BSPPR converters show superior utilization under

specific input/output conditions compared to the baseline PR converter indicating more efficient usage of charges for power delivery and thereby enhancing efficiency.

Table 3.9 PR utilization factor, equivalent PR input/output voltage, and peak-to-peak PR voltage

Topology	K	$V_{in,PR}$	$V_{o,PR}$	$V_{p(p-p)}$
Baseline PR	$\frac{V_{in}}{2(V_{in} - V_o)}$	V_{in}	V_o	V_{in}
FSPPR	$\frac{V_{in}}{2(V_{in} - 2V_o)}$	$\frac{V_{in}}{2}$	V_o	$\frac{V_{in}}{2}$
BSPPR (This work)	$\frac{V_{in}}{2(V_{in} - 2V_o)}$	V_{in}	$2V_o$	V_{in}
MSCPR	$\frac{V_{in}}{2(V_{in} - V_o)}$	$\frac{V_{in} + V_o}{2}$	V_o	$\frac{V_{in} + V_o}{2}$

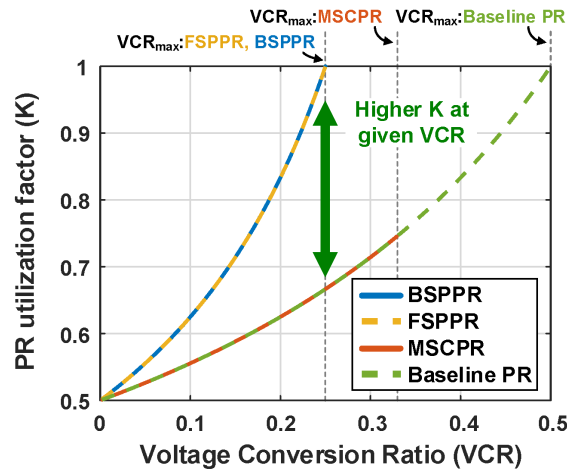


Figure 3.21 PR utilization factor versus VCR of different PR-based converter.

3.4.4.2 PR Resonant Current and PR Efficiency

The generalized PR resonant current amplitude can be expressed as equation (3.36), where the PR utilization factor, K , equivalent PR output voltage, $V_{o,PR}$, and peak-to-peak PR voltage, $V_{p(p-p)}$, are shown in Table 3.9.

$$I_{L,PR(pk)} = \pi \left(\frac{P_o}{2KV_{o,PR}} + f_{sw}C_P V_{p(p-p)} \right) \quad (3.36)$$

By investigating equation (3.36) along with Table 3.9, it can be found that, compared to the baseline converter, the hybrid PR-based converters generally have a smaller PR resonant current due to the merged SC:

- 1) The MSCPR converter lowers $I_{L,PR(pk)}$ by adjusting $V_{p(p-p)}$ from V_{in} to $(V_{in} + V_o)/2$.
- 2) The FSPPR reduces $I_{L,PR(pk)}$ by setting $V_{p(p-p)}$ to $V_{in}/2$ while increasing K value.
- 3) The BSPPR decreases $I_{L,PR(pk)}$ by increasing both $V_{o,PR}$ and K values.

The PR resonant current amplitudes at 48V input voltage and various outputs are depicted in Figure 3.22. It is noticeable that the hybrid PR-based converters have a smaller PR resonant current, aligning with the previous analysis. Particularly, both FSPPR and BSPPR demonstrate even smaller $I_{L,PR(pk)}$ than the MSCPR converter, owing to better K , which implies reduced circulating charges resulting in reduced $I_{L,PR(pk)}$.

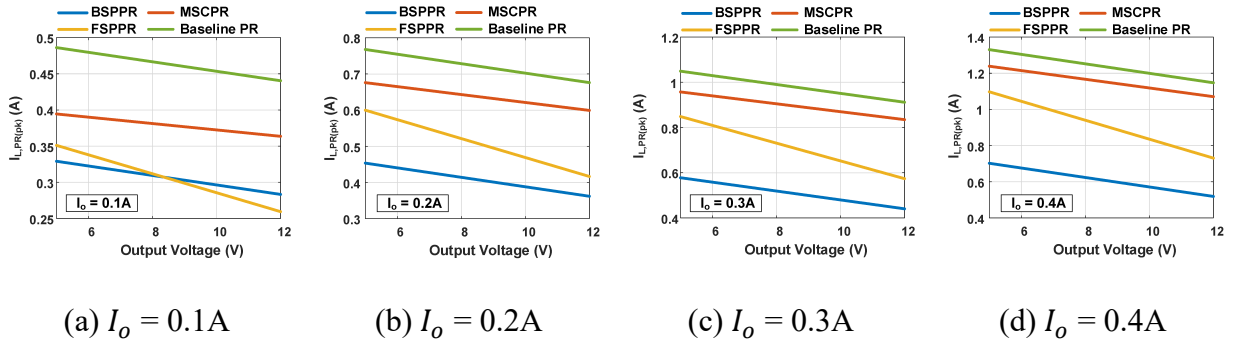


Figure 3.22 Amplitude of PR resonant current at $48V_{in}$.

In the comparison of the FSPPR and BSPPR converters, the amplitude difference arises from the different strategies adopted in $I_{L,PR(pk)}$ reduction, which can be translated into the output term $(P_o/(2KV_{o,PR}))$ and C_P soft-charging term $(f_{sw}C_P V_{p(p-p)})$ reductions in equation (3.36). Similar to the distribution of conduction/switching losses, at light load, the C_P soft-charging

term predominates $I_{L,PR(pk)}$. On the other hand, as output current increases, the output term begins to dominate $I_{L,PR(pk)}$. Since the FSPPR converter reduces $I_{L,PR(pk)}$ by both $V_{p(p-p)}$ and K , $I_{L,PR(pk)}$ of the FSPPR converter is smaller at light loads and high VCR cases, as shown in Figure 3.22(a), compared to the BSPPR converter, which reduces $I_{L,PR(pk)}$ via $V_{o,PR}$ and K . On the other hand, as the output power/current increases, the advantage of the BSPPR, which relocates the PR to the high voltage/low current side, becomes more prominent, presenting a smaller $I_{L,PR(pk)}$ as shown in Figure 3.22(d). Given the same PR devices applied, the reduced $I_{L,PR(pk)}$ in the BSPPR converter indicates the ability to operate at a higher output current than others.

There are several sources of loss contributing to PR losses, such as dielectric, piezoelectric, and elastic losses. However, as reported in [68], dielectric and piezoelectric losses are significantly smaller than elastic losses (mechanical losses) and are considered negligible. Hence, the PR loss and efficiency can be simplified as equations (3.37) and (3.38) where R is the mechanical resistance in the BVD model.

$$P_{loss,PR} = \frac{1}{2} I_{L,PR(pk)}^2 R \quad (3.37)$$

$$\eta_{PR} = \frac{P_o}{P_o + P_{loss,PR}} \quad (3.38)$$

With equations (3.36) and (3.38), the PR efficiency at 48V input voltage and various output conditions are depicted in Figure 3.23. Given that the PR efficiency is directly linked to $I_{L,PR(pk)}$, the BSPPR converter demonstrates superior PR efficiency compared to others due to its reduced $I_{L,PR(pk)}$, especially in higher output current and lower output voltage scenarios.

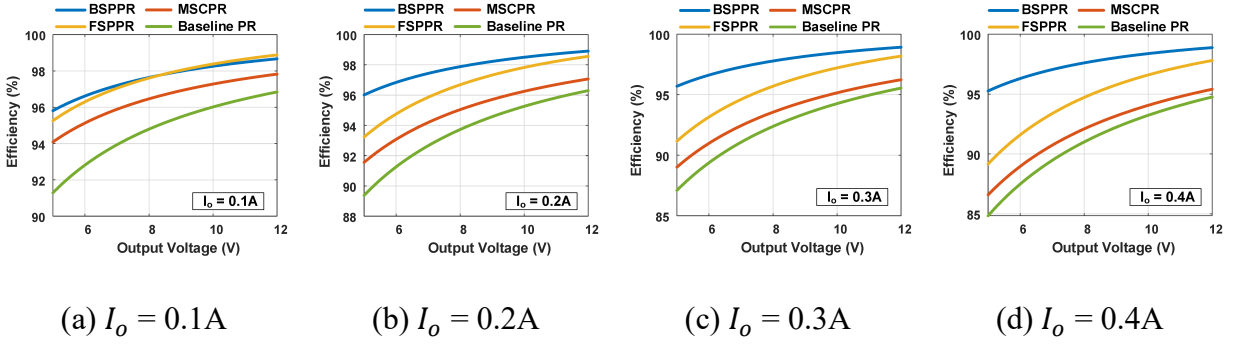


Figure 3.23 PR efficiency at $48V_{in}$.

3.4.5 Experiment Verification

The BSPPR converter prototype, depicted in Figure 3.24, is built alongside configurations to run the circuit as the FSPPR and baseline PR converters, with a PIC181 disk-shaped PR. The experimental parameters are shown in Table 3.10. In this design, the sandwich PR mounting approach is employed[70].

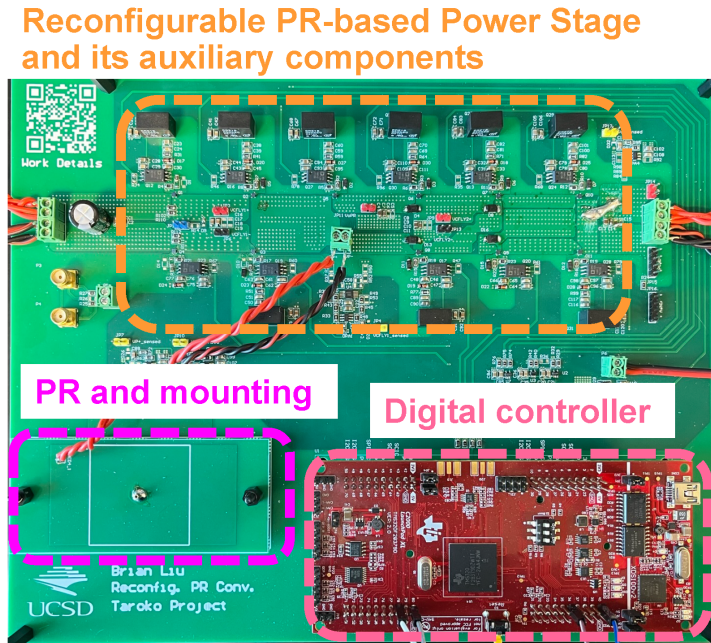
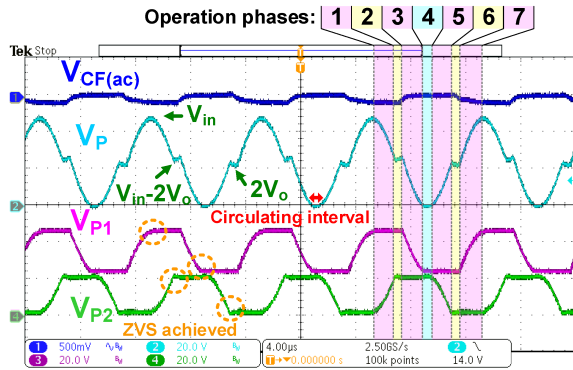


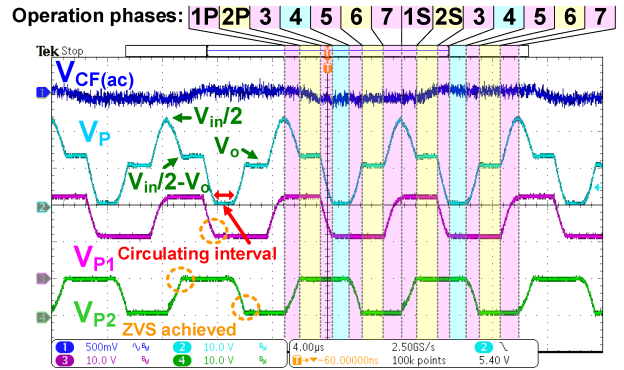
Figure 3.24 The BSPPR converter prototype with reconfigurability as the FSPPR and baseline PR converter.

Table 3.10 Experimental parts and parameters

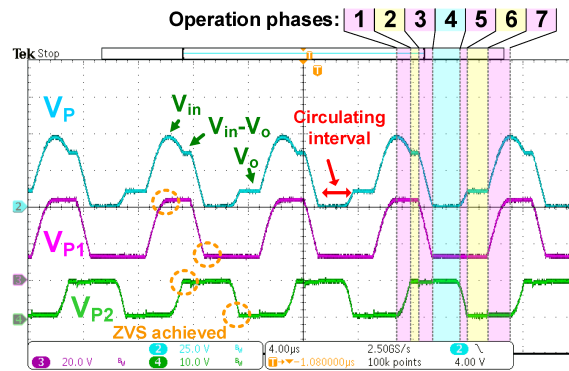
Parts/Parameters	Values	Implementation
Switches (S1-S7)	80V, 10A, 20mΩ	EPC2214
S6,7 parallel diode	40V, 2A	PMEG4020EP
Gate driver	Isolated, 2.3A	ADUM4120
Digital Controller	150MHz	TMS320F28335
Input voltage range V_{in}	36-60 V	-
Output voltage range V_o	4-12 V	-
Output current range I_o	0.05-0.3 A	-
flying capacitor C_F	4.7 μF	MLCC (0603)
Resonant frequency f_r	≈113 kHz	Piezo resonator
Anti-resonant frequency f_r	≈129 kHz	Piezo resonator
Quality factor Q	696	Piezo resonator
FSPPR flying capacitor C_{FF}	4.7 μF	MLCC (0805)



(a) BSPPR



(b) FSPPR



(c) Baseline PR

Figure 3.25 Steady-state operation waveforms @ $V_{in}/V_o = 48/10V$, $I_o = 0.1A$.

The steady-state operation waveforms of both the BSPPR, FSPPR, and baseline PR converters are shown in Figure 3.25 at 48/10V, 0.1A conditions. Based on the waveforms, all converters achieve ZVS but, notably, the BSPPR and FSPPR exhibit shorter PR circulating intervals, implying better PR utilization and efficiency. Moreover, V_{P2} of the BSPPR converter swings between 0 to $2V_o$ indicating an operation at an equivalent PR output voltage of $2V_o$, and consequently, implying a lower $I_{L,PR}$ (high voltage/low current side).

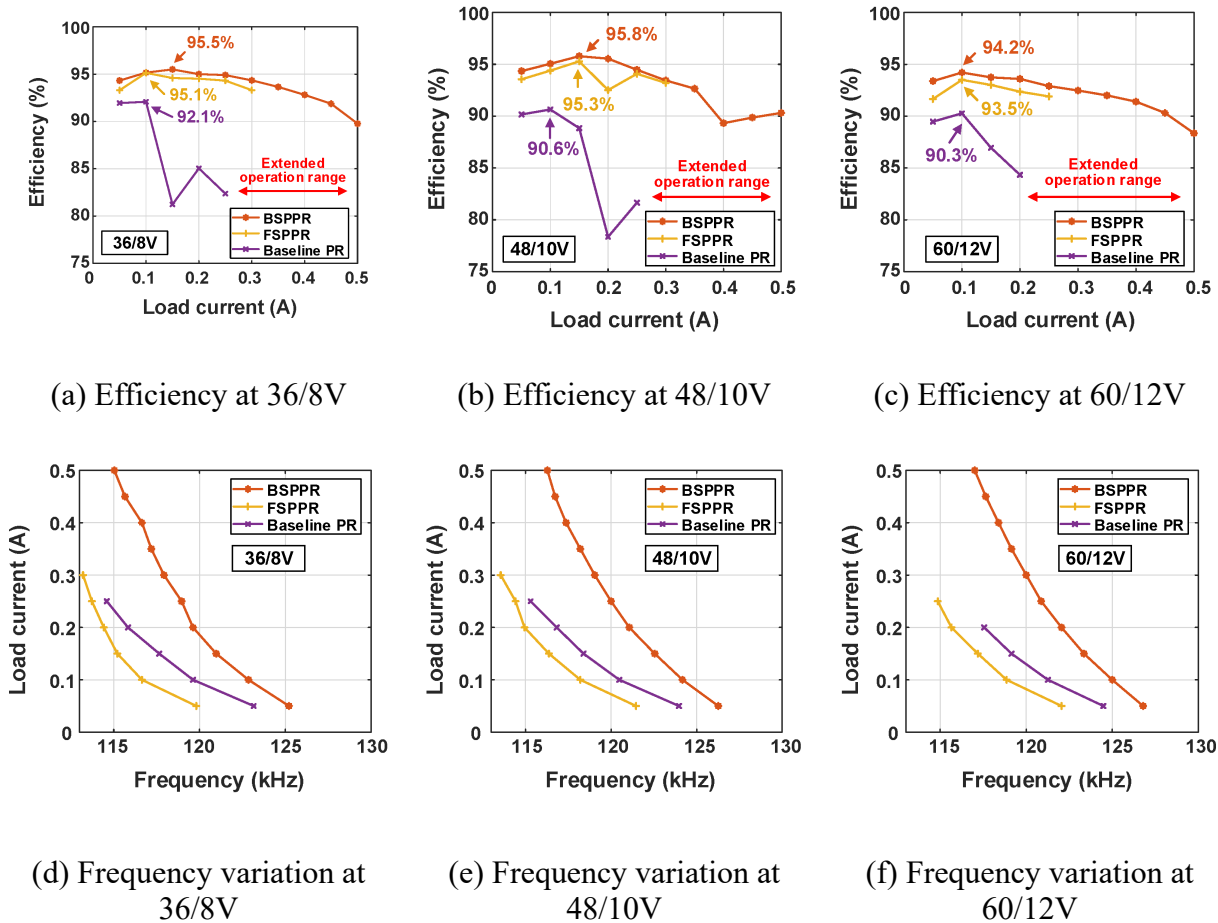


Figure 3.26 Efficiency, and frequency variation comparison at given VCRs.

The measured efficiency comparisons of the BSPPR, FSPPR, and baseline PR converters at the identical input/output conditions are shown in Figure 3.26(a)-(c). Here, the BSPPR converter achieves a peak efficiency of 95.8% while extending its operable load range because of a reduced

$I_{L,PR(pk)}$. Moreover, the BSPPR converter presents enhanced efficiency performance compared to the FSPPR and baseline PR converters across all test points. Note that the efficiency measurement concludes when the PR exhibits unstable behaviors, including low-frequency oscillations and voltage drop over time.

The frequency variations at the identical input/output conditions are depicted in Figure 3.26(d)-(f). In general, the frequency approaches resonant frequency as the load increases, and at the same load condition, the operational frequency tends to decrease with a reduction in input voltage. Here, the BSPPR operates at a slightly higher frequency owing to a higher equivalent PR output voltage, suggesting a better usage of the operable frequency range.

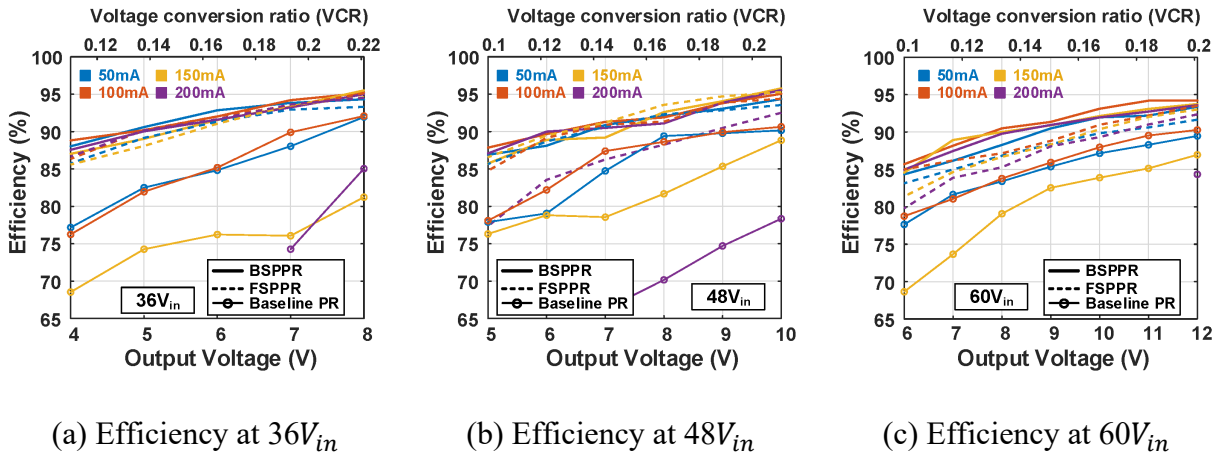


Figure 3.27 Efficiency comparison at given input voltage with different VCRs

The efficiency comparison of the BSPPR, FSPPR, and baseline PR converters at different output conditions is demonstrated in Figure 3.27. As expected, the BSPPR and FSPPR achieve higher efficiency than the baseline PR converter with a maximum of 23.2% and 18.6% efficiency improvement. In addition, the BSPPR converter generally obtained higher efficiency than the FSPPR, especially at lower VCR and higher output current scenarios.

The comparison table is presented in Table 3.11, delineating the volumetric footprints of active and passive power processing components and corresponding performance. As shown, situating the PR on the input side endows the BSPPR converter with enhanced output capabilities and high peak efficiency. Notably, the footprint of MLCC capacitors is small compared to the PR. Moreover, the strategic positioning of the SC network at the BSPPR converter's output side, operating at lower voltages, enables the utilization of compact 0603 MLCCs; in contrast, the FSPPR demands high-voltage capacitors for SC operations, necessitating the use of larger 0805 MLCCs. The combined advantages of the small footprint and low-voltage operation with MLCCs in the BSPPR converter result in marginal footprint augmentation while maximizing output capabilities. Note that power density is calculated as the peak output power divided by the sum of the footprints.

Table 3.11 Comparison table

	Baseline PR [29]	FSPPR [70]	This Work (BSPPR)
Active footprint	5.8 mm^3 (4x GaN)	10.2 mm^3 (7x GaN)	11.7 mm^3 (8x GaN)
Passive footprint	62.8 mm^3 (PR only)	65.2 mm^3 (PR, 1x 0805 Cap.)	65.4 mm^3 (PR, 2x 0603 Cap.)
$P_{o(max)}$	2.5 W	3 W	6 W
Power density	36.4 W/cm^3	39.8 W/cm^3	77.8 W/cm^3
Peak efficiency	92.08%	95.27%	95.8%

3.5 Conclusion

This chapter firstly introduces the piezoelectric materials and vibrations while presenting the BVD model equivalents that is linked to size of the piezoelectric resonators. Then, a frontside series/parallel PR-based (FSPPR) DC-DC converter is proposed to improve the performance of

conventional PR-based converters at low voltage conversion ratios. By leveraging switched capacitor hybridization, the PRs can operate at their optimal conversion ratio, specifically, $VCR_{PR} \approx 0.5$, all while maintaining an overall compact size and all of the advantages of PR-based converters, i.e., ZVS and soft-charging of capacitors. The operation, circuit behavior, and loss model of the proposed topology are presented, analyzed, and validated through simulation, calculation, and experiments. In addition, the size selection and mounting of the piezoelectric resonator are discussed, supported by calculation and measurement results. Finally, a FSPPR converter prototype is built with a disk-shaped PZT piezoelectric resonator operating in a radial vibration mode and can be reconfigured as a co-designed baseline PR-based converter for fair comparisons. The prototype demonstrates 95.27% peak efficiency with up to 14% efficiency improvement compared to the baseline PR-based converter at a 48/10V conversion ratio.

On the other hand, this chapter also introduces a hybrid Backside Series/Parallel PR-based converter (BSPPR) aiming to improve the performance of the hybrid PR-based converters (the FSPPR and MSCPR converters) and baseline PR-based converter when requiring high step-down conversion ratios. Utilizing the hybrid concept similar to the FSPPR converter, the BSPPR converter can operate at a smaller VCR while maintaining decent efficiency performance. Moreover, unlike prior hybrid converters, placing the PR at the output side (low voltage/ high current side), the BSPPR positions the PR at the high voltage/ low current side, reducing PR vibration loss and extending output capability. A physical prototype of the BSPPR converter alongside the baseline PR and FSPPR converter with a 20/0.2mm disk-shaped PIC181 PR was built. Measurement results demonstrated a 95.8% peak efficiency, and enhanced performance compared to the baseline PR and FSPPR converter across various conversion ratios.

Acknowledgements

Chapter 3 is based on and mostly a reprint of the following publication(s):

- W. -C. B. Liu and P. P. Mercier, "A Series/Parallel Magnetic-Less Step-Down Converter based on Piezoelectric Resonators," *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA, 2023, pp. 484-489, doi: 10.1109/APEC43580.2023.10131228.
- W. -C. B. Liu and P. P. Mercier, " A Merged Backside Series Parallel Hybrid Piezoelectric-Resonator-Based DC-DC Converter," *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2024, pp. 2130-2135, doi: 10.1109/APEC48139.2024.10509428.
- W. -C. B. Liu, and P. P. Mercier, " Design and Analysis of A Frontside Series/Parallel Piezoelectric Resonator-based DC-DC Converter," *submitted to IEEE Transactions on Power Electronics (under review)*.

Chapter 4 An Integrated Dual-side Series/Parallel

Piezoelectric Resonator-based DC-DC Converter

4.1 Introduction

To improve the efficiency of PR-based converters at low VCRs, recent art has suggested adopting two-stage switched-capacitor (SC)/PR-based[78] or hybrid SC/PR-based structure[70], [71]. By leveraging the SC stage/network, which handles a portion of the conversion ratio, PRs are more efficiently operated and the excessive PR current at low VCRs is avoided due to enhanced K . In the two-stage configuration[78], an 4:1 SC stage is cascaded with the output of the baseline PR-based converter, preventing the PR stage from directly dealing with the high output current that improves the efficiency and power capability at low VCRs ($0.12 \leq VCR \leq 0.24$). However, the SC stage and the PR-based stage work independently, thereby requiring more active/passive devices (transistors and capacitors) for the additional SC stage. Moreover, the two-stage design occur the cascade loss that could limit the overall performance. On the other hand, in the hybrid configuration, the SC network cooperates with the operation of the PR-based converters, avoiding cascade loss while distributing the voltage drop across low-voltage transistors. For example, the Baseline PR-based converter integrates an SC in front of the PR towards a Frontside Series/Parallel PR-based (FSPPR) converter[70], lowering the equivalent input voltage to the PR and, as a result, improving K as well as efficiency. Meanwhile, the Merged Switched-Capacitor PR-based (MSCPR) converter[71] merged an inter-state SC connecting the input and output, enabling minimum switch counts while reducing the equivalent input voltage to the PR. However, such prior limits the optimal conversion ratio to around 0.25-0.33, which is not favorable for

applications requiring even lower VCRs ($VCRs \leq 0.1$) Importantly, no work has reported operation at low voltage outputs with a high step-down ratio (e.g. $V_{in} \geq 15V, V_o \leq 2V$).

As the two-stage and hybrid strategies become popularized, more and more switches are added to the PR-based configuration, imposing difficulties in driving design and total size considerations for discrete designs[70], [71], [78], which limits the effectiveness of adopting these strategies. Therefore, moving from discrete to highly integrated silicon-based design becomes imminent where the driving circuitry and power transistors can be integrated into a single die, enabling compact design. Unfortunately, no work has reported an integrated circuit designed specifically for PR-based DC-DC conversion.

This Chapter introduces an IC-based hybrid Dual-side Series/Parallel PR (DSPPR) converter that exploits the ability of ICs to offer sophisticated power stages in a small area compared to discrete design, all towards efficient operation at low VCRs ($VCRs \leq 0.1$). The DSPPR topology features: 1) integration of 2:1 series/parallel SC networks at both the input (frontside) and the output (backside) of the PR towards achieving an optimal PR charge transfer utilization at VCR of 0.125 without incurring cascaded losses; 2) adoption of transistor stacking, a technique popularized by hybrid converters[55]-[60], to alleviate voltage stress on power transistors; 3) strategic placement of the PR in the middle of the converter optimizing the equivalent input/output voltage levels to minimize PR loss and enhance output current capability compared to prior arts; 4) preservation of zero-voltage switching (ZVS) and the soft charging of C_P ; 5) soft charging of the frontside flying capacitor, C_{F1} , through the inductive nature of the PR; and 6) self-balancing of the backside flying capacitor, C_{F2} .

4.2 Dual-side Series/Parallel Piezoelectric-Resonator-based DC-DC Converter

The circuit diagram and operation waveforms of the DSPPR converter are illustrated in Figure 4.1 and Figure 4.2(a). Note that, $V_{in,PR}$, and $V_{o,PR}$ in Figure 4.2(a) are the effective input/output voltage applied to the PR, which are $V_{in}/2$ and $2V_o$ in the DSPPR converter. Here, the PR is represented by the BVD model, comprising a mechanical RLC branch and parallel piezoelectric capacitor. By operating the PR within its inductive region, ZVS and soft-charging/discharging of C_p are achieved. In addition, two 2:1 series/parallel switched capacitor (SC) circuits are merged into the input (frontside) and output (backside) of the baseline PR-based converter, each offering an additional 2:1 conversion ratio and thus enabling optimal efficiency at an 8:1 (0.125 VCR) conversion ratio.

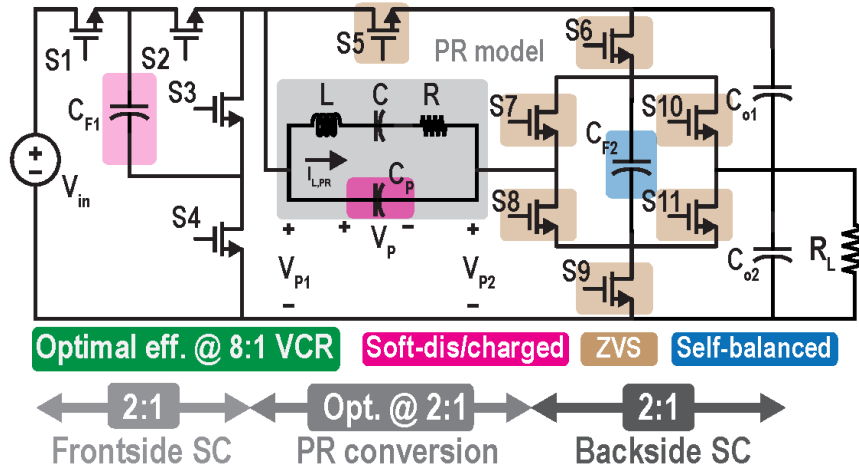
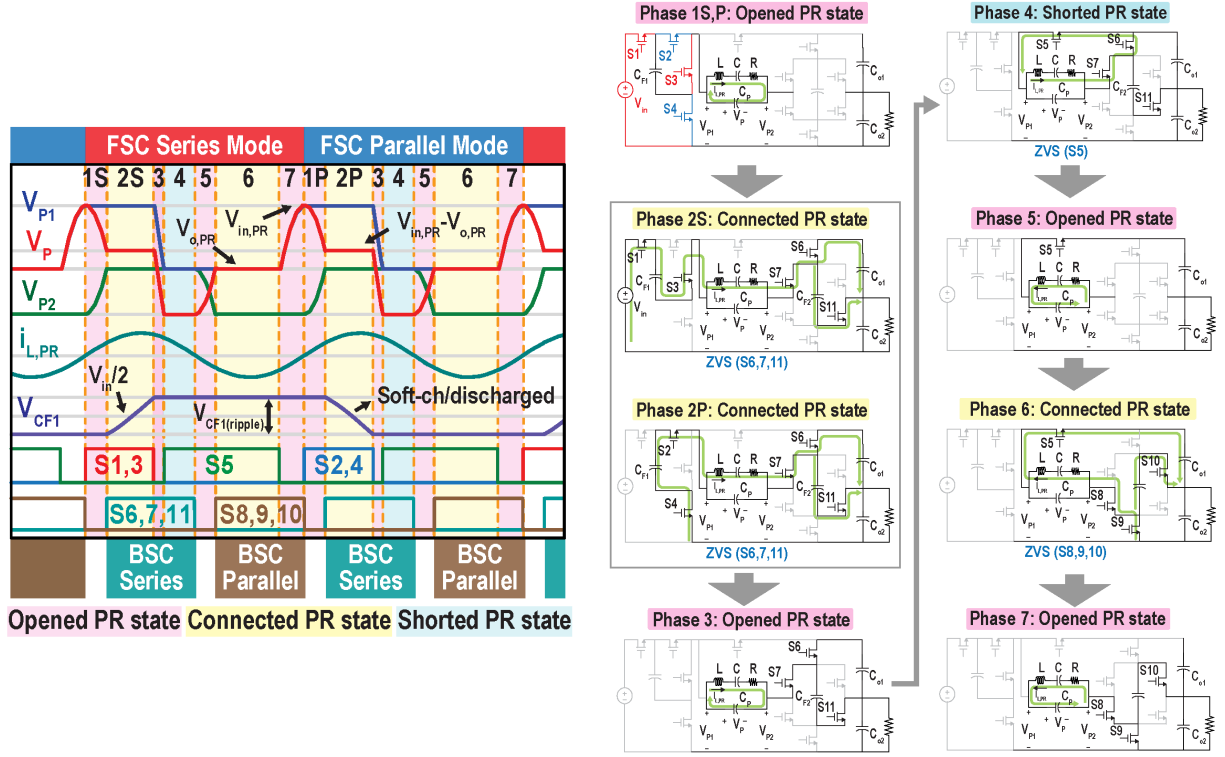


Figure 4.1 Circuit diagram of the Dual-side Series/Parallel PR-based (DSPPR) converter.



(a) Operation waveforms

(b) Operation phases

Figure 4.2 Operation of the Dual-side Series/Parallel PR-based (DSPPR) converter.

In SC configuration, the frontside switched capacitor (FSC), C_{F1} , is clamped to half the input voltage and operated in either series or parallel with the PR inter-cyclically, leading to the reduction in switches' voltage stress (S1-5), particularly in low VCR scenarios, as shown in Table 4.1 and the effective input voltage applied to the PR. Additionally, in a way that is similar to hybrid converters, C_{F1} is soft-charged/discharged by the inductive PR current, $i_{L,PR}$. On the other hand, the backside switched capacitor (BSC), C_{F2} , functions in series or parallel with the load intra-cyclically, enhancing the effective output voltage of the PR with self-balancing and enabling ZVS for switch S10 and S11. Moreover, the BSC decouples the PR from the low voltage/high current output, minimizing the current stress over the PR, for which the device is predominately limited by current density and thereby enhancing the output capability compared to the prior art with the same PR.

Table 4.1 Voltage stress of the power transistors

	Baseline PR	DSPPR
Input-connected switches	$V_{in} - V_o$ (S1)	$V_{in}/2$ (S1-4)
Inter-connected switches	$V_{in} - V_o$ (S2)	$V_{in}/2 - V_o$ (S5)
Output-connected switches	V_o (S3,4)	V_o (S6-11)

According to Figure 4.1 and 4.2(a), it can be observed that the DSPPR topology acts as a single stage, effectively avoiding the cascade loss associated with multi-stage topologies. Moreover, its operation consistently aligns with that of the baseline PR-based converter, considerably simplifying control complexity and facilitating the extension of baseline PR-based control strategies.

The operation phases are shown in Figure 4.2(b). The operation principle of the DSPPR converter is the same as the baseline PR converter in that there is a sequence of 7 phases, yet here phases 1 and 2 interleave their connection (series, S, or parallel, P) to the frontside SC circuit such that control complexity is not increased. Throughout the 7 phases, the PR can be in one of three states: (1) opened PR, (2) connected PR, and (3) shorted PR states. Initially, there are no current paths formed by switches in phase 1, and hence, in this opened PR state, the sinusoidal current formed by the PR, $i_{L,PR}$, discharges C_P . In phase 1S, C_{F1} is connected in the up (series) position, while in the subsequent cycle, in phase 1P, C_{F1} is connected in the down (parallel) position. Once V_{P2} reaches $V_{o,PR}$, S6, S7, and S11 are activated with ZVS, and phase 2 begins, connecting the PR to the input and output for energy delivery. Here, C_{F1} is soft-charged in phase 2S and soft-discharged in phase 2P due to inductive current, $i_{L,PR}$, ensuring charge balance. On the other hand, C_{F2} is in series with the load in both phases 2S and 2P. Phase 3 starts with deactivating switches S1-4, enabling the opened PR state, where $i_{L,PR}$ discharges C_P until $V_{P1} = V_{o,PR}$, enabling ZVS

turn-on for S5. Then, phase 4 initiates, forming a shorted loop where $i_{L,PR}$ circulates until its polarity reverses, after which switches S6, S7, and S11 are opened. This brings the PR back to an open PR state in phase 5, making V_{P2} node decrease until it reaches zero and enabling ZVS turn-on for S8-10. At this point, C_{F2} is in parallel with the load, and the PR is linked to the output, allowing the PR to release energy to the load. Phase 7 begins when S5 turns off, opening the PR, where $i_{L,PR}$ charges C_P until V_{P1} reaches $V_{in,PR}$, minimizing switching loss across S1,3/S2,4 in the next SC cycle.

4.3 Steady-state analysis: PR operation

In this section, a general PR operation and analysis following the methodology reported in [29] will be introduced. Since the operation of the PR is exactly aligned with the baseline PR-based converter and its extension (i.e., the FSPPR converter), the results in this section can be directly applied to these converters.

4.3.1 PR and Overall Voltage Conversion Ratio

Based on the operation waveforms as shown in Figure 4.2(a), the PR must follow the conservation of charge (CoC) and energy (CoE) across an operation cycle to guarantee charge and energy balance.

By utilizing similar method discussed in Chapter 3.4.3.1, the voltage conversion ratio can be derived as equation (4.1), indicating that the effective PR voltage conversion ratio, VCR_{PR} , is determined by the proportions of q_2 and q_4 during the positive half cycle of $i_{L,PR}$. This implies that when phase 2 (input-connected state) encompasses the entire positive half cycle, the VCR is

equal to 0.5; conversely, as phase 4 (shorted state) inhabits over the positive half cycle, the VCR reduces to 0.

$$0 \leq \frac{V_{o,PR}}{V_{in,PR}} = \frac{q_2}{2q_2 + q_4} \leq \frac{1}{2} \quad (4.1)$$

Because of the dual-side 2:1 SCs, the overall conversion ratio of the DSPPR converter can be derived as equation (4.2) by substituting $V_{in,PR} = V_{in}/2$, and $V_{o,PR} = 2V_o$, respectively:

$$0 \leq \frac{V_o}{V_{in}} \leq \frac{1}{8} \quad (4.2)$$

4.3.2 PR Charge Transfer Utilization

The PR charge transfer utilization factor, or PR utilization factor (K), is used to assess how efficiently a particular topology exploits the PR, as outlined in[29]. By definition, K is determined by the ratio of charges in the connected state to the total charges in both the connected and shorted PR states. In the connected state, charges are delivered to the output, whereas they circulate within the converter in the shorted state. Therefore, based on operation waveforms shown Figure 4.2(a), K can be formulated and derived as equation (4.3) by incorporating CoC and CoE (equations (3.29)-(3.31)). Here, K in equation (4.3) resides between 0.5 and 1 and $K = 1$ as $V_{o,PR} = 0.5V_{in,PR}$, implying an optimal operation of $VCR_{PR} = 0.5$. Moreover, with a specific output condition, better utilization denotes a greater proportion of charges delivered to the output (active charges) and a reduction in circulating charges (reactive charges) signifying better efficiency.

$$K = \frac{|q_2| + |q_6|}{|q_2| + |q_4| + |q_6|} = \frac{V_{in,PR}}{2(V_{in,PR} - V_{o,PR})} \quad (4.3)$$

4.3.3 PR Current Amplitude and Loss

Apart from K , the PR current, $i_{L,PR}$, is identified as a metric to evaluate the performance of PR-based converters since the PR current amplitude, $I_{L,PR(pk)}$, indicates how much conduction loss is generated. The $I_{L,PR(pk)}$ can be obtained from the total charge, Q_{tot} , transferred by $i_{L,PR}$, which is expressed as equation (4.4). Here, $i_{L,PR}$ can be viewed as a pure sinusoidal wave with frequency $\omega = 2\pi f_{sw}$ due to the resonant operation with high PR quality factor, Q defined as $Q = \sqrt{L/C}/R$. On the other hand, Q_{tot} comprises of charges used for energy delivering ($I_o/(Kf_{sw})$) and charges used to achieve ZVS ($2C_P V_{pp}$), where V_{pp} is the voltage swing of the PR in a cycle.

$$Q_{tot} = 2 \int_0^{\frac{1}{2f}} i_{L,PR}(t) dt \quad (4.4)$$

Where,

$$i_{L,PR}(t) = I_{L,PR(pk)} \sin(\omega t), \quad Q_{tot} = \frac{I_{o,PR}}{Kf_{sw}} + 2C_P V_{pp}$$

Solving equation (4.4) allows for the derivation of the PR resonant current amplitude, $I_{L,PR(pk)}$, as:

$$I_{L,PR(pk)} = \pi \left(\frac{I_{o,PR}}{2K} + f_{sw} C_P V_{pp} \right) \quad (4.5)$$

With $I_{L,PR(pk)}$ derived, the loss of PR due to mechanical motion, $P_{L,PR}$, can be calculated:

$$P_{L,PR} = \frac{1}{2} R I_{L,PR(pk)}^2 \quad (4.6)$$

As shown in equation (4.5), the amplitude of the PR current under specified operation conditions is influenced by three components: 1) PR utilization, K , 2) effective PR output current, $I_{o,PR}$, and 3) PR voltage swing, V_{PP} . Specifically, minimizing $I_{o,PR}$ and V_{PP} , while maximizing K ,

leads to a reduction in $I_{L,PR(pk)}$ and, consequently, minimizes PR motion loss, $P_{L,PR}$, as elaborated in equation (4.6)

The DSPPR converter, because of the dual-side SC configuration, minimizes $I_{o,PR}$ and V_{PP} while maximizing K . Here, compared to the baseline PR-based converter, $I_{o,PR}$ is reduced from I_o to $0.5I_o$; V_{PP} is reduced from V_{in} to $0.5V_{in}$; K is improved by a higher $V_{o,PR}$ and $V_{in,PR}$ ratio.

4.3.4 Phase Duration for Steady-State Operation

To understand the operation of the DSPPR converter comprehensively, analyzing the impact of each phase duration on the system conversion is crucial. Assuming a lossless system, the duration of each phase is determined by the charge transferred by $i_{L,PR}$, similar to equation (4.4), but with an analysis conducted for each phase, expressed as follows:

$$q_n = \int_{\sum_{i=1}^{n-1} t_i}^{t_n + \sum_{i=1}^{n-1} t_i} i_{L,PR}(t) dt \quad (4.7)$$

In the phase where the PR is open, the charge, q_n , can be calculated using the charge formula ($\Delta Q = C_p \times \Delta V_n$), with ΔV_n representing the voltage charged or discharged during the respective phase. On the other hand, for phases where the PR is connected or shorted, charges can be determined through CoC and CoE (equations (3.29)-(3.31)), along with the lossless PR conversion. Specifically, since phase 2 is the only phase that is connected to the input source, q_2 must follow the conservation of energy ($E_{in,PR} = E_{o,PR}$) and, accordingly, can be calculated. Subsequently, q_4 and q_6 are determined using CoC and CoE (equations (3.29)-(3.31)), based on the equations $q_2 + q_4 + q_6 = 0$ and $(V_{in,PR} - V_{o,PR})q_2 + V_{o,PR}q_6 = 0$.

Finally, q_n can be expressed as:

$$\begin{cases} C_P V_{o,PR}, & n = 1 \\ \frac{1}{V_{in,PR}} \frac{P_o}{f_{sw}}, & n = 2 \\ C_P (V_{in,PR} - V_{o,PR}), & n = 3 \\ \frac{V_{in,PR} - 2V_{o,PR}}{V_{in,PR} V_{o,PR}} \frac{P_o}{f_{sw}}, & n = 4 \\ C_P V_{o,PR}, & n = 5 \\ \frac{V_{in,PR} - V_{o,PR}}{V_{in,PR} V_{o,PR}} \frac{P_o}{f_{sw}}, & n = 6 \\ C_P (V_{in,PR} - V_{o,PR}), & n = 7 \end{cases} \quad (4.8)$$

Combining equations (4.7) and (4.8), the phase duration can be obtained as Figure (4.9):

$$t_n = \frac{1}{\omega} \cos^{-1} \left(\cos \left(\omega \sum_{i=1}^{n-1} t_i \right) - \frac{\omega q_n}{I_{L,PR(pk)}} \right) - \sum_{i=1}^{n-1} t_i \quad (4.9)$$

In this model, the operation frequency, f_{sw} , emerges as the uncertain variable, being analytically unsolvable as reported in [75]. Therefore, for early-stage design time duration evaluation, the resonant frequency serves as a useful reference because the operation frequency of PR-based converters lies within a range between the resonant frequency, f_r , and the anti-resonant frequency, f_{ar} . Additionally, the operation frequency approaches f_r as the output current increases. This approximation facilitates the prediction of PR-based converters' behavior.

Figure 4.3, which showcases V_P and $i_{L,PR}$, validates the proposed time duration model at a 20/2.2V, 0.1A condition with PR parameters listed in Table 4.2. Here, V_P is plotted based on the calculations of the time duration model, t_n , and $i_{L,PR}$, determined by equation (4.5). Two sets of calculation results are presented: 1) calculations using an approximation ($f_{sw} \approx f_r$) for early-stage evaluation, and 2) calculations with the simulated frequency ($f_{sw} = f_{sim}$) for post-design

validation. It can be observed that the calculations are closely aligned with the simulations, attesting the validity of the model.

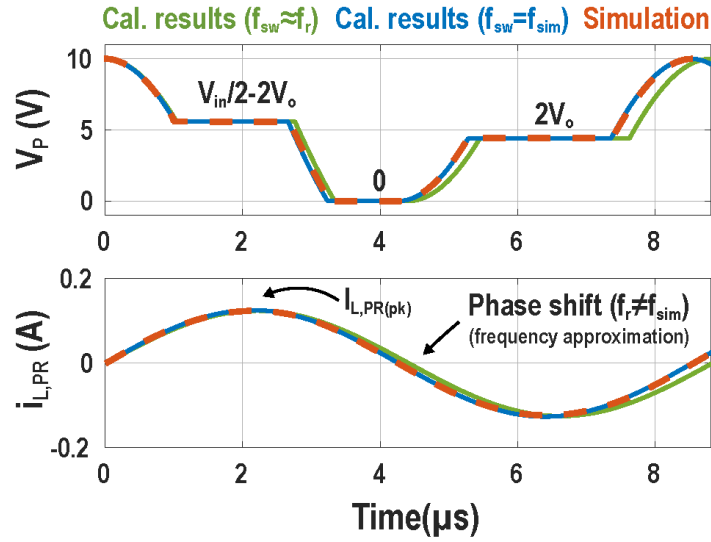


Figure 4.3 Time duration model verification at 20/2.2V, 0.1A

Table 4.2 Parameters of disk-shaped radial-mode piezoelectric resonator in a size of 20/0.2mm (diameter and thickness) and PIC181 material

	C_p	C	L	R	f_r/f_{ar}	Q
	(nF)	(nF)	(μH)	(Ω)	(kHz)	
Value	10.5	5	654.4	0.38	113/129	≈1233

4.3.5 Topological performance comparison

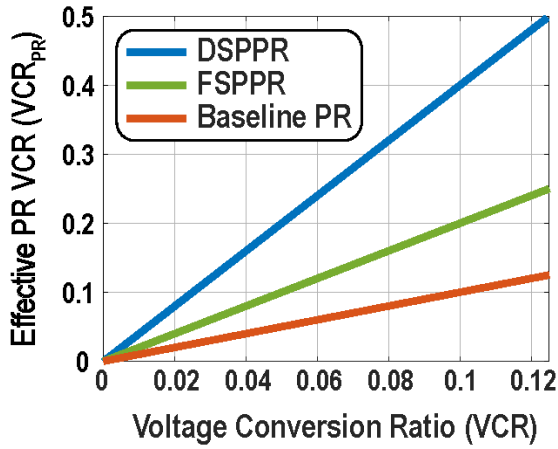
The metrics, specifically VCR , K , $I_{L,PR(pk)}$ and $P_{L,PR}$, presented in steady-state analysis can be applied to topological comparisons, evaluating the performance of the proposed DSPPR converters relative to the prior art. Here, the comparisons emphasize low VCR scenarios, aligning with the objective in this Chapter.

Table 4.3 illustrates the voltage conversion ratio range of the PR-based converters. Due to the SC(s) conversion, the operation range is narrowed down when more SC networks are integrated

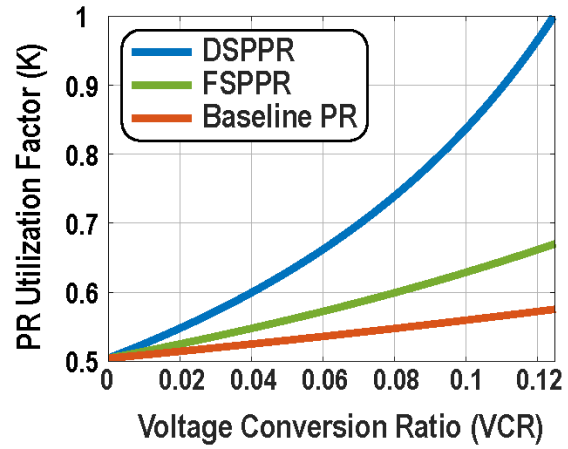
into the baseline PR-based converter. Nevertheless, a reduced overall VCR range comes with a boost in effective VCR_{PR} in the operable range, as shown in Figure 4.4(a). The relationship between VCR_{PR} and PR utilization can be found by rearranging equation (4.3) and is elaborated in equation (4.10) and Figure 4.4(b). As analyzed above, better utilization results in circulating charge reduction, and consequently, leads to better efficiency.

Table 4.3 Voltage conversion Ratio Comparison

Topology	VCR			VCR_{PR}
Baseline PR	0	$\leq \frac{V_o}{V_{in}} \leq$	1/2	VCR
FSPPR	0		1/4	$2 \times VCR$
DSPPR	0		1/3	$4 \times VCR$



(a) PR effective VCR, VCR_{PR}



(b) PR utilization factor, K

Figure 4.4 PR effective VCR, VCR_{PR} and PR utilization factor, K , versus overall VCR

$$K = \frac{1}{2(1 - VCR_{PR})} \quad (4.10)$$

Apart from VCR range and utilization, $I_{L,PR(pk)}$ and $P_{L,PR}$ also serve as metrics to compare the performance since they are directly related to the overall efficiency of the converters. Here,

$I_{L,PR(pk)}$ and $P_{L,PR}$ are plotted along with: 1) output current variation at a given input/output voltage, as illustrated in Figure 4.5(a), and 2) voltage conversion ratio at specific input voltage and load current, as depicted in Figure 4.5(b).

According to the figures, the DSPPR achieves an excellent current reduction compared to the prior art (FSPPR and Baseline PR-based converters), thereby resulting in a loss reduction. Here, the loss is not only the PR loss, as shown in Figure 4.5, but also the conduction loss, $I_{rms}^2 R_{on}$ loss, generated from the switches and relative traces in the system since the PR current, $I_{L,PR}$, always flows through switches at a specific time. In addition to the benefits related to the loss reduction, the operation of the PR, as mentioned, is mainly constrained by the current density. Therefore, the reduction in PR current amplitude (improvement in K) allows the system to handle higher output power. This suggests that the DSPPR converter is capable of higher output power compared to the prior art at a given PR, or on the other hand, at a given power, the DSPPR converter can leverage a smaller power due to current reduction.

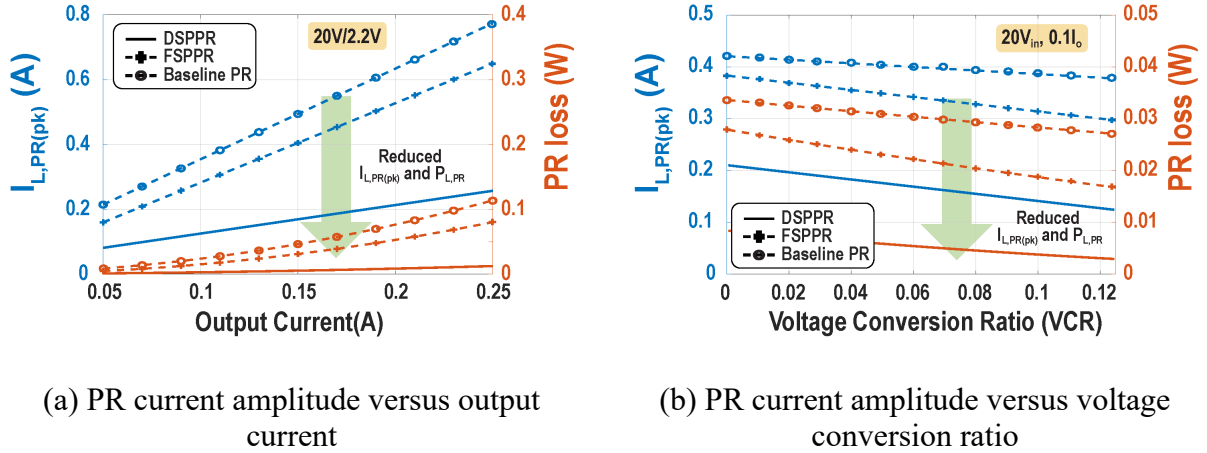


Figure 4.5 PR current amplitude and loss at 20V input voltage with respect to output current and voltage conversion ratio.

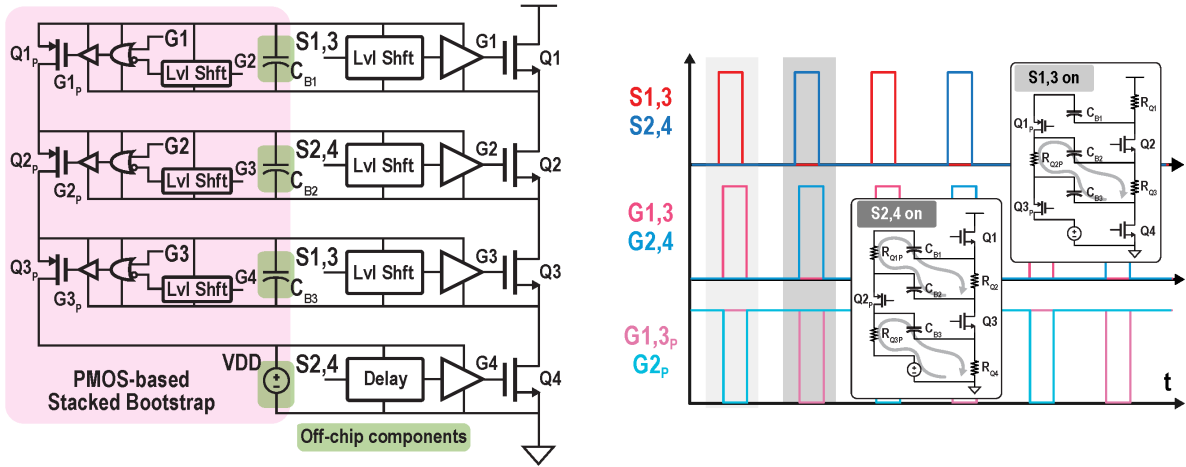
4.4 Circuit Implementation

The circuit diagram of the converter is depicted in Figure 4.1, integrating all power switches along with their corresponding gate drivers and level shifters onto a single die using 180nm BCD technology. On the other hand, all passive components, including the PR, flying capacitors, and bootstrap capacitors, are implemented off-chip. Additionally, due to the complexity of the control timing, off-chip digital control is utilized.

4.4.1 Floating Gate Driving Strategy

In this design, all of the power switches in the DSPPR are implemented by on-chip nMOS transistors, as shown in Figure 4.1. Since multiple power transistors, 9 transistors, are floating relative to the ground, a compact yet efficient driving and level shifting scheme is required. Here, a pMOS-based stacked bootstrap driver approach is employed, where the high-side transistor draws energy from its neighboring low-side transistor while the low-side transistor is turned on, forming a loop for energy delivery.

For instance, consider the frontside SC network in Figure 4.1, whose driving circuit and timing diagram are shown in Figure 4.6. When $S_{1,3}$ is set, C_{B2} charges from C_{B3} ; conversely, when $S_{2,4}$ is set, C_{B1} and C_{B3} charge from C_{B2} and VDD . By repeating this bootstrap operation, all the floating switches can be properly driven from a ground-referenced VDD , and the same logic is applied to the remaining floating transistors. The driving signals after the gate driver, G_n , are also reused for bootstrapping, preventing simultaneous turn-on of the power switch, Q_n , and its corresponding bootstrapping pMOS, Q_{n_p} , where $n = 1, 2, 3$.



(a) Simplified circuit diagram

(b) Timing diagram with equivalent circuits

Figure 4.6 Floating gate driving strategy.

Though the stacked bootstrap strategy can deliver energy from the ground-reference level to floating nodes, the actual driving voltage (voltage of V_{Bx}) of the floating transistor is influenced by several factors during bootstrapping, including bootstrap capacitance, bootstrap time, power consumption, and other parasitics. Therefore, it is important to carefully design the bootstrap capacitor. For example, at given power consumption, path resistance, and bootstrap time (with others assumed to be ideal), the steady-state voltage (V_{BTS} or V_{Bx}) and voltage ripple (ΔV_{BTS} or ΔV_{Bx}) of the bootstrap capacitors, C_{Bx} , can be drawn as Figure 4.7. Here, a trade-off between V_{BTS} and ΔV_{BTS} can be observed. With a large C_{Bx} , V_{BTS} is reduced, whereas a low V_{BTS} could result in increased conduction loss or malfunction to the system. On the other hand, with a small C_{Bx} , ΔV_{BTS} is increased, which degrades the system stability. Thus, a proper value of C_{Bx} is crucial where an acceptable trade-off between 80 to 200nF is observed; 0402 150nF capacitors are selected for this work.

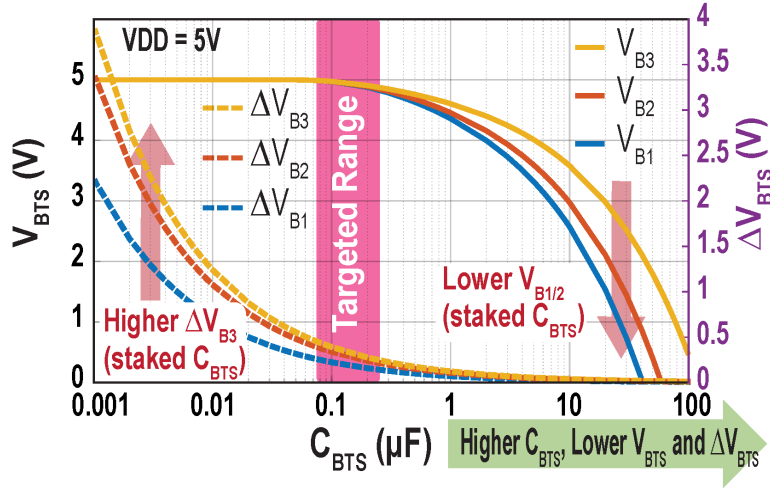


Figure 4.7 Trade-off between bootstrap steady-state voltage and voltage ripple in designing the value of bootstrap capacitor.

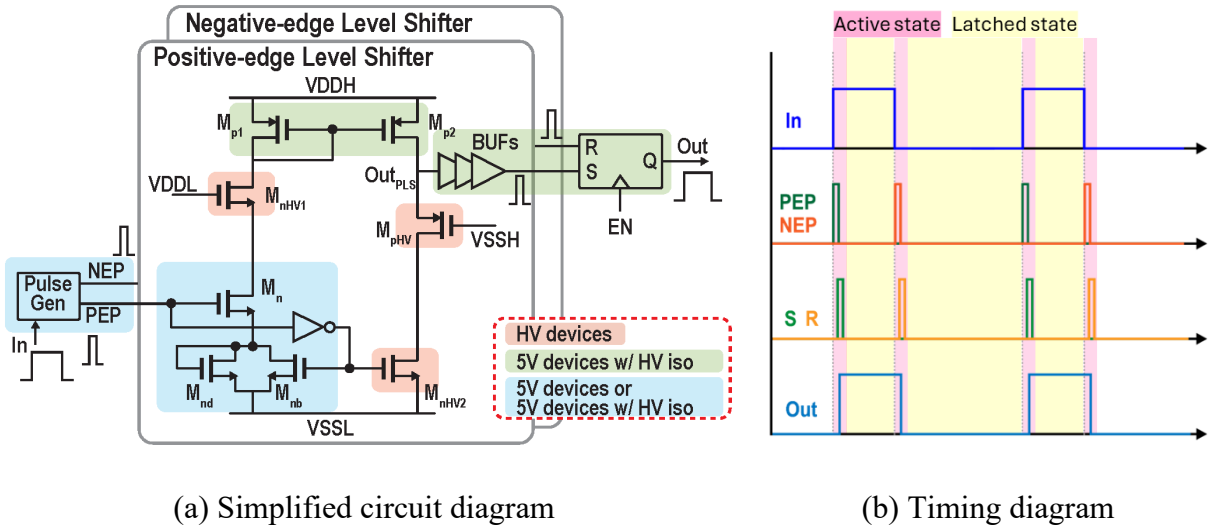


Figure 4.8 Latch-type level shifter with low power consumption.

4.4.2 Level Shifter

Level shifting is accomplished via the circuit in Figure 4.8, based on [79]. This design consists of two identical level shifters responsible for positive and negative edge level shifting, respectively. In operation, positive/negative-edge pulses (*PEP* and *NEP*) are generated by the pulse generator, and fed to their respective level shifters. As *PEP* is set, for example, current flows

through the M_n branch and is mirrored by M_{P1} and M_{P2} , charging output pulse node, Out_{PLS} , and generating a set pulse for the SR latch. When PEP is reset, M_{nHV2} pulls down Out_{PLS} . Thus, the level shifter is briefly activated only when an edge-triggered pulse is received, resulting in a power of $\sim 200\mu W$ at the highest rail voltage (20V) at PR resonant frequency ($\sim 113 kHz$) and propagation delay of 2ns.

4.4.3 PR Constants and BVD Model for Size Selection

Here, following the PR equivalent modeling in equations (3.1)-(3.4), four piezoelectric constants along with geometrical constants are required to model the behavior of disk-shaped radial mode PRs into the BVD model. The piezoelectric constants are 1) dielectric constant, ϵ_{33}^T , 2) quality factor, Q , 3) coupling factor, k_p , and 4) vibrating frequency constant, N_p whereas the geometrical constants are radius, r , and thickness, l . With the constants, the BVD model equivalents can be derived as shown below:

$$C_p = \epsilon_{33}^T (1 - k_p^2) \frac{\pi r^2}{l} \quad (4.11)$$

$$C = k_p^2 C_p \quad (4.12)$$

$$L = \frac{r^2}{\pi^2 N_p^2 k_p^2 C_p} \quad (4.13)$$

$$R = \frac{1}{Q} \sqrt{\frac{L}{C}} = \frac{1}{\pi^2 Q \epsilon_{33}^T N_p (1 - k_p^2) k_p^2} \frac{l}{r} \quad (4.14)$$

Where,

$$k_p = \sqrt{\frac{f_{ar}^2 - f_r^2}{f_r^2}}, \quad Q = \frac{1}{R} \sqrt{\frac{L}{C}}, \quad f_r = \frac{N_p}{2r} = \frac{1}{2\pi\sqrt{LC}}, \quad f_{ar} = \frac{1}{2\pi\sqrt{L \frac{C_p C}{C_p + C}}}$$

It can be found in equation (4.14) that the mechanical resistance, R is minimized by minimizing thickness, l , and maximizing the radius, r , which is the same conclusion as the analysis presented in Chapter 3.3.3. However, there are practical limits that, due to structural stress considerations, the thickness cannot be reduced to infinitesimal levels, and the radius cannot be expanded indefinitely. In the radial mode, the thickness is irrelevant to the resonant frequency. Instead, l defines the maximum allowable voltage applied to the PR, which is typically around $1kV/mm$ for hard-PZT materials. Thus, the thickness must be sufficient to withstand this voltage. On the other hand, the radius determines the resonant frequency. Yet, the large radius shifts the frequency to a low-frequency spectrum while introducing enormous piezo-static capacitance, C_p , leading to excessive PR current.

To find the optimal ratio between thickness and radius, the C_p , f_r , and R can be substituted into equations (4.5) and (4.6). By rearranging the equation, the PR loss with respect to geometrical constants can be expressed as:

$$P_{L,PR} = \frac{\pi^2}{2} \frac{\gamma}{F} (\alpha + \beta F)^2 \quad (4.15)$$

Where,

$$\alpha = \frac{I_{o,PR}}{2k}, \quad \beta = \frac{1}{2} \pi \epsilon_{33}^T N_p (1 - k_p^2) V_{pp}, \quad \gamma = \frac{1}{Q} \frac{1}{\pi^2 \epsilon_{33}^T N_p (1 - k_p^2) k_p^2}, \quad F = r/l$$

By solving $\partial(P_{L,PR})/\partial F = 0$, the optimal ratio could be found as $F = \alpha/\beta$ that lead to minimal PR loss as:

$$P_{L,PR(min)} = 2\pi^2 \alpha \beta \quad (4.16)$$

According to equations (4.5) and (4.15), $I_{L,PR(pk)}$ and PR loss with different radius/thickness ratio (F) can be plotted, as shown in Figure 4.9. Based on this result, the optimal ratio could be identified ($F \approx 250$), which aids in determining the most effective ratio for specific operational conditions. Considering the emphasis on employing COTS PRs, this study utilizes the standard PR dimension table provided by PI Ceramics[67], whose maximal F is 50 (mechanical fabrication limitation). Consequently, a PR with a diameter of 20mm and a thickness of 0.2mm ($F = 50$), made from PIC181 material, has been employed.

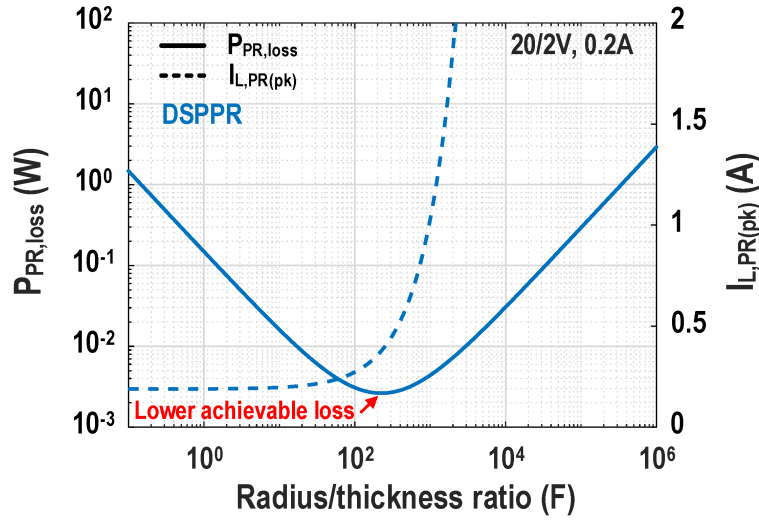


Figure 4.9 PR loss model of the DSPPR converter at 20/2V, 0.2A

4.4.4 PR Mounting Strategy

Piezoelectric materials offer excellent properties, resulting in promising performance in future DC-DC converters; however, the absence of proper packaging and mounting imposes obstacles to unleash their full potential[30], [52]. Given the nature of piezoelectric behavior, PRs are susceptible to stress and contact position over the devices. Incorrect application of force or

misalignment in contact can lead to uneven acoustic wave propagation and, thus, cause a considerable decline in overall performance.

To enable optimal performance, the employed mounting strategy plays a key role. Considering the fairly low Curie temperature and the relatively slim profile of the chosen PR, a non-invasive and heat-free mounting approach is essential, rendering traditional hand-soldering methods inapplicable. As a result, a sandwich-like technique, as illustrated in Figure 4.10, has been adopted following consultations with the foundry.

In Figure 4.10, the PR is connected through two FR-4 PCB plates, where the positive port is joined by a conductive pin and the negative port is directly attached to the circuitry PCB. The copper foils on the plates are expanded to minimize parasitic resistance, while the bottom plate expansion accommodates displacement of the PR that enables centered alignment with the conductive pin. In addition, screws and springs are deployed, facilitating step-less adjustment and locking in the z-direction, thus enabling consistent contact and appropriate stress.

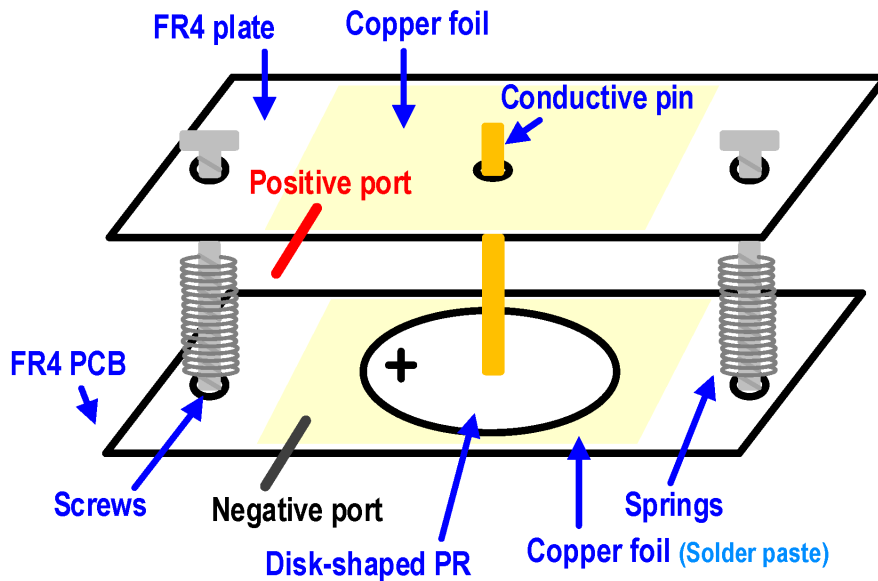
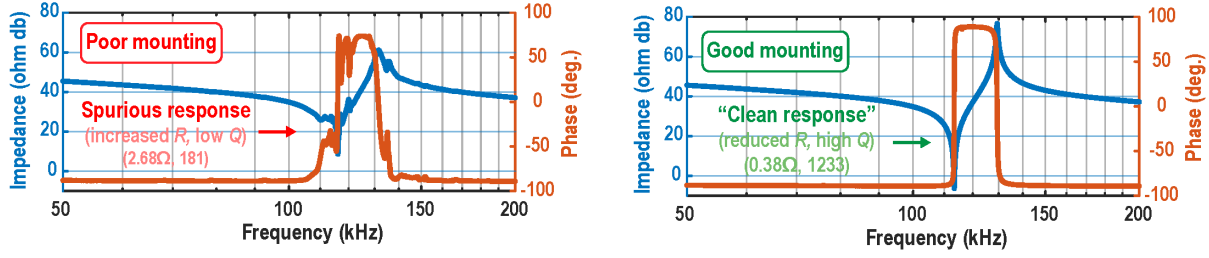


Figure 4.10 Sandwich-like mounting strategy for piezoelectric resonator.



(a) A poor mounting

(b) A good mounting

Figure 4.11 Piezoelectric resonator frequency response.

Figure 4.11 shows the effect of different mounting conditions. Inadequate mounting, as shown in Figure 4.11(a), leads to increased mechanical resistance, R , and spurious responses within the spectrum of interest (inductive region). This degradation in performance can be attributed to excessively light- or heavy-stressed contact, contact misalignment, and macro/micro cracks caused by handling, particularly in slim-PRs. On the other hand, with careful fine-tuning, a clean response can be obtained with proper mounting, as shown in Figure 4.11(b). This optimal response significantly lowers R (reduced from 2.64Ω to 0.38Ω), enabling low-loss operation and enhancing overall system performance. Ultimately, the packaging of PRs remains an important challenge for future work in this area.

4.4.5 Control and Timing

In this study, the DSPPR converter operates under open-loop control, implemented by the C2000 series DSP (F28379D). As shown in Figure 4.2(a), precise control of the turn-on/off timing is essential for stable operation. Here, Figure 4.12 and Table 4.4 illustrate the turn-on/off timing for each signal (S1-S11). Signals (S1,3) and (S2,4) are identical interleaved pairs activated at the beginning of the cycle and deactivated based on voltage regulation, T_{V_o} . Signal S5 engages with ZVS turned on at the beginning of phase 4, $T_{d,S5}$, and disengages according to the duration of

phase 7, $T_{V_{in,PR}}$, where the off-timing ensures that V_{P1} is being charged to $V_{in,PR}$ at phase 7. Signals (S6,7,11) and (8,9,10), operating as out-of-phase pairs within a cycle, initiate with ZVS, $T_{d,BS}$, and terminate at the half, $T_{sw}/2$, or end of the cycle, T_{sw} . Based on Table 4.4, five variables need to be individually controlled in the open-loop testing: 1) cycle period, T_{sw} , 2) turn-on delay of S5, $T_{d,S5}$, 3) turn-on delay for the backside switches (S6-11), $T_{d,BS}$, 4) output regulation timing, T_{Vo} , and 5) $V_{in,PR}$ adjustment timing, $T_{V_{in,PR}}$. Future work will investigate closed-loop control strategies.

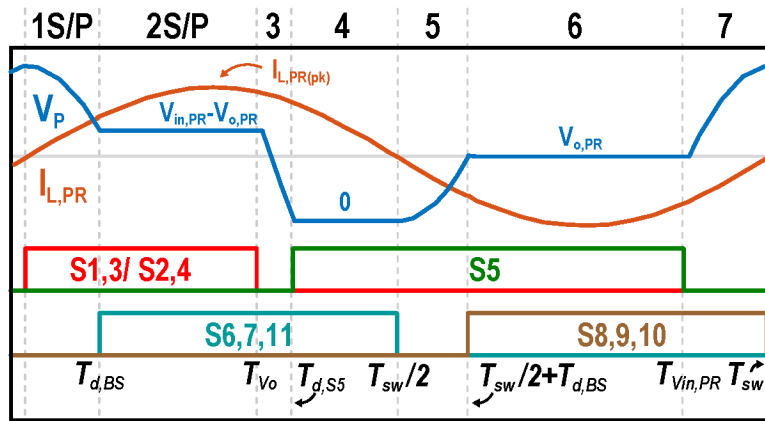


Figure 4.12 Control timing diagram.

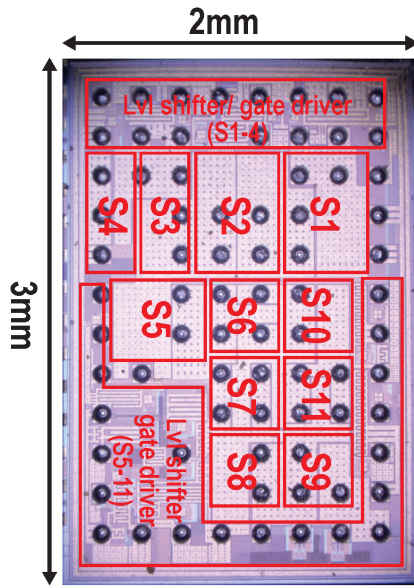
Table 4.4 Timing control of each driving signal.

Signal	Turn-on control	Turn-off control
(S1,3)/ (S2,4)	Beginning of the cycle	V_o regulation (T_{Vo})
S5	ZVS turn on ($T_{d,S5}$)	$V_{in,PR}$ adjustment ($T_{V_{in,PR}}$)
(S6,7,11)	ZVS turn on ($T_{d,BS}$)	Half of the cycle ($T_{sw}/2$)
(S8,9,10)	ZVS turn on ($T_{sw}/2 + T_{d,BS}$)	End of the cycle (T_{sw})

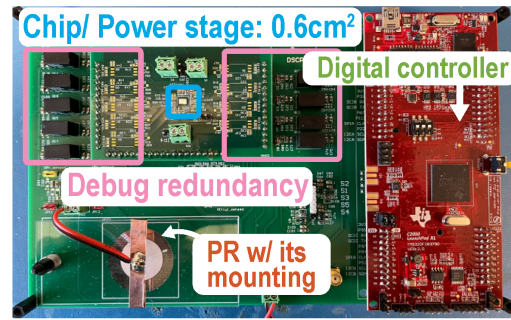
*Timings are referenced to the beginning of the cycle

4.5 Experimental Verification

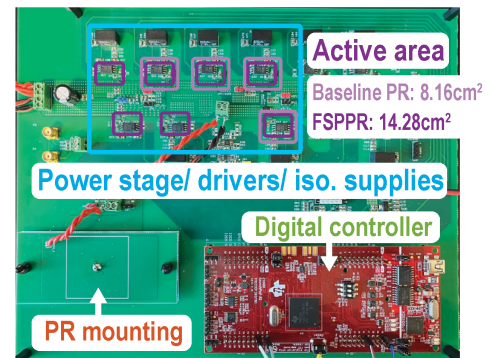
The proposed DSPPR converter utilizes a fully-nMOS design for the power stage and is fabricated in 180 nm BDC process with a die area of 6mm^2 with active switches occupying 70% of the area, as shown in Figure 4.13(a). The chip is designed to operate with 20/0.2mm (diameter/thickness) PIC181 PZT COTS PR, 4x 10 μF 0603 flying/output capacitors, and 9x 150nF 0402 bootstrap capacitors. The circuit implementation is shown in Figure 4.12(b) with a power stage active area of 0.6cm^2 with digital open-loop control adopted. The BVD equivalent parameters of the PR are listed in Table 4.2.



(a) Die micrograph



(b) DSPPR converter in chip design



(c) Co-fabricated FSPPR and Baseline PR-based converters in discrete design

Figure 4.13 Circuit implementations.

Owing to the lack of low-voltage PR-based converters in literature, a discrete prototype, as shown in Figure 4.13(c), which is reconfigurable between baseline PR and FSPPR converters, is implemented using GaN FETs (EPC2214) for direct comparison with prior-art topologies. Here, the active area, including GaN FETs and gate drivers, are 14.3 and 8.2cm^2 , respectively. It can be found that, because of the silicon integration, the IC-based DSPPR design presents a 13-23x smaller active area compared to the discrete implementation.

Here, in comparing the passive footprints of integrated and discrete designs, the integrated DSPPR converter introduces an additional 3x 0603 flying capacitors and 6x 0402 bootstrap capacitors compared to the baseline PR-based converter. Given the same PR (20/0.2mm) utilized, the extra capacitor results in to 7% (4.6mm^3) increase in the passive footprint, where the total passive footprint increases from 64.6mm^3 to 69.2mm^3 , as shown in Figure 4.14.

DSPPR Passive Component Footprint

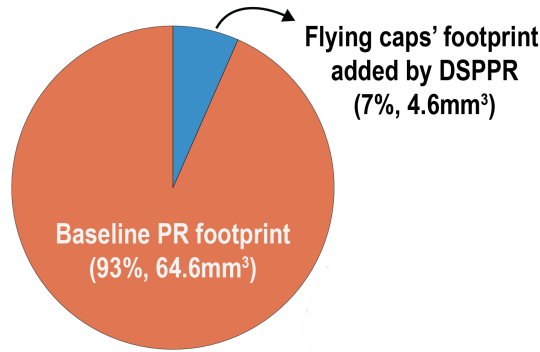


Figure 4.14 Passive footprint comparison.

The steady-state measurements of the DSPPR converter are demonstrated in Figure 4.15(a), revealing that C_{F1} undergoes soft-charging/discharging through $I_{L,PR}$, achieving ZVS across S5-S11, while V_{pp} over the PR is reduced to $V_{in}/2$ and $V_{o,PR}$ is enhanced to $2V_o$, respectively, because of the frontside and backside switched capacitors. In contrast, waveforms for the FSPPR and baseline PR-based converters, as shown in Figure 15(b) and (c) exhibit longer

current circulation intervals along with larger voltage differences between phase 2 and phase 6, $\Delta(V_2 - V_6)$, indicating higher peak resonant current, lower effective PR conversion ratio, VCR_{PR} , and thus, degraded performance.

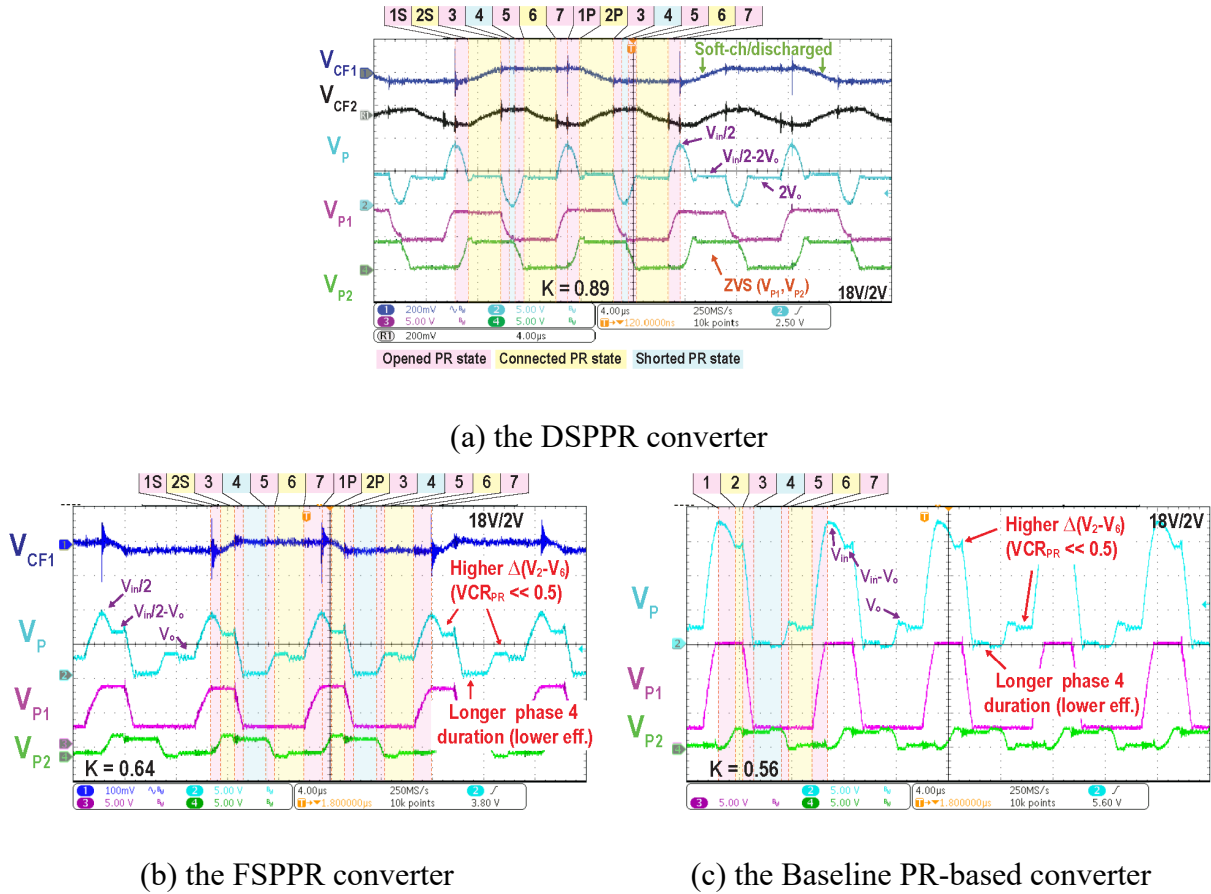
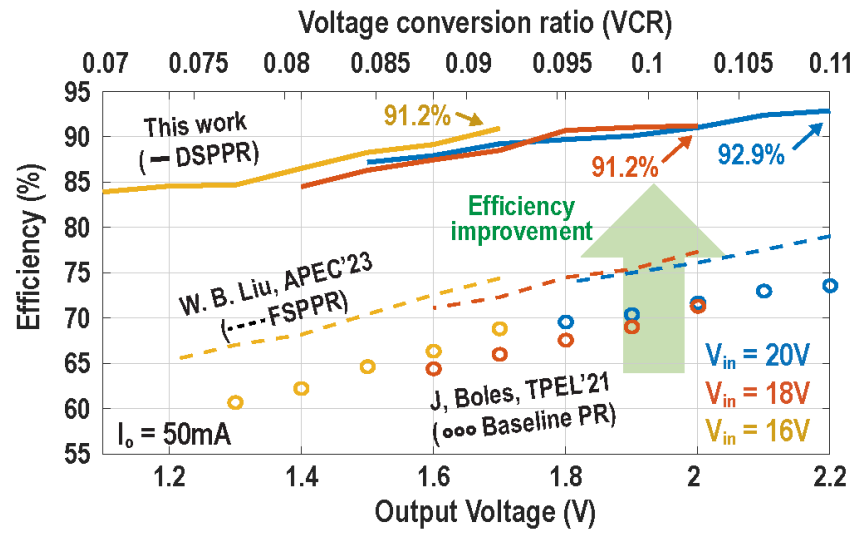


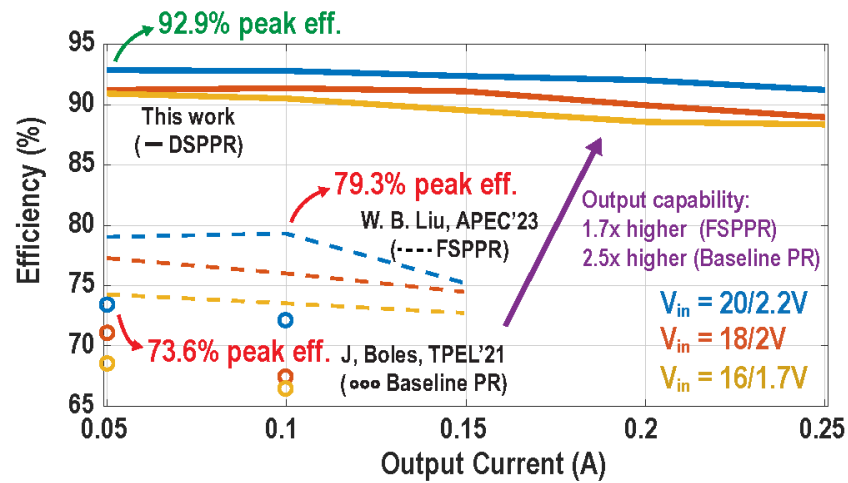
Figure 4.15 Steady-state operation waveforms.

The efficiencies of the PR-based converters are measured under various input, output, and load conditions, as depicted in Figure 4.16, revealing, efficiency improvements of 13.8% and 19.3% under 20/2.2V conditions when compared to the co-designed FSPPR and baseline PR-based converter, respectively, as shown in Figure 4.16(a). Additionally, the DSPPR converter demonstrates up to a 2.5x increase in output capability relative to prior arts, as shown in Figure 4.16(b). The enhanced efficiency and output capacity root from the reduced PR resonant current, $I_{L,PR}$, a result of employing a dual-side hybrid SC configuration. This approach optimizes the PR

utilization factor, K , and effectively reduces the effective PR output current, $I_{o,PR}$. Thus, the related PR vibration loss and conduction loss are both minimized in the proposed DSPPR converter, which outperforms the other two across all test points. Note that, the test terminates by pushing the specific design toward the current limits allowed by the chosen PR where the output voltage decreases over time or unstable oscillations are observed.

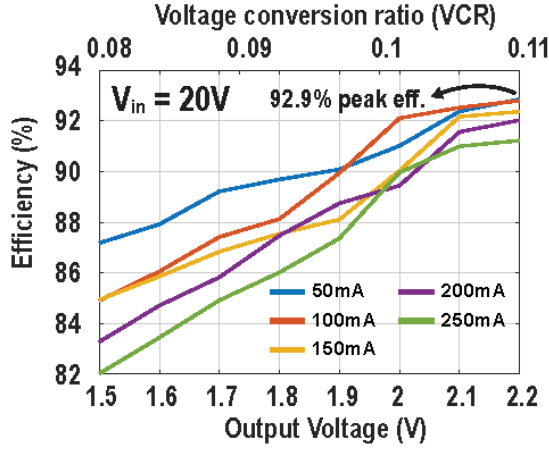


(a) Efficiency at different input/output voltages

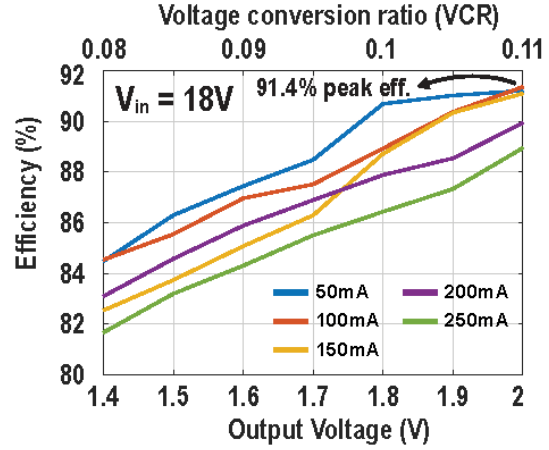


(b) Efficiency at different output current

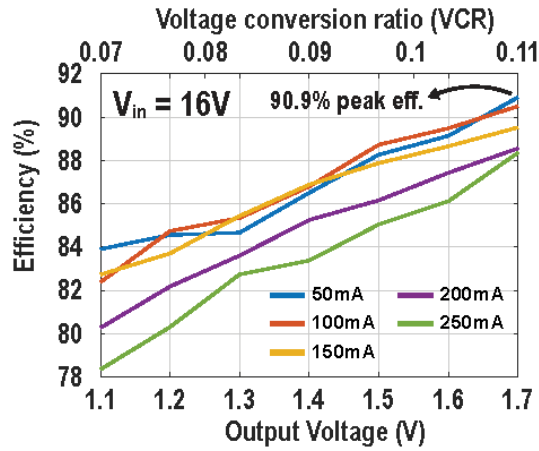
Figure 4.16 Measured efficiency comparison with co-designed PR-based converters.



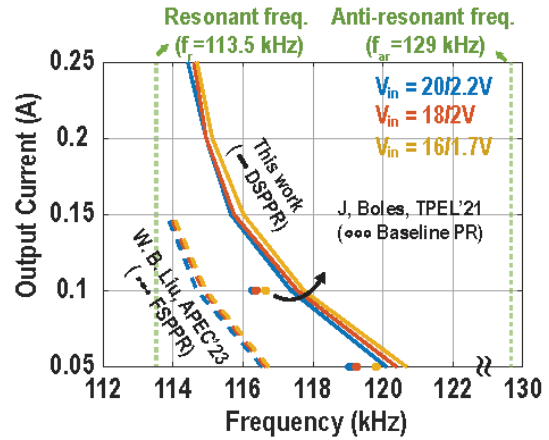
(a) Efficiency at $20V_{in}$



(b) Efficiency at $18V_{in}$



(c) Efficiency at $16V_{in}$



(d) Frequency variation

Figure 4.17 Measured efficiency and frequency variation.

Efficiency measurements of the DSPPR converter across varying output voltages and currents, with a constant input voltage, are detailed in Figure 4.17(a) to (c). The converter demonstrates peak efficiencies of 92.9%, 91.4%, and 90.8% at input voltages of 20V, 18V, and 16V, respectively. Note that, the efficiency improvement against [80] is due to improved PR mounting, which enhanced the quality factor from 649 in [80] to ~ 1233 in this work, illustrated in Table. 4.2 which ultimately reduced the losses in the system. As the output voltage decreases, a monotonic decline in efficiency is observed, attributable to the reduced utilization factor (K),

resulting in an increased $I_{L,PR}$. The frequency variations are also presented in Figure 4.17(b), showcasing a larger utilization of the region between the resonant and anti-resonant frequencies.

Table 4.5 Table of performance comparison

	APEC'20 [77]	TPEL'23 [81]	Discrete test bench		This work
Technology	Discrete				180 HV BCD
Topology	Baseline PR	Dual-Bridge Isolated PR Converter (DB-IPRC)	Baseline PR	Frontside series/parallel PR (FSPPR)	Dual-side series/parallel PR (DSPPR)
PR material	LNO Y + 36° (21/9/0.5mm in LxWxH)	2x PZT C-213 (25/1mm) diameter/thickness	PZT PIC181 (20/0.2mm) diameter/ thickness		PZT PIC181 (20/0.2mm)
V_{in}/V_o range	50V/ 10-40V	12-360V/ 3.3- 346V	16-20V/ 1.1-2.2V		16-20V/ 1.1- 2.2V
Operation frequency	6.3-7.1MHz	~90kH	113-129kHz		113-129kHz
Die/Power SW size	GaN (4x 1.74mm ²)	GaN (8x 58.8mm ²)	GaN (4x 1.82mm ²)	GaN (7x 1.82mm ²)	6mm ²
Active PCB area	N.R.	N.R.	8.16cm ²	14.28cm ²	0.6cm ²
Peak eff. (@ $V_{CR} \leq 0.2$)	~77.5% @50/10V 0.2VCR/ 5W	~91% @ 24/3.3V 0.14VCR/ 0.07W	73.1% @ 20/2.2V 0.11VCR/ 0.11W	78.8% @ 20/2.2V 0.11VCR/ 0.22W	92.9% @20/2.2V 0.11VCR
Efficiency (@ 20/2.2V, 0.05A)	N.R.	~90.7% @ 24/3.3V		78.2%	0.11W
Efficiency (@ 20/2.2V, 0.2A)	N.R.	~77% @ 24/3.3V	N.A.	N.A.	92%

Table 4.5 compares the performance of the proposed DSPPR converter with prior art and co-designed PR-based converters. [77] utilizes an LNO PR, achieving the highest output power due to enhanced current density of LNOs with elevated output voltage but the efficiency is suboptimal. [81] demonstrates excellent performance at low output current scenarios (91% at 24/3.3V, 20mA); however, the efficiency declines sharply as output current increases (55% at

24/3.3V, 200mA) and two PRs are required in this topology. On the other hand, the proposed work shows 92% at a similar scenario, indicating a better output capability with enhanced efficiency. Overall, leveraging the silicon integration and the dual-side hybrid configuration, minimizes silicon area while achieving the highest peak efficiency and the lowest VCRs, at 92.9% efficiency for a 0.11VCR.

4.6 Conclusion

This work presents a dual-side series/parallel PR-based converter implemented in 180 nm BDC technology, striving to improve efficiencies at low VCRs ($VCR \leq 0.1$) while minimizing the silicon and PR area. Incorporating a hybrid approach, popularized in hybrid buck converters, two SCs are merged to the frontside and backside of the baseline PR-based converter, respectively. This configuration enables an optimal operation point of 0.125VCR while placing the PR at the high voltage/low current side, thereby reducing the current stress over PR as well as the current-related losses. Due to the merged SC design, ZVS across S5-11 is maintained and soft-charging of the frontside SC is achieved. In addition, the same operation as the baseline PR-based converter is employed with the self-balanced backside SC, suggesting its compatibility with existing control methods for the PR-based converters. Finally, the system is designed and tested under 16-20/ 1.1-2.2V conditions, revealing a peak efficiency of 92.9%, making a 13%-20% efficiency enhancement, a 13x-23x active area reduction, and a 1.7x-2.5x output capability improvement compared to co-designed PR-based converters.

Acknowledgements

Chapter 4 is based on and mostly a reprint of the following publication:

- W. -C. B. Liu, G. Pillonnet and P. P. Mercier, "8.6 An Integrated Dual-side Series/Parallel Piezoelectric Resonator-based 20-to-2.2V DC-DC Converter Achieving a 310% Loss Reduction," *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2024, pp. 364-366, doi: 10.1109/ISSCC49657.2024.10454471.
- W. -C. B. Liu, G. Pillonnet and P. P. Mercier, " An Integrated Dual-side Series/Parallel Piezoelectric Resonator-based DC-DC Converter," *submitted to IEEE Journal of Solid-State Circuits (invited paper and under review)*.

Chapter 5 Review and Comparison of Low-Voltage-Output High-Step-Down-Ratio Hybrid Switched-Capacitor Piezoelectric-Resonator-based DC-DC Converters

5.1 Review of Hybrid PR-based Converters

To improve the efficiency at low VCRs, various hybrid PR-based converters are proposed[70],[71],[80],[81] and introduced in Chapter 3 and 4. In this section, the four hybrid PR-based converters (Frontside/Backside/Dual-side Series/Parallel and Merge Switched Capacitor PR-based converters) are reviewed along with their baseline PR-based converter are reviewed, as shown in Figure 5.1. The hybrid PR-based DC-DC converters follow the fundamental operating principle of the baseline PR-based converter, yet they incorporate additional switched capacitor(s) that alter the equivalent input and/or output voltage applied to the PR, donated as $V_{in,PR}$ and $V_{o,PR}$ and, as a result, enhance the performance at low VCRs. This section presents the hybrid PR-based converters through generalized operation waveforms, followed by an analysis and generalization of their behavior for comparative evaluation.

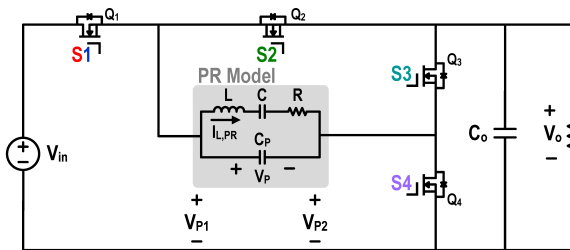


Figure 5.1 Base PR-base Converter.

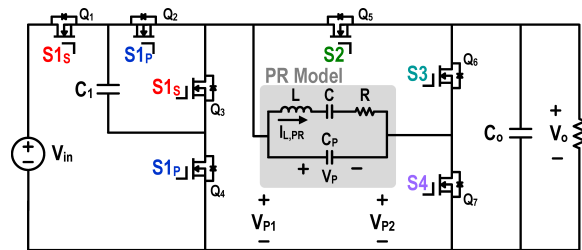


Figure 5.2 Frontside Series/Parallel PR-base Converter (FSPPR).

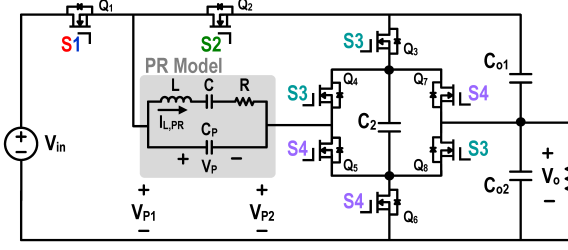


Figure 5.3 Backside Series/Parallel PR-base Converter (BSPPR).

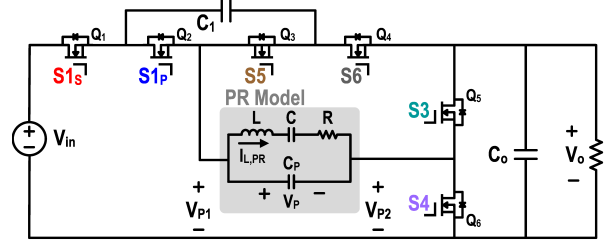


Figure 5.4 Dual-side Series/Parallel PR-base Converter (DSPPR).

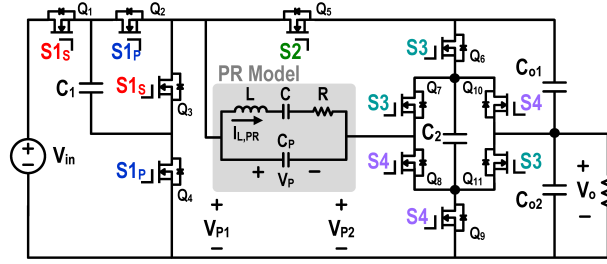


Figure 5.5 Merge Switched Capacitor PR-based converters (MSCPR).

5.1.1 Generalized Operation and Hybrid PR-based Converters

Here, given that this study focuses on VCRs below 0.5, a six-phase sequence of $(V_{in} - V_o, Zero+, V_o)$ is explored which is reported to be one of the most efficient operations [29]. The generalized operation waveforms for hybrid PR-based converters are shown in Figure 5.6, where the converters share the same operation waveforms (V_P , V_{P1} , V_{P2} , and $i_{L,PR}$) yet with different equivalent PR input and output voltage ($V_{in,PR}$ and $V_{o,PR}$), as depicted in Table 5.1. In a cycle, there are seven distinct phases with frontside/merged SC (F/MS) and backside SC (BSC) in series/parallel configurations. The F/MS, adopted in FSPPR, DSPPR, and MSCPR converters, operates in interleaving series and parallel modes between cycles, while the BSC, employed in BSPPR and DSPPR converters, alternates in series or parallel configurations within a cycle.

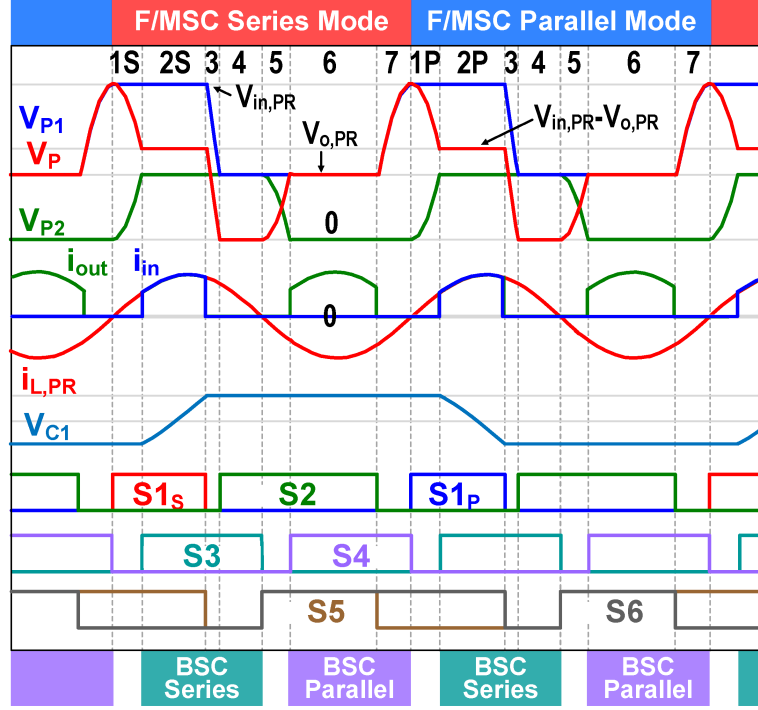


Figure 5.6 Generalized operation waveforms for Step-down PR-based converters. (Compatible with Baseline PR, FSPPR, BSPPR, DSPPR, MSCPR converters)

The connection of PRs can be categorized in three states: (1) opened state, where the PR is opened allowing the PR current, $i_{L,PR}$ to circulate within PR itself while softly charging or discharging C_P ; (2) connected state, in which the PR connects to the input and/or output or both, engaging in energy storage or release and delivering energy to the output; (3) shorted state: where external switches short the PR, forming a freewheeling path to ensure current continuity. For analytical purposes, the equivalent PR input and output voltages are denoted as $V_{in,PR}$, and $V_{o,PR}$, with values varying across different topologies.

Within a cycle, each phase instructs as follows:

- 1) Phase 1S/1P: The PR is opened, causing $i_{L,PR}$ to softly discharge C_P , and thus, leading to a voltage rise in the negative PR node, V_{P2} , until it reaches $V_{o,PR}$.

- 2) Phase 2S/2P: $S3$ is set, activating related switches with zero voltage switching (ZVS), which connects the PR to both input and output, facilitating energy delivery to the output and charging the PR.
- 3) Phase 3: $S1_{S,P}$ is reset, returning the PR to an open state. During this phase, C_P is softly discharged, leading to a decrease of the voltage at the positive PR node, V_{P1} , from $V_{in,PR}$ to $V_{o,PR}$.
- 4) Phase 4: $S2$ is set enabling ZVS for the corresponding switch and establishing a shorted path where $i_{L,PR}$ circulates until its polarity reverses.
- 5) Phase 5: With the PR open, C_P is softly charged by $i_{L,PR}$, leading to a gradual decrease in V_{P2} to 0.
- 6) Phase 6}: $S3$ is set, turning corresponding switches with ZVS that connects the PR to the output and ground. In this connected state, the PR distributes stored energy to the output.
- 7) Phase 7}: The PR returns to the opened state once again, where C_P is soft charged by $i_{L,PR}$, causing V_{P1} to rise until it equals $V_{in,PR}$; thereby, a new cycle is initiated.

Table 5.1 Equivalent PR input/output voltage and peak-to-peak PR voltage swing of hybrid PR-based converters

Topology	$V_{in,PR}$	$V_{o,PR}$	V_{pp}
Baseline PR	V_{in}	V_o	V_{in}
FSPPR	$V_{in}/2$	V_o	$V_{in}/2$
BSPPR	V_{in}	$2V_o$	V_{in}
DSPPR	$V_{in}/2$	$2V_o$	$V_{in}/2$
MSCPR	$(V_{in} + V_o)/2$	V_o	$(V_{in} + V_o)/2$

5.1.1.1 Baseline: Baseline PR-based Converter

The baseline PR-based converter, illustrated in Figure 5.1, consists of four switches configured similarly to a switched-capacitor network found in a three-level buck converter[83] without the output inductor where the SC is replaced by the PR. Unlike the switched capacitor with a fixed 2:1 conversion ratio, this converter supports voltage regulation and zero-voltage switching (ZVS) by operating the PR within its inductive region. The voltage conversion ratio (VCR) spans from zero to 0.5 ($0 \leq \text{VCR} \leq 0.5$) and, at this range, peak efficiency is achieved at a VCR of 0.5, with efficiency decreasing sharply as the VCR moves toward low VCRs, i.e., $\text{VCR} \leq 0.2$ [29]. In the baseline PR-based converter, $V_{in,PR}$ and $V_{o,PR}$ are denoted as V_{in} and V_o , respectively.

5.1.1.2 Variation 1: Frontside Series/Parallel PR-based (FSPPR) Converter

The FSPPR converter, illustrated in Figure 5.2, modifies the baseline PR-based converter by substituting Q_1 with a 2:1 series/parallel frontside switched capacitor (FSC) network, creating a hybrid PR-based converter that is similar to the hybrid buck converter [55-60], [83]. As depicted in Figure 5.6, when, $S1_S$ is set, the switched capacitor, C_1 , is in series with the PR stage and is softly charged by PR inductive current, $i_{L,PR}$; on the other hand, when $S1_P$ is set, C_1 in parallel with the PR stage and is softly discharged by PR inductive current, $i_{L,PR}$. This configuration prevents excessive hard-charging losses during operations. Moreover, with the switched capacitor fixed at $V_{in}/2$, enables an additional 2:1 step-down conversion, allowing the FSPPR converter to keep the equivalent PR voltage conversion ratio, VCR_{PR} , close to 0.5 at lower VCRs, and thus, enhancing efficiency[70]. In addition, ZVS feature is preserved for Q_5 - Q_7 . Here, $V_{in,PR}$ reduces to $V_{in}/2$ owing to the FSC operation and $V_{o,PR}$ stays unchanged as V_o .

5.1.1.3 Variation 2: Backside Series/Parallel PR-based (BSPPR) Converter

The BSPPR converter, illustrated in Figure 5.3, utilizes a similar concept as the FSPPR converter but integrates the 2:1 series/parallel switched capacitor, C_2 , into the backside half-bridge of the baseline PR-based converter. C_2 is controlled by driving signals $S3$ and $S4$ allowing it to operate in series or parallel with the output. Due to this series/parallel arrangement, C_2 is inherently self-balanced to the output voltage, V_o , simplifying control efforts, and shifting the optimal efficiency point to a 0.25 VCR through the extra 2:1 backside switched capacitor (BSC) operation. Moreover, this configuration moves the PR to the high voltage/low current side and, hence, effectively reduces the current stress and I^2R loss within the PR [82]. ZVS across all switches is achieved, further minimizing losses. In the BSPPR converter, $V_{in,PR}$ stays unchanged as V_{in} and $V_{o,PR}$ is boosted to $2V_o$ due to the BSC operation.

5.1.1.4 Variation 3: Dual-side Series/Parallel PR-based (DSPPR) Converter

The DSPPR converter, illustrated in Figure 5.4, employs both frontside SC (FSC) and backside SC (BSC) to the baseline PR-based converter, forming a dual-side series/parallel SC configuration that achieves an optimal efficiency point at a 0.125 VCR. In this setup, FSC operates in a series or parallel configuration with the PR stage controlled by the driving signals, $S1_s$, and $S1_p$, while BSC operates in a series or parallel configuration with the output controlled by the driving signals, $S3$, and $S4$. Additionally, this topology retains all of the benefits from the FSPPR and BSPPR converters, including zero-voltage switching (ZVS), soft charging of C_1 , automatic balancing of C_2 , and reduced PR current stress and losses. Due to the FSC and BSC operations, $V_{in,PR}$ and $V_{o,PR}$ are reduced and boosted to $V_{in}/2$ and $2V_o$ respectively.

5.1.1.5 Variation 4: Merged Switched-Capacitor PR-based (MSCPR) Converter

The MSCPR converter, illustrated in Figure 5.5, couples the merged switched capacitor (MSC), C_1 , to the input and output of the baseline PR-based converter with extra switches that allow the MSC to operate in series or parallel mode, similar to the FSPPR converter. With this MSC operation, the optimal efficiency point is shifted to 0.33 VCR. Moreover, to achieve ZVS across all switches and keep a minimal switch count, the driving strategy is modified, as shown in Figure 5.6, where the asymmetric driving signals, S_5 , and S_6 , are introduced to the MSCPR converter, pushing extra control complexity. Because of the MSC operation, $V_{in,PR}$ reduces to $(V_{in} + V_o)/2$ while $V_{o,PR}$ stays unchanged as V_o .

5.1.2 Topological PR Operation Comparison

Upon examining the general operation, a comparison between hybrid PR-based converters and the baseline PR-based converter is conducted. Utilizing the conservation of charge (CoC) and conservation of energy (CoE), which is extensively applied in Chapter 3 and 4, the voltage conversion range and PR charge transfer utilization (PR utilization) can be derived.

Table 5.2 shows the overall voltage conversion ratio (VCR) range for various hybrid PR-based converters. Additionally, the PR charge utilization for these hybrid PR-based converters is detailed in Table 5.3. By combining the data from Table 5.2 and 5.3, the relationship between PR charge utilization and VCR for the hybrid PR-based converters is illustrated in Figure 5.7.

Table 5.2 Voltage conversion range of different PR-based converters

Topology	VCR		
Baseline PR	0		1/2
FSPPR	0	$\leq \frac{V_o}{V_{in}} \leq$	1/4
BSPPR	0		1/4
DSPPR	0		1/8
MSCPR	0		1/3

Table 5.3 PR charge transfer utilization comparison

	Baseline PR, F/B/DSPPR	MSCPR
K	$\frac{V_{in,PR}}{2(V_{in,PR} - V_{o,PR})}$	$\frac{V_{in}}{2(V_{in} - V_o)}$

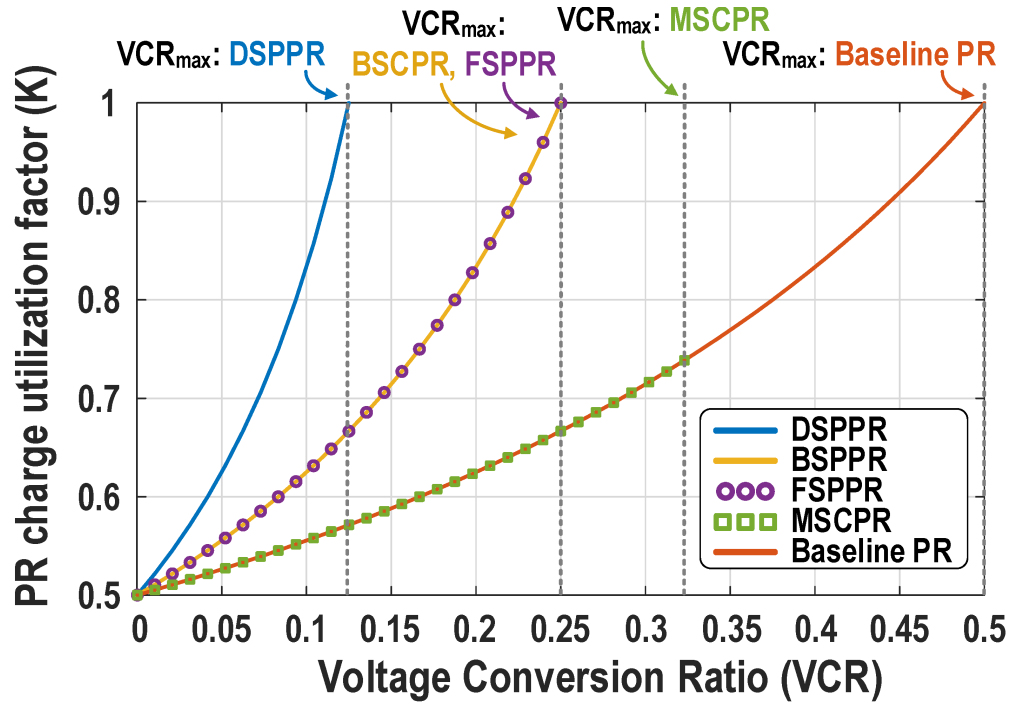


Figure 5.7 PR charge transfer utilization comparison with different conversion ratio.

5.2 Device Size Modelling Framework

In this section, the device sizing model will be presented including, the piezoelectric resonator size/loss model, active device size model, and the capacitor size model. Then, the presented models will be used for topology comparison in the following sections.

5.2.1 Piezoelectric Resonator Loss and Size Scaling Model

To develop a size-based piezoelectric loss model, an initial understanding of how physical parameters (e.g., size, piezoelectric constants) correspond to the equivalent Butterworth-Van Dyke (BVD) model is essential, as introduced in Chapter 3.1. Here, R , L , and C symbolize the mechanical components associated with mechanical vibrations and corresponding loss, while C_p represents the piezo-static capacitor [68] [72].

Before exploring the correlation between the BVD model and the physical parameters, it is crucial to recognize that the vibration modes of PRs can yield varied piezoelectric loss models because of inherent mechanical behavior differences. Given the emphasis on commercially available PRs in this work, disk-shaped PZT PRs have been selected for their regular manufacturing and standard-size availability. Furthermore, to prevent performance deterioration from spurious modes, the radial vibration mode is chosen for its relatively purer frequency response [28] compared to other modes, such as the thickness mode [30].

Here, the BVD model equivalents, defined by physical parameters for a disk-shaped PR operating in radial vibration mode, are detailed in [68] and outlined in equations (5.1)-(5.5)

$$C_p = \epsilon_{33}^T (1 - k_p^2) \frac{A}{l} \quad (5.1)$$

$$C = \frac{2(1 + \sigma^E)}{X_h^2 - (1 - (\sigma^E)^2)} \frac{k_p^2}{1 - k_p^2} C_P \quad (5.2)$$

$$L = \frac{a^2 \rho s_{11}^E (1 - \sigma^E)}{2C_P} \frac{1 - k_p^2}{k_p^2} \frac{X_h^2 - (1 - (\sigma^E)^2)}{X_h^2} \quad (5.3)$$

$$R = \frac{1}{Q_m} \sqrt{\frac{L}{C}} \quad (5.4)$$

$$f_r = \frac{X_h}{2\pi r \sqrt{\rho s_{11}^E (1 - (\sigma^E)^2)}} \quad (5.5)$$

Here, A is the area of the PR, l is the thickness of the PR, r is the radius of the PR, ϵ_{33}^T is the dielectric constant, k_p is the electromechanical coupling factor, σ^E is Poisson's ratio, ρ is the density of the PR material, s_{11}^E is the compliance constant, Q_m is the mechanical quality factor, and X_h is the wave number, which is the solution for the boundary condition of motion displacement in the disk-shaped PR [68].

By substituting equations (5.1) and (5.5) into $I_{L,PR(pk)}$ expression, the peak current, $I_{L,PR(pk)}$, can be rearranged with physical PR parameters, as depicted in equation (5.6). Within this framework, α emerges as a topology-dependent term, exclusively influenced by the topology. In contrast, β is determined by both the physical parameters and the topology. In addition, deriving from equation (5.6), the relationship between $I_{L,PR(pk)}$ and the sizes of PRs can be identified where r and l are the radius and thickness of PRs, respectively.

$$\begin{aligned} I_{L,PR(pk)} &= \pi \left(\frac{P_o}{2KV_{o,PR}} + f_{sw} C_P V_{P(pp)} \right) = \pi \left(\frac{P_o}{2KV_{o,PR}} + \frac{1}{2} \pi N_p \epsilon_{33}^T (1 - k_p^2) V_{P(pp)} \frac{r}{l} \right) \\ &= \pi \left(\alpha + \beta \frac{r}{l} \right) \end{aligned} \quad (5.6)$$

On the other hand, by inserting equations (5.2) and (5.3) into (5.4), the mechanical resistance, R , can be represented by the physical parameters as equation (5.7). Here, R purely depends on material constants and the relationship between R and the sizes of PRs can also be identified.

$$R = \frac{1}{Q_m} \sqrt{\frac{L}{C}} = \frac{1}{\pi Q_m} \frac{X_h^2 - (1 - (\sigma^E)^2)}{2k_p^2 X_h \varepsilon_{33}^T} \sqrt{\frac{\rho s_{11}^E (1 - \sigma^E)}{(1 + \sigma^E)}} \frac{l}{r} \quad (5.7)$$

$$= \gamma \frac{l}{r}$$

Furthermore, equations (5.6) and (5.7) can be incorporated into PR loss expression with the radius and thickness ratio definition (F ratio, $F = r/l$). Then, the piezoelectric loss model for the disk-shaped, radial mode PRs can be expressed as equation (5.8), which draws the same conclusion as equation (4.15) in Chapter 4.

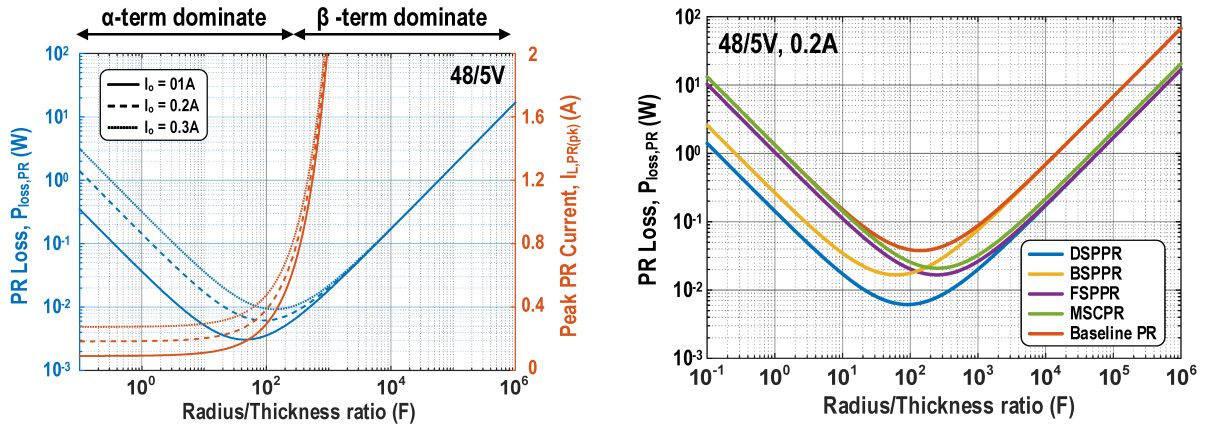
$$P_{loss,PR} = \frac{1}{2} R I_{L,PR(pk)}^2 = \frac{\pi^2 \gamma}{2 F} (\alpha + \beta F)^2 \quad (5.8)$$

According to equation (5.8), it can be found that, given topology and load condition, there is an optimal radius and thickness ratio ($F = \alpha/\beta$) leading to a minimal PR loss, as shown in equation (5.9), which is obtained by solving $\partial(P_{PR,Loss})/\partial F = 0$. Interestingly, the minimal PR loss is proportional to the product of α , β , and γ .

$$P_{loss,PR(min)} = 2\pi^2 \alpha \beta \quad (5.9)$$

Given a specific topology and operational conditions, $I_{L,PR(pk)}$ and $P_{loss,PR}$ can then be plotted, as shown in Figure 5.8(a) where operation conditions of 48/5V with different load conditions are specified for the DSPPR converter. Here, as analyzed, there is a minimal PR loss at a given condition when $F = \alpha/\beta$. Moreover, the figure indicates that as the F ratio is small, the α term (a topology/operation-dependent factor) predominantly influences both $I_{L,PR(pk)}$ and $P_{loss,PR}$

values. On the other hand, as the F ratio increases, the β term becomes more influential on both $I_{L,PR(pk)}$ and $P_{loss,PR}$, making both $I_{L,PR(pk)}$ and $P_{loss,PR}$ load independent. This is attributed to a larger piezo-static capacitor, C_p coming from an increased r/l ratio, which requires substantial charges/current for capacitor charging/discharging during opened-state operations, known as Q_{open} or Q_{ZVS} in [29], [70], [82], [83]. Consequently, both current and PR loss become independent of load in this scenario. Figure 5.8(a) also reveals that selecting a proper PR size that facilitates α -dominant operation can effectively mitigate excessive PR current, $I_{L,PR(pk)}$, reducing both PR vibration loss, $P_{loss,PR}$, and the current-related conduction losses in power switches. Note that the calculation is based on the physical parameters obtained from [67].



(a) Example: PR loss model for DSPPR converter at 48/5V

(b) PR loss model comparison for various hybrid PR-based converters at 48/5V, 0.2A

Figure 5.8 PR loss and size scaling model.

The PR loss model is applicable across various topologies, as demonstrated in Figure 5.8(b) with specified conditions (48/5V, 0.2A). Among these, the DSPPR converter achieves the lowest possible loss, as identified in [80]. Subsequently, while both the BSPPR and FSPPR converters exhibit similar levels of minimum loss, the PR size in the BSPPR converter can be smaller than that in the FSPPR converter, owing to a lower optimal F ratio. Conversely, the baseline PR

converter exhibits the highest minimum loss, corroborated by Figure 5.7, which shows that the baseline PR converter has the least effective utilization of charges at low VCRs ($VCR \leq 0.125$).

5.2.2 Active Switch Loss and Size Scaling Model

Prior to delving into the size and loss model, it is important to highlight the trade-off between switch performance and breakdown voltage rating. [84]-[86] elucidate the relationships among switch size, A_{sw} , on-resistance, R_{on} , and breakdown voltage, V_{bd} . This general relationship, applicable to lateral-type switches, is formulated as equation 5.10, where G_{sw} , V_{bd} , and $\alpha_{A_{sw}}$ are the conductance, breakdown voltage, and scaling coefficient of a switch.

$$A_{sw} \propto G_{sw} V_{bd}^{\alpha_{A_{sw}}} \quad (5.10)$$

The switch parameters (e.g., on-resistance, R_{on} , output capacitance, C_{oss} , and gate charge, Q_g) are typically related to the active switch area, A_{sw} , and breakdown voltage, V_{bd} . Thus, the unit on-resistance, $R_{on(unit)}$, output capacitance, $C_{oss(unit)}$, and gate charge, $Q_{g(unit)}$ can be defined by V_{bd} and the final value of R_{on} , C_{oss} , and Q_g are scaling with the active switch area, A_{sw} . Here, R_{on} , C_{oss} , and Q_g can be written as equations (5.11)-(5.13), where α_x , β_x , and γ_x are corresponding scaling coefficients for the specific parameters and i -th donates as a specific switch in the circuit.

$$R_{on(i)} = \frac{R_{on(unit)}}{A_{sw(i)}^{\gamma_R}} = \frac{\alpha_R V_{bd(i)}^{\beta_R}}{A_{sw(i)}^{\gamma_R}} \quad (5.11)$$

$$C_{oss(i)} = C_{oss(unit)} A_{sw(i)}^{\gamma_C} = \alpha_C V_{bd(i)}^{\beta_C} A_{sw(i)}^{\gamma_C} \quad (5.12)$$

$$Q_{g(i)} = Q_{g(unit)} A_{sw(i)}^{\gamma_Q} = \alpha_Q V_{bd(i)}^{\beta_Q} A_{sw(i)}^{\gamma_Q} \quad (5.13)$$

To validate the switch parameter scaling models equations (5.11)-(5.13), switches from EPC GaN series are selected for their compact packaging, which more accurately represents the actual switch area compared to other standard packaging, i.e., TO-220, TO-24, etc. The model fitting results are shown in Figure 5.9 where R_{on} , C_{oss} , and Q_g are plotted against V_{bd} and A_{sw} . In general, an increase in A_{sw} leads to a decrease in R_{on} while C_{oss} and Q_g tend to increase, as illustrated in Figure 5.9. This implies that, for the i-th switch, there must exist an optimal area leading to minimal losses by trading off R_{on} , C_{oss} , and Q_g values. Note that, the switch size and parameters in Figure 5.9 are obtained from the datasheets with the values in typical corners.

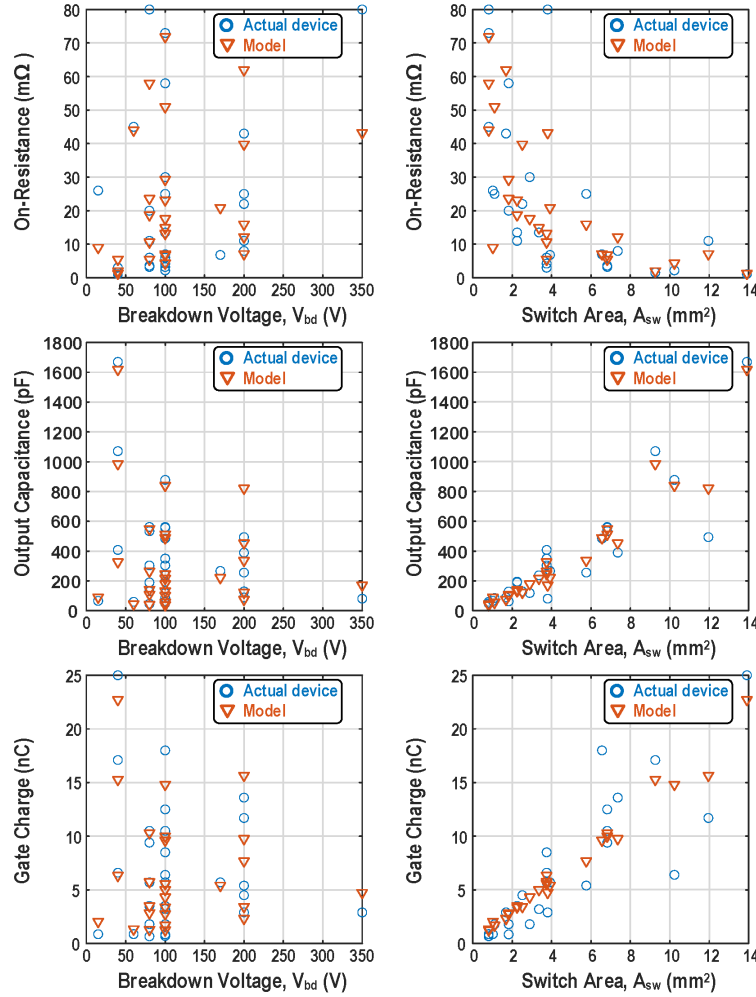


Figure 5.9 Analysis of switch parameter scaling models: EPC GaN switches.

With the scaling model, the loss model of the i -th switch can be built as well, as shown in equation (5.14). Here, the losses include conduction loss, hard-switching loss, and driving loss. By substituting equations (5.11)-(5.13) into equation (5.14), the loss model becomes a function of the V_{bd} and A_{sw} of the i -th switch along with operating conditions (I_{rms} , V_{ds} , V_{gs} , and f_{sw}). This model turns out to be a powerful function in optimizing the converter performance and comparing different topologies, which will be revisited in the next section.

$$P_{loss,sw(i)} = R_{on(i)} I_{rms(i)}^2 + C_{oss(i)} V_{ds(i)}^2 f_{sw} + Q_{g(i)} V_{gs(i)} f_{sw} \quad (5.14)$$

5.2.3 Capacitor Size Scaling Model

In evaluating the size of a capacitor size, the size is directly dictated to the energy capacity by assuming the same energy density in the capacitor. With this assumption, the capacitor sizing model can be written as equation (15) where $V_c(i)$, C_i , and V_i are the area, capacitance, and voltage of the i -th capacitor, respectively.

$$Area_{C(i)} \propto C_i V_i^2 \quad (5.15)$$

Here, once a reference capacitor is selected, the other capacitors can be scaled accordingly. For example, if a 10 μ F/16V 0603 MLCC (size: 1.6x0.8x1mm³) capacitor is chosen as a baseline capacitor, a 20 μ F/16V capacitor is twice in size of the reference capacitor given the same energy density.

5.3 Topological Modeling and Comparison

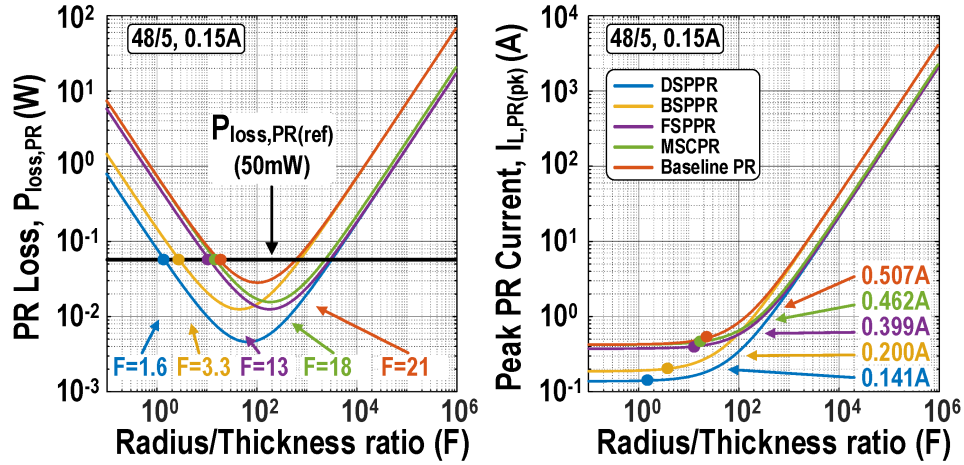
Topological comparisons typically fall into two primary categories: 1) power density at the same efficiency, and 2) maximum achievable efficiency performance at a given size of the main

component, i.e., the PR size in this work. This section demonstrates both approaches to provide insights for the comparison.

5.3.1 Power Density Comparison

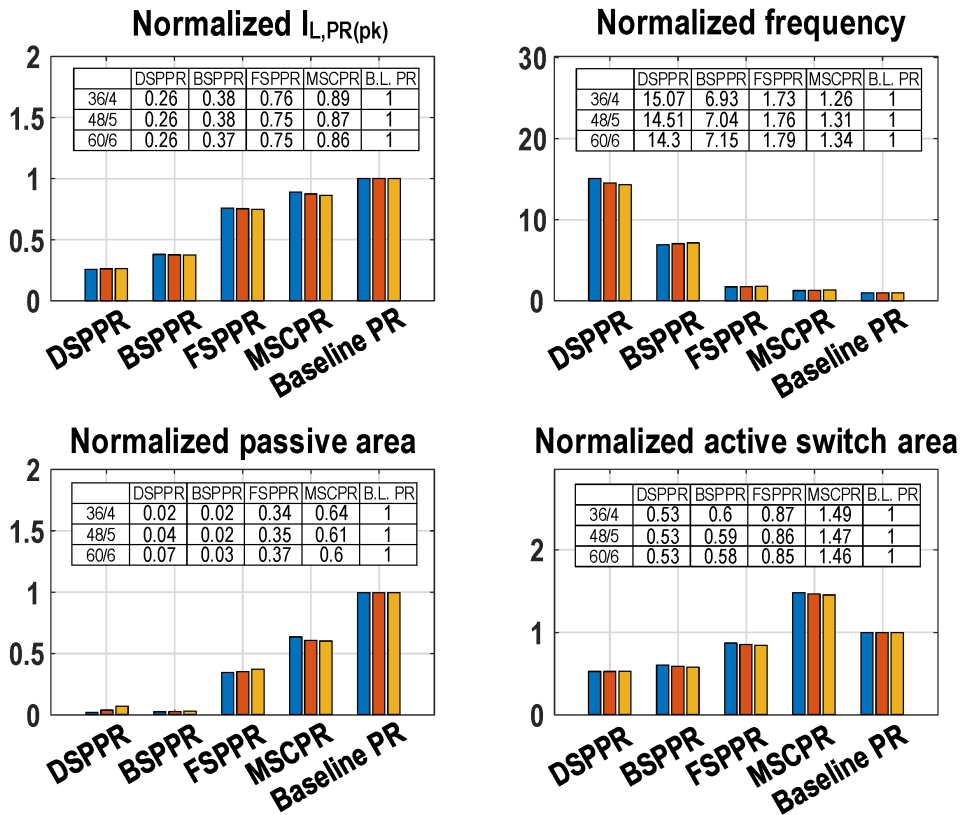
To ensure a fair comparison of power density, the efficiency is assumed to be the same for all converters. In addition, considering the variation in the number of active switches across converters, co-optimization with the PR loss model (Chapter 5.2.1) and switch loss model (Chapter 5.2.2) poses challenges. Consequently, this comparison assumes an equally distributed loss between PR loss, $P_{loss,PR}$, and total switch loss, $P_{loss,sw}$ for all converters with matched efficiency performance. Also, since this work focuses on the radial vibration mode, the thickness of the PR in each converter is presumed to be the same where the PR loss model is sized with the radius of the PR.

Here, the power density comparison is conducted under conditions of (36/4, 48/5, 60/6)V, 0.15A with an overall converter efficiency of 90%, where losses are evenly split between the PR and active switches. Figure 5.10(a) presents the PR loss model comparison at 48/5V and 0.15A conditions, utilizing a PR loss reference, $P_{loss,PR(ref)}$ to represent the PR loss. This comparison reveals that, for a specific PR loss (50mW), each topology yields a unique size ratio, with $I_{L,PR(pk)}$ values distinctly mapped. In this figure, the hybrid PR-based converter presents reduced current stress, allowing them to operate at the same loss with a smaller PR (smaller F ratio). Notably, for a fixed thickness, the DSPPR converter presents the smallest ratio and $I_{L,PR(pk)}$ implying the minimal size and highest resonant frequency along with a reduced current stress over the PR.



(a) PR loss model example with the same loss: 48/5V, 0.15A

Power Density Comparison @ [(36/4V), (48/5V), (60/6V)], 0.15A



(b) Power density comparison results at given operation conditions

Figure 5.10 Power density comparison at 36/4V, 48/5V, and 60/6V with 0.15A output current and 90% efficiency where the loss is evenly distributed to the PR and switches.

After the PR loss and size are analyzed, the total active switch size can be optimized individually for each topology with equation (5.15). In switch size optimization, two things need to be guaranteed: 1) the total switch loss across all converters needs to be the same and 2) the total switch size should be as small as possible for each topology. Hence, the objective function and constraints for the optimization can be expressed as equation (5.16), where the goal is to find a set of switch area solutions, $[A_1, A_2 \dots A_i]$, that minimizes the total area while meeting the loss requirement where the A_{Lo} and A_{Up} are the lower and upper area limit. Various heuristic algorithms can be applied to find the global optimization [87]-[92], i.e. generic algorithm (GA), evolutionary algorithm (EA), simulated annealing (SA)...etc. In this work, the MATLAB built-in fmincon function is employed, which is a multivariable nonlinear programming solver. Note that, the gate driving voltage, $V_{gs(i)}$, is set to be 5V in the following analyses.

$$f(A)_{obj} = \sum_{i=1}^n A_i \quad (5.16)$$

$$\min f(A) \text{ such that } \begin{cases} A_{Lo} \leq A_i \leq A_{Up} \\ P_{loss,target} = P_{loss,sw}(A) \end{cases}$$

Where,

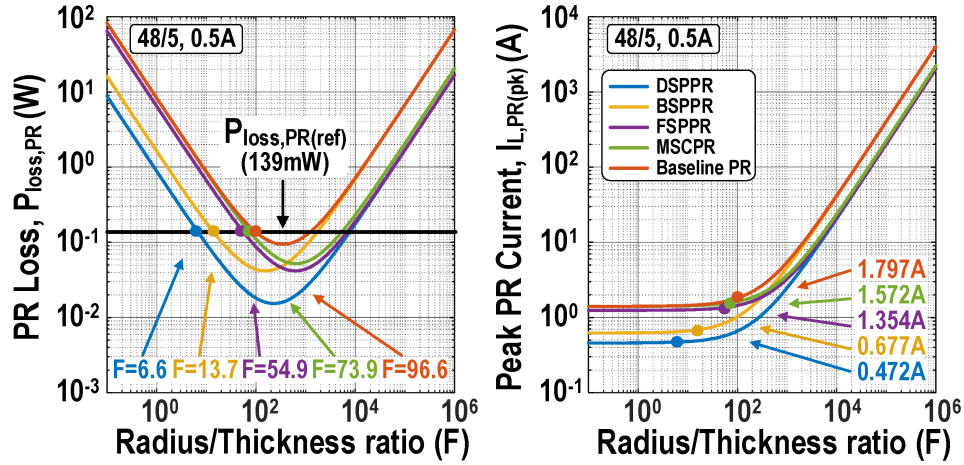
$$P_{loss,sw}(A) = \sum_{i=1}^n (R_{on(i)} I_{rms(i)}^2 + C_{oss(i)} V_{ds(i)}^2 f_{sw} + Q_{g(i)} V_{gs(i)} f_{sw})$$

$$= \sum_{i=1}^n \left(\frac{\alpha_R V_{bd(i)}^{\beta_R}}{A_{sw(i)}^{\gamma_R}} I_{rms(i)}^2 + \frac{\alpha_C V_{bd(i)}^{\beta_C}}{A_{sw(i)}^{\gamma_C}} V_{ds(i)}^2 f_{sw} + \frac{\alpha_Q V_{bd(i)}^{\beta_Q}}{A_{sw(i)}^{\gamma_Q}} V_{gs(i)} f_{sw} \right)$$

The optimization results for the power density comparison, assuming matched overall loss (90% overall efficiency) at 48/5V, 0.2A conditions, are illustrated in Figure 5.10 (b). This figure benchmarks four key metrics: 1) normalized $I_{L,PR(pk)}$, 2) normalized (resonant) frequency, 3)

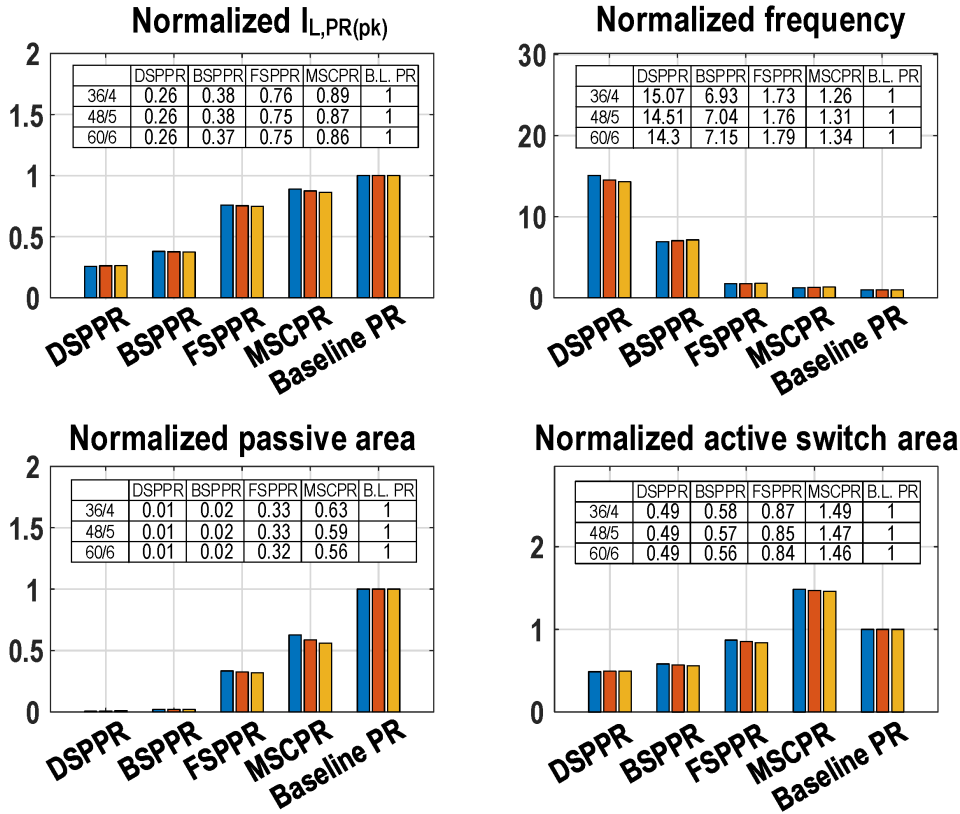
normalized passive area, and 4) normalized active switch area, all relative to the baseline PR-based converter with normalized value marked. The normalized $I_{L,PR(pk)}$ is obtained directly from PR loss model, as an example illustrated in figure 5.10(a) that is mapped from the corresponding F ratio for a specified PR loss. Similarly, the normalized frequency is determined by the F ratio with fixed thickness. The normalized passive area encompasses both the PR and flying capacitor sizes, excluding the output capacitor size because the capacitor size is proportional to the voltage rating, as shown in equation (5.15). The active switch area is optimized based on the model equation (5.16) with switches accounting for half of the total loss and aiming for minimized size. According to Figure 5.10 (b), the DSPPR converter shows excellent balance in passive and active footprints with reduced $I_{L,PR(pk)}$ at a low conversion ratio.

Aside from the analysis at 48/5V, 0.15A conditions, scenarios involving higher currents are also of interest as they lead to increased PR/switch loss, potentially altering optimization outcomes. Thus, conditions of 48/5V, 0.5A with an efficiency of 90% and evenly distributed loss between the PR and switches are depicted in Figure 5.11. Notably, despite differences in normalized values between the 0.15A and 0.5A scenarios, the normalized current and frequency ratios remain consistent across converters. In high output current scenarios, hybrid PR-based converters, particularly the DSPPR and BSPPR, exhibit a significant decrease in $I_{L,PR(pk)}$ (absolute value), attributed to their merged SC(s) and the backside SC configuration that places the PR on the high voltage/low current side, effectively managing the output current. Due to the current reduction, both the passive and active areas of the hybrid PR-based converters become advantageous compared to the baseline PR-based PR converter.



(a) PR loss model example with the same loss: 48/5V, 0.5A

Power Density Comparison @ [(36/4V), (48/5V), (60/6V)], 0.5A



(b) Power density comparison results at given operation conditions

Figure 5.11 Power density comparison at 36/4V, 48/5V, and 60/6V with 0.5A output current and 90% efficiency where the loss is evenly distributed to the PR and switches.

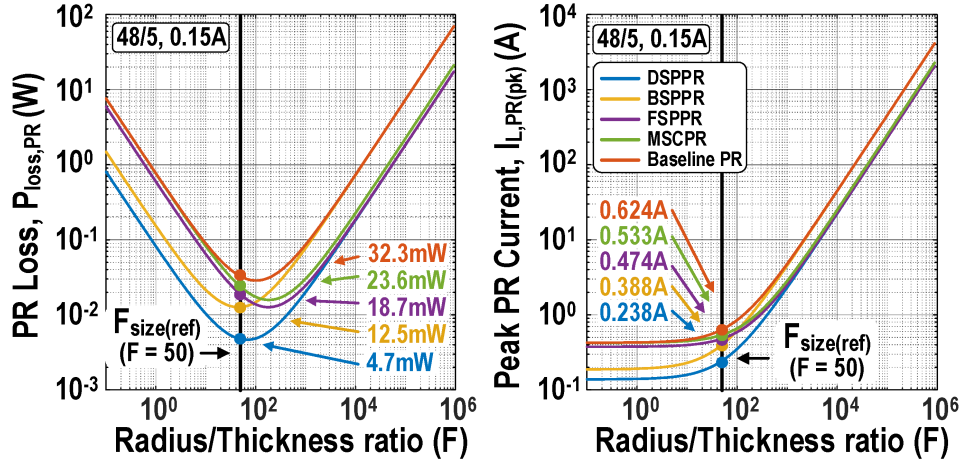
5.3.2 Maximum Achievable Efficiency Comparison

In the comparison of maximum achievable efficiency, the size of the PR is predetermined, with subsequent optimization of switch sizes aimed at minimizing loss. Similar to the power density comparison, this approach utilizes both the loss/size models of PR, equations (5.8) and (5.14). As analyzed in Chapter 5.2.1, a higher F ratio puts the PRs to operate in the β -term dominate region (to the right of the minimum PR loss curve in Figure 5.8(a)) leading to excessive $I_{L,PR(pk)}$. Thus, for this analysis, the F ratio is intentionally set within the α -term dominate region (to the left of the minimum PR loss in Figure 5.8(a)). Moreover, because of the consistent F ratio, all the physical parameters of the PR across each converter remain identical, including f_{sw} , C_P , and so on.

Figure 5.12(a) shows the PR loss model with a F ratio of 50 at 48/5V, 0.15A conditions. With F ratio specified, the individual PR loss and corresponding $I_{L,PR(pk)}$ can be mapped to the figure. In this scenario, the hybrid PR-based converters exhibit lower losses and reduced current due to either enhanced utilization and equivalent PR output voltage, $V_{o,PR}$, or a reduced PR voltage swing, V_{pp} , as detailed in equation (5.6).

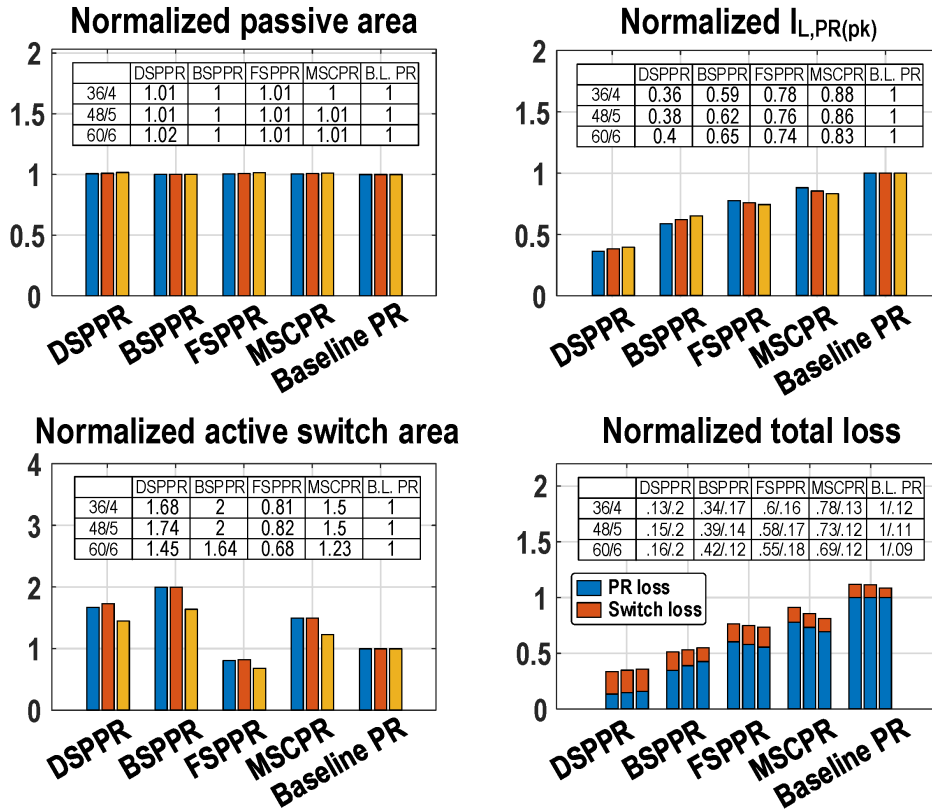
With the PR loss/size model established, optimization for the active switch loss and area is conducted. Unlike the power density optimization, which aims to minimize switch area while equating overall loss, this optimization seeks to minimize the total loss irrespective of area. Hence, the objective function is formulated as equation (5.17), with the intention of identifying a set of area solutions, $[A_1, A_2 \dots A_i]$, that minimizes the overall loss. Then, the multivariable nonlinear programming solver, `fmincon`, from the MATLAB library is applied. It is important to note that the function, $P_{loss,sw}(A)$, referenced in equation (5.17) is identical to that in equation (5.18)

$$f(A)_{obj} = P_{loss,sw}(A), \quad \min f(A) \text{ such that } \{A_{Lo} \leq A_i \leq A_{Up} \quad (5.17)$$



(a) PR loss model example with the same PR size: 48/5V, 0.15A

Efficiency Comparison @ [(36/4V), (48/5V), (60/6V)], 0.15A



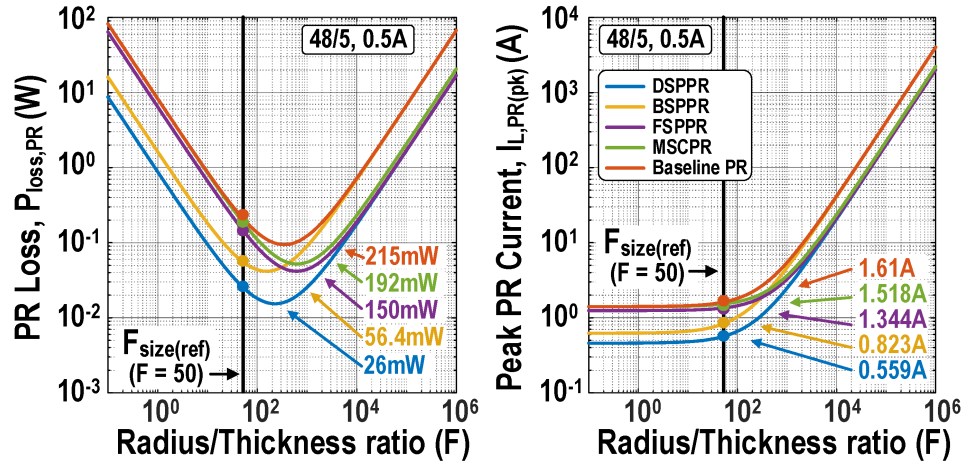
(b) Maximum achievable efficiency comparison results at given operation conditions

Figure 5.12 Maximum achievable efficiency comparison results at given operation conditions

(36/4V, 48/5V, and 60/6V with 0.15A output current and F ratio of 50.

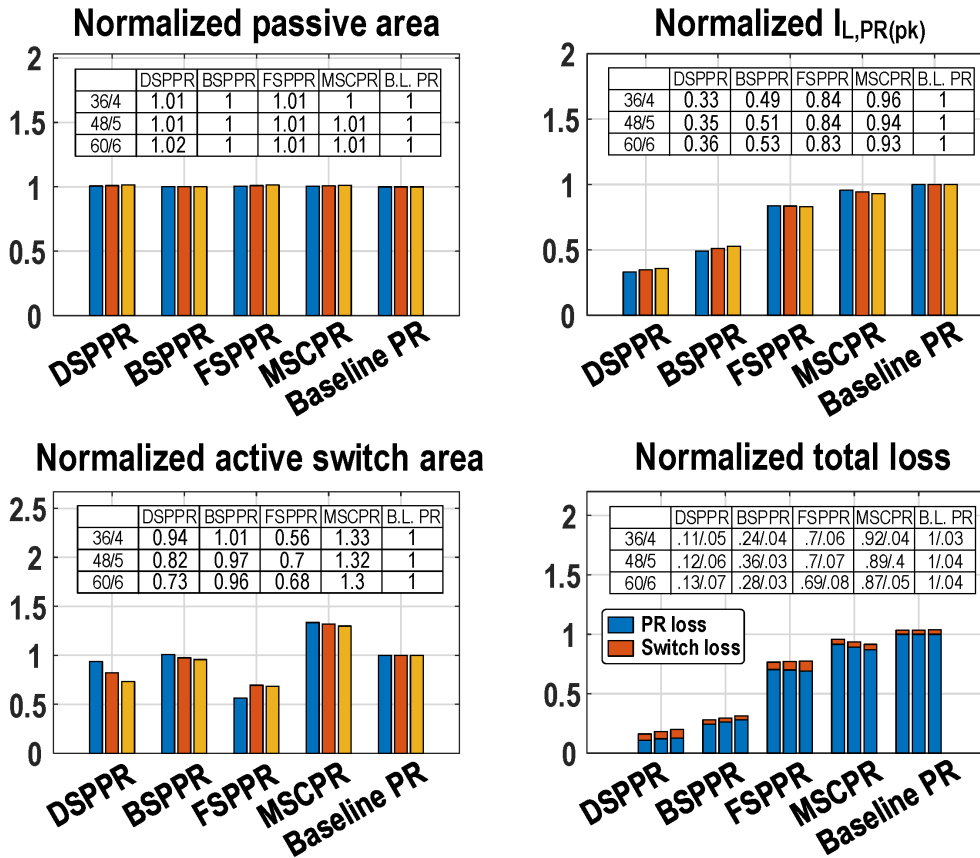
The comparison results are illustrated in Figure 5.12(b), emphasizing four metrics: 1) normalized passive area, 2) normalized $I_{L,PR(pk)}$, 3) normalized active switch area, and 4) normalized total loss. These metrics are benchmarked against the baseline PR-based converter values, with the exception of the loss, which is normalized to the PR loss in the baseline converter rather than the total loss. The normalized passive areas of all PR-based converters are closely matched, with slight variations attributed to flying capacitors, as the PR size largely determines the overall passive area. For normalized $I_{L,PR(pk)}$, the hybrid converters consistently exhibit reduced current stress compared to the baseline converter, as shown in Figure 5.12(a). Regarding the normalized switch area, due to a higher switch count, the hybrid PR-based converters typically show a higher area to reduce the on-resistance created by the stacked switch path, except for the FSPPR converter where the switches stacked at high voltage/low current size minimizing the impact of switch stacking. Finally, the maximum achievable efficiency is calculated, and the hybrid PR-based converters present better efficiency performances compared to the baseline PR-based converter. From the normalized bar figure, even though the loss in the active switch tends to occupy a higher portion of the total loss in the hybrid PR-based converters, particularly in the DSPPR converter owing to more switches, the notable reduction in PR vibration loss outweighs the increased switch losses, thereby rendering better efficiency at low VCRs.

Another comparison can also be made with a higher output current ($I_o = 0.5A$), as shown in Figure 5.13(a). In this scenario, $I_{L,PR(pk)}$ becomes significant and predominately contributes the I^2R loss to the system, where $I_{L,PR(pk)}$ is notably higher than in the (48/5V, 0.15A) case, as shown in Figures 5.12(a) and 5.13(a). This impact can be observed from Figure 5.13(b) that hybrid PR-based converters exhibit reduced normalized switch areas due to the reduced normalized $I_{L,PR(pk)}$ compared to the 0.15A scenario. Particularly, the DSPPR and BSPPR converters showcase a



(a) PR loss model example with the same PR size: 48/5V, 0.5A

Efficiency Comparison @ [(36/4V), (48/5V), (60/6V)], 0.5A



(b) Power density comparison results at given operation conditions

Figure 5.13 Maximum achievable efficiency comparison results at given operation conditions (36/4V, 48/5V, and 60/6V with 0.15A output current and F ratio of 50.

smaller total switch area compared to the baseline PR-base converter in this scenario (high output current case). This demonstrates the advantage of positioning the PR on the high voltage/low current side, as seen with the DSPPR and BSPPR converters, effectively lowering $I_{L,PR(pk)}$ and associated losses. Consequently, due to the reduced current and related loss, the DSPPR and BSPPR converters can be much smaller than the other PR-based converters.

5.3.3 Summary

According to the analysis of power density and maximum efficiency, it is observed that, under specific conditions, a topology with a lower $I_{L,PR(pk)}$ typically demonstrates a better performance. That is, with a reduced $I_{L,PR(pk)}$, a converter can generally achieve a smaller area and/or higher efficiency. Here, $I_{L,PR(pk)}$ can be rewritten as equation (5.18). Given a particular PR size, there are three strategies to reduce $I_{L,PR(pk)}$: 1) reducing the equivalent PR output current, $I_{L,PR(pk)}$, 2) enhancing the PR charge utilization factor, K , and 3) minimizing the peak voltage swing of the PR in a cycle, V_{pp} . The best way is to achieve three of them at the same time; however, it is often hard to have all of them simultaneously. Here, compared to the baseline PR-based converter, the hybrid PR-based converters obtained a reduced current by:

- 1) The MSCPR converter lowers $I_{L,PR(pk)}$ by adjusting V_{pp} from V_{in} to $(V_{in} + V_o)/2$.
- 2) The FSPPR converter reduces $I_{L,PR(pk)}$ by setting V_{pp} to $V_{in}/2$ (by half) while increasing K value.
- 3) The BSPPR converter decreases $I_{L,PR(pk)}$ by reducing $I_{o,PR}$ by half and improving K value.
- 4) The DSPPR converter minimize $I_{L,PR(pk)}$ by halving both $I_{o,PR}$, V_{pp} while enhancing K value.

$$I_{L,PR(pk)} = \pi \left(\frac{I_{o,PR}}{2K} + f_{sw} C_P V_{pp} \right) \quad (5.18)$$

With a general idea that "the lower $I_{L,PR(pk)}$ is, the better performance will be", the topology selections based on operation conditions and PR size can be drawn. Figure 5.14 illustrates examples of best topology at different operation conditions based on the "minimal current rule" (minimal $I_{L,PR(pk)}$). Notably, at different VCRs, the best topology is different due to the difference in operable VCR range and $I_{L,PR(pk)}$ reduction strategy. Note that, the PR thickness is selected to be 0.4mm for 400V input voltage because of the dielectric breakdown strength of PR, which is typical $1kV/mm$ for PZT materials as advised by the foundry.

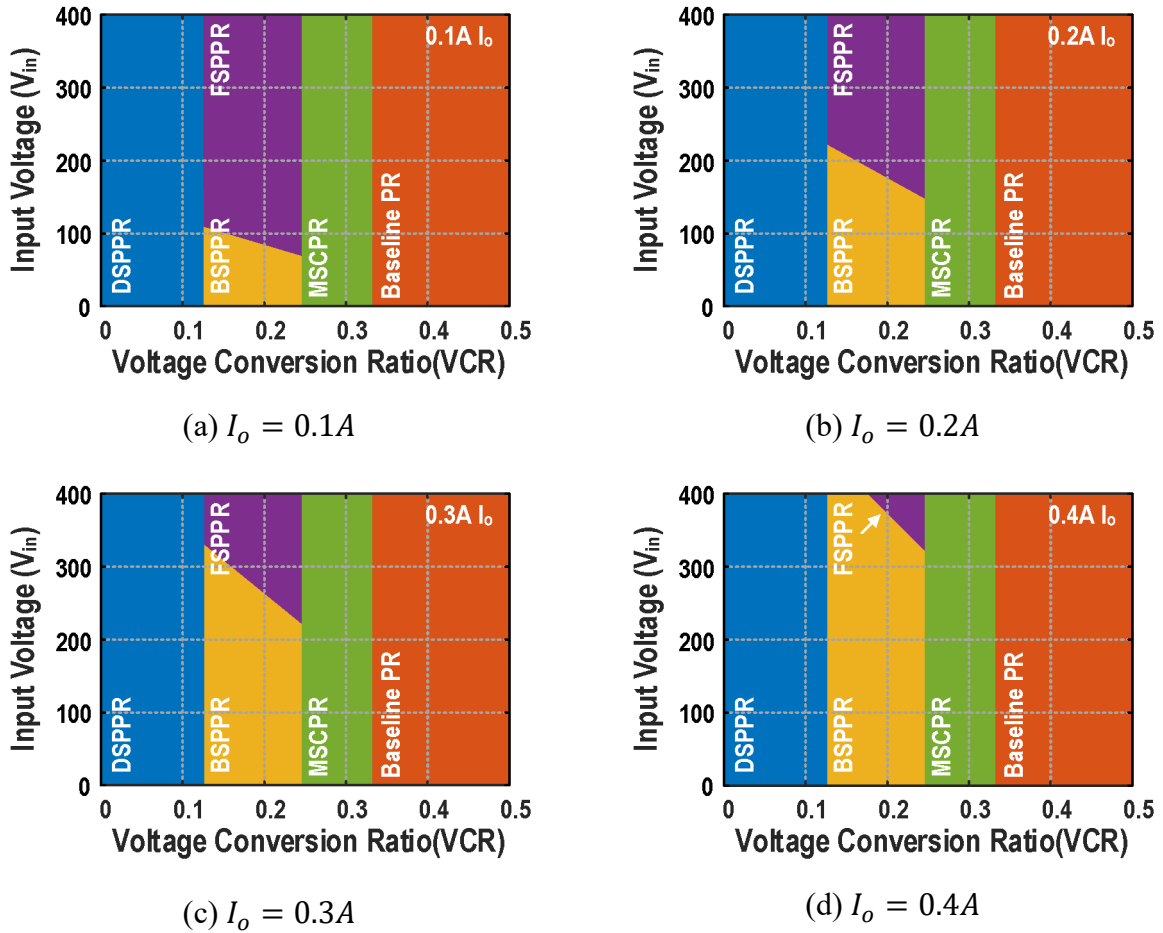


Figure 5.14 Example of hybrid PR-based topology selection based on the value of peak PR resonant current at various input/output voltage.

Here, the trade-off between BSPPR and FSPPR converters raises an interesting discussion: where to put the SCs? It can be found in Figure 5.14 that the FSPPR converter is more advantageous at high input voltage, low output current, and higher VCR conditions because the frontside SC(s) effectively minimizes the PR voltage swing, V_{pp} . On the other hand, the BSPPR converter is more beneficial at low input voltage, high output current, and low VCR conditions since the backside SC(s) effectually reduces the equivalent PR output current, $I_{o,PR}$, by positioning the PR to high voltage and low current side. This conclusion can be directly applied to other high-order SC networks while analyzing topologies. Moreover, based on operation conditions and PR size, the place (frontside, backside, or dual-side) to add SC(s) could be determined with the one with the lowest achievable $I_{L,PR(pk)}$, which is typically trade-off between V_{pp} and $I_{o,PR}$.

Based on the comparison between FSPPR and BSPPR, the SC arrangement of the DSPPR converter can be investigated to determine if the PR-middle strategy is the optimal solution for $VCR \leq 0.125$. Here, the two extra SC arrangements: 4:1 frontside switched capacitor PR-based (FSCPR) and 4:1 backside switched capacitor PR-based (BSCPR) converters can be identified as competitors for the DSPPR converter. Utilizing the idea that a lower $I_{L,PR(pk)}$ can potentially achieve better performance, $I_{L,PR(pk)}$ of the two 4:1 extensions is calculated assuming the same operation sequence, as shown in Figure 5.15. The findings suggest that, similar to the trade-off between BSPPR and FSPPR, the 4:1 FSCPR is more suitable for high input voltage and low output current scenarios, while the 4:1 BSCPR is more advantageous for low input voltage and high output current scenarios, with DSPPR positioned in between. In conclusion, with the minimum $I_{L,PR(pk)}$ reasoning, the topological extensions can be conducted with their optimal operating conditions identified and analyzed, serving as a useful strategy for topology exploration. It should

be noted that there are no specific 4:1 FSCPR or 4:1 BSCPR circuits available; instead, their behavior is identified by assuming the same operation principle.

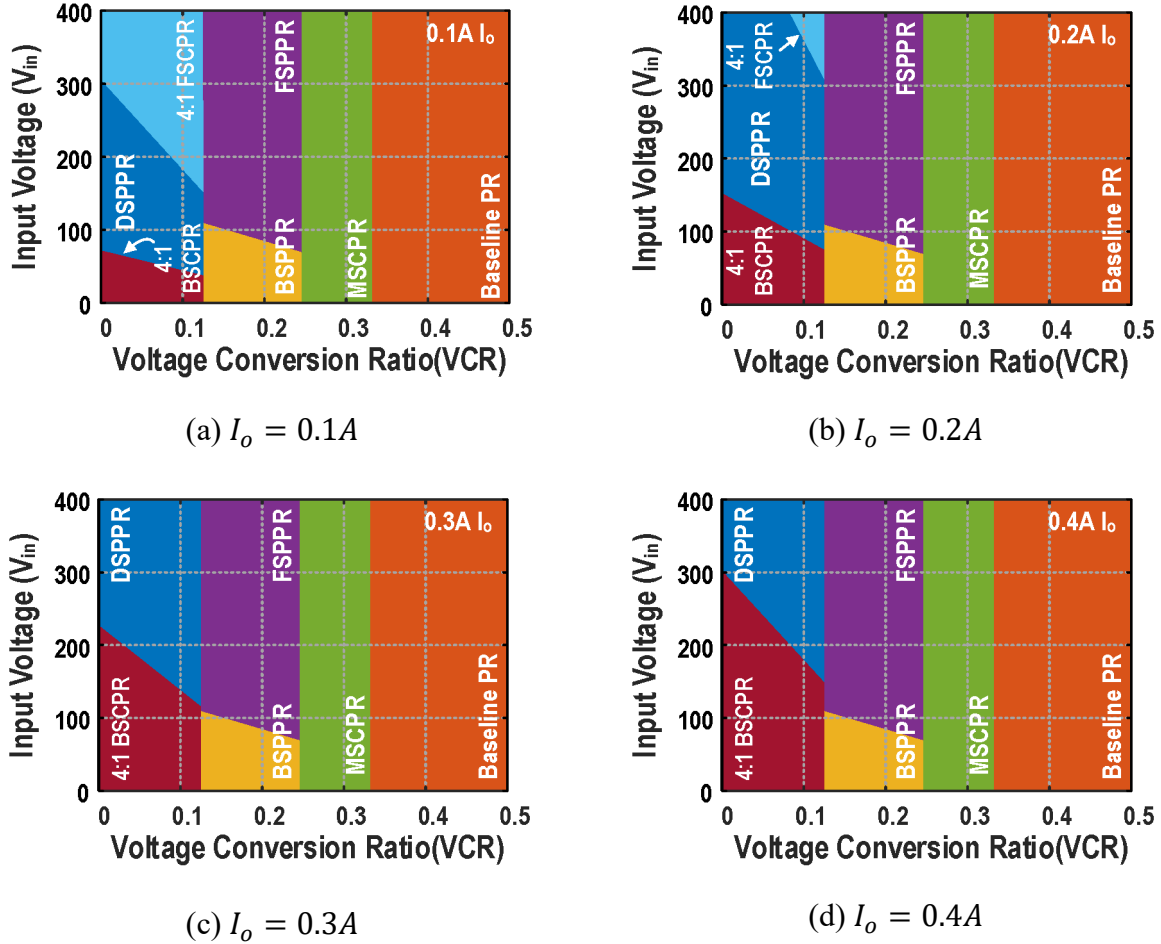


Figure 5.15 Topology selection extension of Figure 5.14 with 4:1 frontside/backside SC topologies included (a) 0.1A, (b) 0.2A, (c) 0.3A. and (d) 0.4A output current (given PR size of 20/0.4mm in diameter and thickness)

5.4 Experimental Verification

To verify the performance between the hybrid PR-based converters, a re-configurable prototype, which can be configured as 1) DSPPR, 2) BSPPR, 3) FSPPR, and 4) baseline PR-based converters, is fabricated with discrete components, as shown in Figure 5.16 where the parameters are shown in Table 5.4. Here, the circular-shaped radial vibration mode PRs are chosen with the material of PIC181 and sizes of 20mm in diameter and (0.2, 1, and 2mm) in thickness with

parameter extraction results illustrated in Table 5.5. Note that, the PR parameters are measured by vector network analyzer (VNA).

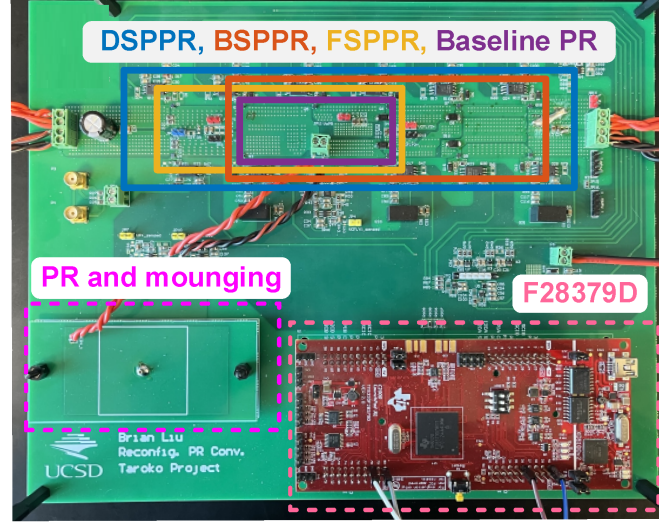


Figure 5.16 A prototype of reconfigurable hybrid PR-based converter.

Table 5.4 Experimental parts and parameters

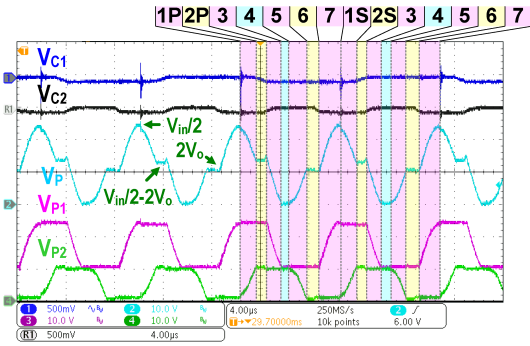
Parts/Parameters	Values	Implementation
Switches (S1-S7)	80V, 10A, 20m Ω	EPC2214
S6,7 parallel diode	40V, 2A	PMEG4020EP
Gate driver	Isolated, 2.3A	ADUM4120
Digital Controller	150MHz	TMS320F28335
Input voltage range V_{in}	36-60 V	-
Output voltage range V_o	4-6 V	-
Output current range I_o	0.05-0.5 A	-
flying capacitor C_{F1}	4.7 μ F	MLCC (0805)
flying capacitor C_{F2}	4.7 μ F	MLCC (0603)

The steady-state waveforms of the four PR-based converters operated under 48/5V, 0.1A with PIC181 (20/0.2) mm disk-shaped PR are demonstrated in Figure 5.17. The PR-based converters achieve ZVS and soft-charging/discharging of C_{F1} during operations. Moreover, each topology has different equivalent PR input and output voltage, $V_{in,PR}$ and $V_{o,PR}$, and therefore,

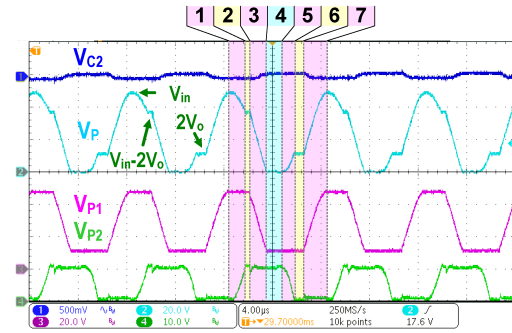
different peak-to-peak PR voltage, V_{pp} , phase 2 voltage, V_2 , and phase 6 voltage, V_6 , are presented. It can be found that the DSPPR has the lowest V_{pp} and voltage difference in phases 2 and 4, $\Delta(V_2 - V_6)$, implying the lowest ZVS charge where Q_{ZVS} is proportional to V_{pp} , and highest VCR_{PR} , where VCR_{PR} equals 0.5 as $\Delta(V_2 - V_6)$ equals 0, and thereby, indicating the best PR utilization with best performance expected.

Table 5.5 Parameters of disk-shaped radial-mode piezoelectric resonator in PIC181 material and various sizes at VNA power of 0dbm (1mW, 50 Ω)

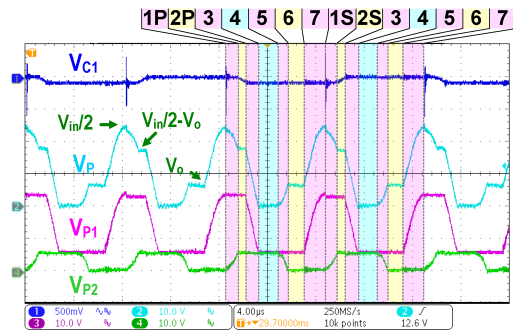
PIC 181 PR size	C_p (nF)	C (nF)	L (mH)	R (Ω)	f_r/f_{ar} (kHz)	Q
20/0.2mm	13.96	4.2	0.47	0.48	113/129	696
20/1mm	3.55	0.95	2.1	1.52	113/128	974
20/2mm	1.4	0.32	6.2	4.01	113/126	1100



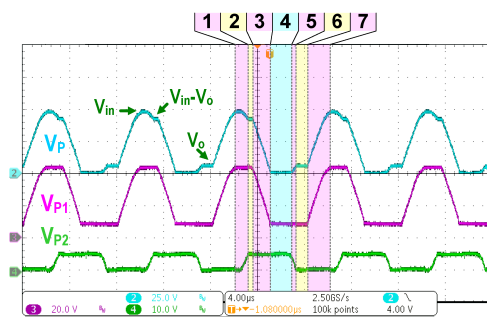
(a) DSPPR converter



(b) BSPPR converter



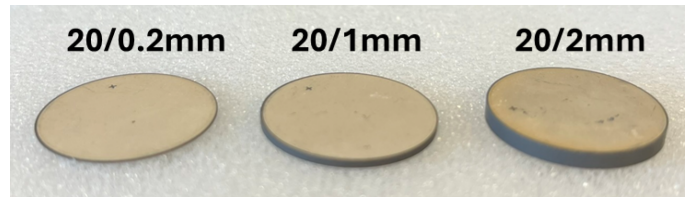
(c) FSPPR converter



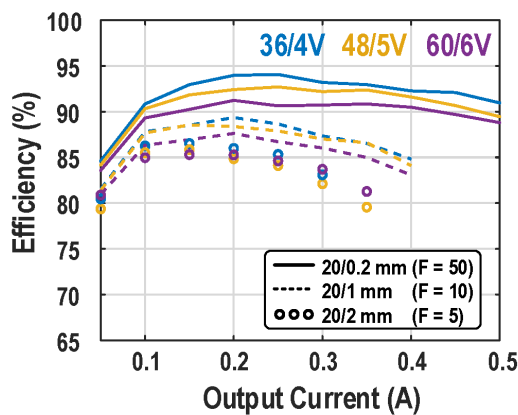
(d) Baseline PR-based converter

Figure 5.17 Steady-state waveforms of PR-based converters at 48/5V 0.1A

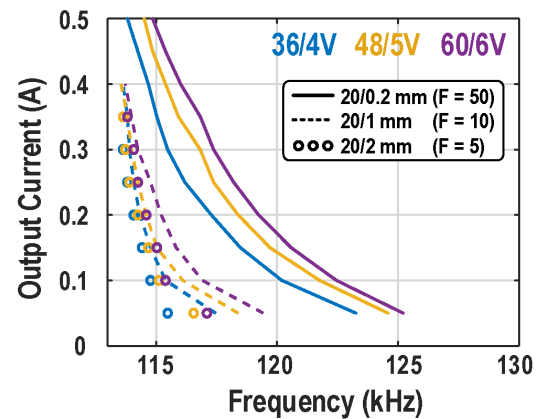
Performance comparisons of different PR radius/thickness ratios, F , within the same topology (the DSPPR converter) and operation conditions are measured, as shown in Figure 5.18. Figure 5.18(b) illustrates the efficiencies of different F across different input/output voltages, and Figure 18(c) presents the frequency variation corresponding to relative operation points shown in Figure 5.18(b). Here, the selected F -ratios are 5, 10, and 50, and, the same radius is chosen for the PRs, ensuring a similar operation frequency range in the radial vibration mode. According to the figures, the results reveal better efficiencies with a larger F . Also, the PRs with a lower F exhibit increased losses at higher output currents. These findings align with the observations in Figure 5.8(a): 1) the PR loss is reduced as F increases in the α -dominant region and 2) the PRs with a low F become significantly lossy as output current increases, with the PR loss represented on a logarithmic scale.



(a) Different-sized PRs



(b) Efficiency comparison



(c) Frequency variation comparison

Figure 5.18 Different-sized PRs and their efficiency and frequency variation comparison under same topology.

As for the frequency variation, the PRs with a lower F typically operate at slightly lower frequencies than those with a higher F under the same input/output conditions, suggesting a restricted operational range for the PRs with a lower F since the operating frequency cannot fall below the resonant frequency, f_r . This variation in operating frequencies originates from differences in their Butterworth-Van Dyke (BVD) model parameters; specifically, the PRs with a lower F display reduced capacitance and increased inductance, as listed in Table 5.5. Additionally, based on Table 5.4, it is more feasible for thicker PRs to achieve a better quality factor because the slim-designed PRs tend to be more sensitive to the mounting strategies.

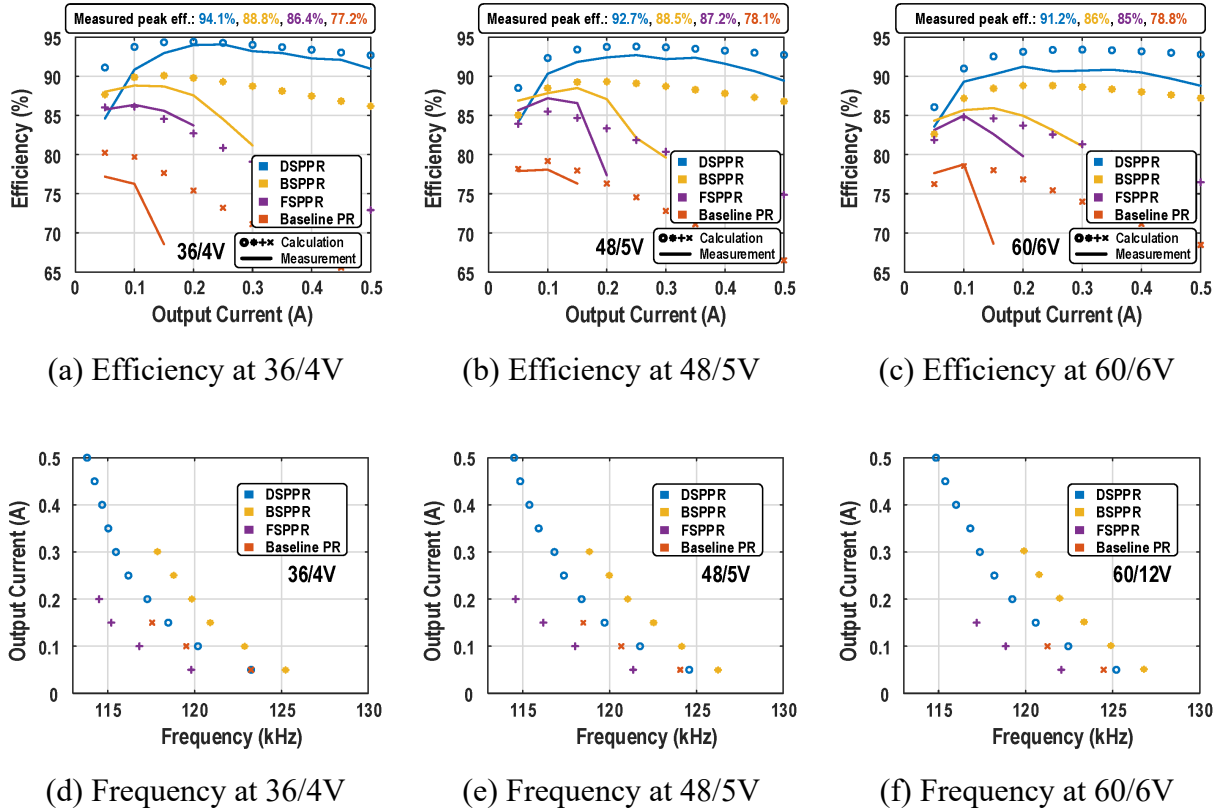


Figure 5.19 Hybrid PR-based converter efficiency and frequency variation comparison with PR of (20/0.2mm) in diameter and thickness.

The efficiency comparisons between topologies utilizing the same PR, (20/0.2mm) PR, with various input/output voltages are measured, as shown in Figure 5.19 along with calculation results. The calculation results are obtained with the PR quality factor (Q -value) of 340 instead of

696 as shown in Table 5.5 because of Q -value degradation with higher power, as shown in Figure 5.20. It can be found that the DSPPR is less efficient than the BSPPR and FSPPR converters because of higher switch counts (conduction loss), and the frontside switches added (switching loss), compared to the FSPPR and BSPPR converters. However, this situation quickly is altered, as output current increases. At a higher output, the DSPPR outperforms the rest of PR-based converters and becomes more and more beneficial with an increase in the load. These results can also be linked to the analysis in Section III part B (Figure. 5.12 and 5.13) that the total loss of the DSPPR converter becomes even more smaller at high current condition compared to the other PR-based converters. (correspond to better efficiency performance). Note that, unlike the integrated circuits, which can design the transistors in arbitrary size, the same transistors, EPC2241, are adopted in this discrete-designed comparison.

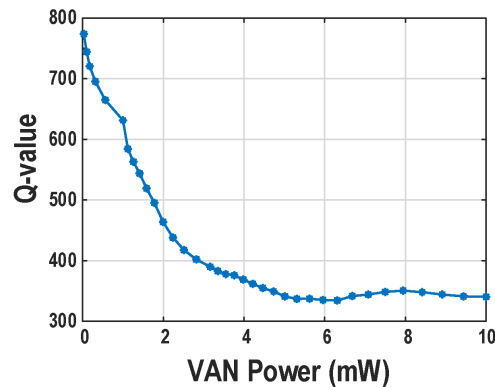


Figure 5.20 Q -value versus VNA power of the PIC181 20/0.2mm piezoelectric resonator.

5.5 Conclusion

This chapter evaluates state-of-the-art hybrid PR-based converters and the baseline PR-based converter by analyzing their PR operation and utilization. Following the comparison of PR operations, a device modeling framework for PRs is introduced along with active switches and capacitors models revisited. This PR framework incorporates the geometrical dimensions and

piezoelectric constants to develop a size-ratio-to-loss model, serving as a powerful tool in optimizing PR size and comparing different PR-based topologies. Subsequently, comprehensive comparisons of hybrid PR-based converters are performed, focusing on power density and maximum achievable efficiency. These comparisons assess PR current amplitude, operating frequency, active/passive footprint, and total loss, offering insights into various PR-based converter designs. A discrete reconfigurable prototype capable of configuring as DSPPR, BSPPR, FSPPR, and baseline PR-based converters is built using PIC181 disk-shaped radial mode PRs in different size ratios (20/0.2 mm, 20/1 mm, and 20/2 mm in diameter and thickness). Using this prototype, the performance of various PR-based converters with identical PR sizes and the impact of different PR sizes within the same topology (the DSPPR converter) are measured and analyzed under $VCR \approx 0.1$ conditions across different input/output scenarios, which are used to verify the proposed PR size-ratio-to-loss model and the comparison analysis.

Acknowledgements

Chapter 5 is based on and mostly a reprint of the following publication:

- W. -C. B. Liu, and P. P. Mercier, " Review and Comparison of Low-Voltage-Output High-Step-Down-Ratio Hybrid Switched-Capacitor Piezoelectric-Resonator-based DC-DC Converters," *in preparation for submission*.

Chapter 6 Closed-loop Control of a Dual-side Series/Parallel Piezoelectric-Resonator-based DC-DC Converters

6.1 Introduction

Piezoelectric resonators (PRs) garner significant attention for their planner form factor, cost-effectiveness, linear frequency scaling, and promising efficiency and power density. As a result, numerous PR-based converters were reported, demonstrating impressive performance across diverse voltage ranges [25], [28-32], [52-54], [65], [66], [69], [74], [77]. On the other hand, [70], [71], [80], [82] shows switched-capacitor hybrid PR-based converters that strive to improve efficiency at low voltage conversion ratios (VCRs), defined as V_o/V_{in} . Additionally, [80] showcases a hybrid PR-based converter realized through integrated circuit (IC) technology, with enhanced efficiency at even lower VCRs ($VCRs \leq 0.1$).

However, most of the reported converters are verified through open-loop testing, disregarding the closed-loop dynamics of PRs within the system [25], [28-32], [52-54], [65], [66], [69], [70], [71], [74], [77], [80], [82]. This omission arises due to the demand for intricate and accurate timing control in PR-based converters. Typically, to ensure optimal performance of a PR-based converter, the controller is required to manage frequency, pulse width, dead time, and phase shift modulations, presenting significant challenges.

Several works have explored closed-loop control strategies for PR-based converters. [93] employs pulse-frequency modulation (PFM) for regulation, yet lacks consideration for optimal timing, potentially resulting in zero-voltage switching (ZVS) losses under variable load conditions. [94] introduced a fixed-frequency control to avoid the spurious modes effects. [95] achieves optimal operation with regulation; however, this control is case-specific and its sense-and-react-

based nature may be susceptible to noise. [96] addresses noise immunity concerns with a static closed-loop control while aiming for optimal operation. Despite these developments, there remains a lack of control strategies specifically for hybrid PR-based converters. Moreover, previous works have not addressed the out-of-phase/frequency behavior, a crucial factor for understanding system dynamics.

This paper introduces a control strategy for hybrid PR-based converters [70], [71], [80], [82], leveraged the phase-locking concept through a "sense and predict" mechanism that examines the out-of-phase/frequency behavior of PR waveforms. This work specifically focuses on the dual-side series/parallel PR-based converter, as shown in Figure 6.1, due to its topology complexity compared to [70], [71], [80], [82]. Importantly, the proposed control method exhibits adaptability, enabling seamless adaption to the aforementioned PR-based converters, as they share similar operational sequences, the six-stage switching sequences, $\{V_{in} - V_o, zero, V_o\}$ defined in [29]. To validate the proposed strategy, a discrete prototype featuring a (20/0.2)mm PZT radial vibration mode PR is constructed, with closed-loop operation managed by a digital controller.

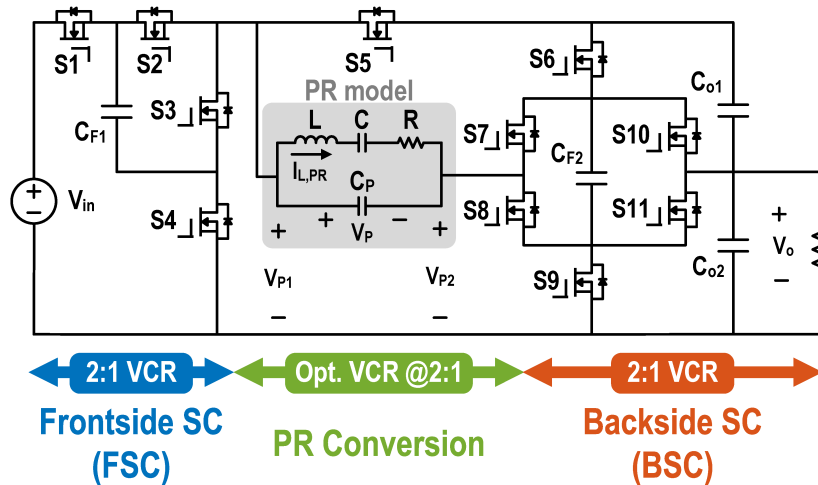


Figure 6.1 Dual-side Series/Parallel PR-based (DSPPR) converter [80].

6.2 Feedback loops and control strategy

According to Figure 6.2, the accurate operating frequency and turned-on/off timings are crucial to achieve optimal performance in a PR-based converter including ZVS, and soft-charging. Here, Figure 6.2 illustrates the driving logic of each driving signal based on the operation waveforms where t_0 to t_6 are the on/off timing of the driving signals.

Given the variable frequency nature of PR operation, the operating frequency needs to be first phase-locked with the PR resonance. This synchronization allows the switches to be turned on/off accordingly, enabling voltage regulation, loss minimization, and ZVS. Therefore, a phase-locked control becomes imperative. Once the frequency and phase are locked, the subsequent driving logic can be determined as follows and the timing control is illustrated in Table 6.1.

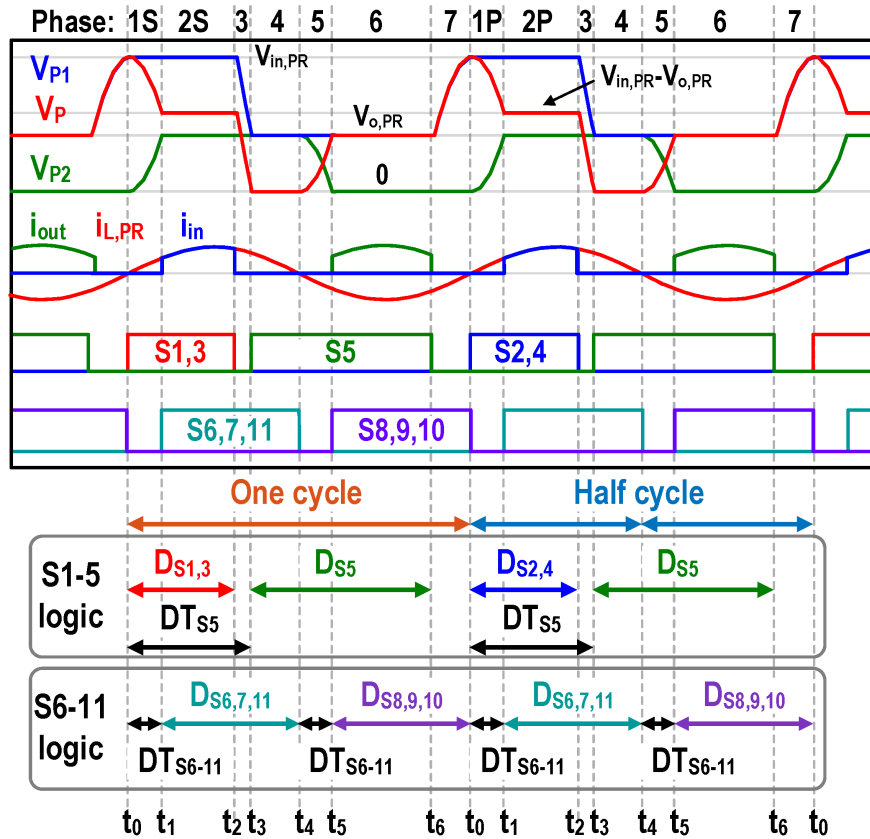


Figure 6.2 Operation waveforms and control logic of the DSPPR converter.

Table 6.1 Timing control of each driving signal

Signal	Turn-on control	Turn-off control
(S1,3)/ (S2,4)	PLL (t_0)	Voltage regulation loop (t_2)
S5	Comparator (t_3)	Loss minimization loop (t_6)
(S6,7,11)	Comparator (t_1)	PLL (t_4)
(S8,9,10)	Comparator (t_5)	PLL (t_0)

- 1) Signal (S1,3), (S2,4): Turned on at the beginning of a cycle, t_0 , and turned off based on the voltage regulation loop, t_2 . Here, the duty cycle of (S1,3) and (S2,4), $D_{S1,3}$ and $D_{S2,4}$ ranges across phases 1 and 2, where phase 2 is the only phase connected to the input; hence, $D_{S1,3}$ and $D_{S2,4}$ can be used to control how much energy is sourced from the input, achieving output voltage regulation. The voltage regulation ability can be verified by solving the voltage conversion ratio of the PR using conservation of charge and energy (CoC and CoE) [29], as shown in equation (6.1). Here, q_n donates to the charger in the n-th phase. Evidently, the portion of q_2 determines the voltage gain and, therefore, the output voltage.

$$0 \leq \frac{V_{o,PR}}{V_{in,PR}} = \frac{q_2}{2q_2 + q_4} \leq \frac{1}{2} \quad (6.1)$$

- 2) Signal (S5): Turned on after a delay time, DT_{S5} when V_{P1} falls to $V_{o,PR}$ at t_3 , and turned off according to the loss minimization loop, t_6 . Here, the turned-off timing is related to the phase 7 duration, during which $i_{L,PR}$ charges C_P . That is, at a given frequency, the duty cycle of S5, D_{S5} determines the phase 7 duration. To ensure precise charging time in phase 7, preventing additional losses, the turned-off timing of S5 is regulated by a feedback compensator within the loss minimization loop.

- 3) Signal (S6,7,11): Turned on after a delay time, DT_{S6-11} when V_{P2} rises to $V_{o,PR}$ at t_1 , and turned off at half cycle, t_4 , where $i_{L,PR}$ reverts its polarity.
- 4) Signal (S8,9,10): The driving signal (S8,9,10) mirrors the signal (S6,7,11) but operates with a 180-degree out-of-phase configuration, which is turned on/off at t_5 and t_0 respectively. Upon closer examination of the delay times, DT_{S6-11} , for (S8,9,10) and (S6,7,11), which is the duration of phases 1 and phase 5 respectively, a pattern emerges. Throughout phases 1 and 5, $i_{L,PR}$ charges/discharges C_P with an identical current amplitude and a voltage difference ($V_{o,PR}$). Furthermore, their deactivation aligns precisely with the zero-crossing of $i_{L,PR}$. Thus, signal (S8,9,10) replicates signal (S6,7,11) with a half-cycle phase shift.

6.2.1 Phase-Locked Loop

Before designing the phase-locked mechanism for a PR-based converter, it is important to understand how the PR behaves during out-of-phase operation, which can be achieved by inspecting V_P , V_{P1} , and V_{P2} during the zero-crossing of $i_{L,PR}$. Given the intricate nature of V_P measurement in practice, the analysis of out-of-phase behavior is conducted through the examination of V_{P1} and V_{P2} . Here, the beginning of a cycle is defined as t_0 , illustrated in Figure 6.2, where $i_{L,PR}$ experiences zero-crossing in the ideal scenario.

6.2.1.1 PR Positive Node Analysis, V_{P1}

The ideal and most common out-of-phase V_{P1} waveforms are depicted in Figure 6.3(a)-(f). Here, two distinct sampling points, denoted as Pre_{smp1} and Pre_{smp2} , are designated for pre-

sampling immediately before a new cycle. According to the pre-sample results in Figure 6.3, the relationship could be partially identified, as shown in Table 6.2.

In an ideal case, V_{P1} gradually rises to $V_{in,PR}$ before the subsequent switches are activated, entering the next phase. However, deviations in the switching frequency, f_{sw} , from the ideal PR operation frequency, f_{PR} , may result in V_{P1} not precisely equating $V_{in,PR}$ at t_0 , as demonstrated in (b)-(f) of Figure 6.3. For instance, in (b)-(d) cases, when the Pre_{smp1} is greater than Pre_{smp2} , f_{sw} is smaller than f_{PR} because the polarity of $i_{L,PR}$ reverses before the new cycle, discharging V_{P1} node, and causing a decrease of V_{P1} as well as Pre_{smp2} value. It is worth noting that, based on Table 6.2, the relationship of f_{sw} and f_{PR} cannot be solely determined by V_{P1} waveforms since t_6 turn-off timing also plays a role in the final result of V_{P1} at t_0 , i.e., case (e) and (f).

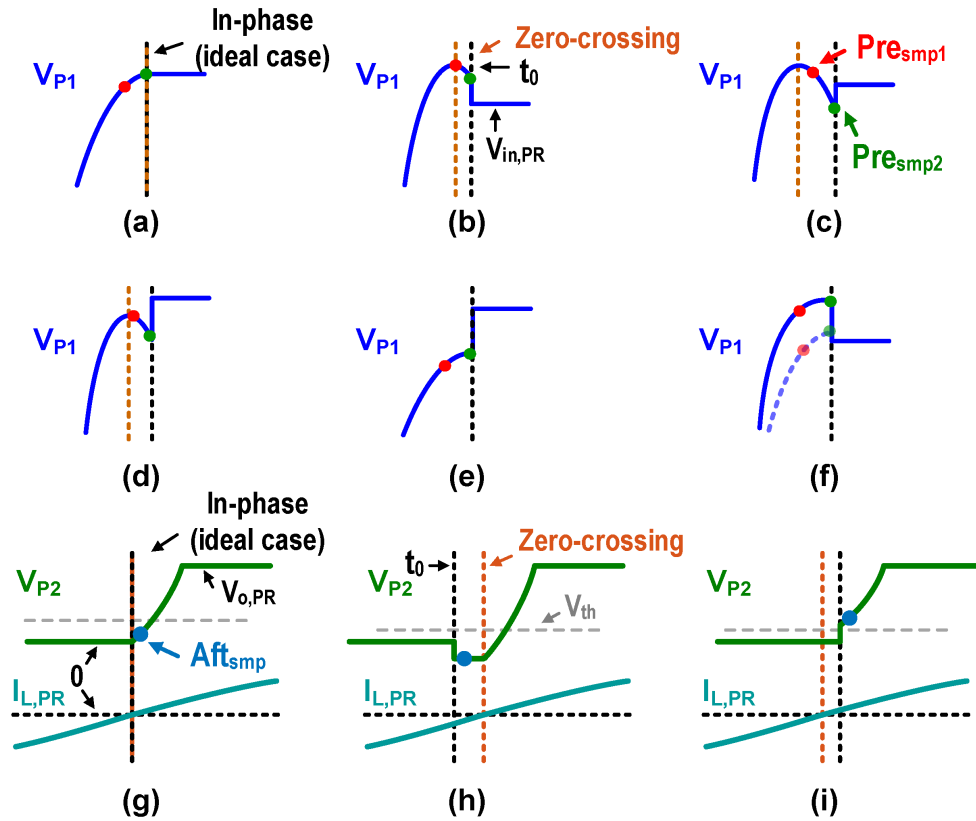


Figure 6.3 PR positive/negative node, V_{P1} , V_{P2} , waveforms in proximity to t_0 .

Table 6.2 V_{P1} and V_{P2} in/out-of-phase waveforms summary

Signal	Case	Observation	Conclusion
V_{P1}	(a)	$Pre_{smp2} \approx V_{in,PR} > Pre_{smp1}$	$f_{sw} \approx f_{PR}$
	(b)	$Pre_{smp1} > Pre_{smp2} > V_{in,PR}$	$f_{sw} < f_{PR}$
	(c)	$Pre_{smp1} > V_{in,PR} > Pre_{smp2}$	$f_{sw} < f_{PR}$
	(d)	$V_{in,PR} > Pre_{smp1} > Pre_{smp2}$	$f_{sw} < f_{PR}$
	(e)	$V_{in,PR} > Pre_{smp2} > Pre_{smp1}$	$f_{sw} > f_{PR}$ or $t_6 > t_{6,ideal}$
	(f)	$Pre_{smp2} > Pre_{smp1} > V_{in,PR}$ or $Pre_{smp2} > V_{in,PR} > Pre_{smp1}$	$t_6 < t_{6,ideal}$
V_{P2}	(g)	$V_{th} > Aft_{smp} > 0$	$f_{sw} \approx f_{PR}$
	(h)	$V_{th} > 0 \geq Aft_{smp}$	$f_{sw} > f_{PR}$
	(i)	$Aft_{smp} > V_{th} > 0$	$f_{sw} < f_{PR}$ or t_6 timing

6.2.1.2 PR Negative Node Analysis, V_{P2}

Apart from V_{P1} waveform, V_{P2} waveform near t_0 appears to be another powerful indicator. Similar to V_{P1} , V_{P2} also provides insights into frequency deviations, as shown in Figure 6.3(g)-(h). Here, an after-sampling point, Aft_{smp} , is assigned to capture V_{P2} after the initiation of a new cycle and a threshold voltage V_{th} is used to determine the frequency deviation.

In Figure 6.3(g)-(h), three scenarios are illustrated: (g) $f_{sw} \approx f_{PR}$, (h) $f_{sw} > f_{PR}$, and (i) $f_{sw} < f_{PR}$ where the conclusion is made in Table 6.2. In case (g), the ideal case, Aft_{smp} is a small positive value due to the soft charging of C_P with a small current at the very beginning of a cycle. In case (h), Aft_{smp} shows a voltage drop, a consequence of the body-diode conduction initiated before zero-crossing, where a current path is established from the ground to the PR input through the body diode of S8 and S9, as well as the path of switches (S1,3) or (S2,4). In case (i), $i_{L,PR}$

reverts before a new cycle, causing discharging of C_P and, hence, presenting a voltage step at t_0 . It is noteworthy that t_6 turn-off timing also affects the voltage step in case (i).

6.2.1.3 Phase-Locked Loop Implementation

Analyzing V_{P1} and V_{P2} waveforms near t_0 provides insights into frequency adjustments, as inferred from Table 6.2. The frequency modulation can be executed based on (a-d), (g), and (h), facilitated by (e), (f), and (i), given that (a-d), (g), and (h) are deterministic cases, while (e), (f), and (i) are indeterministic cases influenced by t_6 timing. For example, upon detecting case (b), the controller can increase f_{sw} to synchronize with f_{PR} ; on the other hand, identifying case (h) allows the controller to decrease f_{sw} to alignment with f_{PR} . That is, according to Table 6.2, a state machine within a digital controller can be designed to achieve frequency/phase alignment.

6.2.2 Voltage Regulation and Loss Minimization Loops

6.2.2.1 Voltage Regulation Loop

The voltage regulation loop involves a feedback mechanism that senses the output voltage and feeds the sensed signal into a proportional-integral (PI) compensation with a reference voltage generating duty cycle commands. The commands are subsequently used to control switches S1-4, which implicitly control energy sourced from the input in phase 2, as shown in Fig. 6.2.

6.2.2.2 Loss Minimization Loop

The loss minimization loop constitutes another feedback operation designed to precisely align V_P with $V_{in,PR}$ at t_0 by leveraging the sampled result, Pre_{smp2} , from the phase-locked loop. This feedback loop feeds Pre_{smp2} to another PI compensator along with $V_{in,PR}$ reference,

generating an off-time command for t_6 in Figure 6.2. This off-timing governs the soft-charging duration of C_p in phase 7 and eventually influences the final V_p value at t_0 .

6.2.3 Frontside Switched Capacitor Balance Loop

The frontside switched capacitor (FSC) operates in a similar way as the three-level buck converter[83], [97]-[99]. In this configuration, the FSC voltage (V_{CF1}) is not self-balanced, leading to voltage drift due to mismatches in parameters such as on-resistance and turn-on duration between series and parallel modes. To address the voltage drift and ensure optimal performance, a "skip and repeat" balance loop, utilizing hysteresis thresholds, is employed, as shown in Figure 6.4. Here, the hysteresis thresholds, V_{thH} and V_{thL} , are set and activate the balance loop control when V_{CF1} reaches these thresholds. Specifically, the series mode (charging mode) is skipped, and the parallel mode (discharging mode) is repeated when $V_{CF1} \geq V_{thH}$, and the opposite action is taken when $V_{CF1} \leq V_{thL}$.

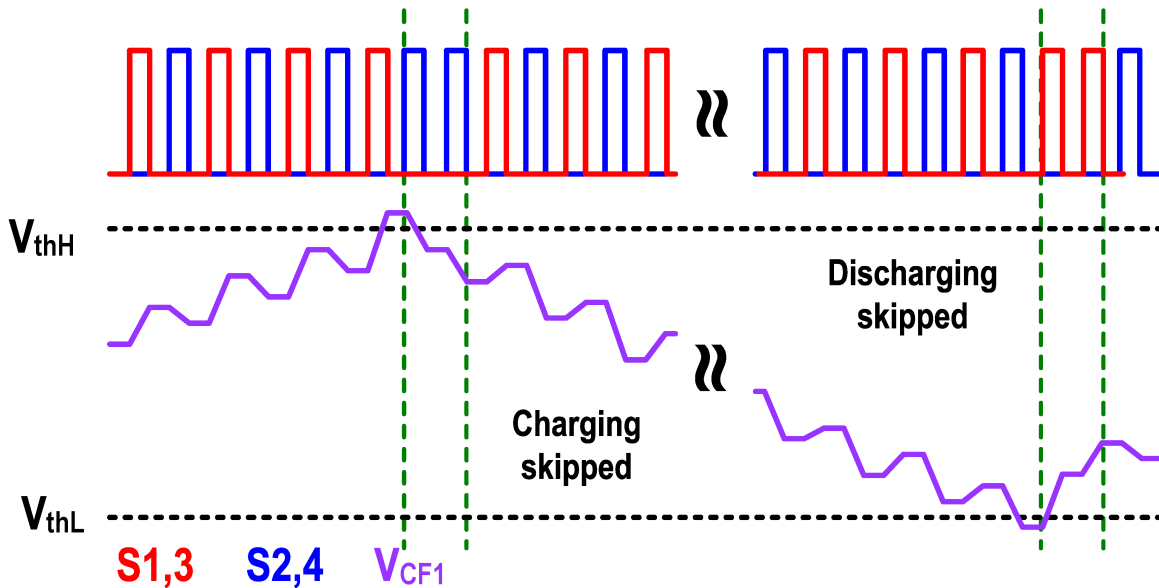


Figure 6.4 Frontside switched capacitor (FSC) balance loop control.

6.2.4 Block Diagram for Closed-Loop Control

The block diagram depicting the finalized closed-loop control is presented in Figure 6.5. Here, the digital controller, TMS320F28397D, is adopted in this work whose analog comparators share the same pin as the ADC blocks, reducing system complexity with four feedbacks, V_{CF1} , V_{P1} , V_{P2} , and V_o . In Figure 6.5, the comparators, $COMP1$, and $COMP2$, share the pins with $ADC1$ and $ADC2$ respectively. Additionally, the reference voltage, $V_{o,PR(ADC)}$, for the comparators can be obtained from oversampling of V_{P2} in $ADC2$. Ultimately, a fully closed-loop system with reduced complexity is designed.

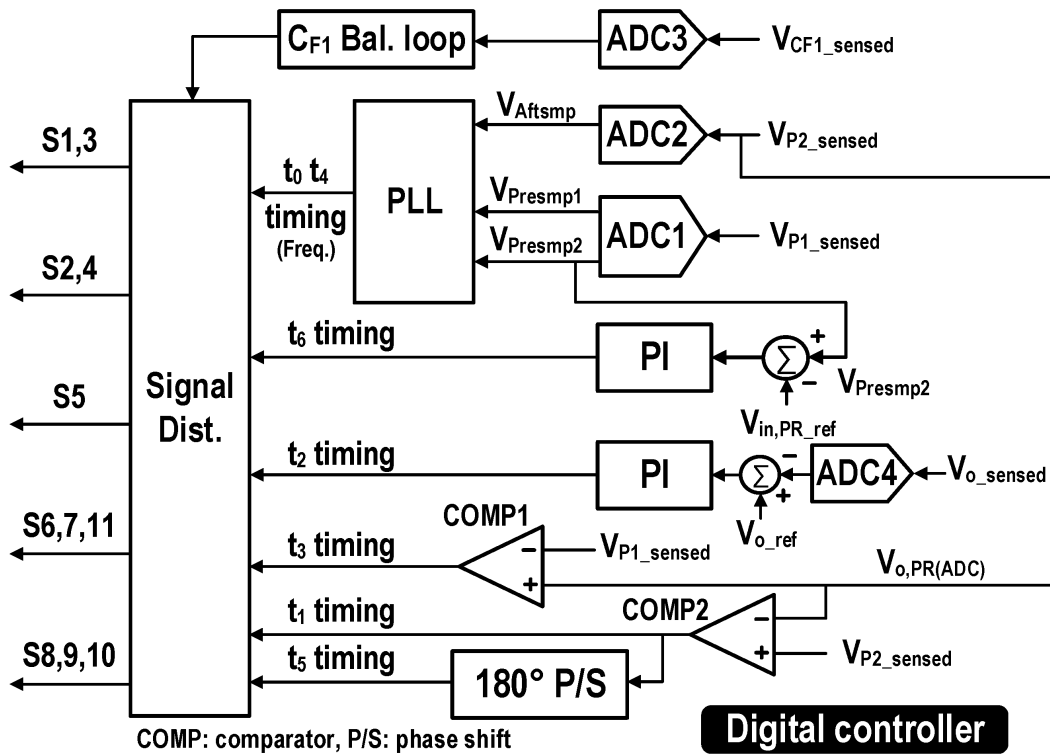


Figure 6.5 Block diagram for the closed-loop control.

6.3 Implementation and Experimental Results

The DSPPR converter prototype is built, as shown in Figure 6.6, with a digital controller, F28379D, operating at 150MHz clock frequency. A disk-shaped PIC 181 PR in size of (20/0.2)mm in radius and thickness is applied to this design, exhibiting resonant and anti-resonant frequencies of 113 and 129kHz, respectively, with a quality factor of ≈ 700 , which donates as $(\sqrt{L/C})/R$. The EPC2241s are adopted as active switches. The output capacitors and flying capacitors are $\approx 10\mu\text{F}$ MLCCs.

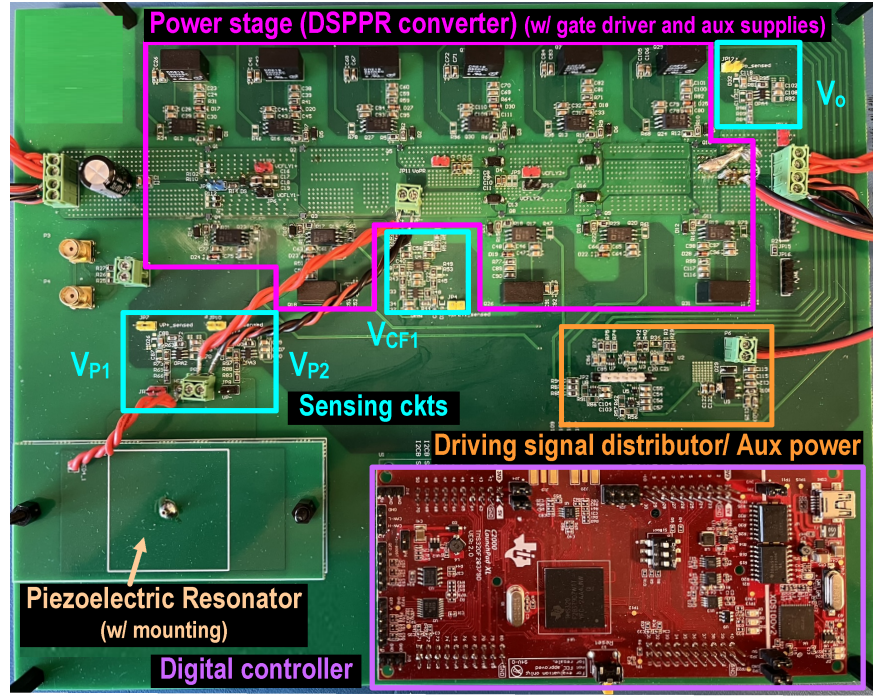


Figure 6.6 Circuit implementation for closed-loop test.

The steady-state waveforms with closed-loop control enabled are shown in Figure 6.7 with each corresponding phase and timing annotated. The measured waveforms are similar to the ideal waveforms, as shown in Figure 6.2, realizing soft-charging of C_p and quasi-ZVS. Due to the inherent non-idealities, e.g., sensing resolution, offsets, and processing delays, the ZVS is not fully achieved.

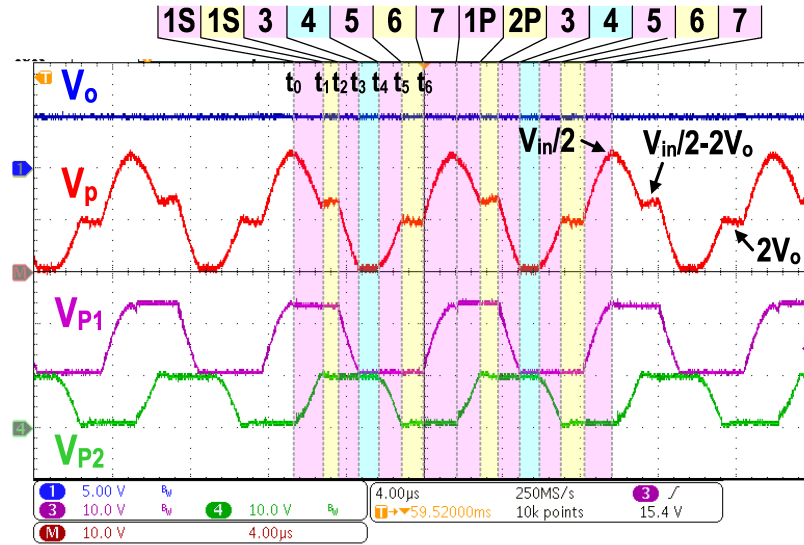
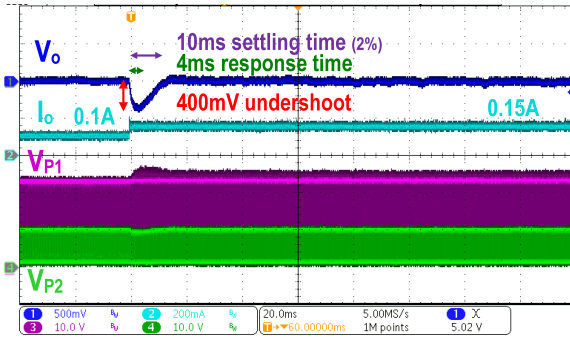
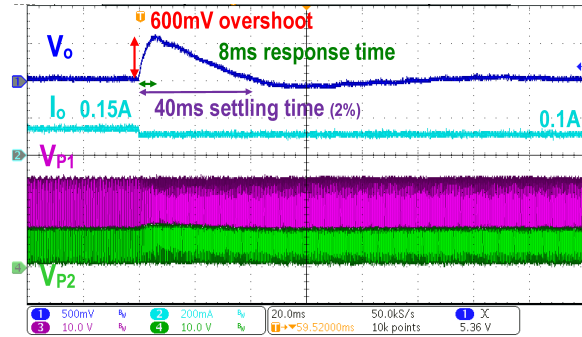


Figure 6.7 Closed-loop steady-state waveforms at 48/5V, 0.1A.

The transient results are demonstrated in Figure 6.8(a) and (b) with a load step from 0.1A to 0.15A and 0.1A/ μ s slew rate. Here, the undershoot voltage, response time, and 2% settling time are 400mV, 4ms, and 10ms respectively in the load step-up while 600mV, 8ms, and 40ms respectively in the load step-down.



(a) Load step-up dynamics (0.1-0.15A)



(b) Load step-down (0.15-0.1A)

Figure 6.8 Transient response at 48/5V, 0.15-0.1A.

The FSC balance waveforms are shown in Figure 6.8, revealing that when the balancing loop is disabled, there is a voltage offset due to parameter mismatch. On the other hand, when the

balancing loop is enabled, the series mode skipped control is activated, repeating an additional discharging operation to realign V_{CF1} to $V_{in}/2$, which is 24V in the test scenario.

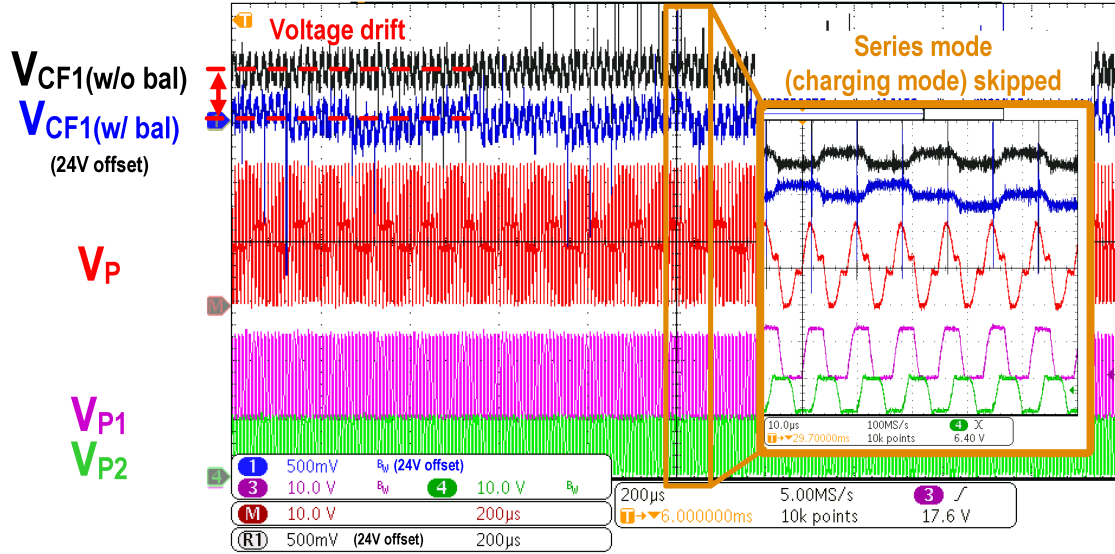


Figure 6.9 Frontside switched capacitor balance waveforms at 48/5V.

6.4 Conclusion

This study introduces a new control strategy for hybrid PR-based converters. Each control timing is illustrated in detail and, accordingly, the driving strategy is concluded. By examining the out-of-phase waveforms of PR, a state machine is designed for PLL control. In addition, the regulation and loss minimization loops are enabled to achieve ideal operation with regulation. Finally, a prototype is built featuring a disk-shaped PIC 181 PR with dimensions of (20/0.2)mm in radius and thickness where the closed-loop control is realized by a digital controller. The measurement results validate the proposed control strategy and demonstrate the regulation ability.

Acknowledgements

Chapter 6 is based on and mostly a reprint of the following publication:

- W. -C. B. Liu, G. Pillonnet and P. P. Mercier, " Closed-loop Control of A Dual-side Series/Parallel Piezoelectric-Resonator-based DC-DC Converter," *in preparation for submission*.

Chapter 7 Summary and Future Work

7.1 Summary of Dissertation

This dissertation explores and develops a range of strategies for designing high-performance DC-DC converters to address the demands of various applications, including consumer electronics, the Internet of Things (IoT), cloud computing, etc. It focuses on three critical aspects: 1) materials, 2) controls, and 3) topologies - each vital for the development of high-performance converters. Initially, a control strategy, Constant On-Time (COT) control, is proposed for conventional inductor-based Buck converters, designed for multi-phase operation with superior transient performance. Subsequently, an emerging technology, piezoelectric resonators (PRs), is introduced. These devices present promising efficiency and power density performance for DC-DC converters. Utilizing this material, various hybrid PR-based converters are proposed accordingly, with physical implementations in both discrete and integrated designs that validate the performance of the proposed topologies. A model linking PR size to system loss is then developed to enable system-level optimization and facilitate comparatively topological analysis. Finally, a control strategy for the hybrid PR-based converters is investigated and developed, showcasing the first closed-loop system for the hybrid PR-based converter.

The contributions for each chapter are illustrate as follows:

Chapter 2, illustrated in Figure 7.1, introduces an ultra-fast transient constant on-time (UFTCOT) control scheme aimed at enabling simple multi-phase operation, stable system performance across a wide input-output range, and excellent load transient response. In this chapter, a small signal model is derived to provide insights into system stability, allowing modulator parameters to be designed with desired closed-loop bandwidth and phase margin. Based

on this model, a generalized duty-cycle-independent Q -value control strategy is developed, which enhances system stability and optimizes transient response throughout a broad input/output range. This Q -value control strategy can be readily extended to several other advanced COT control schemes. A fully discrete prototype is also constructed, showcasing a transient response that is six times faster than that of conventional inverse-charge constant on-time (IQCOT) control.

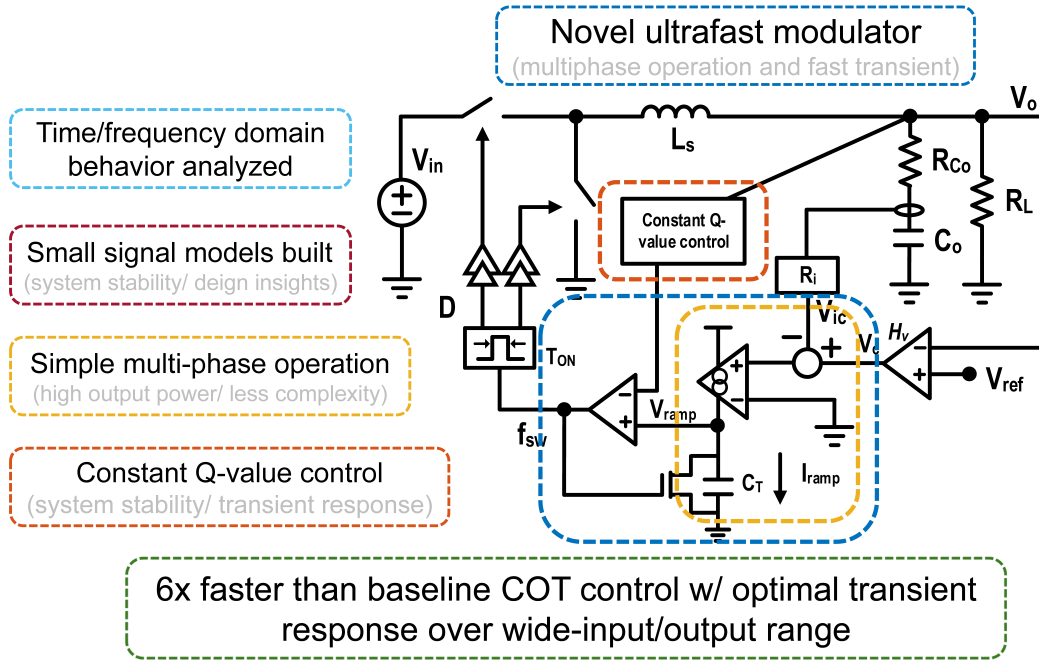


Figure 7.1 Summary of Chapter 2: A Novel Ultra-Fast Transient Constant On-Time Buck Converter with Duty-Cycle-Independent Quality Factors Design for Multi-Phase Operation

Chapter 3 introduces piezoelectric materials and vibrations, presenting the Butterworth-Van Dyke (BVD) model equivalents linked to the size of piezoelectric resonators. The frontside series/parallel PR-based (FSPPR) and Backside Series/Parallel PR-based (BSPPR) DC-DC converters are proposed, incorporating switched capacitors (SCs) into operation, to enhance conventional PR-based converters' performance at low voltage conversion ratios while sharing the same operation principle. In the switched capacitor hybridization, two hybrid strategies are

adopted: 1) the SC-first/PR-last method utilized by the FSPPR converter, and 2) the PR-first/SC-last method employed by the BSPPR converter, as shown in Figure 7.2 and 7.3. By employing the hybrid strategies, both the FSPPR and BSPPR converters operate PRs with a higher PR charge transfer utilization compared to the baseline PR-base converter while maintaining benefits such as zero-voltage switching (ZVS) and soft-charging of capacitors. Additionally, the FSPPR converter is capable of soft-charging/discharging of the flying capacitor while the BSPPR converter achieves self-balancing of its flying capacitor. Moreover, as the operation of PRs are largely limited to their current density, the BSPPR becomes beneficial by moving the PR to its input side (high voltage/low current side), where the output capacity is improved. Finally, both the FSPPR and BSPPR prototypes featuring a disk-shaped PZT piezoelectric resonator in radial vibration mode is constructed, demonstrating a 95.27% and 95.8% peak efficiency with $\sim 14\%$ efficiency improvement over the baseline PR-based converter at a 48/10V conversion ratio. The summaries of the FSPPR and BSPPR converters are illustrated in Figure 7.2 and 7.3.

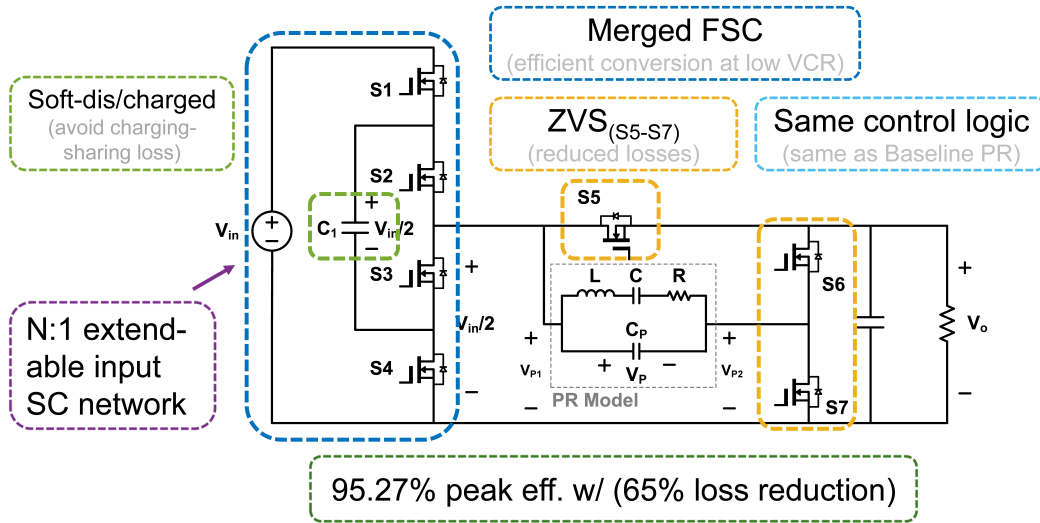


Figure 7.2 Summary of Chapter 3: Frontside series/parallel PR-based (FSPPR) converter

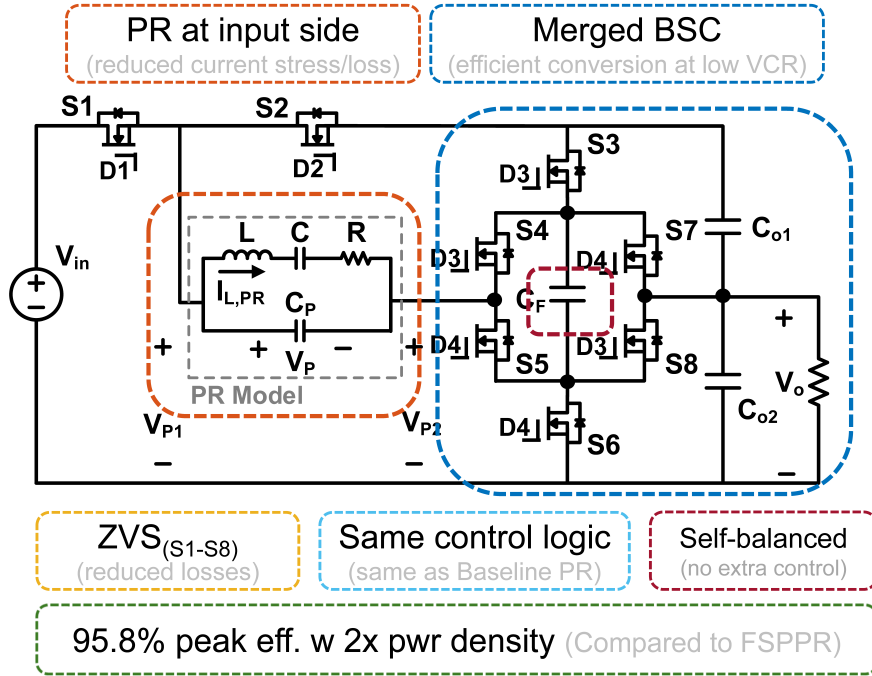


Figure 7.3 Summary of Chapter 3: Backside series/parallel PR-based (BSPPR) converter

Chapter 4, as shown in Figure 7.4, introduces the first integrated circuit design for the dual-side series/parallel PR-based (DSPPR) converter implemented in 180 nm BDC technology. The DSPPR enables efficient PR operations at low VCRs ($VCR \leq 0.1$), while minimizing the silicon and PR area. Leveraging the hybrid concept, two SCs are merged to the frontside and backside of the baseline PR-based converter, respectively. This configuration enables an optimal efficiency of 0.125VCR while placing the PR at the high voltage/low current side, thereby reducing the current stress over PR and the current-related losses while extending the output capability. Finally, the system is designed and tested under 16-20/ 1.1-2.2V conditions, revealing a peak efficiency of 92.9%, making a 13%-20% efficiency enhancement, a 13x-23x active area reduction, and a 1.7x-2.5x output capability improvement compared to co-designed PR-based converters.

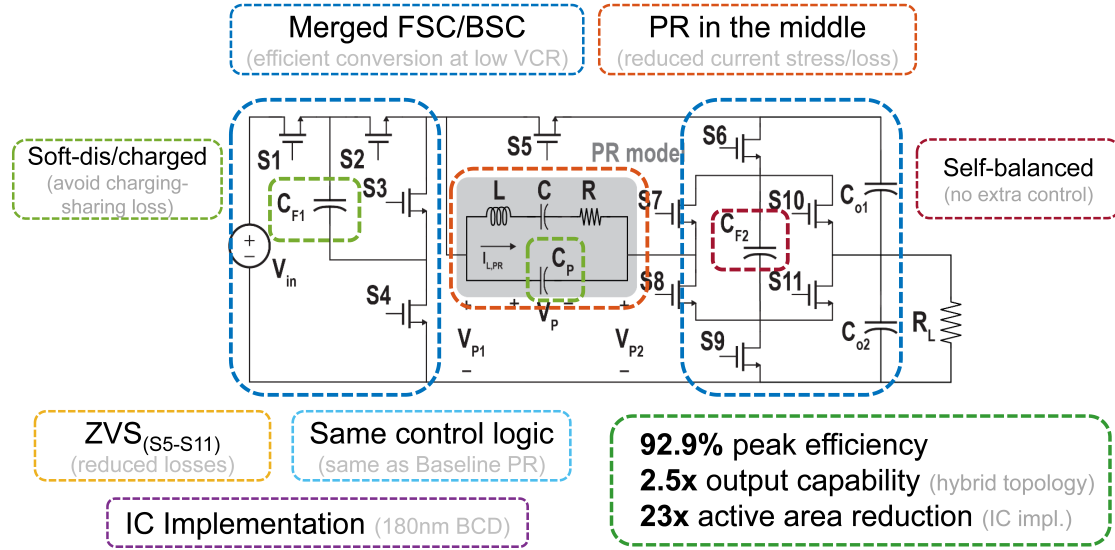


Figure 7.4 Summary of Chapter 4: An Integrated Dual-side Series/Parallel Piezoelectric Resonator-based DC-DC Converter

Chapter 5, as depicted in Figure 7.5, reviews the state-of-the-art hybrid PR-based converters and the baseline PR-based converter by analyzing their PR operation and utilization. Then, a device modeling framework for PRs is proposed along with active switches and capacitors models revisited. This PR framework incorporates the geometrical dimensions and piezoelectric constants to develop a size-ratio-to-loss model, serving as a powerful tool in optimizing PR size and comparing different PR-based topologies. Subsequently, comprehensive comparisons of hybrid PR-based converters are performed, focusing on power density and maximum achievable efficiency. These comparisons assess PR current amplitude, operating frequency, active/passive footprint, and total loss, offering insights into various PR-based converter designs. A discrete reconfigurable prototype capable of configuring as DSPPR, BSPPR, FSPPR, and baseline PR-based converters is built using PIC181 disk-shaped radial mode PRs in different size ratios (20/0.2 mm, 20/1 mm, and 20/2 mm in diameter and thickness).

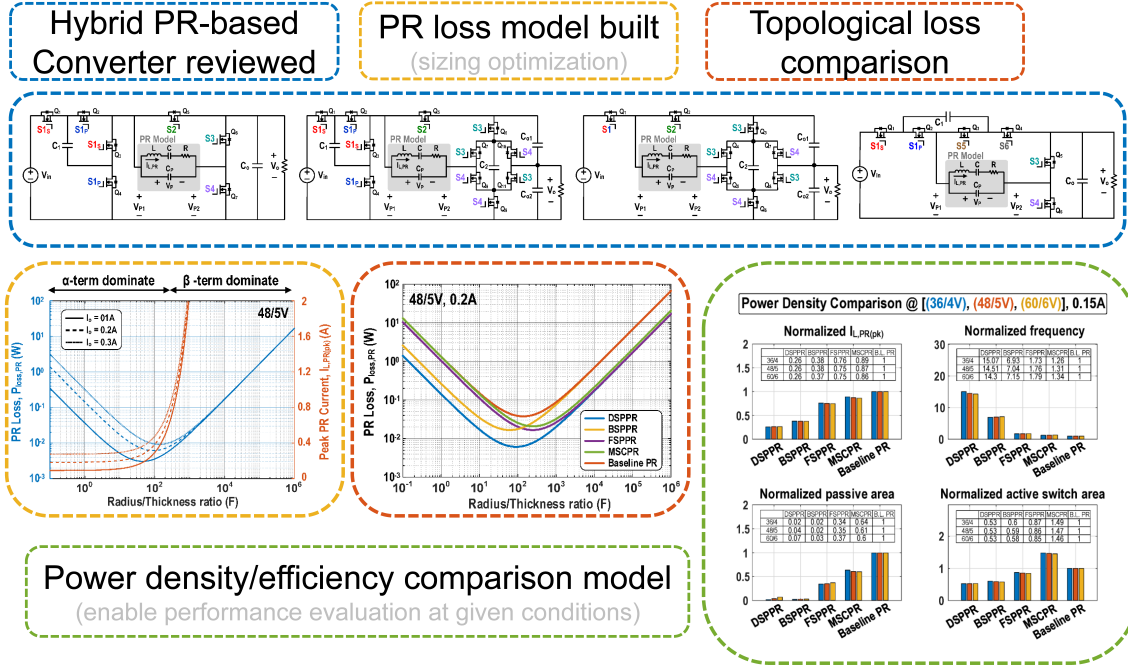


Figure 7.5 Summary of Chapter 5: Review and Comparison of Low-Voltage-Output High-Step-Down-Ratio Hybrid Switched-Capacitor Piezoelectric-Resonator-based DC-DC Converters

Chapter 6 introduces a control strategy for hybrid PR-based converters, featuring the first fully closed-loop control for hybrid PR-based converters. The operation principle is carefully examined leading to the specific control timing and driving strategy. By investigating the out-of-phase waveforms of PR, a state-machine-based PLL control is proposed. In addition, the regulation and loss minimization loops are enabled to achieve ideal operation with regulation. Moreover, the frontside switched capacitor balancing loop is introduced to stabilize the capacitor voltage without voltage drifting. A prototype is built with a disk-shaped PIC 181 PR in dimensions of (20/0.2)mm in radius and thickness, and the closed-loop control is realized by a digital controller. The measurement results validate the proposed control strategy and demonstrate the regulation ability. A summary is illustrated in Figure 7.6.

- 2) Other COT-based control scheme: The COT-based control scheme can be further explored to achieve better stability and transient response. Instead of utilizing the capacitor, other sensing, feedback, and feedforward methods can be further investigated so that simple sensing structures could be built, while achieving a better performance.
- 3) Behavior Modeling of piezoelectric resonators at power applications: While the Butterworth-Van Dyke (BVD) model accurately represents the impedance response measured by a vector network analyzer (VNA), it falls short in scenarios involving power converters, where the power level move from micro/milliwatts range in VNA to tens-watts or sometimes hundreds-watts for power application. On the other hand, experiments have indicated a decline in the mechanical quality factor (Q_m) at higher power levels [70], [80], [82]. As a result, some of the papers reported efficiency degradation in PR-based converters at higher output powers/currents [30], [52], [70], [77], [82], for which the BVD model does not account. Though the spurious modes and out-of-band harmonic hypotheses are plausible [30], [52], and the modified BVD model [73] might be able to model the harmonic loss, which is adopted in [32], the degradation of Q_m is still unresolved, and there is no accurate model for power applications presented yet. Hence, there is a pressing need for an accurate PR behavioral model, specifically for power applications.
- 4) Switched Capacitor hybridization for different PR-based converters: this study extensively explores the baseline PR-based converter [29], Several types of PR-based converters and operation sequences [28], [29], [53], [66], [69], [74], which could benefit from the hybridization, remain unexplored. Therefore, future research could conduct a comprehensive comparison and analysis for these PR-based DC-DC converter.

- 5) Reconfigurable PR-based converters: Several hybrid PR-based converters are proposed; however, as a high order SC network is merged, the operable range narrowed. Thus, to extend the operation range while optimal overall efficiency, a reconfigurable structure can be employed. In this configuration, how to seamless transition between each mode requires additional analysis and control algorithm.
- 6) Operable range extension for PR-based converters: This work specifically focuses on PR operation sequence of $(V_{in,PR} - V_{o,PR}, ZERO+, V_{o,PR})$, which limits the operable VCR to $(0 \leq VCR \leq 0.5)$, $((0 \leq VCR \leq 0.25))$, and $((0 \leq VCR \leq 0.125))$ for the baseline PR-based, F/BSPPR, and DSPPR converters respectively. However, if another sequence $(V_{in,PR} - V_{o,PR}, ZERO-, V_{o,PR})$ is incorporated into the modulation, the operable VCR can be extended to $(0 \leq VCR \leq 1)$, $((0 \leq VCR \leq 0.5))$, and $((0 \leq VCR \leq 0.25))$ for the baseline PR-based, F/BSPPR, and DSPPR converters respectively. Combining future work 5, the overall efficiency can be optimized form 0 VCR to 1 VCR $(0 \leq VCR \leq 1)$.
- 7) Closed-loop performance optimization for PR-based converters: although this study proposed a closed-loop control method for PR-based converters; however, the transient response is not desirable. The future direction could be system level optimization that enhances the transient response.

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