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ABSTRACT

A π-μ decay counter has been designed and used to count positive pions in several synchrotron and cyclotron experiments. Utilizing an improved gate generator and coincidence circuit, the detector possesses a very stable efficiency for counting pions in several energy intervals. The detector is readily adaptable to the addition of extra counters to permit the detection of pions in the presence of large backgrounds.

A STABLE MULTICHANNEL POSITIVE PION DETECTOR[*]

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I. INTRODUCTION

The detection of positive pions on the basis of their π-μ decay, first demonstrated by Jakobson, Schulz, and Steinberger,[1] offers several advantages over other counting methods. Considerably larger backgrounds can be tolerated than with detection by the much slower μ-e decay, first demonstrated for artificially produced pions by Alvarez et al.[2] Although in the latter case the background can be greatly reduced by employing a pulsed beam and counting the μ-e decays only when the beam is off,[3] such a technique is not feasible on many accelerators. Since a π-μ detector telescope can generally be made quite compact, considerably more versatility in the angle of detection and solid angle are possible than with magnetic spectrometers employed to count pions.[4]

Counters requiring a π-μ decay for identification of a pion have not been used very extensively to date. Since the mean life of a pion is 2.54×10^{-8} second,[1] a major obstacle to the satisfactory operation of the counters has been the need to develop suitable fast electronics for counting the π-μ decays in coincidence with delayed electronic gates. In order to have stability in the counting rate, it is important that the gates themselves be stable and have sufficiently fast rise times to result in a plateau for the π-μ decay counting rate as a function of amplitude of the 4.1-Mev μ pulses. These requirements are satisfied by the circuits described below, and the result is a very stable pion detector with considerable versatility.

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II. BASIC CIRCUIT DESCRIPTION

The basic counter arrangement used with the π-μ electronics is shown in Fig. 1. The signals from each counter, which usually consists of a photomultiplier and fast scintillator, are amplified by a wide-band amplifier, such as the Hewlett-Packard distributed amplifier type 460A, before they enter a fast coincidence circuit. Whenever a charged particle passes through the front two scintillators with sufficient energy loss that it could be a pion of the proper energy, a coincidence is made which triggers a gate generator. Often the discrimination level of this coincidence circuit may be set high enough to avoid responding to a large fraction of any background radiation present.

The gate pulse generated by the gate former described below is sent to two different coincidence circuits, as shown in the block diagram. To the other input of each of these coincidence circuits are sent signals from the third counter, in which pions of a certain incident energy come to rest and then undergo a π-μ decay. In order that the output of the first of these coincidence circuits be a measure of the number of π-μ decays in this counter, the delay of the gate input is made long enough so that no coincidences are made by particles passing through all three scintillators, but no longer than necessary so that as many π-μ decays are counted as possible. In practice, a delay of about 2.5×10^{-8} second is found to be optimum. In order to have the output of the second coincidence circuit proportional to what is essentially just the number of accidentals, the gate delay should be longer by several pion mean lives. In view of this, a delay of $\approx 12 \times 10^{-8}$ second has been used. Then when the discrimination levels of the two coincidence circuits are balanced exactly, their difference in counting rate is proportional to the number of π-μ decays, and hence to the number of incident pions in a certain energy interval.

III. DETAILED ELECTRONICS

A. Gate Generator

In conventional gate-pulse-generating circuits, the rise and fall times of the gates, minimum time duration, maximum repetition rate, maximum duty cycle, and maximum power capabilities are seriously restricted by such inherent vacuum tube properties as input capacitance, electron transit time, and peak power rating. These limitations are considerably overcome in the gate generator shown in Fig. 2, which employs the Philips EFP60 secondary emission vacuum tubes.[5]

The first EFP60, designated V_1, is used as a single-stage amplifier with a small amount of positive feedback from the dynode to the cathode through the cathode inductance. This results in an output pulse with an improved rise time which then serves as a good trigger pulse for the gate-former tube V_4. This EFP60 has a negative 5-volt bias on its control grid and is completely nonconducting. A positive pulse from V_1 of sufficient amplitude (≈ 4 volt) causes the dynode and plate currents to become large enough so that the positive feedback loop from the dynode to the grid takes over and drives the grid to a positive potential until the tube saturates due to space-charge limitations at the dynode. The dynode load impedance which determines the gain of the feedback loop consists of the series-parallel combination of Diode 1 with R_4, R_8 and R_9, in parallel with the 200 ohm impedance of a shorted delay line connected to the grid. Thus the total load impedance at the dynode is 100 ohms, which is adequate for the feedback loop. The length of the output gate is determined completely, then, by the length of the shorted delay line. Spurious oscillations in the feedback loop are prevented by the unidirectional clamping action of a 1N36 crystal diode whose anode is grounded and whose cathode is coupled to the dynode by means of capacitor C_9.

Placement of the delay line at the grid, instead of at the anode, reduces the dead time of the circuit between successive gates to less than 2×10^{-7} sec.

Gate pulses having rise times of the order of 6 to 8×10^{-9} second, depending on the shape of the input pulse, and lengths that may be varied from 1.5×10^{-8} to 20×10^{-8} second are derived at the plate of the EFP60. In a typical experiment the gate duration was selected to about 6×10^{-8} second, by use of a 24-ft shorted piece of 200 ohm cable, to optimize the π-μ counting rate without causing an excessive accidental rate which is, of course, proportional to the duration of the gate. It is desirable to have the gate length a multiple of the accelerator rf period so that the average beam intensity is the same during both the prompt and delayed gates irrespective of their relative delay, which as an added precaution should also be a multiple of the rf period. Since these adjustments merely involve changes in length of certain delay cables, the values can be optimised experimentally. Because of the high peak-current emission of the EFP60, the gate amplitudes can be made equal to about 5 volts for an output load consisting of several 125-ohm cables in parallel. A third EFP60, V_6, provides a gate monitor signal of sufficient amplitude to drive a scaler directly with no need for an additional amplifier.

[illegible] Coincidence Circuits

The coincidence circuits, shown in Fig. 3, are similar to the crystal diode coincidence circuit described by Madey, Bandtel, and Frank.[6] In this case, the output pulses from the crystal diode coincidence circuit are amplified by the pentode section of V_1 and then trigger the biased grid of a blocking oscillator. The output pulse from the blocking oscillator has sufficient amplitude to drive a scaler by the cathode follower V_7.

The coincidence circuits display optimum operation for input signals of the order to 2 to 5 volts, for which the singles-to-doubles ratio is about 12 to 1. Such an amplitude is chosen for the input 4.1-Mev pulses by proper adjustment of amplifier gain and photomultiplier voltage; the input gate signals are about 5 volts. Owing to the limiting action of the Hewlett-Packard wide-band amplifiers and to the constant amplitude of the gate pulses, singles are never able to feed through under normal running conditions.

The discrimination level is varied by adjusting the input grid bias of the blocking oscillator by the helipot R_{14}, as shown in Fig. 3. With this adjustment, the discrimination levels of the two coincidence circuits for each counter are equated under normal running conditions by using a 100-kc pulser to generate gate pulses that occur at random times relative to the beam, and hence yield only accidental counts in both coincidence circuits.

IV. PERFORMANCE

The π-μ electronic circuits described here have already been used for several pion-production experiments at the Berkeley synchrotron[7] and 184-inch cyclotron,[8] and have displayed highly satisfactory performance even in the presence of very large electron and gamma backgrounds. Many checks on the validity of detection have been performed, of which the pion mean-life measurement is one of the most significant. A typical mean-life curve is shown in Fig. 4(a).

The stability of the counting efficiency has been of great concern, particularly in experiments requiring many weeks of running time. An indication of this stability is obtained from the shape of the μ-counter voltage plateau shown in Fig. 4(b). During such long runs, the over-all pion-counting efficiency and the relative accidental counting rates of the crystal diode coincidence circuits have been generally observed to remain constant within about 5%.

V. MODIFICATIONS

In Section II the basic π-μ counter arrangement was described. No other detectors or electronics are necessary for a positive identification of pions, but often an excessive background requires the presence of additional counters to reduce the accidental counting rate. Furthermore, the running time required for many experiments can be greatly decreased by the simultaneous use of several scintillators in which π-μ decays are observed. An example of the manner in which additional counters have been used for such purposes is shown in Fig. 5 which was used in a synchrotron experiment in which the electron background was excessive. To decrease the accidental counting rate, extra care was taken to reduce the number of gates generated by particles other than pions. Consequently, the gate generator was triggered only when pulses in Counters 1 and 3 were in coincidence with each other and in anticoincidence with pulses in Counters 2 and 6. This requirement assured (a) that the incident particle did not give a pulse in a Cherenkov radiator, Counter 2, which was insensitive to pions in the energy band selected by the telescope, and (b) that the particle did not have sufficient range to enter Counter 6. Counters 4 and 5, in which the μ pulse is observed, are separated by appropriate amounts of copper absorber and define two energy bands of incident pions. Such use of extra counters and a coincidence-anticoincidence unit[9] is an example of the general way in which the accidental rate may be reduced by proper discrimination against the generation of gates by particles other than pions.

The accidental rate may also be decreased by shortening the gate length at some sacrifice of counting efficiency. Further reduction may be obtained by counting coincidences only when the output pulses from the π-μ counter fall in a certain amplitude interval corresponding to 4.1-Mev μ pulses. Such a single-channel pulse-height analysis is a great improvement over use of a mere threshold discrimination level, as in the fundamental π-μ circuit.

It should be emphasized that these counter and electronic arrangements are only examples of the general way in which the gate-forming and multichannel coincidence circuits described here have been used. Even with several anticoincidence counters and energy bands of pion detection, the entire π-μ electronics occupies a relatively small space and requires little maintenance.

VI. ACKNOWLEDGMENTS

We are indebted to Professor A. C. Helmholz for suggesting several pion experiments for which this detector was originally designed. We wish to thank Mr. Edward Knapp for his contribution to the later phases of the development work. Finally, sincere thanks go to the UCRL Electronics Production Group for constructing all the electronic equipment.

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Figure Captions

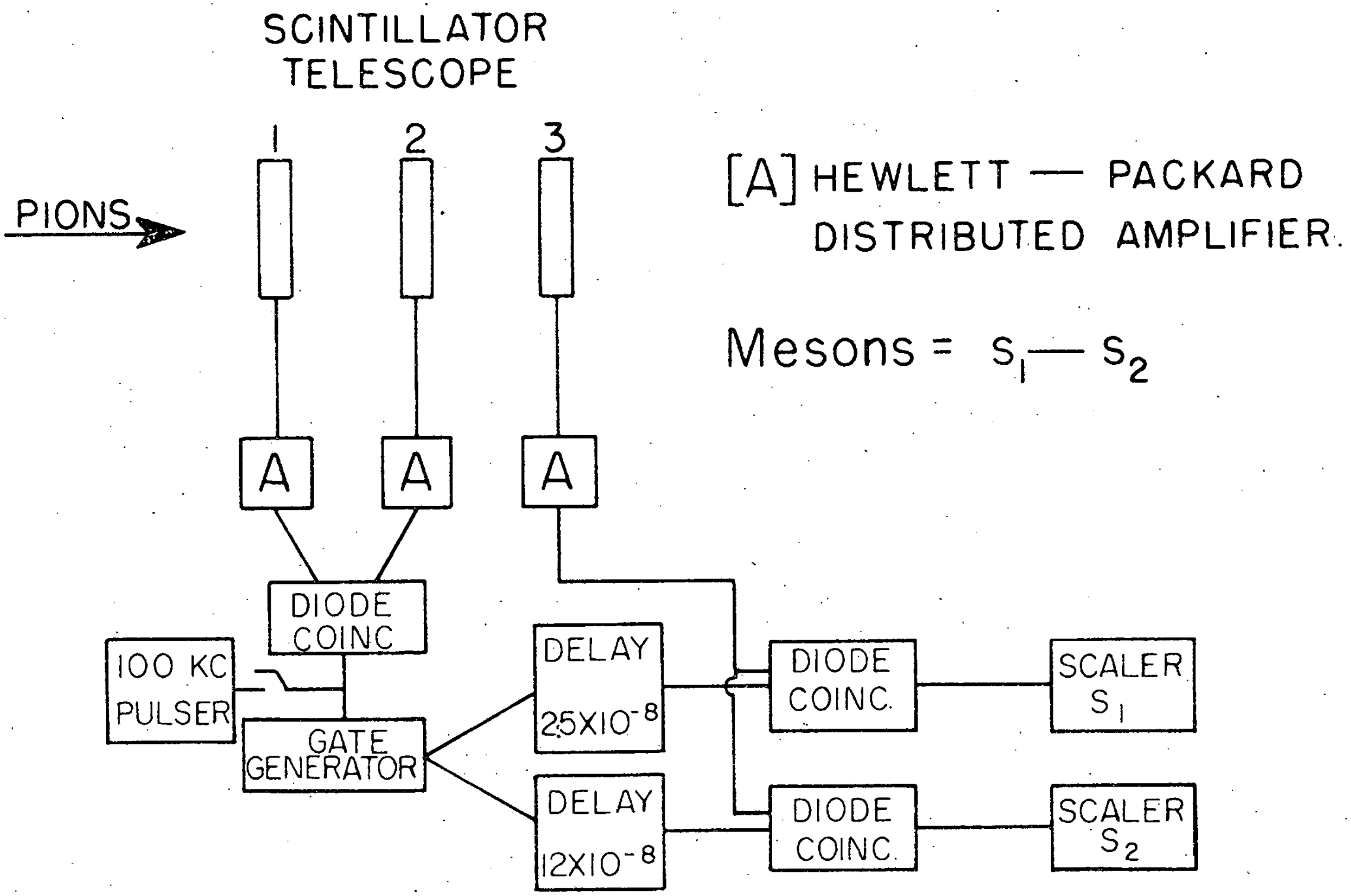
Fig. 1. Block diagram of basic π-μ counter detector.

Fig. 2. Circuit diagram of electronic gate generator.

Fig. 3. Circuit diagram of crystal diode coincidence circuit. Six units of this type are assembled on the same chassis.

Fig. 4. Typical measurement of (a) pion mean life and (b) voltage plateau taken with a plastic scintillator viewed by an RCA 6199 photomultiplier.

Fig. 5. Block diagram of pion-counting telescope with high background discrimination, for detecting pions in two energy intervals.


SCINTILLATOR
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2
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Mesons = $S_1 - S_2$
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SCALER S_1
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Fig 1

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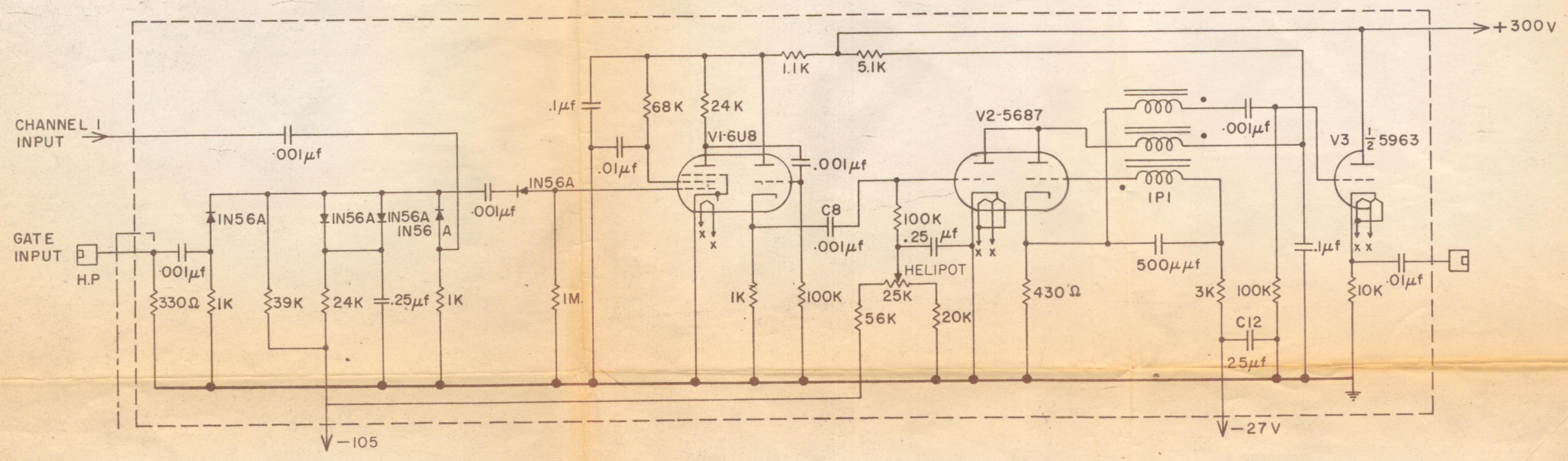

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Fig 3.

Fig. 3

Fig. 3

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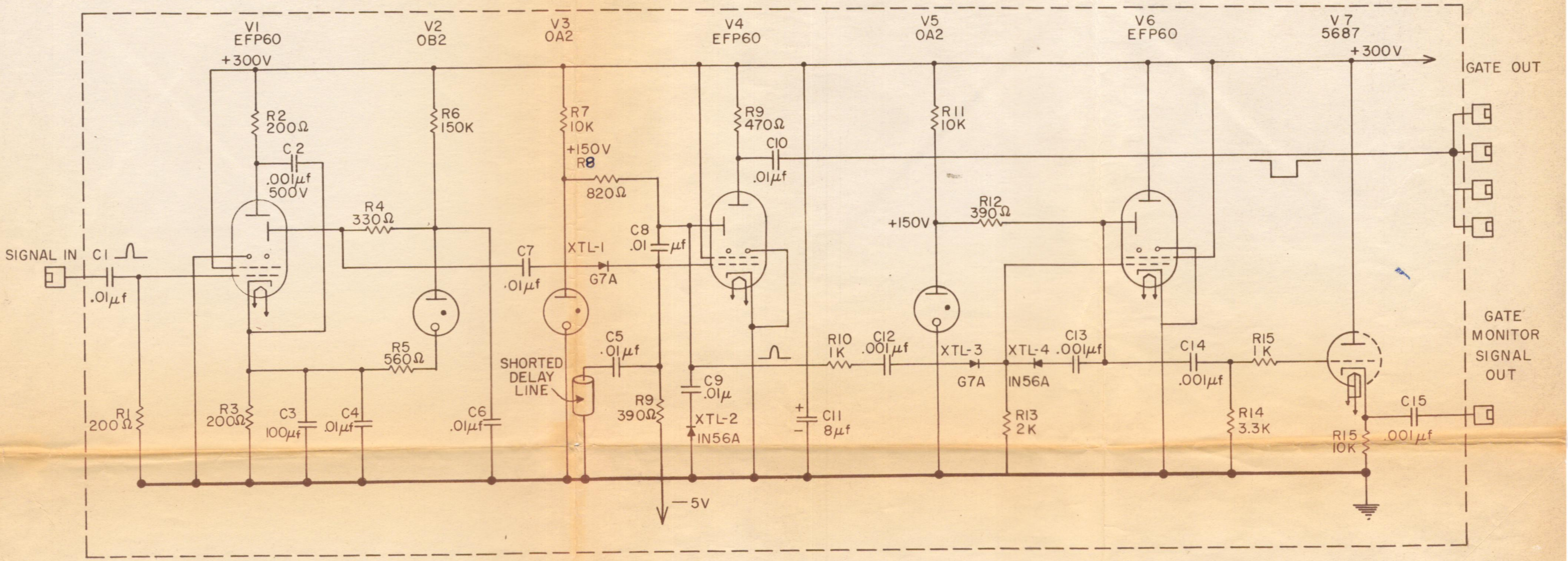

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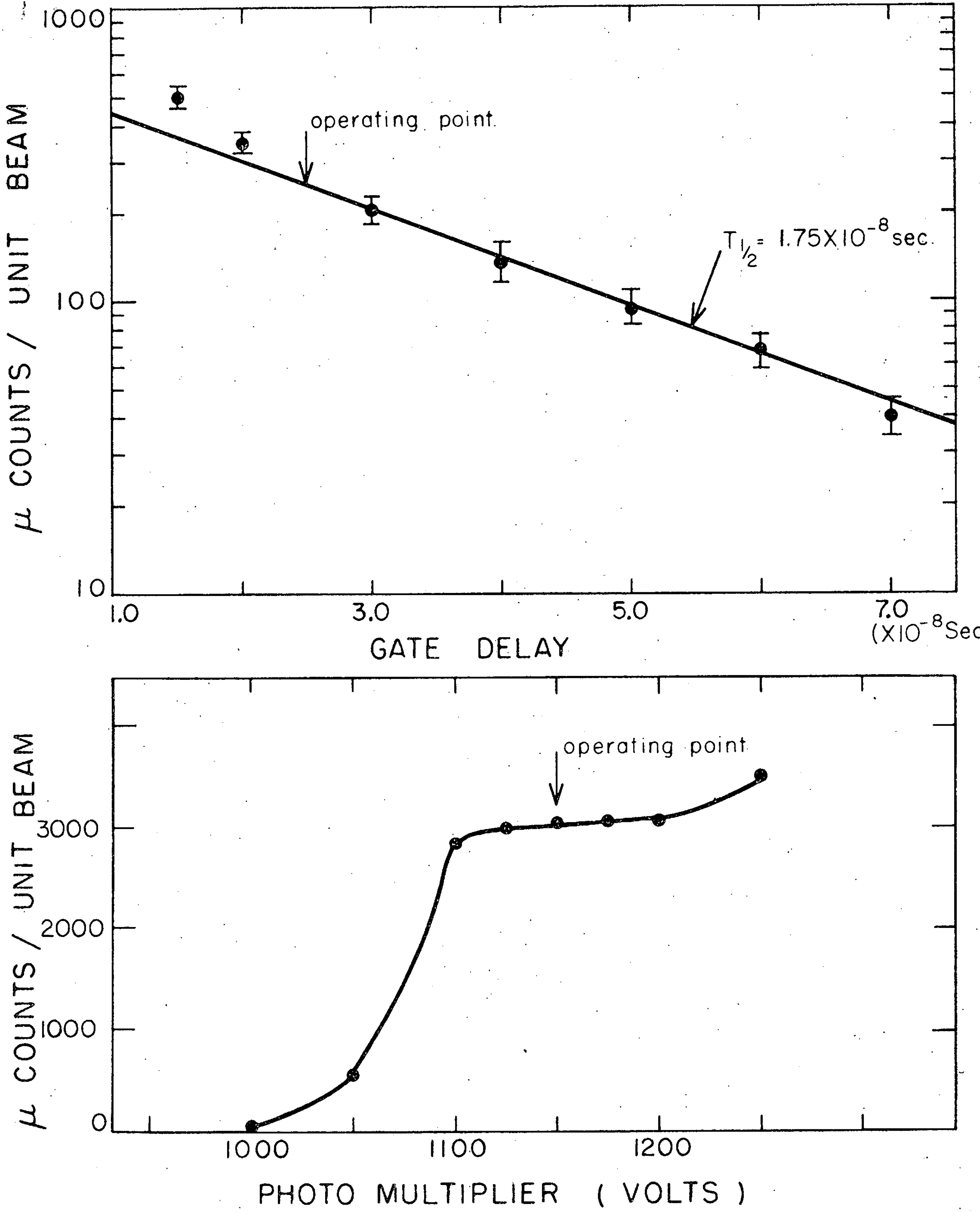
Fig 2

Fig 2



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μ COUNTS / UNIT BEAM
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$T_{1/2} = 1.75 \times 10^{-8}$ sec.
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7.0
$(\times 10^{-8}$ Sec
GATE DELAY
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PHOTO MULTIPLIER (VOLTS)

Fig 4

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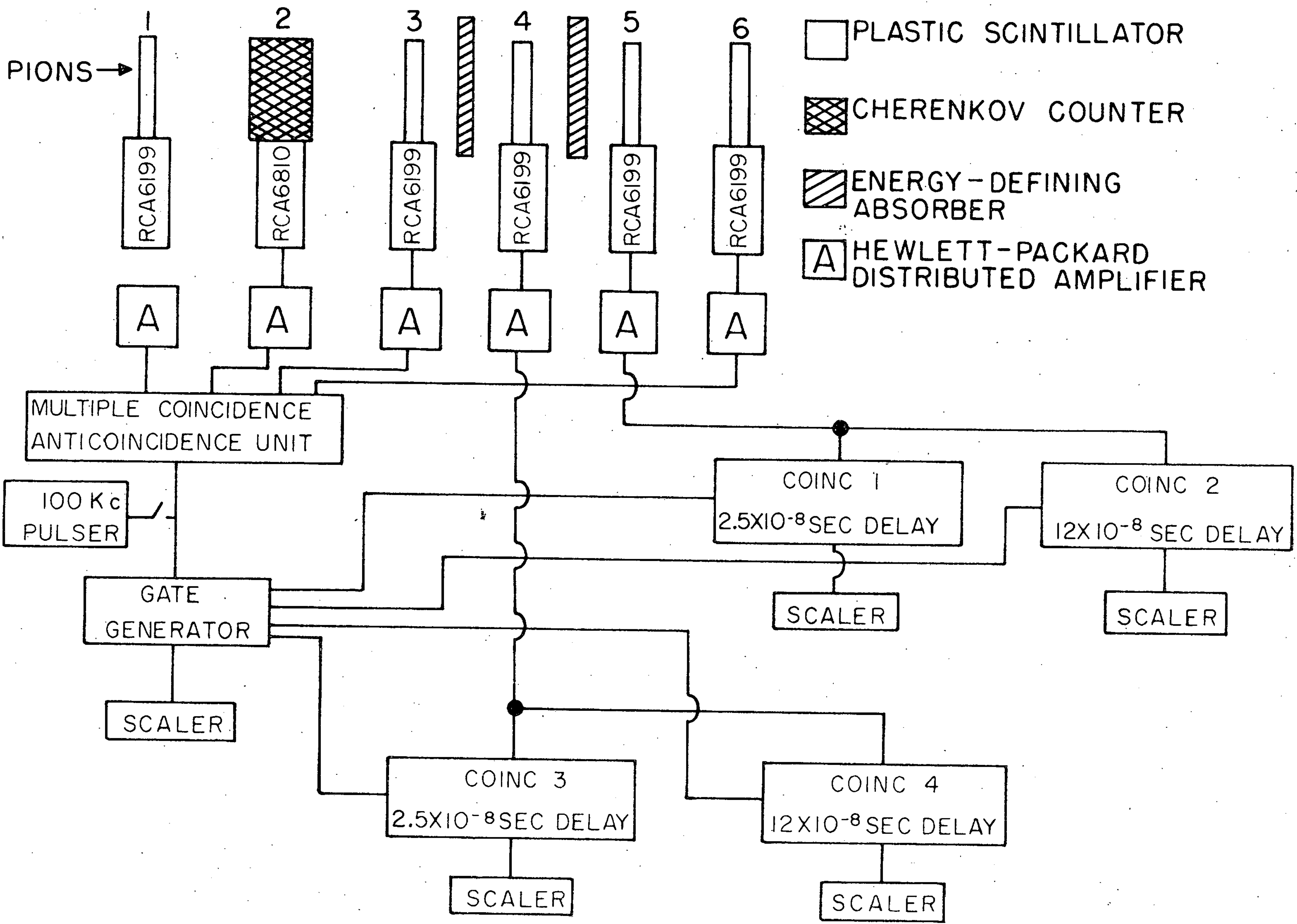
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PLASTIC SCINTILLATOR
CHERENKOV COUNTER
ENERGY-DEFINING ABSORBER
A HEWLETT-PACKARD DISTRIBUTED AMPLIFIER
MULTIPLE COINCIDENCE ANTICOINCIDENCE UNIT
100 Kc PULSER
GATE GENERATOR
SCALER
COINC 1 2.5X10^-8 SEC DELAY
COINC 2 12X10^-8 SEC DELAY
COINC 3 2.5X10^-8 SEC DELAY
COINC 4 12X10^-8 SEC DELAY
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Fig 5

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